

Fast and Memory-Efficient Exact Attention with IO-Awareness

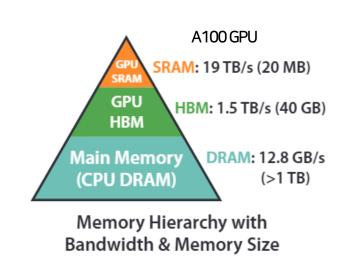
NeurIPS 2022 HUMANE Lab 김태균 2025.03.14



Introduction

- Sparse attention focuses on FLOP reduction but tends to ignore overheads from memory access (IO), resulting in lower wall-clock speed
- An IO-aware attention algorithm is needed to address this issue

=> Therefore, the goal is to reduce HBM access



How to reduce HBM access?

- 1. Computing the softmax reduction
- 2. Not storing the large intermediate attention matrix for the backward pass

How to reduce HBM access?

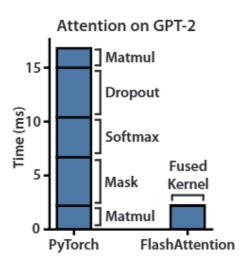
- 1. Computing the softmax reduction => Tiling
- Not storing the large intermediate attention matrix for the backward pass => Recomputation

Background

- Operations
 - compute-bound
 - memory-bound

=> arithmetic intensity $(\frac{FLOPs}{Byte})$

Kernel fusion



FlashAttention

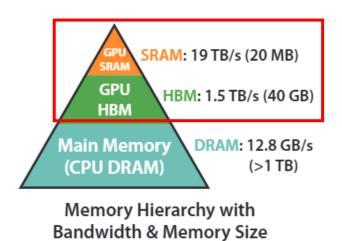
- Goal: avoid r/w the attention matrix to and from HBM
 - Tiling
 - Recomputation

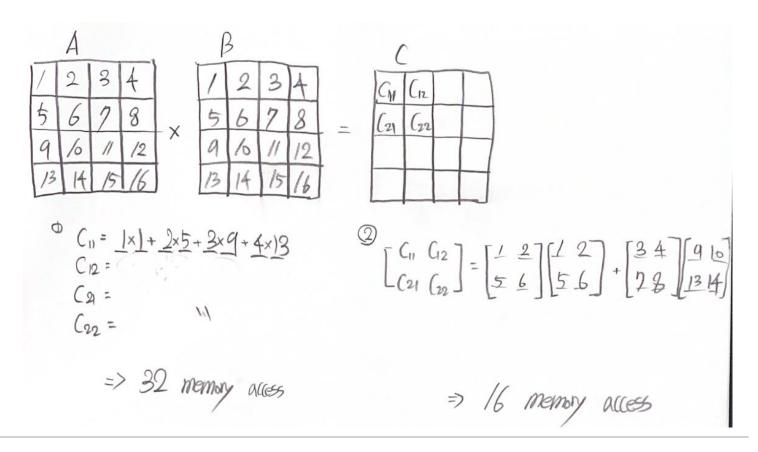
$$S = QK^{T}$$

$$P = softmax(S)$$

$$O = PV$$

- A technique that divides the entire matrix into blocks for computation
 - memory hierarchy
 - matrix multiplication





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- Safe softmax
 - subtract the maximum value to scale down
 - for numerical stability (to prevent overflow)

$$y_i = \frac{e^{x_i}}{V}$$

$$\sum_{j=1}^{V} e^{x_j}$$

$$j=1$$
Algorithm 1 Naive so 1: $d_0 \leftarrow 0$
2: for $j \leftarrow 1, V$ do 3: $d_j \leftarrow d_{j-1} + d_j \leftarrow d_j$
4: end for

Algorithm 1 Naive softmax

1:
$$d_0 \leftarrow 0$$

2: for
$$j \leftarrow 1, V$$
 do

3:
$$d_j \leftarrow d_{j-1} + e^{x_j}$$

4: end for

5: for
$$i \leftarrow 1, V$$
 do

6:
$$y_i \leftarrow \frac{e^{x_i}}{d_V}$$

7: end for

memory access: 3V

$$y_{i} = \frac{e^{x_{i} - \max_{k=1}^{V} x_{k}}}{\sum_{j=1}^{V} e^{x_{j} - \max_{k=1}^{V} x_{k}}}$$

Algorithm 2 Safe softmax

1:
$$m_0 \leftarrow -\infty$$

2: for
$$k \leftarrow 1, V$$
 do

3:
$$m_k \leftarrow \max(m_{k-1}, x_k)$$

5:
$$d_0 \leftarrow 0$$

6: for
$$j \leftarrow 1, V$$
 do

7:
$$d_j \leftarrow d_{j-1} + e^{x_j - m_V}$$

8: end for

9: **for**
$$i \leftarrow 1, V$$
 do

10:
$$y_i \leftarrow \frac{e^{x_i - m_V}}{dx}$$

11: **end for**

memory access: 4V

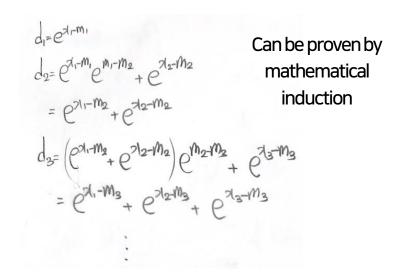
Online normalizer calculation for softmax, arXiv preprint 2018

- Online safe softmax
 - compute m online
 - reduce the number of memory accesses by one

Algorithm 3 Safe softmax with online normalizer calculation

```
1: m_0 \leftarrow -\infty
 2: d_0 \leftarrow 0
3: for j \leftarrow 1, V do
4: m_j \leftarrow \max(m_{j-1}, x_j)
5: d_j \leftarrow d_{j-1} \times e^{m_{j-1} - m_j} + e^{x_j - m_j}
 6: end for
7: for i \leftarrow 1, V do
          y_i \leftarrow \frac{e^{x_i - m_V}}{dv}
9: end for
```

memory access: 3V



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3: for j \leftarrow 1, V do

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5: d_j \leftarrow d_{j-1} \times e^{m_{j-1} - m_j} + e^{x_j - m_j}

6: end for

7: for i \leftarrow 1, V do
```

Attention	Standard	FLASHATTENTION
GFLOPs	66.6	75.2
HBM R/W (GB)	40.3	4.4
Runtime (ms)	41.7	7.3

memory access: 3V

9: end for

Online normalizer calculation for softmax, arXiv preprint 2018

- Online safe softmax
 - compute m online
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$$S = QK^{T}$$

$$P = softmax(S)$$

$$O = PV$$

$$\int_{0}^{\infty} \int_{0}^{\infty} \int_{0}^{\infty} dx = g K_{i}^{T}$$

$$M_{i} = Max (M_{i+1}, \chi_{i})$$

$$d'_{i} = d'_{i+1} e^{M_{i+1} - M_{i}} + e^{\chi_{i} - M_{i}}$$

$$\int_{0}^{\infty} \int_{0}^{\infty} dx = e^{\chi_{i} - M_{i}} \int_{0}^{\infty} dx = e^{\chi_{i} - M_{i}}$$

$$O_{i} = O_{i+1} + O_{i}V_{i}$$

return ON

where N is the number of blocks

return On

$$\int_{0}^{\infty} \mathbf{1} \leq \mathbf{i} \leq \mathbf{i}$$

$$\chi_{i} = \mathbf{i} \leq \mathbf{i$$

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For
$$1 \leq i \leq N$$

$$\chi_{i} = Q K_{i}^{T}$$

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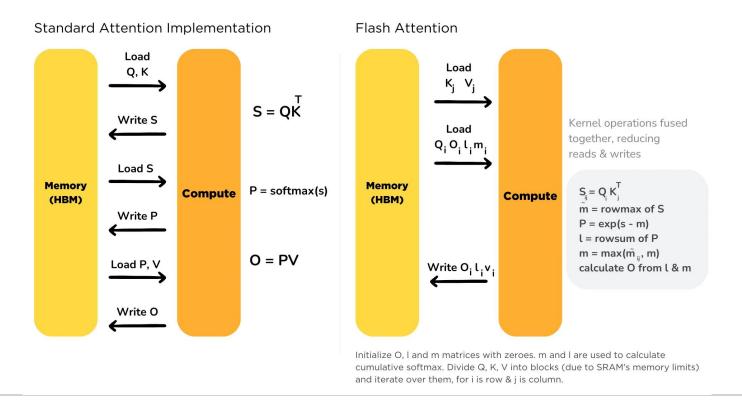
$$\chi_{i} = Max (M_{i+1}, \chi_{i})$$

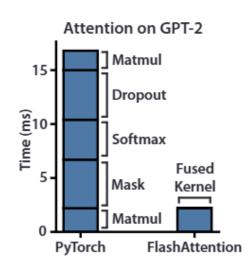
$$\chi_{i} = \chi_{i+1} Max (M_{i+1}, \chi_{i})$$

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Recomputation

 A technique of recompute intermediate values (S, P) during the backward pass instead of storing them





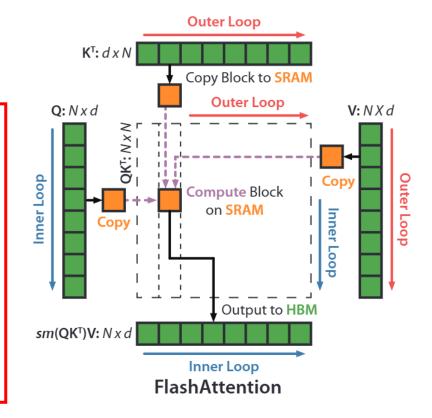
Algorithm

Algorithm 1 FLASHATTENTION

Require: Matrices $\mathbf{Q}, \mathbf{K}, \mathbf{V} \in \mathbb{R}^{N \times d}$ in HBM, on-chip SRAM of size M.

- 1: Set block sizes $B_c = \left\lceil \frac{M}{4d} \right\rceil, B_r = \min\left(\left\lceil \frac{M}{4d} \right\rceil, d\right)$.
- 2: Initialize $\mathbf{O} = (0)_{N \times d} \in \mathbb{R}^{N \times d}, \ell = (0)_N \in \mathbb{R}^N, m = (-\infty)_N \in \mathbb{R}^N$ in HBM.
- 3: Divide **Q** into $T_r = \left\lceil \frac{N}{B_r} \right\rceil$ blocks $\mathbf{Q}_1, ..., \mathbf{Q}_{T_r}$ of size $B_r \times d$ each, and divide \mathbf{K}, \mathbf{V} in to $T_c = \left\lceil \frac{N}{B_c} \right\rceil$ blocks $\mathbf{K}_1, ..., \mathbf{K}_{T_c}$ and $\mathbf{V}_1, ..., \mathbf{V}_{T_c}$, of size $B_c \times d$ each.
- 4: Divide **O** into T_r blocks $O_i,...,O_{T_r}$ of size $B_r \times d$ each, divide ℓ into T_r blocks $\ell_i,...,\ell_{T_r}$ of size B_r each, divide m into T_r blocks $m_1,...,m_{T_r}$ of size B_r each.

```
5: for 1 \le i \le T_c do
             Load \mathbf{K}_i, \mathbf{V}_i from HBM to on-chip SRAM.
             for 1 \le i \le T_r do
                  Load \mathbf{Q}_i, \mathbf{O}_i, \ell_i, m_i from HBM to on-chip SRAM.
  8:
                  On chip, compute S_{ij} = Q_i K_i^T \in \mathbb{R}^{B_r \times B_c}.
  9:
                  On chip, compute \tilde{m}_{ij} = \text{rowmax}(\mathbf{S}_{ij}) \in \mathbb{R}^{B_r}, \tilde{\mathbf{P}}_{ij} = \exp(\mathbf{S}_{ij} - \tilde{m}_{ij}) \in \mathbb{R}^{B_r \times B_c} (pointwise),
10:
                  \tilde{\ell}_{i,i} = rowsum(\tilde{\mathbf{P}}_{i,i}) \in \mathbb{R}^{B_r}.
                  On chip, compute m_i^{\text{new}} = \max(m_i, \tilde{m}_{ij}) \in \mathbb{R}^{B_r}, \ell_i^{\text{new}} = e^{m_i - m_i^{\text{new}}} \ell_i + e^{\tilde{m}_{ij} - m_i^{\text{new}}} \tilde{\ell}_{ij} \in \mathbb{R}^{B_r}.
11:
                  Write \mathbf{O}_i \leftarrow \operatorname{diag}(\ell_i^{\text{new}})^{-1}(\operatorname{diag}(\ell_i)e^{m_i-m_i^{\text{new}}}\mathbf{O}_i + e^{\tilde{m}_{ij}-m_i^{\text{new}}}\tilde{\mathbf{P}}_{ij}\mathbf{V}_j) to HBM.
12:
                  Write \ell_i \leftarrow \ell_i^{\text{new}}, m_i \leftarrow m_i^{\text{new}} to HBM.
13:
14:
             end for
15: end for
```



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16: Return O.

Block-sparse FlashAttention

- Better IO complexity than FlashAttention by a factor proportional to the sparsity ratio
 - Given a predefined block sparsity mask M

$$\mathbf{S} = \mathbf{Q}\mathbf{K}^{\top} \in \mathbb{R}^{N \times N}, \quad \mathbf{P} = \operatorname{softmax}(\mathbf{S} \odot \mathbb{1}_{\tilde{\mathbf{M}}}) \in \mathbb{R}^{N \times N}, \quad \mathbf{O} = \mathbf{P}\mathbf{V} \in \mathbb{R}^{N \times d}$$

Experiments

Training time & model accuracy

Model implementations	OpenWebText (ppl)	Training time (speedup)
GPT-2 small - Huggingface [87]	18.2	9.5 days (1.0×)
GPT-2 small - Megatron-LM $[77]$	18.2	$4.7 \text{ days } (2.0\times)$
GPT-2 small - FlashAttention	18.2	$2.7 \text{ days } (3.5 \times)$
GPT-2 medium - Huggingface [87]	14.2	$21.0 \text{ days } (1.0\times)$
GPT-2 medium - Megatron-LM [77]	14.3	$11.5 \text{ days } (1.8 \times)$
GPT-2 medium - FlashAttention	14.3	6.9 days $(3.0\times)$

Model implementations	Context length	OpenWebText (ppl)	Training time (speedup)
GPT-2 small - Megatron-LM	1k	18.2	4.7 days (1.0×)
GPT-2 small - FlashAttention	1k	18.2	$2.7 ext{ days } (1.7 \times)$
GPT-2 small - FlashAttention	2k	17.6	$3.0 \text{ days } (1.6\times)$
GPT-2 small - FlashAttention	4k	17.5	$3.6 \text{ days } (1.3\times)$

Experiments

Attention runtime & memory benchmarks

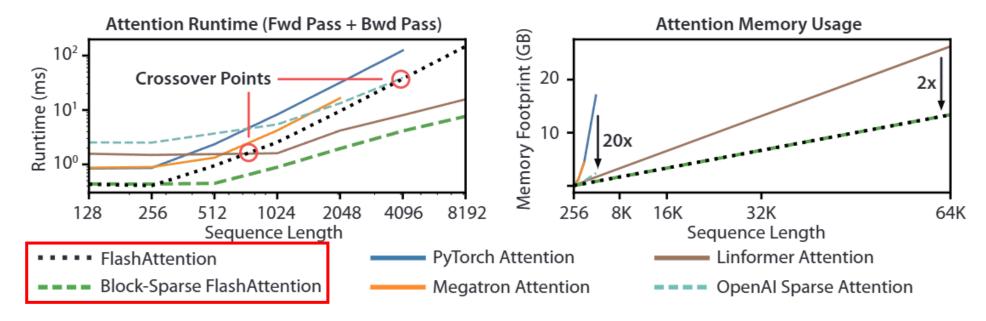


Figure 3: **Left:** runtime of forward pass + backward pass. **Right:** attention memory usage.

Conclusion

Showing significant reduction in HBM accesses compared to standard attention