Complex FFT Accelerator :CORE Generator Specification

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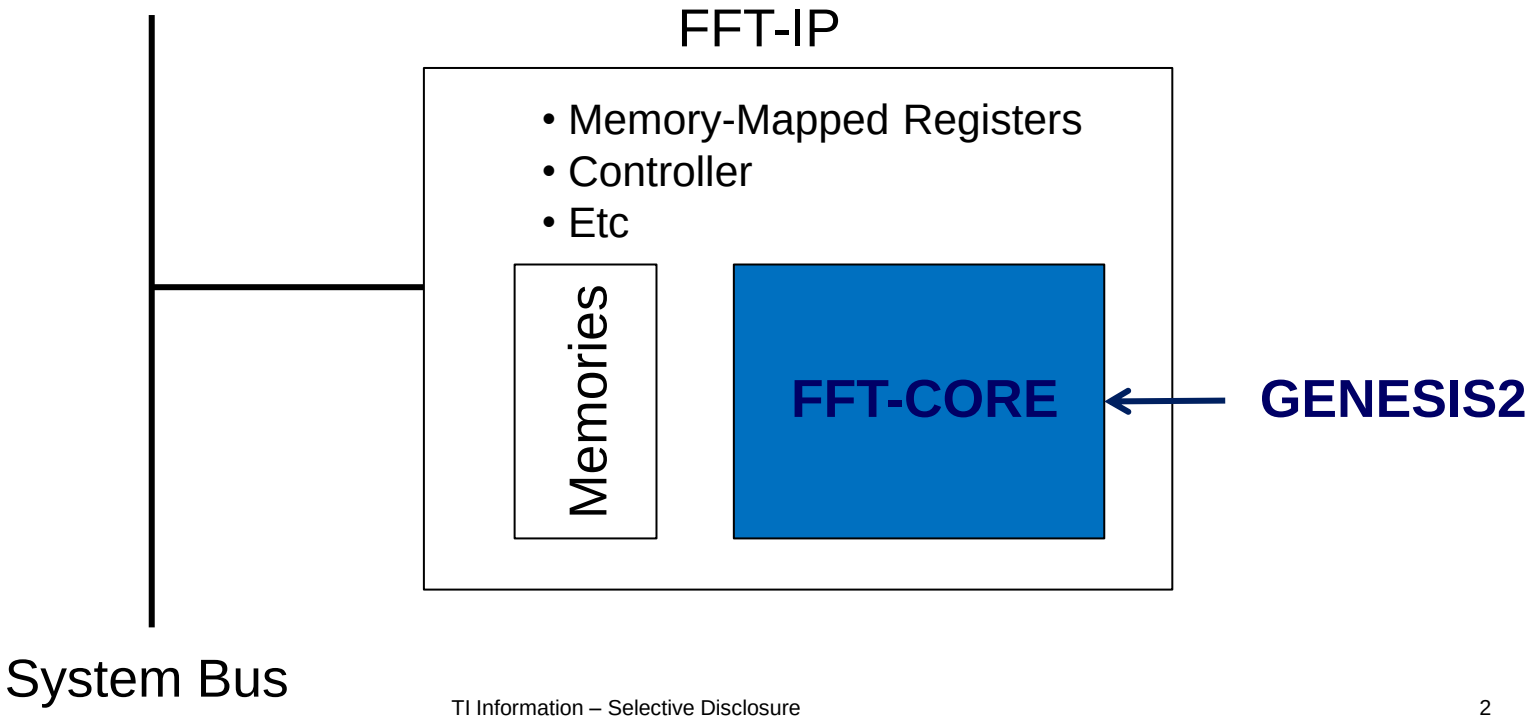
FFT-IP versus FFT-CORE

- FFT-IP is the module directly integrated with SoC/System Bus.
  - Built around FFT-CORE.



FFT-CORE Parameters

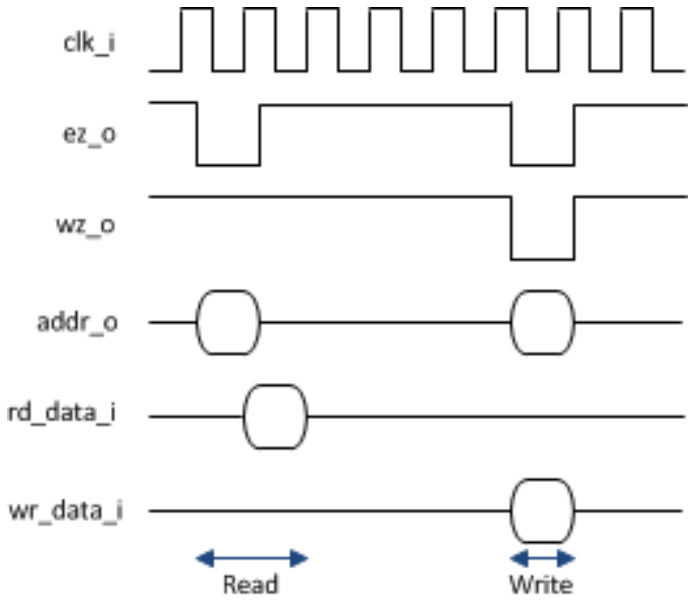
- Input: bit-reversed order, Output: linear order
- At each stage, a scaling should be applied to avoid overflow.
- GENESIS2 Compile-time parameter
  - FFT-Size = N = 2^n: 16,32, …, 8192
  - The number of Radix2 Butterfly operations per 1-clock cycle = R
  - The number of single port memories = 4*R
    - Each bank is N/(4*R)-word and each word stores one complex sample.
  - Fixed-point parameters of input sample, Twiddle factor, and output sample.
    - <I,F> format: I = # of integer bits, F = # of fractional bits.
- No Run-Time Parameter
- Example
  - N=256, R=1
  - 4 single port memories and each single port has 64-wordx32-bit.
  - Input sample: <1,15>
  - Twiddle: <1,15>
  - Output sample: <1,15>

FFT CORE: Input & Output Interfaces

- Inputs
  - clk_i: clock (all F/F is postive-edge)
  - rst_n_i: reset (‘0’: reset)
  - start_i (pulse signal: ‘1’ for 1-clock cycle)
- Outputs
  - busy_o (level signal: ‘1’ while accelerator is in computation).
- Memory Interface Signals
  - For each bank, there are 5 signals.
    - ez_o (memory select: ‘0’ is “selected”)
    - wz_o (write enable: ‘0’ is “enabled”)
    - addr_o[($\log_2$(N/(4R)))-1:0]
    - rd_data_i[2W-1:0]: W is the word-length for real or imag sample.
    - wr_data_o[2W-1:0]: W is the word-length for real or imag sample.
      - W: word-length for real or imaginary sample. If 16-bit is used, one complex number needs 32-bit, Data-In/Data-Out has 32-bit.
      - [2W-1:W]: Imaginary part, [W-1:0]: Real part.

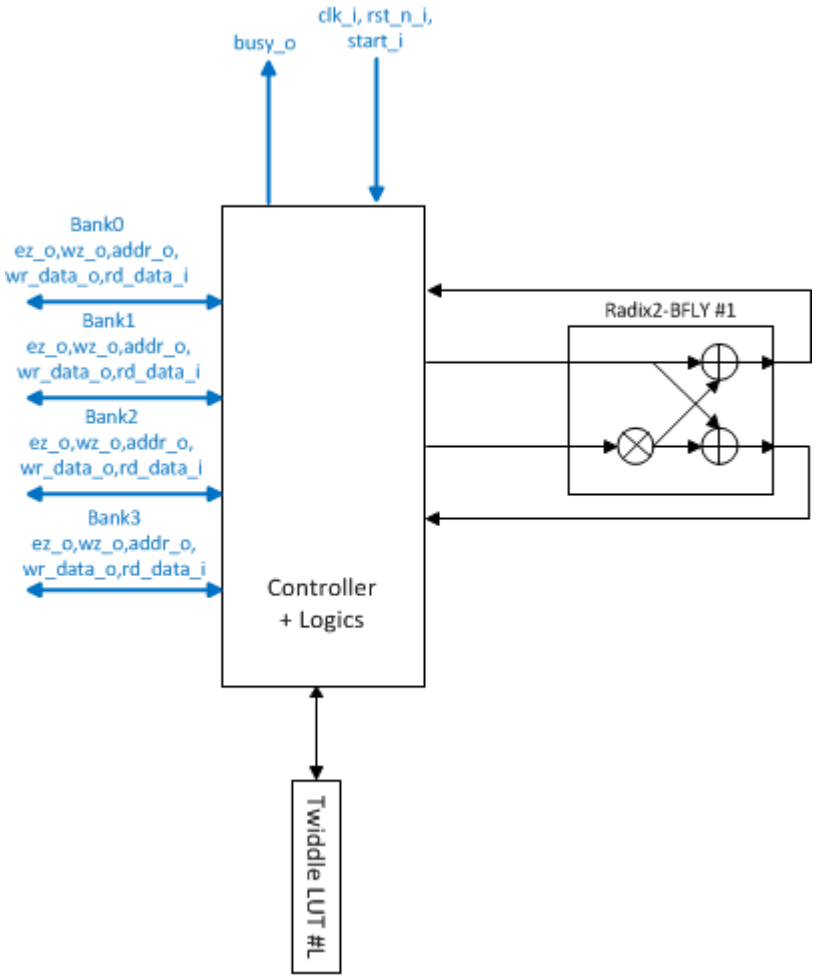
Single Port Memory Timing (example)

- ez_o, wr_o, addr_o, wr_data_o, rd_data_i



N=256, R=1 Example Block Diagram

- Single port memories is outside FFT CORE.
- Bank0: word[0] = The first input sample of N-size FFT.
- Bank3: word[63] = The last input sample of N-size FFT.



Input & Output Signal Timing

- FFT-CORE does not need to worry about data-in and date-out transfers.
  - It is FFT-IP's control machine responsibility.
- Hence, FFT-CORE can assume all input samples are prepared in bit-reverse order when start_i=1.