Complex FFT Accelerator :IP Generator Specification

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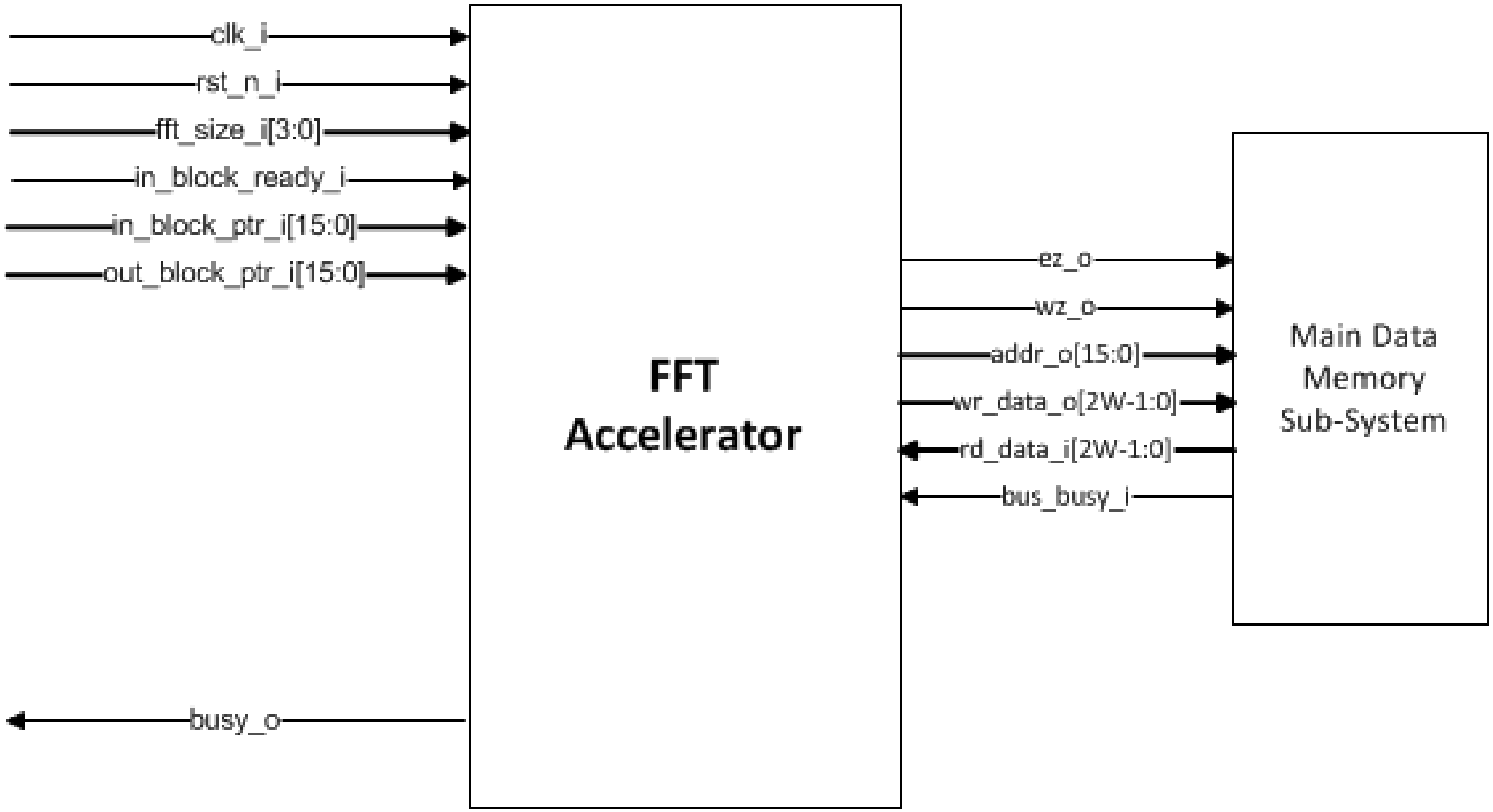
Input & Output Interfaces

- Inputs
  - clk_i: clock (all F/F is postive-edge)
  - rst_n_i: reset (‘0’: reset)
  - fft_size_i : 4-bit (Example: 1010: N=2^10=1024 point FFT).
  - in_block_ready_i (pulse signal: ‘1’ for 1-clock cycle)
  - in_block_ptr_i (16-bit input block pointer pointing to the first complex sample of input block)
  - out_block_ptr_i (16-bit output block pointer pointing to the first complex sample of output block)
- Outputs
  - busy_o (level signal: ‘1’ while accelerator is in computation).
- Memory Bus Master Signals
  - ez_o (memory select: ‘0’ is “selected”), wz_o (write enable: ‘0’ is “enabled”), addr_o[15:0], rd_data_i[2W-1:0], wr_data_o[2W-1:0], and bus_busy_i
    - W: word-length for real or imaginary sample. If 16-bit is used, one complex number needs 32-bit, Data-In/Data-Out has 32-bit.
    - [2W-1:W]: Imaginary part, [W-1:0]: Real part.

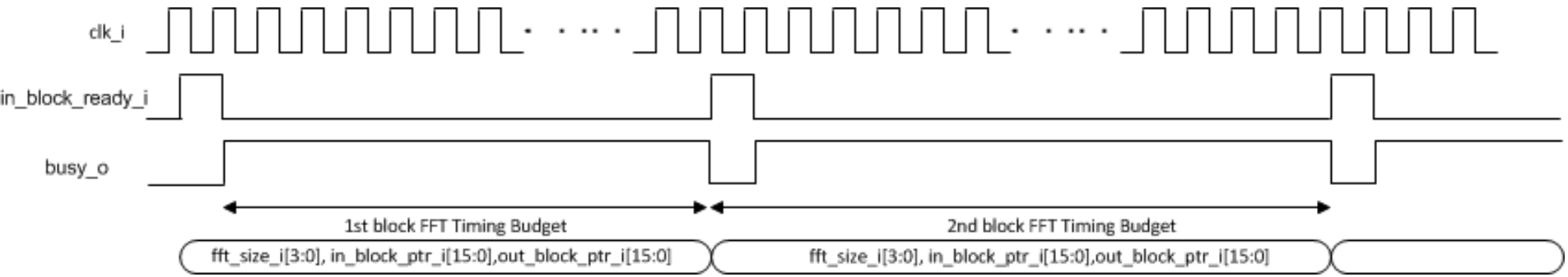
How to interpret input/output pointer

- The very first complex input sample is located at main data memory[in_block_ptr_i].
- The very first complex FFT output sample should be written into main data memory[out_block_ptr_i].

Block Diagram



Input & Output Signal Timing



FFT Core Generator Requirement

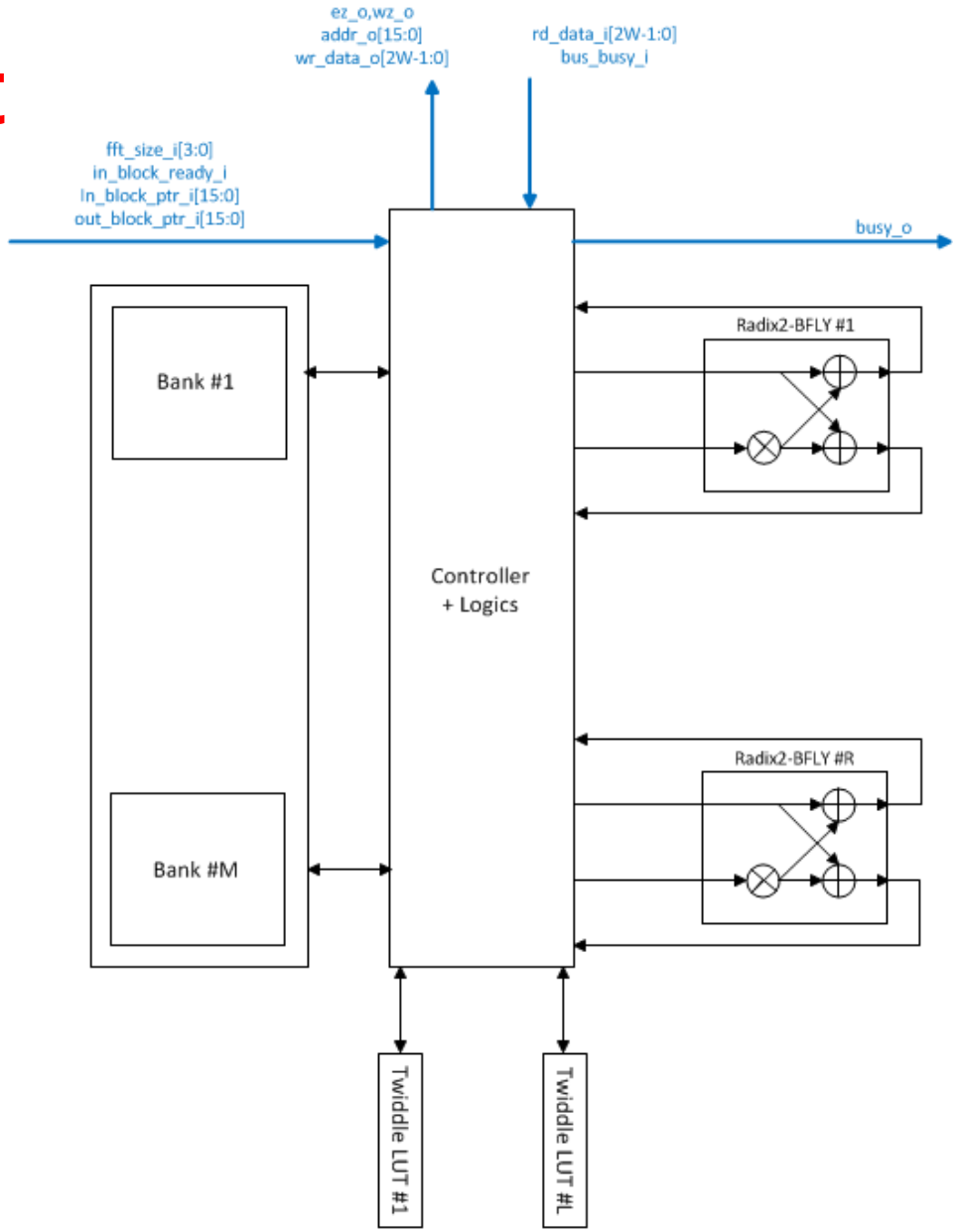
- Parallelism
  - Users should be able to specify the parallelism factor using the following parameters.
    - The required parallelism can be derived from FFT throughput requirement.
  - Parameters
    - Radix-2, Radix-4
    - The number of Radix-2 or Radix-4 BFLY units/cycle
      - Radix-2 Programmable: 0.25, 0.5, 1.0, 2.0 and 4.0
      - Radix-4 Programmable: 0.5, 1.0, 2.0
- Arithmetic
  - Users should be able to chose the desired data-type out of the following choices.
    - Fixed-point or floating point
    - In fixed-point arithmetic
      - Fixed scaling at each stage
      - Dynamic or Block scaling at each stage (at each FFT stage, only if overflow is detected, the scaling is applied).

Demonstrated Use-Case

- Demonstrated Used Case
  - Four-channel 1024-point input FFT
  - Timing budget: 25.6usec
  - FFT accelerator clock speed: 200MHz clock
  - 5120 clock cycles per 4 FFTs
- Architecture candidates
  - option1
    - Generate FFT accelerator where one Radix-2 Butterfly is computed per one cycle (Radix-2 programmable = 1.0 in the previous slide).
    - Make 4 copies of such generated FFT accelerators
  - option2
    - Generate FFT accelerator where four Radix-2 Butterflies are computed per one cycle (Radix-2 programmable = 4 in the previous slide).
  - option3
    - Generate FFT accelerator where one Radix-4 Butterfly is computed per one cycle (Radix-2 programmable = 1. 0 in the previous slide).

Example Architect

- One possible Radix-2 Architecture
  - The number of memory banks=M
  - The number of Twiddle LUTs=L
  - The number of Radix-2 data-path=R
- bus_busy_i can stall CORE
  - If memory access is not granted.



What is expected from GENESIS2 flow

- The generated IP quality should be ready for SoC integration.
  - Module Specification (documentation)
  - Module RTL and compile scripts
  - Makefiles for digital-backend (STA, DFT, FV, LINT, PowerTheater)
  - Testbench / Compile scripts
  - Etc.…