Dual Precision, Rail-to-Rail Output Operational Amplifier

AD8698

FEATURES

Low offset voltage: 100 μV max
Low offset voltage drift: 2 μV/°C max
Low input bias current: 700 pA max
Low noise: 8 nV/√Hz
High common-mode rejection: 118 dB min
Wide operating temperature: −40°C to +85°C
No phase reversal

APPLICATIONS

Photodiode amplifier
Sensors and controls
Multipole filters
Integrator

GENERAL DESCRIPTION

The AD8698 is a high precision, rail-to-rail output, low noise, low input bias current operational amplifier. Offset voltage is a respectable 100 μV max and drift over temperature is below 2 μV/°C, eliminating the need for manual offset trimming. The AD8698 is ideal for high impedance sensors, minimizing offset errors due to input bias and offset currents.

The rail-to-rail output maximizes dynamic range in a variety of applications, such as photodiode amplifiers, DAC I/V amplifiers, filters, and ADC input amplifiers.

The AD8698 dual amplifiers are offered in 8-lead MSOP and narrow 8-lead SOIC packages. The MSOP version is available in tape and reel only.
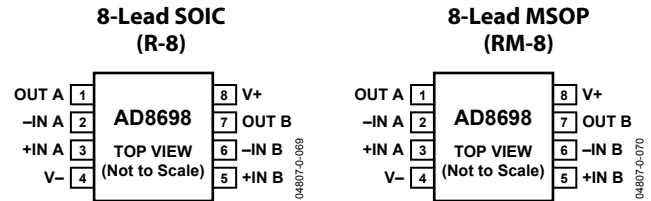
CONNECTION DIAGRAMS

8-Lead SOIC
(R-8)

OUT A	1		8	V+
−IN A	2	**AD8698**	7	OUT B
+IN A	3	TOP VIEW	6	−IN B
V−	4	(Not to Scale)	5	+IN B

04807-0-069

8-Lead MSOP
(RM-8)

OUT A	1		8	V+
−IN A	2	**AD8698**	7	OUT B
+IN A	3	TOP VIEW	6	−IN B
V−	4	(Not to Scale)	5	+IN B

04807-0-070

Figure 1.

AD8698

TABLE OF CONTENTS

REVISION HISTORY

4/04—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm15$ V, $V_{CM} = 0$ V (@$T_A = 25^{\circ}$C, unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			20	100	µV
		-40°C < T_A < $+85^{\circ}$C			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-40°C < T_A < $+85^{\circ}$C		0.6	2	µV/°C
Input Bias Current	I_B				700	pA
		-40°C < T_A < $+85^{\circ}$C			1500	pA
Input Offset Current	I_{OS}				700	pA
		-40°C < T_A < $+85^{\circ}$C			1500	pA
Input Voltage Range	IVR	-40°C < T_A < $+85^{\circ}$C	−13.5V		13.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13.5$ V	118	132		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2$ kΩ, $V_O = \pm13.5$ V	900	1450		V/mV
Input Capacitance	C_{DIFF}			6.5		pF
	C_{CM}			4.6		pF
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Ref. to GND)	V_{OH}	$I_L = 1$ mA, -40°C < T_A < $+85^{\circ}$C	14.85	14.93		V
	V_{OH}	$I_L = 5$ mA, -40°C < T_A < $+85^{\circ}$C	14.6	14.8		V
(Ref. to GND)	V_{OL}	$I_L = 1$ mA, -40°C < T_A < $+85^{\circ}$C		−14.93	−14.6	V
	V_{OL}	$I_L = 5$ mA, -40°C < T_A < $+85^{\circ}$C		−14.82	−14.5	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±2.5 V < V_S < ±15 V	114	132		dB
Supply Current	I_{SY}	$V_O = 0$ V		2.8	3.2	mA
		-40°C < T_A < $+85^{\circ}$C			3.8	mA
Supply Voltage	V_S	-40°C < T_A < $+85^{\circ}$C	±2.5		±15	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2$ kΩ		0.4		V/µs
Gain Bandwidth Product	GBP			1		MHz
Phase Margin	Φ_O				60	Degrees
NOISE PERFORMANCE						
Input Noise Voltage	e_n p-p	0.1 Hz < f < 10 Hz		0.6		µV p-p
Input Voltage Noise Density	e_n	f = 10 Hz		15		nV/√Hz
Input Voltage Noise Density	e_n	f = 1 kHz		8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

AD8698

$V_S = \pm 2.5$ V, $V_{CM} = 0$ V (@$T_A = 25°C$, unless otherwise noted.)

Table 2.

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage		V_{OS}			20	100	μV
			−40°C < T_A < +85°C			300	μV
Offset Voltage Drift		$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C			2	μV/°C
Input Bias Current		I_B				700	pA
			−40°C < T_A < +85°C			1500	pA
Input Offset Current		I_{OS}				700	pA
			−40°C < T_A < +85°C			1500	pA
Input Voltage Range		IVR	−40°C < T_A < +85°C	−1.5		+1.5	V
Common-Mode Rejection Ratio		CMRR	$V_{CM} = \pm 13.5$ V	105	120		dB
Large Signal Voltage Gain		A_{VO}	$R_L = 2$ kΩ, $V_O = \pm 13.5$ V	600	1200		V/mV
Input Capacitance		C_{DIFF}			6.4		pF
		C_{CM}			4.6		pF
OUTPUT CHARACTERISTICS							
Output Voltage Swing	(Ref. to GND)	V_{OH}	$I_L = 1$ mA, −40°C < T_A < +85°C	2.35	2.44		V
		V_{OH}	$I_L = 5$ mA, −40°C < T_A < +85°C	2.1	2.29		V
	(Ref. to GND)	V_{OL}	$I_L = 1$ mA, −40°C < T_A < +85°C		−2.43	−2.2	V
		V_{OL}	$I_L = 5$ mA, $T_A = 25°C$		−2.15	−1.9	V
			$I_L = 5$mA, −40°C<T_A<+85°C			−1.6	
POWER SUPPLY							
Power Supply Rejection Ratio		PSRR	± 2.5 V < V_S < ± 15 V	114	132		dB
Supply Current		I_{SY}	$V_O = 0$ V		2.3	2.8	mA
			−40°C < T_A < +85°C			3.3	mA
Supply Voltage		Vs	−40°C < T_A < +85°C	±2.5		±15	V
DYNAMIC PERFORMANCE							
Slew Rate		SR	$R_L = 2$ kΩ		0.4		V/μs
Gain Bandwidth Product		GBP			1		MHz
Phase Margin		Øo			60		Degrees
NOISE PERFORMANCE							
Input Noise Voltage		e_n p-p	0.1 Hz < f < 10Hz		0.6		μV p-p
Input Voltage Noise Density		e_n	f = 10 Hz		15		nV/√Hz
Input Voltage Noise Density		e_n	f =1 kHz		8		nV/√Hz
Current Noise Density		i_n	f = 1 kHz		0.2		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±15 V
Input Voltage	±V_S
Differential Input Voltage	±V_S
Output Short-Circuit Duration to Gnd	Indefinite
Storage Temperature Range R, RM Packages	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range R, RM Packages	−65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	+300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for devices soldered in circuit boards for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP-8 (RM)	210	45	°C/W
SOIC-8 (R)	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 1000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS
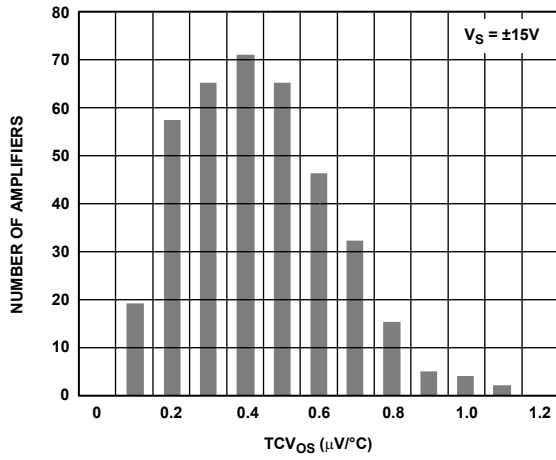
Figure 2. Input Offset Voltage Drift Distribution
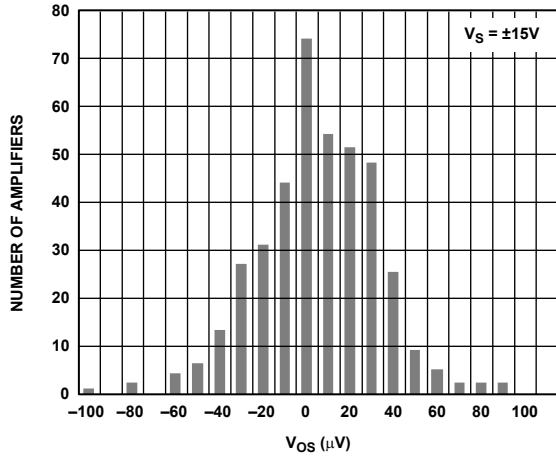
Figure 3. Offset Voltage Distribution
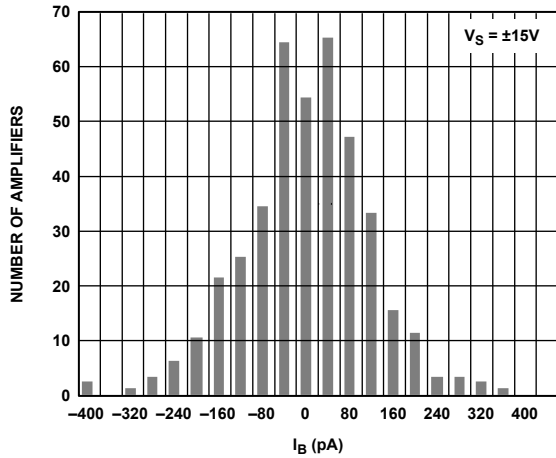
Figure 4. Input Bias Distribution
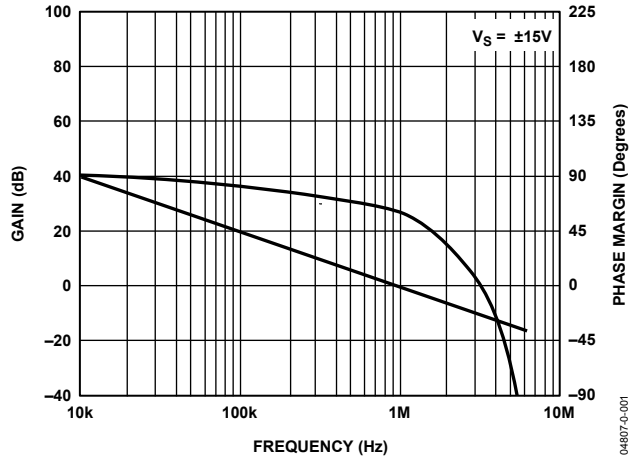
Figure 5. Open-Loop Gain and Phase vs. Frequency
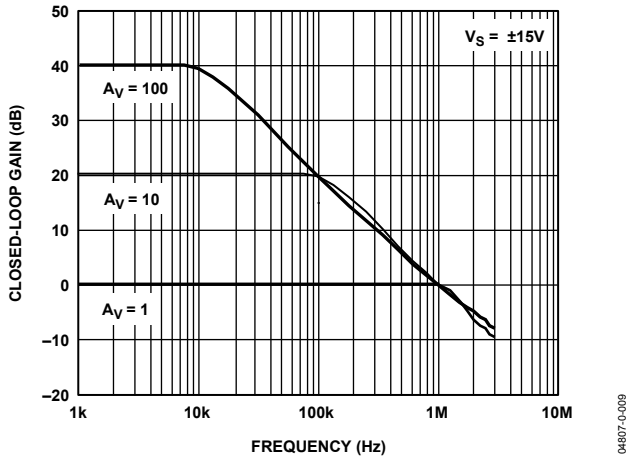
Figure 6. Closed-Loop Gain vs. Frequency
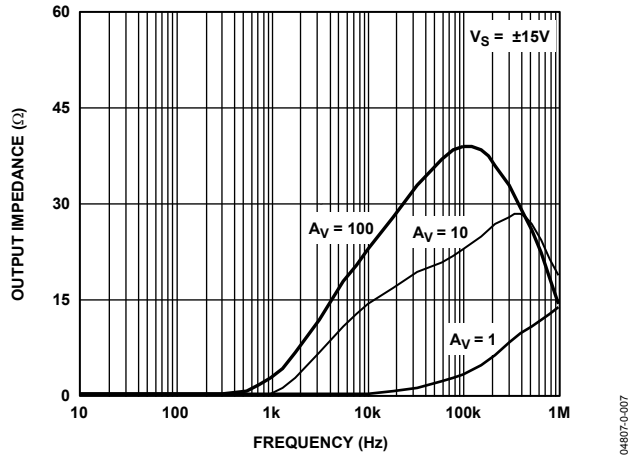
Figure 7. Output Impedance vs. Frequency
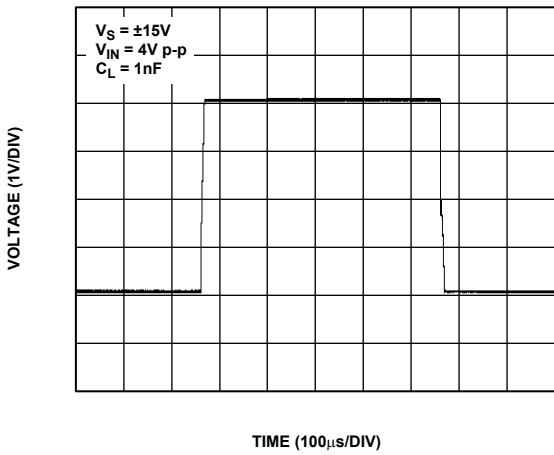
Figure 8. Large Signal Transient Response

Figure 9. Small Signal Transient Response

Figure 10. Overshoot vs. Load Capacitance

Figure 11. Positive Overvoltage Recovery

Figure 12. Negative Overvoltage Recovery
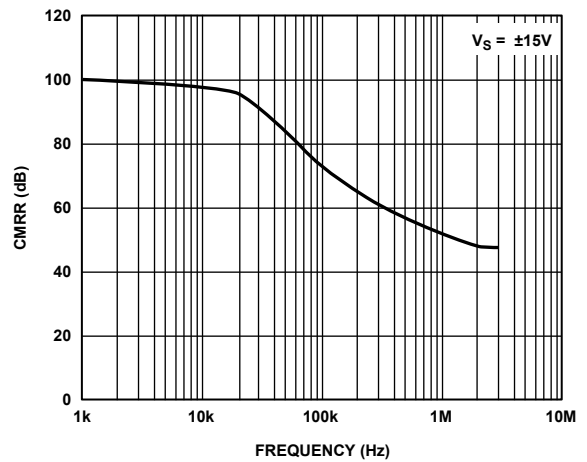
Figure 13. CMRR vs. Frequency
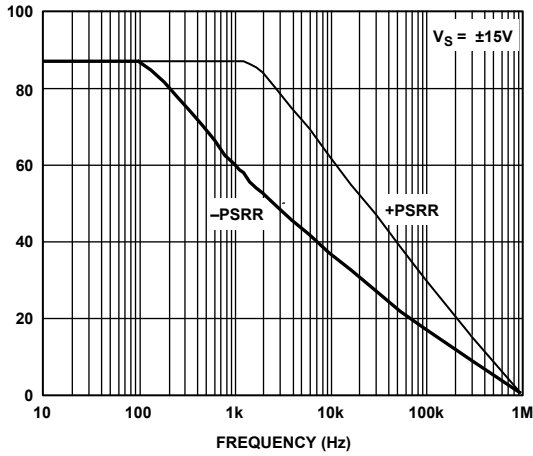
Figure 14. PSRR vs. Frequency

Figure 15. Input Voltage Noise

Figure 16. Voltage Noise Density vs. Frequency

Figure 17. Current Noise Density vs. Frequency

Figure 18. Short-Circuit Current vs. Temperature
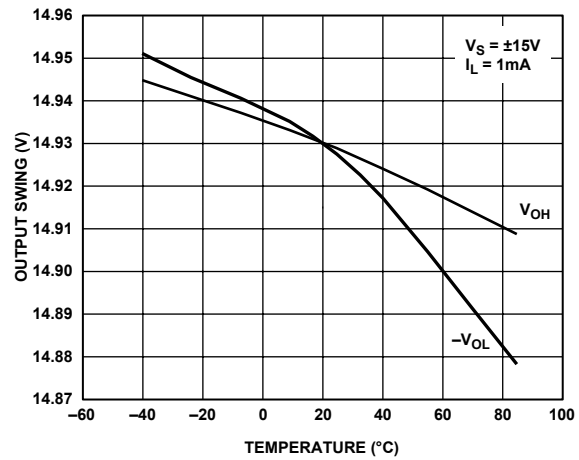
Figure 19. Output Swing vs. Temperature
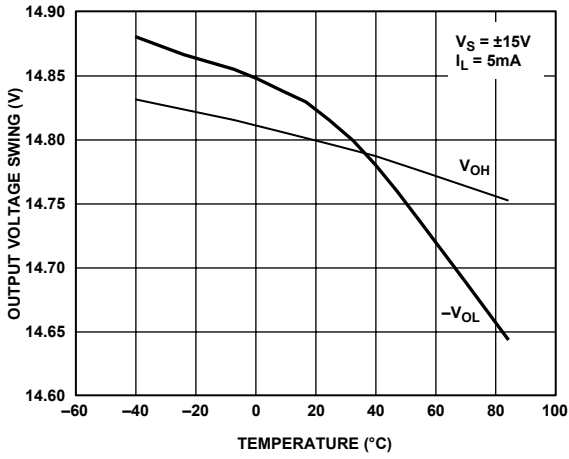
Figure 20. Output Voltage Swing vs. Temperature

Figure 21. Δ Offset Voltage vs. Temperature

Figure 22. CMRR vs. Temperature
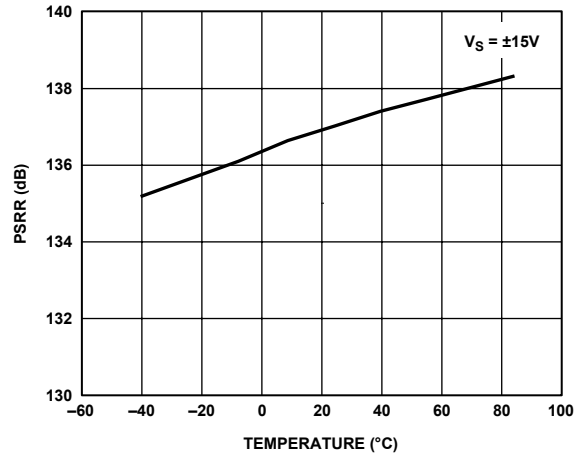
Figure 23. PSRR vs. Temperature
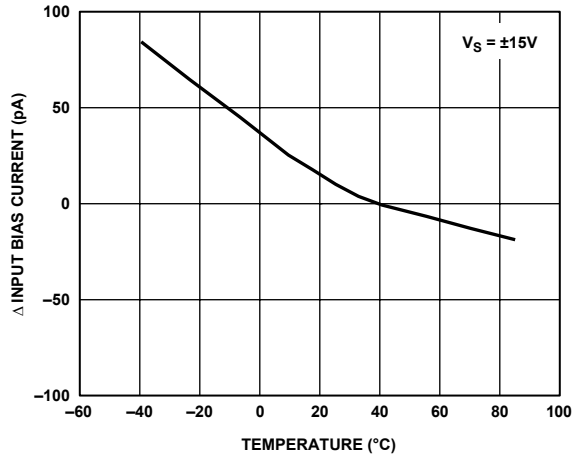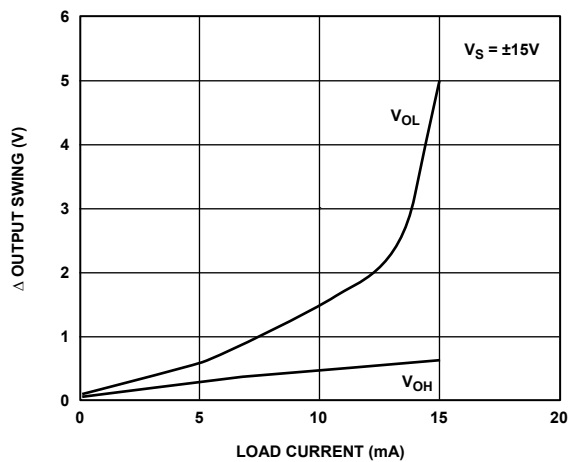

Figure 24. Δ Input Bias Current vs. Temperature
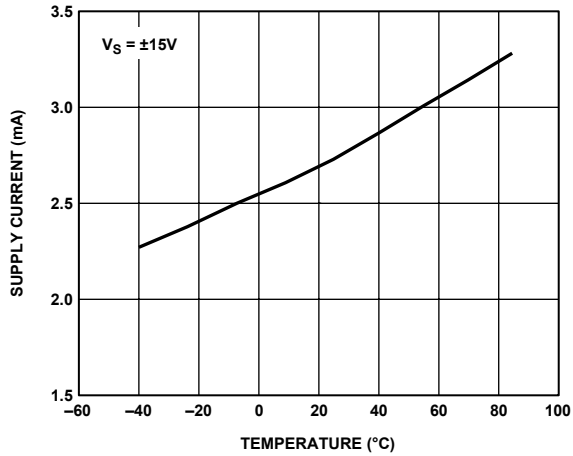

Figure 25. Δ Output Voltage Swing from Rails vs. Load Current

Figure 26. Supply Current vs. Temperature
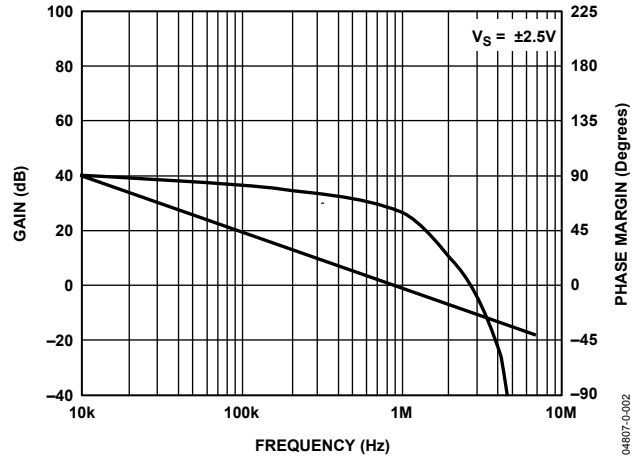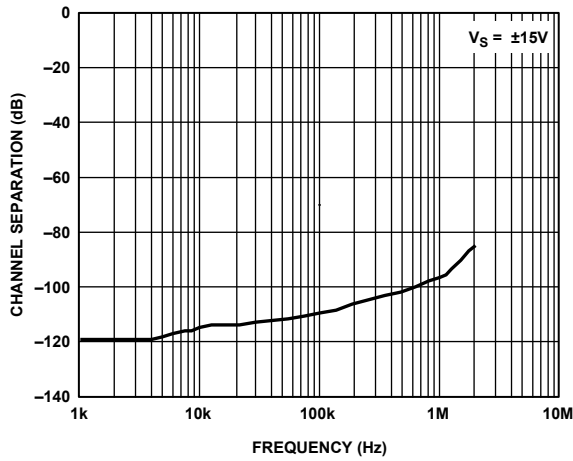

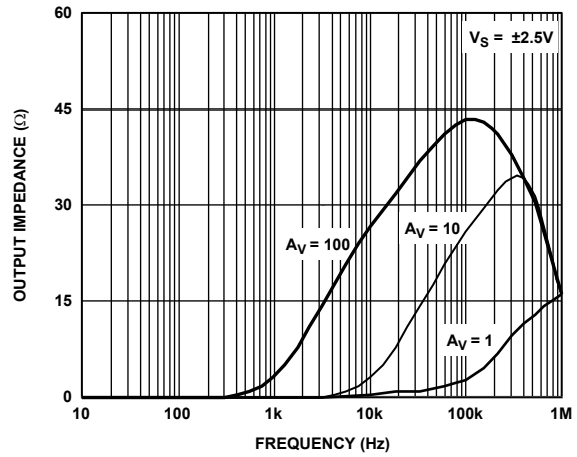Figure 29. Open-Loop Gain and Phase vs. Frequency

Figure 27. Channel Separation

Figure 30. Output Impedance vs. Frequency
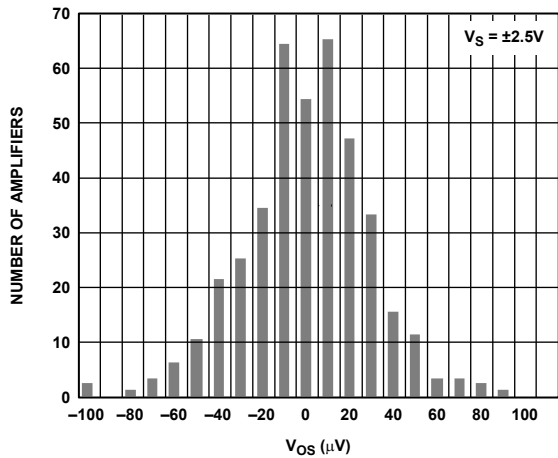

Figure 28. Offset Voltage Distribution
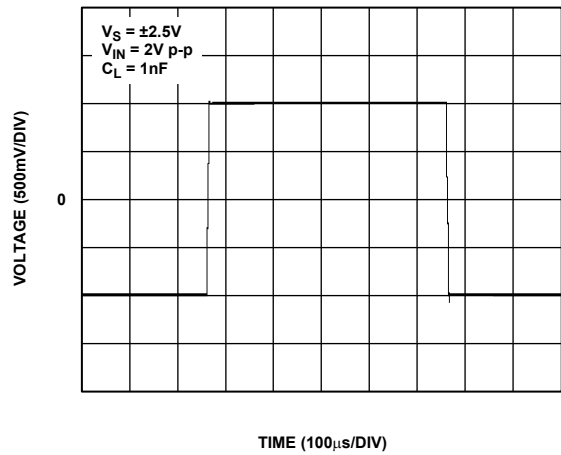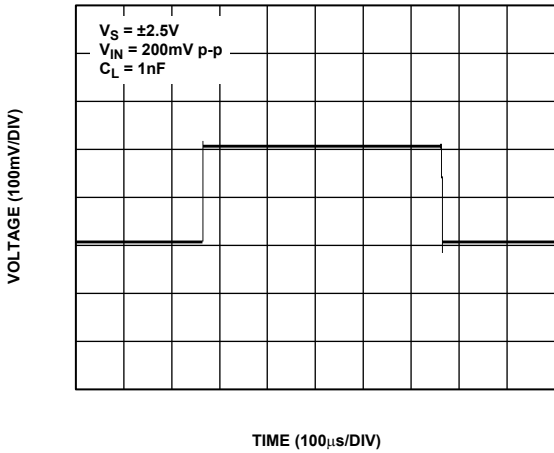

Figure 31. Large Signal Transient Response

Figure 32. Small Signal Transient Response

Figure 35. Negative Overvoltage Recovery
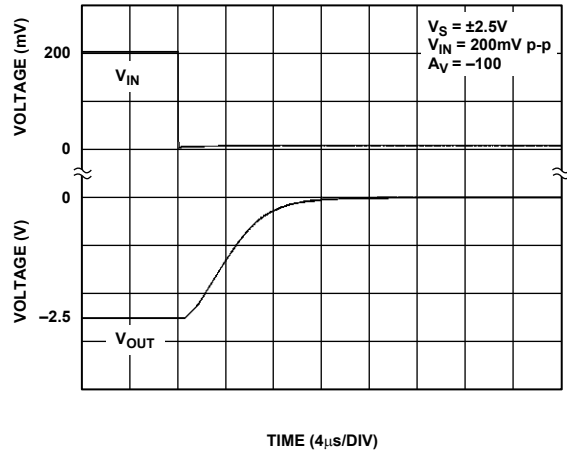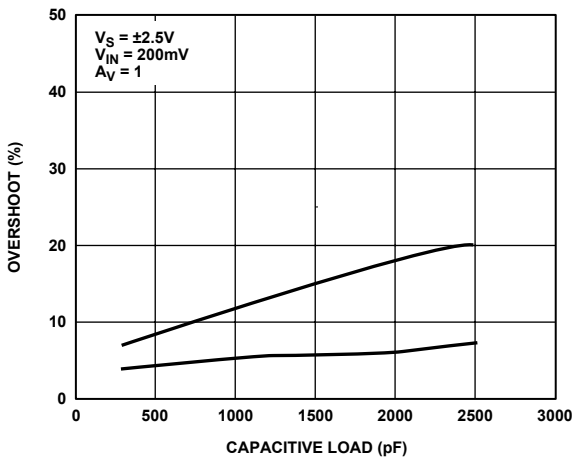

Figure 33. Overshoot vs. Load Capacitance
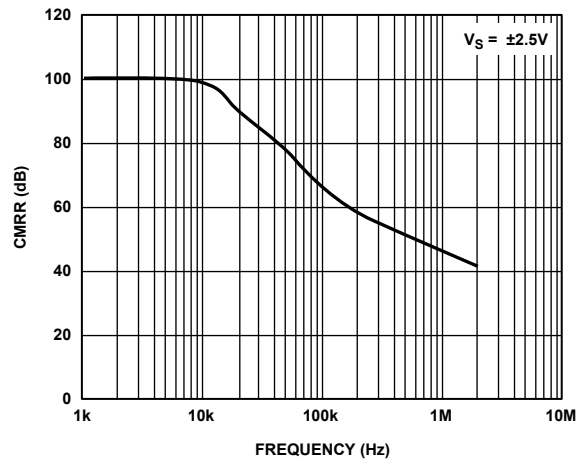
Figure 36. CMRR vs. Frequency

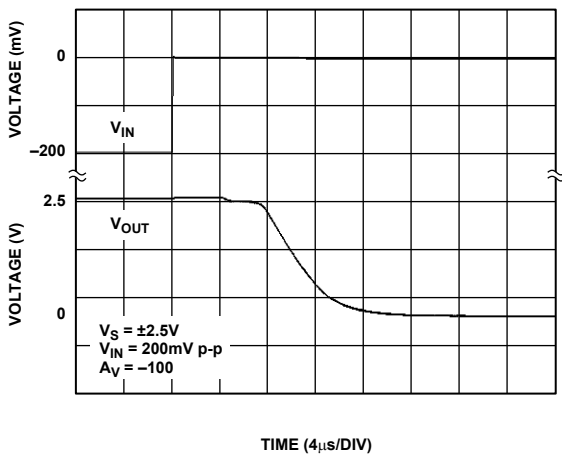*Figure 34. Positive Overvoltage Recovery*
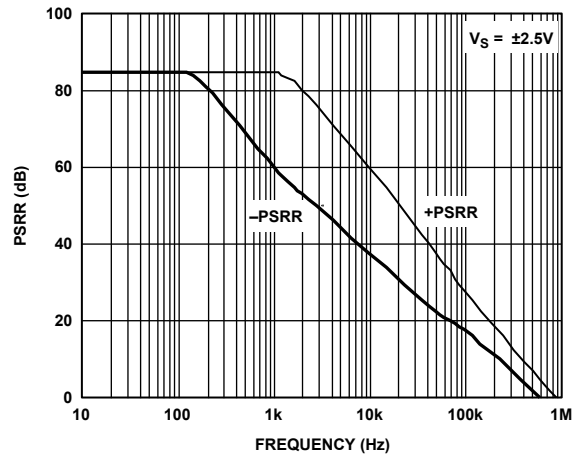
Figure 37. PSRR vs. Frequency
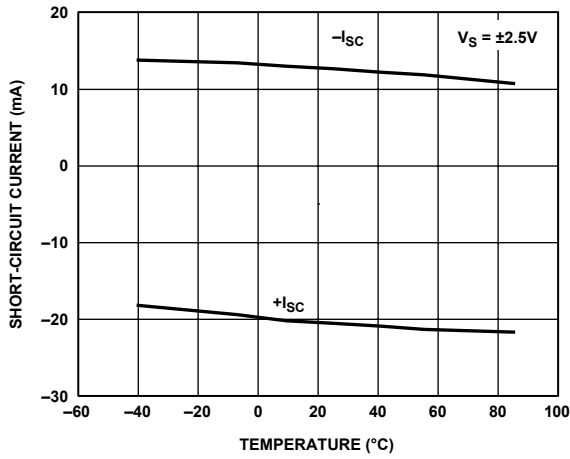
Figure 38. Short-Circuit Current vs. Temperature
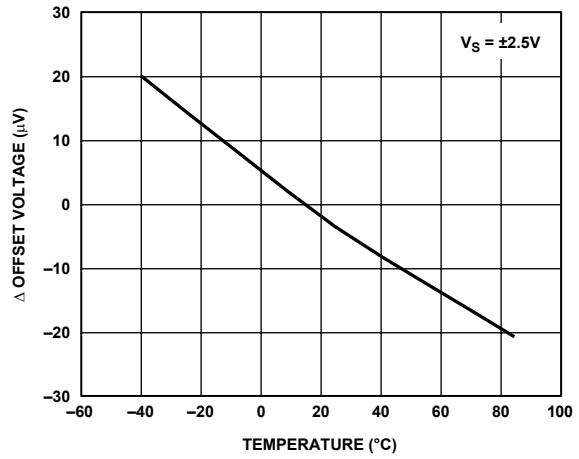
Figure 41. Δ Offset Voltage vs. Temperature
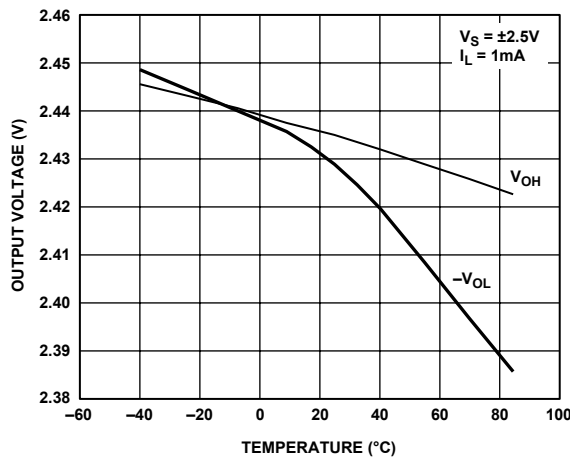
Figure 39. Output Swing vs. Temperature
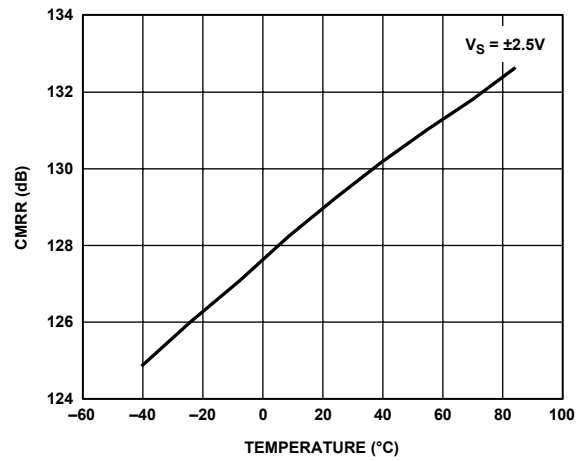
Figure 42. CMRR vs. Temperature
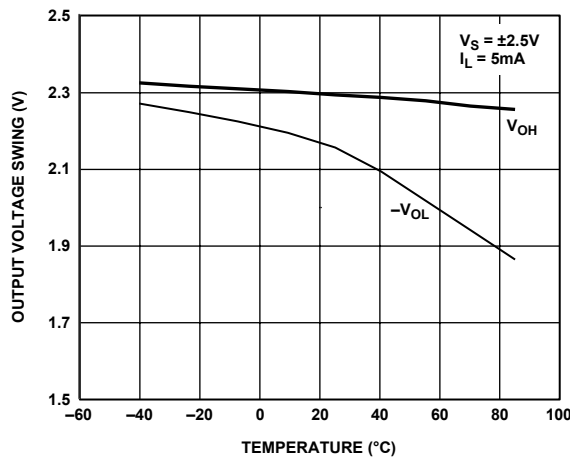
Figure 40. Output Voltage Swing vs. Temperature
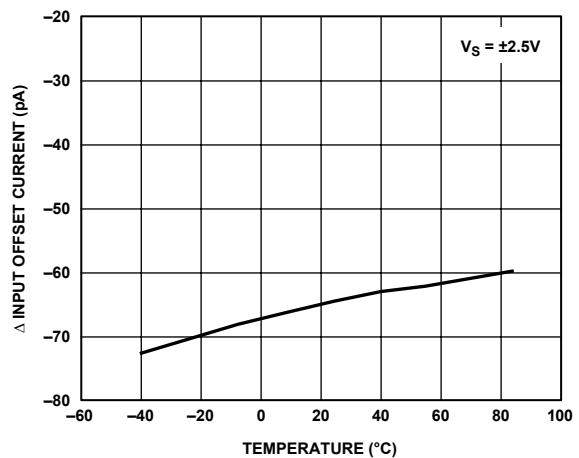
Figure 43. Δ Input Bias Current vs. Temperature
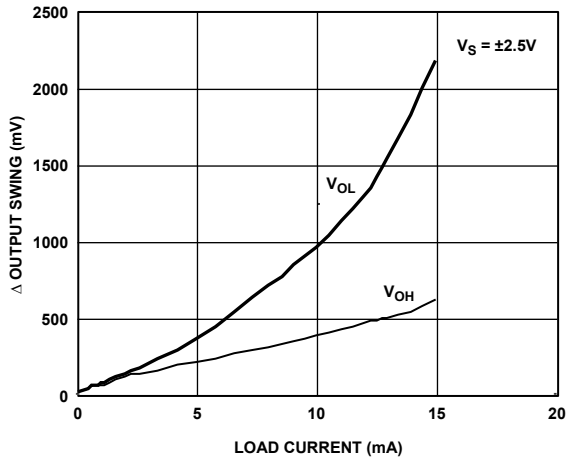
Figure 44. Δ Output Voltage Swing from Rails vs. Load Current

Figure 47. Supply Current vs. Supply Voltage

Figure 45. Supply Current vs. Temperature

Figure 48. Channel Separation

Figure 46. No Phase Reversal

APPLICATIONS

INPUT OVERVOLTAGE PROTECTION

The AD8698 has internal protective circuitry which allows voltages at either input to exceed the supply voltage. However, if voltages applied at either input exceed the supply voltage by more than 2 V, it is recommended to use a resistor in series with the inputs to limit the input current and prevent damaging the device.
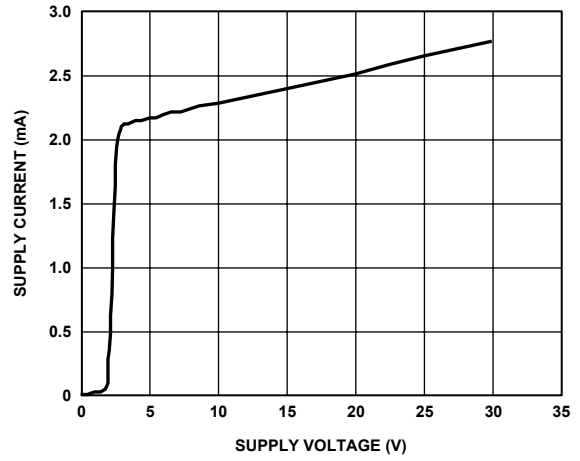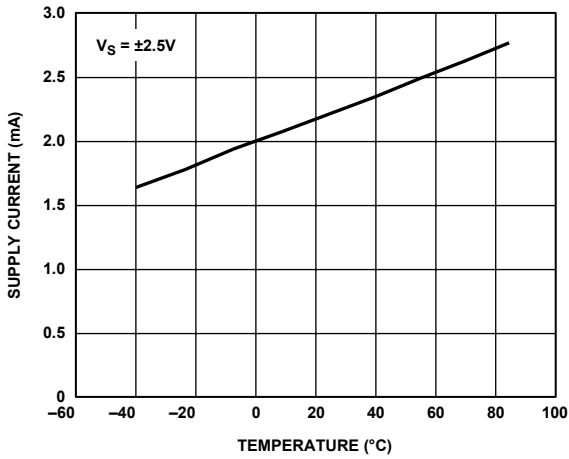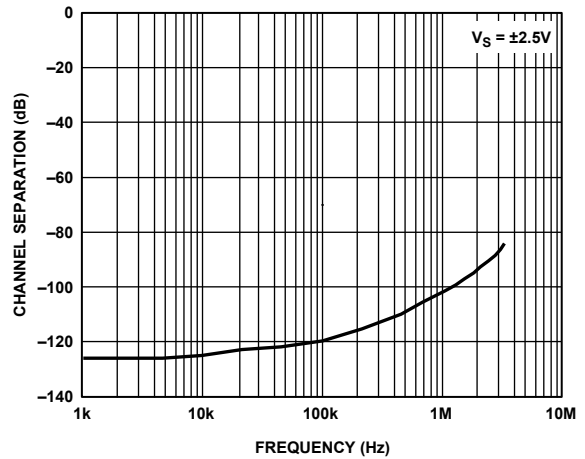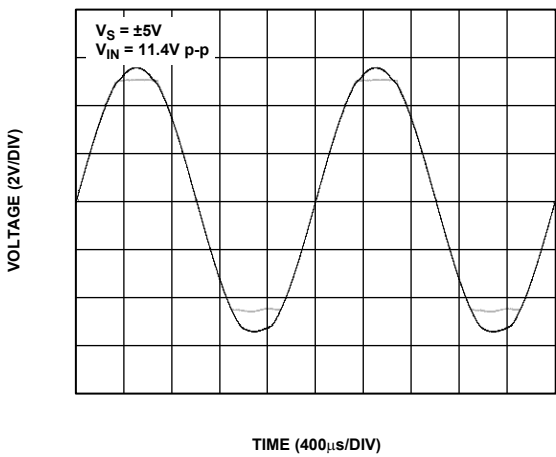
The value of the resistor can be calculated from the following formula:

$$\frac{V_{IN} - V_S}{R_S + 500} \le 5\,\text{mA}$$

DRIVING CAPACITIVE LOADS

The AD8698 is stable even when driving heavy capacitive loads in any configuration. Although the AD8698 will safely drive capacitive loads well over 10 nF, it is recommended to use external compensation should the amplifier be subjected to driving a load exceeding 50 nF. This is particularly important in positive unity gain configurations, the worst case for stability. Figure 49 shows the output of the AD8698 with a 68 nF load in response to a 400 mV signal at its positive input; the overshoot is less than 25% without any external compensation. Using a simple "snubber" network reduces the overshoot to less than 10% as shown in Figure 50.
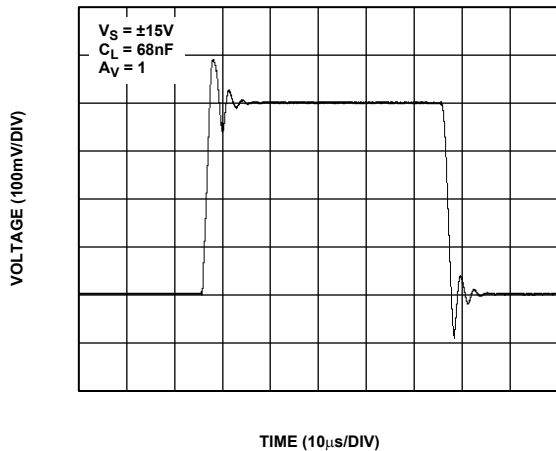
Figure 49. Heavy Capacitive Load Drive without Compensation
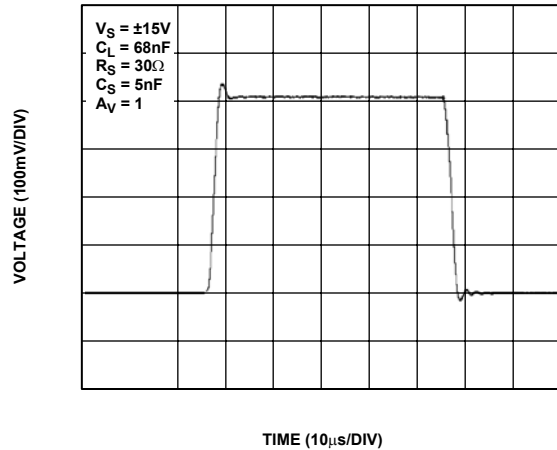
Figure 50. Compensated Capacitive Load Drive with Snubber

The snubber network consists of a simple RC network whose values are determined empirically.
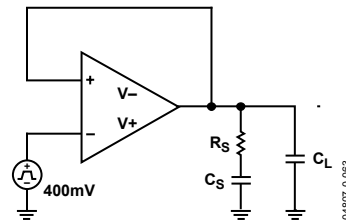
Figure 51. Snubber Network

Table 5 provides a few starting values for optimum compensation.

Table 5. Compensation Values

C_L (nF)	R_S (Ω)	C_S (nF)
47	20	7
68	30	5
100	50	3

The use of the snubber network does not recover the loss of bandwidth incurred by the load capacitance. The AD8698 maintains a unity gain bandwidth of 1 MHz with load capacitances of up to 1 nF.
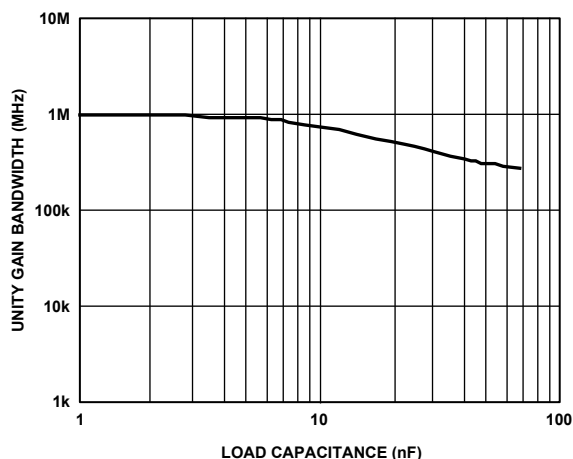
Figure 52. Unity Gain Bandwidth vs. Load Capacitance

Figure 52 shows the unity gain bandwidth as a function of load capacitance.

INSTRUMENTATION AMPLIFIER

Instrumentation amplifiers are used in applications requiring precision, accuracy, and high CMRR. One popular application is signal conditioning in process control, test automation, and measurement instrumentation, where the amplifier is used to amplify small signals.

The triple op amp implementation uses the AD8698 at the front end with the OP184 for optimum accuracy.

The circuit in Figure 53 enjoys a high overall gain, excellent dc performance, high CMRR, as well as the benefit of an output that swings to the supplies.

The CMRR of the in-amp will be limited by the choice of resistor tolerance. R5 is an optional potentiometer that can be used to calibrate the circuit for maximum gain. R7 can be trimmed for optimum CMRR.

The output voltage is given by:

$$V_O = V_{IN}\left(1 + \frac{2R3}{R4}\right)\left(\frac{R2}{R1}\right)$$
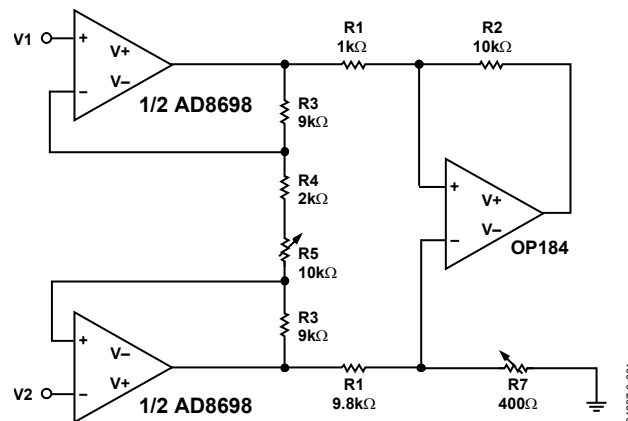
Figure 53. Three Op Amp In-Amp

COMPOSITE AMPLIFIER

The dc accuracy of the AD8698 and the ac performance of the OP184 are combined in the circuit shown in Figure 54. The composite amplifier provides a higher bandwidth, a lower offset voltage, and a higher loop, thereby reducing the gain error substantially.

The circuit shown exhibits a total output rms noise of less than 500 µV, corresponding to less than 3 mV of peak-to-peak noise over approximately a 3 MHz bandwidth. Cf is used to minimize peaking.

The circuit has an inverting gain of 10. In applications with higher closed-loop gains, Cf is necessary to maintain a sufficient phase margin and ensure stability. This results in a narrower closed-loop bandwidth.

Figure 54. Composite Amplifier Circuit

AD8698

LOW NOISE APPLICATIONS

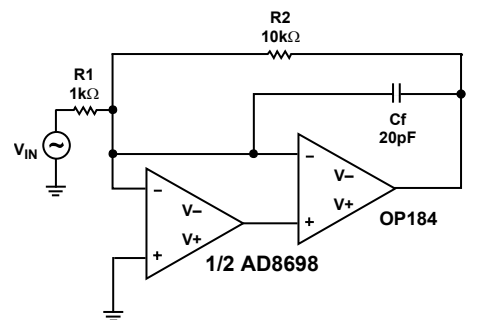In some applications, it is critical to minimize the noise, and although the AD8698 has a low noise of typically 8 nV/√Hz at 1 kHz, paralleling the two amplifiers within the same package reduces the total noise referred to the input to approximately 5.5 nV/√Hz. This simple technique is depicted in Figure 55.
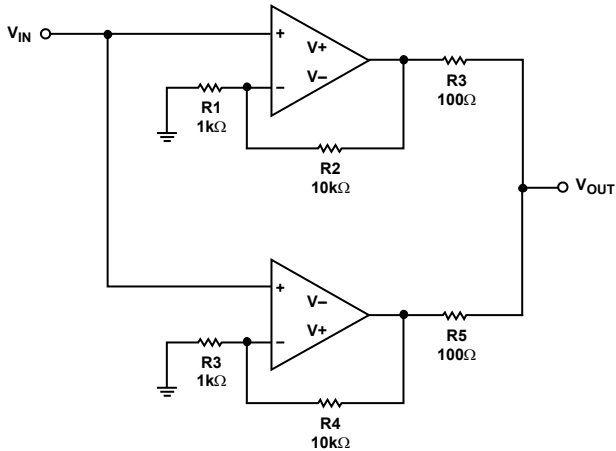

Figure 55. Paralleling Amplifiers

DRIVING ADCs

The AD8698 can drive extremely heavy capacitive loads without any compensation. Sometimes capacitors are placed at the output of the amplifier to absorb transient currents while the op amp is interfaced with the ADC. Most op amps need a small resistor with the output to isolate the load capacitance.

This results in a loss of bandwidth and slows the amplifier down substantially. However, the AD8698 maintains a unity gain bandwidth of 1 MHz with loads of up to 1 nF, as shown in Figure 52.

USING THE AD8698 IN ACTIVE FILTER DESIGNS

The AD8698 is recommended for unity gain filter designs with a corner frequency of up to 100 kHz, one tenth of the op amp's unity gain bandwidth.

If a higher gain is desired, the corner frequency should be chosen accordingly. For example, if the amplifier is configured with a gain of 10, the corner frequency of the filter should not be more than 10 kHz.

An example of an active filter is the Sallen Key. This topology gives the user the flexibility of implementing a low-pass or a high-pass filter by simply interchanging the resistors and the capacitors.

In the high-pass filter of Figure 56, the damping factor Q is set to $1/\sqrt{2}$ for a maximally flat response (Butterworth).

The gain is unity and the bandwidth is 10 kHz with the values shown.
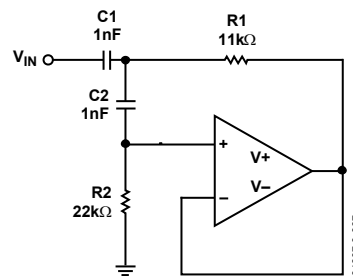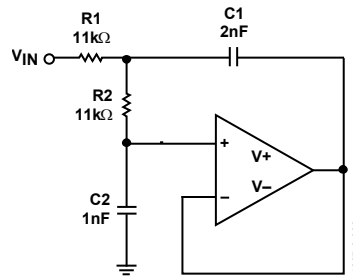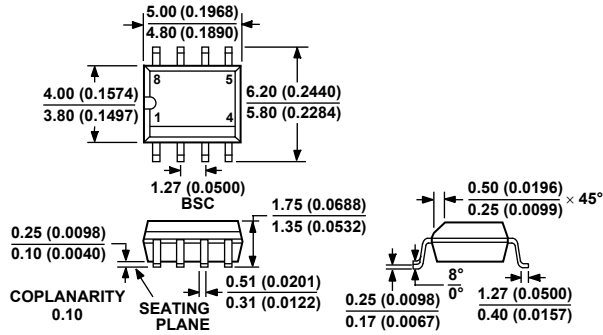

Figure 56. Two Pole High-Pass Filter

*Figure 57. Two Pole Low-Pass Filter*

The circuit of Figure 57 has a bandwidth of 10 kHz and a maximally flat response. In this case, the damping factor is controlled by the ratio of the capacitors and the gain is unity.

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 58. 8-Lead Small Outline IC [SOIC] (R-8)—Dimensions shown in millimeters
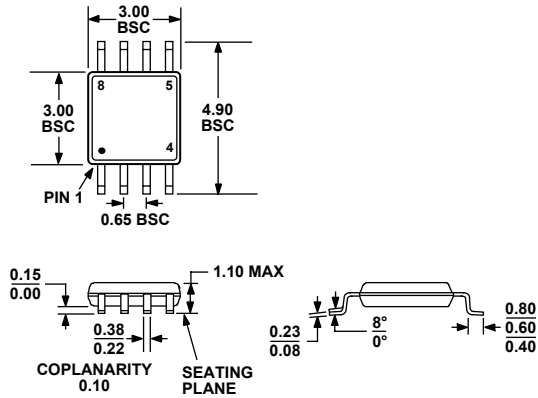
COMPLIANT TO JEDEC STANDARDS MO-187AA

Figure 59. 8-Lead Small Outline IC [SOIC] (RM-8)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Package	Package Description	Package Option	Branding
AD8698ARM-R2	−40°C to +85°C	MSOP	RM-8	A02
AD8698ARM-REEL	−40°C to +85°C	MSOP	RM-8	A02
AD8698AR	−40°C to +85°C	SOIC	R-8	
AD8698AR-REEL	−40°C to +85°C	SOIC	R-8	
AD8698AR-REEL7	−40°C to +85°C	SOIC	R-8	

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