



North South University

Department of Electrical & Computer Engineering

Course Code: CSE 231

Course Name: Digital Logic Design

Final Assessment Report

Spring 2020

Submitted to: Tanjila Farah

Student Name & ID:

ID	Name	Contribution
1731194042	Sudipta Bhatta	

CODE OF HONOR PLEDGE

I pledge on my honor that I have not given or received any unauthorized assistance on this assignment.

Signature: Sudipta

Date: 28 May, 2020

Truth Table

Index	A	B	C	D	a	b	c	d	e	f	g	Output
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	0	0	1
8	1	0	0	0	0	1	1	0	0	0	0	1
11	1	0	1	1	1	1	1	0	0	1	1	9
13	1	1	0	1	0	1	1	0	0	1	1	9

Generalized SOP Functions:

$$a = A'B'CD + AB'CD$$

$$= \Sigma(3, 11)$$

$$b = c = A'B'CO + A'BC'D' + AB'C'D' + AB'CD + ABC'D$$

$$= \Sigma(3, 4, 8, 11, 13)$$

$$d = AB'CD$$

$$= \Sigma(3)$$

$$f = AB'CD + ABC'D$$

$$= \Sigma(11, 13)$$

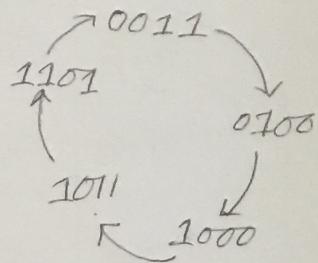
$$g = A'BCD + AB'CD + ABC'D$$

$$= \Sigma(3, 11, 13)$$

Excitation table with D flip-flop

Present State	Next State	D
0	0	0
0	1	1
1	0	0
1	1	1

state diagram



Characteristic table with D flip-flop

Present state $Q_3\ Q_2\ Q_1\ Q_0$	Next state $Q_3\ Q_2\ Q_1\ Q_0$	D			
		D_3	D_2	D_1	D_0
0 0 0 0	0 0 1 1	0	0	1	1
0 0 0 1	- - - -	x	x	x	x
0 0 1 0	- - - -	x	x	x	x
0 0 1 1	0 1 0 0	0	1	0	0
0 1 0 0	1 0 0 0	1	0	0	0
0 1 0 1	- - - -	x	x	x	x
0 1 1 0	- - - -	x	x	x	x
0 1 1 1	- - - -	x	x	x	x
1 0 0 0	1 0 1 1	1	0	1	1
1 0 0 1	- - - -	x	x	x	x
1 0 1 0	- - - -	x	x	x	x
1 0 1 1	1 1 0 1	1	1	0	1
1 1 0 0	- - - -	x	x	x	x
1 1 0 1	0 0 1 1	0	0	1	1
1 1 1 0	- - - -	x	x	x	x
1 1 1 1	- - - -	x	x	x	x

$Q_3 Q_2$	$Q_0 Q_1$	$Q_1 Q_0$	$Q_1 Q_0$	$Q_1 Q_0$	$Q_1 Q_0'$
$Q_3 Q_2'$	0 0	x 1	0 3	x 2	
$Q_3 Q_2$	1 4	x 5	x 7	x 6	
$Q_3 Q_2$	x 12	0 13	x 15	x 14	
$Q_3 Q_2'$	1 8	x 9	1 11	x 10	

$$D_3 = Q_3' Q_2 + Q_3 Q_2'$$

$$= Q_3 \oplus Q_2$$

$Q_3 Q_2$	$Q_1 Q_0$	$Q_1 Q_0'$	$Q_1 Q_0$	$Q_1 Q_0$	$Q_1 Q_0'$
$Q_3 Q_2'$	0 0	x 1	1 3	x 2	
$Q_3 Q_2$	0 4	x 5	x 7	x 6	
$Q_3 Q_2$	x 12	0 13	x 15	x 14	
$Q_3 Q_2'$	0 8	x 9	1 11	x 10	

$$D_2 = Q_2$$

$Q_1 Q_0$	$Q_2' Q_2'$	$Q_1' Q_0$	$Q_1 Q_0$	$Q_1' Q_0'$
$Q_3' Q_2'$	1	x	0	x
$Q_3' Q_2$	0	x	x	x
$Q_3 Q_2$	x	1	x	x
$Q_3 Q_2'$	1	x	0	x
	8	9	11	10
	12	13	15	14

$$D_1 = Q_2' Q_1' + Q_1' Q_0$$

$Q_1 Q_0$	$Q_2' Q_2'$	$Q_1' Q_0$	$Q_1 Q_0$	$Q_1' Q_0'$
$Q_3' Q_2'$	1	x	0	x
$Q_3' Q_2$	0	x	x	x
$Q_3 Q_2$	x	1	x	x
$Q_3 Q_2'$	1	x	1	x
	8	9	11	10
	12	13	15	14

$$D_0 = Q_3 + Q_2' Q_1'$$

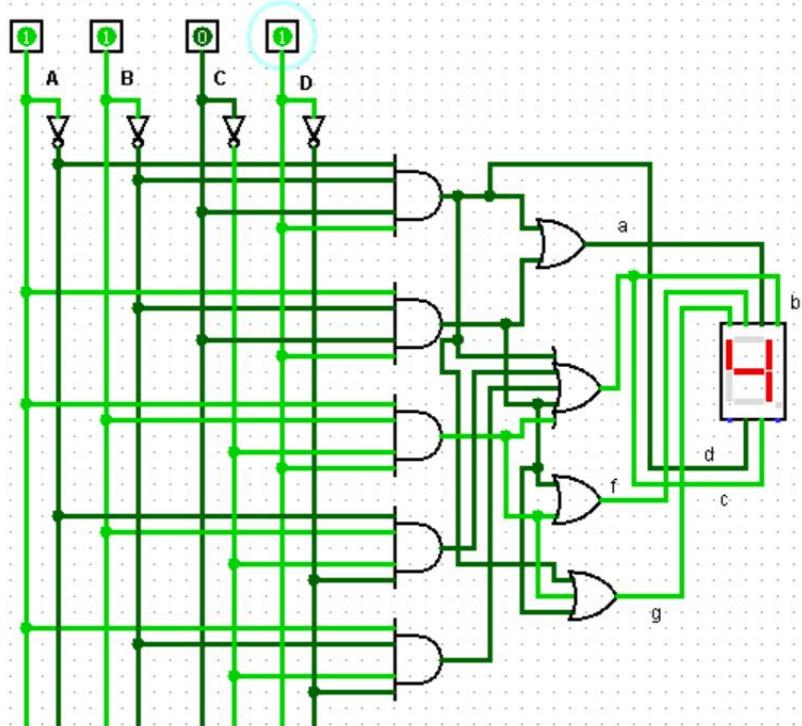


Figure: Combinational Circuit

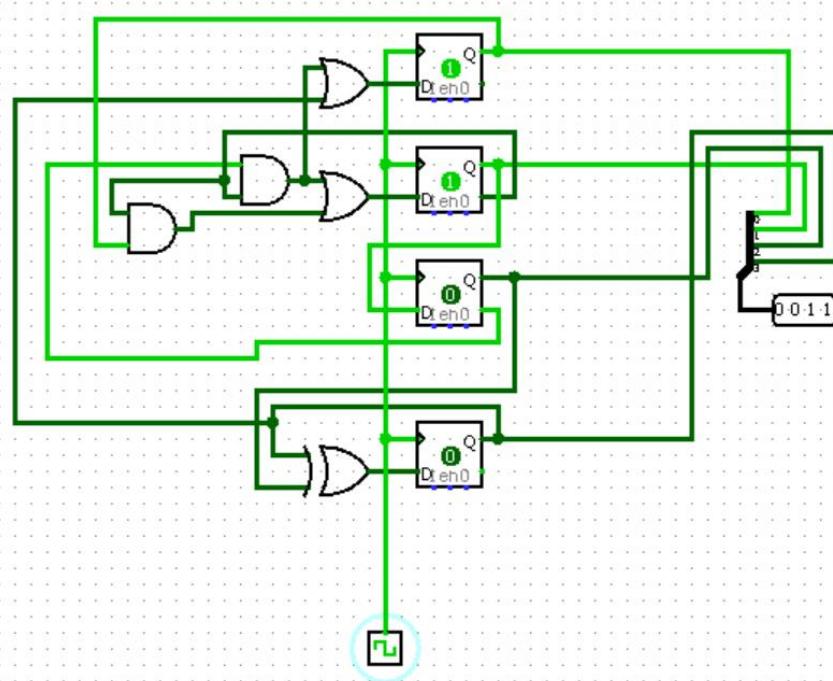
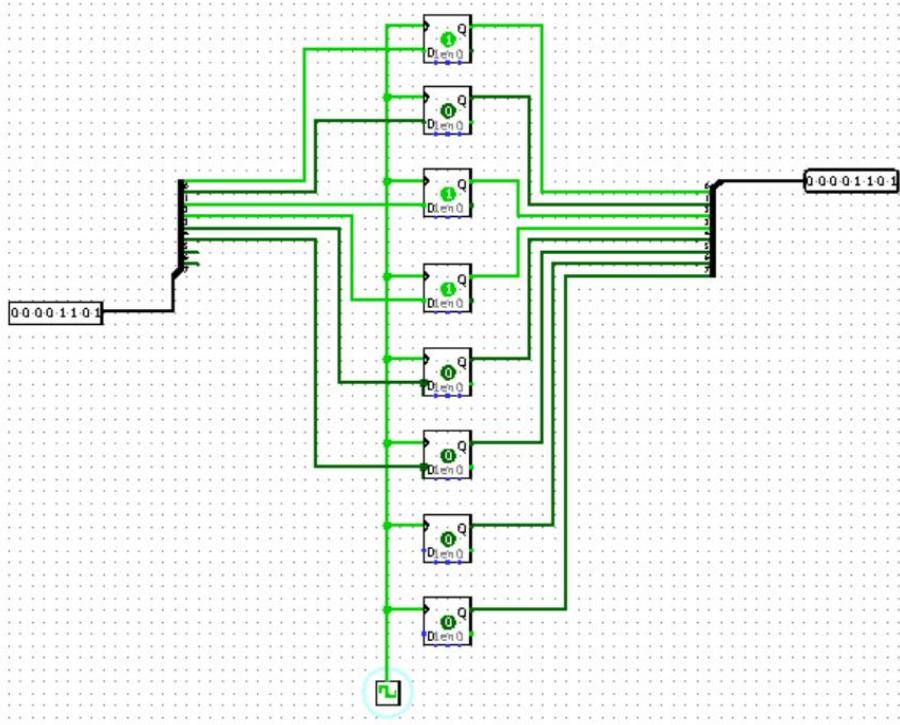


Figure: Counter with D flip-flop



8 bit parallel register with D flip-flop

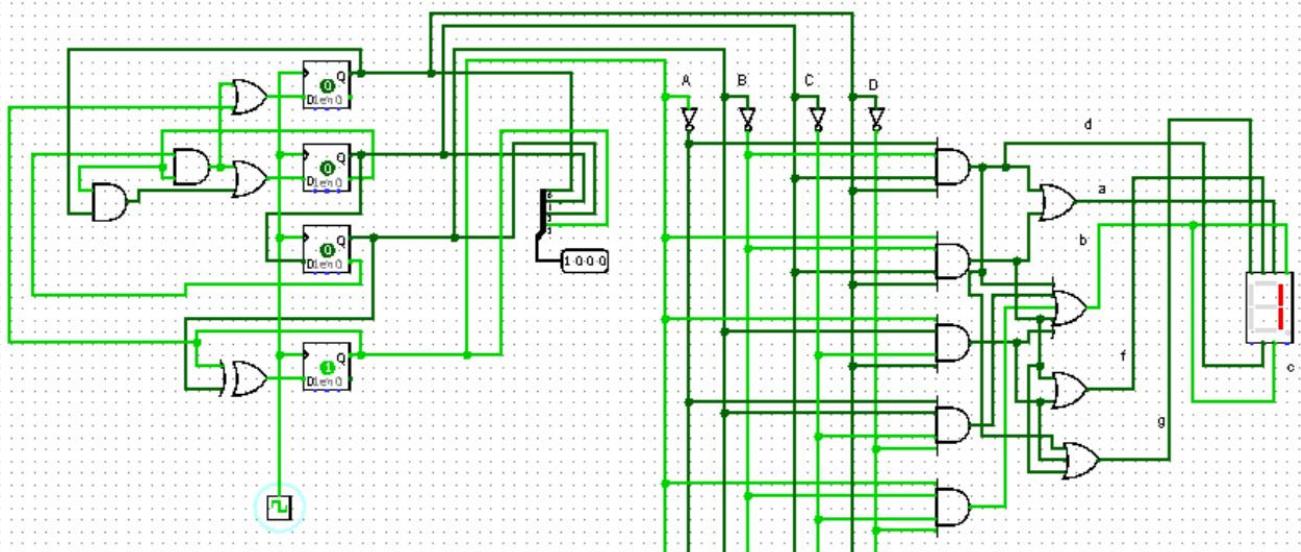


Figure: Sequential Circuit

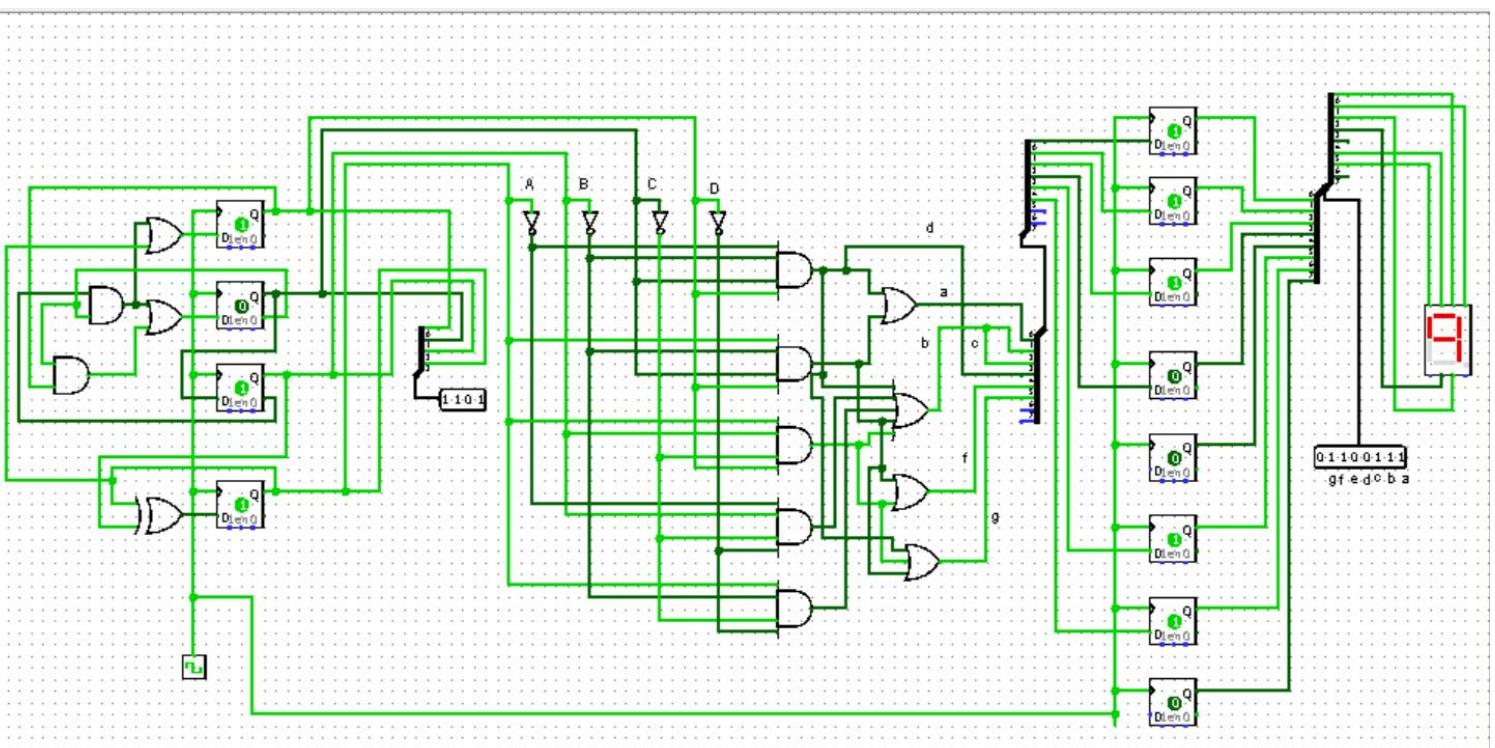


Figure: Sequential and Combinational Circuit using D flip-flop and register