# HD66206

(80-Channel Column/Common Driver for Middle- or Large-sized Liquid Crystal Panel)

HITACHI

Rev 0.2
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## Description

The HD66206 is an 80-channel LCD driver, which is used for liquid crystal dot matrix display. This product can drive various types of liquid crystal displays, from small-sized to monochrome VGA-sized displays. Since this product can function as a column and a common driver, an LCD panel can be configured only with this product.

## Features

- Logic power supply voltage: 2.7 to 5.5V
- Display duty: 1/16 (1/5 bias) to 1/240
- 80 liquid crystal display drive circuits
- Liquid crystal display drive voltage: 6 to 28V
- Data transfer speed
  - 8 MHz max (at 5-V operation)
  - 6.5 MHz max (at 3-V operation)
- Chip enable signal automatic generation
- Standby function
- Controllers that can be used with
  - HD64645/HD64646 (LCTC series)
  - HD66841 (LVIC series)
- Packages
  - TFP-100B
  - No package (bare chip)
- CMOS process

## Ordering information

| Type name | Package |
|---|---|
| HD66206TE | TFP-100B |
| HCD66206 | Bare chip |

## Pin Arrangement

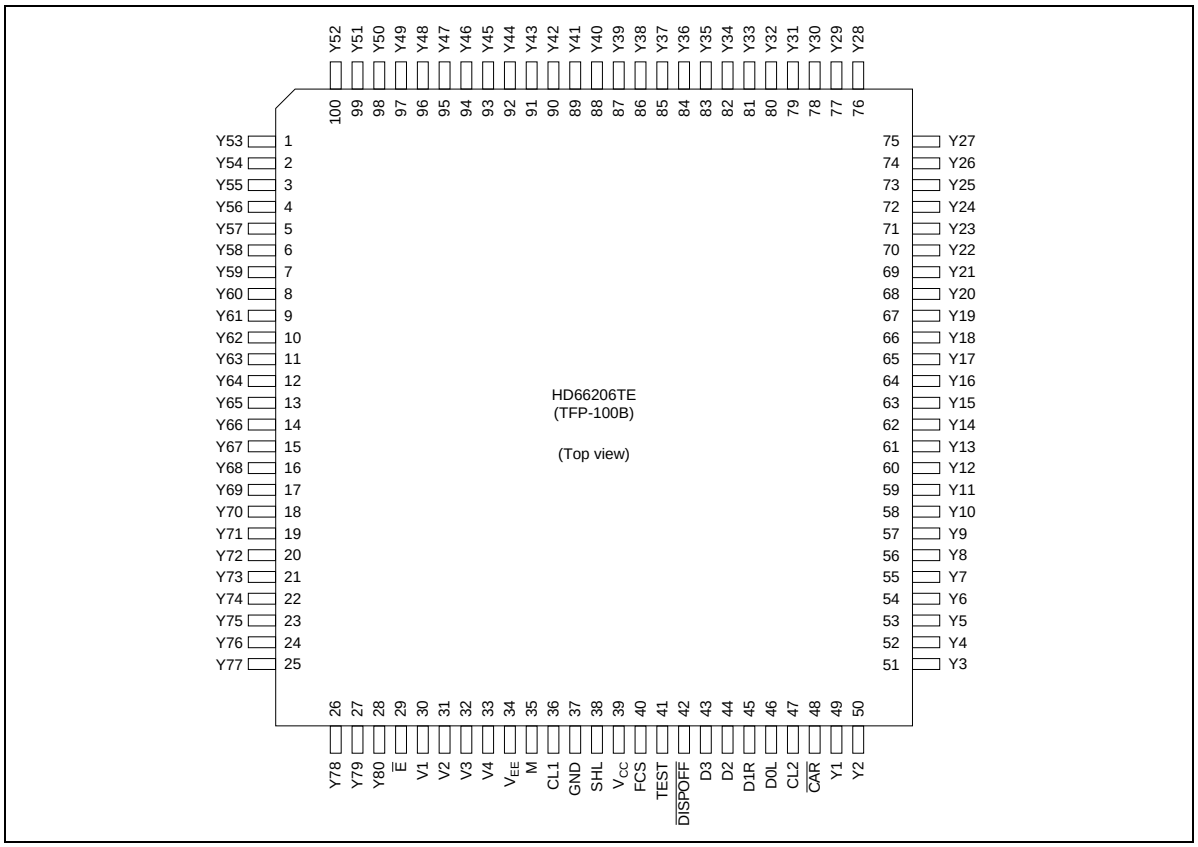


**Figure 1 Pin Arrangement (HD66206TE)**

## Block Diagram

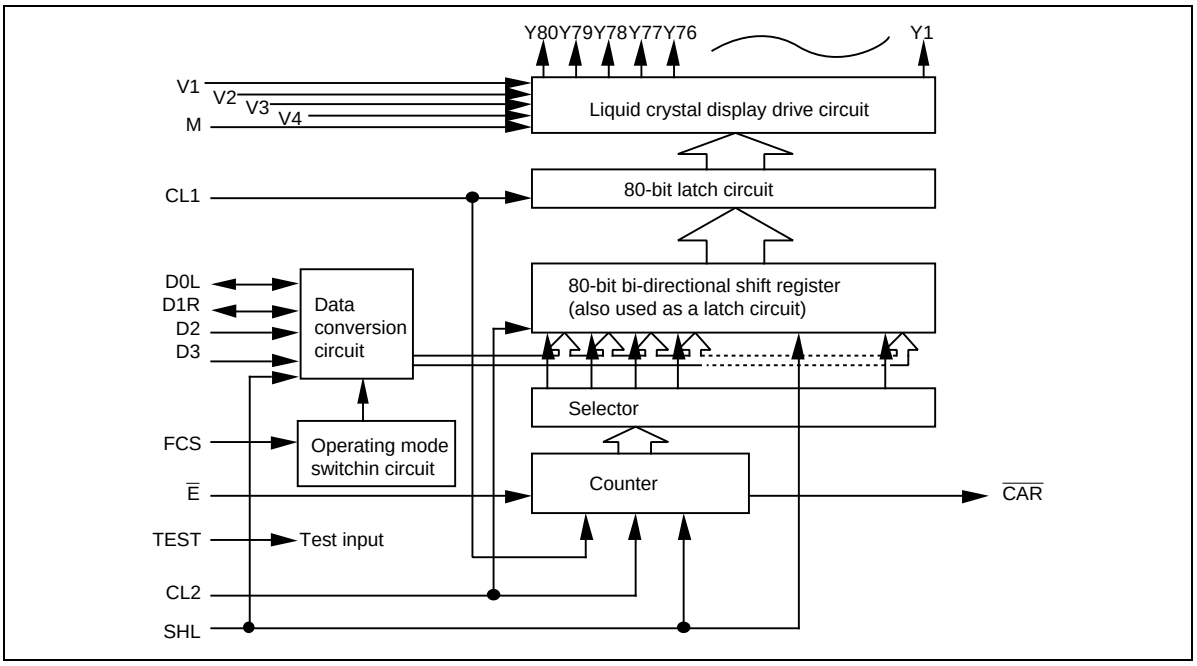


**Figure 2 Block Diagram**

## Block Functions

### Liquid crystal display drive circuit

Generates one of four levels V1 to V4 to the output pin to drive the liquid crystal display according to the combination of data of the 80-bit latch circuit and the M signal.

### 80-bit latch circuit

Latches data of the 80-bit bi-directional shift register (also used as a latch circuit) at the falling edge of CL1, and transmits it to the liquid crystal display drive circuit.

### 80-bit bi-directional shift register (also used as a latch circuit)

When FCS is low, this register functions as an 80-bit shift register. At this time, D0L and D1R are used as data input/output pins. When FCS is high, this register functions as a $20 \times 4$-bit unit latch circuit. At this time, data that is input in parallel to data input pin D0L, D1R, D2 and D3 is converted to 4-bit data, and then is latched to this register according to the latch signal generated by the selector.

### Data conversion circuit

When FCS is low, D0L and D1R are used as data input/output pins. When FCS is high, D0L, D1R, D2, and D3 are input data.

### Selector

Decodes output data from the counter and generates a latch signal. Functions when latching data at serial-latch operation (when FCS is high). At this time, after 80 bits of data Y1 to Y80 are completely latched, the operation of the selector terminates. Even if input data changes, data in the latch circuit is maintained.

### Operating mode switching circuit

Switches common driver operation (when FCS is low) and column driver operation (when FCS is high).

## Pin Function

**Table 1 Pin Functions**

| Classification | Symbol | Pin No. | Pin Name | Input/ Output | Function |
|---|---|---|---|---|---|
| Power supply | $V_{CC}$<br>GND<br>$V_{EE}$ | 39<br>37<br>34 | $V_{CC}$<br>GND<br>$V_{EE}$ | — | $V_{CC}$–GND: Logic power supply<br>$V_{CC}$–$V_{EE}$: Power supply for driving the liquid crystal display. |
| | V1<br>V2<br>V3<br>V4 | 30<br>31<br>32<br>33 | V1<br>V2<br>V3<br>V4 | Input | Power supply voltage for liquid crystal display drive level.<br>See Figure 3. |
| Control signal | CL1 | 36 | Clock 1 | Input | Column driver data latch signal. Data is latched at the falling edge of this signal. Set this signal low in common driver operation. |
| | CL2 | 47 | Clock 2 | Input | In column driver operation, used as a display data latch signal.<br>In common driver operation, used as a line selection data shift signal.<br>In both operations, this signal is valid at its falling edge. |
| | M | 35 | M | Input | AC conversion signal for liquid crystal display drive output. |
| | SHL | 38 | Shift left | Input | Control signal for inverting data output destination.<br>1. In column driver operation<br>See Figure 4.<br>2. In common driver operation<br>SR1, SR2, SR3, ...., SR80 correspond to Y1, Y2, Y3, ...., Y80 outputs.<br>When SHL is low, data is input to D0L pin and output from D1R pin. D2 and D3 are set low.<br>When SHL is high, the relationships between D0L and D1R are reverse.<br>See Table 2. |
| | $\overline{E}$ | 29 | Enable | Input | When FCS is high, data latch starts by setting the $\overline{E}$ signal low.<br>When FCS is low, set the $\overline{E}$ signal high.<br>The relationships between the $\overline{E}$ signal, the FCS signal, data latch operation, and driver function are as show in Table 3 |

**Table 1 Pin Function (cont)**

| Classification | Symbol | Pin No. | Pin Name | Input/ Output | Function |
|---|---|---|---|---|---|
| Control signal | $\overline{CAR}$ | 48 | Carry | Output | When FCS is high, a chip enable signal is transferred to the next IC from this pin. Connect this pin to $\overline{E}$ of the next IC. When FCS is low, open this pin. |
| | $\overline{DISPOFF}$ | 42 | Display off | Input | When this signal is low, liquid crystal display drive output is set at V1 level and liquid crystal display is turned off. At this time, internal display data is not affected. When this signal is high, the operation returns to the normal status. |
| | D0L<br>D1L | 46<br>45 | Data0 (L)<br>Data1 (R) | Input/ output | In column driver operation, input display data to D0L, D1R, D2, and D3 pins. In common driver operation, when SHL is high, D0L and D1R pins are display data output and input pins, respectively, and vice versa when SHL is low. At this time, set D2 and D3 low. |
| | D2<br>D3 | 44<br>43 | Data2<br>Data3 | Input | When display data is high, liquid crystal display drive output is selection level and the display is on, and when display data is low, they are non-selection level and off, respectively. |
| | FCS | 40 | Function select | Input | Control signal to select each operating mode. When the FCS pin is high, the operating mode is column driver, and when it is low, the operation mode is common driver. |
| | TEST | 41 | TEST | Input | Test pin. Set this pin low. |
| Liquid crystal display drive output | Y1 to Y80 | 49 to 100<br>1 to 28 | Y1 to Y80 | Output | Liquid crystal display drive output. One of four levels V1 to V4 is output according to the combination of the M signal and display data. See Figures 5 and 6. |

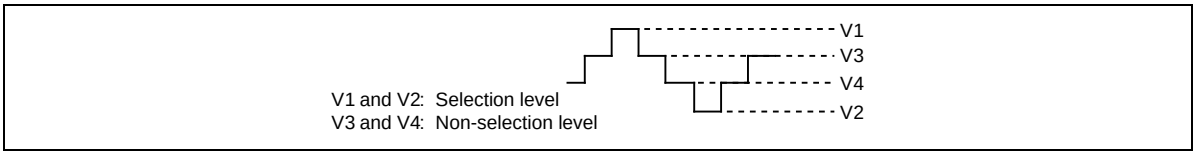


**Figure 3 Liquid Crystal Display Drive Level**

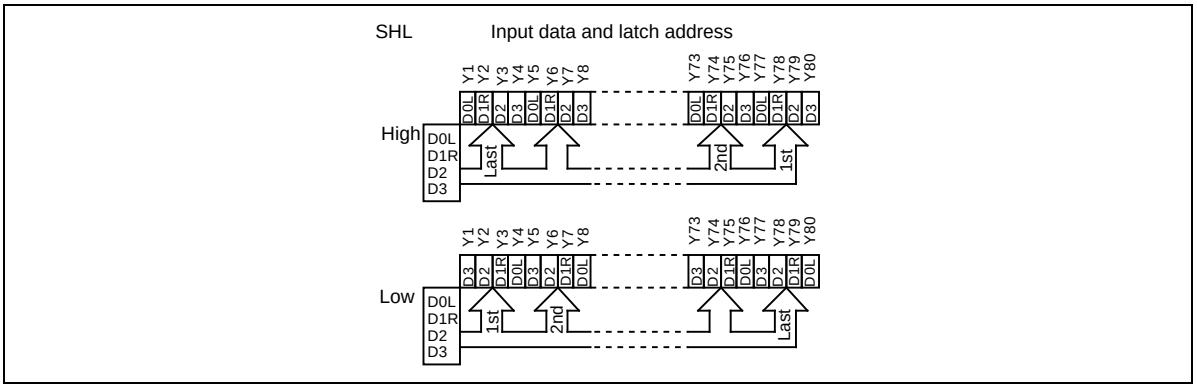


**Figure 4 Column Driver Operating Mode**

**Table 2 Common Driver Operation**

| SHL | Shift Register Shift Direction | | | | | Common Signal Scan Direction | |
|---|---|---|---|---|---|---|---|
| Low | D0L | SR 1 | SR 2 ..... | SR 80 | D1R | Y1 | Y80 |
| High | D1R | SR 80 | SR 79 ..... | SR 1 | D0L | Y80 | Y1 |

**Table 3 Relationship between FCS, $\overline{E}$, Data Latch Operation, and Driver Function**

| FCS | $\overline{E}$ | Data Latch Operation | Driver Function |
|---|---|---|---|
| High | Low | Enabled | Column driver |
| | High | Disabled | |
| Low | High | — | Common driver |

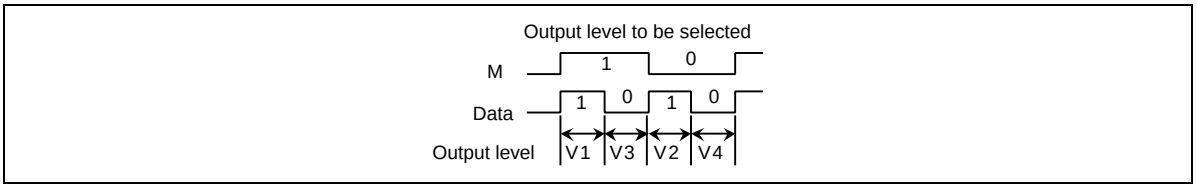


**Figure 5 Liquid Crystal Display Drive Output in Column Driver Operation**

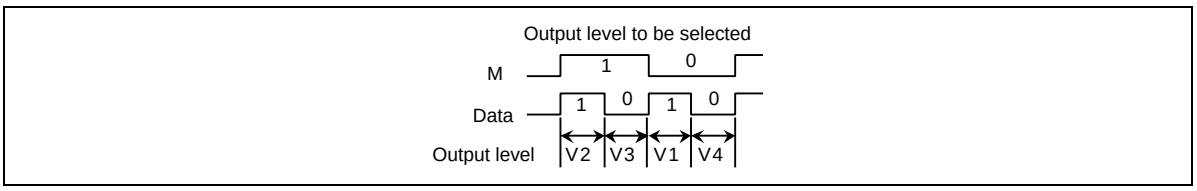


**Figure 6 Liquid Crystal Display Drive Output in Common Driver Operation**

## Application Examples

Figure 7 shows an example when configuring the 640 × 240-dot LCD panel using the HD66206.

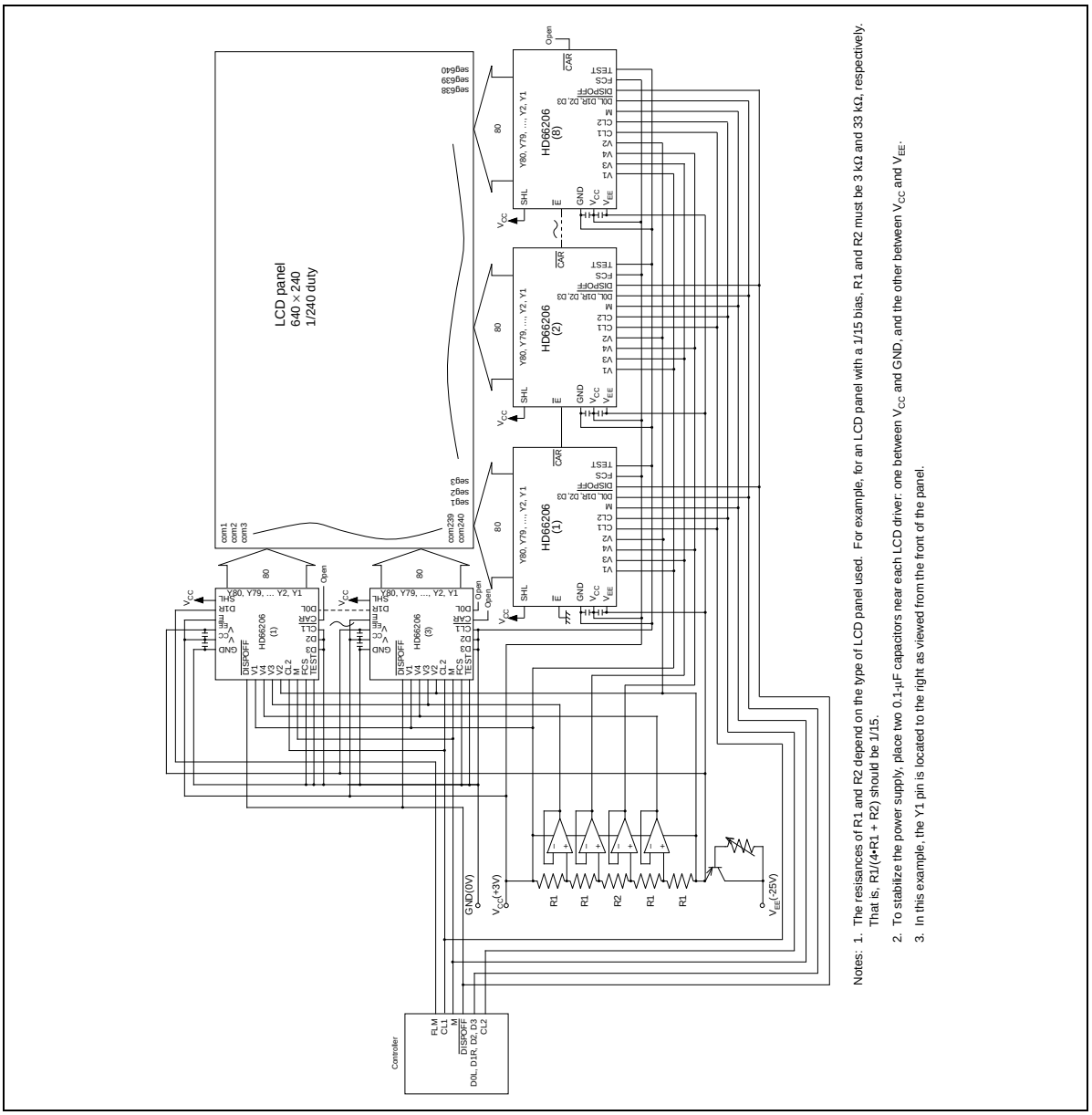


**Figure 7 Application Example**

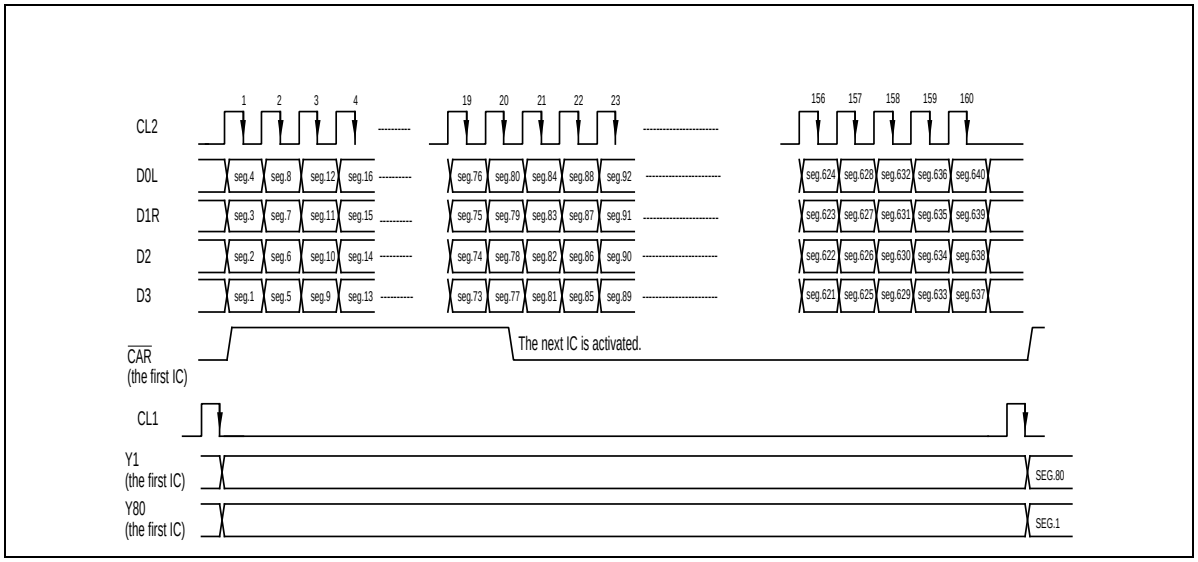


**Figure 8 Timing Charts for Application Example in Column Driver Operation**

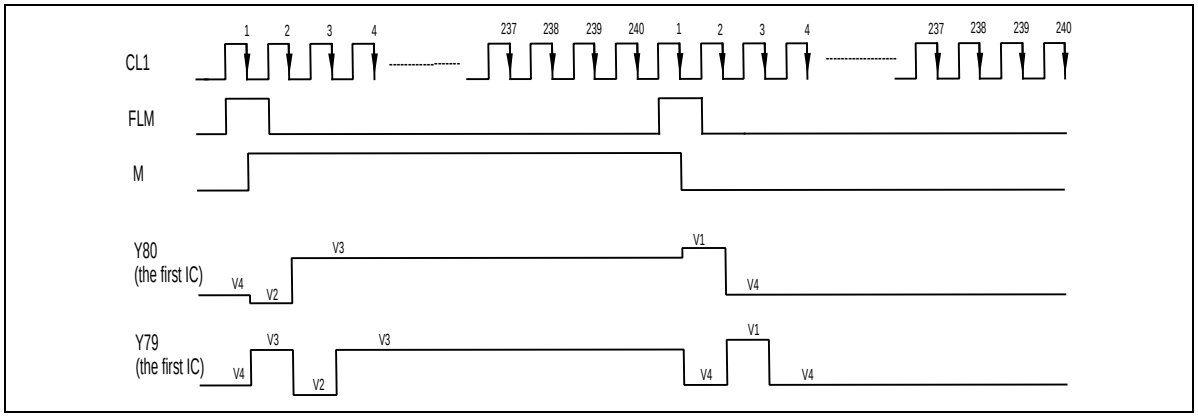


**Figure 9 Timing Charts for Application Example in Common Driver Operation**

## Absolute Maximum Ratings

| Item | | Symbol | Ratings | Unit | Note |
|---|---|---|---|---|---|
| Power supply voltage | Logic circuit | $V_{CC}$ | –0.3 to +7.0 | V | 1 |
| | Liquid crystal display drive circuit | $V_{EE}$ | $V_{CC}$ – 30.0 to $V_{CC}$ + 0.3 | V | |
| Input voltage (1) | | VT1 | –0.3 to $V_{CC}$ + 0.3 | V | 1 and 2 |
| Input voltage (2) | | VT2 | $V_{EE}$ – 0.3 to $V_{CC}$ + 0.3 | V | 1 and 3 |
| Operating temperature | | $T_{opr}$ | –20 to +75 | °C | |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C | |

Notes: 1. Measured relative to GND (0V).
2. Applies to CL1, CL2, M, SHL, $\overline{E}$, D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$ pins.
3. Applies to V1 to V4 pins.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

## Electrical Characteristics

**DC Characteristics 1 ($V_{CC}$ = 5V ± 10%, GND = 0V, $V_{CC} - V_{EE}$ = 6 to 28V, and Ta = –20 to 75 °C, unless otherwise stated)**

| Item | Symbol | Applicable Pin | Min. | Typ. | Max. | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| Input high level voltage | VIH | CL1, CL2, M, SHL, $\overline{E}$, D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$ | 0.7 × $V_{CC}$ | — | $V_{CC}$ | V | | |
| Input low level voltage | VIL | | 0 | — | 0.3 × $V_{CC}$ | V | | |
| Output high level voltage | VOH | $\overline{CAR}$, D0L, D1R | $V_{CC}$ – 0.4 | — | — | V | $I_{OH}$ = –0.4 mA | |
| Output low level voltage | VOL | $\overline{CAR}$, D0L, D1R | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| Vi-Yj on resistance | $R_{ON1}$ | Y1 to Y80, V1 to V4 | — | — | 2.0 | kΩ | $I_{ON}$ = 100 µA, $V_{CC} - V_{EE}$ = 28V | 1 and 5 |
| | $R_{ON2}$ | | — | — | 4.0 | kΩ | | 1 and 4 |
| Input leakage current (1) | $I_{IL1}$ | CL1, CL2, M, SHL, $\overline{E}$, D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$ | –5 | — | 5 | µA | VIN = $V_{CC}$ to GND | |
| Input leakage current (2) | $I_{IL2}$ | V1 to V4 | –25 | — | 25 | µA | VIN = $V_{CC}$ to $V_{EE}$ | |
| Consumption current (1) | $I_{GND1}$ | — | — | — | 3.0 | mA | $f_{CL2}$ = 8.0 MHz, $f_{CL1}$ = 50 kHz, $f_M$ = 2.3 kHz, $V_{CC}$ = 5V, $V_{CC} - V_{EE}$ = 28V, Checker data, FCS = high | 2 and 4 |
| Consumption current (2) | $I_{ST}$ | — | — | — | 200 | µA | | 2 to 4 |
| Consumption current (3) | $I_{EE1}$ | — | — | — | 500 | µA | | 2 and 4 |
| Consumption current (4) | $I_{GND2}$ | — | — | — | 100 | µA | $f_{CL1}$ = 50 kHz, $f_M$ = 2.3 kHz, $V_{CC}$ = 5V, $V_{CC} - V_{EE}$ = 28V, FCS = low | 2 and 5 |
| Consumption current (5) | $I_{EE2}$ | — | — | — | 500 | µA | | 2 and 5 |

**DC Characteristics 2 ($V_{CC}$ = 2.7 to 4.5V, GND = 0V, $V_{CC} - V_{EE}$ = 6 to 28V, and Ta = –20 to 75 °C, unless otherwise stated)**

| Item | Symbol | Applicable pin | Min. | Typ. | Max. | Unit | Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| Input high level voltage | VIH | CL1, CL2, M, SHL, $\overline{E}$, D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$ | $0.8 \times V_{CC}$ | — | $V_{CC}$ | V | | |
| Input low level voltage | VIL | | 0 | — | $0.2 \times V_{CC}$ | V | | |
| Output high level voltage | VOH | $\overline{CAR}$, D0L, and D1R | $V_{CC}$ – 0.4 | — | — | V | $I_{OH}$ = –0.4 mA | |
| Output low level voltage | VOL | $\overline{CAR}$, D0L, and D1R | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| Vi-Yj on resistance | $R_{ON1}$ | Y1 to Y80, and V1 to V4 | — | — | 2.0 | kΩ | $I_{ON}$ = 100 µA<br>$V_{CC} - V_{EE}$ = 2 8V | 1 and 5 |
| | $R_{ON2}$ | | — | — | 4.0 | kΩ | | 1 and 4 |
| Input leakage current (1) | $I_{IL1}$ | CL1, CL2, M, SHL, $\overline{E}$, D0L, D1R, D2, D3, FCS, TEST, and $\overline{DISPOFF}$ | –5 | — | 5 | µA | VIN = $V_{CC}$ to GND | |
| Input leakage current (2) | $I_{IL2}$ | V1 to V4 | –25 | — | 25 | µA | VIN = $V_{CC}$ to $V_{EE}$ | |
| Consumption current (1) | $I_{GND1}$ | — | — | — | 1.5 | mA | $f_{CL2}$ = 6.5 MHz<br>$f_{CL1}$ = 40.6 kHz<br>$f_M$ = 1.8 kHz<br>$V_{CC}$ = 3.0V<br>$V_{CC} - V_{EE}$ = 28V<br>Checker data<br>FCS = high | 2 and 4 |
| Consumption current (2) | $I_{ST}$ | — | — | — | 100 | µA | | 2 to 4 |
| Consumption current (3) | $I_{EE1}$ | — | — | — | 500 | µA | | 2 and 4 |
| Consumption current (4) | $I_{GND2}$ | — | — | — | 50 | µA | $f_{CL1}$ = 40.6 kHz<br>$f_M$ = 1.8 kHz<br>$V_{CC}$ = 3.0V<br>$V_{CC} - V_{EE}$ = 28V<br>FCS = low | 2 and 5 |
| Consumption current (5) | $I_{EE2}$ | — | — | — | 500 | µA | | 2 and 5 |

Notes: 1. Indicates the resistance between one pin from Y1 to Y80 and another pin from the V pins V1 to V4, when a load current is applied to the Y pin; defined under the following conditions:

In column driver operation

V1 and V3 = $V_{CC}$ – 2/10 ($V_{CC} - V_{EE}$)

V4 and V2 = $V_{EE}$ + 2/10 ($V_{CC} - V_{EE}$)

In common driver operation

V1 and V3 = $V_{CC}$ – 2/10 ($V_{CC} - V_{EE}$)

V4 and V2 = $V_{EE}$ + 2/10 ($V_{CC} - V_{EE}$)

V1 and V3 should be near the VCC level, and V4 and V2 should be near the $V_{EE}$ level. All these voltage pairs should be separated by less than Δ V, which is the range within which $R_{ON}$, the LCD drive circuits' output impedance, is stable. Note that Δ V depends on power supply voltage $V_{CC} - V_{EE}$. See Figure 10.

2. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, VIH and VIL must be held to $V_{cc}$ and GND, respectively.
3. $V_{cc}$ – GND current at standby ($\overline{E}$ input = high)
4. Applies to column driver operation.
5. Applies to common driver operation.

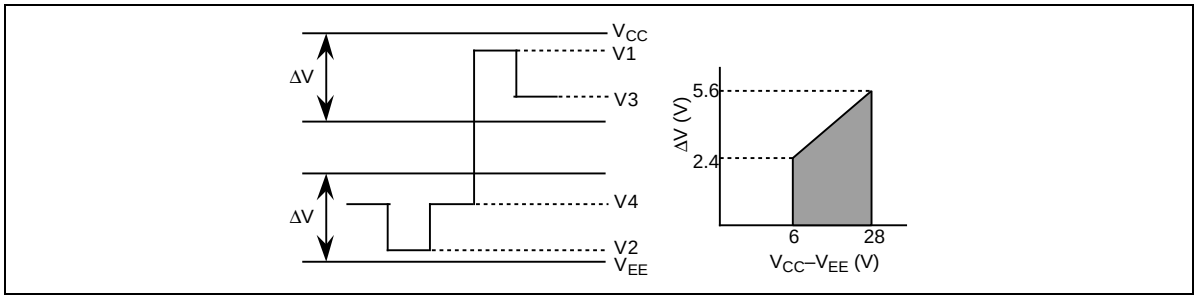


**Figure 10 Relationship between Driver Output Waveform and Level Voltages**

### Pin Configuration

Each pin configuration is shown below.

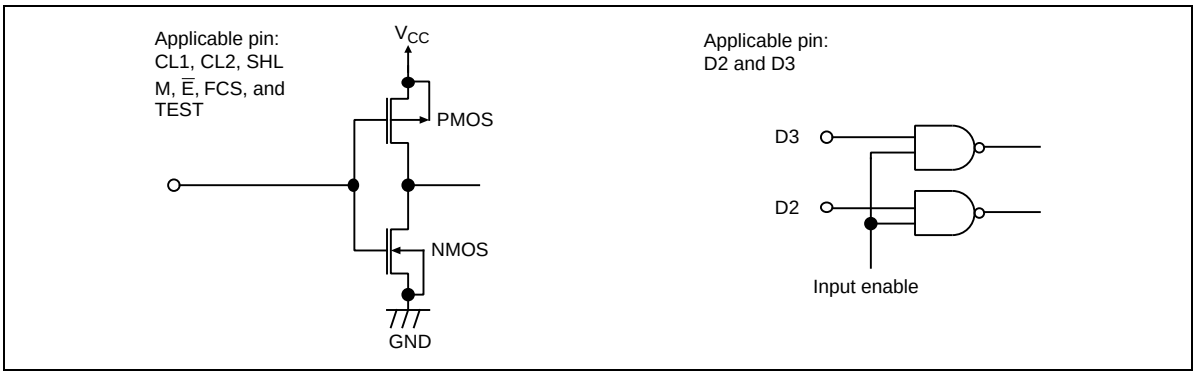


**Figure 11 Input Pin Configuration**

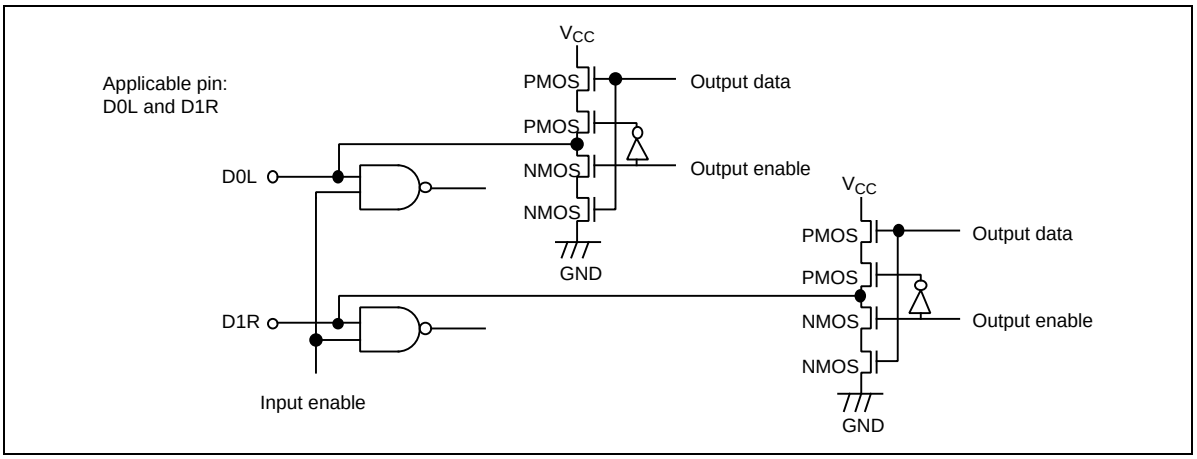


**Figure 12 Input/Output Pin Configuration**

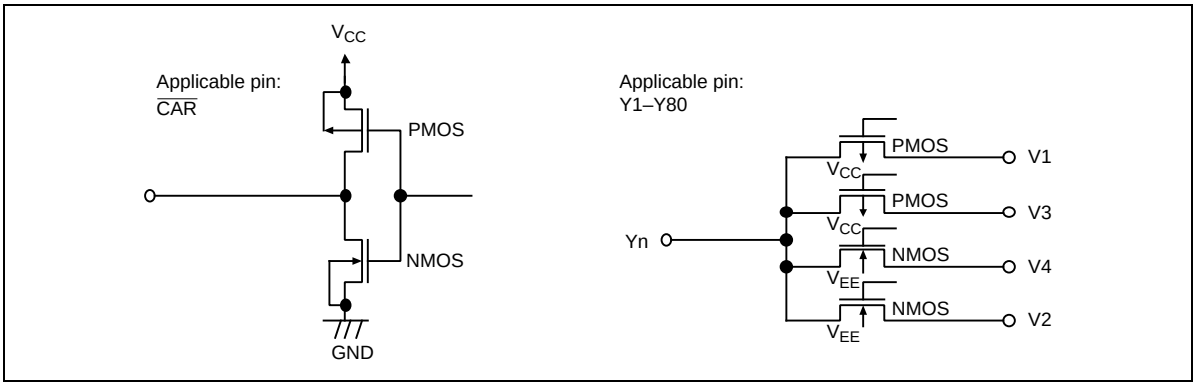


**Figure 13 Output Pin Configuration**

**AC Characteristics 1 (In Column Driver Operation) ($V_{CC}$ = 5V ± 10%, GND = 0V, $V_{CC}$ – $V_{EE}$ = 6 to 28V, and Ta = –20 to +75 ° C, unless otherwise stated)**

| Item | Symbol | Applicable Pins | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Clock cycle time | $t_{CYC}$ | CL2 | 125 | — | ns | |
| Clock high level width | $t_{CWH}$ | CL2 and CL1 | 40 | — | ns | |
| Clock low level width | $t_{CWL}$ | CL2 | 40 | — | ns | |
| Clock setup time | $t_{SCL}$ | CL1 and CL2 | 80 | — | ns | |
| Clock hold time | $t_{HCL}$ | CL1 and CL2 | 80 | — | ns | |
| Clock rise time | $t_r$ | CL1 and CL2 | — | 1 | ns | 1 |
| Clock fall time | $t_f$ | CL1 and CL2 | — | 1 | ns | 1 |
| Data setup time | $t_{DS}$ | D0L, D1R, D2, D3, and CL2 | 20 | — | ns | |
| Data hold time | $t_{DH}$ | D0L, D1R, D2, D3, and CL2 | 20 | — | ns | |
| Enable setup time | $t_{ESU}$ | $\overline{E}$ and CL2 | 20 | — | ns | |
| Carry output delay time | $t_{CAR}$ | $\overline{CAR}$ and CL2 | — | 70 | ns | 2 |
| M phase difference | $t_{CM}$ | M and CL1 | — | 300 | ns | |
| CL1 cycle time | $t_{CL1}$ | CL1 | $t_{CYC} \times 50$ | — | ns | |

**AC Characteristics 2 (In Column Driver Operation) ($V_{CC}$ = 2.7 to 4.5V, GND = 0V, $V_{CC}$ – $V_{EE}$ = 6 to 28V, and Ta = –20 to +75 ° C, unless otherwise stated)**

| Item | Symbol | Applicable pins | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Clock cycle time | $t_{CYC}$ | CL2 | 152 | — | ns | |
| Clock high level width | $t_{CWH}$ | CL2 and CL1 | 65 | — | ns | |
| Clock low level width | $t_{CWL}$ | CL2 | 65 | — | ns | |
| Clock setup time | $t_{SCL}$ | CL1 and CL2 | 80 | — | ns | |
| Clock hold time | $t_{HCL}$ | CL1 and CL2 | 120 | — | ns | |
| Clock rise time | $t_r$ | CL1 and CL2 | — | 1 | ns | 1 |
| Clock fall time | $t_f$ | CL1 and CL2 | — | 1 | ns | 1 |
| Data setup time | $t_{DS}$ | D0L, D1R, D2, D3, and CL2 | 50 | — | ns | |
| Data hold time | $t_{DH}$ | D0L, D1R, D2, D3, and CL2 | 50 | — | ns | |
| Enable setup time | $t_{ESU}$ | $\overline{E}$ and CL2 | 30 | — | ns | |
| Carry output delay time | $t_{CAR}$ | $\overline{CAR}$ and CL2 | — | 100 | ns | 2 |
| M phase difference | $t_{CM}$ | M and CL1 | — | 300 | ns | |
| CL1 cycle time | $t_{CL1}$ | CL1 | $t_{CYC} \times 50$ | — | ns | |

Notes: 1. Clock rise time ($t_r$) and clock fall time ($t_f$) must satisfy the following conditions:
$t_r$ and $t_f < (t_{CYC} – t_{CWH} – t_{CWL})/2$
$t_r$ and $t_f \leq 50$
2. Defined by connecting the load circuit shown in Figure 14.

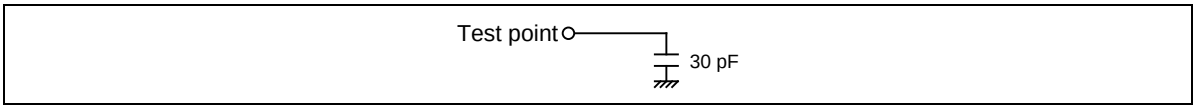


**Figure 14 Load Circuit**

**AC Characteristics 3 (In Common Driver Operation) ($V_{CC}$ = 2.7 to 5.5V, GND = 0V, $V_{CC}$ – $V_{EE}$ = 6 to 28V, and Ta = –20 to +75 ° C, unless otherwise stated)**

| Item | Symbol | Applicable Pins | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Clock cycle time | $t_{CYC}$ | CL2 | 10 | — | µs | |
| Clock high level width | $t_{CWH}$ | CL2 | 80 | — | ns | |
| Clock low level width | $t_{CWL}$ | CL2 | 1.0 | — | µs | |
| Clock rise time | $t_r$ | CL2 | — | 30 | ns | |
| Clock fall time | $t_f$ | CL2 | — | 30 | ns | |
| Data setup time | $t_{DS}$ | D0L, D1R, and CL2 | 100 | — | ns | |
| Data hold time | $t_{DH}$ | D0L, D1R, and CL2 | 100 | — | ns | |
| Data output delay time | $t_{DD}$ | D0L, D1R, and CL2 | — | 7.0 | µs | 1 |

Note: Defined by connecting the load circuit shown in Figure 15.

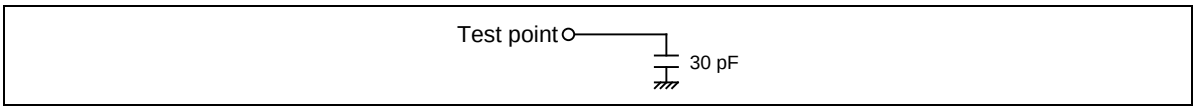


**Figure 15 Load Circuit**

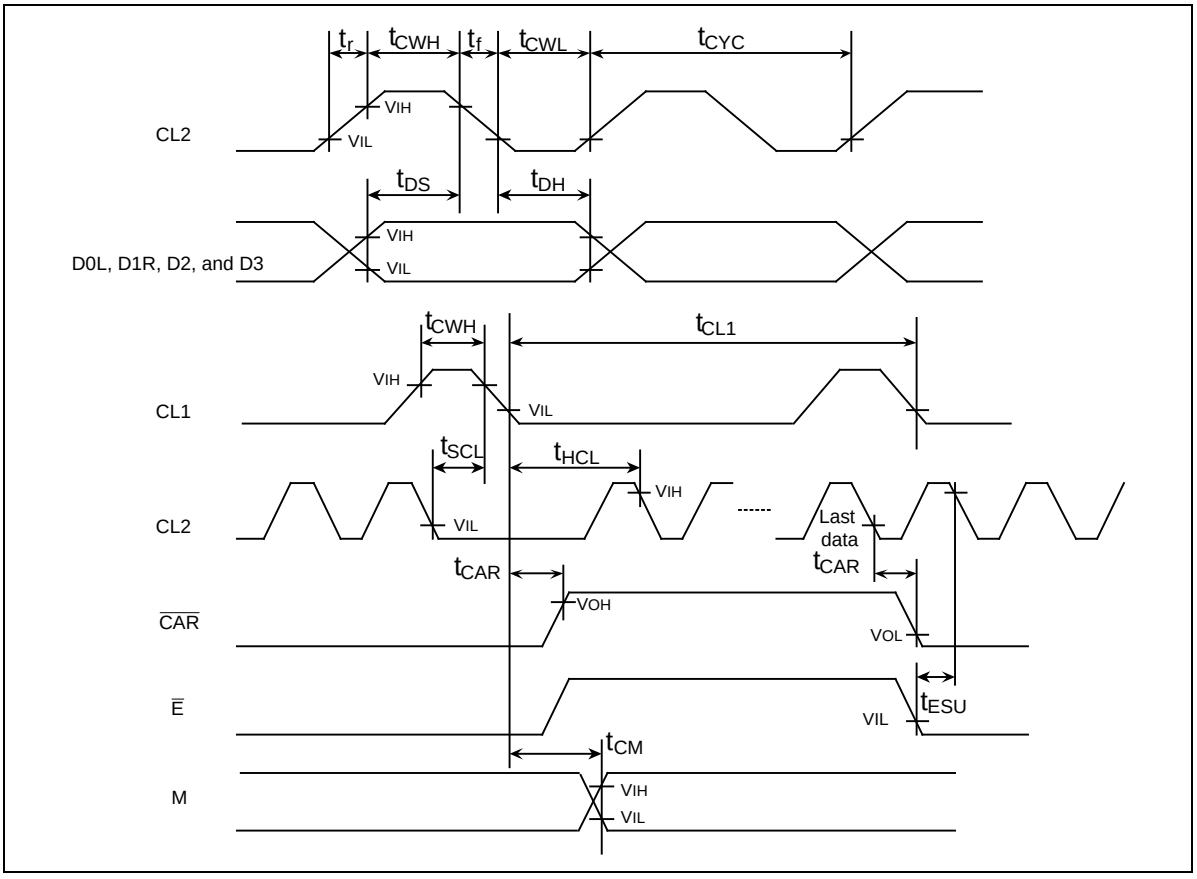


**Figure 16 Common Driver Operation Timing**

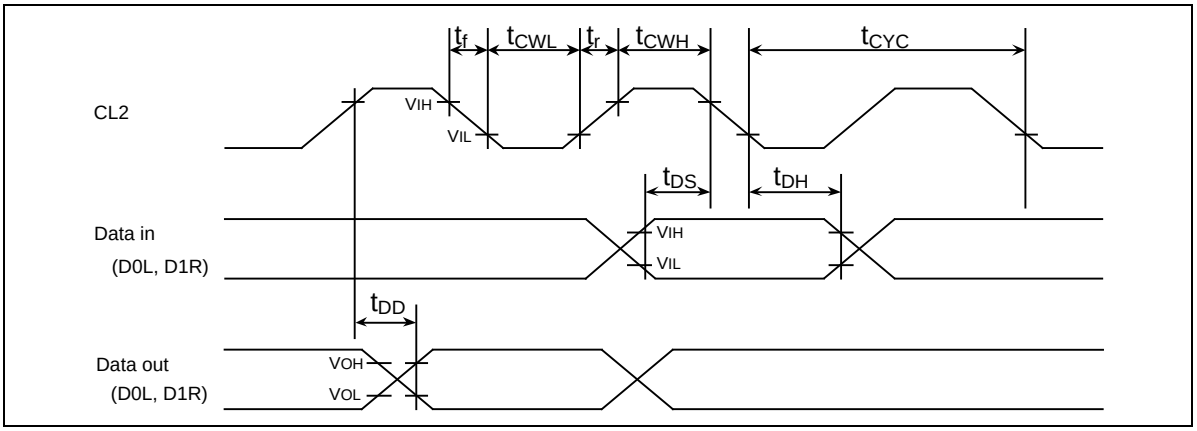


**Figure 17 Common Driver Operation Timing**