

# Reconfigurable Content-Based Router Using Hardware-Accelerated Language Parse

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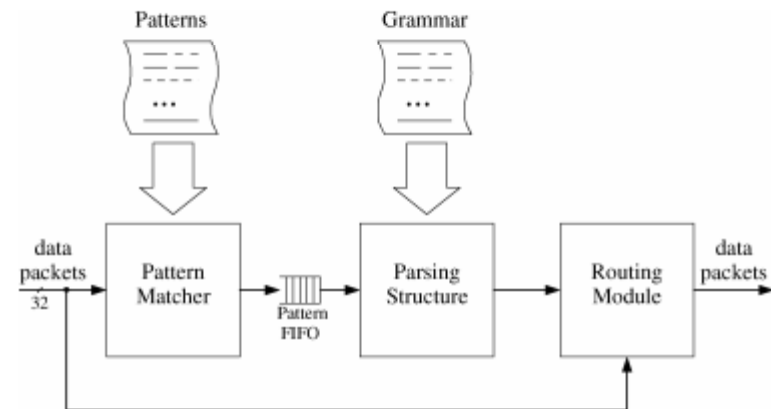


# High Speed Pattern Matching

- Increased need for fast and flexible pattern matcher
- A new **high-speed** architecture that is both scalable and capable of searching for regular expressions.
- A technique for mapping regular grammars directly onto FPGA hardware
- This idea used to develop a content-based router that is capable of multi-gigabit speed
- Focus on:
  - Hardware-accelerated pattern matching and parsing
  - Hardware-accelerated Language Parsing
  - Content based routing module

# Content based router architecture

- The format of packets to be routed are specified using grammars and XML is format to exchange information over networks.
- To do the content based routing , the router consists of 2 extra modules that are the **Parsing structure** and the **Routing Module**.
- The generated **Parsing structure** processes packets one pattern at a time. During processing, all signals from the pattern matcher sent to the routing module accompanied by the state of the parsing structure which indicates where in the grammar each pattern is found that allows the routing module to make more intelligent decisions.



# Question

*Why was there a need for Hardware-Accelerated Language Parser in a Content based Router?*

- *High Speed due to Hardware*
- *Most of the work before was based on performance and size of pattern matchers, which was not at sufficient for application such as NIDS and content based routing.*
- *Pattern based matchers concepts based on Pre-decoded Character Bits, Pipelined Regular Expression Chain, Pipeline character Grid and Time Segment matching determine if a given pattern is present in a packet without considering the context of the pattern in the data stream.*
- *It required a higher level of understanding of the data inside the packet with the use of a Parser inside our system. This higher level of understanding for reducing the no. of false positives.*