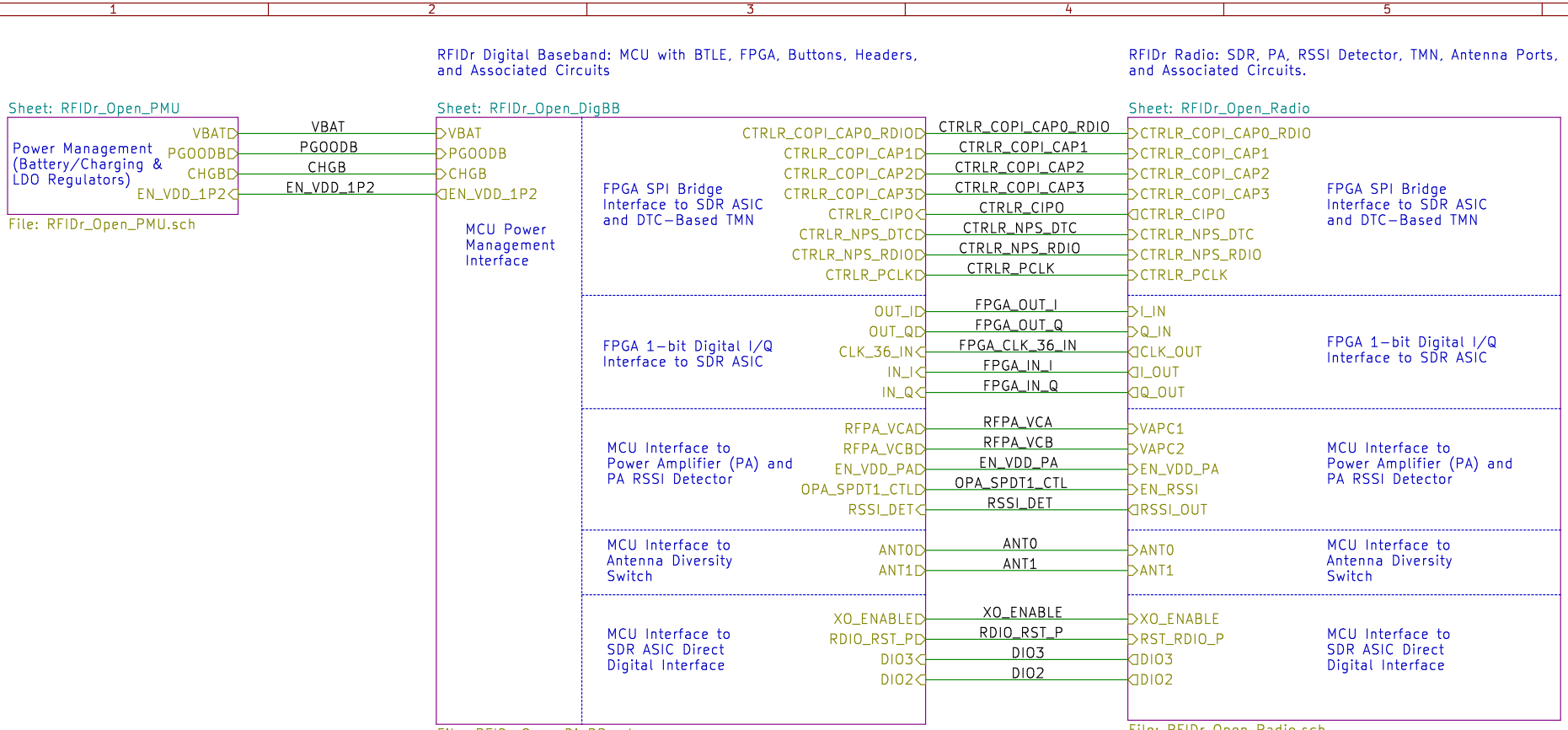
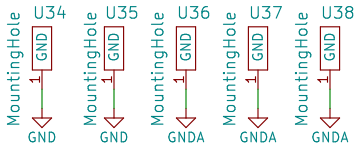
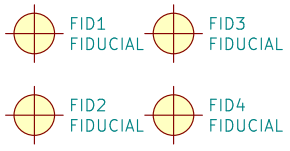


Mounting Holes for Standoffs



Fiducials for Pick and Place Assembly Alignment



Schematic Summary: Top Level

This is the top level of the RFIDr reader design.
Subschematics are:
- PMU (Power Management Unit)
- Digital Baseband (MCU, FPGA, other associated circuits)
- Radio (Software-Defined Radio, Power Amplifier, Tunable Microwave Network, etc.)

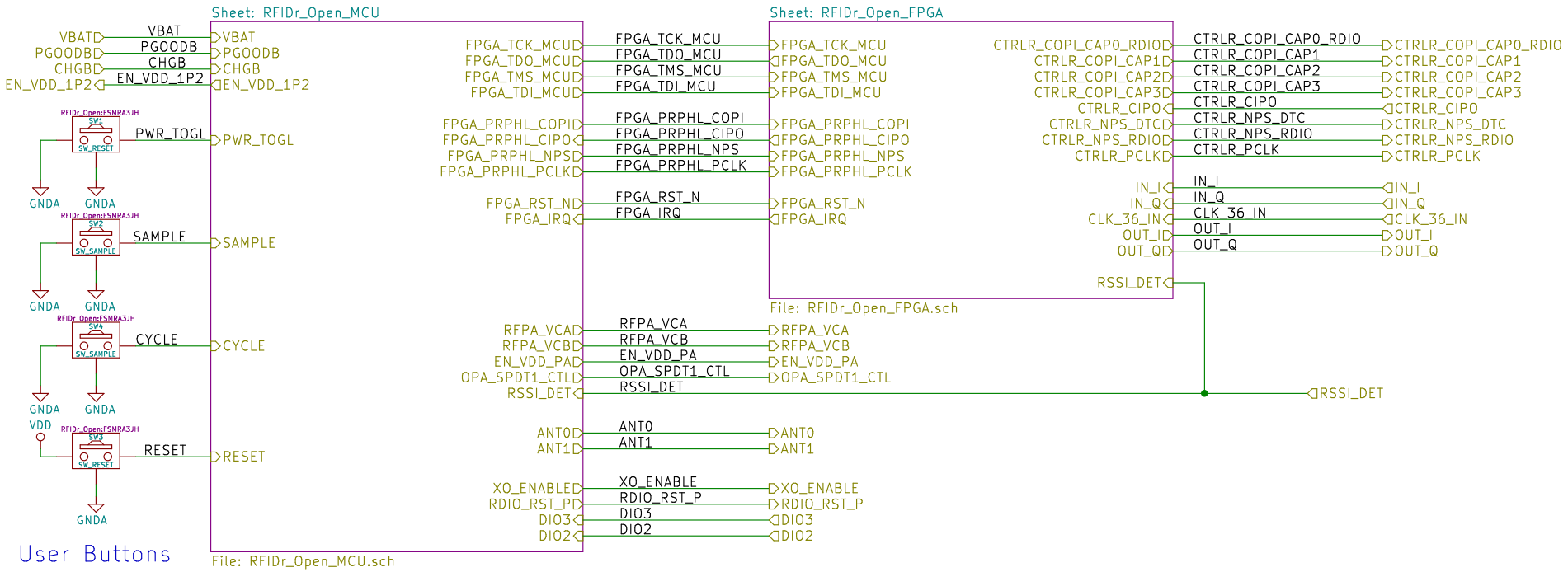
Superlative Semiconductor LLC

Sheet: /
File: RFIDr_Open_Top.sch

Title: RFIDr Top Level

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/17

Schematic Summary: DigBB
This schematic is another high-level schematic which separates the MCU and the FPGA. The FPGA performs all of the real-time digital baseband operations of the RFIDr reader, while the MCU performs less time-critical, but more behaviorally complex operations.



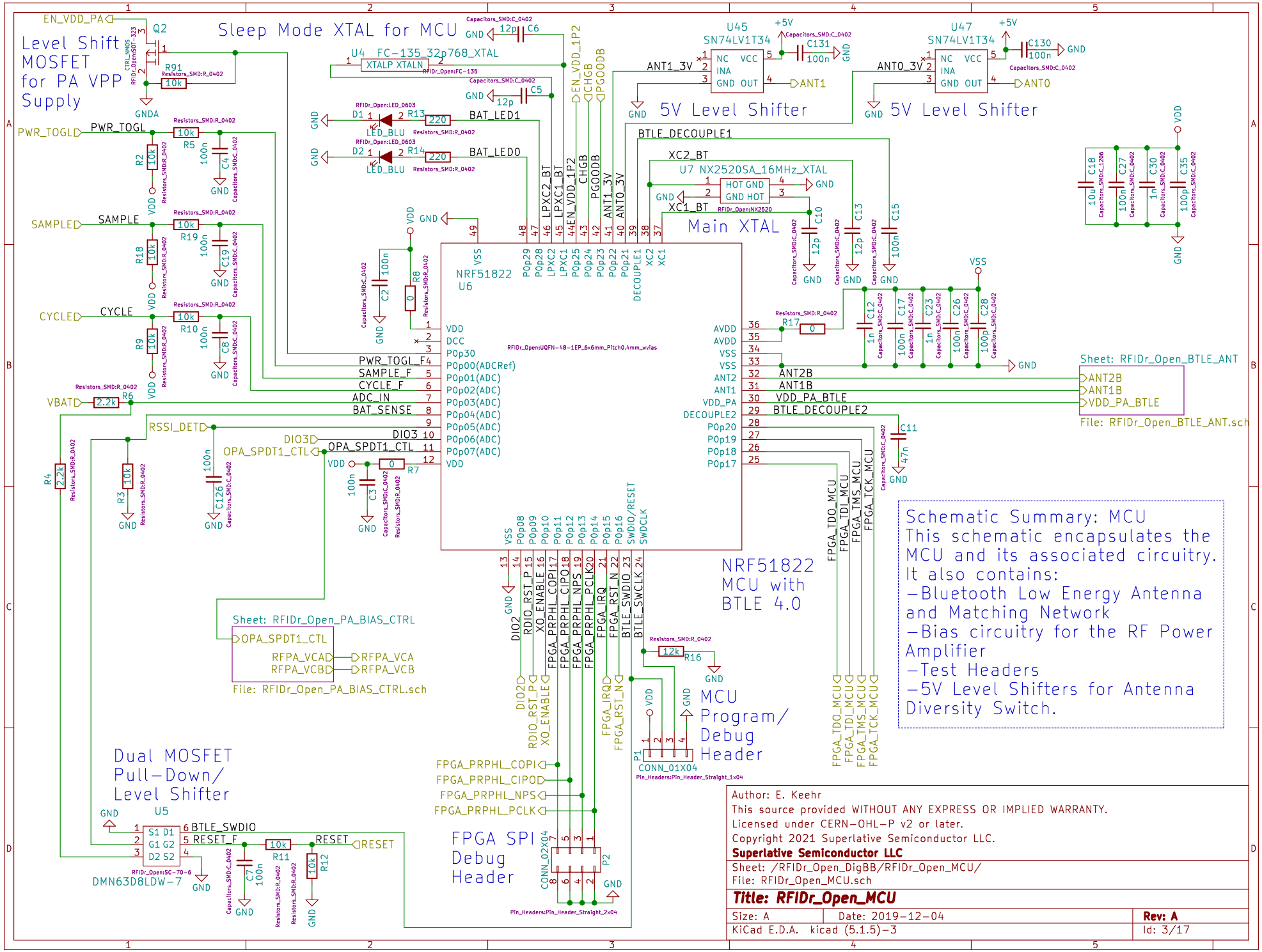
Design Note:
The user buttons were added in when it was thought that the RFIDr reader may become a consumer product.
Power toggle was to turn the reader on/off.
Sample was to search for a particular tag.
Cycle was to cycle through a list of items in a smartphone app.
Reset was to reset, of course.

Superlative Semiconductor LLC

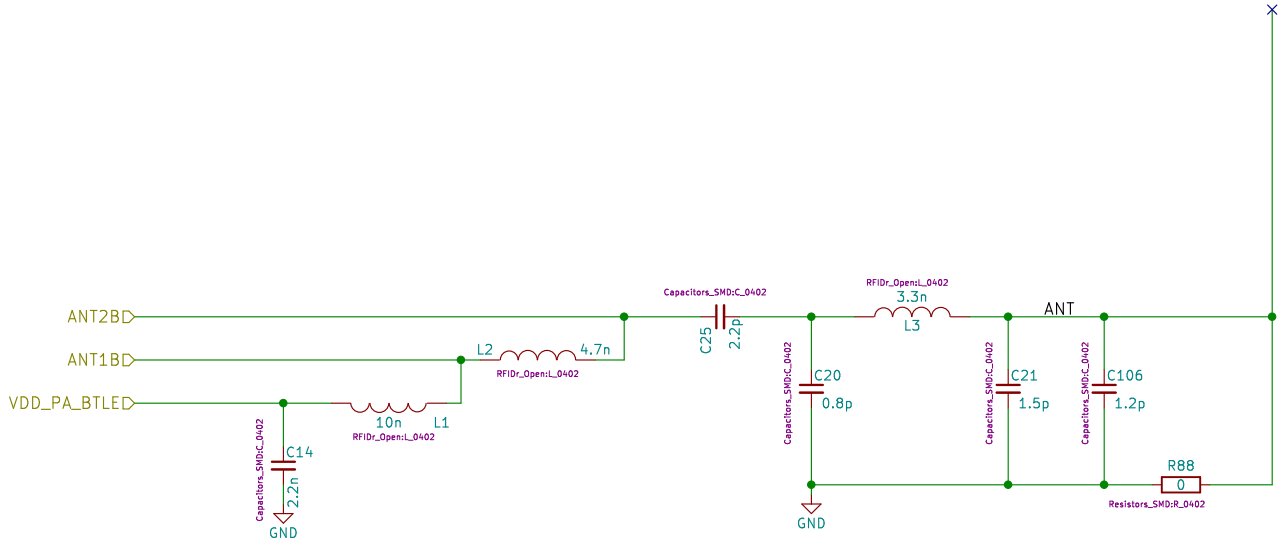
Sheet: /RFIDr_Open_DigBB/
File: RFIDr_Open_DigBB.sch

Title: RFIDr_Open_DigBB

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/17


Level Shift MOSFET for PA VPP Supply
Sleep Mode XTAL for MCU
5V Level Shifter
5V Level Shifter
Main XTAL
NRF51822 MCU with BTLE 4.0
Schematic Summary: MCU
This schematic encapsulates the MCU and its associated circuitry. It also contains:
–Bluetooth Low Energy Antenna and Matching Network
–Bias circuitry for the RF Power Amplifier
–Test Headers
–5V Level Shifters for Antenna Diversity Switch.
Dual MOSFET Pull–Down/ Level Shifter
FPGA SPI Debug Header
MCU Program/ Debug Header
Sheet: RFIDr_Open_PA_BIAS_CTRL
File: RFIDr_Open_PA_BIAS_CTRL.sch
Sheet: RFIDr_Open_BTLE_ANT
File: RFIDr_Open_BTLE_ANT.sch
Author: E. Keehr
This source provided WITHOUT ANY EXPRESS OR IMPLIED WARRANTY.
Licensed under CERN–OHL–P v2 or later.
Copyright 2021 Superlative Semiconductor LLC.
Superlative Semiconductor LLC
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_MCU/
File: RFIDr_Open_MCU.sch
Title: RFIDr_Open_MCU
Size: A
Date: 2019–12–04
Rev: A
KiCad E.D.A. kicad (5.1.5)–3
Id: 3/17

Design Note: Metallization on net "ANT" should realize an inverted-F antenna.



Schematic Summary: BTLE_ANT
Here, we follow the recommended matching network from the Nordic PCA10001 Development PCB (antenna is a bit different).

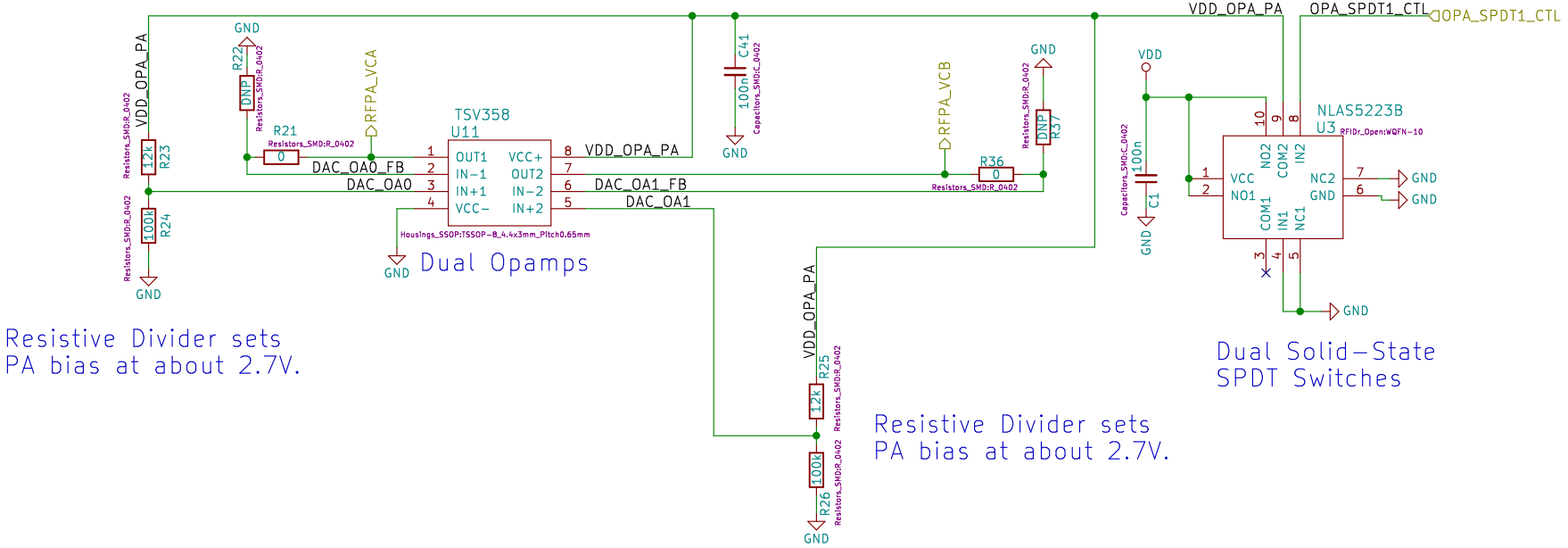
Superlative Semiconductor LLC

Sheet: /RFIDr_Open_DigBB/RFIDr_Open_MCU/RFIDr_Open_BTLE_ANT/
File: RFIDr_Open_BTLE_ANT.sch

Title: RFIDr_Open_BTLE_ANT

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/17

Schematic Summary: PA BIAS Control
In this schematic, bias voltages for the PA are generated via resistor strings and unity-gain biased opamps.
It was intended in the future that the PA bias be made adjustable on-the-fly, but
this was a way it could be made easily adjustable by changing a resistor divider.
The resistive dividers could use capacitive decouping to ground at the output
voltage node, but tests have shown this makes no difference to reader performance.



Superlative Semiconductor LLC

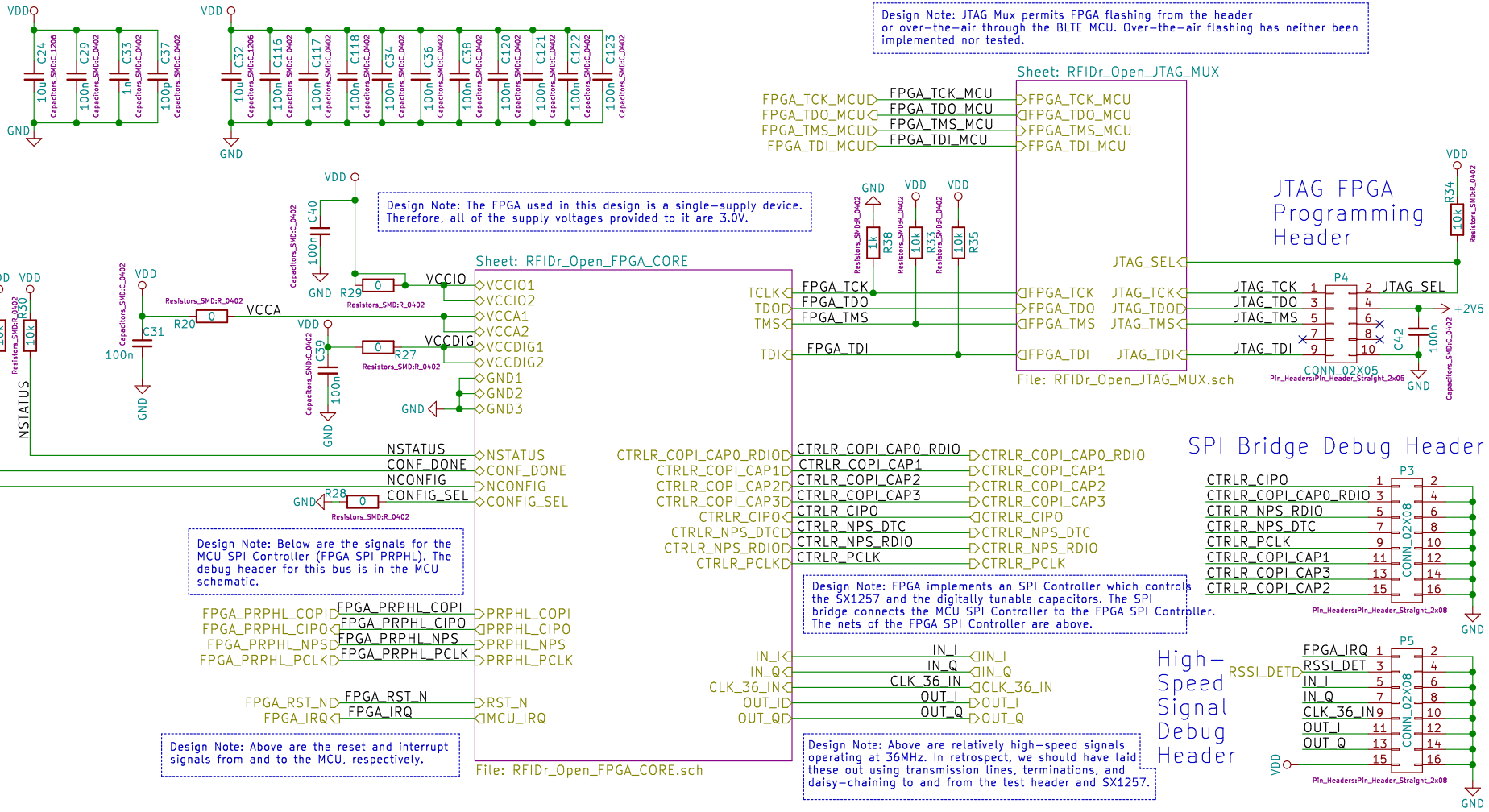
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_MCU/RFIDr_Open_PA_BIAS_CTRL/
File: RFIDr_Open_PA_BIAS_CTRL.sch

Title: RFIDr_Open_PA_BIAS_CTRL

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/17

Schematic Summary: FPGA

This schematic simplifies the set of nets interfacing the FPGA to the rest of the reader.
The real-time digital back end of the RFID reader's software-defined radio resides on the FPGA.

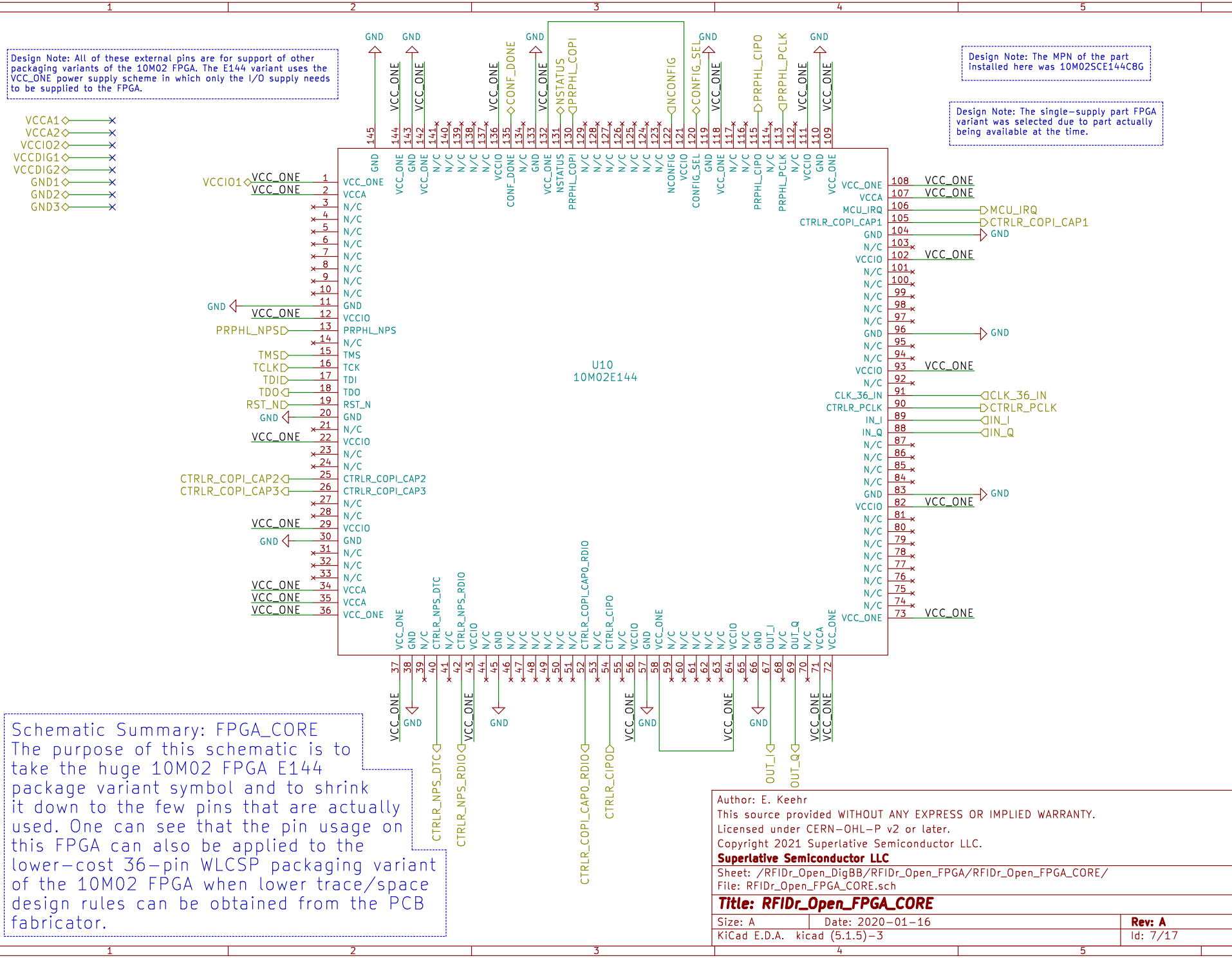


Superlative Semiconductor LLC

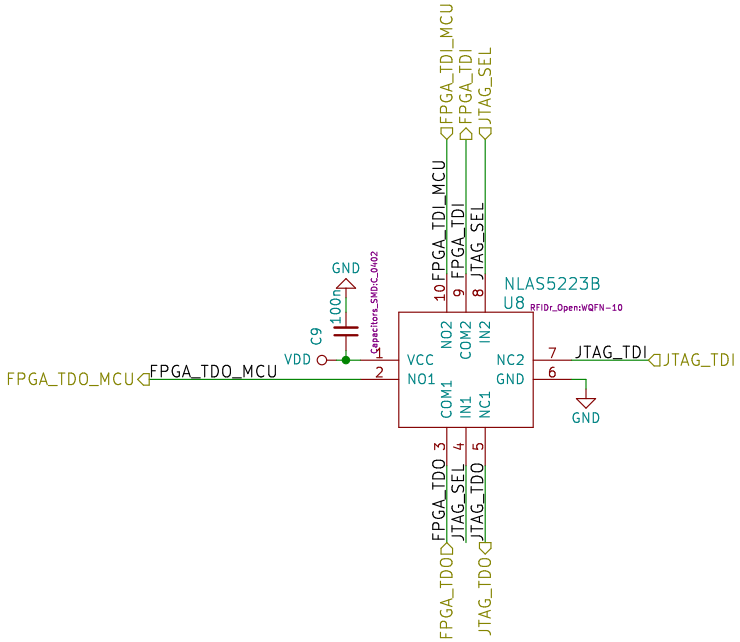
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_FPGA/
File: RFIDr_Open_FPGA.sch

Title: RFIDr_Open_FPGA

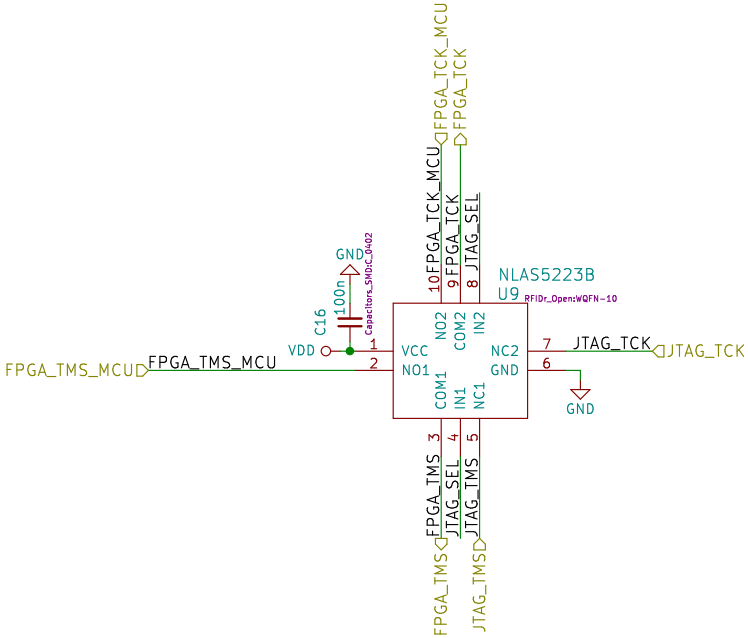
Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 6/17


Design Note: All of these external pins are for support of other packaging variants of the 10M02 FPGA. The E144 variant uses the VCC_ONE power supply scheme in which only the I/O supply needs to be supplied to the FPGA.
Design Note: The MPN of the part installed here was 10M02SCE144C8G
Design Note: The single-supply part FPGA variant was selected due to part actually being available at the time.
U10
10M02E144
VCCA1
VCCA2
VCCIO2
VCCDIG1
VCCDIG2
GND1
GND2
GND3
VCCIO1
PRPHL_NPS
TMS
TCLK
TDI
TDO
RST_N
CTRLR_COPI_CAP2
CTRLR_COPI_CAP3
MCU_IRQ
CTRLR_COPI_CAP1
CLK_36_IN
CTRLR_PCLK
IN_I
IN_Q
OUT_I
OUT_Q
CTRLR_NPS_DTC
CTRLR_NPS_RDIO
CTRLR_COPI_CAP0_RDIO
CTRLR_CIPO
Schematic Summary: FPGA_CORE
The purpose of this schematic is to take the huge 10M02 FPGA E144 package variant symbol and to shrink it down to the few pins that are actually used. One can see that the pin usage on this FPGA can also be applied to the lower-cost 36-pin WLCSP packaging variant of the 10M02 FPGA when lower trace/space design rules can be obtained from the PCB fabricator.
Author: E. Keehr
This source provided WITHOUT ANY EXPRESS OR IMPLIED WARRANTY.
Licensed under CERN-OHL-P v2 or later.
Copyright 2021 Superlative Semiconductor LLC.
Superlative Semiconductor LLC
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_FPGA/RFIDr_Open_FPGA_CORE/
File: RFIDr_Open_FPGA_CORE.sch
Title: RFIDr_Open_FPGA_CORE
Size: A
Date: 2020-01-16
Rev: A
KiCad E.D.A. kicad (5.1.5)-3
Id: 7/17

Schematic Summary: JTAG MUX
This pair of dual solid-state switches permits programming of the FPGA either through an onboard header, or over-the-air through the MCU. So far, over-the-air FPGA reprogramming has not been implemented or tested.



Dual Solid-State SPDT Switches



Dual Solid-State SPDT Switches

Superlative Semiconductor LLC

Sheet: /RFIDr_Open_DigBB/RFIDr_Open_FPGA/RFIDr_Open_JTAG_MUX/
File: RFIDr_Open_JTAG_MUX.sch

Title: RFIDr_Open_JTAG_MUX

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/17

POWER TREE: [USB_VBUS (5V)] ->1019mA -> [VCC (4.4V)] -----> 850mA -> [VPP (Switched 4.4V)] -> 850mA -> [RF Power Amplifier]
|
V -> 10mA -> [2 LEDs]
|
V -> about 0mA -> [+2V5] -> about 0mA -> [+5V] -> [Level shifters for antenna diversity switch control (MCU Schematic)]
|
V -> about 0mA -> [+1V2] -> Not used here, used for other 10M02 FPGA package variants.
|
V -> 159.3mA -> [VDD (3.0V) - Digital Supply] -----> 32.5mA ->[FPGA]
|
V --> 18mA -> [3 LEDs]
|
V --> 5mA -> [MCU Digital]
|
V --> 16mA -> [VSS (3.0V)] -> 16mA -> [MCU BTLE Radio PA]
|
V --> 87.8mA -> [VAA (3.0V)] -----> 85mA -> [SX1257 SDR ASIC Max Power]
|
V --> 2.2mA -> [XTAL OSC]
|
V --> 0.6mA -> [DTC-Based TMN]

Schematic Summary: PMU (Power Management Unit)

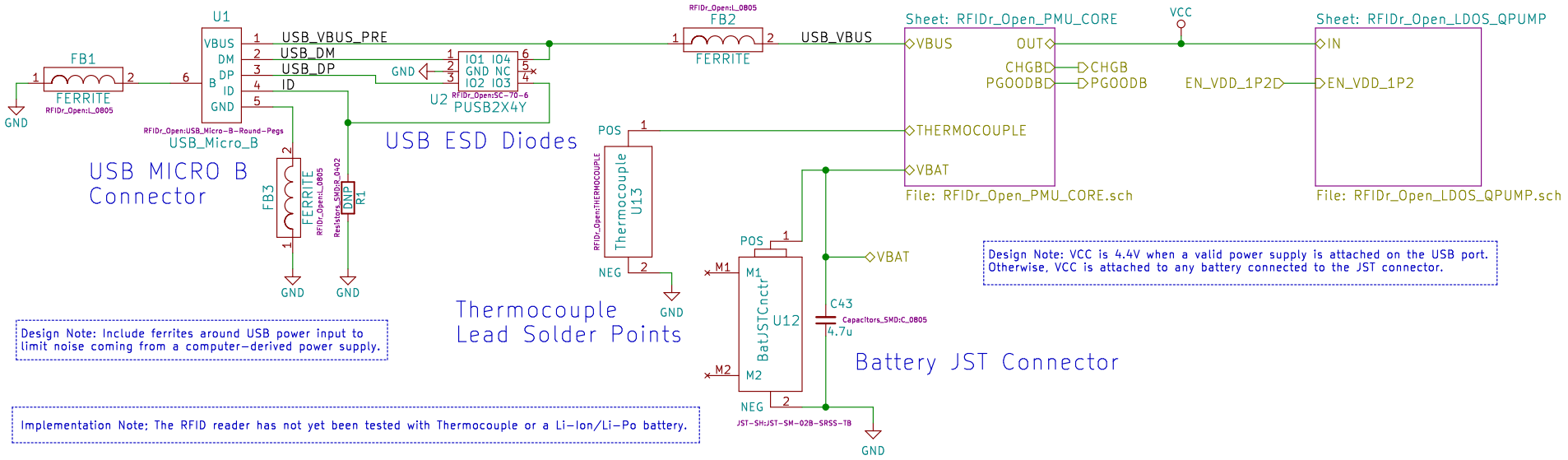
This schematic is the top level of the power management on the RFIDr reader.

Subunits include:

- USB Micro-B Charging port (this schematic)
- Li-Ion battery and thermcouple access (this schematic)
- PMU CORE (BQ24073 charging chip and associated passives)
- LDOS/QPUMP (LDOs and Charge Pump for derived supply voltages)

Implementation Note: The BQ24073 power management chip can accept 4.35V to 6.6V on VBUS. Typical VBUS value is 5V.

Layout Note: USB_VBUS, USB_VBUS_PRE, VCC, and VBAT lines should all be sized to carry about 1.5A of current. The BQ24073 power management chip limits input current to about 1.36A.

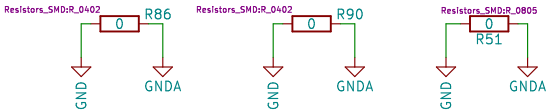


Design Note: Include ferrites around USB power input to limit noise coming from a computer-derived power supply.

Design Note: VCC is 4.4V when a valid power supply is attached on the USB port. Otherwise, VCC is attached to any battery connected to the JST connector.

Implementation Note: The RFID reader has not yet been tested with Thermocouple or a Li-Ion/Li-Po battery.

Design Note: These resistors contact digital ground (GND) to analog ground (GNDA). This is done in a quasi-star ground configuration where the analog ground/supply (VAA) is derived from the digital 3.0V supply (VDD) due to layout constraints (namely digital circuitry being in between the power and analog circuitries).



Superlative Semiconductor LLC

Sheet: /RFIDr_Open_PMU/
File: RFIDr_Open_PMU.sch

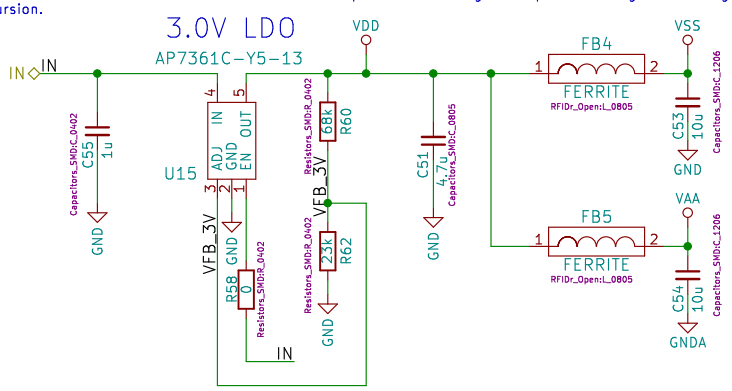
Title: RFIDr_Open_PMU

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/17

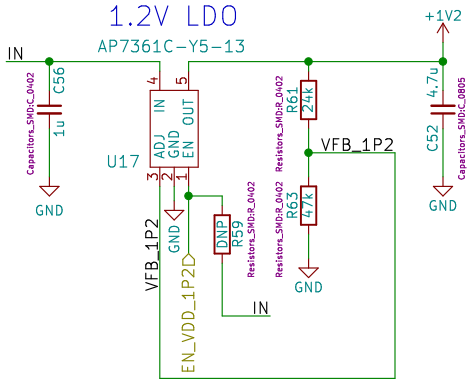
Schematic Summary: LDOS_QPUMP

This schematic contains several LDOs and a charge pump which are used to derive various supplies for the RFIDr reader.

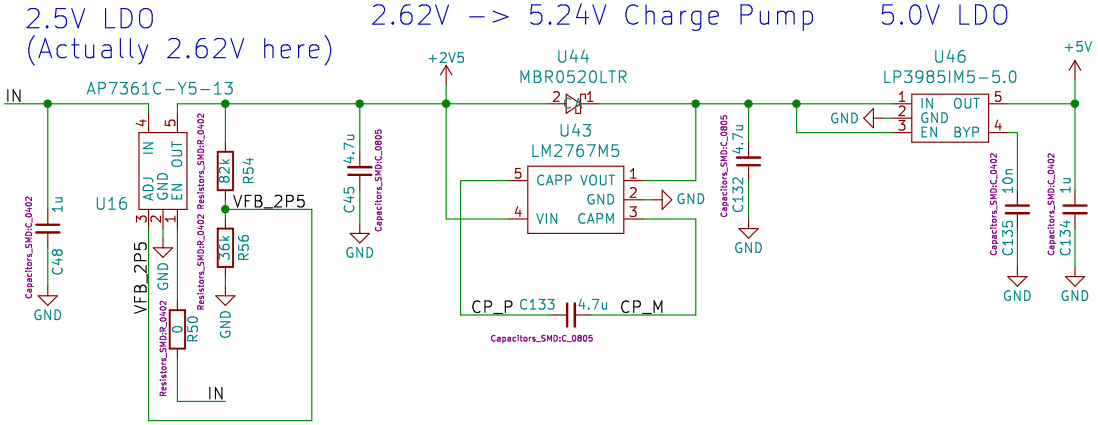
Design Note: VDD, VSS, and VAA are 3.0V supplies that supply the bulk of the analog and I/O circuits around the RFID reader.
See the Power Tree at the next highest schematic up in the hierarchy for more details.
The 3.0V level was chosen because it is the minimum acceptable for the digital chipset, allowing for the largest battery voltage excursion.



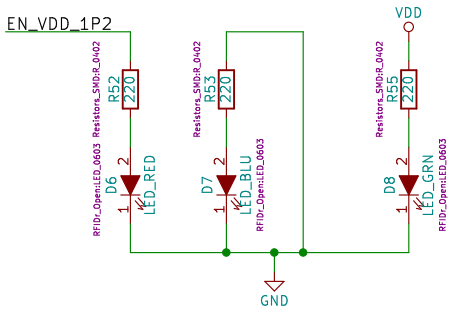
Design Note: The 1.2V LDO isn't used in this design. It's just in place for when the FPGA is swapped out with the lower-cost WLCSP 10M02 variant which does not use a single-supply scheme.



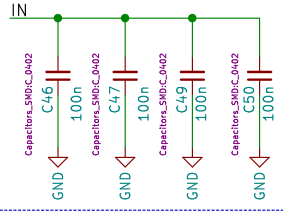
Design Note: The 2.5V supply supplies the JTAG interface and a 2.5V -> 5V charge pump.
The 5V charge pump is critical for achiving low distortion on the antenna diversity switch while still being able to operate the system off of a battery.
The 2.5V supply is also used for different 10M02 packaging variants.



Diagnostic LEDs



Local Decoupling Caps



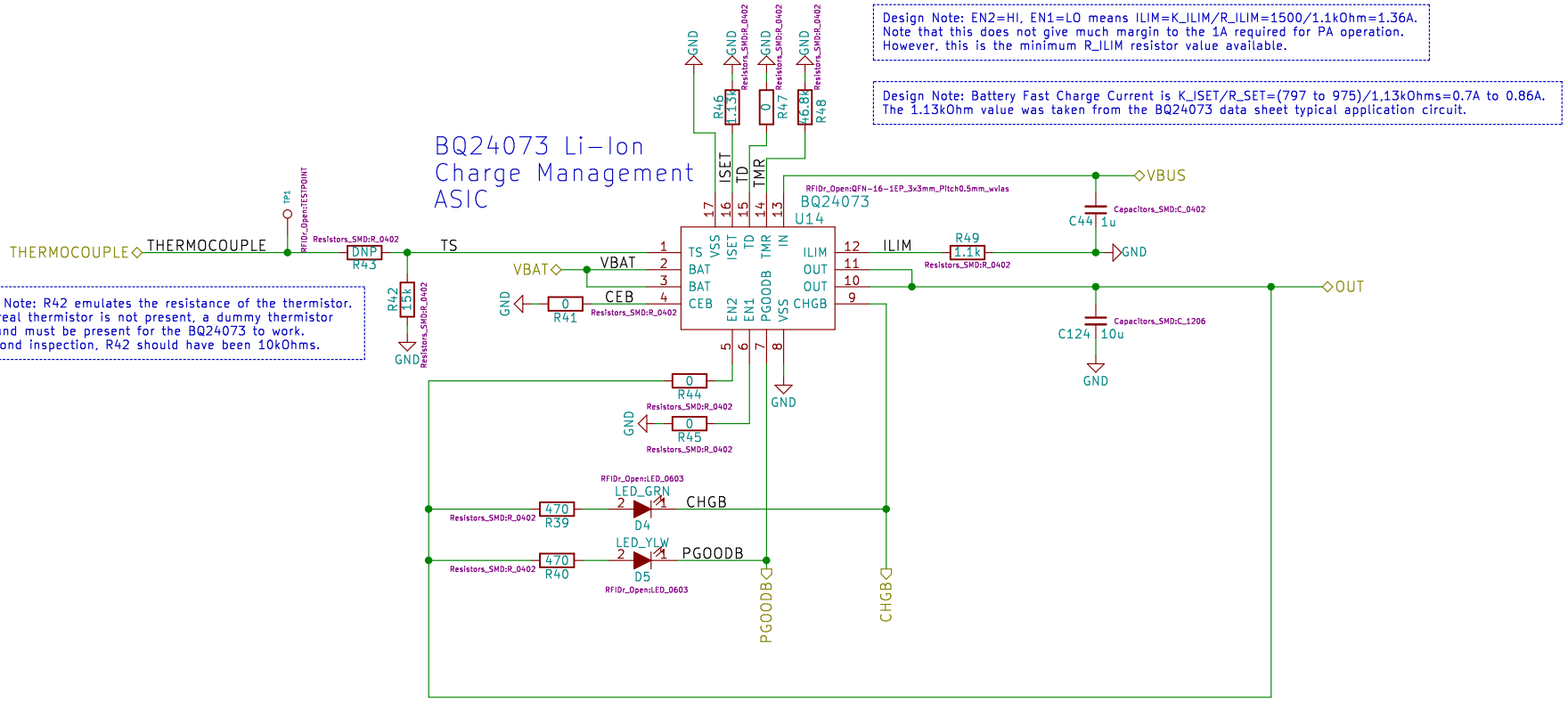
Superlative Semiconductor LLC

Sheet: /RFIDr_Open_PMU/RFIDr_Open_LDOS_QPUMP/
File: RFIDr_Open_LDOS_QPUMP.sch

Title: RFIDr_Open_LDOs_QPUMP

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 10/17

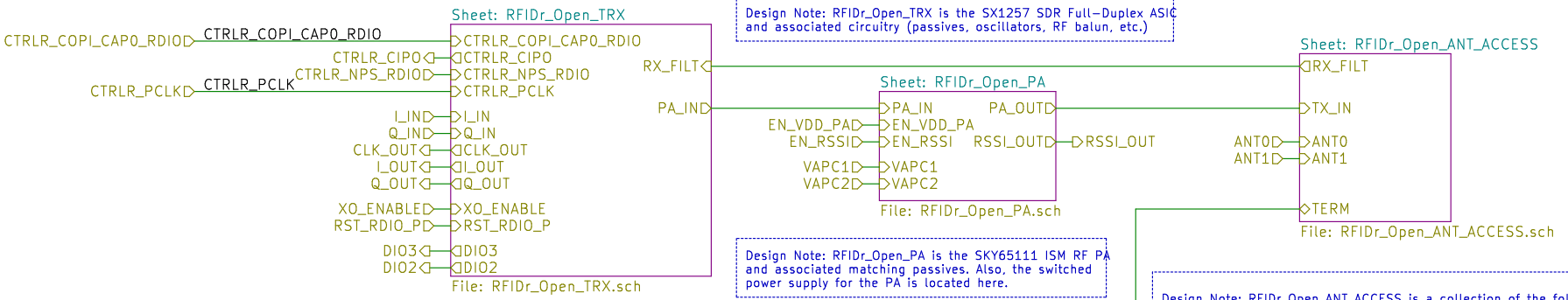
Schematic Summary: PMU_CORE
This schematic encapsulates the BQ24073 and its associated passives. BQ24073 is an integrated Li-Ion charging solution which accepts power from a 5V source which it can use to charge a battery or to power a device. In the absence of external power, the BQ24073 routes battery power to the device's internal circuity. Operation of the reader with battery has not yet been tested.

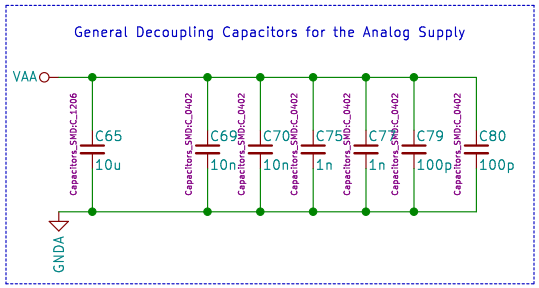


Author: E. Keehr	
This source provided WITHOUT ANY EXPRESS OR IMPLIED WARRANTY.	
Licensed under CERN-OHL-P v2 or later.	
Copyright 2021 Superlative Semiconductor LLC.	
Superlative Semiconductor LLC	
Sheet: /RFIDr_Open_PMU/RFIDr_Open_PMU_CORE/	
File: RFIDr_Open_PMU_CORE.sch	
Title: RFIDr_Open_PMU_CORE	
Size: A	Date: 2020-05-21
KiCad E.D.A. kicad (5.1.5)-3	Id: 11/17

Rev: A

Schematic Summary: Radio
This schematic contains all of the circuitry operating at radio frequencies.
In addition, layout in this area is done with substantial ground shielding to promote RF isolation between various blocks in this subschematic.
Subschematics include:
TRX: The Transmit/Receive Software Defined Radio ASIC and associated circuits.
PA: The Power Amplifier.
ANT_ACCESS: Various components supporting access to the antenna by the PA and SDR ASICs.
ReflNW: Reflection Network – a Tunable Microwave Network which enables TX cancellation.
RF_VIAS: RF Vias for ground shielding.





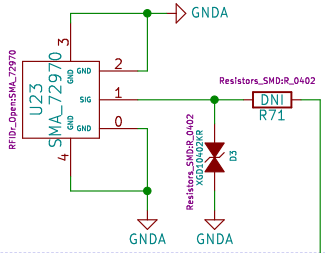
Superlative Semiconductor LLC

Sheet: /RFIDr_Open_Radio/
File: RFIDr_Open_Radio.sch

Title: RFIDr_Open_Radio

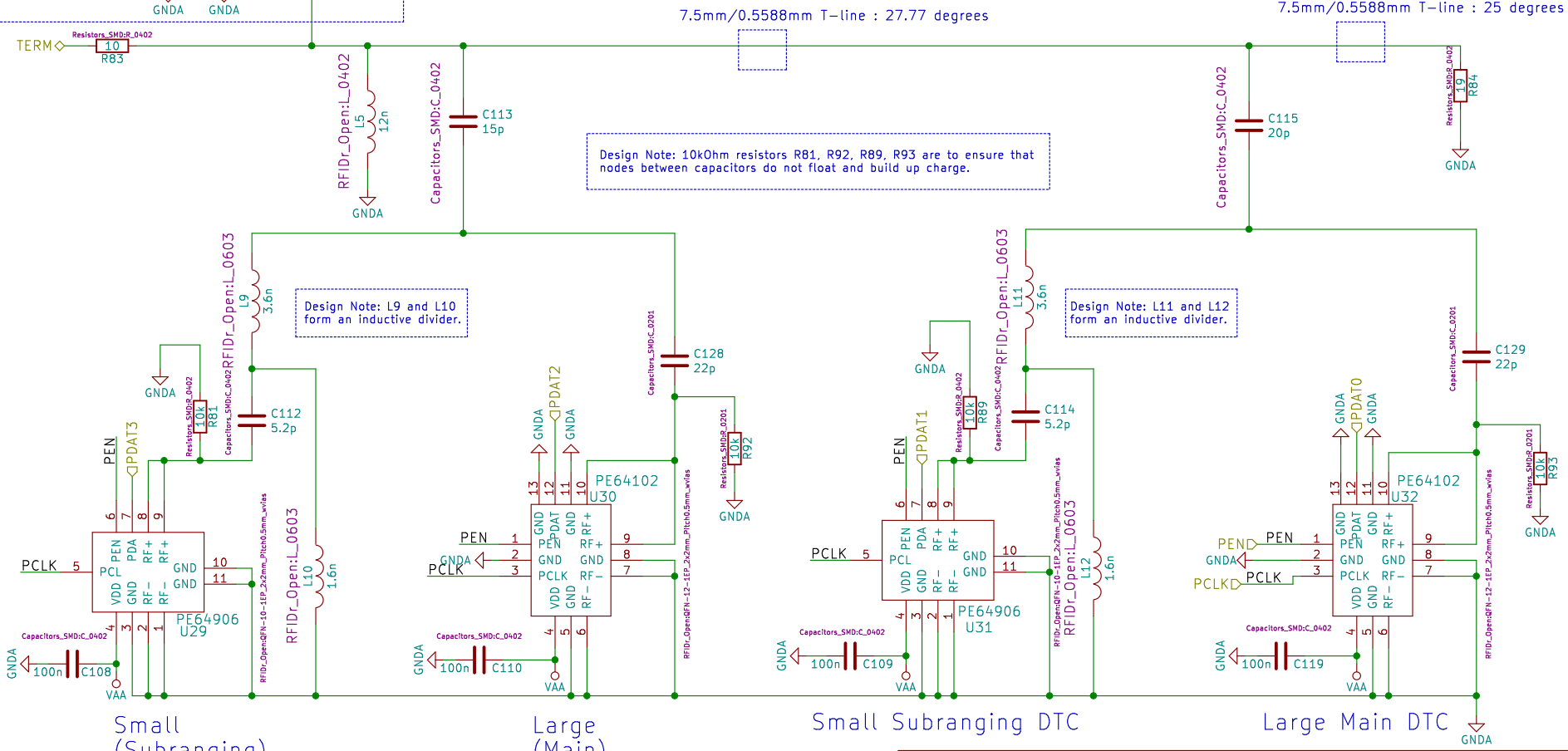
Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 12/17

Design Note: This port is used to characterize the Tunable Microwave Network when R71 is populated and R83 is DNIed.



Schematic Summary: RefINW (Reflection Network)

This is the Tunable Microwave Network, which is covered in more detail here: https://ieeexplore.ieee.org/document/8376194.
It is comprised of 4 digital tunable capacitors along with inductive dividers designed such that the small DTCs subrange the large ones for enhanced resolution for generating a TX cancellation signal.

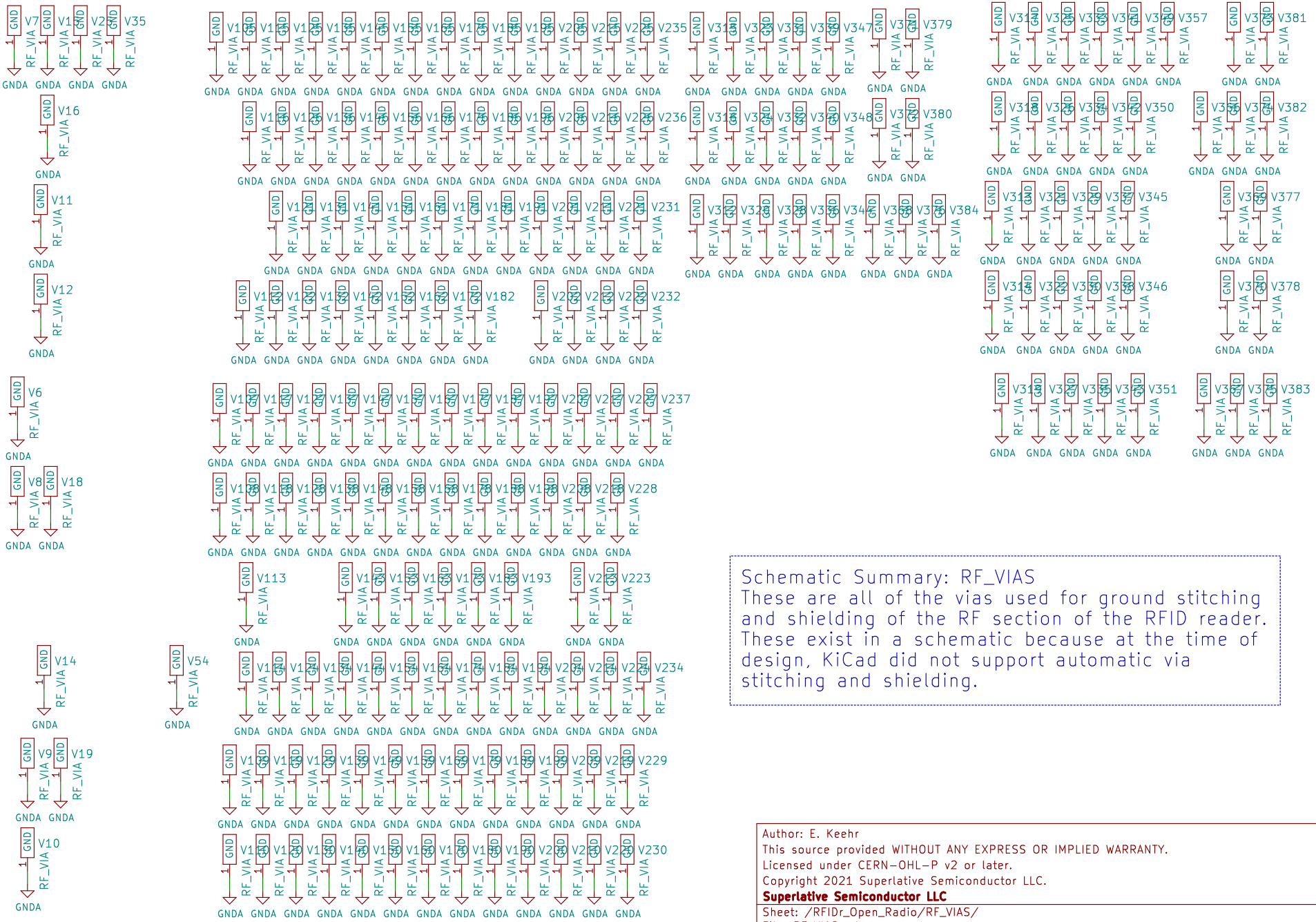


Superlative Semiconductor LLC

Sheet: /RFIDr_Open_Radio/RFIDr_Open_RefINW/
File: RFIDr_Open_RefINW.sch

Title: RFIDr_Open_RefINW

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 13/17

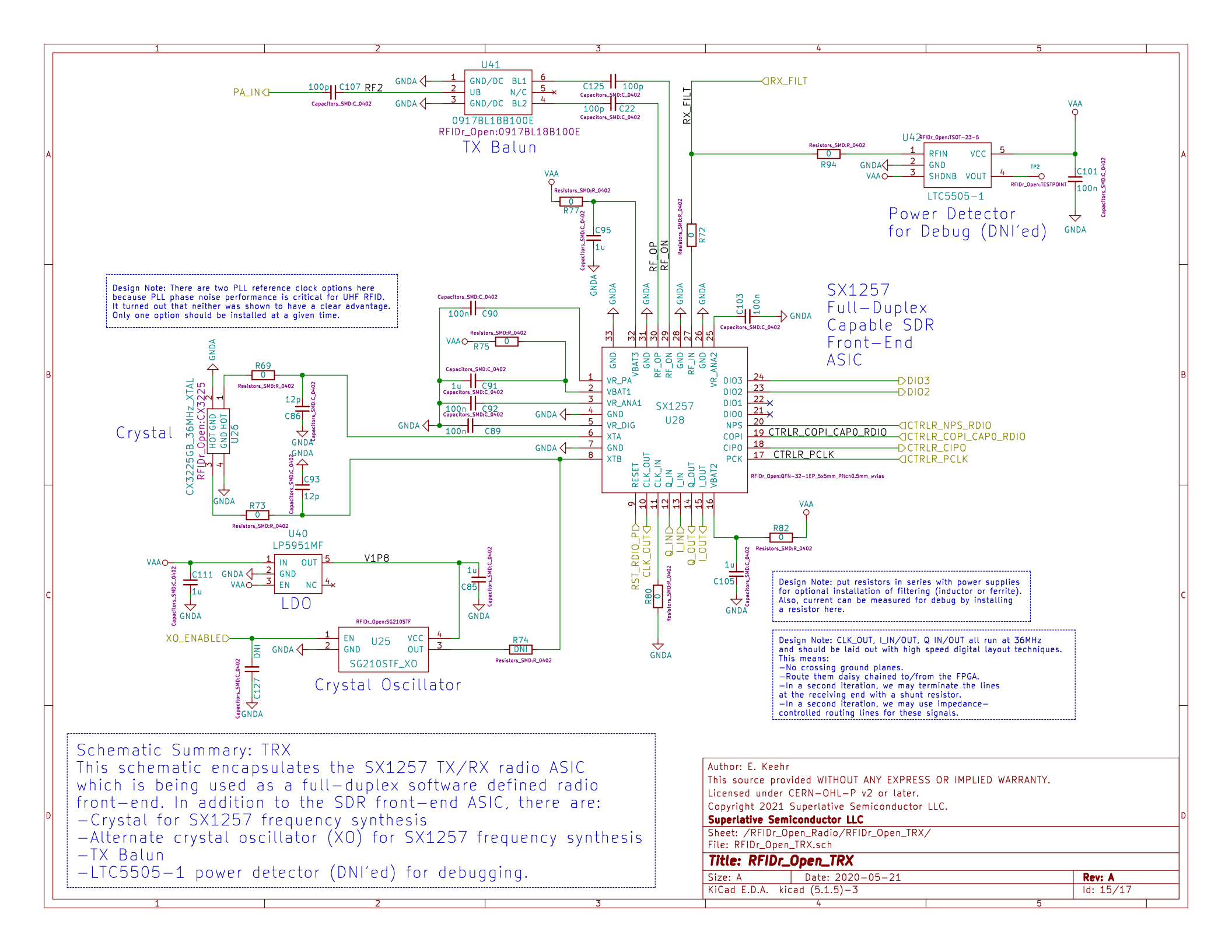


Superlative Semiconductor LLC

Sheet: /RFIDr_Open_Radio/RF_VIAS/
File: RF_VIAS.sch

Title: RF_VIAS

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 14/17



Schematic Summary: TRX

This schematic encapsulates the SX1257 TX/RX radio ASIC which is being used as a full-duplex software defined radio front-end. In addition to the SDR front-end ASIC, there are:

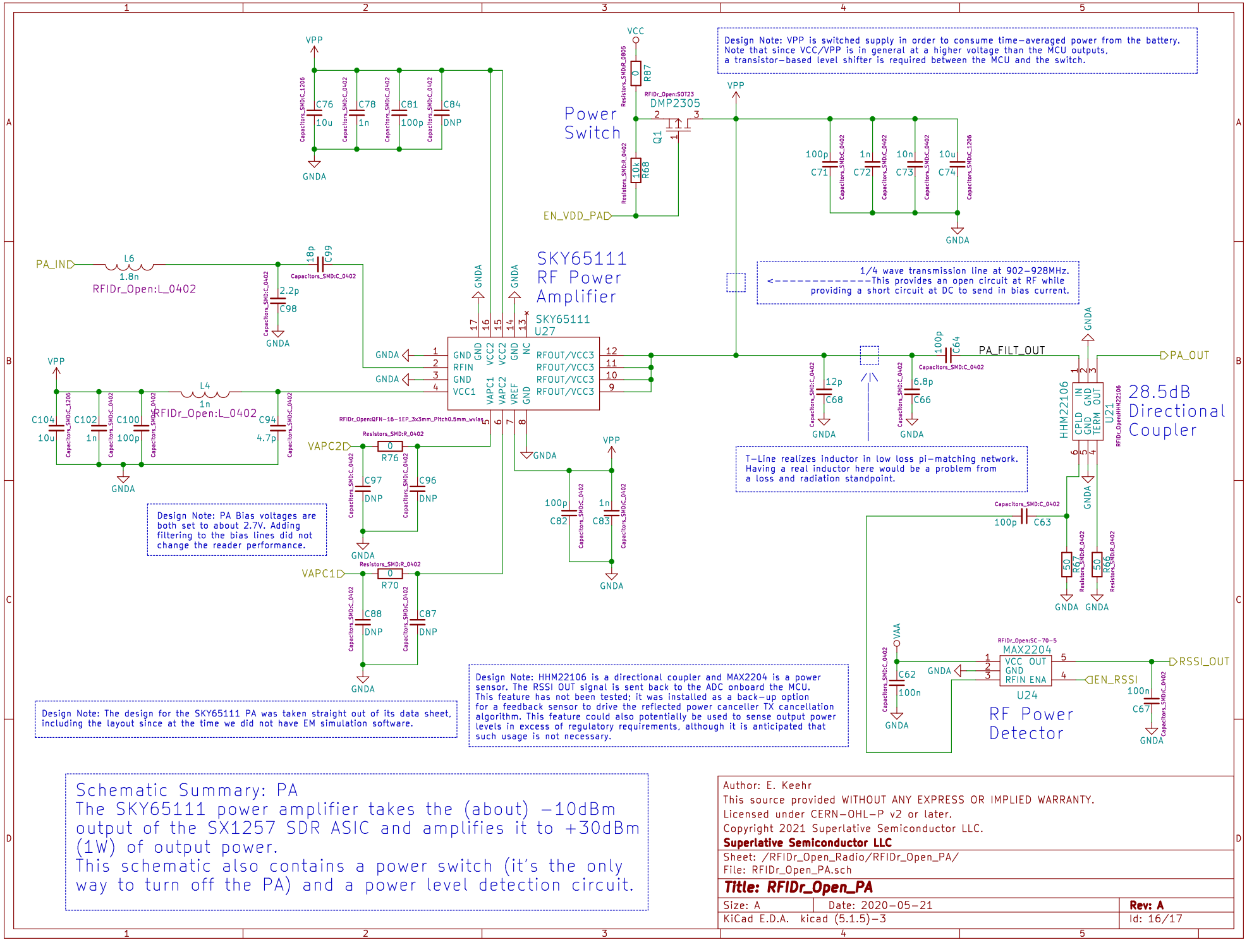
- Crystal for SX1257 frequency synthesis
- Alternate crystal oscillator (XO) for SX1257 frequency synthesis
- TX Balun
- LTC5505-1 power detector (DNI'ed) for debugging.

Superlative Semiconductor LLC

Sheet: /RFIDr_Open_Radio/RFIDr_Open_TRX/
File: RFIDr_Open_TRX.sch

Title: RFIDr_Open_TRX

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 15/17


Design Note: VPP is switched supply in order to consume time-averaged power from the battery.
Note that since VCC/VPP is in general at a higher voltage than the MCU outputs,
a transistor-based level shifter is required between the MCU and the switch.
Power Switch
DMP2305
Q1
R87
R68
10k
EN_VDD_PA
VCC
VPP
GNDA
C76
10u
C78
1n
C81
100p
C84
DNP
C71
100p
C72
1n
C73
10n
C74
10u
SKY65111
RF Power Amplifier
SKY65111
U27
GND
RFIN
GND
VCC1
VAPC1
VAPC2
VREF
GND
GND
VCC2
VCC2
GND
NC
RFOUT/VCC3
RFOUT/VCC3
RFOUT/VCC3
RFOUT/VCC3
PA_IND
L6
1.8n
18p
C99
2.2p
C98
L4
1n
C104
10u
C102
1n
C100
100p
C94
4.7p
C68
12p
C66
6.8p
C64
100p
PA_FILT_OUT
PA_OUT
1/4 wave transmission line at 902-928MHz.
<----------This provides an open circuit at RF while
providing a short circuit at DC to send in bias current.
T-Line realizes inductor in low loss pi-matching network.
Having a real inductor here would be a problem from
a loss and radiation standpoint.
HHM22106
CPLD
GND
TERM
IN
GND
OUT
U21
28.5dB Directional Coupler
VAPC2
VAPC1
R76
R70
C97
DNP
C96
DNP
C88
DNP
C87
DNP
C82
100p
C83
1n
C63
100p
R67
50
R66
50
Design Note: PA Bias voltages are
both set to about 2.7V. Adding
filtering to the bias lines did not
change the reader performance.
Design Note: The design for the SKY65111 PA was taken straight out of its data sheet,
including the layout since at the time we did not have EM simulation software.
Design Note: HHM22106 is a directional coupler and MAX2204 is a power
sensor. The RSSI OUT signal is sent back to the ADC onboard the MCU.
This feature has not been tested; it was installed as a back-up option
for a feedback sensor to drive the reflected power canceller TX cancellation
algorithm. This feature could also potentially be used to sense output power
levels in excess of regulatory requirements, although it is anticipated that
such usage is not necessary.
VAA
C62
100n
MAX2204
VCC
GND
RFIN
OUT
ENA
U24
EN_RSSI
RSSI_OUT
C67
100n
RF Power Detector
Schematic Summary: PA
The SKY65111 power amplifier takes the (about) -10dBm
output of the SX1257 SDR ASIC and amplifies it to +30dBm
(1W) of output power.
This schematic also contains a power switch (it's the only
way to turn off the PA) and a power level detection circuit.
Author: E. Keehr
This source provided WITHOUT ANY EXPRESS OR IMPLIED WARRANTY.
Licensed under CERN-OHL-P v2 or later.
Copyright 2021 Superlative Semiconductor LLC.
Superlative Semiconductor LLC
Sheet: /RFIDr_Open_Radio/RFIDr_Open_PA/
File: RFIDr_Open_PA.sch
Title: RFIDr_Open_PA
Size: A
Date: 2020-05-21
Rev: A
KiCad E.D.A. kicad (5.1.5)-3
Id: 16/17

Design Note: 10dB directional coupler, 6dB attenuator, and 3dB filter reduce reflected signal from antenna by 19dB to protect the SX1257 RX RF input. The absolute maximum rating of the SX1257 RX RF input is +6dBm, so for +30dBm PA output power, the antennas connected to the antenna ports must have S11 < −5dB over all operational frequencies.

Design Note: R64, R65, R95, and R57 realize a method to bypass the SKY13350 Antenna Diversity Switch.
On the original iteration of this design, it was found that distortion due to this switch prevented RX reception at high TX output power levels.
This is fixed by using a +5V chage pump and level shifters to drive the SKY13350 control ports.
This installable bypass option was put in the schematic to facilitate any further debugging with this switch.

RF Attenuator − 6dB was actually installed.

U39 SF2049E

PAT1220 U33

900 MHz U.S. License−Free Channel Filter (about 3dB Insertion Loss)

J0910CF15B0100

10dB Directional Coupler

Design Note: LEDs on antenna control nets are for debugging purposes.

SKY13350 U22

Antenna Diversity Switch

Antenna SMA Connectors

SMA_72970 U18

SMA_72970 U19

Design Note: 10dB Directional Coupler multiplexes RX and TX onto the antenna. Since RX and TX operate at the same frequencies, TX cancellation in the RX path is required to receive signal at any meaningful level.

Design Note: The SKY13350 Antenna Diversity Switch permits one to attach two antennas in different orientations to the reader to permit tags reads for all tag orientations and placments around the reader.

Currently it is recommended that the alternate antennta port (U19) be terminated in a 50 ohm SMA termination so that the reader can determine if the SX1257 PLL has gotten itself into a state where (our best guess is) the TX preamplifier can pull on the RX PLL, increasing RX noise.

Schematic Summary: ANT_ACCESS

The antenna access schematic comprises a hodgepodge of circuits related to antenna access. From left to right:

- −RX 902−928MHz channel filter
- −RX attenuator (for SX1257 RX protection).
- −Directional coupler (for TX/RX antenna access)
- −Diversity switch LEDs and current−limit resistors.
- −SKY13350 antenna diversity switch.
- −Antenna SMA connectors and ESD protection.

Superlative Semiconductor LLC

Sheet: /RFIDr_Open_Radio/RFIDr_Open_ANT_ACCESS/
File: RFIDr_Open_ANT_ACCESS.sch

Title: RFIDr_Open_ANT_ACCESS

Size: A	Date: 2020−05−21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)−3		Id: 17/17