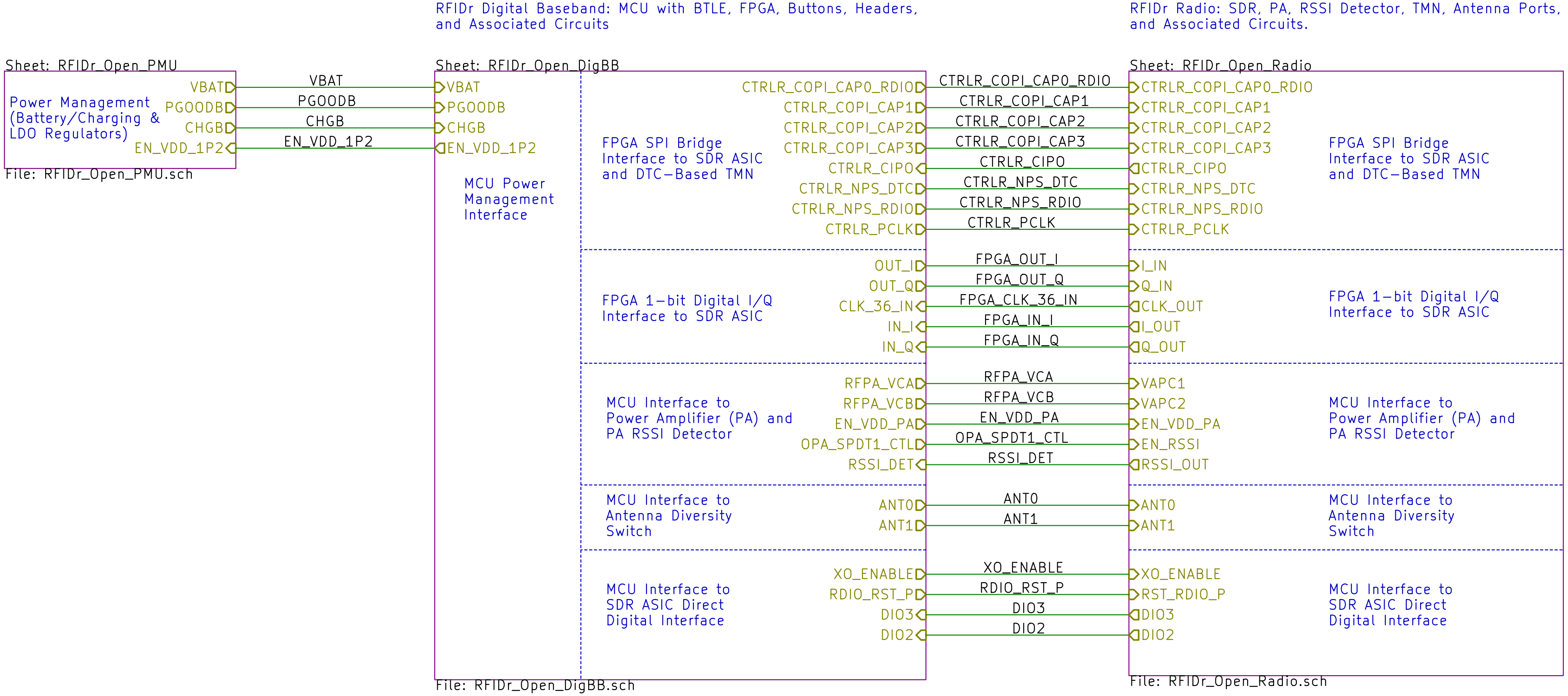

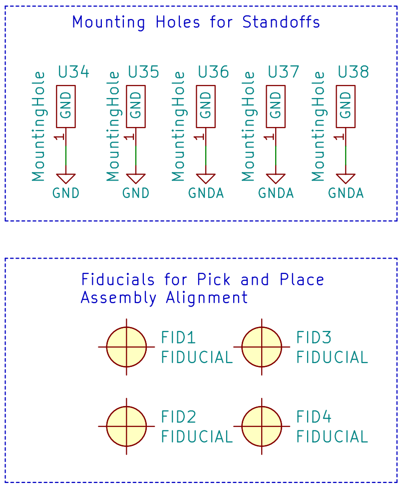

Schematic Summary: Top Level
This is the top level of the RFIDr reader design.
Subschematics are:
-PMU (Power Management Unit)
-Digital Baseband (MCU, FPGA, other associated circuits)
-Radio (Software-Defined Radio, Power Amplifier, Tunable Microwave Network, etc.)

Author: E. Keehr

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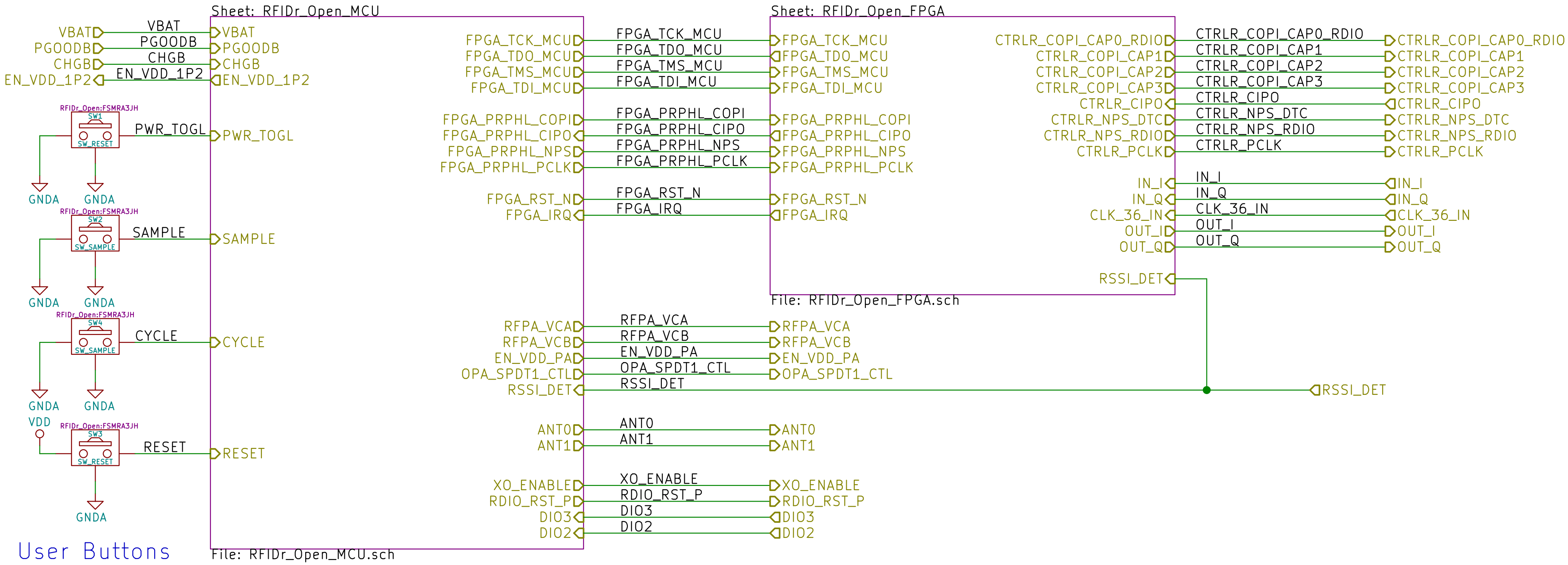
Sheet: /
File: RFIDr_Open_Top.sch

Title: RFIDr Top Level

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/17

Schematic Summary: DigBB
This schematic is another high-level schematic which separates the MCU and the FPGA.
The FPGA performs all of the real-time digital baseband operations of the RFIDr reader,
while the MCU performs less time-critical, but more behaviorally complex operations.



Design Note:
The user buttons were added in when it was thought
that the RFIDr reader may become a consumer product.
Power toggle was to turn the reader on/off.
Sample was to search for a particular tag.
Cycle was to cycle through a list of items in a smartphone app.
Reset was to reset, of course.

Author: E. Keehr

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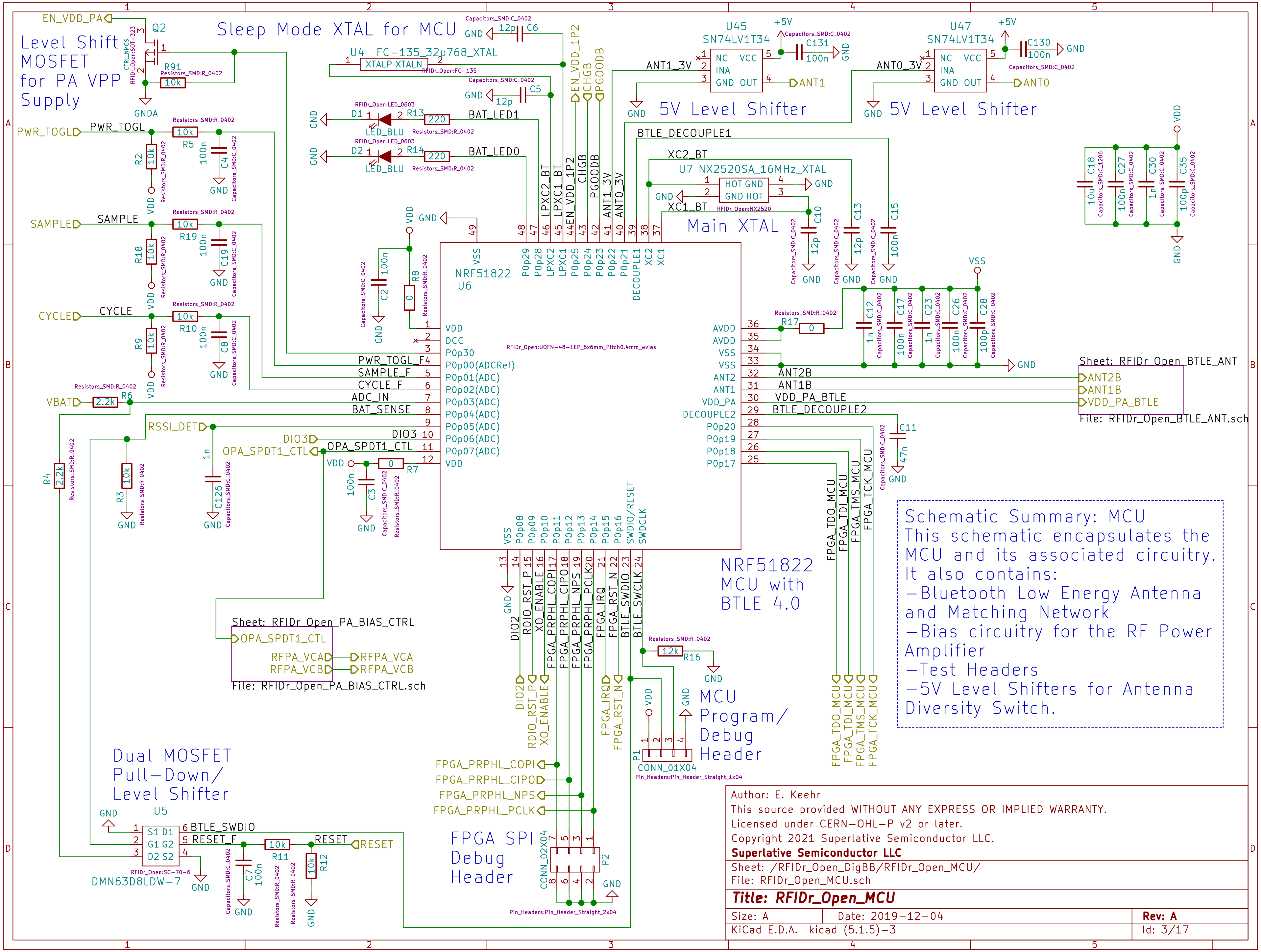
Sheet: /RFIDr_Open_DigBB/
File: RFIDr_Open_DigBB.sch

Title: RFIDr_Open_DigBB

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/17



Level Shift MOSFET for PA VPP Supply
Sleep Mode XTAL for MCU
5V Level Shifter
5V Level Shifter
Main XTAL
NRF51822 MCU with BTLE 4.0
Schematic Summary: MCU
This schematic encapsulates the MCU and its associated circuitry.
It also contains:
-Bluetooth Low Energy Antenna and Matching Network
-Bias circuitry for the RF Power Amplifier
-Test Headers
-5V Level Shifters for Antenna Diversity Switch.
Sheet: RFIDr_Open_BTLE_ANT
File: RFIDr_Open_BTLE_ANT.sch
Sheet: RFIDr_Open_PA_BIAS_CTRL
File: RFIDr_Open_PA_BIAS_CTRL.sch
Dual MOSFET Pull-Down/ Level Shifter
MCU Program/ Debug Header
FPGA SPI Debug Header
U6 NRF51822
U45 SN74LV1T34
U47 SN74LV1T34
U4 FC-135_32p768_XTAL
U7 NX2520SA_16MHz_XTAL
U5 DMN63D8LDW-7
Q2
P1 CONN_01X04
P2 CONN_02X04
EN_VDD_PA
PWR_TOGL
SAMPLE
CYCLE
VBAT
RSSI_DET
DIO3
OPA_SPDT1_CTL
RFPA_VCA
RFPA_VCB
ANT1_3V
ANT0_3V
ANT1
ANT0
BAT_LED1
BAT_LED0
BTLE_DECOUPLE1
BTLE_DECOUPLE2
XC2_BT
XC1_BT
ANT2B
ANT1B
VDD_PA_BTLE
FPGA_TDO_MCU
FPGA_TDI_MCU
FPGA_TMS_MCU
FPGA_TCK_MCU
DIO2
RDIO_RST_P
XO_ENABLE
FPGA_PRPHL_COPI
FPGA_PRPHL_CIPO
FPGA_PRPHL_NPS
FPGA_PRPHL_PCLK
FPGA_IRQ
FPGA_RST_N
BTLE_SWDIO
BTLE_SWCLK
RESET
Author: E. Keehr
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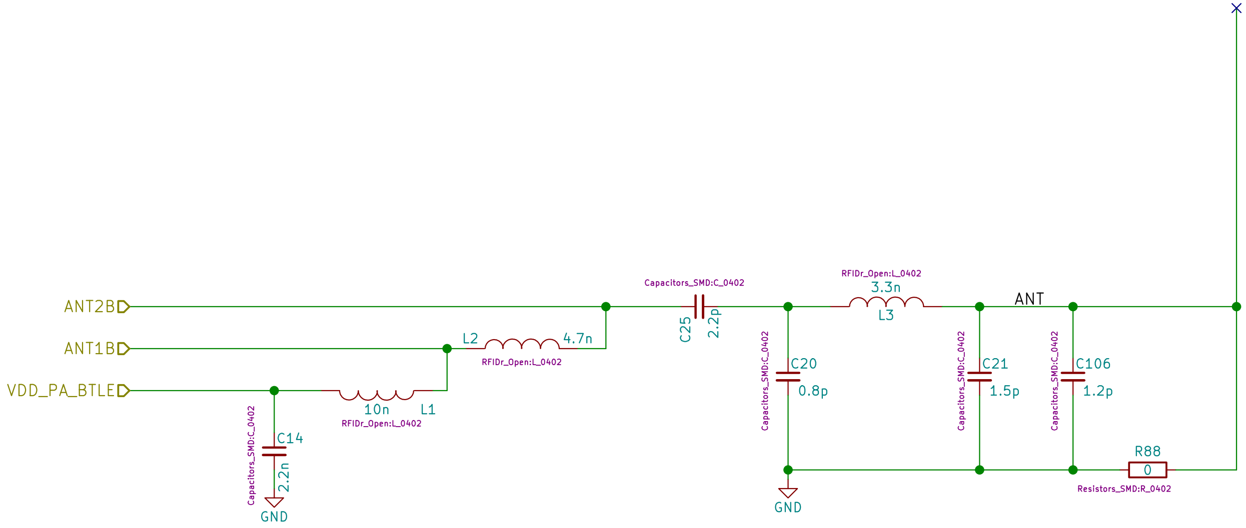
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_MCU/
File: RFIDr_Open_MCU.sch
Title: RFIDr_Open_MCU
Size: A
Date: 2019-12-04
Rev: A
KiCad E.D.A. kicad (5.1.5)-3
Id: 3/17

Design Note: Metallization on net "ANT"
should realize an inverted-F antenna.



Schematic Summary: BTLE_ANT
Here, we follow the recommended
matching network from the Nordic
PCA10001 Development PCB
(antenna is a bit different).

Author: E. Keehr

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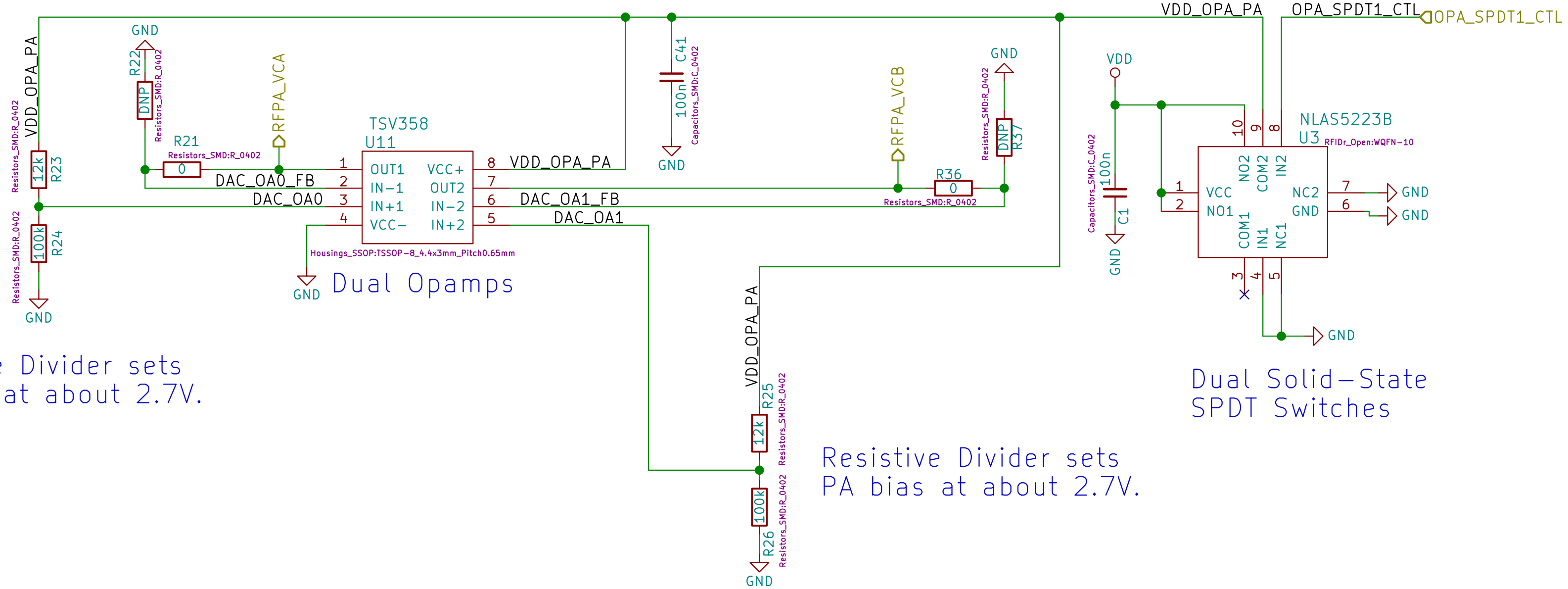
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_MCU/RFIDr_Open_BTLE_ANT/
File: RFIDr_Open_BTLE_ANT.sch

Title: RFIDr_Open_BTLE_ANT

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/17

Schematic Summary: PA BIAS Control
In this schematic, bias voltages for the PA are generated via resistor strings and unity-gain biased opamps.
It was intended in the future that the PA bias be made adjustable on-the-fly, but
this was a way it could be made easily adjustable by changing a resistor divider.
The resistive dividers could use capacitive decouping to ground at the output
voltage node, but tests have shown this makes no difference to reader performance.



Resistive Divider sets
PA bias at about 2.7V.

Dual Solid-State
SPDT Switches

Resistive Divider sets
PA bias at about 2.7V.

Author: E. Keehr

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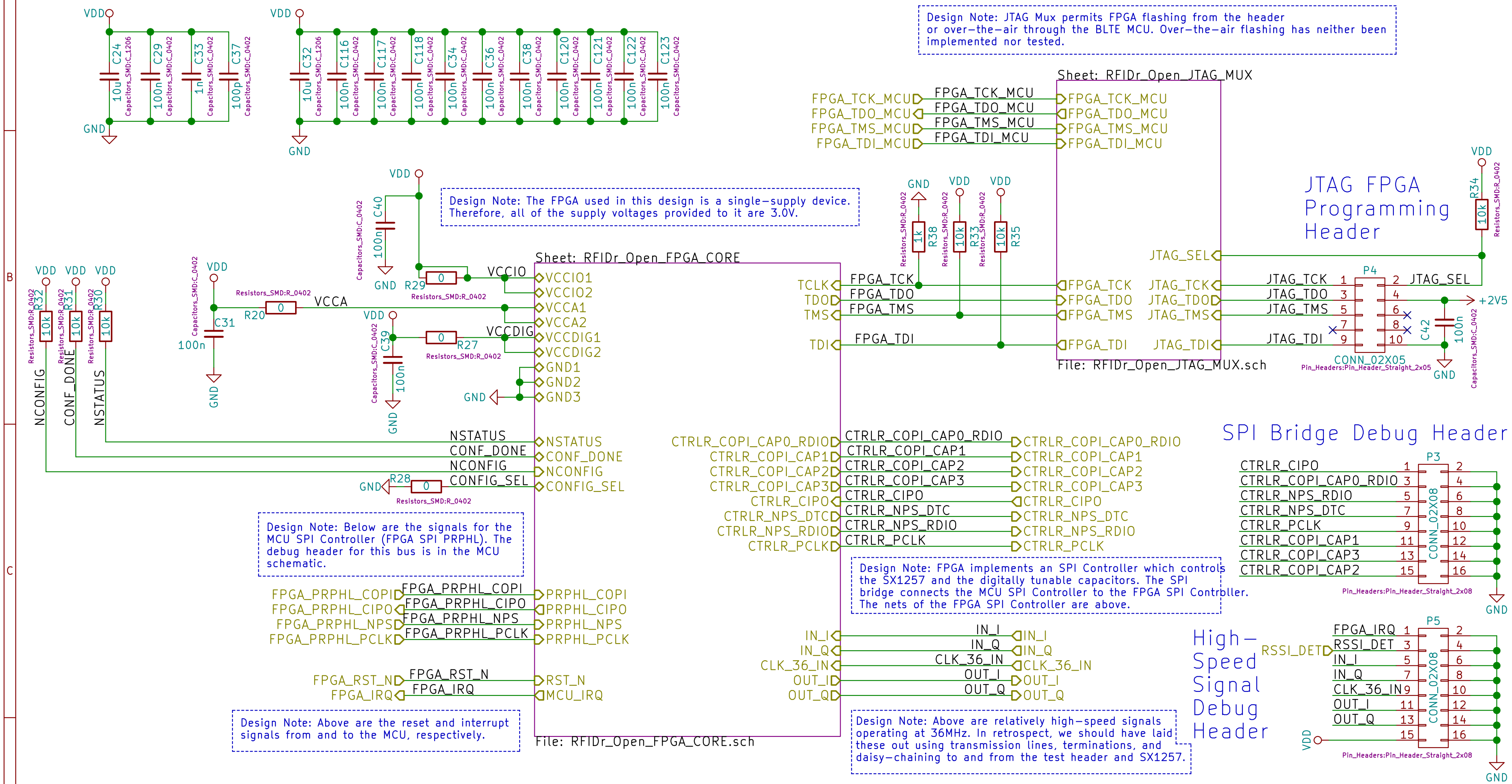
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_MCU/RFIDr_Open_PA_BIAS_CTRL/
File: RFIDr_Open_PA_BIAS_CTRL.sch

Title: RFIDr_Open_PA_BIAS_CTRL

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/17

Schematic Summary: FPGA
This schematic simplifies the set of nets interfacing the FPGA to the rest of the reader.
The real-time digital back end of the RFID reader's software-defined radio resides on the FPGA.



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Sheet: /RFIDr_Open_DigBB/RFIDr_Open_FPGA/
File: RFIDr_Open_FPGA.sch

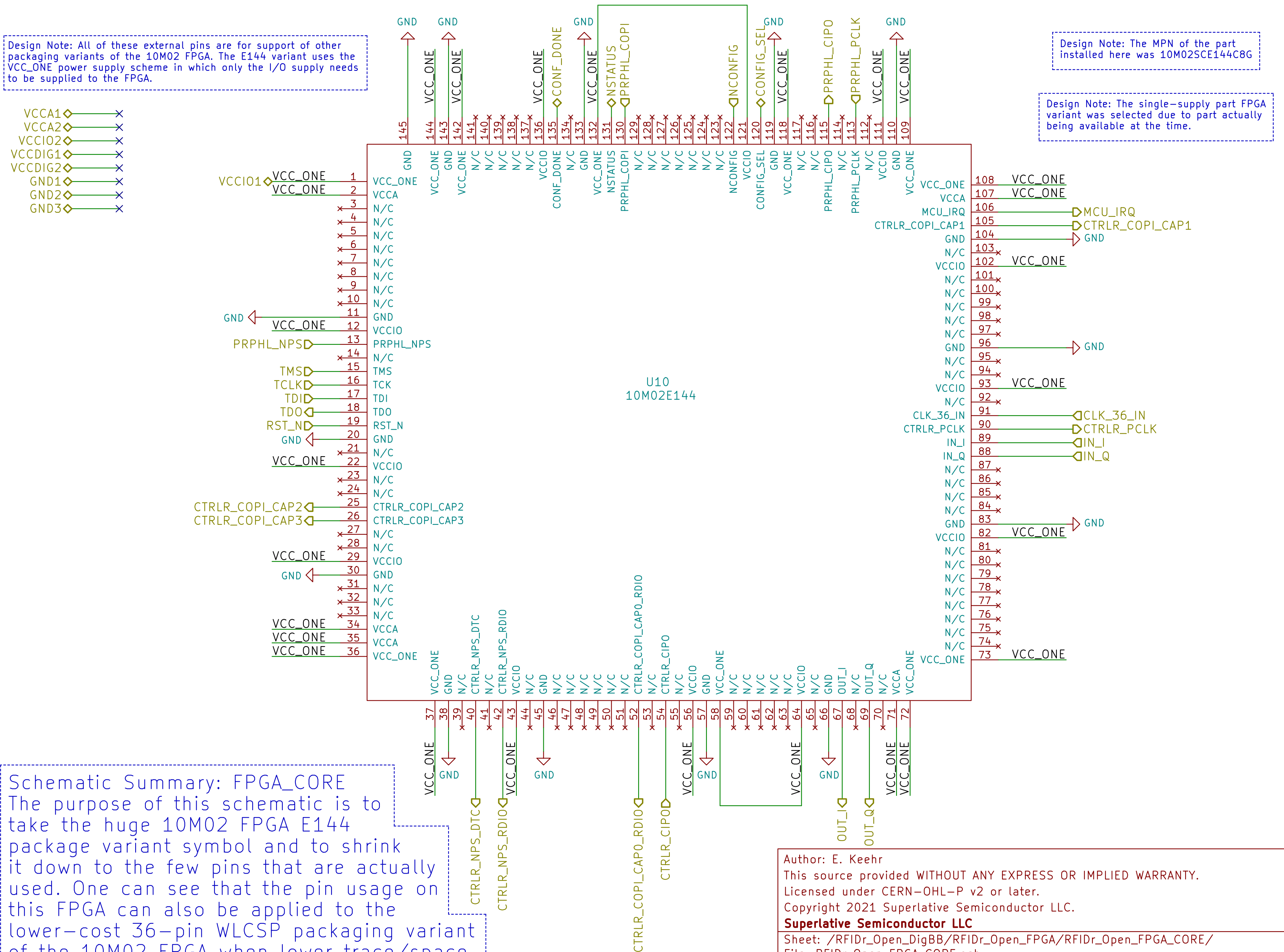
Title: RFIDr_Open_FPGA

Size: A | Date: 2019-12-04 | **Rev: A**
KiCad E.D.A. kicad (5.1.5)-3 | Id: 6/17

Design Note: All of these external pins are for support of other packaging variants of the 10M02 FPGA. The E144 variant uses the VCC_ONE power supply scheme in which only the I/O supply needs to be supplied to the FPGA.

Design Note: The MPN of the part installed here was 10M02SCE144C8G

Design Note: The single-supply part FPGA variant was selected due to part actually being available at the time.



Schematic Summary: FPGA_CORE
The purpose of this schematic is to take the huge 10M02 FPGA E144 package variant symbol and to shrink it down to the few pins that are actually used. One can see that the pin usage on this FPGA can also be applied to the lower-cost 36-pin WLCSP packaging variant of the 10M02 FPGA when lower trace/space design rules can be obtained from the PCB fabricator.

Author: E. Keehr

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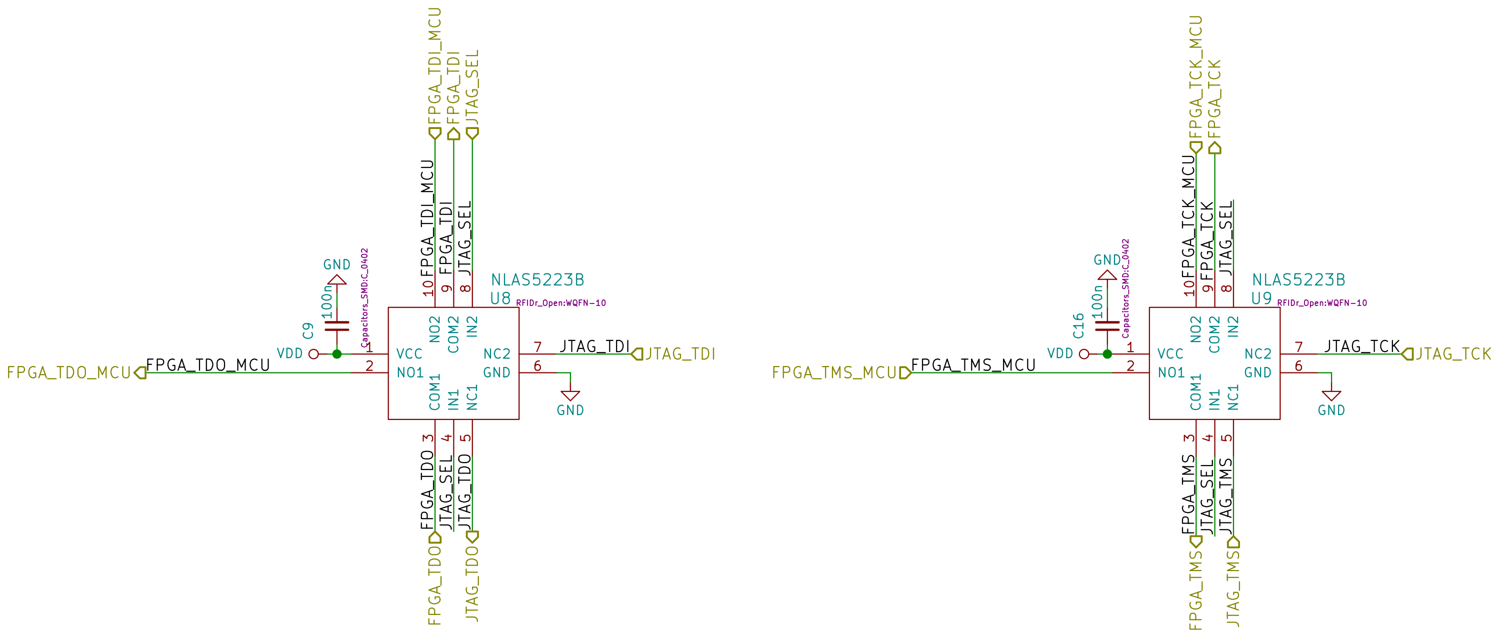
Sheet: /RFIDr_Open_DigBB/RFIDr_Open_FPGA/RFIDr_Open_FPGA_CORE/
File: RFIDr_Open_FPGA_CORE.sch

Title: RFIDr_Open_FPGA_CORE

Size: A	Date: 2020-01-16	Rev: A
KiCad E.D.A. kicad (5.1.5)-3		Id: 7/17

Schematic Summary: JTAG MUX
This pair of dual solid-state switches permits programming of the FPGA either through an onboard header, or over-the-air through the MCU. So far, over-the-air FPGA reprogramming has not been implemented or tested.



Dual Solid-State SPDT Switches

Dual Solid-State SPDT Switches

Author: E. Keehr

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Sheet: /RFIDr_Open_DigBB/RFIDr_Open_FPGA/RFIDr_Open_JTAG_MUX/
File: RFIDr_Open_JTAG_MUX.sch

Title: RFIDr_Open_JTAG_MUX

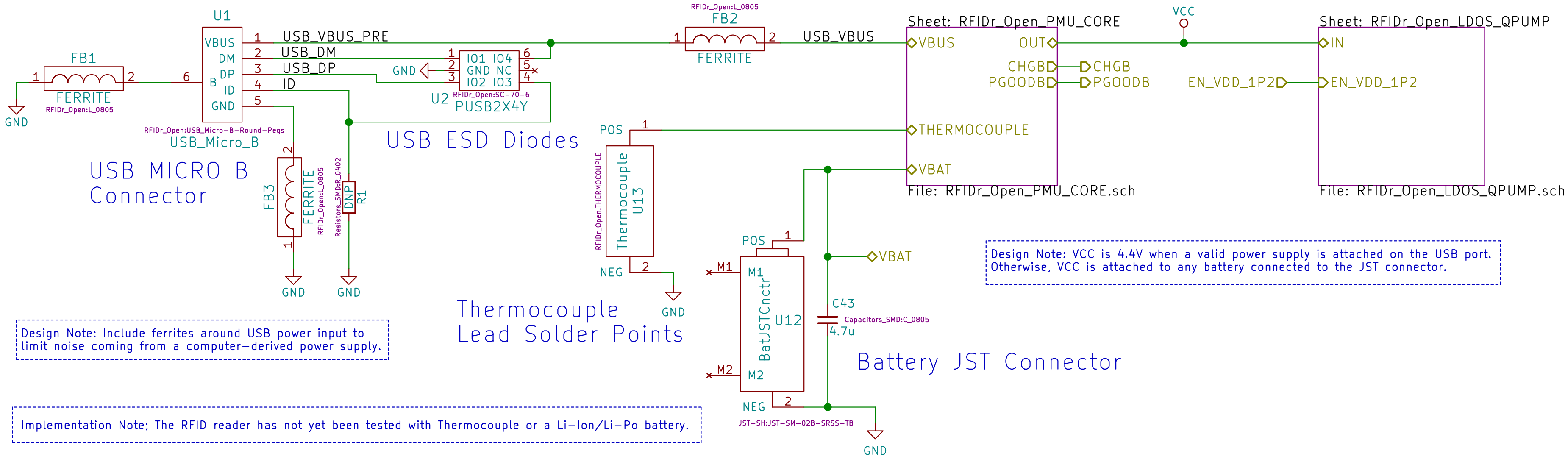
Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 8/17

```
POWER TREE:  [USB_VBUS (5V)] ->1019mA -> [VCC (4.4V)] ----> 850mA -> [VPP (Switched 4.4V)] -> 850mA -> [RF Power Amplifier]
                                                  |
                                                  V -> 10mA ->  [2 LEDs]
                                                  |
                                                  V -> about 0mA ->  [+2V5] -> about 0mA -> [+5V] -> [Level shifters for antenna diversity switch control (MCU Schematic)]
                                                  |
                                                  V -> about 0mA ->  [+1V2] -> Not used here, used for other 10M02 FPGA package variants.
                                                  |
                                                  V -> 159.3mA ->  [VDD (3.0V) - Digital Supply] ----> 32.5mA ->[FPGA]
                                                                                       |
                                                                                       V--> 18mA ->  [3 LEDs]
                                                                                       |
                                                                                       V--> 5mA ->  [MCU Digital]
                                                                                       |
                                                                                       V--> 16mA ->  [VSS (3.0V)] -> 16mA -> [MCU BTLE Radio PA]
                                                                                       |
                                                                                       V--> 87.8mA ->  [VAA (3.0V)] ----> 85mA -> [SX1257 SDR ASIC Max Power]
                                                                                                              |
                                                                                                              V--> 2.2mA ->  [XTAL OSC]
                                                                                                              |
                                                                                                              V--> 0.6mA ->  [DTC-Based TMN]
```

Schematic Summary: PMU (Power Management Unit)
This schematic is the top level of the power management
on the RFIDr reader.
Subunits include:
-USB Micro-B Charging port (this schematic)
-Li-Ion battery and thermcouple access (this schematic)
-PMU CORE (BQ24073 charging chip and associated passives)
-LDOS/QPUMP (LDOs and Charge Pump for derived supply voltages)

Implementation Note: The BQ24073 power management chip can accept 4.35V to 6.6V on VBUS. Typical VBUS value is 5V.

Layout Note: USB_VBUS, USB_VBUS_PRE, VCC, and VBAT lines should all be sized to carry about 1.5A of current.
The BQ24073 power management chip limits input current to about 1.36A.

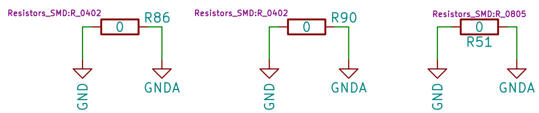


Design Note: VCC is 4.4V when a valid power supply is attached on the USB port.
Otherwise, VCC is attached to any battery connected to the JST connector.

Design Note: Include ferrites around USB power input to
limit noise coming from a computer-derived power supply.

Implementation Note; The RFID reader has not yet been tested with Thermocouple or a Li-Ion/Li-Po battery.

Design Note: These resistors contact digital ground (GND) to analog ground (GNDA).
This is done in a quasi-star ground configuration where the analog ground/supply (VAA)
is derived from the digital 3.0V supply (VDD) due to layout constraints
(namely digital circuitry being in between the power and analog circuitries).



Author: E. Keehr

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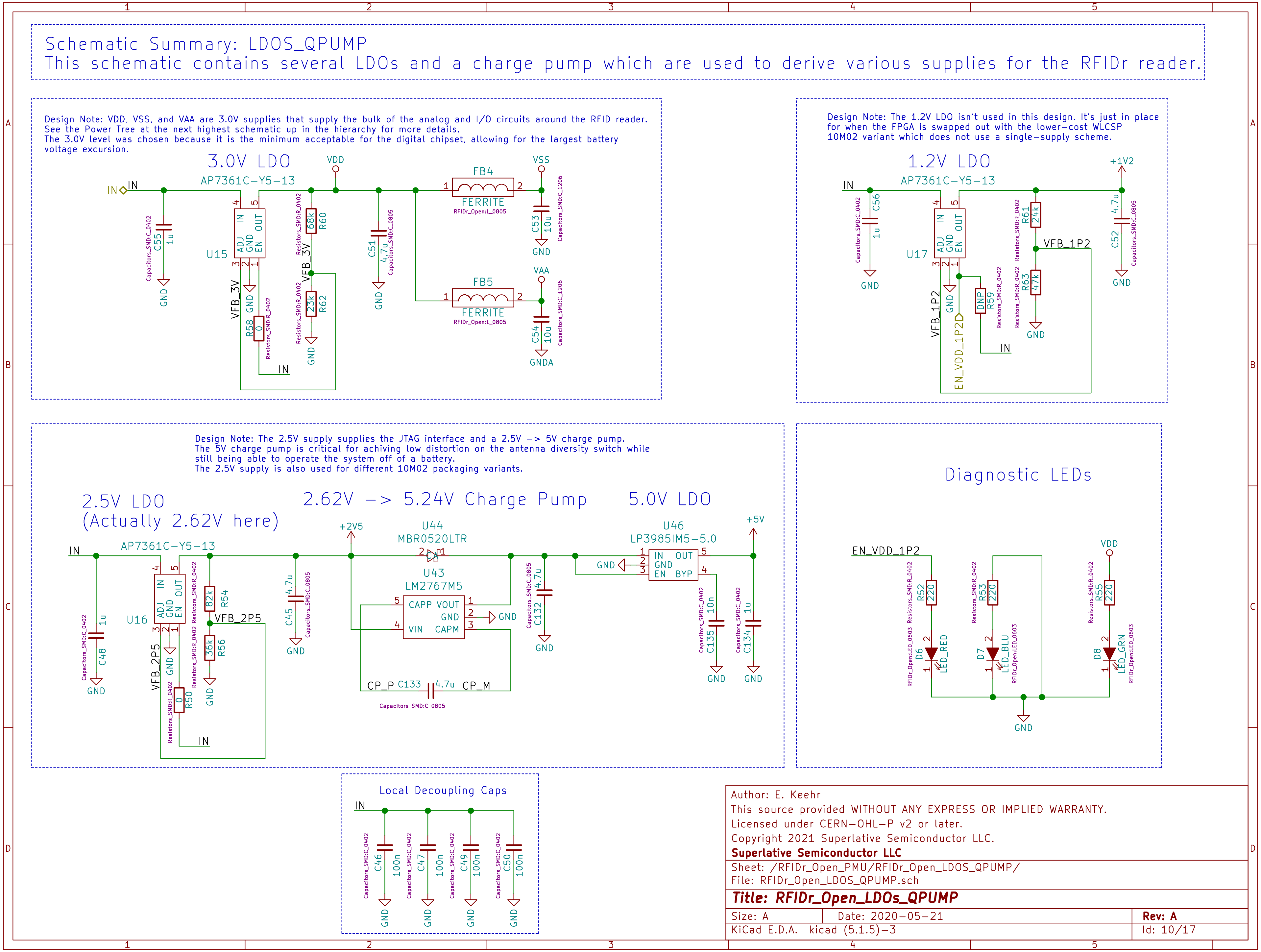
Sheet: /RFIDr_Open_PMU/
File: RFIDr_Open_PMU.sch

Title: RFIDr_Open_PMU

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 9/17



Schematic Summary: LDOS_QPUMP
This schematic contains several LDOs and a charge pump which are used to derive various supplies for the RFIDr reader.
Design Note: VDD, VSS, and VAA are 3.0V supplies that supply the bulk of the analog and I/O circuits around the RFID reader.
See the Power Tree at the next highest schematic up in the hierarchy for more details.
The 3.0V level was chosen because it is the minimum acceptable for the digital chipset, allowing for the largest battery voltage excursion.
3.0V LDO
AP7361C-Y5-13
U15
VDD
VSS
VAA
FB4
FB5
FERRITE
GND
GNDA
IN
VFB_3V
C55 1u
C51 4.7u
C53 10u
C54 10u
R60 68k
R62 23k
R58 0
Design Note: The 1.2V LDO isn't used in this design. It's just in place for when the FPGA is swapped out with the lower-cost WLCSP 10M02 variant which does not use a single-supply scheme.
1.2V LDO
AP7361C-Y5-13
U17
+1V2
VFB_1P2
EN_VDD_1P2
C56 1u
C52 4.7u
R61 24k
R63 47k
R59 DNP
Design Note: The 2.5V supply supplies the JTAG interface and a 2.5V -> 5V charge pump.
The 5V charge pump is critical for achiving low distortion on the antenna diversity switch while still being able to operate the system off of a battery.
The 2.5V supply is also used for different 10M02 packaging variants.
2.5V LDO
(Actually 2.62V here)
2.62V -> 5.24V Charge Pump
5.0V LDO
AP7361C-Y5-13
U16
+2V5
VFB_2P5
U44
MBR0520LTR
U43
LM2767M5
U46
LP3985IM5-5.0
+5V
CP_P
CP_M
C133 4.7u
C48 1u
C45 4.7u
C132 4.7u
C135 10n
C134 1u
R54 82k
R56 36k
R50 0
Diagnostic LEDs
EN_VDD_1P2
VDD
R52 220
R53 220
R55 220
D6 LED_RED
D7 LED_BLU
D8 LED_GRN
Local Decoupling Caps
C46 100n
C47 100n
C49 100n
C50 100n
Author: E. Keehr
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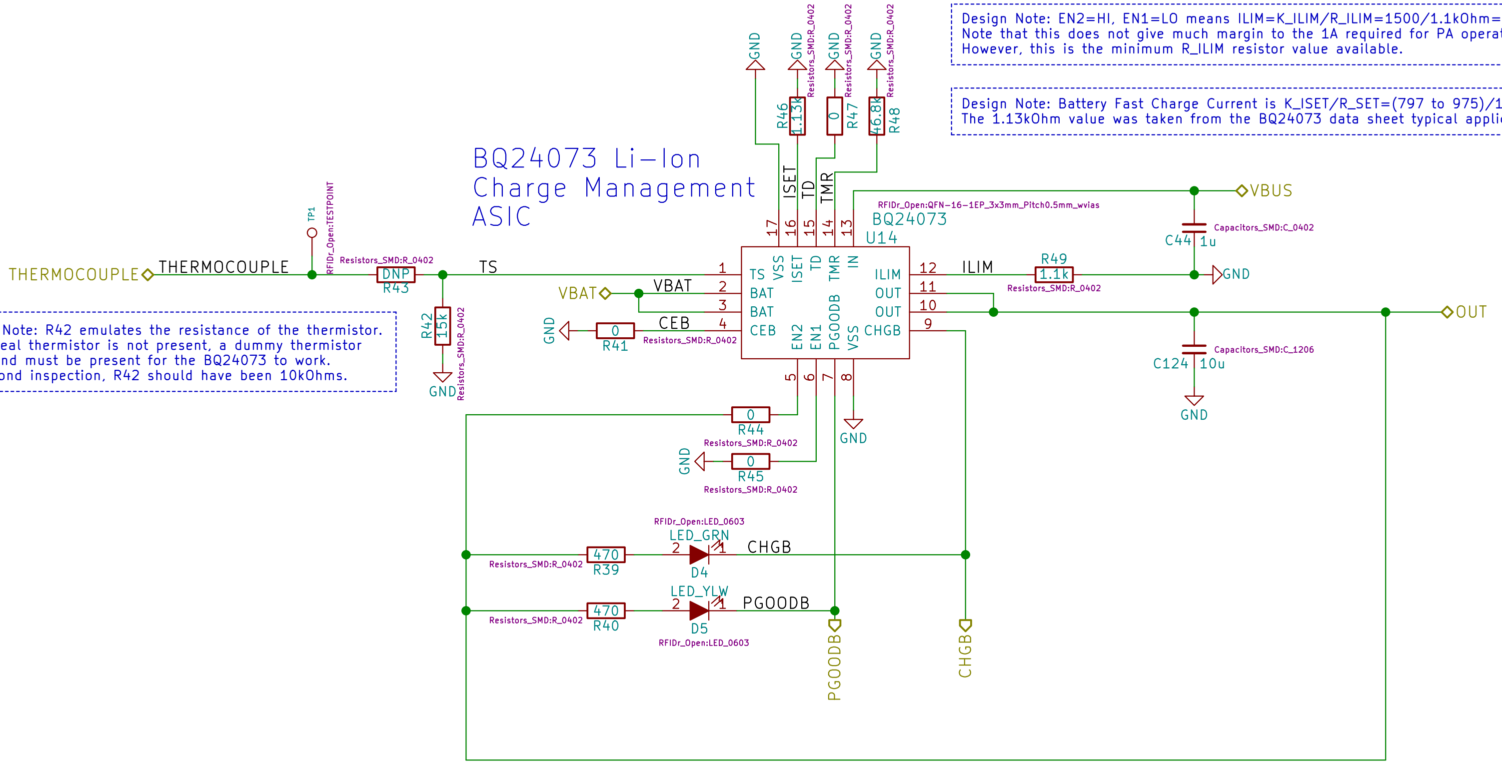
Sheet: /RFIDr_Open_PMU/RFIDr_Open_LDOS_QPUMP/
File: RFIDr_Open_LDOS_QPUMP.sch
Title: RFIDr_Open_LDOs_QPUMP
Size: A
Date: 2020-05-21
Rev: A
KiCad E.D.A. kicad (5.1.5)-3
Id: 10/17

Schematic Summary: PMU_CORE
This schematic encapsulates the BQ24073 and its associated passives. BQ24073 is an integrated Li-Ion charging solution which accepts power from a 5V source which it can use to charge a battery or to power a device. In the absence of external power, the BQ24073 routes battery power to the device's internal circuity. Operation of the reader with battery has not yet been tested.

Design Note: EN2=HI, EN1=LO means ILIM=K_ILIM/R_ILIM=1500/1.1kOhm=1.36A. Note that this does not give much margin to the 1A required for PA operation. However, this is the minimum R_ILIM resistor value available.

Design Note: Battery Fast Charge Current is K_ISET/R_SET=(797 to 975)/1.13kOhms=0.7A to 0.86A. The 1.13kOhm value was taken from the BQ24073 data sheet typical application circuit.

BQ24073 Li-Ion Charge Management ASIC



Design Note: R42 emulates the resistance of the thermistor. If the real thermistor is not present, a dummy thermistor to ground must be present for the BQ24073 to work. On second inspection, R42 should have been 10kOhms.

Design Note: LED resistors should probably be increased to 2kOhms in future iterations to save current/reduce LED brightness.

Design Note: For Input below the OVP threshold and above 4.4V, output is 4.4V. When the input is out of the operation range, OUT is connected to the battery. (From BQ24073 data sheet).

Author: E. Keehr

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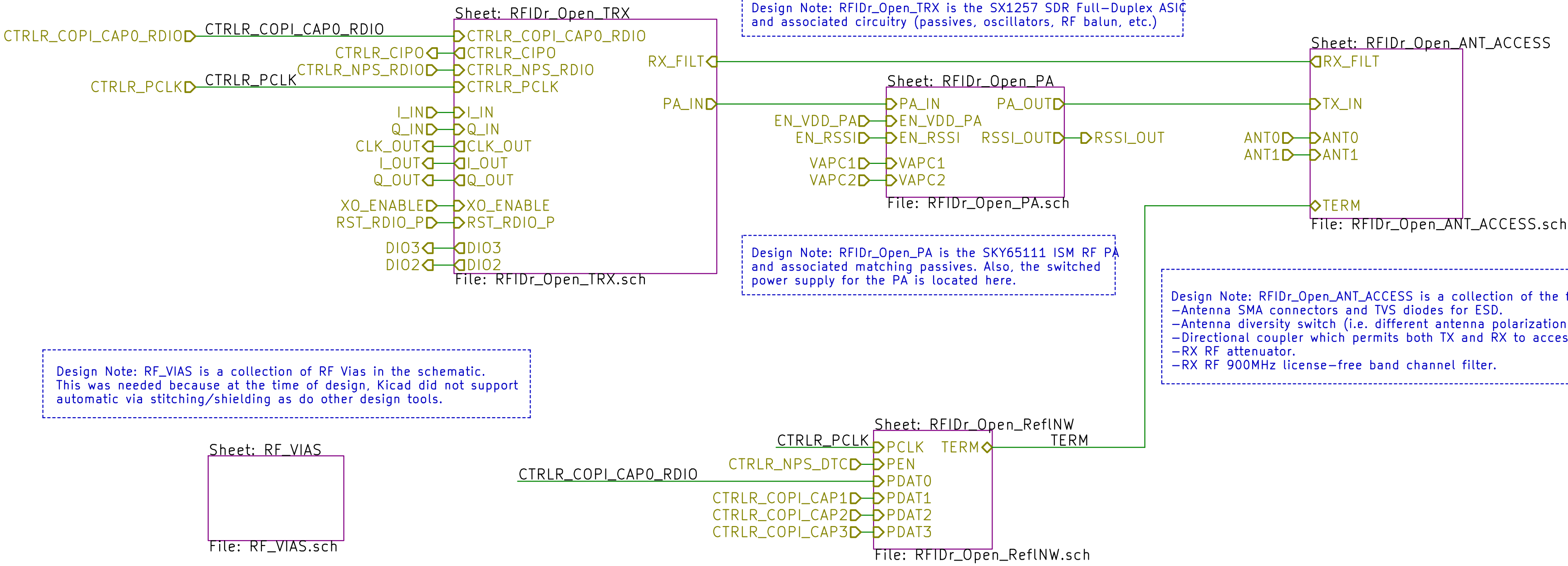
Sheet: /RFIDr_Open_PMU/RFIDr_Open_PMU_CORE/
File: RFIDr_Open_PMU_CORE.sch

Title: RFIDr_Open_PMU_CORE

Size: A	Date: 2020-05-21	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 11/17

Schematic Summary: Radio
This schematic contains all of the circuitry operating at radio frequencies.
In addition, layout in this area is done with substantial ground shielding to promote RF isolation between various blocks in this subschematic.
Subschematics include:
TRX: The Transmit/Receive Software Defined Radio ASIC and associated circuits.
PA: The Power Amplifier.
ANT_ACCESS: Various components supporting access to the antenna by the PA and SDR ASICs.
ReflNW: Reflection Network - a Tunable Microwave Network which enables TX cancellation.
RF_VIAS: RF Vias for ground shielding.



Design Note: RFIDr_Open_TRX is the SX1257 SDR Full-Duplex ASIC and associated circuitry (passives, oscillators, RF balun, etc.)

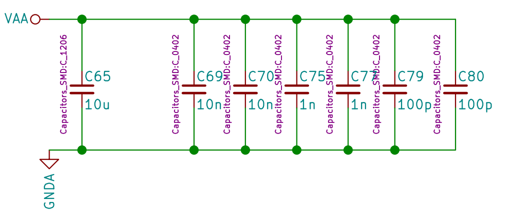
Design Note: RFIDr_Open_PA is the SKY65111 ISM RF PA and associated matching passives. Also, the switched power supply for the PA is located here.

Design Note: RFIDr_Open_ANT_ACCESS is a collection of the following:
-Antenna SMA connectors and TVS diodes for ESD.
-Antenna diversity switch (i.e. different antenna polarizations).
-Directional coupler which permits both TX and RX to access the antenna.
-RX RF attenuator.
-RX RF 900MHz license-free band channel filter.

Design Note: RF_VIAS is a collection of RF Vias in the schematic. This was needed because at the time of design, Kicad did not support automatic via stitching/shielding as do other design tools.

Design Note: RFIDr_Open_ReflNW is the Subranging Tunable Microwave Network that was the subject of its own IEEE paper at IEEE RFID 2018. Along with the directional coupler in the antenna access network, it forms a Reflected Power Canceller which cancels TX leakage in the RX section of the radio.

General Decoupling Capacitors for the Analog Supply



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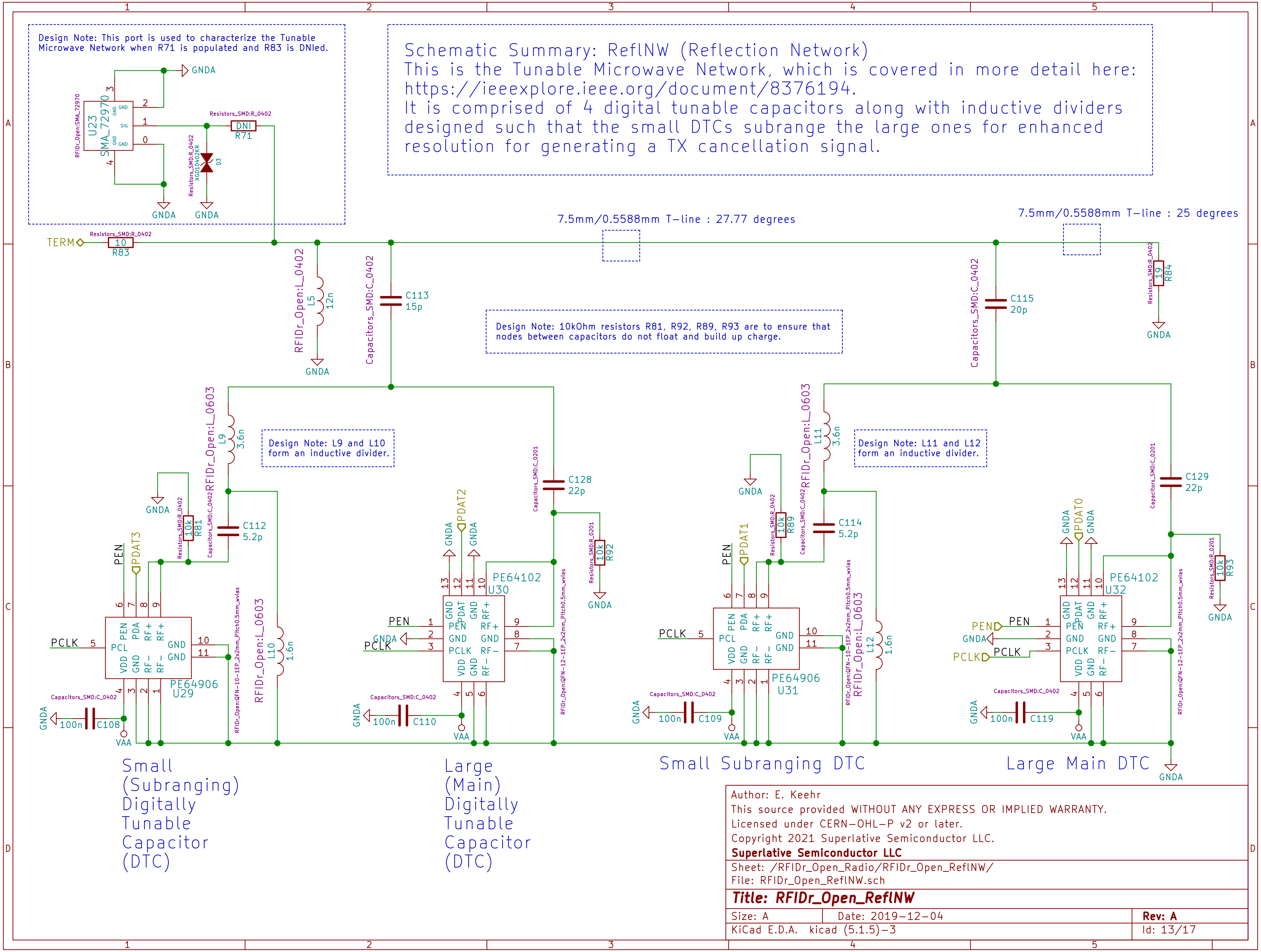
Sheet: /RFIDr_Open_Radio/
File: RFIDr_Open_Radio.sch

Title: RFIDr_Open_Radio

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 12/17


Design Note: This port is used to characterize the Tunable Microwave Network when R71 is populated and R83 is DNIed.
Schematic Summary: ReflNW (Reflection Network)
This is the Tunable Microwave Network, which is covered in more detail here: https://ieeexplore.ieee.org/document/8376194.
It is comprised of 4 digital tunable capacitors along with inductive dividers designed such that the small DTCs subrange the large ones for enhanced resolution for generating a TX cancellation signal.
7.5mm/0.5588mm T-line : 27.77 degrees
7.5mm/0.5588mm T-line : 25 degrees
Design Note: 10kOhm resistors R81, R92, R89, R93 are to ensure that nodes between capacitors do not float and build up charge.
Design Note: L9 and L10 form an inductive divider.
Design Note: L11 and L12 form an inductive divider.
TERM
R83
R71
DNI
U23
SMA_72970
D3
L5
12n
C113
15p
C115
20p
R84
19
L9
3.6n
L10
1.6n
C112
5.2p
R81
10k
C128
22p
R92
10k
L11
3.6n
L12
1.6n
C114
5.2p
R89
10k
C129
22p
R93
10k
PE64906
U29
PE64102
U30
PE64906
U31
PE64102
U32
C108
100n
C110
100n
C109
100n
C119
100n
PEN
PCLK
PDAT3
PDAT2
PDAT1
PDAT0
GNDA
VAA
Small (Subranging) Digitally Tunable Capacitor (DTC)
Large (Main) Digitally Tunable Capacitor (DTC)
Small Subranging DTC
Large Main DTC
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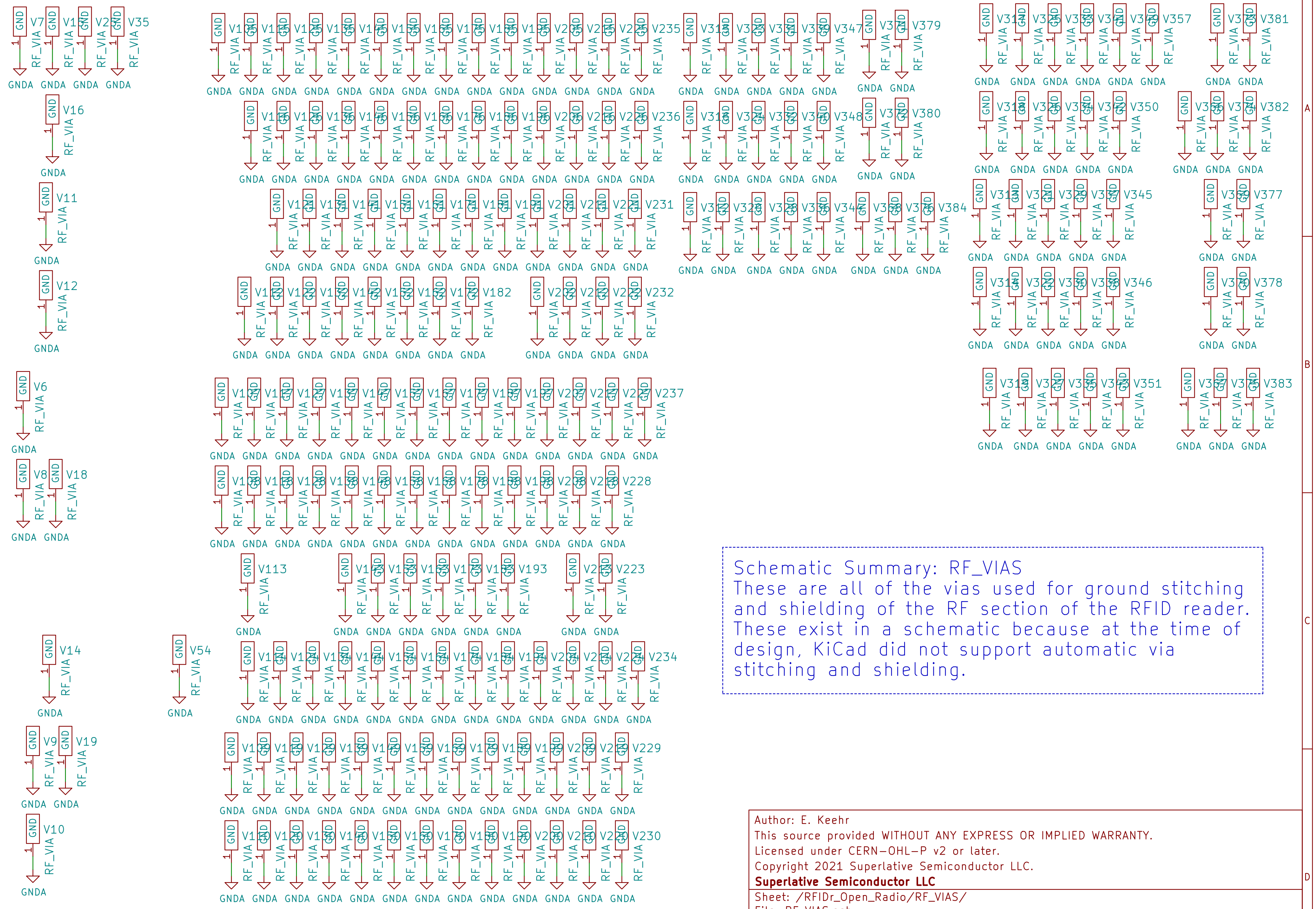
Sheet: /RFIDr_Open_Radio/RFIDr_Open_ReflNW/
File: RFIDr_Open_ReflNW.sch
Title: RFIDr_Open_ReflNW
Size: A
Date: 2019-12-04
Rev: A
KiCad E.D.A. kicad (5.1.5)-3
Id: 13/17



Schematic Summary: RF_VIAS
These are all of the vias used for ground stitching and shielding of the RF section of the RFID reader. These exist in a schematic because at the time of design, KiCad did not support automatic via stitching and shielding.

Author: E. Keehr

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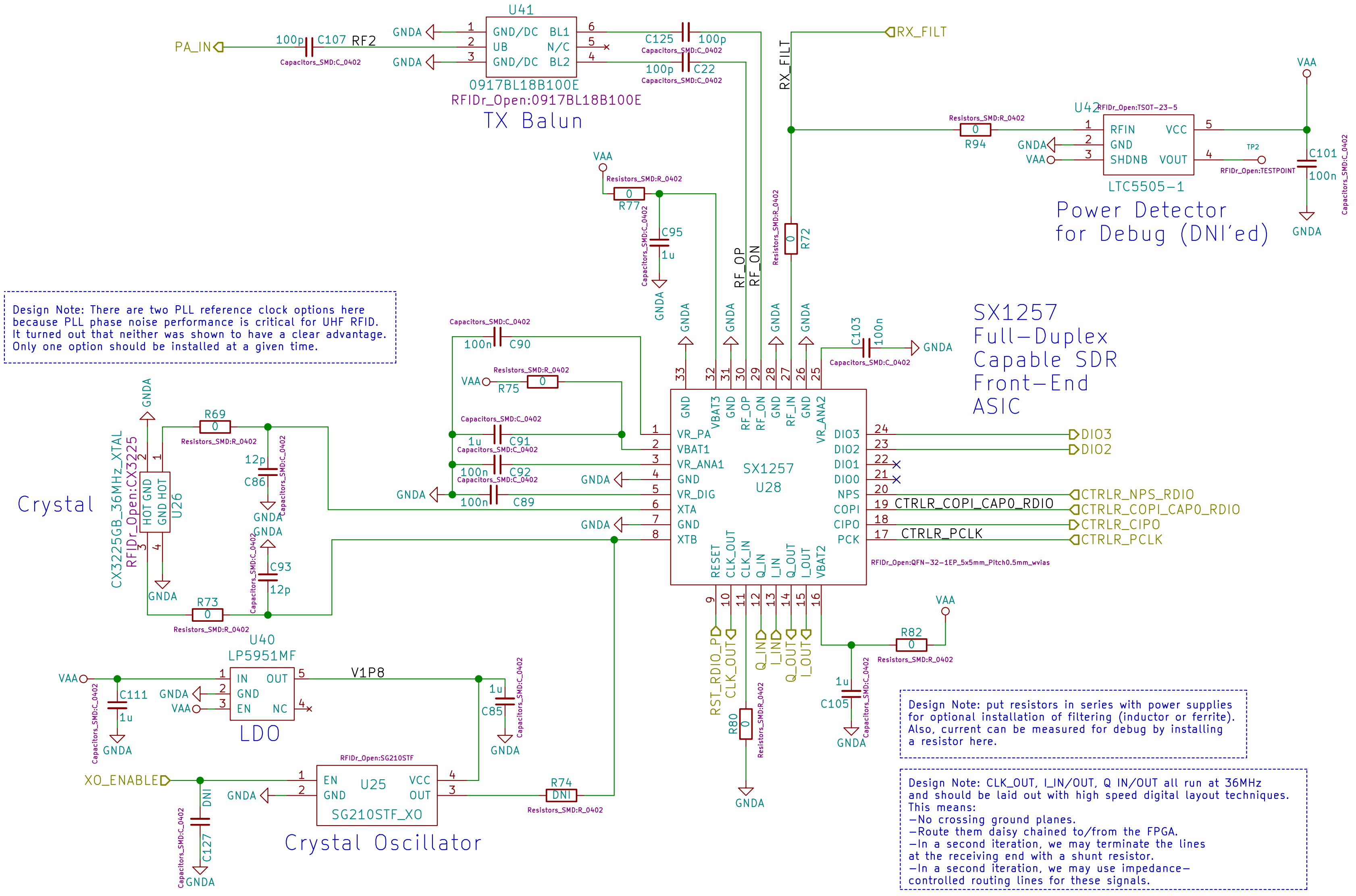
Sheet: /RFIDr_Open_Radio/RF_VIAS/
File: RF_VIAS.sch

Title: RF_VIAS

Size: A	Date: 2019-12-04	**Rev: A**
KiCad E.D.A. kicad (5.1.5)-3		Id: 14/17



Design Note: There are two PLL reference clock options here because PLL phase noise performance is critical for UHF RFID. It turned out that neither was shown to have a clear advantage. Only one option should be installed at a given time.

Design Note: put resistors in series with power supplies for optional installation of filtering (inductor or ferrite). Also, current can be measured for debug by installing a resistor here.

Design Note: CLK_OUT, I_IN/OUT, Q IN/OUT all run at 36MHz and should be laid out with high speed digital layout techniques. This means:
- No crossing ground planes.
- Route them daisy chained to/from the FPGA.
- In a second iteration, we may terminate the lines at the receiving end with a shunt resistor.
- In a second iteration, we may use impedance-controlled routing lines for these signals.

Schematic Summary: TRX
This schematic encapsulates the SX1257 TX/RX radio ASIC which is being used as a full-duplex software defined radio front-end. In addition to the SDR front-end ASIC, there are:
- Crystal for SX1257 frequency synthesis
- Alternate crystal oscillator (XO) for SX1257 frequency synthesis
- TX Balun
- LTC5505-1 power detector (DNI'ed) for debugging.

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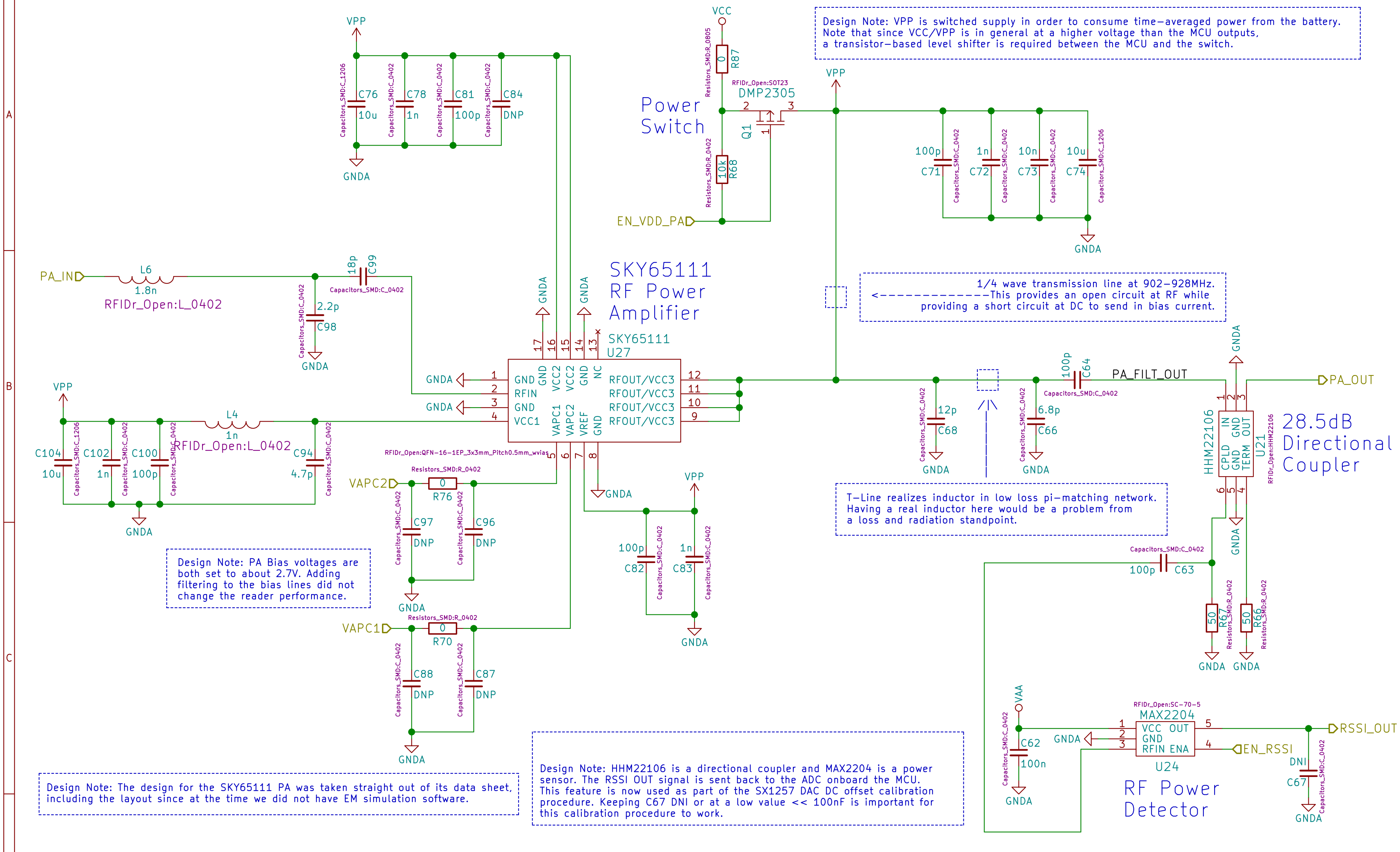

Schematic Summary: PA

The SKY65111 power amplifier takes the (about) -10dBm output of the SX1257 SDR ASIC and amplifies it to +30dBm (1W) of output power.

This schematic also contains a power switch (it's the only way to turn off the PA) and a power level detection circuit.

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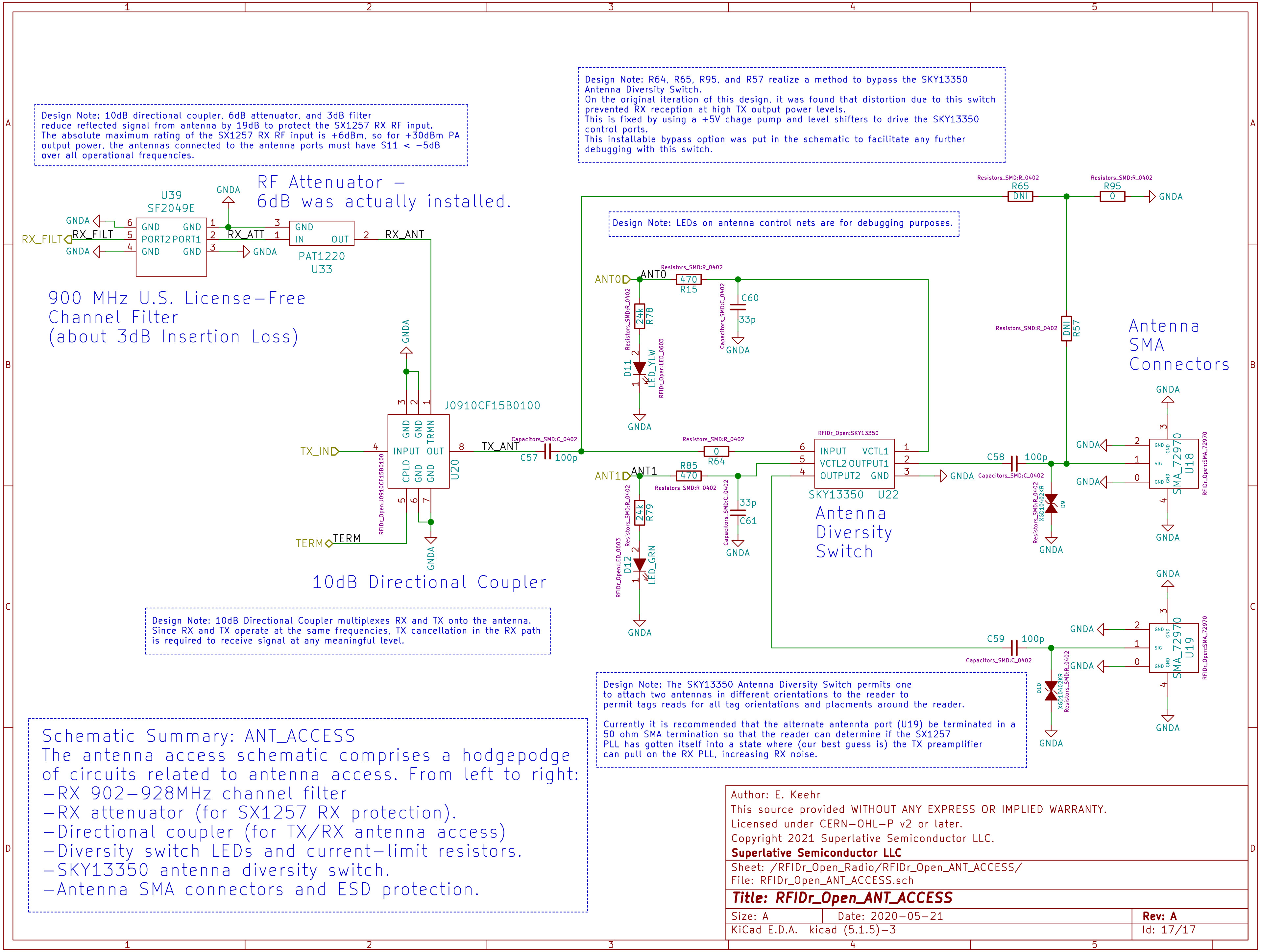

Design Note: 10dB directional coupler, 6dB attenuator, and 3dB filter reduce reflected signal from antenna by 19dB to protect the SX1257 RX RF input. The absolute maximum rating of the SX1257 RX RF input is +6dBm, so for +30dBm PA output power, the antennas connected to the antenna ports must have S11 < -5dB over all operational frequencies.

Design Note: R64, R65, R95, and R57 realize a method to bypass the SKY13350 Antenna Diversity Switch.
On the original iteration of this design, it was found that distortion due to this switch prevented RX reception at high TX output power levels.
This is fixed by using a +5V chage pump and level shifters to drive the SKY13350 control ports.
This installable bypass option was put in the schematic to facilitate any further debugging with this switch.

Design Note: LEDs on antenna control nets are for debugging purposes.

Design Note: 10dB Directional Coupler multiplexes RX and TX onto the antenna. Since RX and TX operate at the same frequencies, TX cancellation in the RX path is required to receive signal at any meaningful level.

Design Note: The SKY13350 Antenna Diversity Switch permits one to attach two antennas in different orientations to the reader to permit tags reads for all tag orientations and placments around the reader.

Currently it is recommended that the alternate antenna port (U19) be terminated in a 50 ohm SMA termination so that the reader can determine if the SX1257 PLL has gotten itself into a state where (our best guess is) the TX preamplifier can pull on the RX PLL, increasing RX noise.

Schematic Summary: ANT_ACCESS

The antenna access schematic comprises a hodgepodge of circuits related to antenna access. From left to right:

- RX 902-928MHz channel filter
- RX attenuator (for SX1257 RX protection).
- Directional coupler (for TX/RX antenna access)
- Diversity switch LEDs and current-limit resistors.
- SKY13350 antenna diversity switch.
- Antenna SMA connectors and ESD protection.

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