PowerPC Key Messages

- At inception PowerPC was developed as a **scaleable** architecture which would be deployed into the embedded market
  - Established the architecture in the computing market first
  - Focusing efforts on embedded and emerging markets
- PowerPC is one of three strategic processor architectures for Motorola moving into the next century
  - Highest performance, long-term support, corporate commitment
  - Most extensive architecture product porfolio in the industry
  - AltiVec extension to PowerPC architecture provides high-performance high-bandwidth computational capability
  - Continuing to expand the PowerPC portfolio with microprocessors and integrated devices
- Motorola is a technology leader
  - 1998 sales of 89M units of 32-bit microprocessors
  - Selected as Number One Preferred Embedded Processor Supplier in all categories in 1998 EETimes Embedded Systems Survey
  - PowerPC Architecture chosen for current and planned embedded designs more than any other architecture in 1998 EETimes Embedded Systems Survey

PowerPC: The Choice for Embedded Designs

- Superscalar RISC Architecture: Maximum Performance & Flexibility
  - Offers a wide range of cost-effective, high-performance, low-power solutions
  - Instruction-set compatibility across entire product line, from integrated controllers to leading-edge processors
  - Expanded capability with the AltiVec™ technology and new SIMD instructions
- Compelling Price/Performance Ratio
- Aggressive Technology/Process Roadmap
  - Excellent power/performance quotient
- Strong footprint compatibility across broad performance range
- Separate Address and Data busses for maximum performance
- Extended Temperature and Multiprocessing Versions Available
- Broad selection of development tools
  - PowerPC processors are supported by more than 40 RTOSes, including Sun Chorus, Enea OSE, Green Hills velOSity, ISI pSOS, LynxOS, Microware OS-9, and WindRiver VxWorks
- Commitment to support PowerPC long term
  - Continue to foster architecture development and broaden product line
  - Product line longevity

PowerPC Announcements

- **MPC7400, Motorola's first G4 processor, with AltiVec™ technology**
  - Showcased products from multiple customers at Horizons press event, 9/13-14/99
  - Frequencies up to 500-MHz announced on 8/31/99
  - New vector execution unit with 128-bit data paths and registers
  - Provides SIMD operation and acceleration for many types of code
- **MPC755 and MPC745 disclosed at Embedded Processor Forum**
  - New embedded features added to G3 family
- **MPC750 now available up to 400 MHz**
  - G3 processor at higher speeds with 1.9V core and lower power dissipation
  - 740 also offered in the new process at 333 MHz
- **MPC8240 and MPC8260 - High-performance Integrated Processors**
  - Both combine 603e processor core with on-chip peripheral logic
  - MPC8240 supports 64-bit 100-MHz memory, 32-bit 66-MHz PCI, DMA and other embedded features
  - MPC8260 provides enhanced Communication Processor Module

PowerPC in Publications

- PowerPC G3 performance recognized by Publish magazine
  - September 2, 1998: Motorola was noted as a winner of their sixth annual Publish Impact Awards
  - MPC750 praised for its advanced technology manufacturing process, its optimized design, and for its new, more efficient approach in handling the level 2 cache memory
- PowerPC 750 was given the Editor's Choice award for Best RISC Processor of 1997 by Microprocessor Report

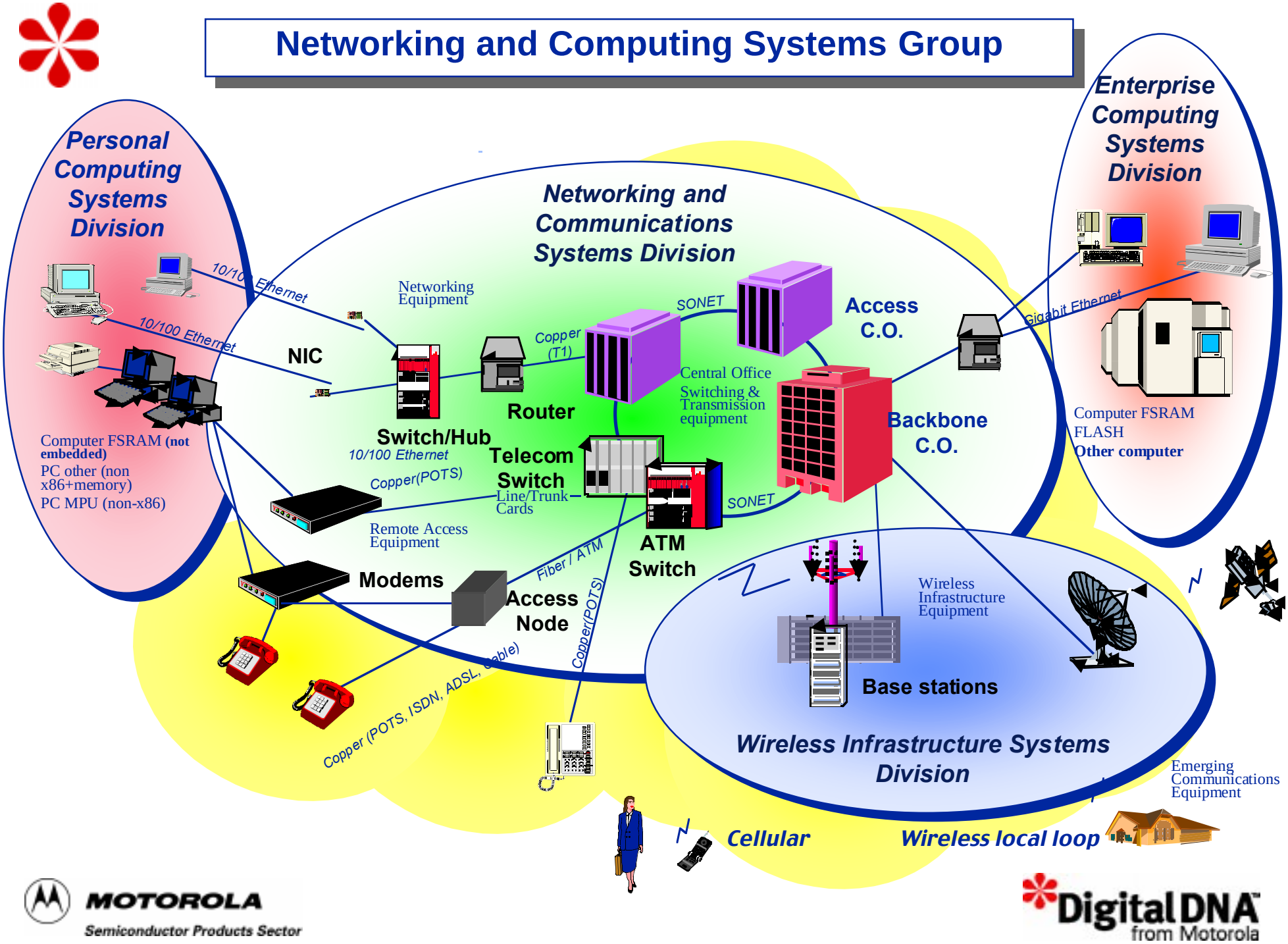
PowerPC 750

Editor's Choice: 1997 RISC Processor of the Year

--Microprocessor Report 12-29-97

PowerPC MOTOROLA

Networking and Computing Systems Group



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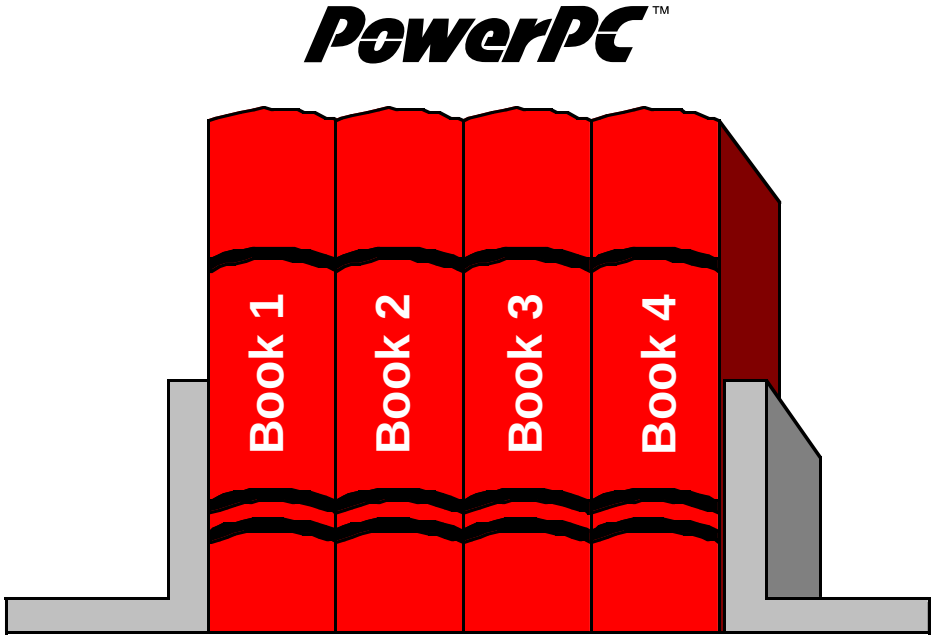
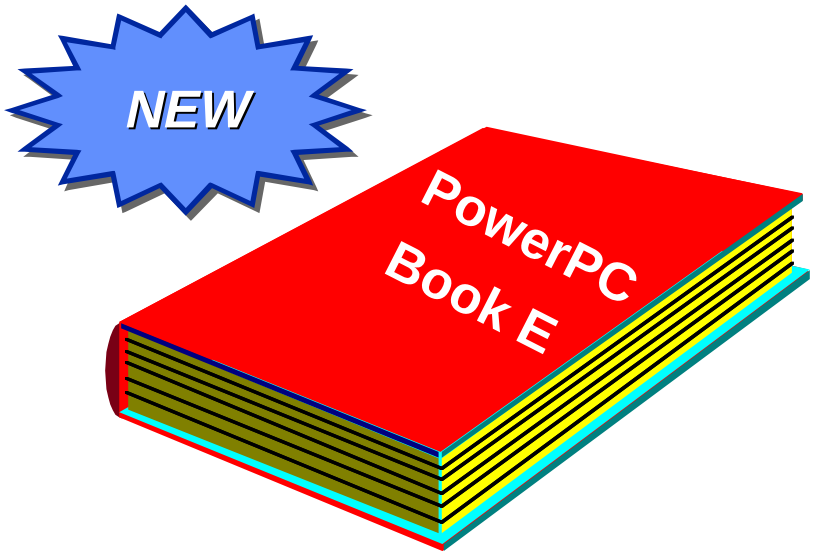
Updates to the AIM alliance

- June 11, 1998: Motorola SPS announces taking 100% ownership of Somerset PowerPC design center from IBM
- Somerset incorporated as the foundation of the core technology group within NCSG under Bertrand Cambou
- PowerPC will continue and grow as the leading-edge performance architecture of Motorola SPS
- Motorola will continue to preserve compatibility via architectural agreement with IBM
- Motorola and IBM will continue second-source agreement for current dual-source parts and reserve the right to engage in partnership on future devices
- Book “E” embedded agreement and architectural board will allow expansion and revision of the architecture to address specific market needs, while preserving architectural compatibility

The PowerPC Architectural Definition





Current PowerPC Definition contained in 4 books

- Book 1: PowerPC user mode instructions
- Book 2: Memory model, Cache control, etc.
- Book 3: Supervisor level
- Book 4: Device specific details

Compilation of Books 1-3 are available in "PowerPC Microprocessor Family: The Programming Environments for 32-Bit Microprocessors" (doc# MPCFPE32B/AD REV.1)

Book E to define embedded specific architecture

- Based on established PowerPC architecture
- Software-compatible with existing PowerPC Designs
- Motorola and IBM's new embedded designs will converge around Book-E compatibility

What is “Book E”?

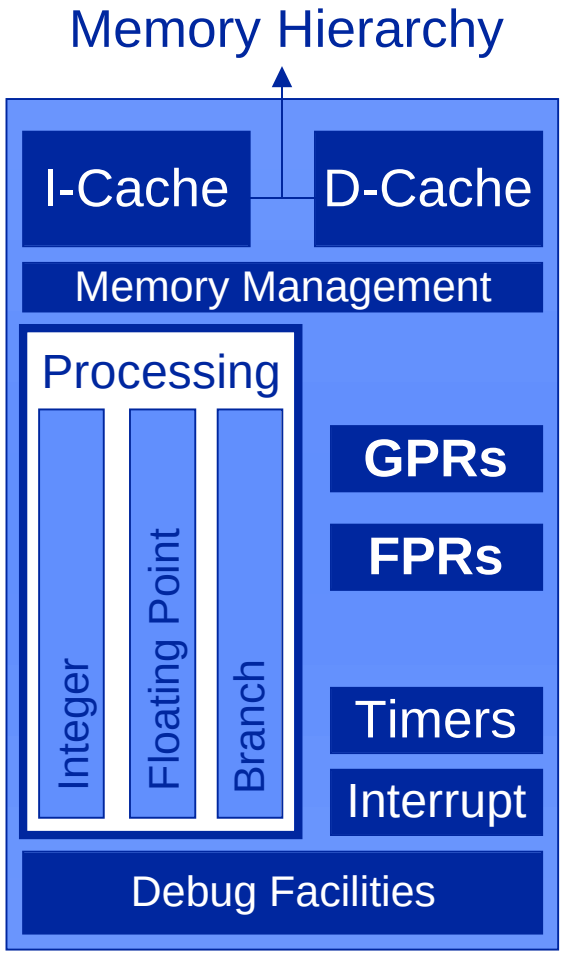
- Book E is the project name for the collaborative effort between Motorola and IBM to enhance the PowerPC Architecture™
- Book E is a complete architectural definition, not just an addendum to the PowerPC Architecture
- Book E objectives:
  - Provide an enhanced architecture definition with 64-bit capabilities
  - Increase architectural flexibility
  - Deliver optimizations specific to embedded systems
  - Eliminate non-substantive architectural differences in future IBM and Motorola embedded PowerPC implementations
  - Provide compatibility for existing PowerPC applications
- The Book E specification is available today at:

  http://motorola.com/PowerPC

  http://www.chips.ibm.com/products/powerpc

Complete 64-bit architecture

- 64-bit addressing required for high-performance apps (e.g. RAID, networking, telecom)
- 64-bit Book E processors can execute 32- and 64-bit applications
  - Supports 32-bit legacy code
- Book E allows 32-bit or 64-bit processor implementations
  - Optimize cost and performance for diverse system requirements



Book E Features

- Book E allows Application-Specific Processing Units (APU) for instruction set extensions
  - An APU design can be:
    - » Simple, sharing use of GPR file
    - » Complex, separate AP register file with direct load/store access
- Unified 32-/64-bit architecture and MMU, without modes
  - Single MMU covers both 32- and 64-bit address translation
  - Easier OS migration
  - 84 new instructions for 64-bit addressing and extended arithmetic
- Adaptable memory management for diverse operating environments
  - Architected software-managed TLB
    - » System defines page table size, location, organization, supported page sizes, and TLB replacement strategy
  - Variable page sizes, 1KB to 1TB
    - » More efficient memory allocation
    - » Compact TLB can map large memory
- High-performance memory architecture
  - Improved memory barrier mechanisms
  - Support for cache locking
    - » Architected exception types and vectors for lock-related errors

Book E Features, con't

- Two interrupt priority levels for real-time systems
  - Critical interrupt level for critical input, debug, watchdog
    - » Low latency response to high-priority devices
    - » Robust software debug of non-critical handlers
  - Non-critical interrupt level for TLB miss, memory protection, illegal op-codes, etc.
- Robust debug for high-performance systems
  - Architected debug framework for application developers and tool vendors
    - » Instruction address compare
    - » Data address compare
    - » Other debug events
  - Architecture permits subset of debug facilities
- Expanded timer facilities for hard real-time constraints
  - 64-bit time base register, for general system time maintenance
  - Improved 32-bit decrementer
    - » Auto-reload and auto-stop modes
    - » SW timer for multitasking
  - Fixed interval timer, for periodic system maintenance
  - Watchdog timer, for system error recovery

Book E Architectural Compatibility

- Backward and forward compatibility with existing PowerPC implementations
  - Previous PowerPC 32-bit application binaries will run unmodified on new Book E implementations
  - New Book E 32-bit application binaries will run unmodified on previous PowerPC implementations
- Improvements for system software
  - Significant enhancements for RTOS memory management
  - More robust interrupt handling
- Consistent architecture for application and tool developers

PowerPC™ Embedded Customers - Public

- **Networking**
  - 3Com
  - Advanced Fibre Communications
  - Aptis
  - Aware
  - Bay Networks
  - Diba
  - Foundry Networks
  - Motorola ISG
  - Neoware
  - RPCG
  - Paradyne
  - Samsung
  - Visual Networks
- **Networked Printers**
  - Kyocera
  - Fuji Xerox
  - Xerox
- **Networked Storage**
  - Data General Clariion
- **Various Embedded**
  - Cetia
  - CSPI
  - DY 4 Systems
  - Force Computers
  - Heurikon
  - Huawei-China
  - Kodak
  - Konami
- **Various Embedded Continued**
  - LeCroy
  - MA Lighting
  - Mercury Computer Systems
  - Motorola MCG
  - NEC
  - Newbridge Networks
  - Omnibyte
  - PEP Modular Computers
  - Radstone Technology
  - Sega
  - Sky Computers
  - Smart Modular Technologies
  - Synergy Microsystems
  - Tadpole Technology
  - Transtech Parallel Systems
  - V•I Computer
  - Vul Computer
- **Telecom**
  - ABB Switchgear
  - ADC Kentrox/Telecom
  - Brooktrout
  - Fujitsu
  - Lucent
  - Marconi
  - Motorola CIG
  - Nortel
  - Paradyne
  - Performance Technologies
  - Telrad

PowerPC Applications and Markets

PowerPC™ Applications and Markets	603e EC603e	8240	75x 74x	821 823 823e	85x 860 8260	505 509 555	MPC7400 AltiVec
Networking Infrastructure	●	●	●		●		●
Telecom Equipment	●	●	●		●		●
Printers & Imaging	●	●			●		●
Industrial Control	●	●	●	●		●	●
Symmetric Multiprocessing							●
Network Computers & Thin Clients	●	●	●	●	●		
Internet Access Devices	●	●		●	●		
Home Entertainment	●	●		●	●		
PDAs & Personal Communications				●			
Digital Cameras				●			
Automotive Powertrain				●		●	
Car Navigation Systems & GPS				●		●	
Avionics	●	●	●				●
Notebook and Desktop Computers			●				●

Motorola's PowerPC Families

CPUs

G4 Family

* Highest performance processors with AltiVec™ technology
* G4 architecture based on G3 family with new features
* More powerful FPU, support for SMP, enhanced system bus

G3 Family

* High performance processors with backside L2 cache I/F
* Larger internal caches, second integer unit added over G2
* SW compatible with complete line of G2 CPUs

G2 Family

* Ultimate low-cost, low-power CPU solution
* 32 or 64 bit data bus for design flexibility
* Ceramic BGA packaging now, PBGA in progress

Integrated Devices

MPC800 and MPC8000 Family

* Highly integrated designs
* PowerPC core with on-chip peripherals
* Utilized for internetworking, data communications, storage devices, and portable electronics

MPC500 Family

* From Transportation Systems Group
* Automotive and other high-end controller applications requiring integrated part w/ FPU

HiPerMOS Process Roadmap

Dual Inlaid Copper with SiOF Low K ILD

Dual Inlaid Copper Interconnect

TFSOI

HiPerMOS 7
0.10 - .08
1.2 volts

HiPerMOS 6
0.13 - .10
1.5 volts

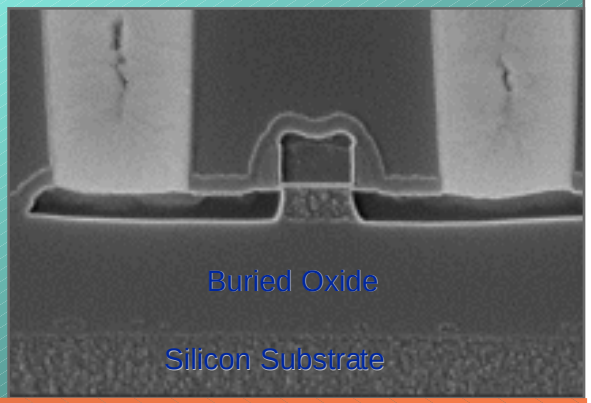
HiPerMOS 5
0.15 - .12
1.8 volts

HiPerMOS 4
0.18
1.8 volts

HiPerMOS 3
0.27
2.5 volts

HiPerMOS 2
0.35
2.5 volts

HiPerMOS 1
0.50 - L-Effective Physical Gate Length
3.3 volts



Process Performance

Production Dates

1994 | 1995 | 1996 | 1997 | 1998 | 1999 | 2000 | 2001

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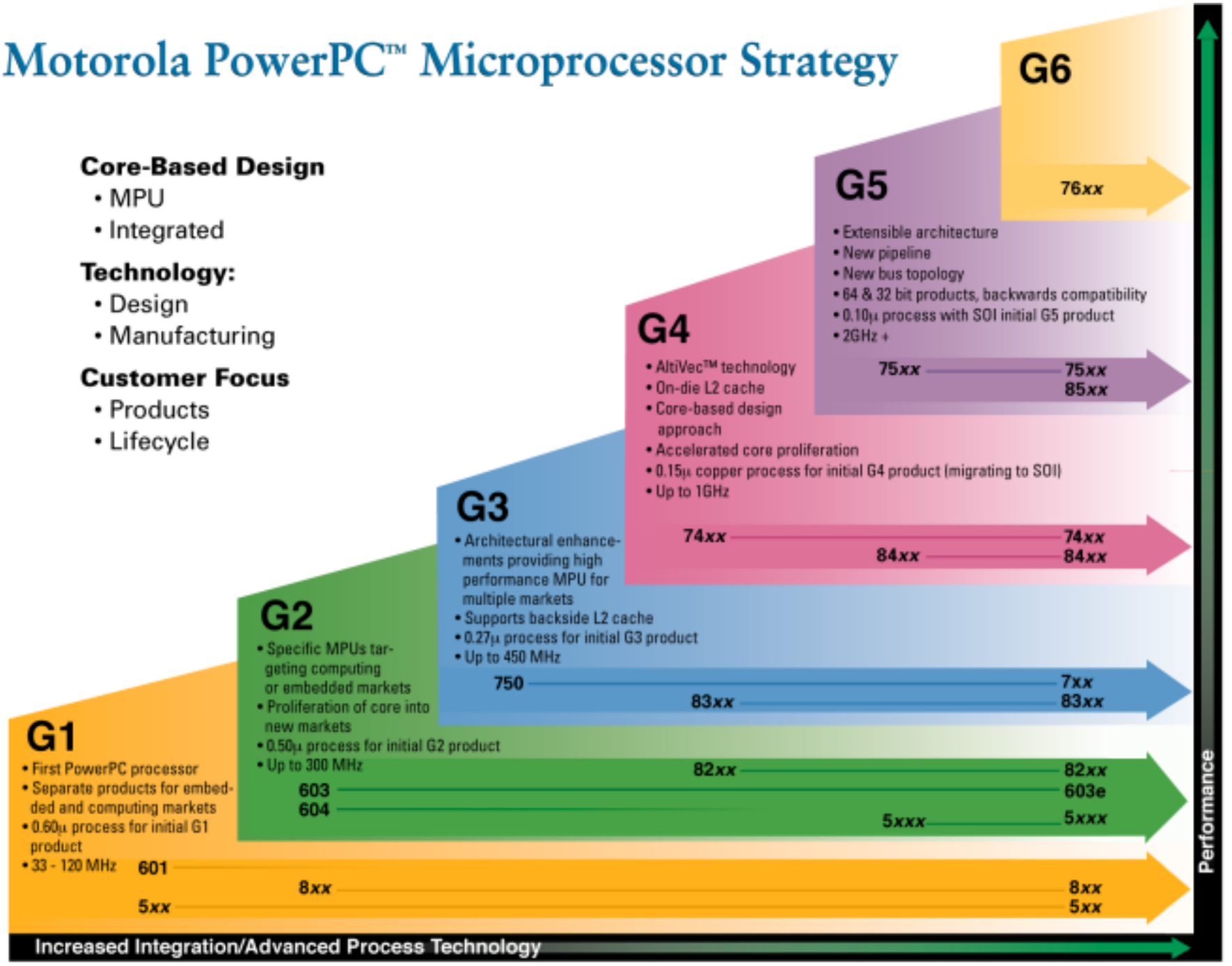
Motorola PowerPC™ Microprocessor Strategy

Core-Based Design
- MPU
- Integrated

Technology:
- Design
- Manufacturing

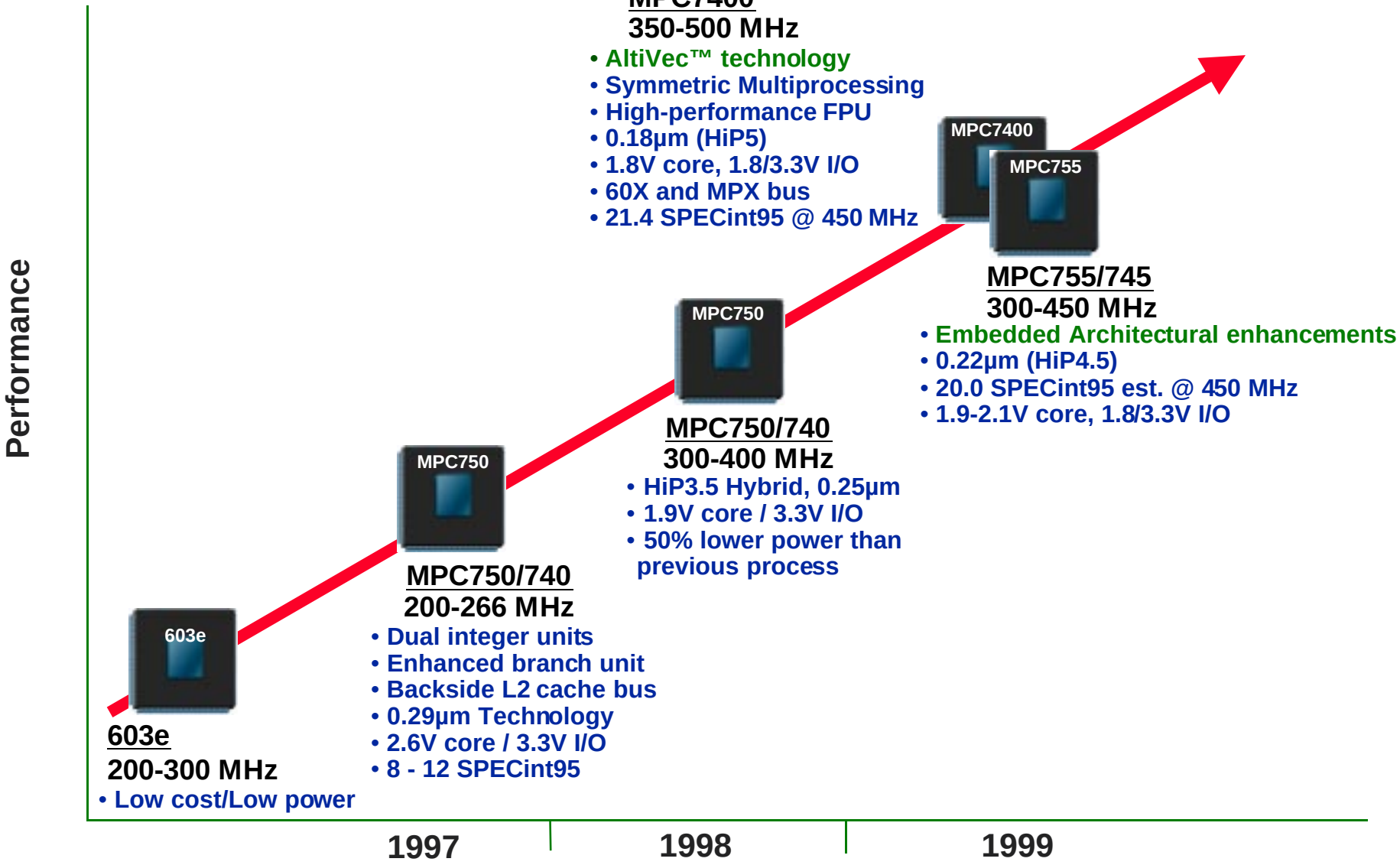
Customer Focus
- Products
- Lifecycle



1991 — 200x

6xx, 7xx, 7xxx — high performance microprocessor targeting computing and high-end embedded
8xx, 8xxx — integrated processor targeting the communications and consumer markets
5xx, 5xxx — integrated processor targeting the Transportation market

Motorola PowerPC Microprocessor Roadmap



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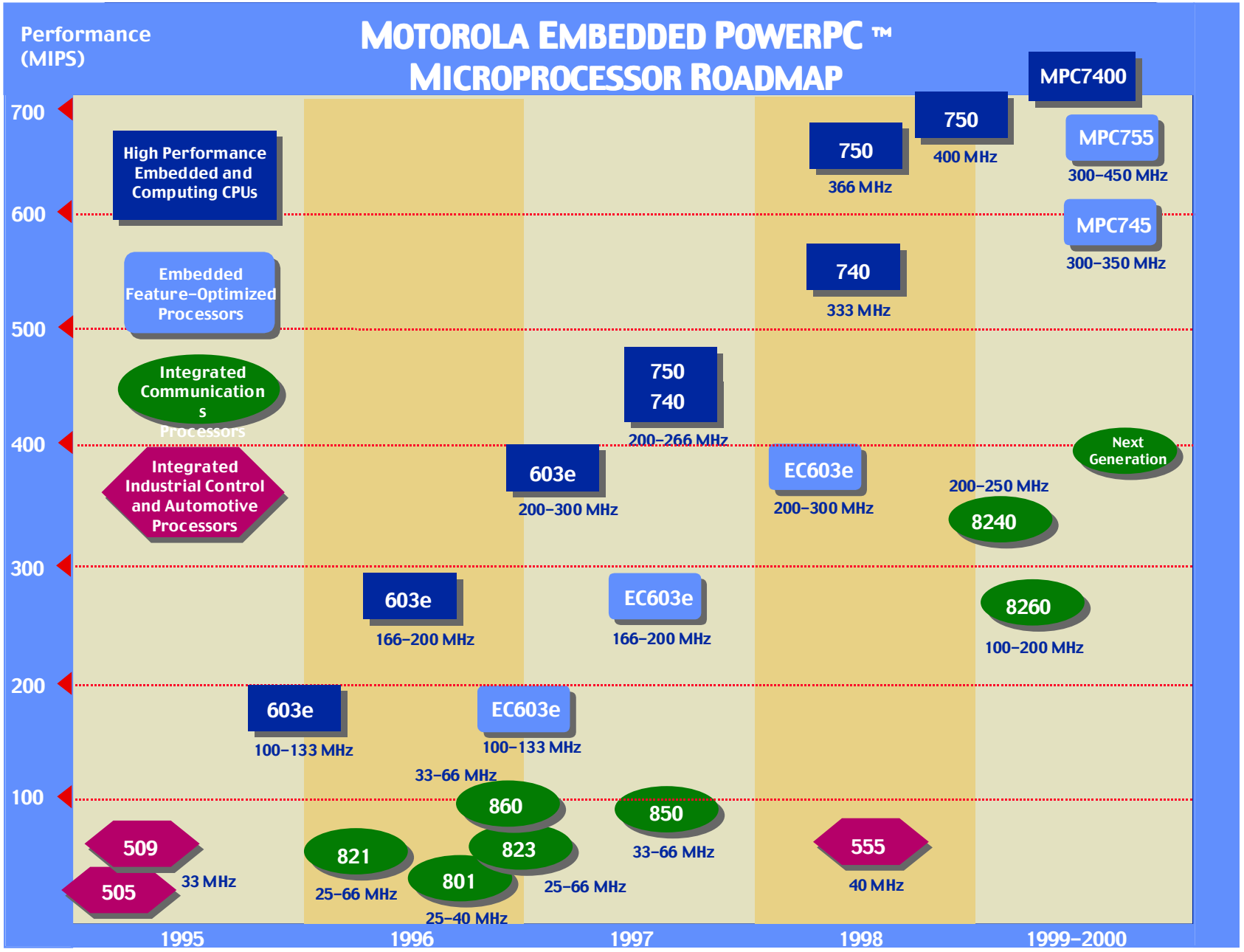

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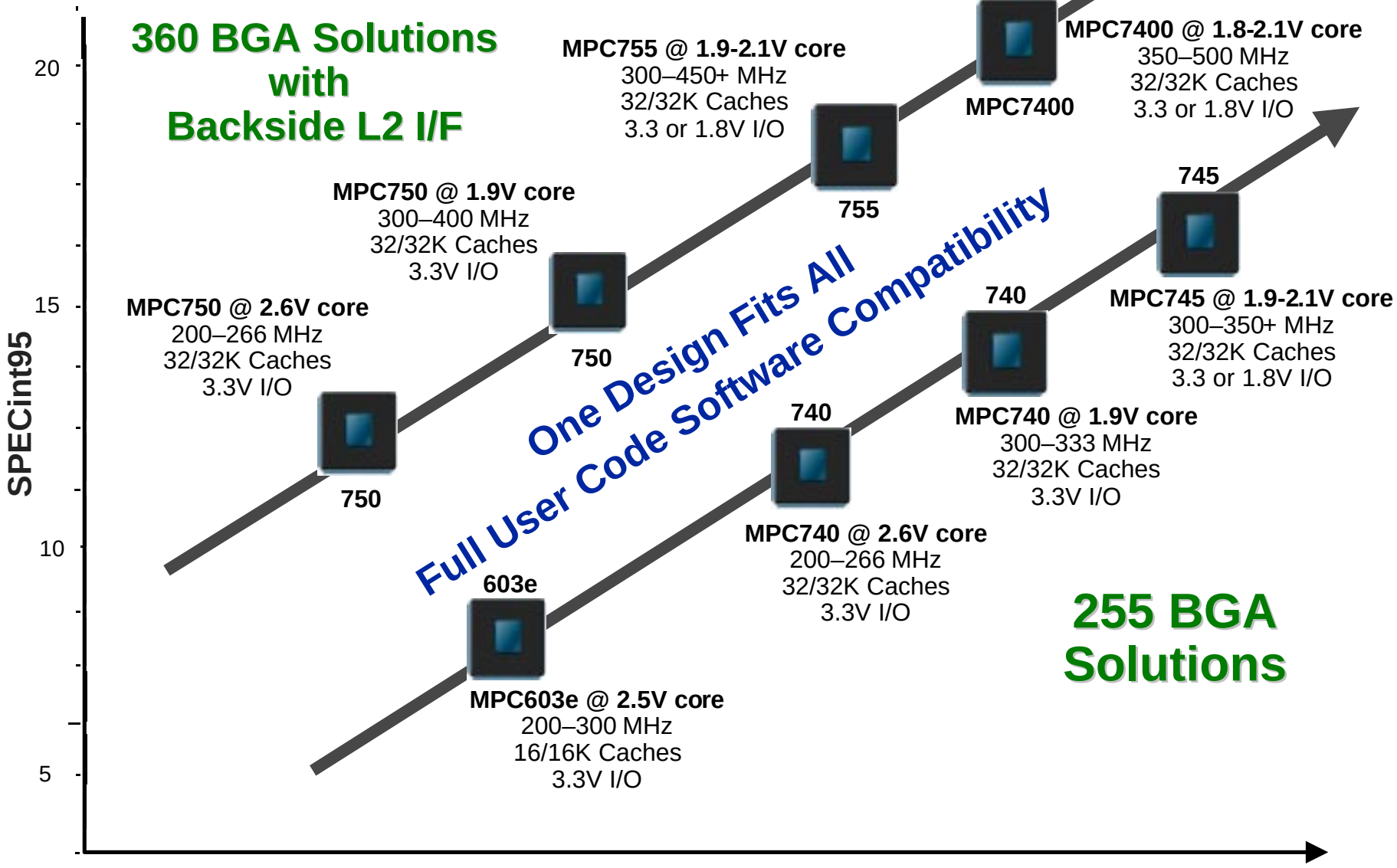
PowerPC *Footprint* Compatibility



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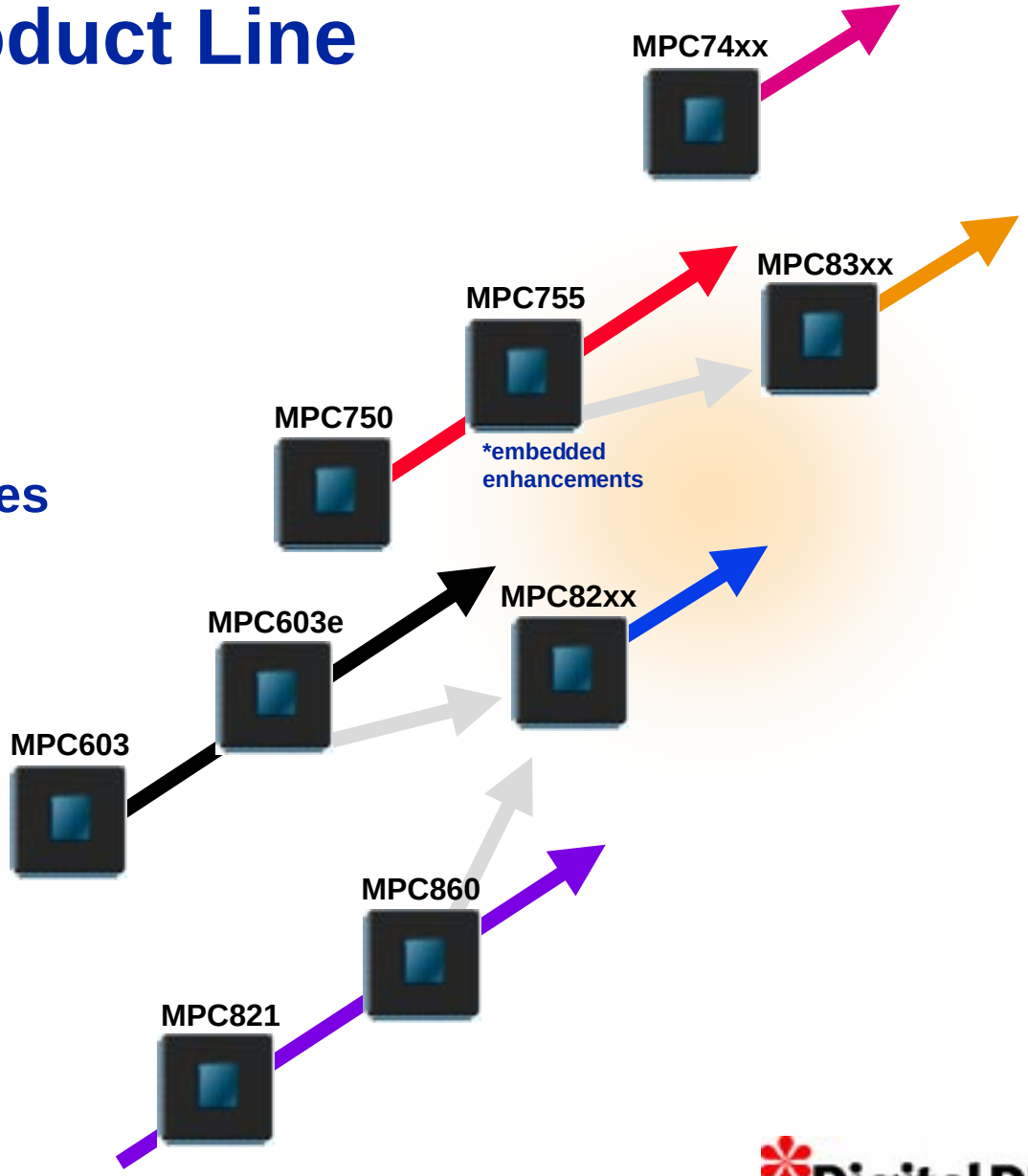
Motorola Embedded PowerPC Product Line

- High performance microprocessors
- Highly integrated devices
- Technologies from each combine to create new best-in-class products



Smaller, Cooler, Faster

- Continual process evolution provides faster processors with reduced power requirements
- All parts share same 60X bus interface and 255 CBGA footprint
- Core voltages will change with process technology
- I/O voltages will change at a slower rate
- Manufacturing efficiencies will allow regular pricing reductions

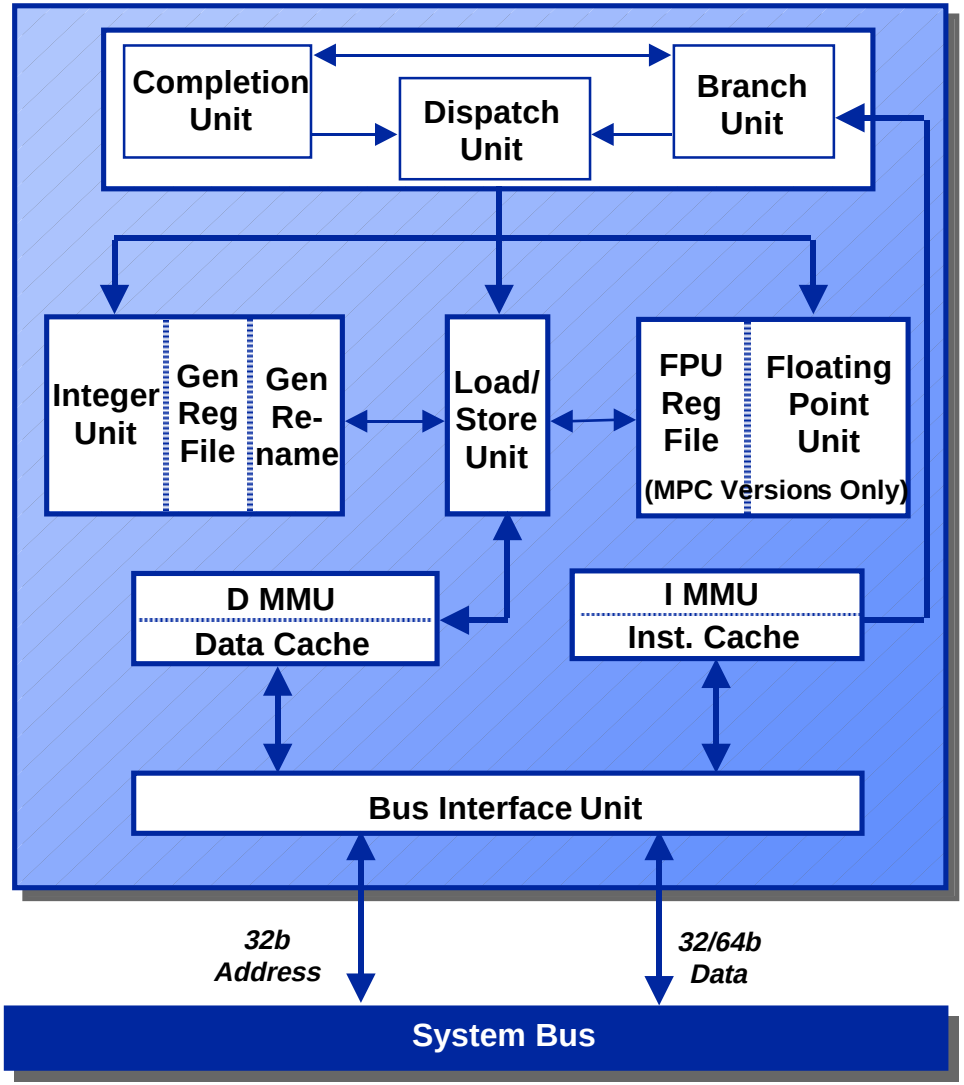
603e	**603p**	**603r**
100-133 MHz	166-200 MHz	200-300 MHz
98 sq mm	81 sq mm	42 sq mm
3.3V core	2.5V core	2.5V core
4.2W	4.0W	4.0W

MPC/MPE603e Overview

- **Features**
  - Superscalar (3 IPC)
  - Dual 16KB caches, Dual MMUs
  - Double precision FPU (MPC versions only)
  - On-chip debug support (JTAG/COP)
- **Power Management**
  - Dynamic power management on decode
  - Low power static design
  - Nap and doze and sleep modes for power savings with bus snoop in doze mode
- **Performance**

	MIPS	SPECint95 (est)	SPECfp95 (MPC only)
– 133 MHz	188	3.9	3.1
– 200 MHz	283	5.6	4.0
– 300 MHz	423	7.4	6.1

- **Technology**
  - 0.5 and **0.29 µm** CMOS
  - 3.3V -> **2.5V core**, 3.3V I/O (5V I/O tolerant)
  - 240 pin CQFP (up to133 MHz) or **255 CBGA**
  - 100, 133, **200, 266, and 300** MHz
- **Schedule**
  - MPC and MPE Production Now for all speeds
  - Also available in industrial temp
  - 200-MHz (HiP 3) to be offerred in **Plastic BGA** - available 2H99



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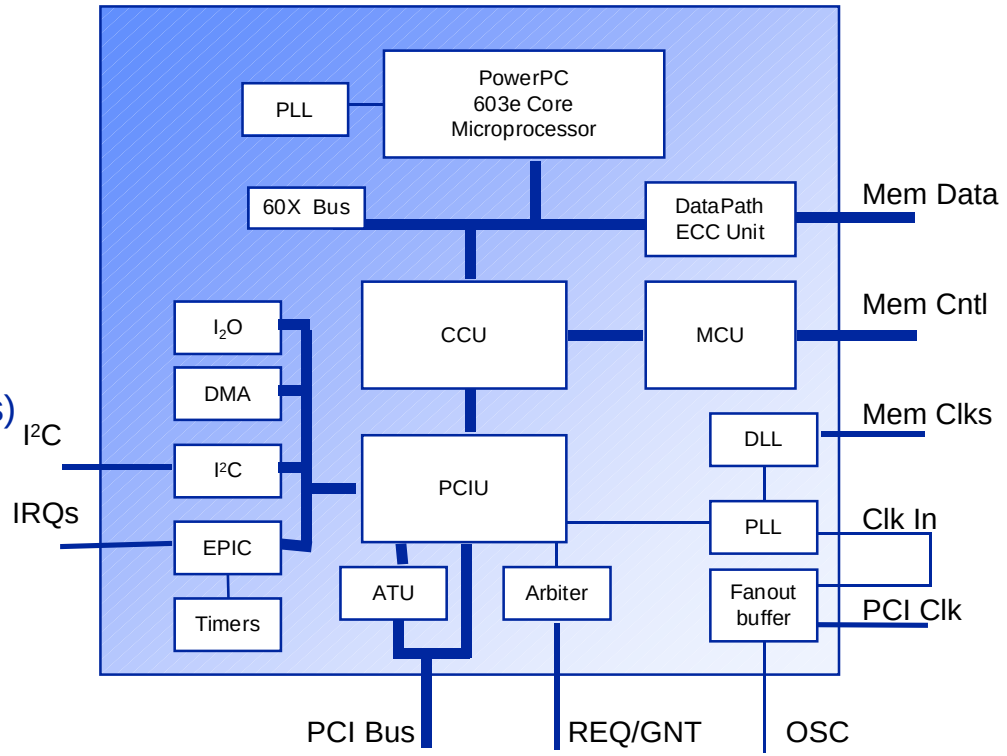
MPC8240 Overview

➤ Features

- Integrated 100 to 250 MHz 603e core microprocessor
  - » Cache-locking (3 of 4 ways)
- Integrated 32-bit PCI:
  - » 33 & 66 MHz PCI 2.1 compliant interface
  - » Big and Little-endian support
  - » Master and Agent mode support
  - » PCI Arbiter
- Integrated memory control (up to 100 MHz):
  - » Bus width 32- or 64-bit
  - » DRAM (SDRAM, FPM, EDO) Up to 1GB
  - » Parity / ECC Support for EDO and SDRAM
  - » ROM/Flash ROM (up to 16MB)
  - » Port X interface
- 2-Channel DMA (Direct and Chaining Modes)
- Messaging Unit (I_2O) and I^2C support
- EPIC Interrupt Controller
- Address Translation Unit
- Clock generation for PCI, Memory
- Integrated power management
- Performance Monitors
- JTAG Boundary Scan Support



➤ Technology

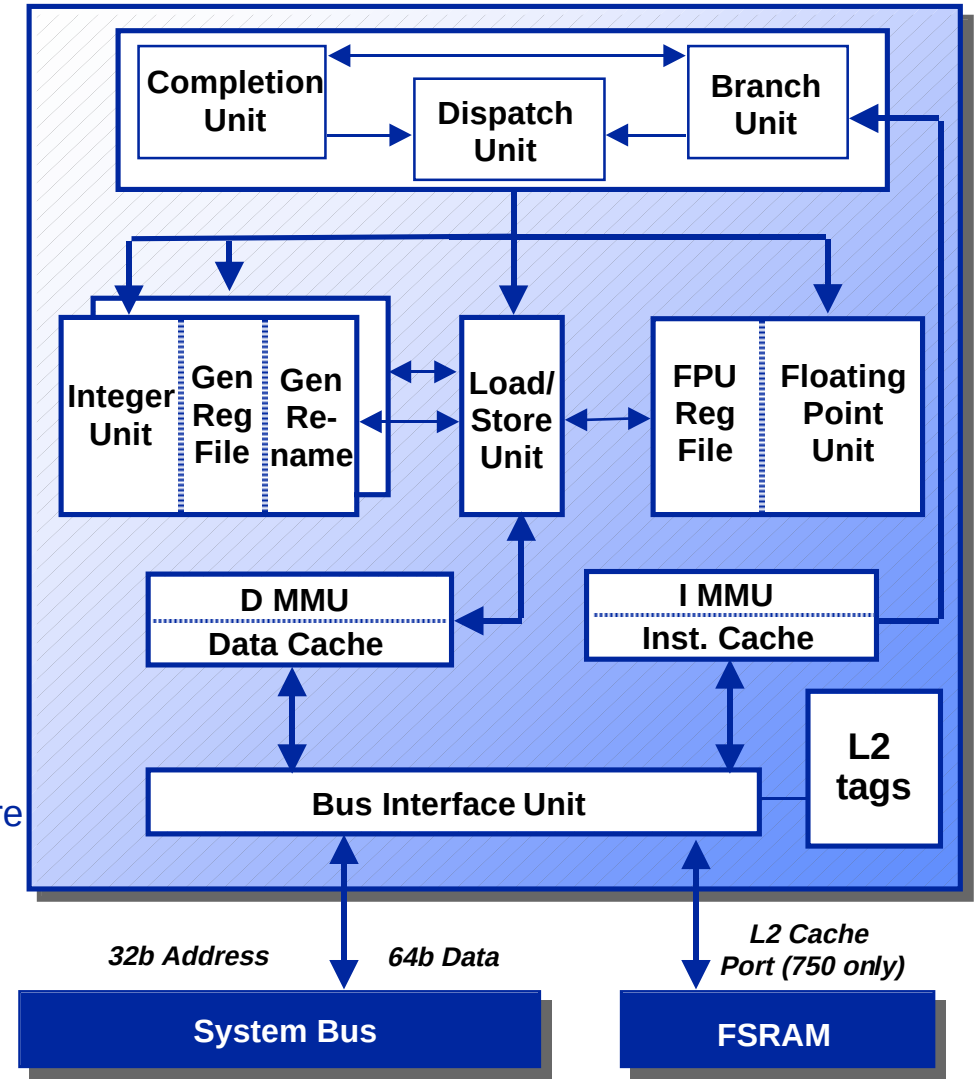
- 0.35µm CMOS, 2.5V core, 3.3V I/O, 5V tolerant on PCI bus
- Offered at 200 and 250 MHz; see spec for lower frequency operation
- 352-pin TBGA

➤ Schedule

- Production Now
- Extended temp planned for 1Q00

MPC750 and MPC740 Overview

- **Features**
  - Superscalar (3 IPC: 2 Instructions + Branch)
  - Dual 32KB Instr & Data non-blocking caches, Dual MMUs
  - Hardware Tablewalk
  - Double precision FPU
  - On-chip debug support (JTAG/COP)
  - External L2 cache interface on MPC750 with integrated controller and cache tags, 256 KB, 512 KB & 1 MB 2-way set associatively
- **Power Management**
  - Dynamic power management on decode
  - Low power static design
  - 3.4W power consumption (typ) @ 300MHz
  - Nap, doze and sleep modes for power savings
- **Performance Estimate**
  - 17.7 SPECint95 @ 400MHz (18.8 peak)
  - 11.7 SPECfp95 @ 400MHz (12.2 peak)
- **Technology**
  - **0.29**/0.25µm CMOS, 3.3V I/O, 2.6V or 1.9V core
  - 255 BGA (740), 360 BGA (750)
  - **200, 233, 266**, 300, 333 MHz for 740/750
  - 366 and 400 MHz avail in 750 package
- **Schedule**
  - **200-266 (2.6V)** in Production Now; Industrial Temp also available
  - 300-400 (1.9V) in Production Now



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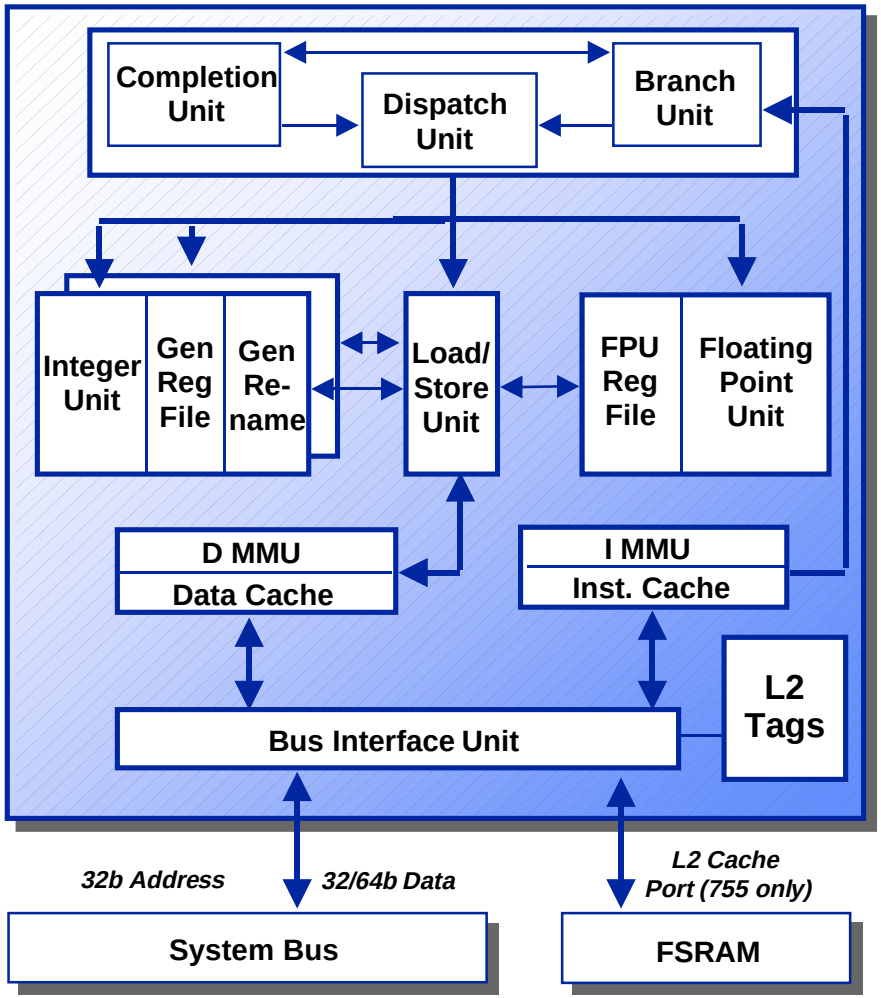
Motorola's MPC755 and MPC745

- **Features**
  - Footprint compatible with MPC750 and MPC740
  - Superscalar (3 IPC: 2 instructions + branch)
  - 32KB instr & data non-blocking caches, dual MMUs
  - Hardware tablewalk
  - **Optional software tablewalk**
  - Double precision FPU
  - External L2 cache interface with integrated controller and cache tags for up to 1MB on MPC755
  - **Cache locking (6 of 8 ways or entire cache lockable)**
  - **8 iBAT and 8 dBAT registers**
  - **Direct mapped SRAM capability (L2 tags bypassed)**
  - **Address parity on L2 cache (hashed w/ data parity bits)**
  - **32-bit data bus support**
  - On-chip debug support (JTAG/COP)
- **Power Management**
  - Dynamic power management on decode
  - Low power static design
  - Doze, nap, and sleep modes for power savings
- **Performance/Power Estimate**
  - **20.0 SPECint95 (est) @ 450 MHz**
  - **Less than 4.5 watts typical @ 400 MHz**



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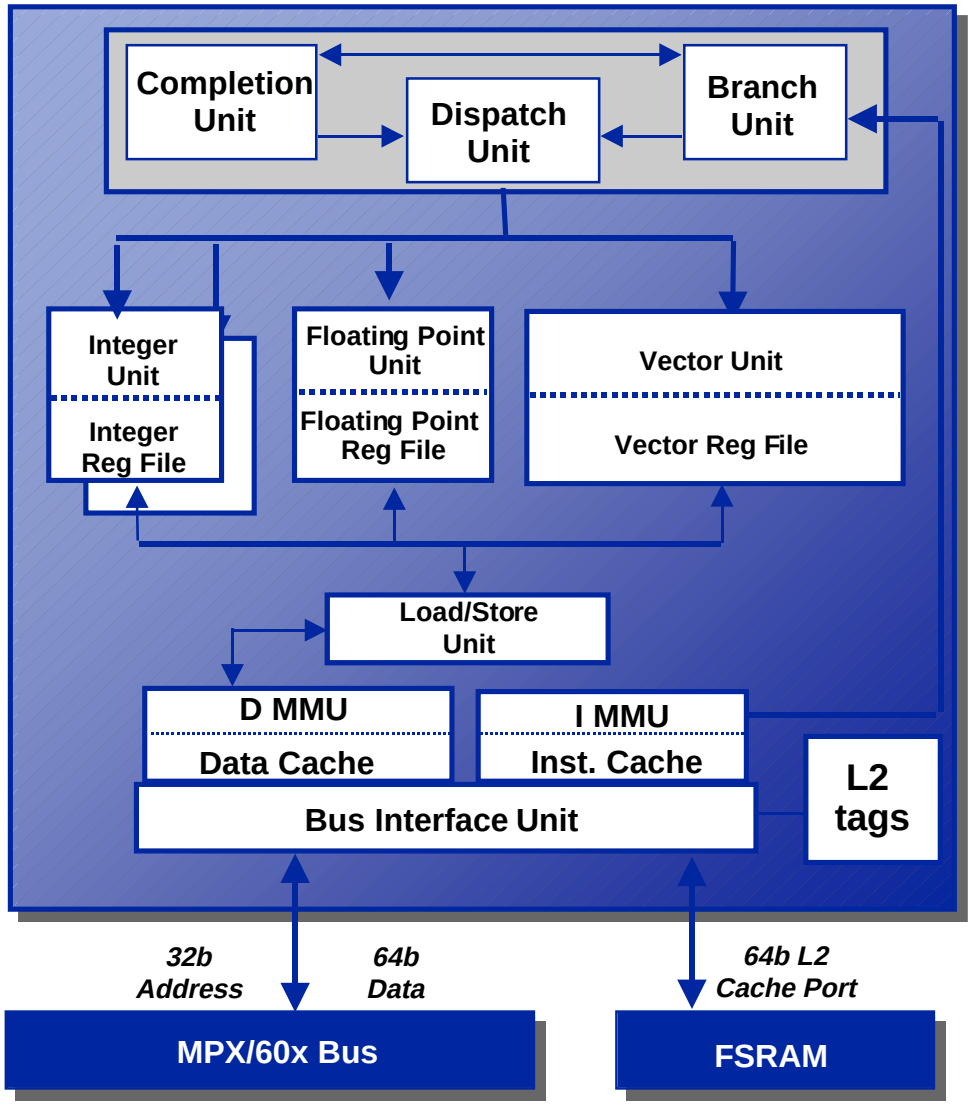
MPC7400 Overview

- **Features**
  - High frequency superscalar PowerPC core
  - High performance FPU provides faster multiplication
  - **AltiVec™ Technology**: 128-bit wide Vector Unit
    - Ideal for SIMD algorithmic data processing
    - 128 bit acceleration for non-vectorizable code
  - Expanded Memory SubSystem bandwidth with 128-bit wide internal paths
  - Dual 32KB Instruction & Data caches
  - Up to 2 MB backside L2 cache with support for Late Write SRAM and BurstRAM
  - High Bandwidth MPX Bus (also 60x bus mode)
  - Full symmetric multiprocessing (MERSI) capability
  - On-chip debug support (JTAG/COP)
- **Power Management**
  - Nap, doze and sleep modes for power savings
  - Low Power Dissipation for embedded applications
- **Technology**
  - 0.15µm HiP5.6, 1.8-2.0V core, 1.8/3.3V programmable I/O, 1.8/2.5/3.3V programmable L2
  - 360 CBGA, 83 mm^2 die size
  - 350 - 500 MHz (L & N specs)
- **Performance Estimate**
  - 21.4 SPECint95 @ 450 MHz
- **Schedule**
  - Production - Up to 450 MHz Now — 500 MHz planned for 4Q99



altivec technology

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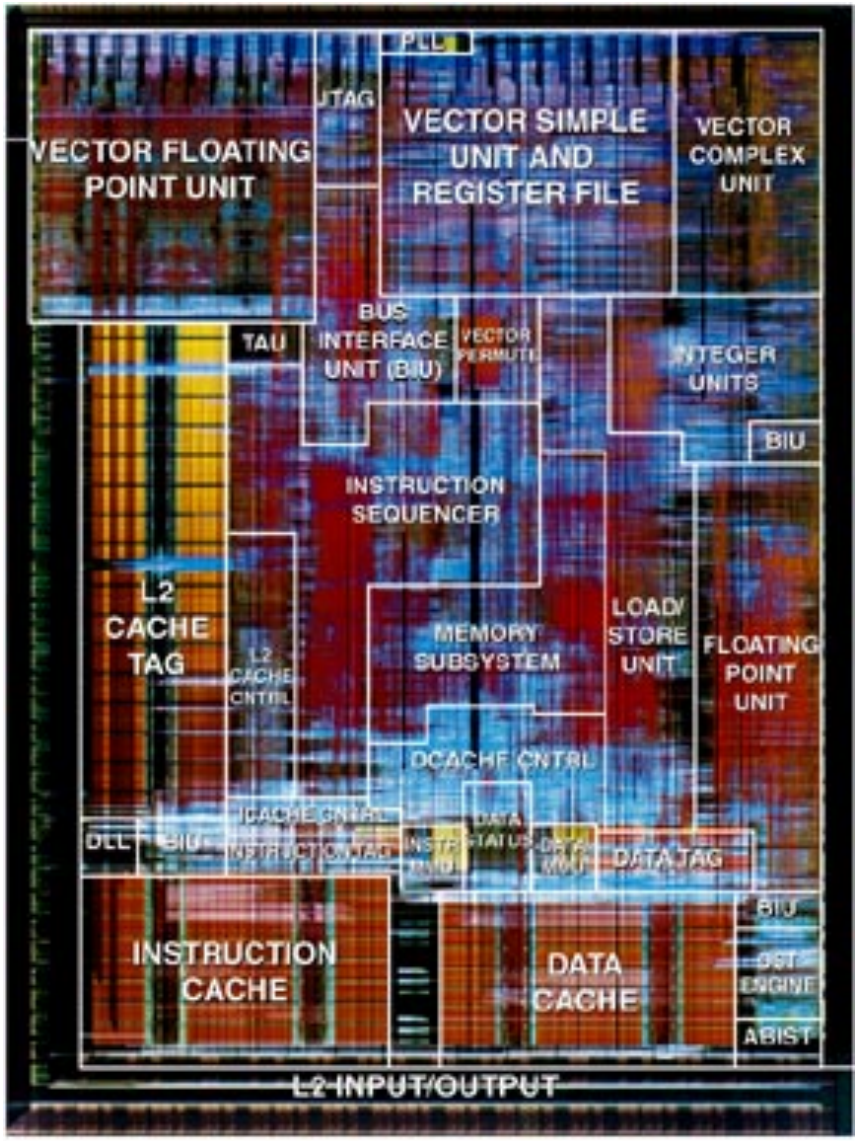
MPC7400 – Motorola's Fourth-Generation PowerPC™ Microprocessor



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Digital DNA™ from Motorola

G4 Product Goals

- Ultra high-bandwidth capability
- High-performance algorithm engine
- Maximize floating-point performance
- 100% compatibility with existing PowerPC™ Architecture
- Full symmetric multiprocessing support
- Provide upgrade path for existing systems
- Provide these features & performance without exceeding the third-generation PowerPC model of sub-100mm^2 die with under 10 Watt typical power dissipation

G4 Markets and Applications

Computing Market Applications

* High performance computing systems
* 3D Graphics
  * Games, Entertainment
  * High precision CAD
* High bandwidth data communications
* Real-time Continuous Speech I/O
* Soft-Modem: V.34, 56K, G.lite
* Motion Video
  * MPEG2, MPEG4
  * H.234
* High Fidelity Audio
  * 3D Audio, Dolby Digital (AC-3)
* Virtual Reality

Embedded Market Applications

* Access Concentrators/DSLAMs
  * ADSL and Digital Data Concentrators
* Speech Recognition
* Voice/Sound Processing
* Image and Video Processing
* Array Numeric Processing
* Basestation Processing

G4 Performance

- Benchmarks (estimated)
  - SPECint95 21.4
  - SPECfp95 20.5

    at 450 MHz with 2 MB backside L2 at 2:1 and a 100MHz memory bus
- AltiVec Applications Performance (measured)
  - Embedded and computing market examples
    - FIR Filters
      - 9x speedup over PowerPC without AltiVec Technology
      - Sustained performance of 5 taps/cycle for 16-bit real FIR
    - Encryption/key generation
      - 15x speedup over PowerPC without AltiVec Technology for Diffie-Helman key exchange
    - Image Processing
      - 11x speedup over PowerPC without AltiVec Technology solution for cycles/pixel on median filtering

Motorola PowerPC CPU Summary

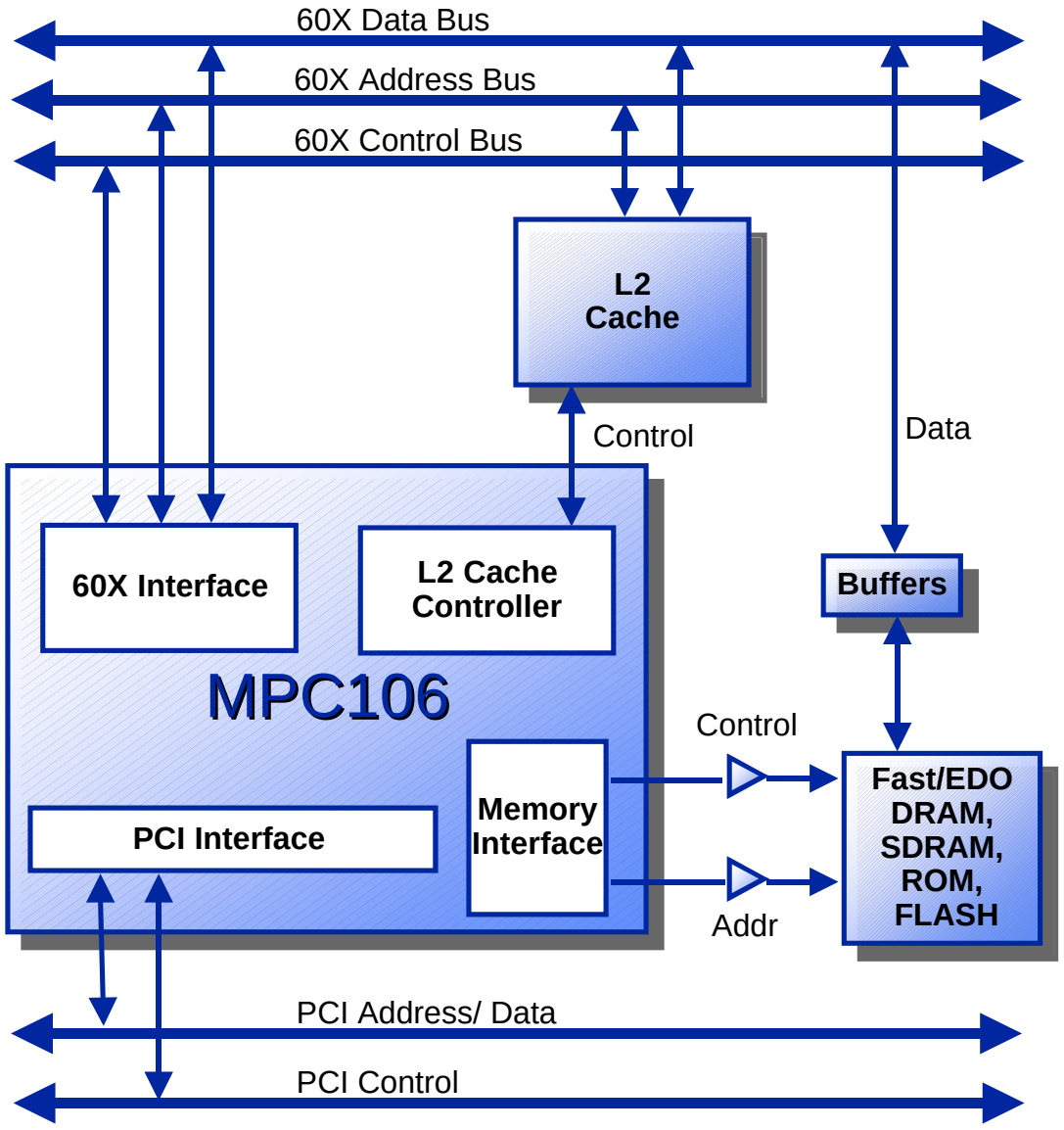
	EC603e		603e		8240	740		750		7400
	100-133 MHz	**200-300 MHz**	100-133 MHz	**200-300 MHz**	**200-266 MHz**	**200-266 MHz**	300-333 MHz	**200-266 MHz**	300-400 MHz	350-500 MHz
CPU Speed - Internal	100 MHz 133 MHz	200 MHz* 266 MHz 300 MHz	100 MHz 133 MHz	200 MHz* 266 MHz 300 MHz	200 MHz* 250 MHz	200 MHz 233 MHz 266 MHz	300 MHz 333 MHz	200 MHz 233 MHz 266 MHz	300 MHz 333 MHz 366 MHz 400 MHz	350 MHz 400 MHz 450 MHz 500 MHz
CPU Bus Dividers	x1.5, x2, x2.5, x3, x3.5, x4	x2, x2.5, x3, x3.5, x4, x4.5, x5, x5.5, x6	x1.5, x2, x2.5, x3, x3.5, x4	x2, x2.5, x3, x3.5, x4, x4.5, x5, x5.5, x6	x2, x2.5, x3, x3.5, x4, x4.5, x5, x5.5, x6	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8, x9
Bus Interface	64- & 32-bit modes	64- & 32-bit modes	64- & 32-bit modes	64- & 32-bit modes	64-bit memory bus 32-bit PCI bus	64 bits	64 bits	64 bits	64 bits	64 bits
Instructions per Clock	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)	3 (2+branch)
L1 Cache	16 Kbyte inst 16 Kbyte data	16 Kbyte inst 16 Kbyte data	16 Kbyte inst 16 Kbyte data	16 Kbyte inst 16 Kbyte data	16 Kbyte inst 16 Kbyte data	32 Kbyte inst 32 Kbyte data	32 Kbyte inst 32 Kbyte data	32 Kbyte inst 32 Kbyte data	32 Kbyte inst 32 Kbyte data	32 Kbyte inst 32 Kbyte data
Backside L2 Cache Support								256, 512 Kbyte 1 Mbyte	256, 512 Kbyte 1 Mbyte	512 Kbyte 1 or 2 Mbyte
Core-to-L2 Frequency Divisions								1:1, 1.5:1, 2:1, 2.5:1, 3:1	1:1, 1.5:1, 2:1, 2.5:1, 3:1	1:1, 1.5:1, 2:1, 2.5:1, 3:1 , 3.5:1, 4:1
Typical/Maximum Power Dissipation	4.2W/5.3W @ 133 MHz	4.0W/6.0W @ 300 MHz	4.2W/5.3W @ 133 MHz	4.0W/6.0W @ 300 MHz	3.0W @ 200 MHz	5.7W/7.9W @ 266 MHz	4.2W/6.0W @ 333 MHz	5.7W/7.9W @ 266 MHz	5.8W/8.0W @ 400 MHz	5.0W/11.5W @ 400 MHz
Die Size	—	—	98 sq mm	42 sq mm	78 sq mm	67 sq mm	67 sq mm	67 sq mm	67 sq mm	83 sqmm
Package	240 CQFP 255 CBGA	255 CBGA	240 CQFP 255 CBGA	255 CBGA †	352 TBGA	255 CBGA	255 CBGA	360 CBGA	360 CBGA	360 CBGA
Process	0.5µ 4LM	0.29µ 5LM	0.5µ 4LM	0.29µ 5LM	0.29µ 5LM	0.29µ 5LM	0.25µ 5LM	0.29µ 5LM	0.25µ 5LM	0.18µ 5LM
Voltage	3.3V	3.3V i/o 2.5V int	3.3V	3.3V i/o 2.5V int	3.3V i/o 2.5V int	3.3V i/o 2.6V int	3.3V i/o 1.9V int	3.3V i/o 2.6V int	3.3V i/o 1.9V int	1.8/2.5/3.3V i/o 1.8V int
SPECint95 (est.)	3.9 @ 133 MHz	7.4 @ 300 MHz	3.9 @ 133 MHz	7.4 @ 300 MHz	6.6 @ 266 MHz	11.5 @ 266 MHz	14.4 @ 333 MHz	12.0 @ 266 MHz	18.8 @ 400 MHz	21.4 @ 450 MHz
SPECfp95 (est.)	—	—	3.1 @ 133 MHz	6.1 @ 300 MHz	5.5 @ 266 MHz	6.9 @ 266 MHz	8.7 @ 333 MHz	7.4 @ 266 MHz	12.2 @ 400 MHz	20.4 @ 450 MHz
Other Performance	188 MIPS @ 133 MHz	423 MIPS @ 300 MHz	188 MIPS @ 133 MHz	423 MIPS @ 300 MHz	375 MIPS @ 266 MHz	488 MIPS @ 266 MHz	610 MIPS @ 333 MHz	488 MIPS @ 266 MHz	733 MIPS @ 400 MHz	825 MIPS @ 450 MHz
Samples	NOW	NOW	NOW	NOW	NOW	NOW	NOW	NOW	NOW	NOW
Production	NOW	NOW	NOW	NOW	NOW	NOW	NOW	NOW	NOW	NOW (500-4Q99)
Execution Units	Integer Branch Load/Store System	Integer Branch Load/Store System	Integer Float Branch Load/Store System	Integer Float Branch Load/Store System	Integer Float Branch Load/Store PCI, DMA, Memory Control	Integer (2) Float Branch Load/Store System	Integer (2) Float Branch Load/Store System	Integer (2) Float Branch Load/Store System	Integer (2) Float Branch Load/Store System	Integer (2) Float Vector Branch Load/Store System
*** See Hardware Specification for operation down to 80 MHz**			Also available in industrial temp	Also available in industrial temp	**† PBGA planned**	Also available in industrial temp		Also available in industrial temp		

MOTOROLA
Semiconductor Products Sector

Digital DNA from Motorola

MPC106 Overview

- **Features**
  - Integrated 32-bit PCI:
    - 16.67MHz - 33MHz PCI 2.1 interface
    - Big and Little-endian support
    - Full PCI support: lock, memory coherent, sleep mode
    - No glue logic necessary
  - Integrated memory control:
    - DRAM (fast page mode or EDO, 64-bit, parity), up to 1GB
    - SDRAM support
    - ROM/Flash ROM (up to 16MB)
    - ECC on DRAM and 13th address bit
  - Integrated power management:
    - Nap, doze, sleep and suspend modes
  - JTAG Boundary Scan Support
- **Performance Features**
  - Works with L2 cache or second processor
  - Write buffering to and from PCI
- **Technology**
  - 0.5µm QLM CMOS, 3.3V (TTL comp I/O)
  - 304-pin CBGA
- **Schedule**
  - 66 MHz and 83 MHz available now
  - Also available in industrial temp
  - **Not recommended for new designs**



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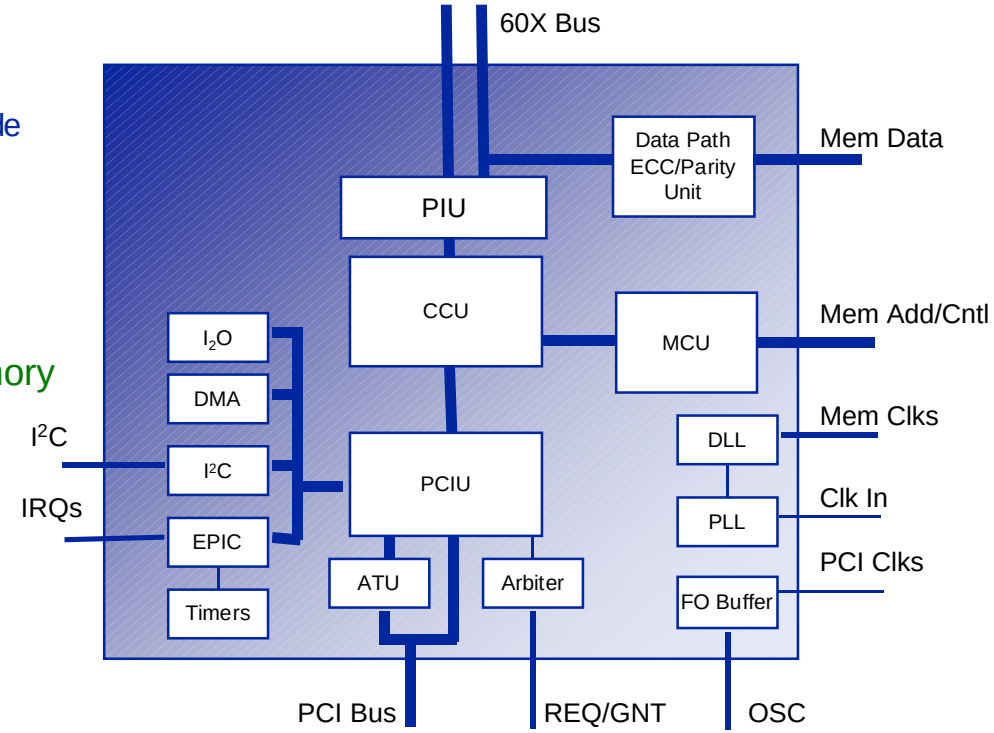
Digital DNA from Motorola

MPC107 Overview

➤ Features

- 60x processor bus supports 66, 83, 100 MHz
- Integrated memory control (20-100 MHz):
  - » Up to 1GB of DRAM (FPM, EDO), SDRAM, 32- or 64-bit
  - » Separate memory data bus w/buffers for parity or ECC
  - » ROM/Flash ROM (up to 144MB)
- Integrated 32-bit PCI:
  - » 33 & 66 MHz PCI 2.1 interface, 5V tolerant
  - » Full PCI support: lock, memory coherent, sleep mode
  - » Master and Agent mode support
  - » Support for multiple 107 devices on PCI bus
  - » PCI Arbiter (5 req/gnt pairs)
- Support for 2-way SMP and Local Bus Slave
- EPIC Interrupt Controller
- Clock generation and buffering for PCI and memory
- I^2C (Master and Slave modes)
- Message Unit (I_2O support)
- Two-channel DMA (direct and chaining modes)
- Integrated power management:
  - » Nap, doze, sleep and suspend modes
- JTAG Boundary Scan Support



➤ Technology

- 0.35µm CMOS (HiP3.0), 2.5V core, 2.5/3.3V I/O
- Package: 503 CBGA (32.5 x 32.5 mm)

➤ Schedule

- Samples available now, Production 4Q99
- PBGA (33 x 33 mm) 1H00

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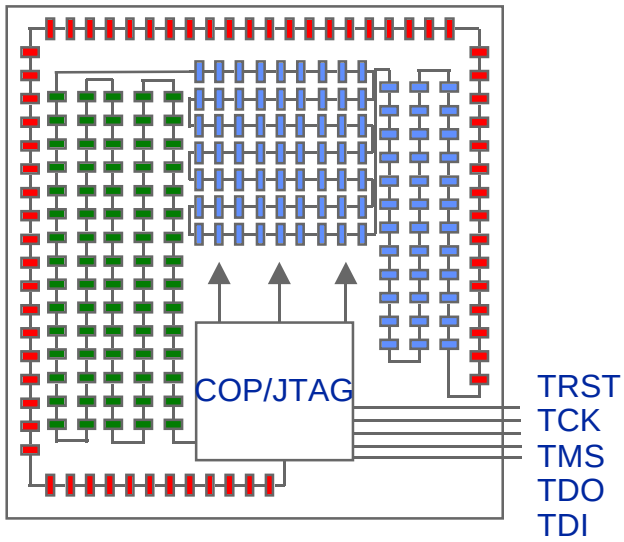
Extended Temp PowerPC CPUs

- Networking customers are moving more intelligence to the periphery of networks, requiring extended temp CPUs for outdoor applications
- Motorola selling industrial temp range (-40° -> +105°C Tj) in standard packaging and enabling two partners to help provide these devices
- Chip Supply and Thomson-CSF are Motorola's partners
  - Each can buy standard parts and die to upscreen for industrial temp range and Military requirements, and provide standard or special packaging
  - Each will be selling devices through their own channels
  - Agreements include Motorola's right to sell industrial temp devices to our customers through our channels (including our distributors)
  - Motorola reserves rights to internally test and supply ext temp devices
  - Includes 603E @ 100 and 133, 603R @ 200 and 266 MHz, and 106 @ 66 MHz
  - Offerings expanded in May 1999 to include MPC750 and MPC740 rev 3.1 @ 200 and 266 MHz and 106 @ 83 MHz

COP Interface

- COP stands for Common On-chip Processor
- The commands used by the COP are loaded using the JTAG protocol
- The COP enables access to internal nodes of the chip through latches located on a single scan chain
- The scan chain's length differs for each member of each family
- Complete visibility to every internal signal
  - Many nodes of interest, e.g. GPRs, FPRs, caches, etc. are not on the scan chain, but can be read indirectly through the scan chain
- COP implemented as an extension to the JTAG interface
- App note available on including header for COP interface in designs



Leading PowerPC™ 60x/7xx 3rd Parties

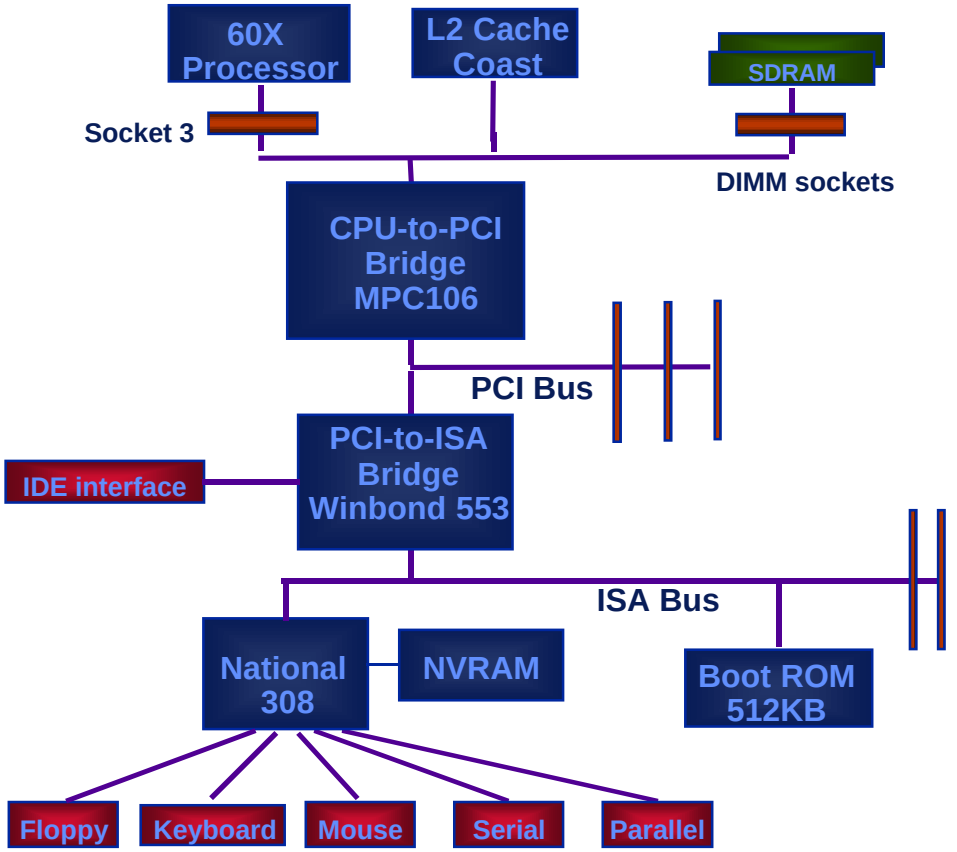
	Compiler	Debugger	Emulator	OS
➤ Accelerated Technology				X
➤ Applied Microsystems		X	X	
➤ Cygnus Solutions	X	X		
➤ Diab-SDS	X	X		
➤ Enea		X		X
➤ EST		X	X	
➤ Green Hills Software	X	X		
➤ Hewlett-Packard			X	
➤ Integrated Systems, Inc.		X		X
➤ Lynx Real-TIme Systems	X	X		X
➤ Mentor Graphics Microtec Div	X	X		X
➤ MetaWare	X	X		
➤ Metrowerks	X	X		
➤ Microware	X	X		X
➤ Precise Software				X
➤ QNX Software Systems	X	X		X
➤ Sun Microsystems (Chorus)				X
➤ Tektronix			LA	
➤ Wind River Systems	X	X		X

PowerPC 60x/7xx Evaluation Boards

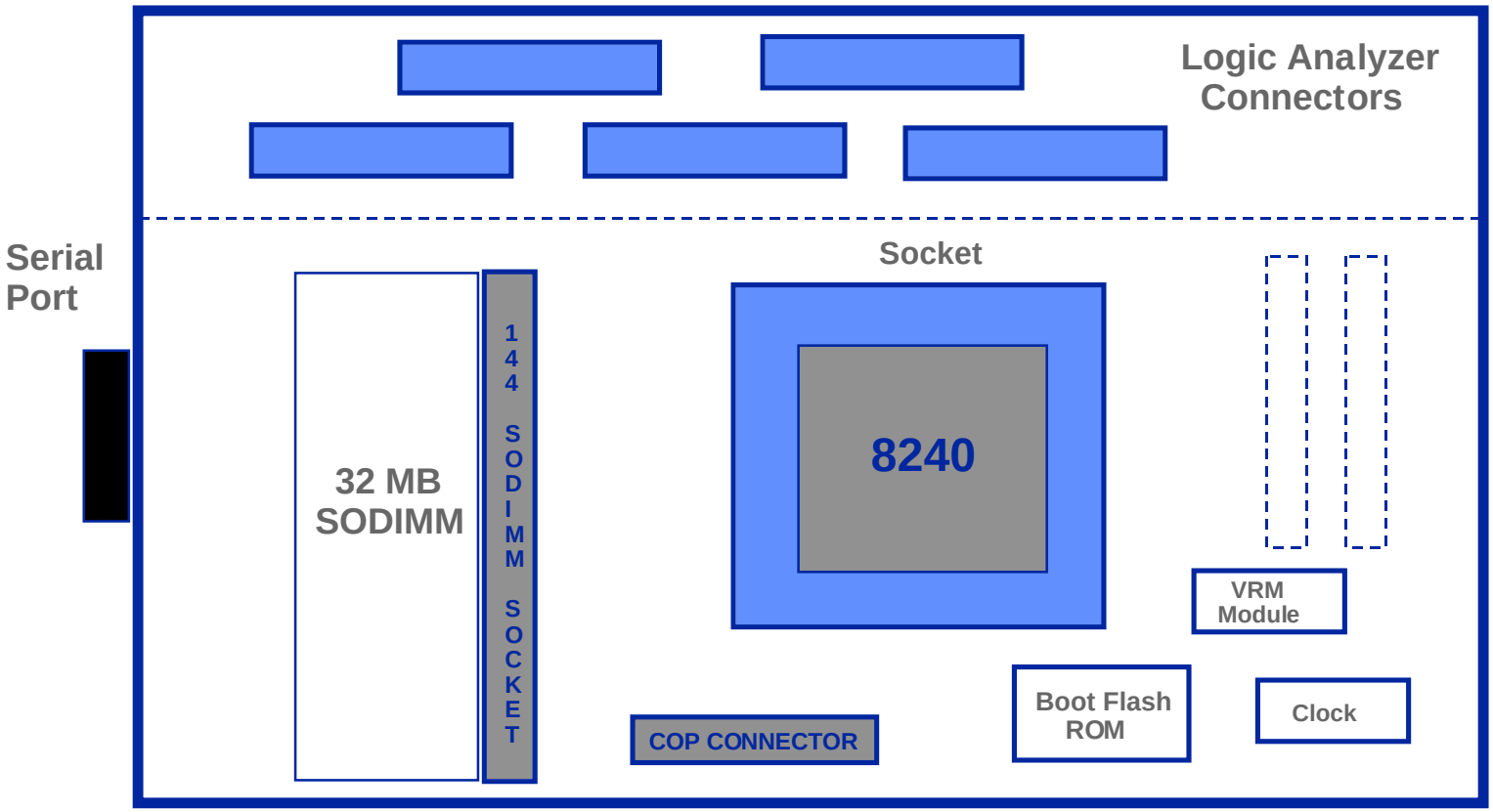
- **Sandpoint Embedded Development Platform**
  - Intended for RTOS-based system development and evaluation
    - » Enea OSE,ISI pSOS, Wind River VxWorks ported
  - CPUs interchangeable via PCI Mezzanine cards
  - Expandable with Serial/Parallel, IDE, SVGA I/O; PCI & ISA; COP connector
  - DINK-32 boot ROM; full source and board schematics available on web
  - List price $2415 includes ATX-factor case with power supply
- **Excimer X3 Evaluation Board**
  - Intended for architectural evaluation and education
    - » Bundling evaluation compiler/debugger CDROMs, Macraigor COP Wiggler
  - Implementation of minimal 603e system design application note AN1769/D
  - Serial I/O and COP connector; no expandability
  - DINK-32 boot ROM; full source and board schematics available on web
  - List price $495 includes cables and power supply

Yellowknife X4 Development Platform

- CPU
  - Supports 60x and 7xx CPUs
  - VRM for auto voltage selection
  - CPU on interposer (PGA Socket 3)
  - 66, 75, 83 MHz CPU bus
- Single chip MPC 106 PCI bridge and L2 memory controller
- Memory
  - 512KB L2 on motherboard
  - 2 slots SDRAM DIMMs (16MB std config)
- Peripherals configurable
  - 3 PCI slots, 2 ISA slots
- PCI 2.1 Compliant (33 MHz)
- ATX Form factor, 6 layer PCB
- DINK-32 debugger source code included
- Initialization routines for key chips
  - Source code included
- Order part number PPCEVAL-YK-EX4



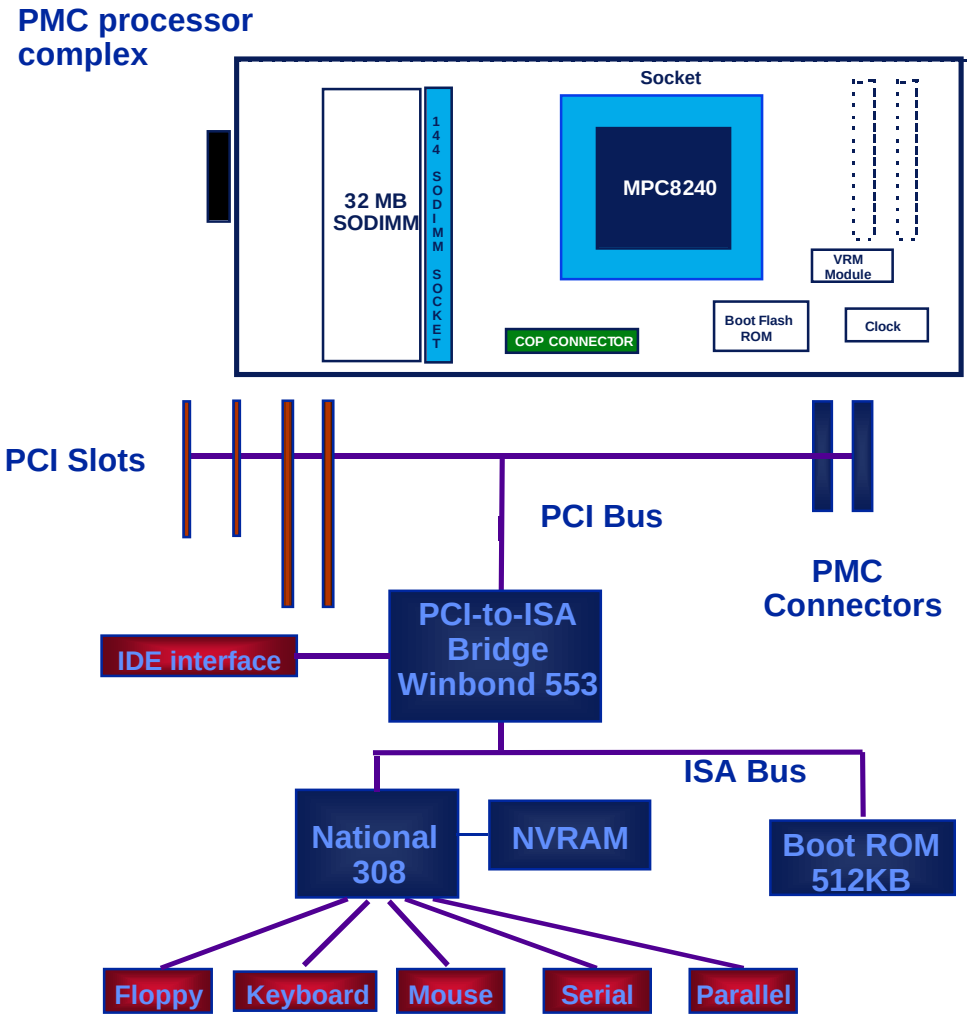
Example of MPC8240 Card with Debug



- Includes: PMC connectors, MPC8240, 32 MB SDRAM SODIMM, clock circuitry, VRM, COP connector
- Schematics available - contact Local Sales Office or Distributor

Sandpoint Development Platform

- Processor complex
  - PMC connector either 32-bit or 64-bit
  - standard PMC connectors
- Peripherals configurable
  - 4 PCI slots
    - Two 32-bit 5 volt slots
    - Two 64-bit 3.3 volt slots
- PCI 2.1 Compliant (33 MHz)
- 2 serial com ports
- IDE connector 33 Mhz ATAPI
- ATX Form factor
- Debugger source code included
- Initialization routines for key chips
  - Source code included
- Sandpoint shipped with chassis and power supply
- Available now with MPC8240 PMC
  - PPCEVAL-SP2-8240
  - PPCEVAL-SP2-7400
  - PPCEVAL-SP2-750
- MPC7400 and MPC750 PMCs also include MPC107 chipset



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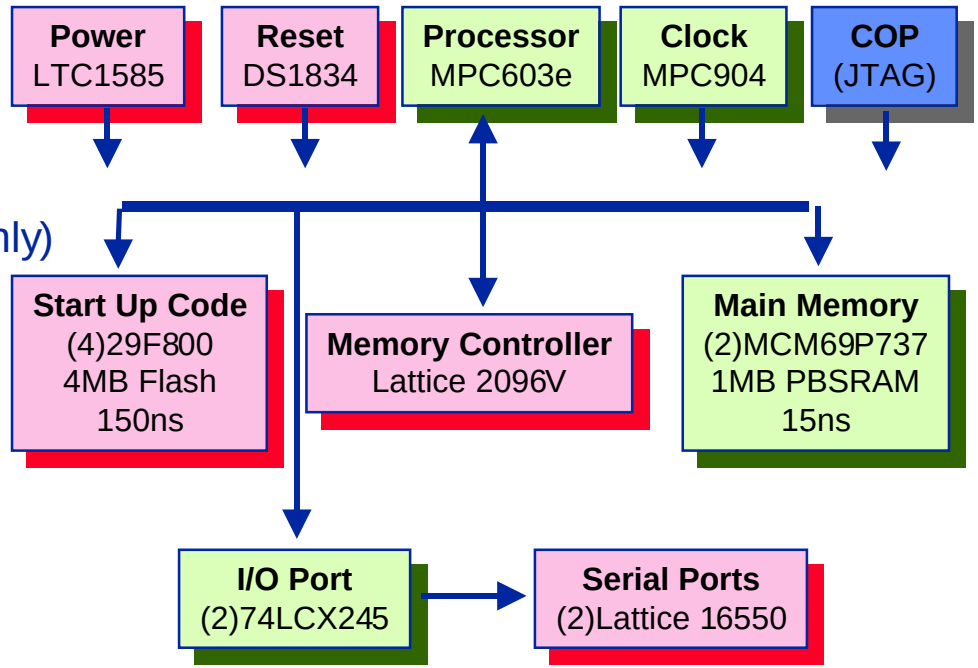
Excimer X3 Embedded Evaluation Board

Familiarization or educational board
(not intended for application or RTOS development)

- **CPU**
  - MPC603e @266+MHz (may vary)
  - 66 MHz memory bus
- **FPGA memory controller**
- **Memory**
  - 1MB Pipeline Burst SRAM (3/1/1/1)
  - 4MB Flash ROM (9 clks; single beat only)
  - No other expansion
- **Peripherals**
  - 2 RS232 serial ports
  - 8-bit data bus and chip selects on pins
- **Complete demonstration kit for $495!**
  - 4.75” x 5.75” Evaluation board
  - 5 volt power supply
  - ROM monitor (DINK-32) in Flash & serial cable
  - JTAG i/f board (Wiggler™) & parallel cable
  - Compiler and debugger evaluation CDROMs
  - Order PPCEVAL-XMER3



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PowerPC Application Notes

- **Available at http://www.mot.com/SPS/PowerPC/teksupport/teklibrary/**
- **"Designing G4 Systems"**
  - Describes G4 bus arbitration and pinout differences from G3 processors
  - Order by **AN1795/D**
- **"PowerPC Backside L2 Timing Analysis"**
  - Provides information on designing fast L2 cache interface
  - Order by **AN1794/D**
- **"Performance Differences between the MPC8240 and the MPC106"**
  - Details performance issues and benefits of the MPC8240
- **"PowerPC Microprocessor Clock Modes"**
  - Describes PowerPC µP Clocking Operation, device numbering methodology, test methodology/issues and timing considerations
  - Order by **AN1269/D**
- **"PowerPC 603 Hardware Interrupt Latency in Embedded Applications"**
  - Describes service of external interrupts in 603 system in light of performance features such as Branch Folding, Superscalar Pipelining, and Multiple Instruction Completion
  - Order by **AN1267/D**
- **"Multiprocessor Systems and the PowerPC 603e™ Microprocessor"**
  - Describes hardware and software issues associated with MPC603 and MPC603e multiprocessor systems
  - Order by **AN1294/D**
- **"Designing PCI 2.1-Compliant MPC106 Systems"**
  - Describes how to design with the MPC106 for a PCI 2.1 compliant system
- **"SDRAM System Design using the MPC106"**
  - Describes system design with the MPC106 and SDRAM.

PowerPC 6xx Literature

- PowerPC Microprocessor Family: The Programming Environments
  - Complete Architectural reference for the entire 6xx family
  - Instruction Reference, Memory Management, Cache Models, Multiprocessor Support
  - Order by *MPCFPE/AD*
- PowerPC Microprocessor Family: The Programmer's Reference Guide
  - Pocket-sized quick reference for common 6xx information, instruction set fields, exception vectors
  - Order by *MPCPRG/D*
- The PowerPC Architecture: A Specification For A New Family Of RISC Processors
  - Also referred to as "Books I, II and III" of the PowerPC Architecture specification
  - Formal specification maintained by the PowerPC Architectural Review Board
  - Currently reflects architectural revision level 1.05
  - Order by *TB335/D*
- AltiVec™ Technology Programming Environments Manual and Programming Interface Manual
  - Relates AltiVec technology to both the 64- and the 32-bit portions of the PowerPC architecture.

PowerPC 6xx Literature

- Available at http://www.mot.com/SPS/PowerPC/teksupport/teklibrary/
- AltiVec™ Technology Fact Sheet and White Paper
  - Summarizes the AltiVec Technology and its features
  - Order by ALTIVECFACT/D and ALTIVECWP/D
- PowerPC 6xx or 7xx Fact Sheet
  - One page overview of a specific 6xx or 7xx processor
- PowerPC 6xx or 7xx RISC Microprocessor Technical Summary
  - Technical overview of a specific 6xx or 7xx microprocessor
- PowerPC 6xx or 7xx RISC Microprocessor User's Manual
  - Covers *implementation-specific* details for each 6xx or 7xx processor
  - Supplemented by "The Programming Environments" for instruction set details
- PowerPC 6xx or 7xx RISC Microprocessor Hardware Specifications
  - Contains overview, pinout, electrical and thermal specifications and general packaging information for a specific 6xx or 7xx microprocessor
- BGA Package Design Manual
  - Covers C4, CBGA and PBGA packaging
  - Good overview for users regarding BGA use
  - Order by *C4PKGUSERGUIDE/D*
  - Several white papers on BGA assembly and thermal issues also available

PowerPC Support and Resources

- Motorola PowerPC WWW Site
  - **http://www.mot.com/PowerPC**
  - Hardware and Software Support Information
  - All Publicly-Released Technical Documents
    - » Hardware Specifications, Application Notes, Reference Manuals
  - Reference platform information
  - BSDL Files & IBIS Models
  - Current Press Releases
  - Web links to PowerPC hardware and software vendors

Let us know what you would like to see on the site by mailing webmaster@risc.sps.mot.com

Summary

PowerPC™

- PowerPC is a ***scaleable*** architecture that enables broad product range
  - From low-cost embedded solutions to high-end computing solutions
  - Continue to expand the architecture with AltiVec technology
- Leadership semiconductor processes, quality and manufacturing
- Product line longevity and commitment
- Networking and embedded applications driving performance envelope
- PowerPC has the strongest RISC microprocessor portfolio in the world
  - High performance PowerPC CPUs with competitive prices
  - Broadest range of footprint compatible CPUs
  - Broadest range of integrated processors
  - Broadest tools support