

Networking Systems Division (NSD)

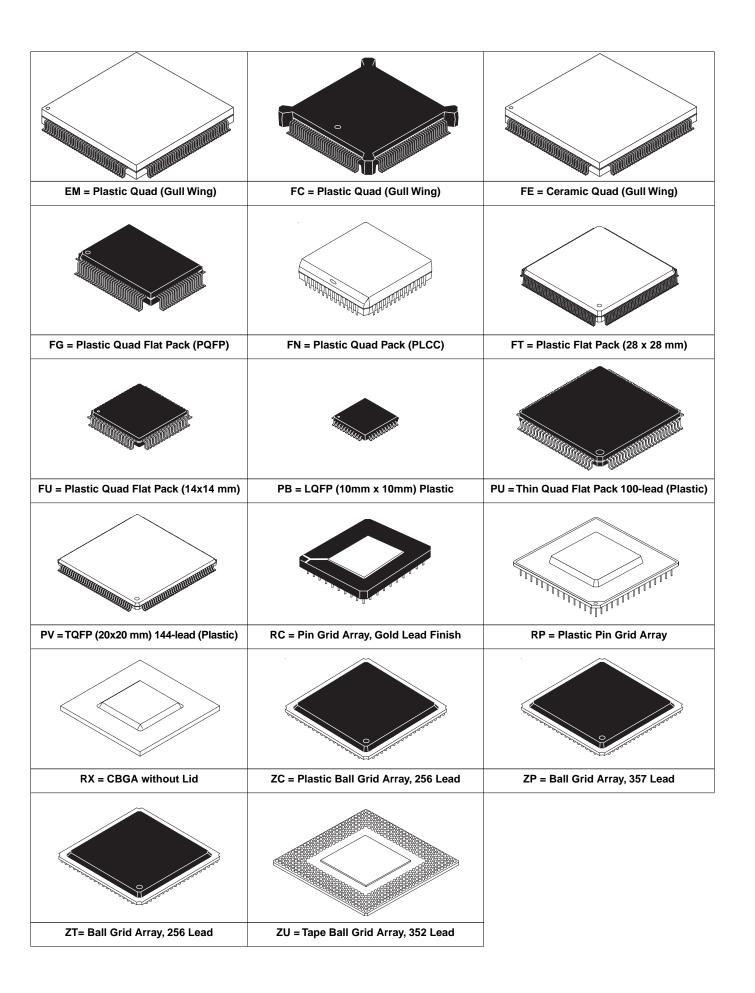
Personal Computing Systems Division (PCSD)

Product Information

3rd QUARTER 1999

PowerPC™ Microprocessors
Integrated PowerPC Microprocessors
Networking & Communications 68K Processors
68K/ColdFire® Microprocessors
Integrated 68K/ColdFire Microprocessors
Timing Solutions
Networking Systems Memory





100, 600, and 700 Series PowerPC Processors & Chipsets Standard temp: 0° to +105°CTj (junction temperature)

| Device No. | Package | Speeds | Apps Modr | Rev | Process | Voltage Core | Voltage IO/tol. | SOQ | MPQ | POQ | Description |
|--|---|---|----------------------------|---|---|--|--|--|--|--|--|
| 105 XPC105A | 304-Lead RX | 66 | С | D=2.4 | HiP1.0 | 3.3±5% | 3.3/5.0 | 1 | 1 | 55 | 60x to PCI bridge, L2 cache controller, memory controller with support for DRAM, SDRAM, ROM, and flash ROM. Not recommended for new designs. |
| 106 MPC106A MPC106A MPC106A | 304-Lead RX 304-Lead RX 304-Lead RX | 66 83 66, 83 | C D T | G=4.0 G=4.0 G=4.0 | HiP 1.4 HiP 1.4 HiP 1.4 | 3.3±5% 3.3±5% 3.3±5% | 3.3/5.0 3.3/5.0 3.3/5.0 | 1 1 0 | 1 1 4 | 55 55 55 | 60x to PCI bridge, multiple-processor support, L2 cache controller, memory controller with support for EDO/FPM, DRAM, SDRAM, ROM, and flash ROM. |
| EC603e KMPE603E MPE603E MPE603E KXPE603P XPE603P MPE603R | 240-Lead FE 240-Lead FE 255-Lead RX 240-Lead FE 240-Lead FE 255-Lead RX | 100, 133 100, 133 100, 133 100, 133 166, 200 166, 200 200, 266, 300 | | N=4.1 N=4.1 N=4.1 E=2.1.1 E=2.1.1 C=2.1 | HiP 1.3 HiP 1.3 HiP 1.3 HiP 2.0 HiP 2.0 HiP 3.0 | 3.3±5% 3.3±5% 3.3±5% 2.5±5% 2.5±5% 2.5±5% | 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 | 2 0 1 2 0 | 2 24 1 2 24 1 | 2 24 60 2 24 60 | 32-bit PowerPC superscalar MPU (3 instructions per cycle) with dual 16k instruction and data caches, 32-and 64-bit external data bus, 2.5- or 3.3-volt core and 3.3-volt I/O. |
| KMPC603E MPC603E MPC603E MPC603E MPC603E MPC603E KXPC603P XPC603P MPC603R MPC603R | 240-Lead FE 240-Lead FE 240-Lead FE 255-Lead RX 255-Lead RX 240-Lead FE 240-Lead FE 240-Lead RX 255-Lead RX | 100, 133 100, 133 100, 133 100, 133 100, 133 100, 133 166, 200 166, 200 200, 266, 300 200, 266 | | N=4.1 N=4.1 N=4.1 N=4.1 N=4.1 E=2.1.1 E=2.1.1 C=2.1 C=2.1 | HiP 1.3 HiP 1.3 HiP 1.3 HiP 1.3 HiP 1.3 HiP 2.0 HiP 2.0 HiP 2.0 HiP 3.0 | 3.3±5% 3.3±5% 3.3±5% 3.3±5% 3.3±5% 2.5±5% 2.5±5% 2.5±5% 2.5±5% | 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 3.3/5.0 | 2 0 0 1 0 2 0 0 1 1 | 2 24 64 1 60 2 24 24 1 | 2 24 24 60 60 2 24 24 60 60 | 32-bit PowerPC superscalar MPU (3 instructions per cycle) with dual 16k instruction and data caches, single/double precision IEEE FPU, 32- and 64-bit external data bus, 2.5- or 3.3-volt core and 3.3-volt I/O. |
| 740/750 XPC740A XPC750A MPC740A MPC740A MPC750A XPC740P XPC750P XPC750P XPC750P | 255-Lead RX 360-Lead RX 255-Lead RX 360-Lead RX 360-Lead RX 360-Lead RX 360-Lead RX | 200, 233, 266 200, 233, 266 200, 266 200, 266 300, 333 300, 333 400 366 | L T T L L P | E=2.2 E=2.2 H=3.1 H=3.1 E=1.2 E=1.2 E=1.2 E=1.2 | HiP 3.0 HiP 3.0 HiP 3.0 HiP 3.5 HiP 3.5 HiP 3.5 HiP 3.5 | 2.6±0.1 2.6±0.1 2.6±0.1 2.6±0.1 1.9±0.1 1.9±0.1 2.05±0.05 2.05±0.05 | 3.3 3.3 3.3 3.3 3.3 3.3 3.3 3.3 | 1 1 0 0 1 1 1 | 1 1 60 44 1 1 1 | 60 44 60 44 60 44 44 44 | 32-bit PowerPC superscalar MPU (3 instructions per cycle) with dual 32k instruction and data caches, single/double precision IEEE FPU, and 64-bit external data bus. The 750 also has external 12 cache interface (up to 1 meg) with integrated controller and cache tags. |

MPC801, 850 and 860 Integrated PowerPC Communications Processors standard temp: 0° to +95°CTJ (junction temperature)

| Device No. | Package | Speeds | Rev | Device Name | Temp* (-40 to +95 Tj) | SOQ | MPQ | POQ | BRICK | Description |
|---|--|--|---|---------------------------------------|--|--|--|--|------------|--|
| XPC801 XPC850 XPC850DC XPC850DE XPC850DH XPC850SE XPC850SR | ZT ZT ZT ZT ZT ZT ZT ZT ZT | 25, 40 33, 50 33, 50, 66 33, 50, 66 33, 50, 66 33, 50, 66 33, 50, 66 | A A A A | Low-Cost Integrated PowerPC MPU | CZT CZT 50 CZT 50 CZT 50 CZT 50 CZT 50 | 0 0 0 0 0 | 60 60 60 60 60 60 | 300 300 300 300 300 300 300 300 | | Low cost general purpose Embedded PowerPC MPU. The MPC801 is not recommended for new designs. |
| | | | | | | For sar KXPC8 | | r - KXPC | 801, KXPC8 | 350, KXPC850DC, KXPC850DE, KXPC850DH, KXPC850SE, |
| XPC860 XPC860DC XPC860DE XPC860DH XPC860EN XPC860MH XPC860SR XPC860T XPC860DT | ZP | 33, 50, 66 33, 50, 66 | C.1 C.1 C.1 C.1 C.1 C.1 C.1 B.3/B.5 B.3/B.5 | PowerQUICC™ PowerPC MPU | CZP 33, 50 CZP 33, 50 | 0 0 0 0 0 0 0 | 44 44 44 44 44 44 44 | 220 220 220 220 220 220 220 220 220 220 | | PowerQUICC family with embedded PowerPC superscalar MPU with dual 4k I-cache and D-cache with MMUs integrated with CPM (Communication Processing Module) of earlier generation 68360 QUICC™ plus DSP capability. Rev. Col. PCN issued 22 June 1998. |
| | | | | | | For sample order—KXPC860, KXPC860EN, KXPC860DC, KXPC860DE, KXPC860DH, KXPC860MH, KXPC86SR, KXPC860T. | | | | |

EN = Ethernet; DC = Dual Channel; DE = Dual Ethernet; DH = two channel w/HDLC; DT = two SCCs w/10/100; MH = Four Channel w/HDLC; SE = Single Ethernet; SR = Four Channel w/Ethernet, multi-HDLC, ATM; T = 10/100 Four Channel w/HDLC.

MPC850/MPC860 Processor Derivatives

| Device | 850 | 850DC | 850DE | 850DH | 850SE | 850SR | 860 | 860DC | 860DE | 860DH | 860EN | 860MH | 860SR | 860T | 860DT |
|---|-----|-------|-------|-------|-------|-------|-----|-------|-------|-------|-------|-------|-------|--------|--------|
| Serial Communciations Controllers (SCCs) | 1 | 2 | 2 | 2 | 1 | 2 | 4 | 2 | 2 | 2 | 4 | 4 | 4 | 4 | 2 |
| Ethernet | Yes | SCC1 | Yes | Yes | Yes | Yes | _ | SCC1 | Yes | Yes | Yes | Yes | Yes | 10/100 | 10/100 |
| ATM | _ | _ | _ | _ | _ | Yes | _ | _ | _ | _ | _ | _ | Yes | _ | _ |
| USB | Yes | Yes | Yes | Yes | _ | Yes | _ | _ | _ | _ | _ | _ | _ | _ | _ |
| MHDLC | _ | _ | _ | Yes | _ | Yes | _ | _ | _ | Yes | _ | Yes | Yes | Yes | Yes |
| PCMCIA | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |

MPC821 and 823 Integrated PowerPC Microprocessors for Portable Systems

| Device No. | Package | Speeds | Rev | Device Name | Temp | SOQ | MPQ | POQ | Description | | | |
|------------|----------|--------------------------|----------|------------------------|----------------------------------|--------------------------|--|------------|-----------------------------------|--|--|--|
| XPC821 | ZP ZP | 25 50, 66 | B3 B3 | Portable System MPU | CZP 25 | 0 | 0 44 220 PowerPC MPU for personal systems. | | | | | |
| | | | | | | For sar | For sample order - SPAK821 | | | | | |
| XPC823 | ZT ZC | 66, 75, 81 66, 75, 81 | A A | Portable System MPU | CZT 66, 75, 81 CZT 66, 75, 81 | 2 2 | 60 84 | 300 420 | PowerPC MPU for mobile computing. | | | |
| | | | | | | For sample order—SPAK823 | | | | | | |

MPC8240 Integrated PowerPC Processors Standard temp: 0° to +105°C Tj (junction temperature)

| Device No. | Package | Speeds | Apps Modr | Rev | Process | Voltage Core | Voltage IO/tol. | SOQ | MPQ | POQ | Description |
|--|---|----------------------------------|--------------|-------------------------------|-------------------------------|----------------------------------|-------------------------------|-------------|---------------|---------------|---|
| 8240 XPC8240 XPC8240 KXPC8240 | 352-Lead ZU 352-Lead ZU 352-Lead ZU | 200, 266 200, 266 200, 266 | P L L | C=1.1.1 C=1.1.1 C=1.1.1 | HiP 3.0 HiP 3.0 HiP 3.0 | 2.5 ± 5% 2.5 ± 5% 2.5 ± 5% | 3.3/5.0 3.3/5.0 3.3/5.0 | 0 0 2 | 24 24 2 | 24 24 2 | 32-bit superscalar PowerPC processor core with integrated peripheral logic. Supports up to 100 MHz 64-bit memory interface and 32-bit PCI interface up to 66 MHz. |
| KXPC = Sample | XPC = Sample | | | ds: L = 105 | °C Tj; P=70° | СТј | | | | | |

68K Integrated Communications Processors

| Device No. | Package | Speeds | Rev | Device Name | Temp* (-40 to +85°C) | SOQ | MPQ | POQ | Brick | Description |
|-------------------------------------|--|---|--------------------------------------|--|--|--------------------------------------|--|--|-------------------|--|
| MC68302 MC68302V | 132-Lead RC 132-Lead FC 144-Lead PV 144-Lead PV | 16, 20, 25 16, 20, 25 16, 20, 25, 33 16 @ 3.3V | C C C | Integrated Multiprotocol Processor (IMP) | CRC16, 20 CFC16, 20 CPV16 CPV16V | 0 0 0 0 | 14 36 60 60 | 14 144 300 300 | 180 300 300 | 68000 core with three high-performance multiprotocol serial channels also on-chip DMA, RAM, timers, I/O, chip select, and wait state interrupt controller. |
| | | | | | | For FC | PV samp | le order- | -SPAK30 | D2FCXXC, SPAK302PVXXC |
| XC68EN302 | 144-Lead PV | 20, 25 | В | Integrated Multiprotocol Processor with | CPV20 | 0 | 60 | 300 | 300 | Full 68302, plus separate IEEC 802.3 ethernet MAC channel and full DRAM controller |
| | | | | Ethernet Controller | | For PV | sample o | rder—SF | AKEN30 |)2PVXXB |
| XC68LC302 XC68LC302V | 100-Lead PU | 16, 20, 25 @ 5V 16, 20 @ 3.3V | B B | Low-Cost Integrated Multiprotocol Processor | CPU16, 20 CPU16V | 0 | 84 | multiprotocol serial channels; al | | Static EC000 Core Processor with two high-performance multiprotocol serial channels; also on-chip DMA, RAM, timers, I/O, chip selects, and wait state interrupt control- ler. |
| | | | | | | For PU | sample o | rder—SF | PAKLC30 | 2PUXXB |
| MC68QH302 | 144-Lead PV | 16, 20, 25 | С | Quad-HDLC Integrated | | 0 | 60 | 300 | 300 | 68302 derivative with support for up to four HDLC transparent channels. Pin compatible with 68302. |
| | | | | Multiprotocol Processor | | | | | 12PVXXC | |
| MC68360V MC68EN360 MC68EN360V | 240-Lead EM 357-Lead ZP 241-Lead RC 240-Lead EM 357-Lead ZP 240-Lead EM 357-Lead ZP 241-Lead RC 240-Lead EM 357-Lead ZP | 25,33 @ 5.0V 25 @ 3.3V 25, 33 @ 5.0V 25 @ 3.3V | K K L L K K L L | OUICCTM QUad Integrated Communications Controller | CEM25 CZP25 CRC25 CEM25 CZP25 CRC25 | 0 0 0 0 0 0 0 0 | 24 44 10 24 44 24 44 10 24 44 | 120 220 10 120 220 120 220 10 120 220 | | CPU32 + core with System Integration Module (SIM) and four high-performance SCCs support numerous protocols. Two SCCs support Ethernet on "EN" version. |
| | | | | | | SPAKE | | 25VL Fo | or ZP san | |
| MC68MH360V | 240-Lead EM 357-Lead ZP 241-Lead RC 240-Lead EM 357-Lead ZP | 25,33@5.0V 25@3.3V | K K K L | Multichannel HDLC Controller | CEM25 CZP25 CRC25 | 0 0 0 0 | 24 44 10 24 44 | 120 220 10 120 220 | | One-chip integrated microprocessor and peripheral combination with four SCCs, two serial management controllers (SMCs) and one serial peripheral interface (SPI). |
| | | | | | | For MI SPAKN | H sample //H360ZP | order—S XXK, SPA | PAKMH: KMH360 | 360EMXXK, SPAKMH360EMXXVL, SPAKMH360RLXXK, DZPXXVL |
| MC68606 | 84-Lead FN | 12,16 | С | | CFN12, 16 | 1 | 1 | 15 | | Implements CCITT Q.920/Q.921 link access procedure (LAPB) specified at ISO level 2 for both signaling and data applications in an ISDN. |
| MC68824 | 84-Lead FN | 10, 12, 16 | Н | Token Bus Controller (TBC) | | 1 | 1 | 15 | | Implements IEEE 802.4 Token Bus Media Access Control which GM MAP specifies in layer 2. Manages access to media, fault recovery, and frame formatting. Runs at speeds down to 10 Kb/s. |

68K Networking & Communications Support Devices

| Device No. | Package | Speeds | Rev | Device Name | Description |
|------------|------------|--------|-----|-----------------------------------|---|
| MC68184 | 40-Lead PL | | | Broadband I/F Controller (BIC) | Macrocell implementation of the digital portion of the IEEE 802.4 Broadband Physical layer. 1, 5, 10 Mb/s serial speed. Contact ASIC Division, Chandler, AZ (602) 821-4597. |
| MC68194 | 52-Lead FJ | | | Carrierband Modem (CBM) | A bipolar implementation of the IEEE 802.4 Carrierband Physical layer. 1, 5, 10 Mb/s serial speed. Contact IC Logic Division, Mesa AZ (602) 962-3005. |

68K Stand-Alone CPUs

| Device No. | Package | Speeds | Rev | Device Name | Temp** (-40 to +85°C) | SOQ | MPQ | POQ | BRICK | Description |
|------------|---|---|-------------|--|--------------------------------------|------------------|-----------------------|------------------------|------------|---|
| MC68EC000 | 68-Lead FN 64-Lead FU | 8, 10, 12, 16, 20 8, 10, 12, 16, 20 | | 8-/16-/32-Bit HCMOS Embedded MPU | | 0 | 18 84 | 1008 252 | 420 | Low-cost embedded control MPU with 8-/16-bit selectable data bus. |
| | | | | | | For FN | FU samp | le order– | -SPAKEC00 | 00FNXX, SPAKEC000FUXX |
| MC68HC000 | 68-Lead FN, 68-Lead RC | 8, 10, 12, 16, 20 8, 10, 12, 16 | | HCMOS 16-/32-Bit MPU | CFN8, 10, 12, 16 CRC8, 10, 12, 16 | 5 0 0 | 5 78 21 | 160 780 210 | | Completely pin and timing MC68000-compatibility with a tenth of the power dissipation. |
| | | | | | | | FN, P, RC 1000RCXX | | rder—SPAI | CHC000FCXX, SPAKHC000FNXX, SPAKHC000PXX, |
| MC68HC001 | 68-Lead FN, 68-Lead RC | 8, 10, 12, 16, 8, 10, 12, 16 | | Staticlly Switchable 8- /16-Bit Data Bus | CFN8, 10 CRC8 | 0 | 18 21 | 1008 210 | | Functionally compatible with MC68000 and MC68008. |
| | | | | | | For FN | RC samp | le order– | -SPAKHC0 | 01FNXX, SPAKHC001RCXX* |
| MC68SEC000 | 64-Lead FU, 68-Lead PB | 10, 16, 20 10, 16, 20 | | 8-/16-/32-Bit Static HCMOS Embedded MPU | CFN8, 10 CRC8 | 0 | 84 1 | 252 1 | | Static version of the MC68EC000. |
| | | | | | | For FU | sample o | rder—SP | AKSEC000F | CUXX |
| MC68020 | 114-Lead RC 132-Lead FE* 114-Lead RP 132-Lead FC | 12*, 16, 20, 25, 33 16, 20, 25, 33 16, 20, 25 16, 20, 25 16, 20, 25, 33 | E E E | 32-Bit MPU | CRC16, 20, 25 CRP16 CFC16, 25 | 1 0 1 0 | 1 36 1 36 | 14 180 13 144 | 180 | Complete 32-bit MPU. 5-Gbyte linear address space. Coprocessor interface. Instruction cache. Dynamic bus sizing. Excellent MPU for graphics control. On-chip cache speeds drawing algorithms. Bit field support for pixel manipulation. |
| | | | | | | For FC, | FE sample | e order— | -SPAK020F(| CXXE, SPAK020FEXXE |
| MC68EC020 | 100-Lead FG 100-Lead RP | 16, 25 16, 25 | | 32-Bit Embedded MPU | CFG16 CRP25 | 0 1 | 66 1 | 264 13 | 330 | 32-bit data bus MPU with 24-bit address bus. Instruction cache. Dynamic bus sizing. Coprocessor interface. Low-cost packaging. |
| | | | | | | For FG | sample o | rder—SP | AKEC020FC | XXX |
| MC68030 | 128-Lead RC | 16,20,25,33,40,50 | С | Enhanced 32-Bit MPU | CRC25,33 | 1 | 1 | 14 | | Complete 32-bit MPU with on-chip instruction and data caches, |
| coooc | 124-Lead RP 132-Lead FE | 16,20,25,33 16,20,25,33 | CCC | Elimanosa de Britin d | CRP16,20,25,33 | 1 0 | 1 36 | 14 180 | | internal parallel buses, enhanced bus controller, and on-chip MMU. |
| | | | | | | For FE | sample or | der—SP | AK030FEXX | C |
| MC68EC030 | 124-Lead RP 132-Lead FE | 25, 40 25, 40 | C | Embedded MPU | CRP25 | 1 1 | 1 36 | 14 180 | | 32-bit MPU for embedded applications. On-chip instruction and data cache provide high-speed access for control routines and data. Utilizes low-cost DRAM bus interface. |
| | | | | | | For FE, | PV sampl | le order— | -SPAKEC03 | OFEXXC, SPAKEC030PVXXC |
| MC68040 | 179-Lead RC 184-Lead FE | 25, 33, 40 25, 33, 40 | | 32-Bit MPU MMU FPU | | 1 0 | 1 24 | 10 96 | | Complete 32-bit MPU with on-chip instruction/data caches (4k bytes each). On-chip MMU. Full IEEE floating point, multiprocessing support with full M68000 Family compatibility. |
| | | | | | | For FE | sample or | der—SP. | AK040FEXX | |
| MC68EC040 | 179-Lead RC 184-Lead FE | 20, 25, 33, 40 20, 25, 33, 40 | | Embedded 32-Bit High Performance Proces- sor | | 1 0 | 1 24 | 10 96 | 120 | High-performance 32-bit MPU with on-chip instruction and data cache provides high-speed access for control routines and data. Utilizes low-cost DRAM bus interface. |
| | | | | | | For sar | nple order | r—SPAK | 68EC040RC | XX, SPAKEC040FEXX, SPAKEC040FSXX |
| MC68LC040 | 179-Lead RC 184-Lead FE | 20, 25, 33, 40 20, 25, 33, 40 | | High Performance 32- Bit Processor | | 1 0 | 1 24 | 10 96 | 120 | 68040-compatible integer unit and MMU. Ideal solution for cost- sensitive computer or sophisticated embedded applications. |
| | | | | | | For FE | sample or | der—SP. | AKLC040FE | XX |
| MC68040V | 179-Lead RC 184-Lead FE | 25, 33,40 @ 3.3 V 25,33 @ 3.3 V | | 32-Bit MPU MMU, Low-Voltage | | 1 0 | 1 24 | 0 96 | | Low-voltage complete 32-bit MPU with on-chip instruction/data caches (4k bytes each). On-chip MMU. Multiprocessing support. |
| | | | | | | For FE | L sample or | der—SP. | AKEC040VF | I EXX, SPAKEC040VRCXX |
| MC68060 | 206-Lead RC | 50 | | Superscalar 32-Bit Processor | | 0 | 1 | 10 | | RISC hybrid superscalar MPU with full M68000 Family compati- bility Includes dual integer units, on-chip instruction/data caches (8K bytes each), on-chip MMU, and full IEEE compliant |
| MC68EC060 | 206-Lead RC 304-Lead ZU | 50, 66, 75 50, 66, 75 | | Superscalar 32-Bit Processor | | 0 1 | 1 27 | 10 27 | | FPU. RISC hybrid superscalar MPU with full M68000 Family compati- bility includes dual integer units, on-chip instruction/data caches (8K bytes each), ideal for high-performance embedded control applications. |
| MC68LC060 | 206-Lead RC | 50, 66, 75 | | Superscalar 32-Bit Processor | | 0 | 1 | 10 | | RISC hybrid superscalar MPU with full M68000 Family compati- bility. Includes dual integer units, on-chip instruction/data caches (8K bytes each) and on-chip MM/U. |
| MC68882 | 68-Lead RC 68-Lead FN | 16,20,25,33,40,50 16,20,25,33,40 | A A | Enhanced Floating- Point Coprocessor (EFPCP) | CRC16,20,25,33 CFN16,20,25,33 | 1 1 | 1 1 | 21 18 | | Pin-to-pin timing and software compatibility with MC68881. Dual ported registers and increased pipelining allows 2-4 × performance of MC68881. |

68K General-Purpose Integrated Processors

| Device No. | Package | Speeds | Rev | Device Name | Temp** (-40 to +85°C)** | SOQ MPQ POQ BRICK Description | | | Description | |
|-----------------------|---|--|------------------|---|--|-------------------------------|----------------------------|----------------------------|-------------------|--|
| MC68306 | 132-Lead FC 144-Lead PV | 16,20 16,20 | В | Integrated EC000 Processor | CFC16 | 0 | 36 60 | 144 600 | 300 | 68000 CPU, 68681 DUART, DRAM control all in one chip. |
| | | | | | | For FC, | PV sampl | e order— | -SPAK306F | CXXB, SPAK306PVXXB |
| XC68307* XC68307V* | 100-Lead FG 100-Lead PU 100-Lead FG 100-Lead PU | 16 16 8,16 @ 3.3 V 8,16 @ 3.3 V | | Integrated Multiple Bus Processor | CFG16 | 0 0 0 0 | 66 84 66 84 | 264 420 264 420 | | Static EC000 Core Processor, UART, M-Bus Dual Timers, 8051 interface, dynamic 68000 bus. |
| | | | | | | For FG, | PU samp | le order— | -SPAK307F | GXX, SPAK307FGXXV, SPAK307PUXX, SPAK307PUXXV |
| MC68340 MC68340V | 144-Lead FE* 144-Lead PV 144-Lead FT 144-Lead FE* 144-Lead PV | 16, 25 16, 25 16, 25 16 @ 3.3V 16 @ 3.3V | E E E E | Integrated Processor with DMA | CFE16, CFE25 CPV16, CPV25 CFT16, CFT25 | 0 0 0 0 | 24 60 24 24 60 | 96 60 96 96 60 | 120 300 120 | CPU32 core processor for data movement applications. Two channel DMA, two serial channels, two timers, chip selects, wait-state generation, and glue logic. MC68340V is the 3.3 volt version of the MC68340. |
| | | | | | | For FE, | FT, and P | V sample | order—SP | AK340FEXXE, SPAK340FTXXVE, SPAK340PVXXVE |
| * Not recommen | * Not recommended for new designs. ** Extended temperature devices with minimum order requirements. | | | | | | | | | |

ColdFire Processors

| Device No. | Package | Speeds | Rev | Device Name | Temp** (-40 to +85°C)** | SOQ | MPQ | POQ | BRICK | Description |
|----------------|-----------------------|-----------------|-----------|---|----------------------------|--------|-----------|-----------|-----------|--|
| MCF5102 | 144-Lead PV | 16, 20, 25, 33 | В | Embedded 68K/ColdFire MPU | | 0 | 60 | 240 | | ColdFire microprocessor designed for cost-sensitive embedded control applications. In addition to executing ColdFire code, this first family member is designed with additional capabilities that allow it to execute existing M680x0 code. Processor includes on-chip instruction/data caches (2K/1K respectively). |
| | | | | | | For PV | sample o | rder—SP | AK5102PVX | XB |
| XCF5202 | 100-Lead PU | 16, 25, 33 | А | Embedded 68K/ColdFire MPU | CPU25A | 0 | 84 | 420 | | ColdFire microprocessor designed for cost-sensitive embedded control applications. This member features a 2K unified cache. |
| | | | | | | For PU | sample o | rder—SF | AK5202PU) | XXA |
| MCF5204 | 100-Lead PU | 16, 25, 33 | А | Embedded Integrated 68K/ColdFire | CPU25A | 0 | 84 | 84 | | ColdFire microprocessor designed for cost-sensitive embedded control applications with UART, 2 timers. |
| | | | | MPU | | For PU | sample o | rder—SF | AK5204PU) | XXA |
| MCF5206 | 160-Lead FT | 16, 25, 33 | | Embedded Integrated 68K/ColdFire | CFT16 CFT25 | 0 | 24 | 120 | | ColdFire microprocessor designed for cost-sensitive embedded control applications with UART, 2 timers, DRAM controller. |
| | | | | MPU | | For FT | sample or | der—SP | AK5206FTX | X |
| XCF5206e | 160-Lead FT | 40, 54 | | Embedded Integrated 68K/ColdFire MPU | CFT40 | 24 | 24 | 120 | | Enhanced, pin-compatible version of 5206 with larger caches and SRAM, 2 UARTs, 2 timers, DMA, MAC, HW Divide. 3.3V with 5V-tolerant I/O. |
| | | | | IVIPU | | For sa | mple orde | r - SPAK | 206EFTXX | SPAK5206ECFT40 |
| XCF5307 | 208-Lead FT | 66, 90 | | Embedded Integrated 68K/ColdFire MPU | CFT66 | 0 | 24 | 120 | | ColdFire Version 3 microprocessor with Multiply-Accumulate (MAC) unit, SDRAM Controller, DMA Controller, 2 UARTs, and 2 timers. |
| | | | | IVIPU | | For FT | sample or | der - SPA | K5307FTX | < |
| * Not recommer | nded for new designs. | ** Extended ten | nperature | devices with minimum o | order requirements. | 1 | | | | |

End-of-Life Devices

| Device | Last Buy | Last Ship | Replacement |
|--------------------------------|-------------------------------|-------------------------------|---|
| MPC604R | 1/21/00 | 7/21/00 | MPC740, MPC750, PowerPC G4 |
| MC68349 MC68330 MC68330V | 6/30/99 6/30/99 6/30/99 | 4/30/00 4/30/00 4/30/00 | MCF5206e, MCF5307 MCF5206e, MCF5307 MCF5206e, MCF5307 |

Timing Solutions

| Device No. | Description | Output Level | Max. Output to Output Skew* | Max. Output (MHz) | Q Output | Q' Output | Packages | Status |
|----------------|--|-----------------|--------------------------------|----------------------|---------------|-----------|----------|---------|
| MC88915FN55 | Low Skew CMOS PLL Clock Driver | CMOS | 0.5 | 13.75, 27.5, 55 | 7 | 1 | 28 PLCC | NOW |
| MC88915FN70 | Low Skew CMOS PLL Clock Driver | CMOS | 0.5 | 17.5, 35, 70 | 7 | 1 | 28 PLCC | NOW |
| MC88915T | Low Skew CMOS PLL Clock Drivers, 3-State | CMOS | 0.5 | 33, 66, 133, 160 | 7 | 1 | 28 PLCC | NOW |
| MC88916 | Low Skew CMOS PLL Clock Driver With Processor Reset | CMOS | 0.5 | 20, 40, 80 | 5 | 1 | 20 SOIC | NOW |
| MC88920 | Low Skew CMOS PLL Clock Driver With Power Down/Up | CMOS | 0.5 | 12.5, 25, 50 | 5 | 1 | 20 SOIC | NOW |
| MC88921 | Low Skew CMOS PLL Clock Driver With Power Down/Up | CMOS | 0.5 | 80 | 2 | 1 | 20 SOIC | NOW |
| MC88LV915T | Low Voltage Low Skew CMOS PLL Clock Driver 3-State | LVCMOS | 0.5 | 100 | 7 | 1 | 28 PLCC | NOW |
| MC88LV926 | Low Skew CMOS PLL 68060 Clock Driver | LVCMOS | 0.5 | 66 | 4 | 1 | 20 SOIC | NOW |
| MPC903/904/905 | 1:6 PCI Clock Generator/Fanout Buffer | LVCMOS | 0.4 | 66 | 6 | _ | 16 SOIC | NOW |
| MPC930/931 | Low Voltage PLL Clock Driver | LVCMOS | 0.5 | 125 | 5 | _ | 32 LQFP | NOW |
| MPC932 | Low Voltage PLL Clock Driver | LVCMOS | 0.6 | 120 | 6 | _ | 32 LQFP | NOW |
| MPC940L | Low Voltage 1:18 Clock Distribution Chip | LVCMOS | 0.25 | 200 | 18 | _ | 32 LQFP | NOW |
| MPC941L | Low Voltage 1:27 Clock Distribution Chip | LVCMOS | 0.25 | 200 | 27 | _ | 52 LQFP | 4Q99 |
| MPC947 | Low Voltage 1:9 Clock Distribution Chip | LVCMOS | 0.5 | 100 | 9 | _ | 32 LQFP | NOW |
| MPC948 | Low Voltage 1:12 PECL To CMOS Clock Driver | LVCMOS | 0.35 | 150 | 12 | _ | 32 LQFP | NOW |
| MPC948L | Low Voltage 1:12 PECL To CMOS Clock Driver | LVCMOS | 0.35 | 150 | 12 | _ | 32 LQFP | NOW |
| MPC949 | Low Voltage 1:15 PECL To CMOS Clock Driver | LVCMOS | 0.35 | 150 | 15 | _ | 52 LQFP | NOW |
| MPC950/951 | Low Voltage PLL Clock Driver | LVCMOS | 0.35 | 200 | 9 | _ | 32 TQFP | NOW |
| MPC952 | Low Voltage PLL Clock Driver | LVCMOS | 0.35 | 180 | 11 | _ | 32 TQFP | NOW |
| MPC953 | Low Skew PLL Zero Delay Buffer | LVCMOS | 0.15 | 120 | 9 | _ | 32 LQFP | NOW |
| MPC954 | 1:10 SDRAM Zero Delay Buffer | LVCMOS | .20 | 100 | 10 | _ | 24 TSSOP | 3Q99 |
| MPC972/973 | Low Voltage PLL Clock Driver | LVCMOS | 0.35 | 180 | 14 | _ | 52 TQFP | NOW |
| MPC974 | Low Voltage PLL Clock Driver | LVCMOS | 0.35 | 125 | 15 | _ | 52 LQFP | NOW |
| MPC980 | Dual 3.3V Clock Generator | LVCMOS | 0.5 | 66 | 10 | _ | 52 LQFP | NOW |
| MPC990/991 | Low Voltage PLL Clock Driver | ECL/PECL | 0.1 | 400 | diff 14/pairs | _ | 52 TQFP | NOW |
| MPC992 | Low Voltage PECL PLL Clock Driver | ECL/PECL | 0.1 | 100 | diff 7/pairs | _ | 32 LQFP | NOW |
| MPC993 | Dynamic Switch PLL Clock Driver | LVPECL | .10 | 240 | diff 5/pairs | _ | 32 TQFP | NOW |
| MPC996 | Low Voltage PLL | ECLPECL | _ | 350 | 12 | _ | 32 TQFP | 3Q99 |
| MPC9109 | 1:18 LVCMOS Fanout Buffer | LVCMOS | .20 | 100 | 18 | _ | 32 TQFP | NOW |
| MPC9120 | 1:10 LVCMOS Fanout Buffer — Bx Intel Mobile | LVCMOS | .25 | 100 | 10 | _ | 28 SSOP | Planned |
| MPC9121 | PC Clock Generator — Bx Intel Mobile | _ | _ | _ | _ | _ | _ | NOW |
| MPC9140 | 1:18 LVCMOS Fanout Buffer — Bx Intel Desktop | LVCMOS | .25 | 100 | 18 | _ | 48 SSOP | NOW |
| MC12429 | High Frequency PLL Clock Generator | LVPECL | _ | 400 | diff1/pair | _ | 28 PLCC | NOW |
| MC12430 | High Frequency PLL Clock Generator | LVPECL | _ | 800 | diff1/pair | _ | 28 PLCC | NOW |
| MC12439 | High Frequency PLL Clock Generator | LVPECL | _ | 800 | diff1/pair | _ | 28 PLCC | NOW |
| MPC911 | Low Voltage 1:9 Differential ECL/HSTL to HSTL Clock Driver | HSTL | 0.05 | 200 | 9 | 9 | 28 PLCC | NOW |
| MPC9100 | Low voltage Dual PLL Clock Driver | LVCMOS | _ | 14, 31, 45 | 3 | _ | 32 LQFP | NOW |
| XC100EP111 | Low Voltage 1:10 Diff ECL/PECL/HSTL Clock Driver | LVPECL | 0.035 | 1500 | diff 10/pairs | _ | 32 LQFP | MC 9/99 |
| XC100EP210 | Low Voltage 1:5 Diff ECL/PECL Clock Driver | LVPECL | 0.035 | 1500 | diff 5/pairs | _ | 32 LQFP | MC 9/99 |
| PC100EP221 | Low Voltage 1:20 Diff ECL/PECL Clock Driver | LVPECL | 0.05 | 1500 | diff 20/pairs | _ | 52 LQFP | Planned |
| PC100EP223 | Low Voltage 1:22 Diff PECL/HSTL Clock Driver | LVPECL | 0.05 | 250 | diff 22/pairs | _ | 64 LQFP | MC 9/99 |
| | | _ | _ | _ | _ | _ | | |

Late Write RAMs (Synchronous)

| Category | Organization | V _{DD} | Device No. | Pin Count | Package | Speeds | Prod. Status | Description |
|----------|--------------|-----------------|------------|--------------|------------------------------|--------------------------------------|----------------------------------|---|
| 8M | 512K x 18 | 2.5V - 3.3V | MCM63L918A | 119 | (FC) FC-PBGA | 3.8 / 4.0 / 4.2 / 4.5 ns Latency | Now | Register/Latch. Extended HSTL I/Os |
| | | | MCM63R918 | 119 | (RS) FC-CBGA (FC) FC-PBGA | 3.0 / 3.3 / 3.7 / 4.0 / 4.4 / 5.0 ns | Now | Register/Register. HSTL I/Os |
| | | | MCM63R918A | 119 | (FC) FC-PBGA | 3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns | Now | Register/Register. Extended HSTL I/Os |
| | 256K x 36 | 2.5V - 3.3V | MCM63L836A | 119 | (FC) FC-PBGA | 3.8 / 4.0 / 4.2 / 4.5 ns Latency | Now | Register/Latch. Extended HSTL I/Os |
| | | | MCM63R836 | 119 | (RS) FC-CBGA (FC) FC-PBGA | 3.0 / 3.3 / 3.7 / 4.0 / 4.4 / 5.0 ns | Now | Register/Register. HSTL I/Os |
| | | | MCM63R836A | 119 | (FC) FC-PBGA | 3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns | Now | Register/Register. Extended HSTL I/Os |
| 4M | 256K x 18 | 2.5V - 3.3V | MCM63R818 | 119 | (FC) FC-PBGA | 3.0 / 3.3 / 3.7 / 4.0 ns | Now | Register/Register. HSTL I/Os |
| | | 3.3V | MCM69R819A | 119 | (ZP) PBGA | 5.0 / 6.0 / 7.0 ns | Now | Register/Register. LVTTL I/Os. Not rec. for new designs. |
| | | | MCM69L819A | 119 | (ZP) PBGA | 8.5 / 9.0 / 9.5 ns Latency | Now | Register/Latch. LVTTL I/Os. Not rec. for new designs. |
| | | | MCM69R818C | 119 | (ZP) PBGA | 4.0 / 4.4 / 5.0 / 6.0 / 7.0 ns | Now | Register/Register. HSTL I/Os. Process shrink. |
| | | | | MCM69L818C | 119 | (ZP) PBGA | 5.5 / 6.5 / 7.5 / 8.5 ns Latency | Con- tact Fac- tory |
| | | | MCM69R820C | 119 | (ZP) PBGA | 4.0 / 4.4 / 5.0 / 6.0 / 7.0 ns | Now | Register/Register. Process shrink. 2.5 V I/Os. |
| | 128K x 36 | 2.5V - 3.3V | MCM63R736 | 119 | (FC) FC-PBGA | 3.0 / 3.3 / 3.7 / 4.0 ns | Now | Register/Register. HSTL I/Os |
| | | 3.3V | MCM69R737A | 119 | (ZP) PBGA | 5.0 / 6.0 / 7.0 ns | Now | Register/Register. LVTTL I/Os. Not rec. for new designs. |
| | | | MCM69L737A | 119 | (ZP) PBGA | 8.5 / 9.0 / 9.5 ns Latency | Now | Register/Latch. LVTTL I/Os. Not rec. for new designs. |
| | | | MCM69R736C | 119 | (ZP) PBGA | 4.0 / 4.4 / 5.0 / 6.0 / 7.0 ns | Now | Register/Register. HSTL I/Os. Process shrink. |
| | | | MCM69L736C | 119 | (ZP) PBGA | 5.5 / 6.5 / 7.5 / 8.5 ns Latency | Con- tact Fac- tory | Register/Latch. HSTL I/Os. Not recommended for new designs. |
| | | | MCM69R738C | 119 | (ZP) PBGA | 4.0 / 4.4 / 5.0 / 6.0 / 7.0 ns | Now | Register/Register. Process shrink. 2.5 V I/Os. |
| 1M | 64K x 18 | 3.3V | MCM69R618 | 119 | (ZP) PBGA | 4.4 / 5.0 / 6.0 / 7.0 ns | Now | Register/Register. HSTL I/Os. Not rec. for new designs. |
| | 32K x 36 | 3.3V | MCM69R536 | 119 | (ZP) PBGA | 4.4 / 5.0 / 6.0 / 7.0 ns | Now | Register/Register. HSTL I/Os. Not rec. for new designs. |

Double Data Rate (DDR) RAMs

| M8 | 512K x 18 | 2.5V | MCM64E918 | 153 | (FC) FC-PBGA | 3.0 / 3.3 / 4.0 / 4.4 ns | Now | Data Rate 2x clock rate. |
|----|-----------|------|-----------|-----|--------------|--------------------------|-----|--------------------------|
| | 256K x 36 | 2.5V | MCM64E836 | 153 | (FC) FC-PBGA | 3.0 / 3.3 / 4.0 / 4.4 ns | Now | Data Rate 2x clock rate. |

BurstRAMs (Synchronous)

| Category | Organization | V_{DD} | Device No. | Pin Count | Package | Speeds | Prod. Status | Description |
|-------------------------------------|--------------|----------|------------|--------------|------------------------|----------------------------|-----------------|--|
| 8M | 512K x 18 | 3.3V | MCM63B919 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.0 / 8.0 / 8.5 ns Latency | 1Q00 | 2.5 V/3.3 V I/O flow–through or pipelined (225 / 200 / 166 MHz). |
| | 256K x 36 | 3.3V | MCM63B837 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.0 / 8.0 / 8.5 ns Latency | 1Q00 | 2.5 V/3.3 V I/O flow-through or pipelined (225 / 200 / 166 MHz). |
| 4M | 256K x 18 | 3.3V | MCM69P819 | 100 119 | (TQ) TQFP (ZP) PBGA | 166 / 150 / 133 MHz | Now | 2.5 V/3.3 V I/O pipelined. |
| | | | MCM69F819 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.5 / 8.0 / 8.5 / 11.0 ns | Now | 2.5 V/3.3 V I/O flow–through. |
| | | | MCM63B819A | 100 119 | (TQ) TQFP (ZP) PBGA | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 2.5 V/3.3 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |
| | | 2.5V | MCM64B819A | 100 119 | (TQ) TQFP (ZP) PBGA | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 2.5 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |
| (4M contin- ued on next page) | | 1.8V | MCM65B819A | 100 119 | (TQ) TQFP (ZP) PBGA | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 1.8 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |

BurstRAMs (Synchronous) (Continued)

| Category | Organization | V _{DD} | Device No. | Pin Count | Package | Speeds | Prod. Status | Description |
|---------------------|--------------|-----------------|------------|--------------|------------------------|---------------------------------------|-----------------|--|
| 4M (continued | 128K x 36 | 3.3V | MCM69P737 | 100 119 | (TQ) TQFP (ZP) PBGA | 200 / 183 / 166 / 150 / 133 MHz | Now | 2.5 V/3.3 V I/O pipelined. |
| from previous page) | | | MCM69F737 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.5 / 8.0 / 8.5 / 11 ns | Now | 2.5 V/3.3 V I/O flow–through. |
| | | | MCM63B737A | 100 119 | (TQ) TQFP (ZP) PBGA | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 2.5 V/3.3 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |
| | | 2.5V | MCM64B737A | 100 119 | (TQ) TQFP (ZP) PBGA | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 2.5 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |
| | | 1.8V | MCM65B737A | 100 119 | (TQ) TQFP (ZP) PBGA | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 1.8 V I/O flow-through or pipelined (250 / 225 / 200 MHz). |
| | 128K x 32 | 3.3V | MCM63P733A | 100 | (TQ) TQFP | 150 / 133 / 117 / 100 / 90 MHz | Now | 2.5 V/3.3 V I/O pipelined. |
| | | | MCM63F733A | 100 | (TQ) TQFP | 8.5 / 9.0 / 10.0 / 11.0 ns | Now | 2.5 V/3.3 V I/O flow-through. |
| | | | SCM63F733A | 100 | (TQ) TQFP | 10.0 / 11.0 ns | Now | 2.5 V/3.3 V I/O flow-through, - 40° to + 85°C. |
| | | | MCM63B733A | 100 | (TQ) TQFP | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 2.5 V/3.3 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |
| | | 2.5V | MCM64B733A | 100 | (TQ) TQFP | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 2.5 V I/O flow–through or pipelined (250 / 225 / 200 MHz). |
| | | 1.8V | MCM65B733A | 100 | (TQ) TQFP | 6.5 / 7.0 / 8.0 ns Latency | 4Q99 | 1.8 V I/O flow-through or pipelined (250 / 225 / 200 MHz). |
| 1M | 64K x 18 | 3.3V | MCM69F618C | 100 | (TQ) TQFP | 7.5 / 8.0 / 8.5 / 9.0 /10.0 / 12.0 ns | Now | Flow-through BurstRAM, 5 V tolerant on all pins. |
| | | | MCM69P618C | 100 | (TQ) TQFP | 133 / 125 / 100 / 83 / 75 MHz | Now | Pipelined BurstRAM, 5 V tolerant on all pins. |
| | | 5V | MCM67B618A | 52 | (FN) PLCC | 8.5 / 9.0 / 10.0 / 12.0 ns | Now | Flow-through BurstRAM for Pentium, MIPS. |
| | | | MCM67M618A | 52 | (FN) PLCC | 9.0 / 10.0 / 12.0 ns | Now | Flow-through BurstRAM for PowerPC. |
| | 32K x 36 | 3.3V | MCM69F536C | 100 | (TQ) TQFP | 7.5 / 8.0 / 8.5 / 9.0 /10.0 / 12.0 ns | Now | Flow-through BurstRAM, 5 V tolerant on all pins. |
| | | | MCM69P536C | 100 | (TQ) TQFP | 133 / 125 / 100 / 83 / 75 MHz | Now | Pipelined BurstRAM, 5 V tolerant on all pins. |

ZBT™ (Zero Bus Turnaround™) RAMs (Synchronous)

| Category | Organization | V _{DD} | Device No. | Pin Count | Package | Speeds | Prod. Status | Description |
|----------------------------------|--------------|-----------------|---------------|--------------|------------------------|-------------------------------|-----------------|---|
| 8M | 512K x 18 | 3.3V | MCM63Z918 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.0 / 8.0 / 8.5 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4099. |
| | | | MCM63Z916 | 100 119 | (TQ) TQFP (ZP) PBGA | 10.0 / 11.0 / 15.0 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| | | 2.5V | MCM64Z918 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.0 / 8.0 / 8.5 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| | | | MCM64Z916 | 100 119 | (TQ) TQFP (ZP) PBGA | 10.0 / 11.0 / 15.0 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| | 256K x 36 | 3.3V | MCM63Z836 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.0 / 8.0 / 8.5 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| | | | MCM63Z834 | 100 119 | (TQ) TQFP (ZP) PBGA | 10.0 / 11.0 / 15.0 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| | | 2.5V | MCM64Z836 | 100 119 | (TQ) TQFP (ZP) PBGA | 7.0 / 8.0 / 8.5 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| | | | MCM64Z834 | 100 119 | (TQ) TQFP (ZP) PBGA | 10.0 / 11.0 / 15.0 ns Latency | 1Q00 | Pipelined or flow-through with back-to-back read/write write/read cycles. Sampling 4Q99. |
| 4M | 256K x 18 | 3.3V | MCM63Z818 | 100 | (TQ) TQFP | 143 / 133 / 100 MHz | Now | Pipelined with back-to-back read/write write/read cycles. |
| | | | MCM63Z819 | 100 | (TQ) TQFP | 10.0 / 11.0 / 15.0 ns | Now | Flow-through with back-to-back read/write write/read cycles. |
| | 128K x 36 | 3.3V | MCM63Z736 | 100 | (TQ) TQFP | 143 / 133 / 100 MHz | Now | Pipelined with back-to-back read/write write/read cycles. |
| | | | MCM63Z737 | 100 | (TQ) TQFP | 10.0 / 11.0 / 15.0 ns | Now | Flow-through with back-to-back read/write write/read cycles. |
| CAMs (| Content A | ddres | sable Memory) | , | | | | |
| CAMs | 16K x 64 | 3.3V | MCM69C432 | 100 | (TQ) TQFP | 180 ns Match Time | Now | Content addressable memory for communication applications 16K connections. |
| | 4K x 64 | 3.3V | MCM69C232 | 100 | (TQ) TQFP | 160 ns Match Time | Now | Content addressable memory for communication applications 4K connections. |
| Tag RA | Ms | | | | | | | |
| Tag RAMs | 64K x 18 | 3.3V | MCM69T618 | 100 | (TQ) TQFP | 5 ns | Now | 100 MHz Data/Tag RAM. For MIPS R5000, Pentium Pro, and graphics accelerators applications. Not recommended for new designs. |
| Integra | ted Cache | Soluti | ions | | 1 | ' | ļ | |
| Integrated Cache Solutions | 32K x 72 | 3.3V | MPC2605 | 241 | (ZP) PBGA | 83 / 66 MHz | Now | Integrated L2 cache for PowerPC processors. One component for 256KB, two for 512KB, and four for 1MB L2 cache solution. |

ZBT™ (Zero Bus Turnaround™) RAMs (Synchronous)

(Continued)

| | | | <u> </u> | | | | | | | |
|-------------------------------|--------------|----------|------------|--------------|-----------|----------------|-----------------|---|--|--|
| Category | Organization | V_{DD} | Device No. | Pin Count | Package | Speeds | Prod. Status | Description | | |
| Separate and Dual I/O Devices | | | | | | | | | | |
| 4M | 512K x 9 | 5V | MCM67Q909 | 86 | (ZP) PBGA | 10.0 / 12.0 ns | Now | General synchronous separate I/O with write pass through. 3.3 V output levels. Not recommended for new designs. | | |
| | 128K x 36 | 3.3V | MCM63D736 | 176 | (TQ) TQFP | 100 / 133 MHz | 1Q00 | Dual address, Dual I/O NetRAM pipelined per port chip enable. | | |
| 1M | 128K x 9 | 5V | MCM67Q709A | 86 | (ZP) PBGA | 10.0 ns | Now | General synchronous separate I/O with write pass through. 3.3 V output levels. Not recommended for new designs. | | |
| | 32K x 36 | 3.3V | MCM69D536 | 176 | (TQ) TQFP | 6.0 / 8.0 ns | Now | Dual address, dual I/O. NetRAM. | | |
| | 64K x 18 | 3.3V | MCM69D618 | 100 | (TQ) TQFP | 6.0 / 8.0 ns | Now | Dual address, dual I/O. NetRAM. | | |

Asynchronous RAMs

| Category | Organization | V _{DD} | Device No. | Pin Count | Package and Width in mils | Speeds | Prod. Status | Description |
|----------|--------------|-----------------|------------|--------------|---------------------------|------------------------------|-----------------|--|
| 4M | 512K x 8 | 3.3V | MCM6946 | 36 44 | 400 (YJ) SOJ (TS) TSOP | 10.0 / 12.0 / 15.0 ns | Now | Not recommended for new designs. |
| | 256K x 16 | 3.3V | MCM6343 | 44 | 400 (YJ) SOJ (TS) TSOP | 11.0 / 12.0 / 15.0 ns | Now | Not recommended for new designs. |
| | 1M x 4 | 3.3V | MCM6949 | 32 | 400 (YJ) SOJ | 10.0 / 12.0 / 15.0 ns | Now | Not recommended for new designs. |
| 3M | 128K x 24 | 3.3V | MCM6341 | 119 | (ZP) PBGA | 10.0 / 11.0 / 12.0 / 15.0 ns | Now | DSP applications for base stations and other communication applications. Industrial temperature. |
| 1M | 64K x 18 | 5V | MCM67A618A | 52 | (FN) PLCC | 10.0 / 12.0 / 15.0 ns | Now | General asynchronous, latched address and data. |
| | 128K x 8 | 3.3V | MCM6926A | 32 | 400 (WJ) SOJ | 8.0 / 10.0 / 12.0 / 15.0 ns | Now | EOL Status – Last Purchase January 2000. |
| | 256K x 4 | 3.3V | MCM6929A | 32 | 400 (WJ) SOJ | 8.0 / 10.0 / 12.0 / 15.0 ns | Now | EOL Status – Last Purchase January 2000. |

Documentation

To download documentation for Motorola PowerPC1xx, 6xx and 7xx CPUs:

http://motorola.com/SPS/PowerPC/teksupport/teklibrary/.

To download documentation for MPC8xx, MPC8xxx, and 68K integrated communications controllers:

http://motorola.com/SPS/RISC/netcomm/docs/pubs/.

To download documentation for 68K/ColdFire processors: http://motorola.com/SPS/HPESD/prod/docframe/ docs frame.html.

To download documentation for Motorola timing solutions: http://www.design-net.com/books/html/br1333_index.html.

For printed documentation for NSD and PCSD devices: http://www.design-net.com/home2/lit_ord.html.

Development Tools

For information on third-party tools for PowerPC1xx, 6xx and 7xx CPUs:

http://motorola.com/PowerPC/3rdparty/.

To download freeware tools for MPC8xx, MPC8xxx, and 68K integrated communications controllers, point your browser to: http://motorola.com/SPS/RISC/netcomm/tools/.

For information on third-party tools for 68K/ColdFire processors: http://motorola.com/SPS/HPESD/devprg/frames/mem_frame.html.

World Wide Web

Motorola PowerPC home page: http://motorola.com/PowerPC/

PowerPC 100, 600 and 700 series CPUs: http://motorola.com/PowerPC/products/semiconductor/ chips.html

AltiVec™ Technology http://motorola.com/AltiVec/

Networking & Communications (NetComm) home page: http://motorola.com/netcomm/

MPC801, MPC821, MPC823, MPC850, MPC860, MPC8260 and 68K

communications controllers:

http://www.mot.com/SPS/RISC/netcomm/prod/index.html

68K/ColdFire Processors home page: http://motorola.com/ColdFire/

Motorola timing solutions home page: http://www.design-net.com/logic/

Motorola FSRAM products home page: http://motorola.com/fastrams/

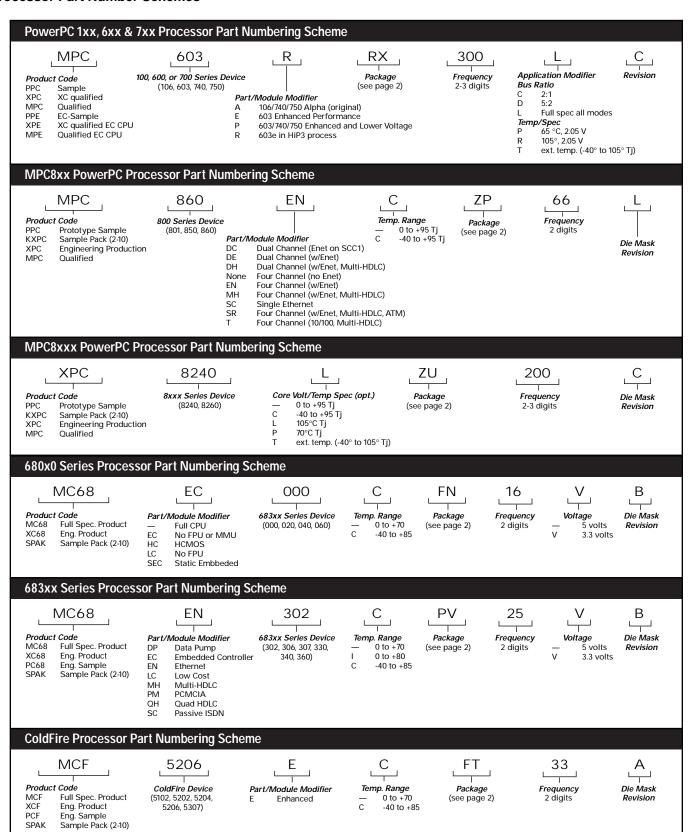
SPS Customer Response Center: http://www.design-net.com/home2/cust_serv.html

General product information on other devices: http://motorola.com/SPS/General/chips.html

Information on other Motorola products: http://motorola.com/General/prodport.html

Comments on other Motorola products: http://motorola.com/cgi-bin/web-comments2

Processor Part Number Schemes



Motorola Literature Distribution Centers:

USA/EUROPE: Motorola Literature Distribution; P.O.Box 5405, Denver Colorado 80217

Tel.: 1-800-441-2447 (in U.S.) or 1-303-675-2140

WWW: http://ldc.nmd.com/

JAPAN: Nippon Motorola Ltd. SPD, Strategic Planning Office 4-32-1, Nishi-Gotanda Shinagawa-ku, Tokyo 141, Japan

Tel.: 81-3-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.

Silicon Harbour Centre 2, Dai King Street, Tai Po Industrial Estate

Tai Po, New Territories, Hong Kong Mfax™: RMFAX0@email.sps.mot.com;

TOUCHTONE: 1-602-244-6609 US & Canada ONLY: 1-800-774-1848 WWW: http://sps.motorola.com/mfax INTERNET: http://motorola.com/sps/

Technical Information:

Motorola, Inc. SPS Customer Support Center 1-800-521-6274

Email: crc@wmkmail.sps.mot.com
Document Comments: FAX 1-512-895-2638
Attn: NSD Marketing Communications

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. PowerPC, the PowerPC logo, PowerPC 740, PowerPC 740, PowerPC750 are trademarks of International Business Machines Corporation and are used by Motorola, Inc. under license therefrom. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

