Gate drives

From previous notes we have seen that a good gate drive circuit should have a low source impedance. There are a number of other desirable features:

- The ability to drive the gate negative with respect to the source. This accelerates turn-off
- Fast rise and fall times for output voltages (and currents)
- Electrical isolation (between gate signal source and power circuit). This provides an added layer or protection and allows us to overcome the difficulties that arise when a number of MOSFETs must be driven whose source terminals are at different potentials.
- Good noise immunity (a low source impedance can achieve this)
- Over-current protection.

Figure 1 below shows a circuit that meets some of these requirements.

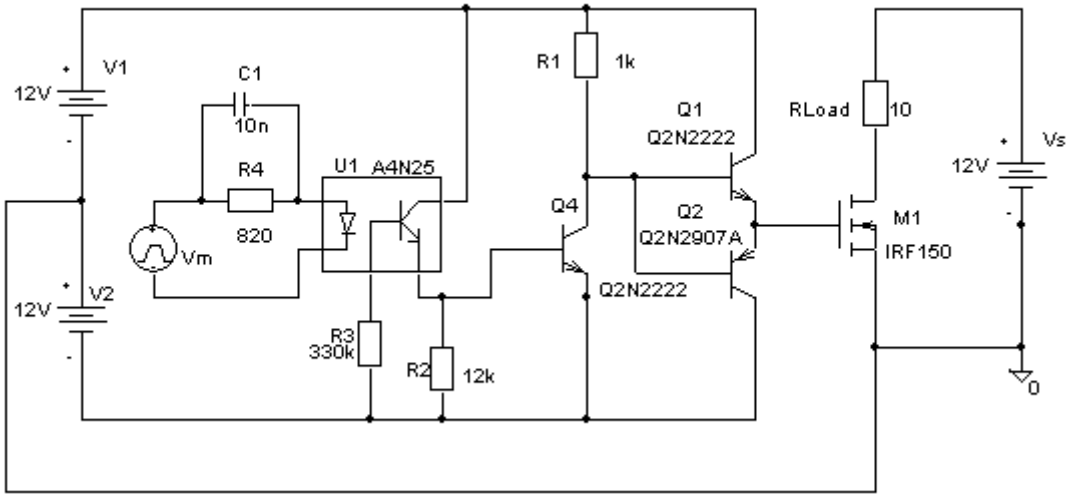

Figure 1: An opto-isolated gate drive made with discrete components

The signal source in this case is Vm which perhaps could originate in a microprocessor. U1 is an opto-isolator. Opto-isolators provide electrical isolation between different parts of a circuit. Signals are transmitted within opto-isolators using infra-red radiation (rather than by electrical means). The opto-isolator shown is a simple, single transistor. If current flows in the opto-diode (see Figure 2), the front-end transistor turns on. The “current gain” (or more usually current transfer ratio) of single-transistor opto-isolators is usually quite low (less than 0.5 or 50%) thus the collector current in the front-end transistor must be kept below the diode current to ensure that the transistor remains saturated.

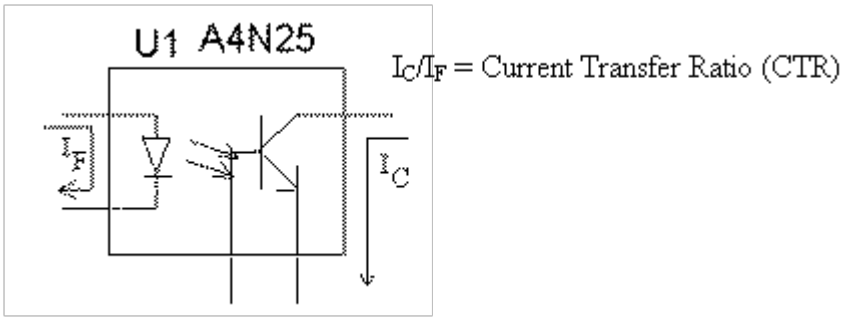

Figure 2: A 4N25 opto-isolator

Transistors Q1,Q2 and Q4 amplify the signal to ensure that the signal out to the MOSFET (Figure 3) has a steep rise time. This circuit exhibits a turn-on delay of about 2 microseconds which arises from the slow turn-off of the opto-transistor. In some cases, such as in bridge applications, such a turn on delay can be useful as it can allow other transistors sufficient time to turn off.

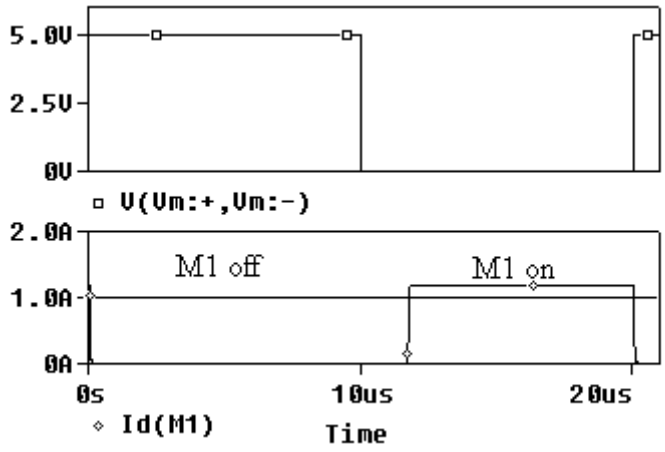

Figure 3: Drain current in relation to gate drive signal

Figure 4 shows a MOSFET bridge circuit. This type of circuit can pose particular difficulties as the source terminals of the 4 MOSFET's may be at different potentials.

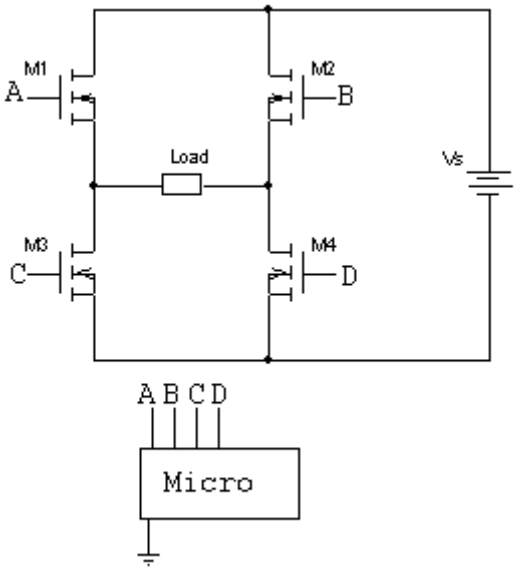

Figure 4 : Interconnection between gate drives and a controller

The microprocessor generates 4 control signals ABCD which much be connected to the gates of M1,2,3,4 respectively. Current returns to the microprocessor via its earth/ground pin which must be connected to the source terminals of each of the MOSFETS. Doing this would however bypass M3 and M4 resulting in damage to M1 and M2 when they turn on.

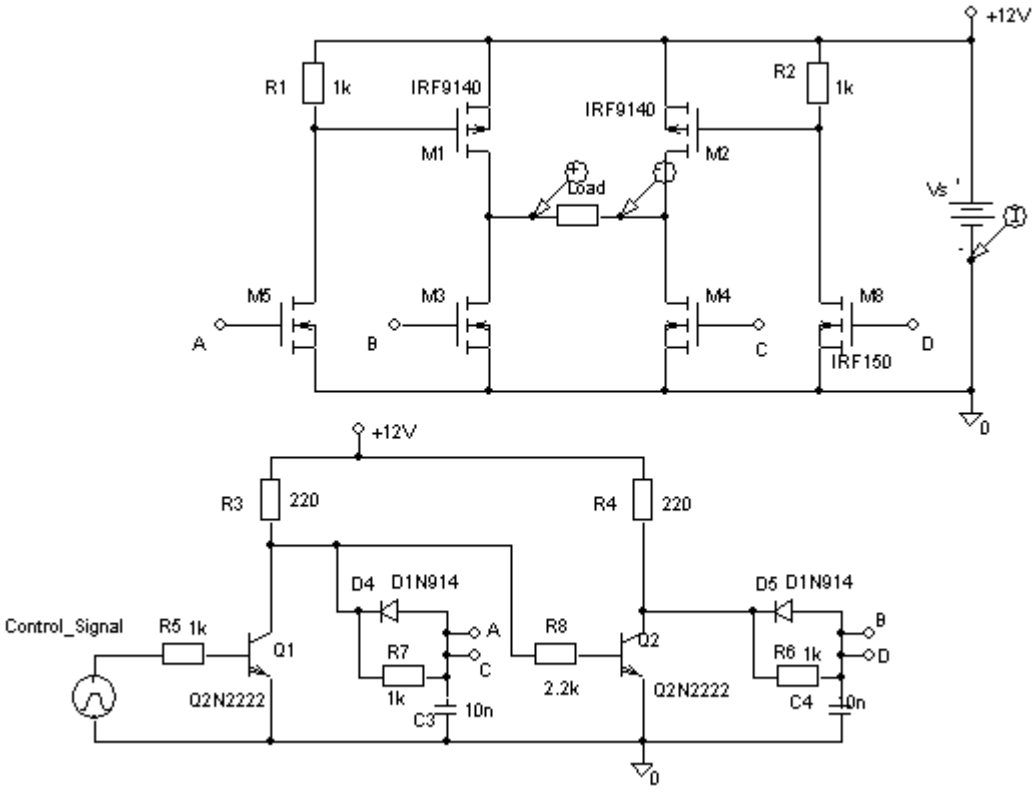

Figure 5 : A low voltage bridge

There are various solutions to the problem presented in Figure 4. If the voltage (Vs) is low enough, it may be possible to use complimentary MOSFETS (P-channel devices in place of M1 and M2) and drive them as shown in Figure 5.

An alternative to this approach is to use a “high-side”/ “low-side” driver chipset which typically integrates a circuit similar to that shown in Figure 6. Figure 7(a) and7(b) show the charge pump (made up of C1 and D1) which provides the high side driver with a power supply in action.

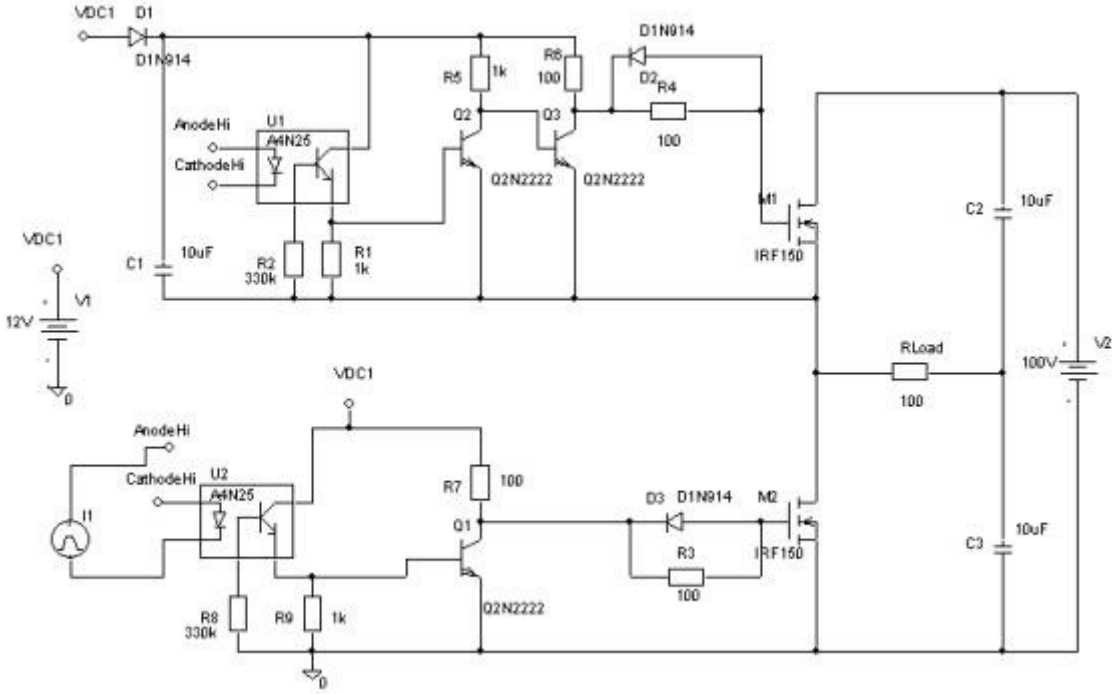

Figure 6: A charge pump based high/low side driver

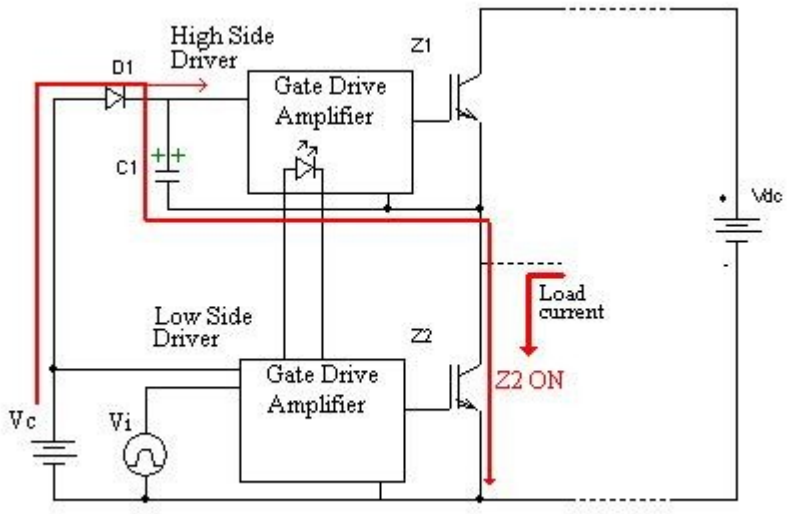

Figure 7a: Charging the upper capacitor

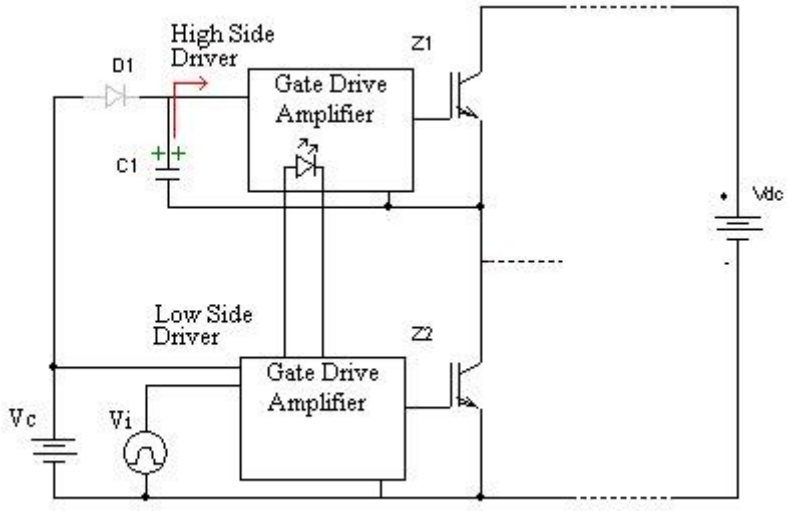

Figure 7b: Capacitor energy reserve used to power upper driver

Many of the above circuits have been improved and integrated over the past number of years. Opto-isolators such as the 6N137 provide easy to use digital output with very little propagation delay

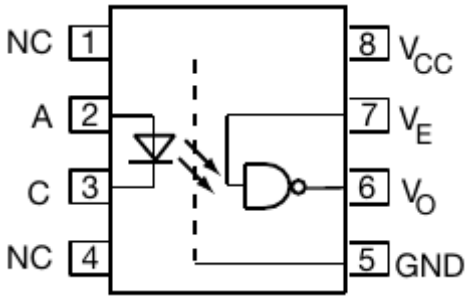

Figure 8: 6N137 digital opto-issolator

Full or half bridge drivers such as the LT1160 provide integrated solutions for inverters, while fully integrated inverters such as the STGIB15CH60TS offer complete inverter solutions