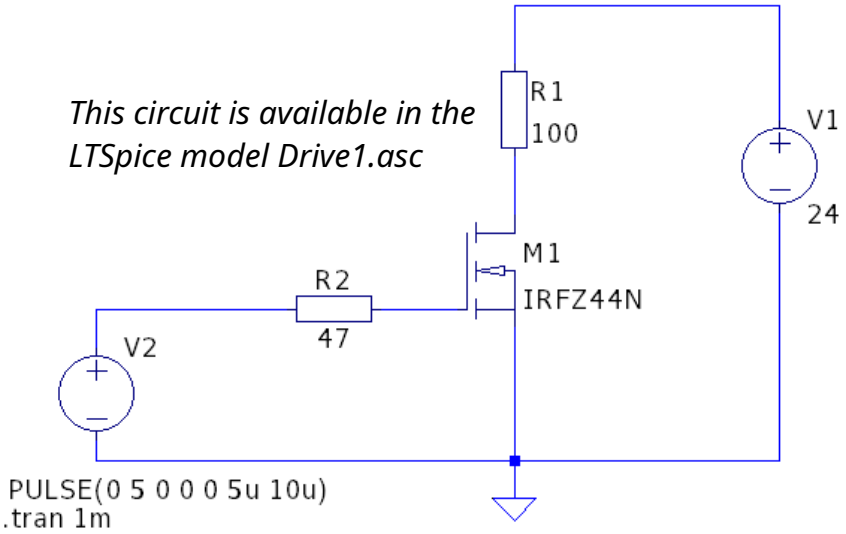
MOSFET switching and gate drives

In this lab you will explore the switching of MOSFETS.

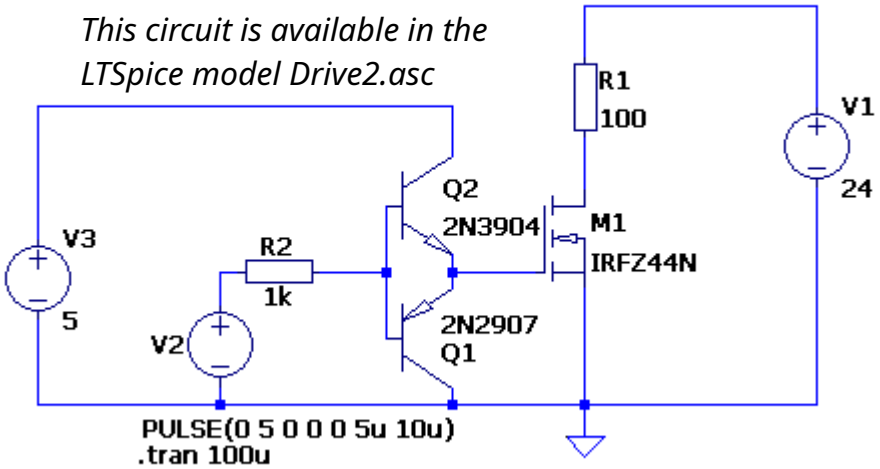
Circuit 1



Run the above model for 100uS and capture a screen shot of the following graphs (use multiple plot-panes)
V2, Ig for M1, Vds for M1, Power loss in M1.

Comment on how these graphs change when the gate resistor R2 is increased.
How does a bipolar gate drive fare (+/-12) – if better, why?

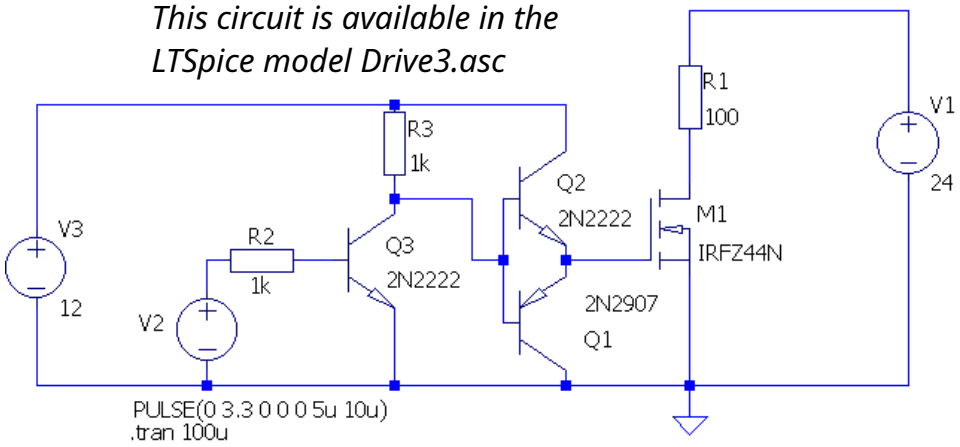
Circuit 2



How does the performance of Drive2 differ from Drive1 – is it an improvement and if so, how?

Circuit 3

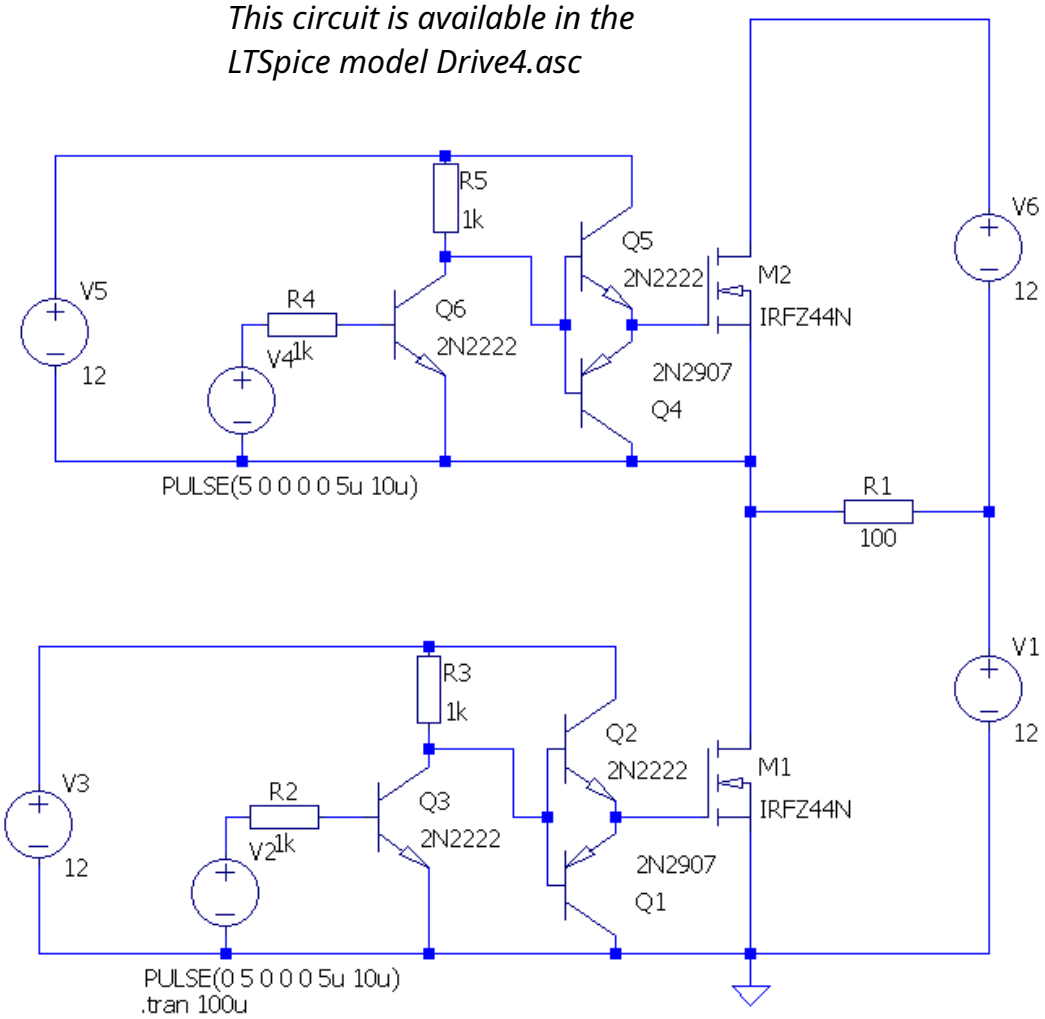
This circuit is available in the LTSpice model Drive3.asc



Circuit3 is a further refinement on Circuit2. The introduction of Q3 allows the signal source voltage to be different to the gate drive voltage – how does this help?

Circuit 4

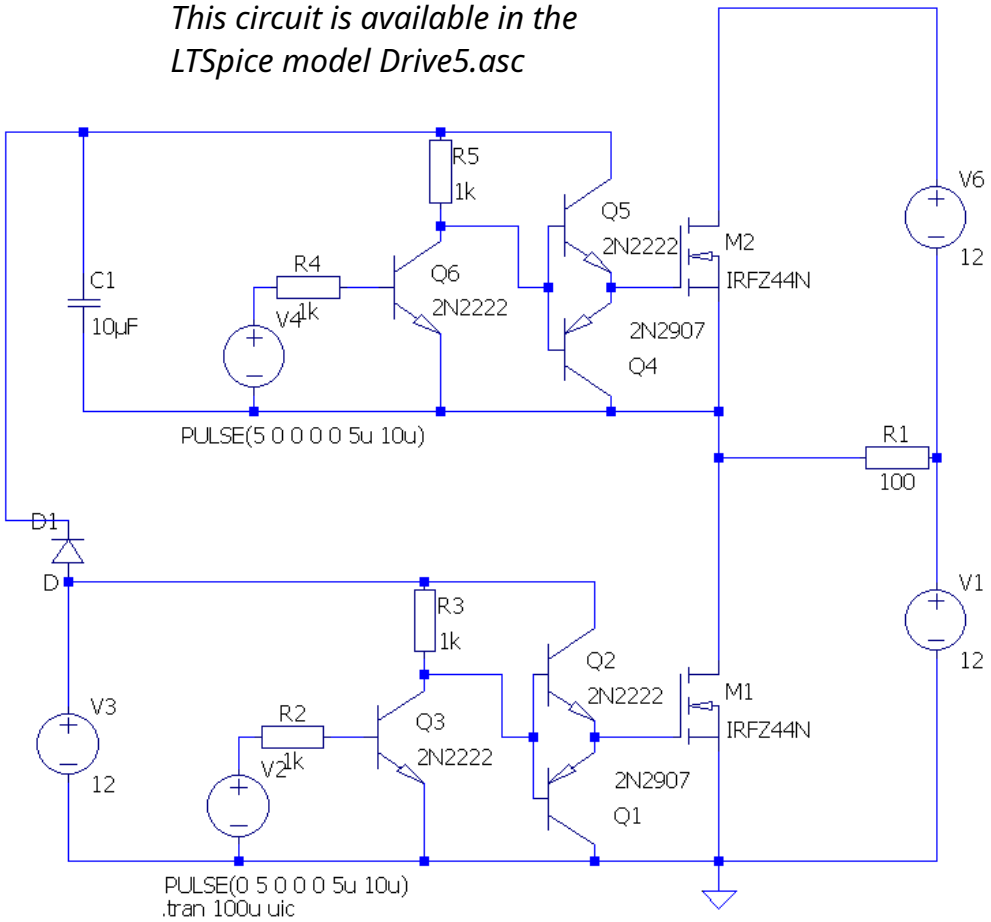
This circuit is available in the LTSpice model Drive4.asc



Circuit 4 includes two copies of the drive circuit from Circuit3 to allow upper and lower MOSFETS in a half bridge to be driven. Plot the voltage ***across*** R1 (not the voltage with respect to ground). Show that the voltage on the emitter of Q6 is very different to the voltage on the emitter of Q3 and hence rules out the possibility of the gate drives sharing a common ground.

Circuit 5

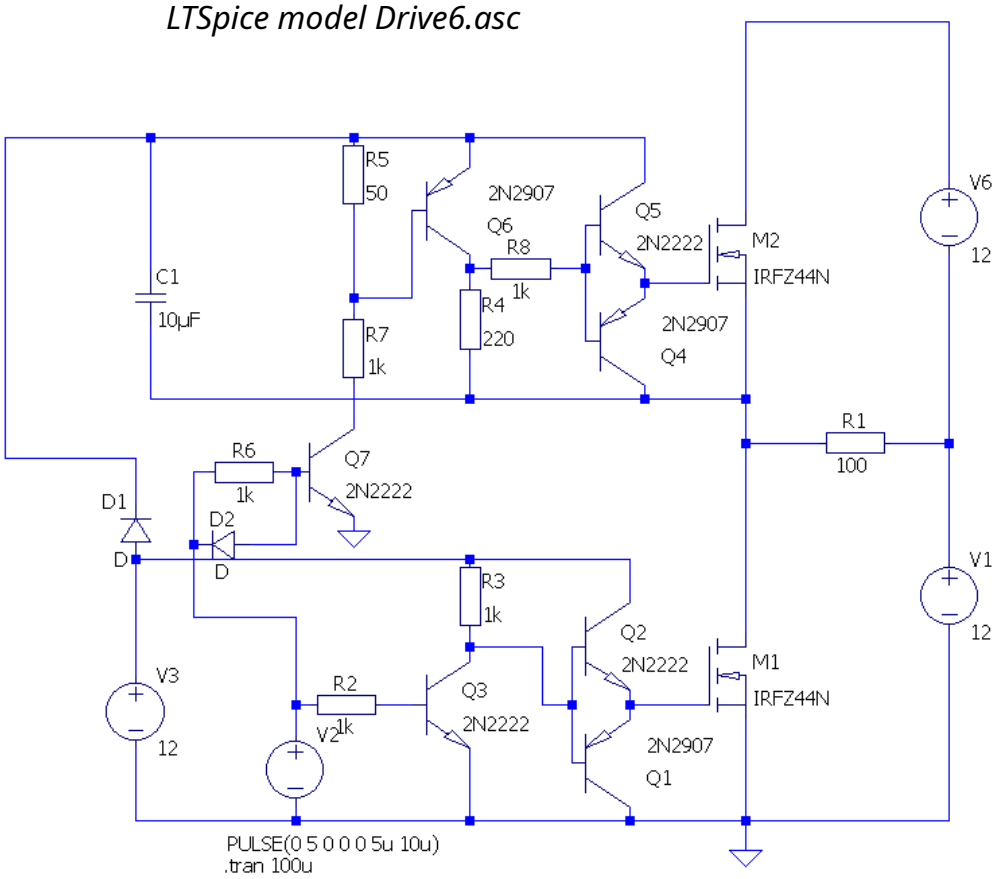
This circuit is available in the LTSpice model Drive5.asc



Circuit 5 is a refinement of Circuit 4. It allows us to eliminate the power source for the upper gate drive – how is this achieved? How does the size of C1 affect the performance of the circuit (i.e. if it is made MUCH larger or MUCH smaller)

Circuit 6

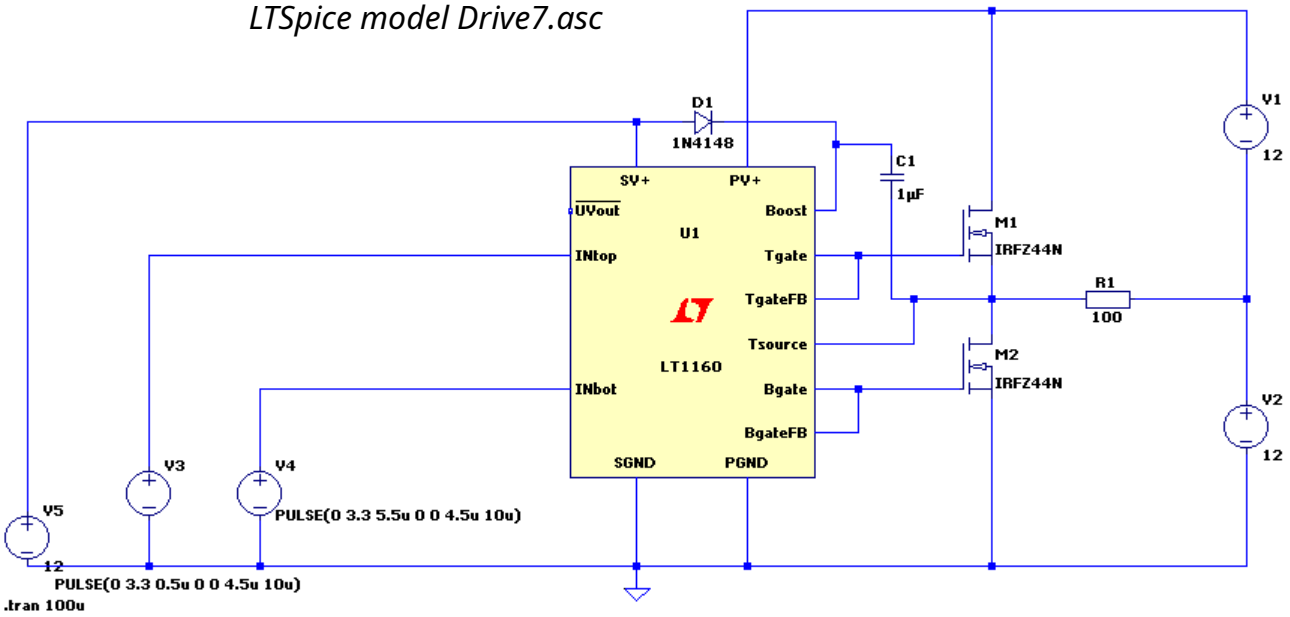
This circuit is available in the LTSpice model Drive6.asc



Circuit 6 derives the signal for the upper transistor from the lower signal. Draw up a table showing the on/off state for all transistors in the circuit when the input is high and low.
Plot the drain current of M2 – why is it showing such huge peaks?

Circuit 7

This circuit is available in the LTSpice model Drive7.asc



Circuit 7 is a commercial high/low side gate driver. Compare its performance with circuit 6 in the following areas:

shoot-through (better? If so how is this achieved)
input – output delay for rising and falling edges.

Additional task: Identify a high/low gate drive IC such as the one in Circuit 7 which also includes over current protection.