# Comp Arch HW #4

② In order for state 1, state 10, and state 0 The control values for this new state are PCWrite, PCSource=10, RegDst=10, MemtoReg=10, and RegWrite, A new state 10 is added from state 1. RegDst and MemtoReg corresponding values in the other state need to change as well to reflect this enhancement, because RegDst and MemtoReg are now 2 bits. We see the changes in fig. A3.2 using graded Work C. by what we got in part(b), it will take 3 cycles to do the jal instruction (State 0, State 1, state 10, state 0)

③ In order to take RS as an input, Mux into Write register port of Register file needs to expand, it needs to expand into 2 more inputs - from register A and from register B. The state diagram should also have 2 more states - Write A from RT field and to write B into Rs field.

~~You need to perform~~ you need to do it 2 times to swap the registers - it's very similar to the write back state of R-type instructions. all of this will take 4 cycles to finish.

⑨ just branch

④ In the Fetch stage, it would affect ~~all of the instructions~~ the PC+4 so therefore it would affect all of the instructions.

PC+4 moves it to mux-0 to PC-source=00, which makes the PC+4 go to the PC and the PCWrite Makes the PC move PC+4

① ~~Even~~ ALUOP = 010 you can assumes does addition.

In order for us to read whats in the register rs, we need to connect the intermediate register B to the memory unit. To do the addition with register rs. we also need to feed MDR (which will have Mem(rt)) into the ALU.