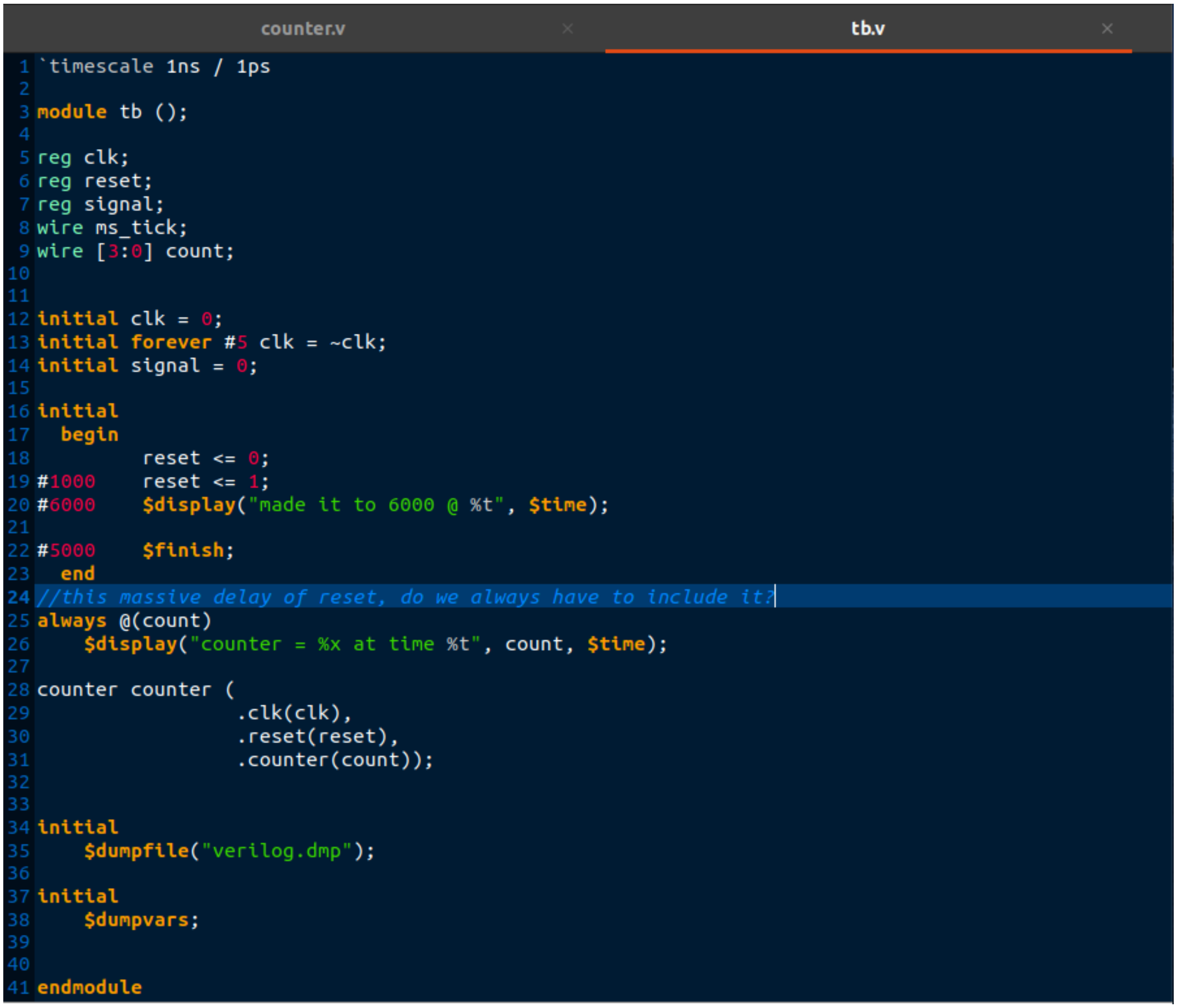
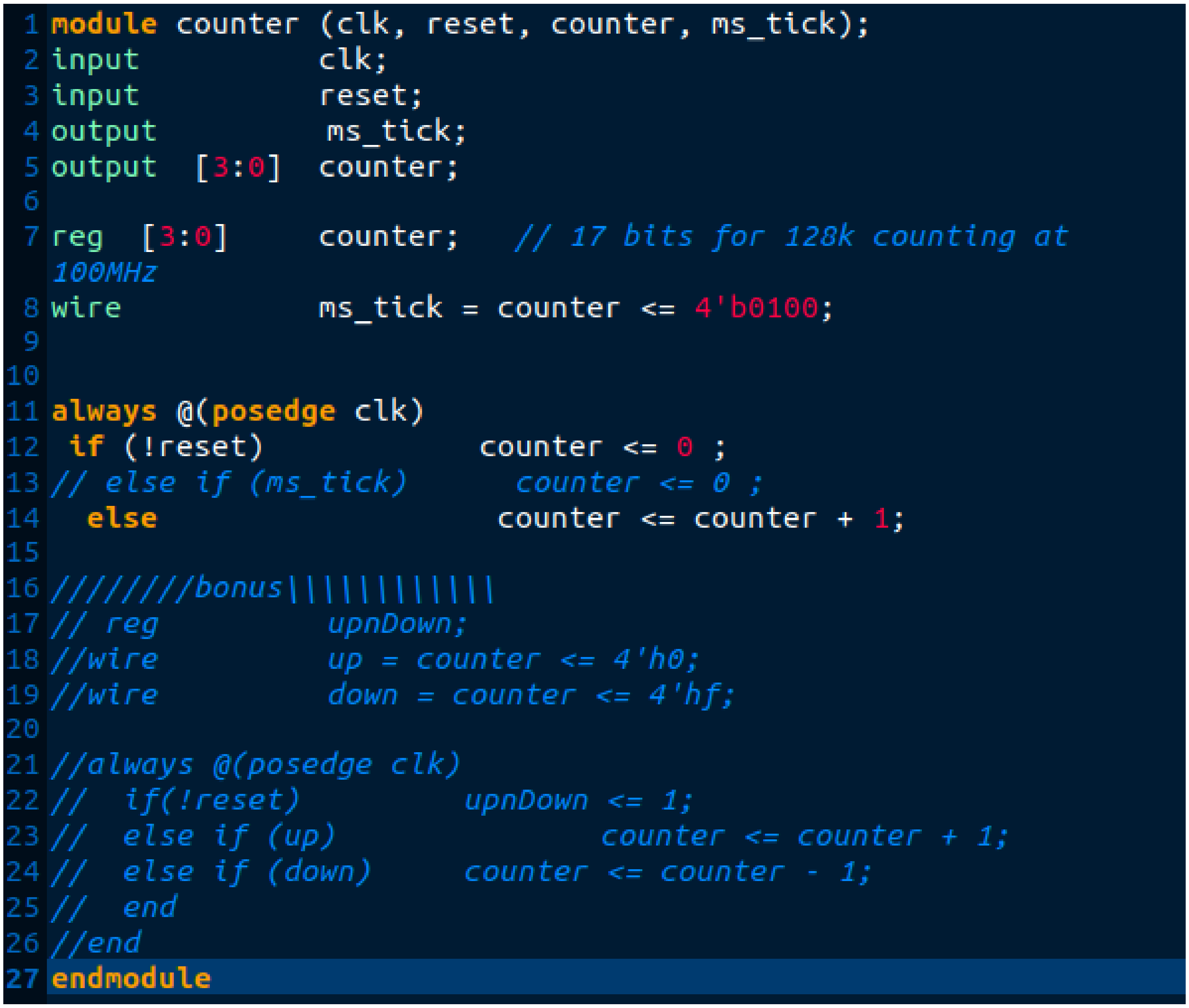
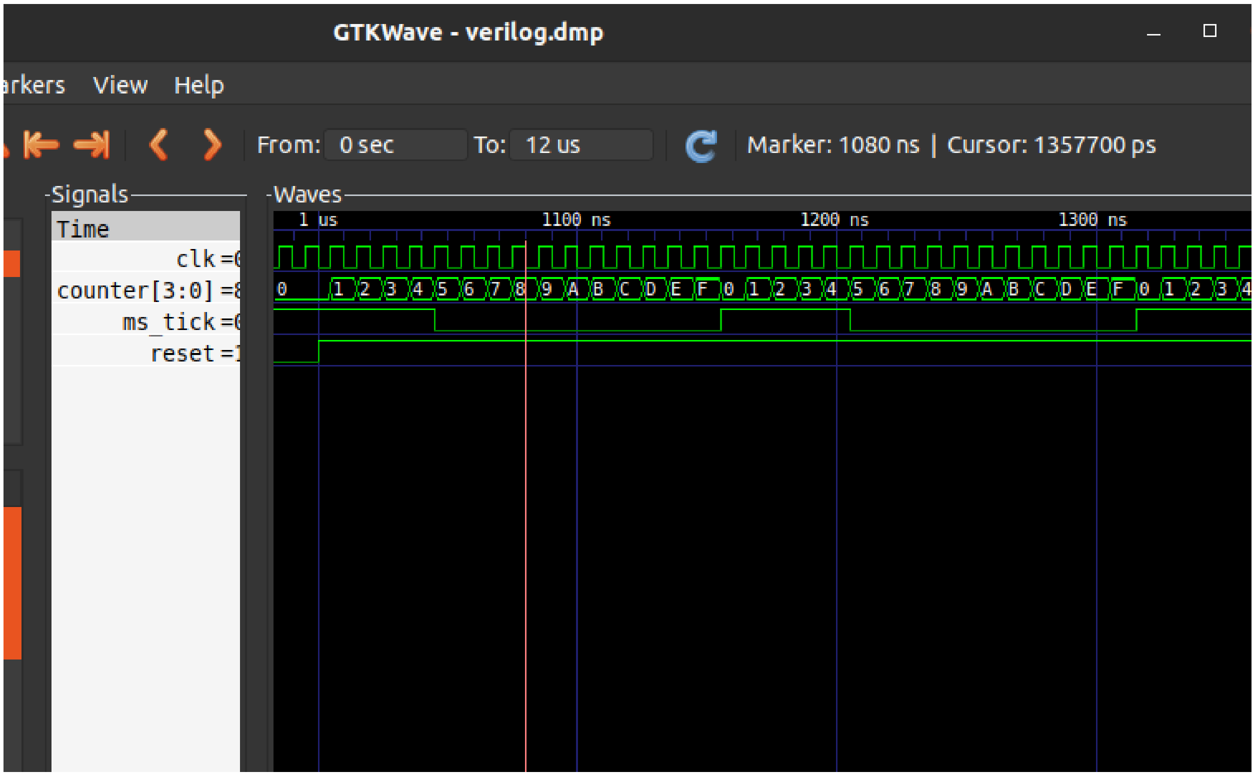


```verilog
`timescale 1ns / 1ps

module tb ();

reg clk;
reg reset;
reg signal;
wire ms_tick;
wire [3:0] count;


initial clk = 0;
initial forever #5 clk = ~clk;
initial signal = 0;

initial
  begin
         reset <= 0;
#1000    reset <= 1;
#6000    $display("made it to 6000 @ %t", $time);

#5000    $finish;
  end
//this massive delay of reset, do we always have to include it?
always @(count)
    $display("counter = %x at time %t", count, $time);

counter counter (
                 .clk(clk),
                 .reset(reset),
                 .counter(count));


initial
    $dumpfile("verilog.dmp");

initial
    $dumpvars;


endmodule
```



```
module counter (clk, reset, counter, ms_tick);
input          clk;
input          reset;
output         ms_tick;
output  [3:0]  counter;

reg  [3:0]     counter;   // 17 bits for 128k counting at 100MHz
wire           ms_tick = counter <= 4'b0100;


always @(posedge clk)
 if (!reset)            counter <= 0 ;
// else if (ms_tick)      counter <= 0 ;
  else                   counter <= counter + 1;

////////bonus\\\\\\\\\\\\
// reg         upnDown;
//wire         up = counter <= 4'h0;
//wire         down = counter <= 4'hf;

//always @(posedge clk)
//  if(!reset)         upnDown <= 1;
//  else if (up)               counter <= counter + 1;
//  else if (down)     counter <= counter - 1;
//  end
//end
endmodule
```



GTKWave - verilog.dmp

From: 0 sec To: 12 us

Marker: 1080 ns | Cursor: 1357700 ps

Signals

```
Time
         clk =0
counter[3:0] =8
     ms_tick =0
       reset =1
```

arkers
View
Help
Waves
1 us
1100 ns
1200 ns
1300 ns
0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4