Product Specification

(Preliminary)

Part Name	:	OEL Display Module
Customer Part ID	:	
WiseChip Part ID	:	UT-2896KSWGG01
Doc No.	:	SAS1-0H021-A

Customer:
Approved by

From: WiseChip Semiconductor Inc.
Approved by

WiseChip Semiconductor Inc.

8, Kebei RD 2, Science Park, Chu-Nan, Taiwan 350, R.O.C.

Notes:

1. Please contact WiseChip Semiconductor Inc. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.
3. All of WiseChip product compliance with below :
   a. Directive of European RoHS (2011/65/EU) and latest directive (EU) 2015/863.
   b. Directive of Packaging and Packaging Waste, 94/62/EC.
   c. Halogen Free, (IEC 61249-2-21).

Revised History

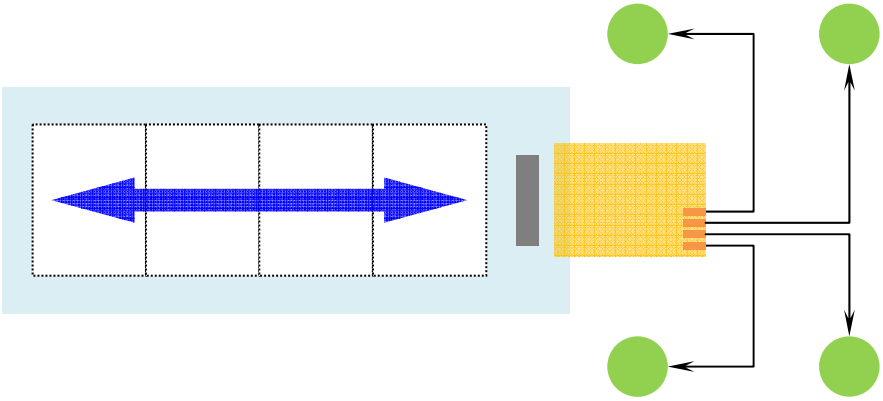
Part Number	Revision	Revision Content	Revised on
UT-2896KSWGG01	A	New	August 03, 2020

Contents

1. Basic Specifications

1.1 Display / Touch Specifications

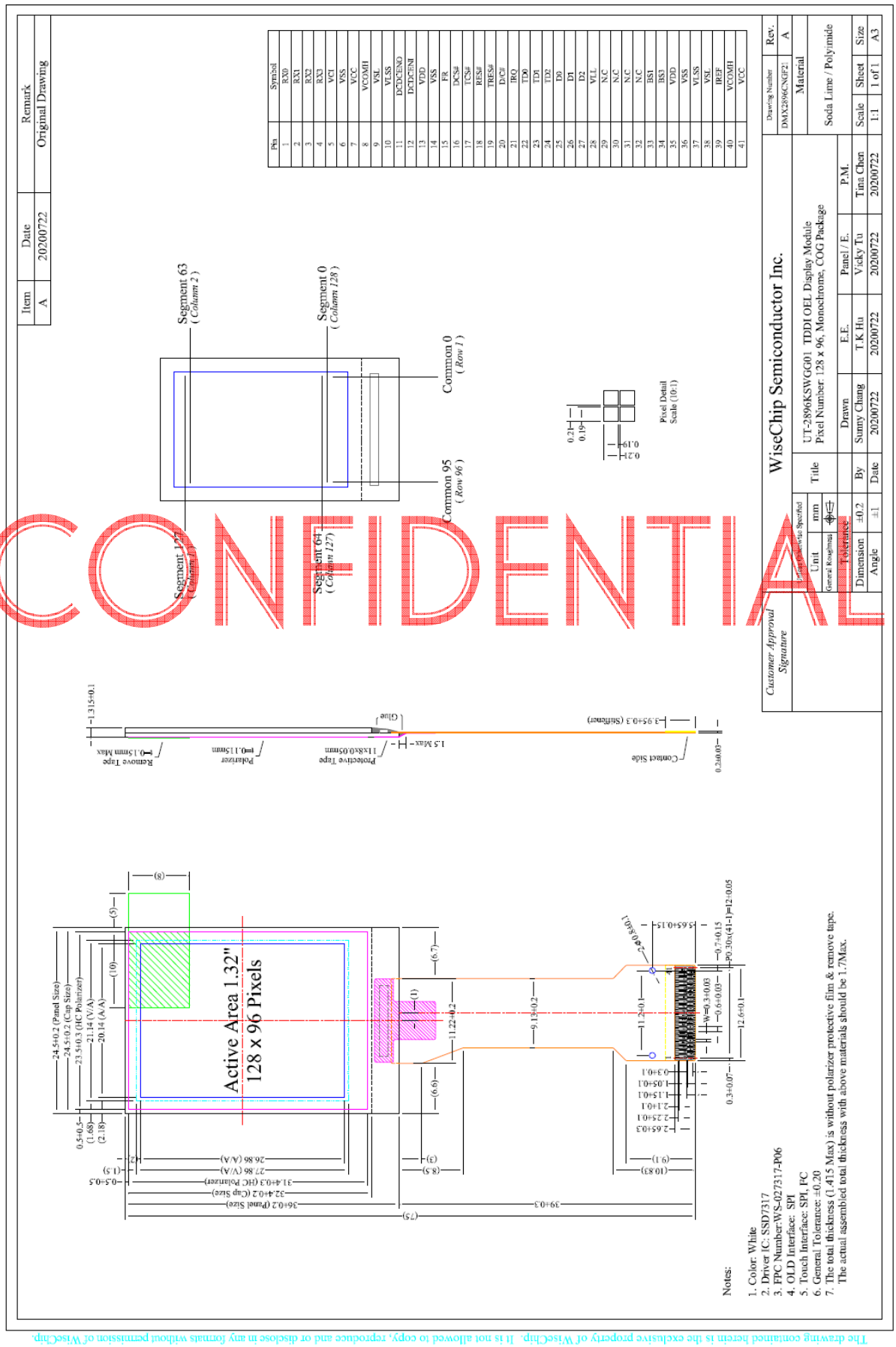
1) Display Mode : Passive Matrix
2) Display Color : Monochrome (White)
3) Drive Duty : 1/96 Duty
4) Touch Mode : 4 In-Cell Keys with 1D Slide + 4 Outside Keys



1.2 Mechanical Specifications

1) Outline Drawing : According to the annexed outline drawing
2) Number of Pixels : 128 × 96
3) Module Size : 24.50 × 75.00 × 1.40 (mm)
4) Panel Size : 14.00 × 28.00 × 1.40 (mm) including "Anti-Glare Polarizer"
5) Active Area : 10.86 × 21.74 (mm)
6) Pixel Pitch : 0.17 × 0.17 (mm)
7) Pixel Size : 0.15 × 0.15 (mm)
8) Weight : T.B.D. (g) ± 10%

1.3 Mechanical Drawing



1.4 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
13, 35	VDD	P	**Power Supply for Core Logic** This is a voltage supply pin. It must be connected to external source. * The ripple noise on this pin should be suppressed within 100mV.
5	VCI	P	**Power Supply for Touch Analog Driving** This is a voltage supply pin. It must be connected to external source & always be equal to or higher than V_{DD}. Do not share the power with other ICs especially those generating high frequency signals. ensure a clean power. * The ripple noise on this pin should be suppressed within 100mV.
6, 14, 36	VSS	P	**Ground of Logic Circuit** This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
7, 41	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. It must be supplied externally. * The ripple noise on this pin should be suppressed within 200mV in touch period.
10, 37	VLSS	P	**Ground of Analog Circuit** This is the analog ground pin. They should be connected to V_{SS} externally.
Driver			
39	IREF	P	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and GND. Set the current at 18.75μA maximum.
8, 40	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is for the voltage output high level for COM signals. A capacitor should be connected between this pin and GND.
9, 38	VSL	P	**Voltage Output Low Level for SEG Signal** This is segment voltage reference pin. When external V_{SL} is not used, this pin should be left open. When external V_{SL} is used, this pin should connect with resistor and diode to ground.
External IC Communication			
12	DCDCENI	I	**Enable Input Pin for External DC/DC Circuit Control** It could connect to V_{DD} to enable external DC/DC circuit control function. It must be connected to external ground if it is not used.
11	DCDCENO	O	**Enable Output Pin for External DC/DC Circuit** It is used as the external DC/DC circuit enabled/disabled control for low power mode (LPM) application. It should be left open if it is not used.
15	FR	O	**Frame Frequency Triggering Signal** This pin will send out RAM write synchronization signal that could be used to identify the driver status. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be left open if it is not used.
Interface			
33 34	BS1 BS3	I	**Communicating Protocol Select** These pins are MCU interface selection input. See the following table: BS3 / BS1 / Display / Touch 0 / 0 / 4-wire SPI / SPI 0 / 1 / I^2C / SPI 1 / 0 / 4-wire SPI / I^2C 1 / 1 / I^2C / I^2C
18	RES#	I	**Power Reset for Controller and Driver** This pin is master reset signal input. When the pin is low, initialization of the chip is executed.
16	DCS#	I	**Chip Select for Display Interface** This pin is the chip select input for display interface. The display is enabled for MCU communication only when CS# is pulled low.

1.4 Pin Definition

Pin Number	Symbol	I/O	Function
Interface (Continued)			
20	D/C#	I	**Data/Command Control** When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
25~27	D0~D2	I/O	**Serial Data Input/Output and clock for Display** When serial interface mode is selected, D2, D1 should be tied together and serves as serial data input: SDIN and D0 is the serial clock input: SCLK; When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
19	TRES#	I	**Power Reset for Controller and Driver for Touch Interface** This pin is reset signal input of touch interface. When the pin is low, initialization of the chip is executed.
17	TCS#	I	**Chip Select for Touch Interface** This pin is the chip select input for touch interface. The touch is enabled for MCU communication only when TCS# is pulled low.
22~24	TD0~TD2	I/O	**Serial Data Input/Output and clock for Touch Interface** When serial interface mode is selected, TD2 serves as serial data output: SDOUT, TD1 serves as serial data input: SDIN and TD0 is the serial clock input: SCLK; When I2C mode is selected, TD2, TD1 should be tied together and serve as SDAout, SDAin in application and TD0 is the serial clock input, SCL.
21	IRQ	O	**Interrupt Signal** This pin is interrupt signal for touch reporting.
Outside Touch Keys			
1 2 3 4	RX0 RX1 RX2 RX3	-	**Reserved Pin for "1D Slide + 4 Outside Keys" Application** It should be left open if it is not used.
Reserve			
28	VLL	-	**Reserved Pin** Logic low (same voltage level as VSS) for internal connection of input and I/O pins. No need to connect to external ground. This pin should be kept NC.
29, 32	N.C.	-	**Reserved Pin** This is dummy pin. Do not group or short NC pins together. It must be floated.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4.0	V	1, 2
Supply Voltage for Touch driving	V_{CI}	-0.3	4.0	V	1, 2
Supply Voltage for Display	V_{CC}	0	15.0	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (150 cd/m^2)		7,500	-	hour	4

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 4	120	150	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = V_{CI} =3.3V, V_{CC} = 12.0V.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	3.3	3.5	V
Supply Voltage for Touch	V_{CI}		3.0	3.3	3.5	V
Supply Voltage for Display	V_{CC}	Note 5	11.5	12.0	12.5	V
High Level Input	V_{IH}		0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
Operating Current for V_{DD}+V_{CI}	I_{DD_CI}		-	1.6	2.4	mA
Operating Current for V_{CC}	I_{CC}	Note 6	-	6.3	7.9	mA
		Note 7	-	12.1	15.1	mA
		Note 8	-	18.5	23.1	mA
Sleep Mode Current for V_{DD}+V_{CI}	$I_{DD\_CI, SLEEP}$		-	35	55	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 6: V_{DD} = V_{CI} =3.3V, V_{CC} = 12.0V, 30% Display Area Turn on.
Note 7: V_{DD} = V_{CI} =3.3V, V_{CC} = 12.0V, 50% Display Area Turn on.
Note 8: V_{DD} = V_{CI} =3.3V, V_{CC} = 12.0V, 100% Display Area Turn on.

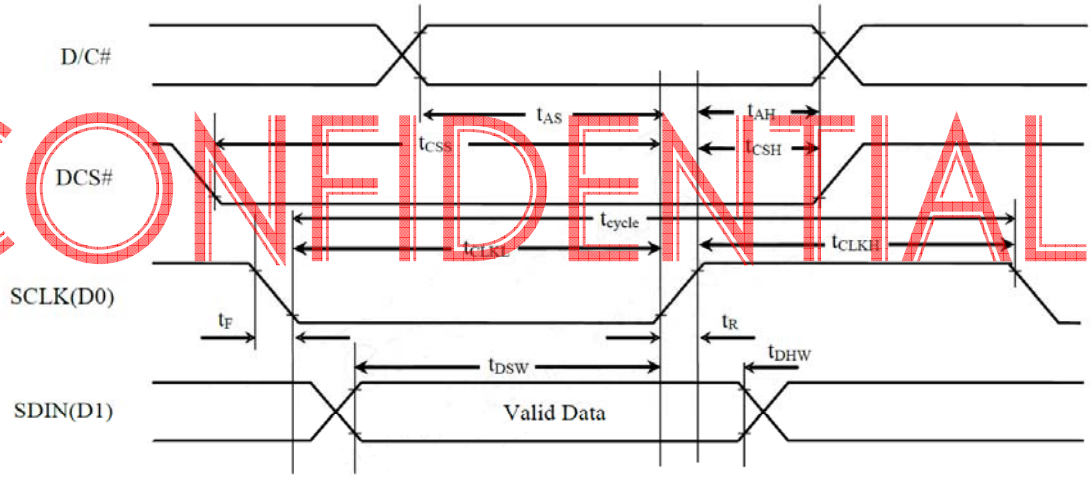
* Software configuration follows Section 4.5 Initialization.

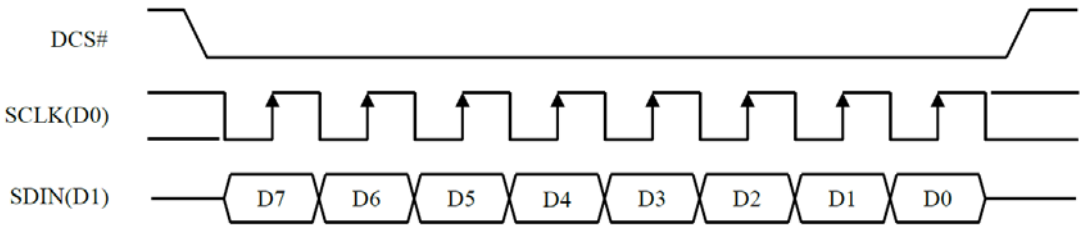
3.2 AC Characteristics

3.3.1 4-wire SPI Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	20	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	25	-	ns
t_{CLKL}	Clock Low Time	30	-	ns
t_{CLKH}	Clock High Time	30	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 1.65V to 3.5V, T_a = 25°C)

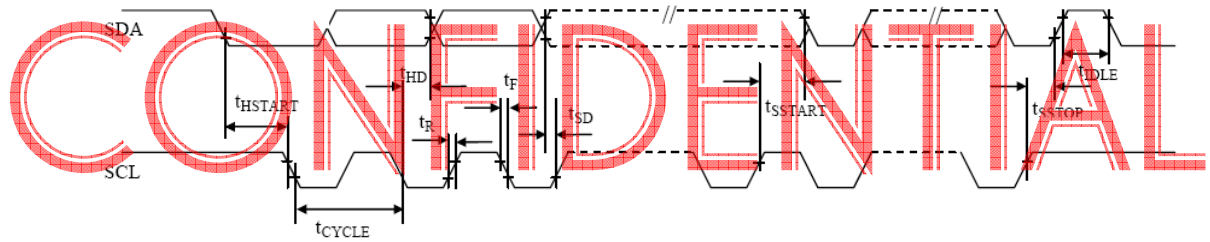




3.3.2 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* (V_{DD} - V_{SS} = 1.65V to 3.5V, T_a = 25°C)



4. Functional Specification

4.1 Commands

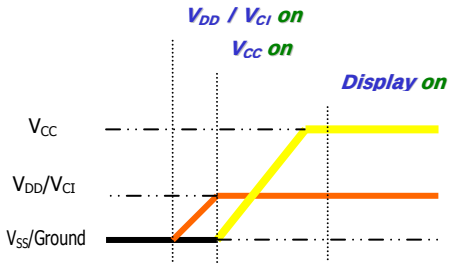
Refer to the Technical Manual for the SSD7317

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

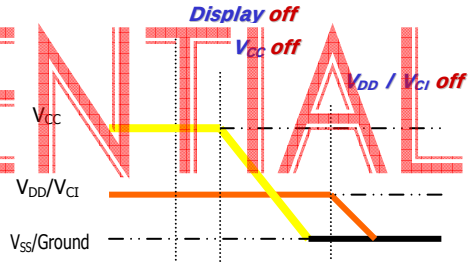
4.2.1 Power up Sequence:

1. Power up V_{DD} / V_{CI}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD} / V_{CI}



Note 9:

1) Since an ESD protection circuit is connected between V_{DD}, V_{CI} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{CI} are ON and V_{CC} is OFF.
2) V_{CC} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CI} , V_{CC}) can never be pulled to ground under any circumstance.
4) V_{DD}, V_{CI} should not be power down before V_{CC} power down.

4.3 Reset Circuit

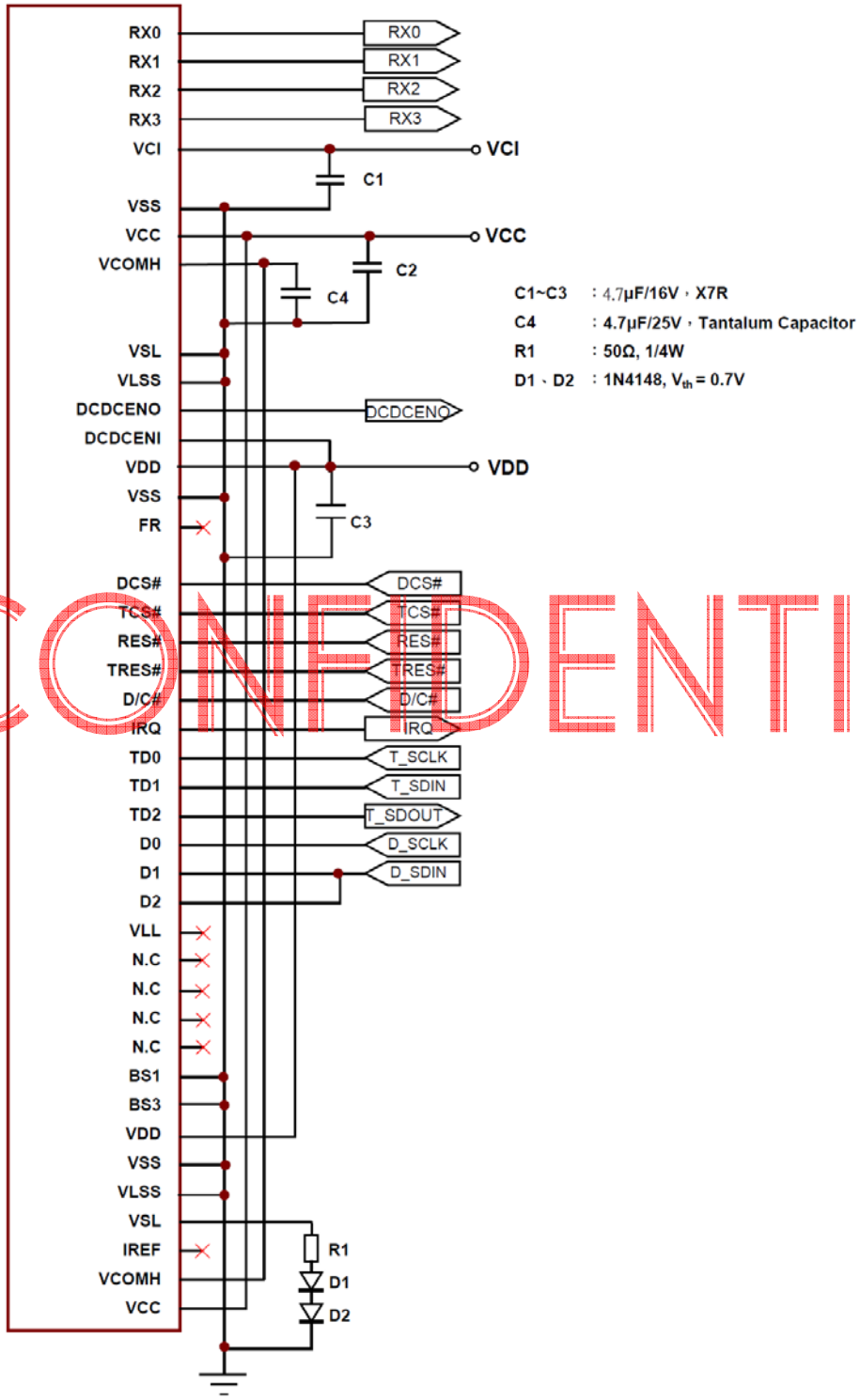
When RES# input is low, the chip is initialized with the following status:

1. Display is OFF.
2. 128×96 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to address 00h and COM0 mapped to address 00h).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM address 0.
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

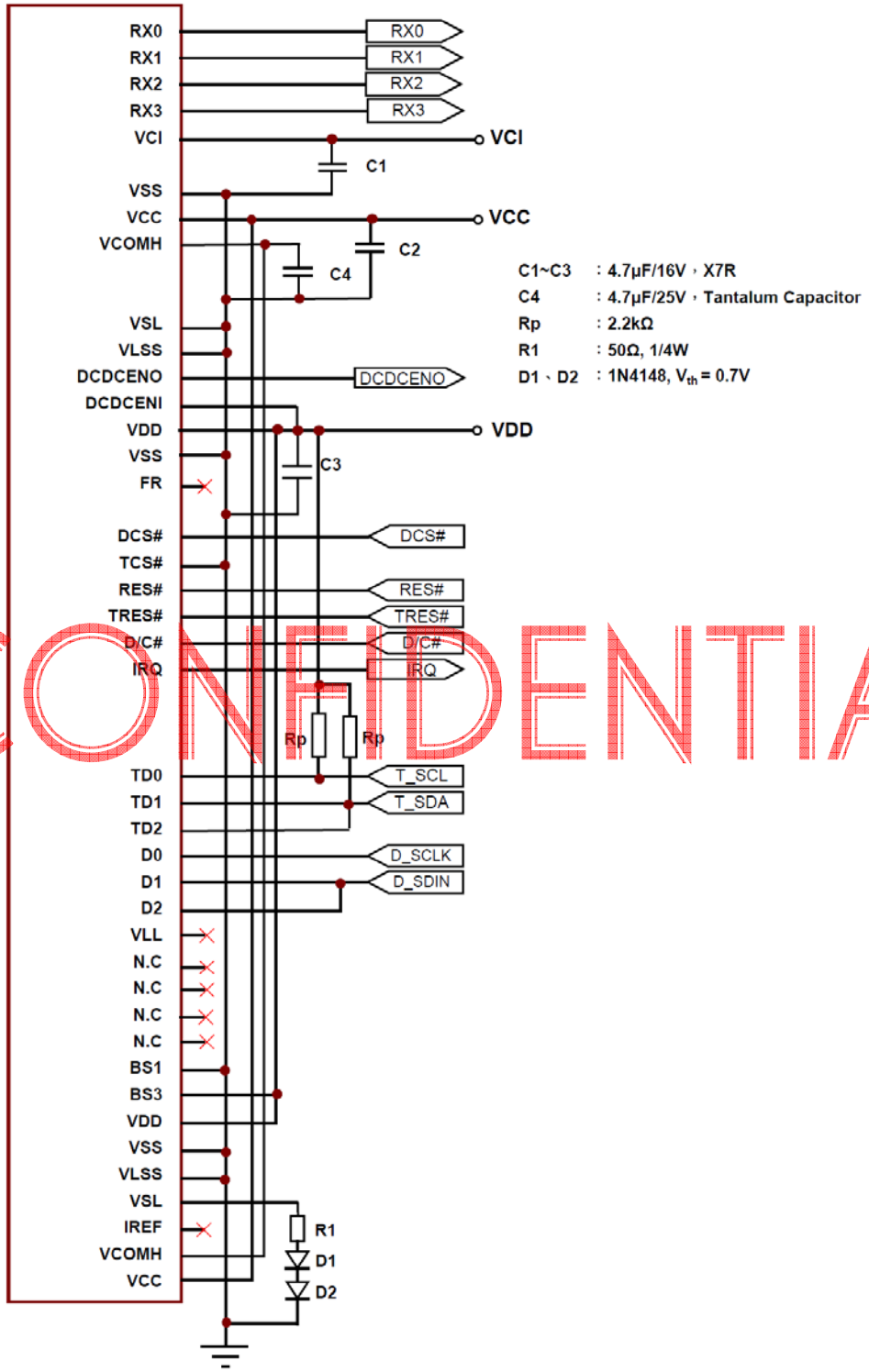
Touch initialization and firmware should be sent again after reset.

4.4 Application Circuit

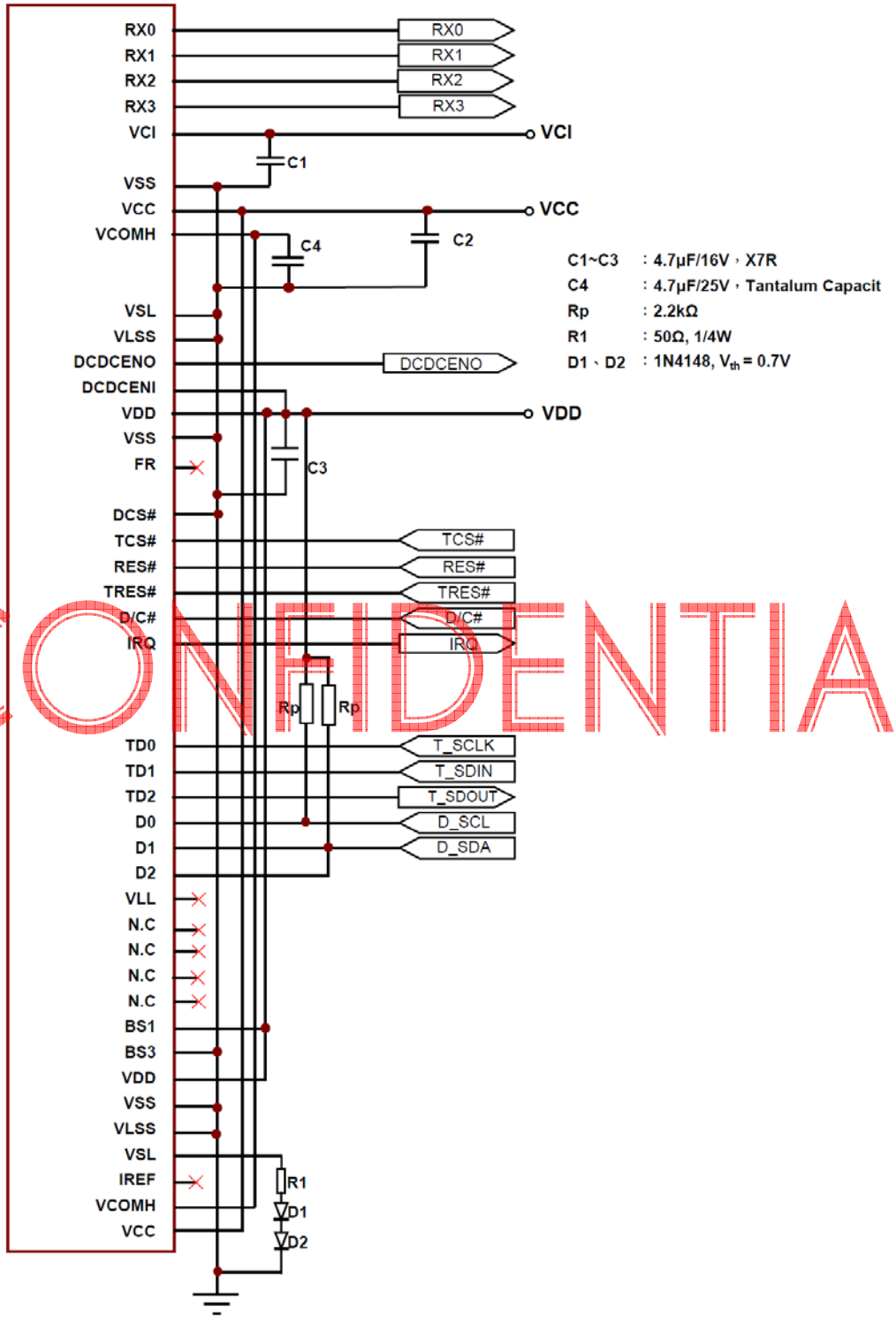
4.4.1 Display by 4-wire SPI Interface + Touch by SPI Interface (1D Slide + 4 Outside Keys)



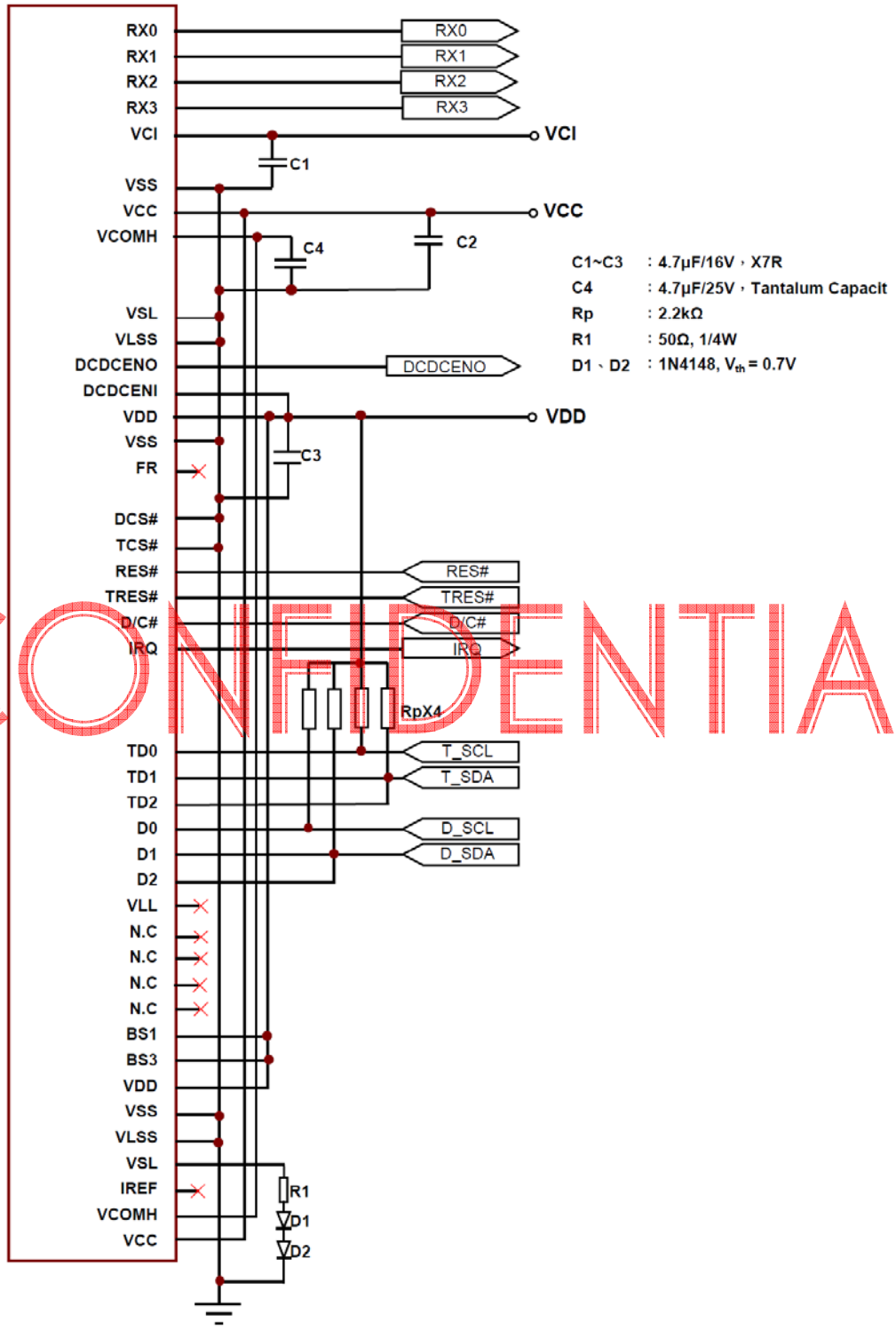
4.4.2 Display by 4-wire SPI Interface + Touch by I^2C Interface (1D Slide + 4 Outside Keys)



4.4.3 Display by I²C Interface + Touch by SPI Interface (1D Slide + 4 Outside Keys)



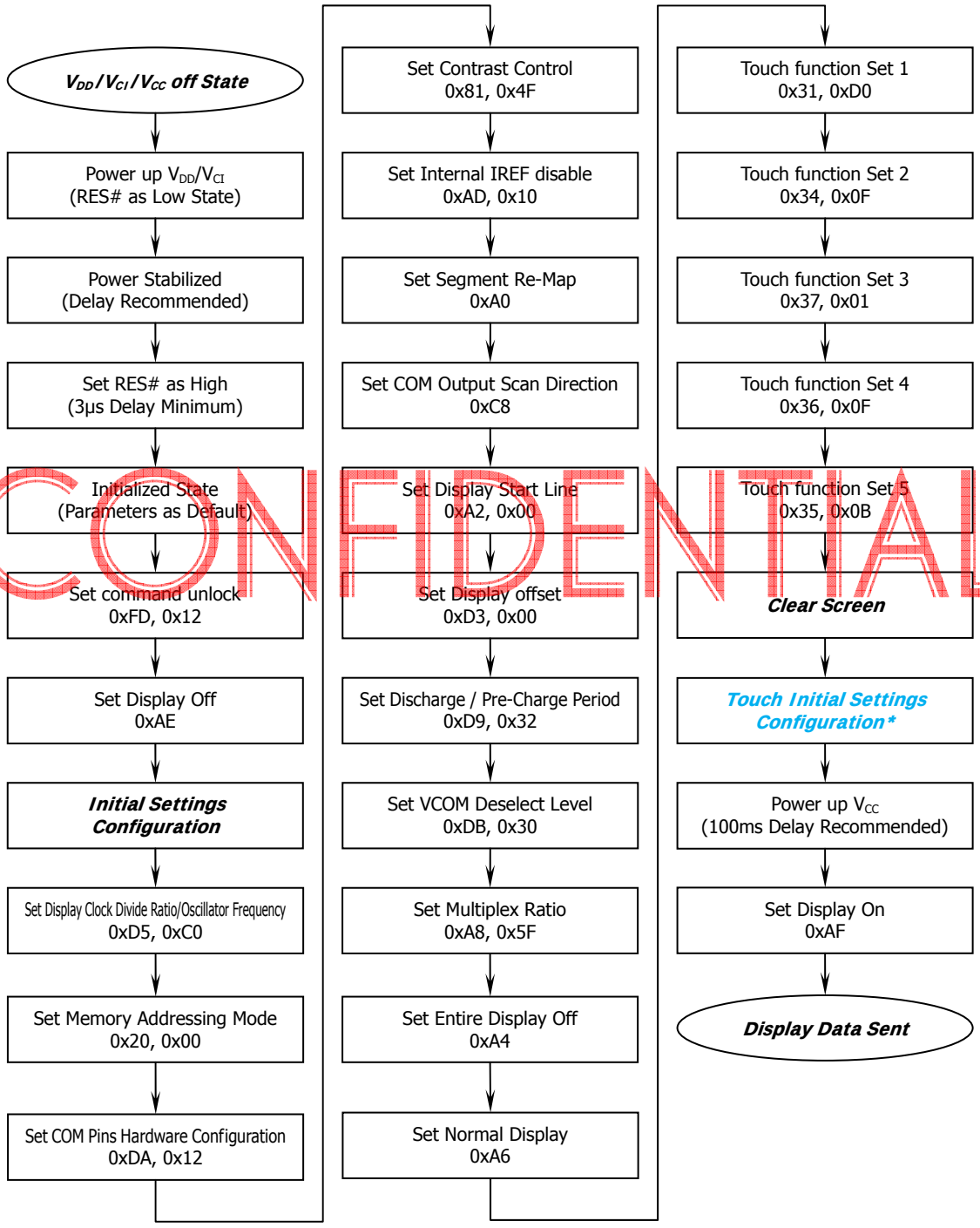
4.4.4 Display by I²C Interface + Touch by I²C Interface (1D Slide + 4 Outside Keys)



4.5 Actual Application Example

Command usage and explanation of an actual example

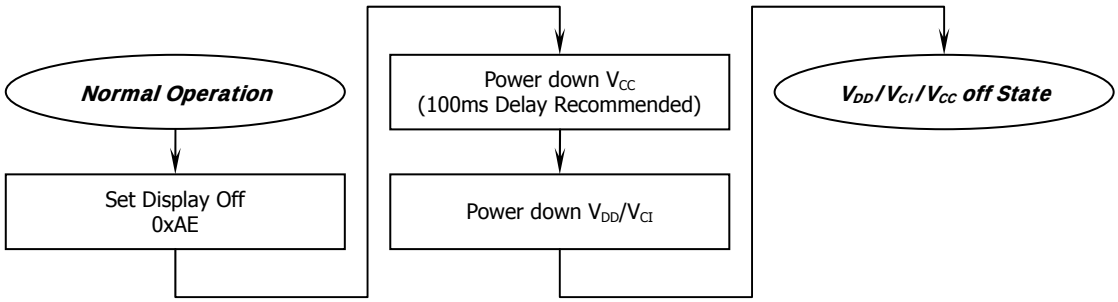
<Power up Sequence>



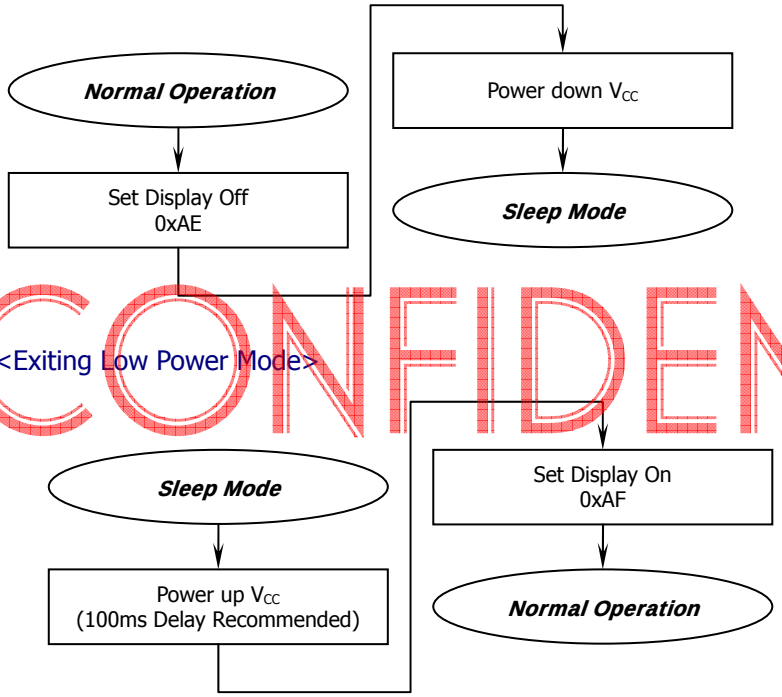
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

- Touch Initial Settings Configuration refer to sample code.

<Power down Sequence>



<Entering Low Power Mode>

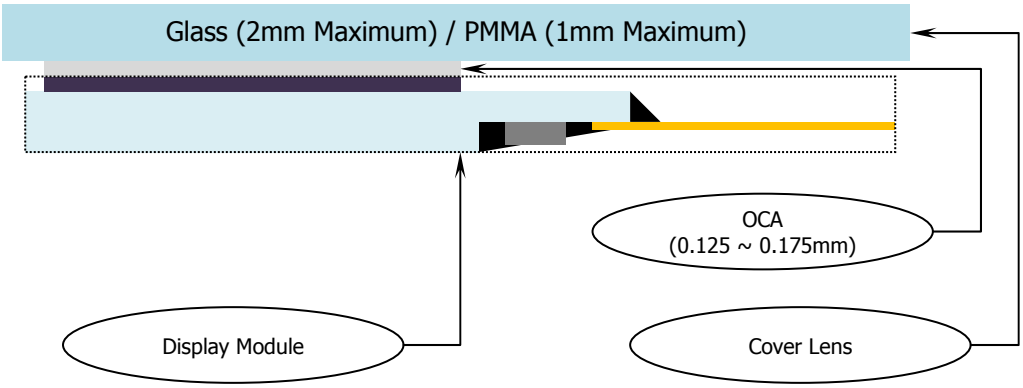


<Exiting Low Power Mode>

4.6 Module Stacks Guideline

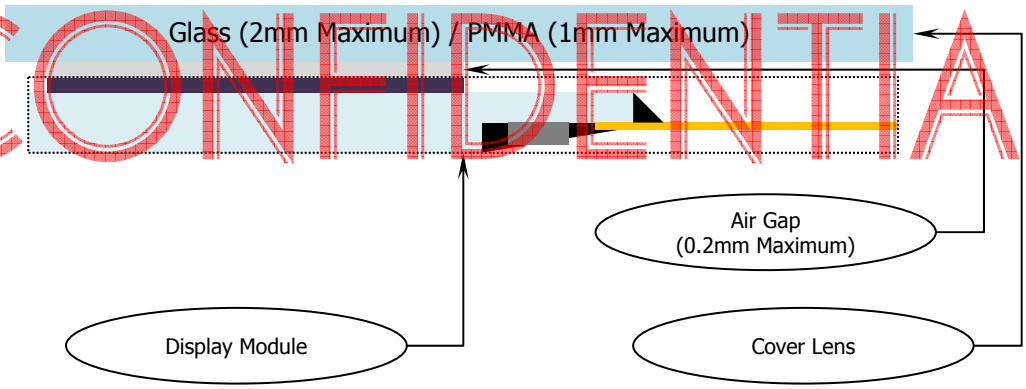
4.6.1 Stacking by Optical Bonding (Recommendation)

Please contact WiseChip if it is considering to have thicker cover lens.



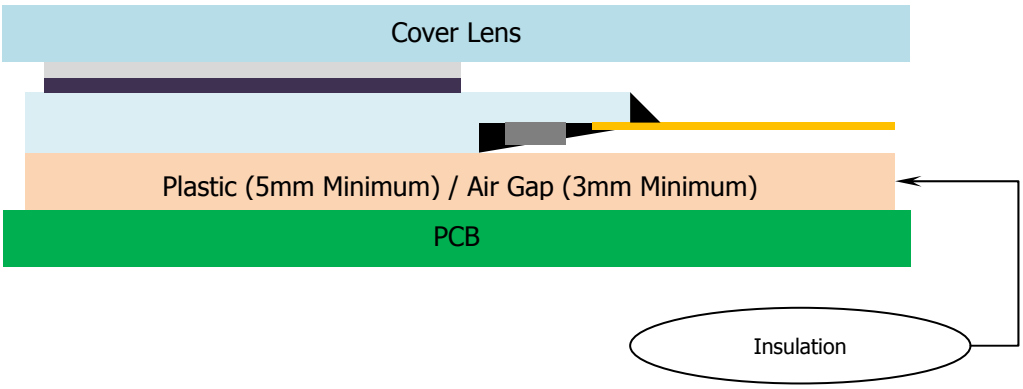
4.6.2 Stacking by Air Bonding

Please do not have thicker cover lens.



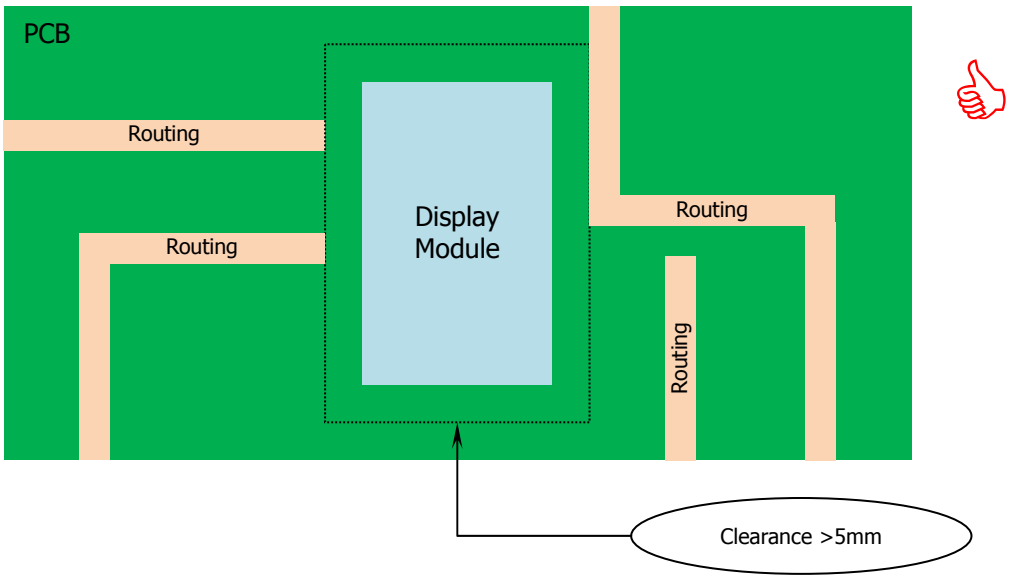
4.6.3 Module Stacks (Recommendation)

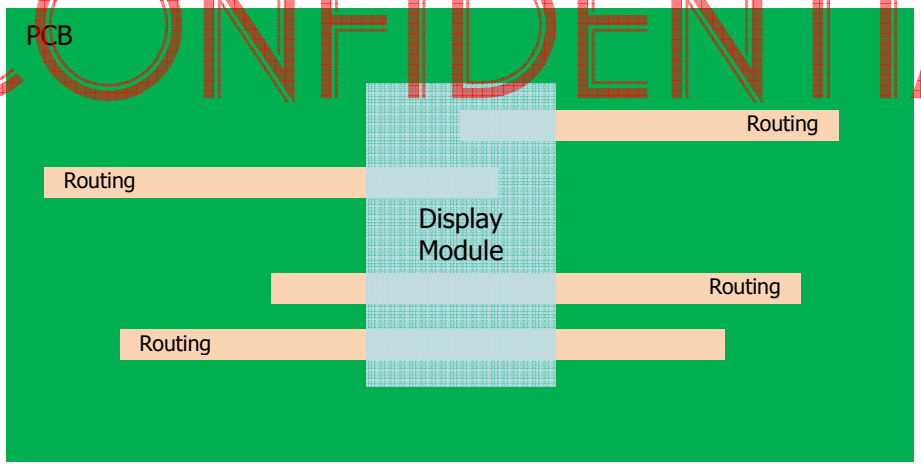
It is recommended to place a fixed non-conductive insulation plane, such as plastic or air gap, under the display and in-between PCB.

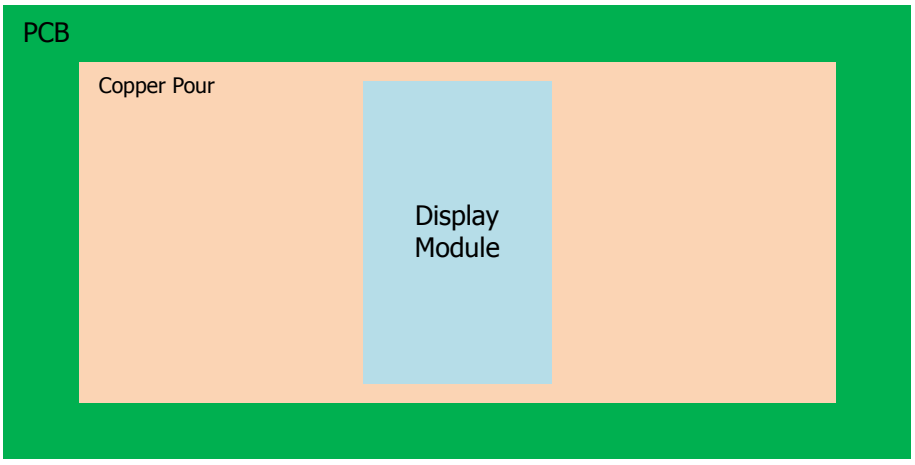


4.6.4 Module Stacks on PCB without Insulation

If the module is directly placing on the PCB, there cannot be a conductive material under module. Please make sure there is no copper pour plane or metal trace under module.







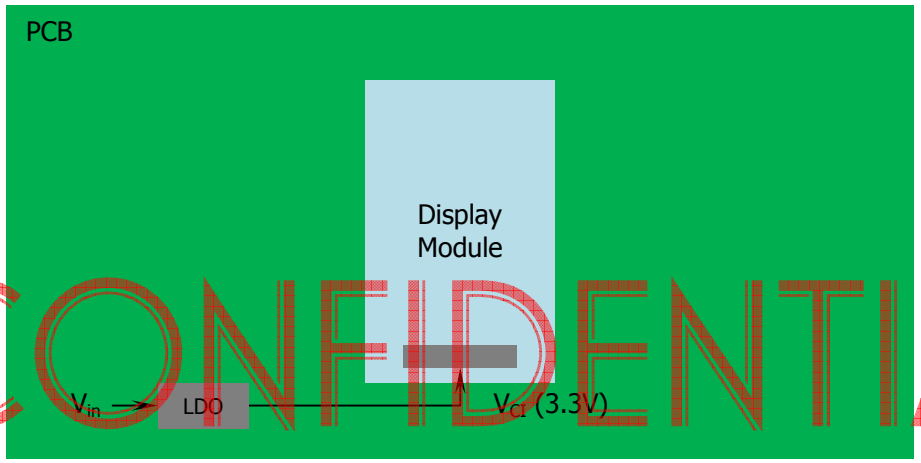
4.7 Power Supply Guideline

4.7.1 Power Ripple Noise Suppression

Power	Ripple (Peak to Peak)	Notes
V_{DD}	≤ 100mV	
V_{CI}	≤ 100mV	
V_{CC}	≤ 200mV	In Touch Period

4.7.2 V_{CI} Supply

Do not share the power of V_{CI} with other ICs especially the high frequency signals. Please ensure a clean power input to V_{CI}. For example, using low dropout regulator (LDO) for power step down instead of DC/DC switching regulator.



5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	60°C, 240 hrs	The operational functions work.
Low Temperature Operation	-20°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

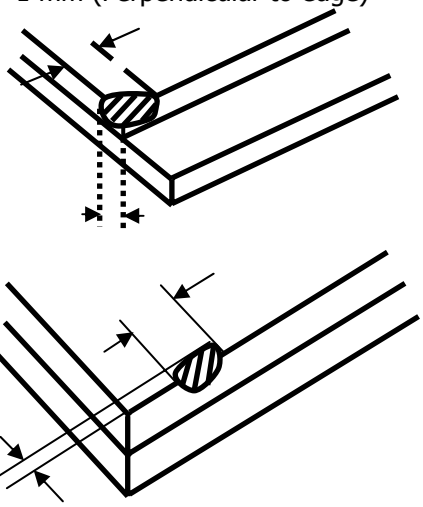
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

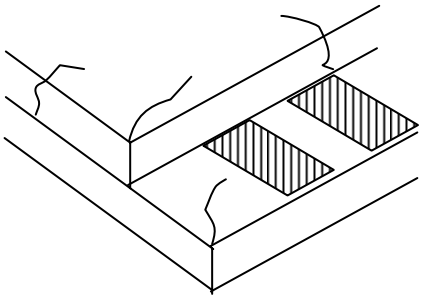
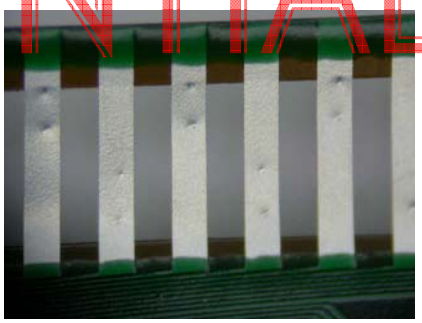
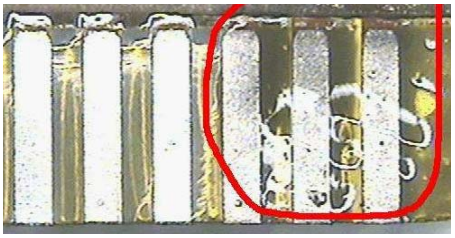
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

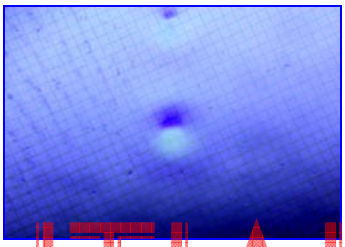
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 3 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

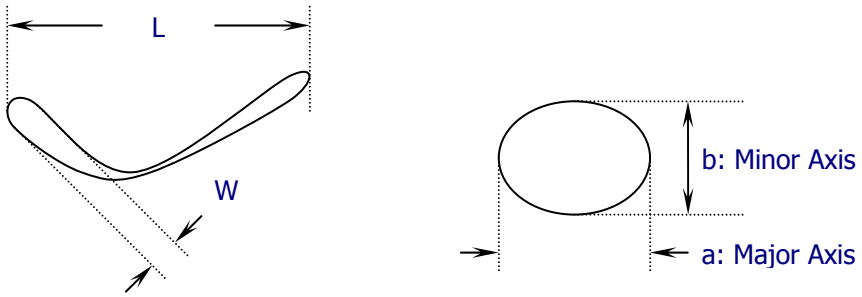
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

6.3.2 Cosmetic Check (Display Off) in Active Area

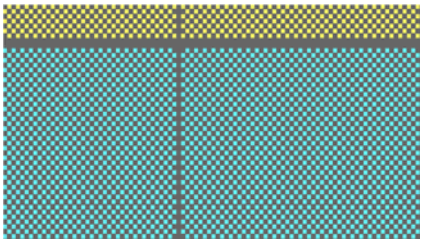
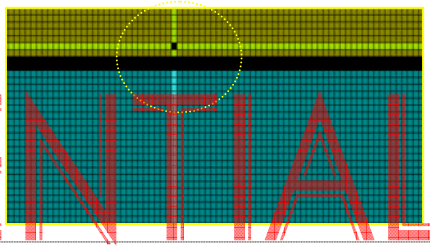
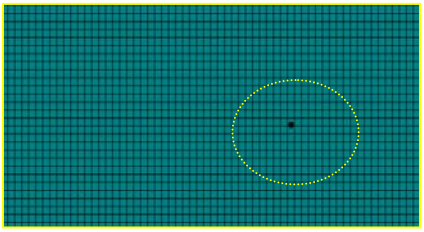
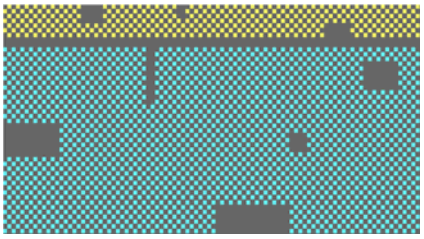
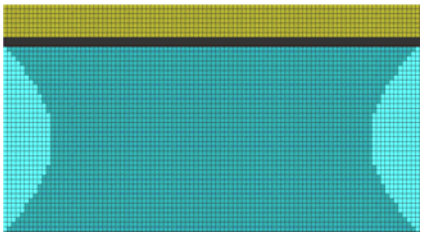
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Spot-Shape Defect (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

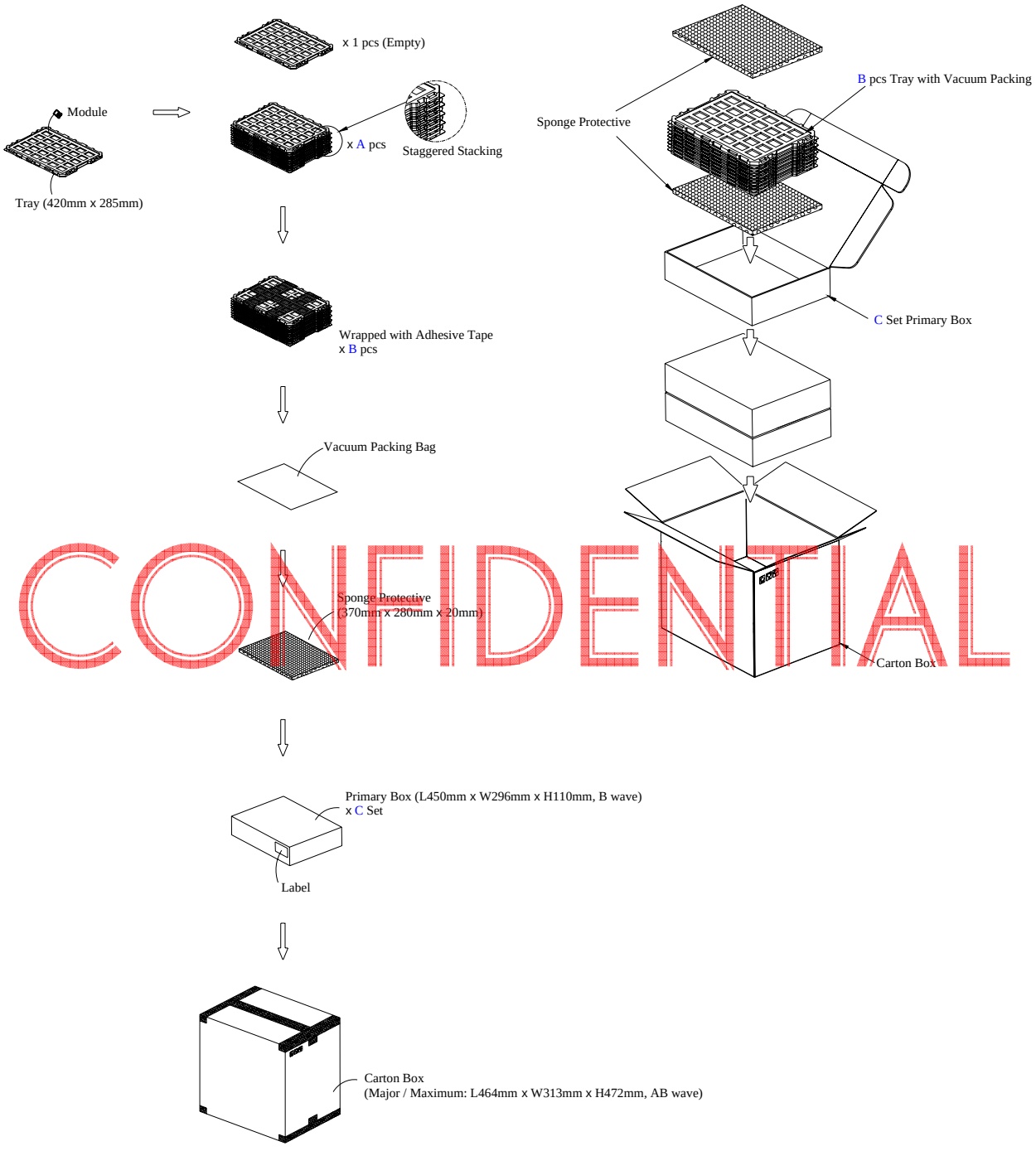
* Protective film should not be tear off when cosmetic check.
* Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



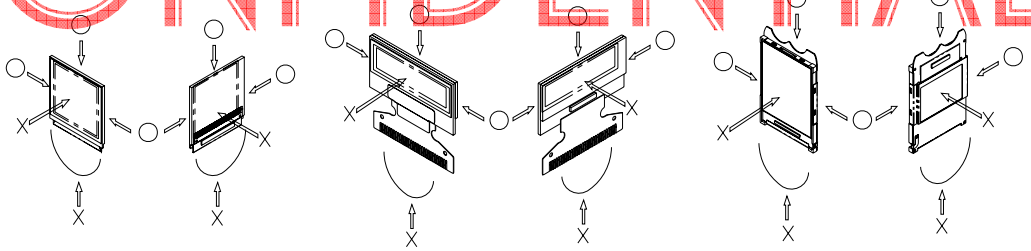
Item		Quantity	
Module		**2400**	**per Primary Box**
Holding Trays	**(A)**	**20**	**per Primary Box**
Total Trays	**(B)**	**21**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol.
   Also, pay attention that the following liquid and solvent may spoil the surface becoming cloudy without proper handling:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure

to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from WiseChip Semiconductor Inc.)
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD7317
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

Warranty:

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. WiseChip Semiconductor Inc. shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

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