This document include explanations for HW3 and prepared according to the HW3 pdf.

You need to compress your hw3 project before the submission, this is named qar file (StudentNumber.qar), How to do it is in the PS folder.

For report part,
You need to write a testbench module and show testbench results for each module with SS (like and32, or32, etc.). For MULT32 part you need to try 2 different numbers in test case (x1*x2 and x3*x4). For ALU32 part you need to try 2 different numbers for all operations in ALU (Select:000 x1+x2 result= , …, Select=111 x1|x2 resut=…, Select:000 x3+x4 result= , …, Select=111 x3|x4 resut=…,)

For MUL32 in this report, you need to add first three design states (1. State diagram 2. State table 3. Boolean expressions)

Multiplication part for HW3, this is about Control part:
1. State diagram
2. State table
3. Boolean expressions
4. Verilog implementation (control.v)
5. Simulation results

Control part, generate signals that are shift right, write, reset, checking32bit (you can choose another name).

You will design a FSM controller in Verilog but without using all capabilities of Verilog. Actually, you will first draw the state diagram and derive the state table and derive the Boolean expressions. Only after then you will implement the Boolean expressions through Verilog.

You cannot use behavioral Verilog. You will use “always@” only for register definition in multiplier control part.

ALU part for HW3:

You can use 4-bit adder in PS folder. You can use only “for” keyword to obtain and,or,xor,nor,not gates. This is just example:

```
for(i=0; i< 32;     i=i+1)
    not modulename (inp[i], outp[i]);
```
