



High performance RISC CPU

ÿ Only 35 instructions need to be learned
ÿ All instructions are single cycle (except branch jumps)
ÿ Storage architecture
ÿ Program ROM: 3k x 14bits
ÿ Data RAM: 256 x 8bits ÿ Data EEPROM: 128 x 8bits
ÿ 8-layer hardware stack
ÿ Optional instruction cycle: 2T/4T
ÿ 125ns @ 2T, 16MHz, VDDÿ2.7V

Special microcontroller characteristics

ÿ Operating temperature range: -40ÿ~85ÿ
ÿ Wide operating voltage range: 1.9V~5.5V
ÿ Clock source
Two internal clocks
13.5M/16M high-speed and high-precision HIRC
i. Support software fine-tuning, 2.5‰ per step
32k low-speed and low-power LIRC
Crystal oscillator and external clock input
Crystal clock missing detection
Two-speed clock startup under crystal clock configuration
ÿ Slow clock cycle measurement
ÿ With 7-bit preset Divided 16-bit watchdog, the clock source can be selected
Select ÿ Power-on reset delay counter
ÿ Low power mode SLEEP
The system clock can choose to keep running or shut down
ÿ Low voltage reset LVR:
2.0V/2.2V/2.5V/2.8V/3.1/3.6V/4.1V
ÿ Low voltage detection LVD:
ÿ 1.2V/2.0V/2.4V/2.7V/3.0V/3.3V/3.6V/4.0 IN
ÿ Or external input voltage
Supports ISP and online debugging OCD
hardware breakpoints
Soft reset, single step, pause, jump, etc. ÿ Program ROM partition protection function
ÿ Package form: ÿ SOP8, MSOP10, SOP14, SOP16, SOP20, TSSOP20, DIP20

Peripheral characteristics

ÿ GPIO
General IO with independent control in 18 directions:
PORTA, PORTB, PORTC
ÿ 8 wake-up pins: PORTA ÿ 18 pins with open-drain function, independent control
ÿ 18 pins with pull-down function, independent control
ÿ 18 pins with pull-down function, independent control
ÿ ADC input channel : AN0-7
ÿ 8 programmable source currents PC0-1, PB2-7: 3/6/24mA@5V

ÿ 8 programmable sink current IOs: max 55mA@5V
ÿ Support remapping of pin second function
ÿ 12-bit bit
SAR ADC
ÿ 8 external channels + 3 internal reference voltage channels
ÿ Internal reference voltage: VDD, 0.5V, 2V, 3V
ÿ External reference: VREFP, VREFN
ÿ Timer0
ÿ 8-bit timer with 8-bit prescaler, clock source
Optional
ÿ Timer1
ÿ 12-bit timer, clock source optional
ÿ Timer2
ÿ 16-bit timer with 4-bit prescaler and 4-bit postscaler
ÿ Internal slow clock
measurement
ÿ 4 PWM channels with independent polarity and independent duty cycle
ÿ 1 pair of complementary PWM outputs with dead zone control,
which can be mapped to up to 6 IOs
ÿ Duty cycle and period register double buffering
Clock source:
HIRC, crystal clock, 2 times of HIRC, 2 times of crystal clock, and instruction clock, system clock, LIRC
ÿ Can keep working in sleep mode
ÿ Brake input
ÿ Buzzer mode
ÿ Single pulse mode



Selection table

model	PROM(ŷ) DROM(byte)	SRAM(byte)		I/Os	Timers	encapsulation
FT61F131B-RB	3k	128	256	6	3	SOP8
FT61F13F-RB				8		MSOP10
FT61F132A-RB				12		SOP14
FT61F133A-RB				14		SOP16
FT61F135-RB				18		SOP20
FT61F135-TRB				18		TSSOP20
FT61F135-DRB				18		DIP20



Table of contents

High performance RISC CPU.....	- 1 -
Special microcontroller features.....	- 1 -
Peripheral Characteristics.....	- 1 -
Selection table.....	- 2 -
1. System functional block diagram and pin locations.....	12
1.1. Pin diagram.....	13
1.2. Pin Description.....	14
2. Special function register.....	16
2.1. SFR ₀ BANK0	16
2.2. SFR ₁ BANK1	17
2.3. SFR ₂ BANK2	18
2.4. SFR ₃ BANK3	19
2.4.1. STATUS register, address 0x03, 0x83	20
2.5. PCL and PCLATH.....	twenty one
2.5.1. Modify PCL	21
2.6. INDF and FSR registers.....	22
2.7. About register reserved bits.....	twenty two
3. System clock source.....	twenty three
3.1. Clock source mode.....	twenty three
3.2. External clock mode.....	twenty four
3.2.1. Oscillator Start-up Timer (OST).....	twenty four
3.2.2. EC mode.....	twenty four
3.2.3. LP and XT modes.....	twenty four
3.3. Internal clock mode.....	twenty four
3.3.1. Frequency selection bit (IRCF).....	25
3.3.2. HIRC and LIRC clock switching timing.....	25
3.3.3. Relationship between frequency and minimum operating voltage.....	26
3.3.4. HIRC frequency fine-tuning.....	27



3.4.	Clock switching.....	27
3.4.1.	System Clock Select (SCS) bit.....	27
3.4.2.	Oscillator Start-up Timeout Status (OSTS) bit.....	27
3.5.	Two-Speed Clock Startup Mode.....	28
3.5.1.	Two-speed startup mode configuration.....	28
3.5.2.	Two-speed starting sequence.....	28
3.6.	Fail-Safe Clock Monitor.....	29
3.6.1.	Fault protection detection.....	29
3.6.2.	Fail-safe operation.....	29
3.6.3.	Clearing fault protection conditions.....	30
3.6.4.	Reset or wake up from sleep.....	30
3.7.	Summary of registers related to clock source.....	31
3.7.1.	OSCCON register, address 0x8F.....	31
3.7.2.	FOSCCAL register, address 0x0D.....	32
3.7.3.	MSCON1 register, address 0x18E.....	32
4.	Reset source.....	33
4.1.	POR power-on reset.....	34
4.2.	External reset MCLR.....	34
4.3.	PWRT (power-on timer)	34
4.4.	BOR low voltage reset.....	35
4.5.	LVD low voltage detection.....	35
4.5.1.	Detecting external voltage.....	35
4.6.	Error command reset.....	35
4.7.	Timeout action.....	35
4.7.1.	PCON register.....	36
4.8.	Power-on configuration process.....	36
4.9.	Power-on verification process.....	36
4.10.	PCON register, address 0x8E.....	39
4.11.	LVDCON register, address 0x110.....	40
4.12.	LVDTRIM register, address 0x19F.....	40



4.13.	Configuration register summary.....	41
4.13.1.	UCFG0, PROM address 0x2000.....	41
4.13.2.	UCFG1, PROM address 0x2001.....	42
4.13.3.	UCFG2, PROM address 0x2002.....	43
4.13.4.	UCFG3, PROM address 0x2003.....	44
4.13.5.	MAINCSUM (Address: 0x2007).....	44
5.	Watchdog timer.....	45
5.1.	Watchdog.....	45
5.2.	Watchdog clock source.....	46
5.3.	Summary of registers related to watchdog.....	46
5.3.1.	WDTCON register, address 0x18	47
6.	Interruption.....	48
6.1.	INT external interrupt.....	49
6.2.	Port change interrupt.....	49
6.2.1.	Clearing the PAIF flag.....	49
6.3.	Interrupt response.....	50
6.4.	Live saving during interruption.....	50
6.5.	About interrupt flags.....	50
6.6.	Summary of interrupt-related registers.....	51
6.6.1.	INTCON register, address 0x0B/0x8B	51
6.6.2.	PIR1 register, address 0x0C.....	52
6.6.3.	PIE1 register, address 0x8C	53
6.6.4.	IOCA register, address 0x96.....	53
7.	Sleep mode.....	54
7.1.	Wake-up mode.....	54
7.2.	Watchdog wakeup.....	55
7.3.	Wake-up from interrupt.....	55
7.4.	About the first instruction after SLEEP.....	55
8.	Data EEPROM.....	56
8.1.	Programming Data EEPROM Steps.....	56



8.2. Reading data EEPROM.....	58
8.3. About the programming cycle.....	58
8.4. Single Programming Mode of EEPROM.....	58
8.5. Summary of registers related to data EEPROM.....	59
8.5.1. EEDAT register, address 0x9A.....	59
8.5.2. EEADR register, address 0x9B	59
8.5.3. EECON1 register, address 0x9C	60
8.5.4. EECON2 register, address 0x9D	60
9. 12bit ADC module.....	61
9.1 ADC configuration.....	61
9.1.1 Port configuration.....	62
9.1.2 Channel selection.....	62
9.1.3 Trigger mode selection.....	62
9.1.4 Trigger source selection.....	62
9.1.5 Trigger type selection.....	62
9.1.6 Trigger delay configuration.....	62
9.1.7 ADC reference voltage.....	63
9.1.8 Conversion clock.....	63
9.1.9 Interrupts.....	64
9.1.10 Format of conversion results.....	65
9.1.11 Threshold comparison.....	65
9.2 How ADC works.....	66
9.2.1 Starting the conversion.....	66
9.2.2 Conversion completed.....	66
9.2.3 Terminating conversion.....	66
9.2.4 ADC operation in sleep mode.....	66
9.2.5 A/D conversion steps.....	67
9.2.6 A/D acquisition time requirements.....	68
9.3 Summary of registers related to ADC.....	69
9.3.1 ADRESL, address 0x111	69



9.3.2 ADRESH, address 0x112.....	69
9.3.3 ADCON0, address 0x113.....	70
9.3.4 ADCON1, address 0x114.....	71
9.3.5 ADCON2, address 0x115.....	72
9.3.6 LEBCON register, address 0x185.....	73
9.3.7 ADCON3, address 0x186.....	73
9.3.8 ADCMPH, address 0x187.....	74
9.3.9 ADDLY/LEBPRL, address 0x188	74
9.3.10 VRP5VCAL, address 0x97.....	74
9.3.11 VR2VCAL, address 0x108	75
9.3.12 VR3VCAL, address 0x11F	75
10. Timer 0.....	76
10.1. Timer0 timer mode.....	76
10.1.1. Timer0 clock source.....	77
10.1.2. Reading and writing the TMR0 register.....	77
10.2. Timer0 Counter Mode.....	77
10.2.1. Software configurable prescaler circuit.....	77
10.2.2. Timer 0 interrupt.....	78
10.2.3. Driving Timer 0 with an external clock	78
10.2.4. Status in sleep mode.....	78
10.3. Summary of registers related to Timer0.....	79
10.3.1. OPTION register, address 0x81.....	79
10.3.2. TMR0, address 0x01.....	80
10.3.3. T0CON0, address 0x1F.....	80
11. Timer 1.....	81
11.1. Timer1 Working Principle.....	81
11.2. Reading and writing of Timer1 count value.....	82
11.3. Summary of registers related to Timer1.....	82
11.3.1. PR1L register, address 0x116,0x117.....	82
11.3.2. TMR1 register, address 0x118, 0x119.....	83



11.3.3.	T1CON0 register, address 0x11A	83
12.	Timer 2.....	84
12.1.	Timer2 working principle.....	85
12.2.	Updates about PR2.....	85
12.3.	Reading and writing of Timer2 count value.....	86
12.4.	Timer2 prescaler clear.....	87
12.5.	Timer2 clock source.....	87
12.6.	Working while sleeping.....	87
12.7.	Summary of registers related to Timer2.....	88
12.7.1.	PR2 register, address 0x91, 0x92	88
12.7.2.	TMR2 register, address 0x11, 0x13	88
12.7.3.	T2CON0 register, address 0x12	89
12.7.4.	T2CON1 register, address 0x9E.....	90
13.	PWM module.....	91
13.1.	cycle.....	91
13.2.	Duty cycle.....	92
13.3.	Clock source selection.....	92
13.4.	PWM status during sleep	92
13.5.	P1A dead time.....	93
13.6.	Faulty brake.....	93
13.6.1.	Braking status.....	94
13.6.2.	Troubleshooting.....	94
13.6.3.	Automatic restart.....	94
13.7.	Updates to the period and duty cycle registers.....	95
13.8.	Buzzer mode (Buzzer)	96
13.9.	Single pulse output.....	96
13.10.	PWM output remapping.....	96
13.11.	The second function output of P1C and P1D.....	97
13.12.	Summary of registers related to PWM1.....	98
13.12.1.	P1ADTL register, address 0x0E	98



13.12.2. P1BDTL register, address 0x0F.....	99
13.12.3. P1CDTL register, address 0x10.....	99
13.12.4. P1DDTL register, address 0x8.....	99
13.12.5. TMR2L register, address 0x11.....	99
13.12.6. TMR2H register, address 0x13	100
13.12.7. T2CON0 register, address 0x12	100
13.12.8. P1ADTH register, address 0x14	100
13.12.9. P1BDTH register, address 0x15	100
13.12.10. P1CDTH register, address 0x1A	101
13.12.11. P1DDTH register, address 0x9	101
13.12.12. P1CON register, address 0x16	101
13.12.13. P1BR0 register, address 0x17	102
13.12.14. P1BR1 register, address 0x19	103
13.12.15. P1OE2 register, address 0x11B	104
13.12.16. P1OE register, address 0x90	105
13.12.17. PR2L register, address 0x91.....	105
13.12.18. PR2H register, address 0x92	106
13.12.19. P1POL register, address 0x99.....	106
13.12.20. P1POL2 register, address 0x109.....	107
13.12.21. P1AUX register, address 0x1E	108
14. I/O end.....	109
14.1. PORTx port and TRISx register.....	109
14.2. Other functions of the port.....	110
14.2.1. Weak pull-up.....	110
14.2.2. Weak pull-down.....	110
14.2.3. ANSEL register.....	110
14.3. Source current selection.....	110
14.4. Sink current selection.....	110
14.5. Open drain function.....	111
14.6. Summary of registers related to GPIO.....	111



14.6.1. WPUA, address 0x95.....	111
14.6.2. WPUB, address 0x10D.....	112
14.6.3. WPUC, address 0x93.....	112
14.6.4. TRISA, address 0x85.....	112
14.6.5. TRISB, address 0x86.....	113
14.6.6. TRISC, address 0x87.....	113
14.6.7. PORTA, address 0x05.....	113
14.6.8. PORTB, address 0x06.....	114
14.6.9. PORTC, address 0x7.....	114
14.6.10. WPDA, address 0x89.....	114
14.6.11. WPDB, address 0x10E.....	115
14.6.12. WPDC, address 0x8D.....	115
14.6.13. PSRCB1, address 0x88.....	115
14.6.14. PSRCB2, address 0x10C.....	116
14.6.15. PSRCC, address 0x94.....	116
14.6.16. PSINKB, address 0x10F.....	117
14.6.17. PSINKC, address 0x9F.....	117
14.6.18. ODCONA, address 0x105	117
14.6.19. ODCONB, address 0x106	118
14.6.20. ODCONC, address 0x107.....	118
14.6.21. ANSEL0, address 0x11E.....	118
15. Slow Clock Measurements.....	119
15.1. Measurement principle.....	119
15.2. Steps.....	120
15.3. Summary of registers related to slow clock measurement.....	120
15.3.1. MSCON0 register, address 0x1B	121
15.3.2. SOSCPR register, address 0x1C, 1D	122
16. Instruction Set Summary.....	123
17. Chip electrical characteristics.....	125
17.1. Limit parameters.....	125



17.2.	Built-in high-frequency oscillator (HIRC)	125
17.3.	Built-in low-frequency oscillator (LIRC).....	125
17.4.	Low Voltage Reset Circuit (LVR).....	126
17.5.	Low voltage detection circuit (LVD).....	126
17.6.	Power-on reset circuit (POR)	126
17.7.	I/O PAD circuit.....	127
17.8.	Overall operating current (IDD).....	128
17.9.	AC Electrical Parameters.....	128
17.10.	12bit ADC characteristics.....	129
17.11.	DC and AC characteristic curves.....	130
17.11.1.	HIRC vs VDD (TA=25°C).....	130
17.11.2.	LIRC vs VDD (TA=25°C).....	131
17.11.3.	IDD vs Freq (2T, TA=25°C) under different VDD	131
17.11.4.	ISB (sleep current) changes with temperature curve under different VDD.....	132
17.11.5.	IOH (L0 -3mA) vs VOH @VDD=5V at different temperatures	132
17.11.6.	IOH (L1 -6mA) vs VOH @VDD=5V at different temperatures	133
17.11.7.	IOH (L2 -18mA) vs VOH @VDD=5V at different temperatures	133
17.11.8.	IOH (L3 -24mA) vs VOH @VDD=5V at different temperatures	134
17.11.9.	IOL (L0 35mA) vs VOL @VDD=5V at different temperatures	134
17.11.10.	IOL (L1 53mA) vs VOL @VDD=5V at different temperatures	135
17.11.11.	IOL (L2 55mA) vs VOL @VDD=5V at different temperatures	135
18.	Chip packaging information.....	136
	Appendix 1, Document Change History.....	143

1. System functional block diagram and pin locations

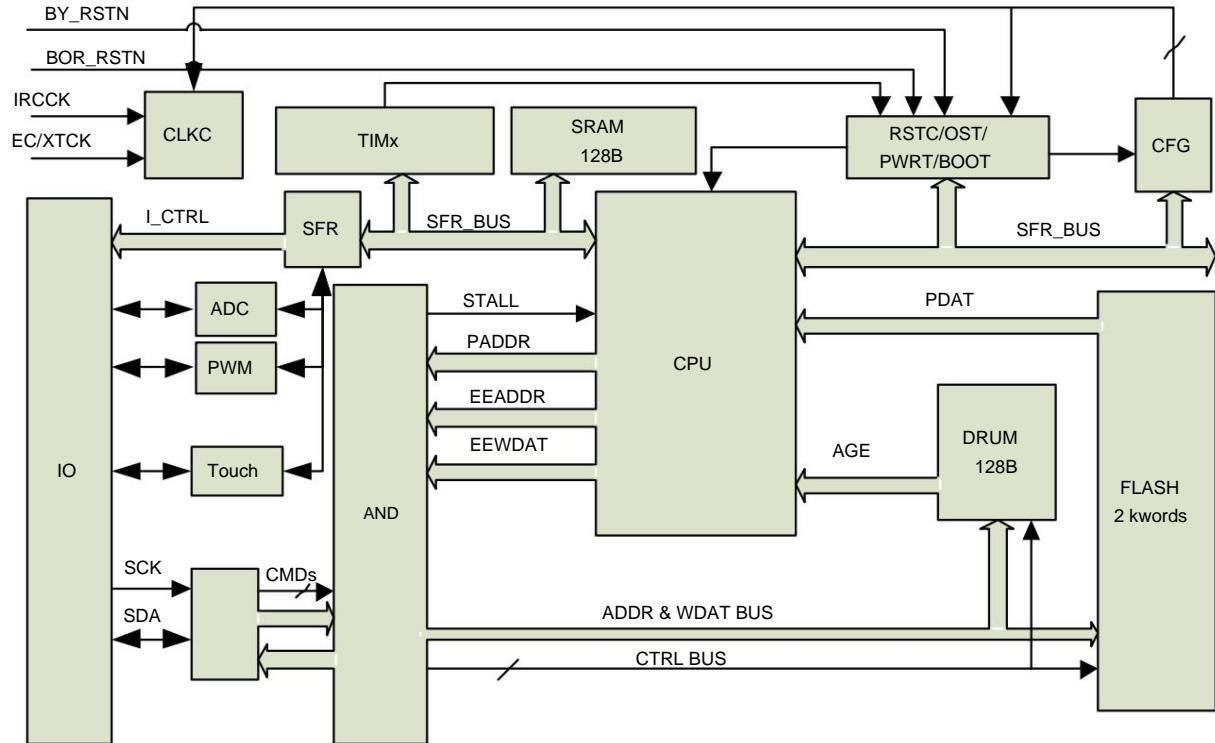


Figure 1.1 Overall functional block diagram of the chip

1.1. Pin diagram



Figure 1.2 SOP8 pin position

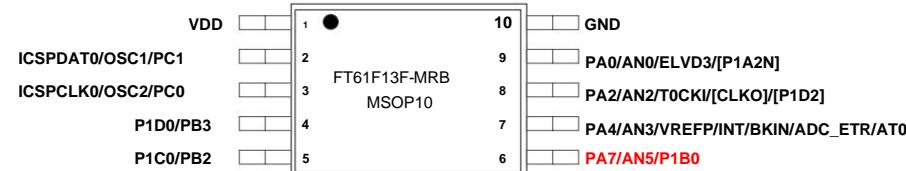


Figure 1.3 MSOP10 pin location

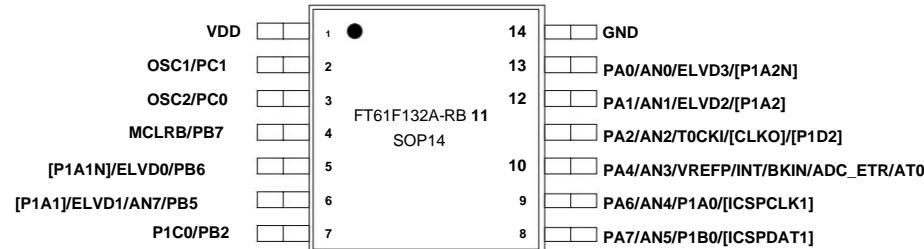


Figure 1.4 SOP14 pin position

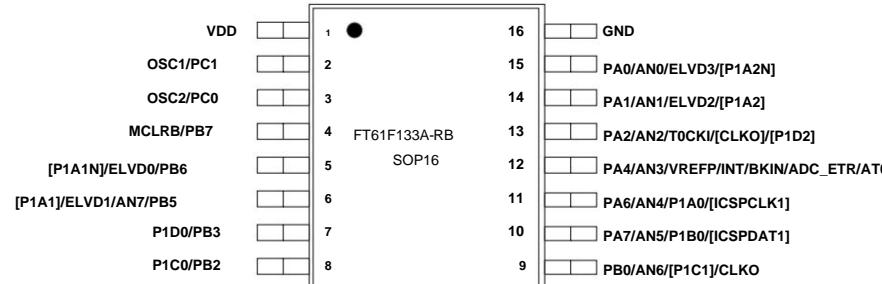


Figure 1.5 SOP16 pin position

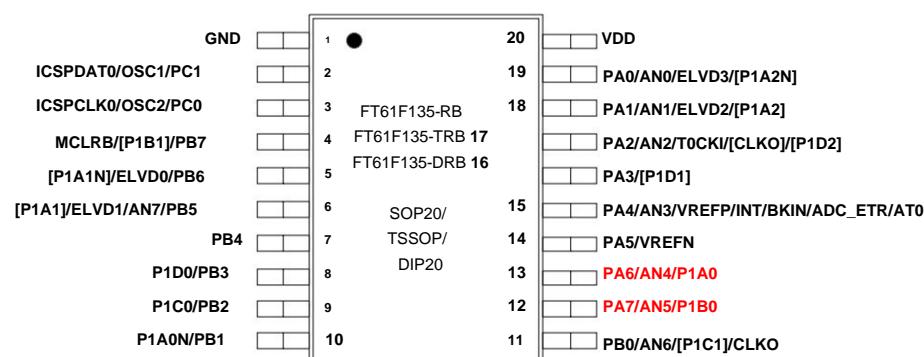


Figure 1.6 SOP20/TSSOP20/DIP20 pin position

1.2.Pin description

SOP20	Pin name	Type	INT input	Main func.	Pullup/down
1	GND	Ground	-	Ground	
2	PC1/OSC1/ICSPDAT	IO	-	PC1	ÿ
	OSC1, transistor pin 1				
	ISPDAT, ISP data IO				
3	PC0/OSC2/ICSPCLK	IO	-	PC0	ÿ
	OSC2, transistor pin 2				
	ISPCK, ISP clock input				
4	PB7/[P1B1]/MCLRB	IO	-	PB7	ÿ
	[P1B1], mapping output of P1B				
	MCLRB, external reset input				COULD
5	PB6/ELVD0/[P1A1N]	IO	-	PB6	ÿ
	ELVD0, external LVD detection input 0				
	[P1A1N], mapping output of P1A0N				
6	PB5/ AN7/ELVD0/[P1A1]	IO	-	PB5	ÿ
	AN7, analog input channel 7				
	ELVD1, external LVD detection input 1				
	[P1A1], mapping output of P1A0				
7	PB4/ ATEST0	IO	-	PB4	ÿ
	ATEST0, internal test pin 0				
8	PB3 /P1D0	IO	-	PB3	ÿ
	P1D0, PWMD output				
9	PB2 / P1C0	IO	-	PB2	ÿ
	P1C0, PWMC output				
10	PB1/P1A0N	IO	-	PB1	ÿ
	P1A0N, PWM output of P1A0N				
11	PB0/AN6/[P1C1]/CLKO	IO	-	PB0	ÿ
	AN6, analog input channel 6				
	[P1C1], mapping output of P1C				
	CLKO, command clock output				
12	PA7/AN5/P1B0/[ICSPCLK1]	IO	ÿ	PA7	ÿ
	AN5, analog input channel 5				
	P1B0, PWM output of PWMB				
	[ICSPCLK1], ISP data mapping IO				
13	PA6/AN4/P1A0/[ICSPCLK1]	IO	ÿ	PA6	ÿ
	AN4, analog input channel 4				
	P1A0, PWM output of P1A0				
	[ICSPCLK1], ISP clock map input				



SOP20	Pin name	Type	INT input	Main func. Pullup/down
14	PA5/VREFN	IO	ÿ	PA5 ÿ
	VREFN, ADC external negative reference input			
15	PA4/AN3/VREFP /INT/BKIN/ADC_ETR/ATO	IO	ÿ	PA4 ÿ
	AN4, analog input channel 4			
	VREFP, ADC external positive reference input			
	INT, external interrupt input			ÿ
	BKIN, PWM brake input			
	ADC_ETR, ADC external trigger signal input			
	ATO, TEST test pin			
16	PA3/[P1D1]	IO	ÿ	PA3 ÿ
	[P1D1], mapping output of P1D			
17	PA2/AN2/T0CKI/[CLKO]/[P1D2]	IO	ÿ	PA2 ÿ
	AN2, analog input channel 2			
	T0CKI, Timer0 external clock			
	[CLKO], system clock mapping output pin			
	[P1D2], mapping output of P1D			
18	PA1/AN1/ELVD2/[P1A2]	IO	ÿ	PA1 ÿ
	AN1, analog input channel 1			
	ELVD2, external LVD detection input 2			
	[P1A2], mapping output of P1A0			
19	PA0/AN0/ELVD3/[P1A2N]	IO	ÿ	PA0 ÿ
	AN0, analog input channel 0			
	ELVD3, external LVD detection input 3			
	[P1A2N], mapping output of P1A0N			
20	VDD	Power	-	Power



2.Special function register

2.1. SFRyBANK0

ADDR Name		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	BY reset
BANK0										
0	INC									xxxx xxxx
1	TMRO									xxxx xxxx
2	PCL									0000 0000
3	STATUS	FSRB8		PAGE[1:0]	/TF	/PF		HC	C	0001 1xxx
4	FSR									xxxx xxxx
5	BRINGS	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	xxxx xxxx
6	PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	xxxx xxxx
7	PORTC	-	-	-	-	-	-	PC1	PC0	yyyy yyxx
8	P1DDTL									0000 0000
9	P1DDTH									0000 0000
A	PCLATH	-	-	-						yyyo 0000
B	INTCON	GIE	LIKE THIS	T0IE	NOT	PAY	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMIF	LVDIF ACMIF TMR1IF			OSFIF	TMR2IF	ADCIF	0000 0000
D	FOSCCAL									0110 1000
AND	P1ADTL									0000 0000
F	P1BDTL									0000 0000
10	P1CDTL									0000 0000
11	TMR2L									0000 0000
12	T2CON0	PR2U		TOUTPS[3:0]			TMR2ON		T2CKPS[1:0]	0000 0000
13	TMR2H									0000 0000
14	P1ADTH									0000 0000
15	P1BDTH									0000 0000
16	P1CON	P1AUE								0000 0000
17	P1BR0	P1BEVT		P1BKS[2:0]		P1BSS[1:0]		P1ASS[1:0]		0000 0000
18 WDTCON —				WCKSRC[1:0]		WDTPS[3:0]				SWDTEN yy000 1000
19	P1BR1		P1D2SS[1:0]		P1DSS[1:0]		P1C2SS[1:0]		P1CSS[1:0]	0000 0000
1A	P1CDTH									0000 0000
1B MSCON0 —			— ROMLPE CLKOS SLVREN CKMAVG CKCNTI T2CKRUN	0001 0000						
1C SOSCPRL						SOSCPR [7:0]				1111 1111
1D SOSCPRH —										yyyy 1111
1E	P1AUX	-	-	P1BSS[1:0]		P1CF2E	P1CF2	P1DF2E	P1DF2	yy00 0000
1F	T0CON0	-	-	-	— TOON	T0CKRUN			T0CKSRC[1:0]	yyyy 1000
20~3F										xxxx xxxx
40~7F										xxxx xxxx



2.2. SFR_yBANK1

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	BY reset
BANK1										
80	INC									xxxx xxxx
81	OPTION	/PAPU INTEDG		T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL									0000 0000
83	STATUS	FSRB8	PAGE[1:0]		/TF	/PF		HC	C	0001 1xxx
84	FSR									xxxx xxxx
85	TRISA									1111 1111
86	TRISB									1111 1111
87	TRISC	-	-	-	-	-	-		TRISC[1:0]	ÿÿÿ ÿÿ11
88	PSRCB1									1111 1111
89	WPDA									0000 0000
8A	PCLATH	-	-	-						ÿÿ0 0000
8B	INTCON	GIE	LIKE THIS	T0IE	NOT	PAY	TOIF	INTF	PAIF	0000 0000
8C	PIE1	THIS	CKMIE	LVDIE ACM	PIE TMR1IE OS	FIE TMR2IE				ADCIE
8D	WPDC	-	-	-	-	-	-			PORTC weak pull-down controlÿÿ ÿÿ00
8E	PCON		LVDL[3:0]		LVDEN LVDW		/BY		/THERE IS	0000 0xqq
8F	OSCCON LFMOD		IRCF[2:0]		OSTS	HTS	LTS		SCS	0101 x000
90	P1OE	P1C0OE P1B0OE P1A2NOE	P1A2OE P1A1NOE	P1A1OE P1A0NOE					P1A0OE	0000 0000
91	PR2L									1111 1111
92	PR2H									1111 1111
93	WPUC	-	-	-	-	-	-			PORTC weak pull-up controlÿÿ00
94	PSRCC	-	-	-	-					ÿÿÿ 1111
95	WPUA									1111 1111
96	JOKE									0000 0000
97	VRP5VCAL									xxxx xxxx
98		-								0000 0000
99	P1POL	P1C0P	P1B0P P1A2NP	P1A2P P1A1NP	P1A1P P1A0NP				P1A0P	0000 0000
9A	EDTA									0000 0000
9B	EEADR									0000 0000
9C	EECON1	- Reserved	WREN3 WRE	N2 WRERR WRE	N1 PONLY				RD	ÿ000 x000
9D	EECON2	-	-	-	-	-	-	-	WR	ÿÿÿ ÿÿ00
9E	T2CON1	-	-	- P1OS	P1BZM				T2CKSRC[2:0]	ÿÿ0 0000
9F	PSINKC	-	-	-	-	-	-		PSINKC[1:0]	ÿÿÿ ÿÿ00
A0-BF										xxxx xxxx
C0-EF										xxxx xxxx
F0-FF										xxxx xxxx

2.3. SFR \ddot{y} BANK2

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	BY reset
BANK2										
100	INC									xxxx xxxx
101	RXRSM	-	-	RSVH1 RSVH1X RSAST			RSBST	REB	RSDATA $\ddot{y}00$	0010
102	PCL									0000 0000
103	STATUS	FSRB8	PAGE[1:0]	/TF	/PF		HC	C		0001 1xxx
104	FSR									xxxx xxxx
105	EPISODE					ODCON[7:0]				0000 0000
106	ODCONB					ODCONB[7:0]				0000 0000
107	ODCONC —		-	-	-	-			ODCONC[1:0]	$\ddot{y}yyy \ddot{y}00$
108	VR2VCAL					VR2VCAL[7:0]				xxxx xxxx
109	P1POL2	P1D2P	P1D1P	P1D0P —		— P1C1P		P1B1P	— 000 \ddot{y} 00 \ddot{y}	
10A	PCLATH	-	-	-						$\ddot{y}00$ 0000
10B	INTCON	GIE	LIKE THIS	T0IE	NOT	PAY	T0IF	INTF	PAIF	0000 0000
10C	PSRCB2 —		-	-	-					$\ddot{y}yyy$ 1111
10D	WPUB					WPUB[7:0]				0000 0000
10E	WPDB									0000 0000
10F	PSINKB				PSINKB[7:2]					0000 00 \ddot{y}
110	LVDCON		-		LVDP	LVDDEB		LVDM[2:0]		$\ddot{y}00$ 1100
111	ADDRESS									xxxx xxxx
112	ADRESH									xxxx xxxx
113	ADCON0 —				CHS[3:0]		ADEX GO/DONE ADON $\ddot{y}000$ 0000			
114	ADCON1 ADFM				ADCS[2:0]	ADNREF[1:0]		ADPREF[1:0]		0000 0000
115	ADCON2		ADINTREF[1:0]		ETGTYPE[1:0]	ADDLY.8		ETGSEL[2:0]		0000 0000
116	PR1L									1111 1111
117	PR1H		-							$\ddot{y}yyy$ 1111
118	TMR1L					Timer1[7:0]				0000 0000
119	TMR1H		-							$\ddot{y}yyy$ 0000
11A	T1CON0		-		T1CKPSA T1CKRUN T1ON			T1CKSRC[1:0]		$\ddot{y}00$ 0000
11B	P1OE2 P1D2DE P1D1OE P1D0OE —					— P1C1OE P1B1OE — 000 \ddot{y} 00 \ddot{y}				
11C	-					-				--
11D	-					-				--
11E	ANSEL0					ANSEL0[7:0]				0000 0000
11F	VR3VCAL					VR3VCAL[7:0]				xxxx xxxx
120-16F						SRAM BANK2 (80Bytes), Physical address 0xB0-0xFF				xxxx xxxx
170-17F						SRAM, access 0x70-0x7F of BANK0				xxxx xxxx

2.4. SFR $\ddot{\text{y}}$ BANK3

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	BY reset
BANK3										
180	INC									xxxx xxxx
181	SECCODE									xxxx xxxx
182	PCL									0000 0000
183	STATUS	FSRB8		PAGE[1:0]	/TF	/PF	with	HC	C	0001 1xxx
184	FSR									xxxx xxxx
185	LEBCON	LIFE		LEBCH[1:0]	— EDGS —			— — 00 $\ddot{\text{y}}$ 0yyy		
186	ADCON3	ADFBEN	ADCMPOP	ADCPEN — LEBADT —				— — 00 $\ddot{\text{y}}$ 0yyy		
187	ADCMPH									0000 0000
188	ADDLY									0000 0000
18A	PCLATH	—	—	—						yy $\ddot{\text{y}}$ 0 0000
18B	INTCON	GIE	LIKE THIS	TOIE	NOT	PAY	TOIF	INTF	PAIF	0000 0000
18C	—				—					—
18D	—				—					—
18E	MSCON1									HIRCM yy $\ddot{\text{y}}$ yy0
19F	LVDTRIM —			LVDADJ[3:0]			LVRADJ[2:0]			yy100 0011
1A0-1EF				—						—
1F0-1FF										xxxx xxxx

Notice:

1. **INDF** is not a physical register;
2. The gray part indicates that it is not implemented;
3. Do not write 1 to unimplemented register bits , which may be used in future chip upgrades;

2.4.1. STATUS register, address 0x03, 0x83

Bit	7	6	5	4	3	2	1	0
Name	FSRB8	PAGE[1:0]		/TF	/PF	WITH	HC	C
Reset	0	00		1	1	x	x	x
Type	RW	RW		RO	RO	RW	RW	RW

Bit	Name	Function
7	FSRB8	Bit 8 of the FSR register, and FSR form a 9-bit register, used in indirect addressing See the INDF and FSR register section for details.
6:5	PAGE	PAGE: Register storage area selection bit (for direct addressing) 11 = Bank 3 (0x180 – 0x1FF) 10 = Bank 2 (0x100 – 0x17F) 01 = Bank 1 (0x080h – 0xFFh) 00 = Bank 0 (0x00h – 0x7Fh)
4	/TF	/TF: timeout status bit 1 = After power-up, the CLRWDT instruction or the SLEEP instruction was executed 0 = WDT timeout occurred
3	/PF	/PF: power-down flag 1 = After power-on reset or execution of CLRWDT instruction 0 = SLEEP instruction executed
2	WITH	Z: zero flag 1 = The result of an arithmetic or logical operation is zero 0 = The result of an arithmetic or logical operation is non-zero
1	HC	HC: Half carry/borrow bit (ADDW, ADDL, SUBL and SUBWF instructions). For borrow, the polarity is reversed. 1 = A carry from the 4th low-order bit of the result to the high-order bit occurred 0 = No carry-out from the 4th low-order bit of the result to the high-order bit occurred
0	C	C: Carry/borrow bit (ADDW, ADDW, SUBL and SUBWF instructions) 1 = A carry from the most significant bit of the result occurred 0 = No carry from the most significant bit of the result occurred

/TF	/PF	condition
1	1	Power on or low voltage reset
0	IN	WDT reset
0	0	WDT wake up
IN	IN	MCLR reset occurs during normal operation
1	0	MCLR reset occurs during sleep state

Notice:

1. Like other registers, the status register can also be used as the target register of any instruction. If an instruction affects **Z**, **HC** or **C**

Bit instructions use the status register as the target register and will prohibit writing operations on these three bits. They are only affected by the logical results and are set 1 or cleared to 0. Therefore, when an instruction is executed with the status register as the destination register, the STATUS content may be different from the expected inconsistent;

2. It is recommended to only use the **BCR**, **BSR**, **SWAPR** and **STR** instructions to change the status register.

2.5. PCL and PCLATH

The program counter (PC) is 12 bits wide. The lower 8 bits come from the readable and writable PCL register, and the upper 4 bits (PC<11:8>) come from PCLATH.

Cannot read and write directly. Whenever a reset occurs, PC will be cleared to 0. The figure below shows two scenarios for loading PC values. Note the LCALL on the right side of the picture and LJUMP instructions. Since the opcode in the instruction is 11 bits and the PC of the chip is exactly 11 bits, PCLATH is not needed at this time.

To be used.

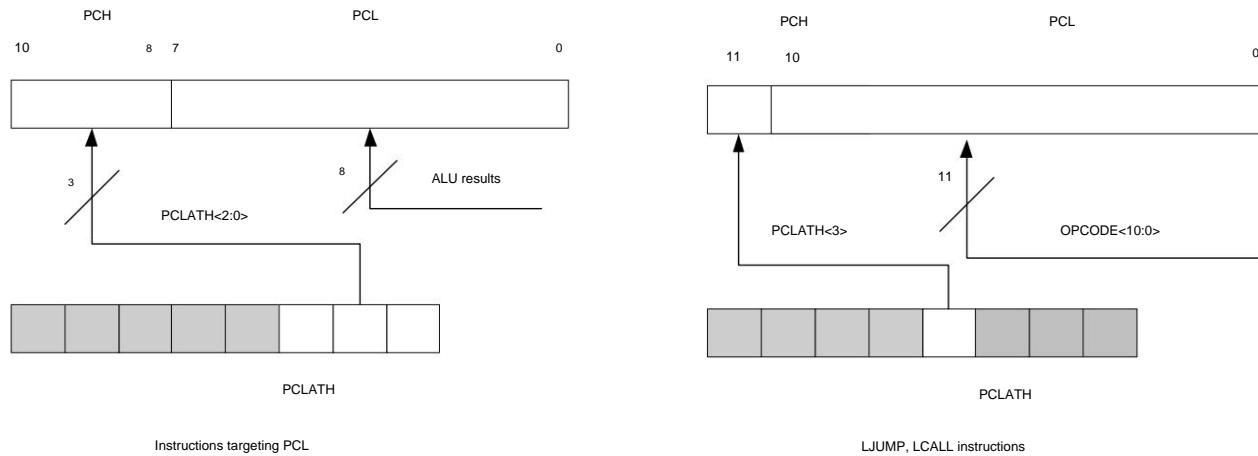


Figure 2.1 PC loading under different circumstances

2.5.1. Modify PCL

Execution of any instruction with the PCL register as the destination register will also cause the program counter PC<10:8> bits to be replaced by the contents of PCLATH. this

The entire contents of the program counter can thus be changed by writing the required upper 3 bits to the PCLATH register.

LJUMP instructions are calculated by adding an offset to the program counter (ADDWR PCL). Jump by modifying the PCL register

Particular caution should be exercised when jumping to lookup tables or program branch tables (computing LJUMP). Assuming that PCLATH is set to the starting address of the table, if the table

The length is greater than 255 instructions, or if the lower 8 bits of the memory address rollover from 0xFF to 0x00 in the middle of the table, then each table

When a rollover occurs between the starting address and the target address in the table, PCLATH must be incremented.

2.6. INDF and FSR registers

INDF is not a physically existing register. Addressing INDF will result in indirect addressing, and the addressable range is 0–255. Any use of INDF

Register instructions actually access the unit pointed to by the file selection register FSR.

Indirect reads from INDF will return 0. Writing to INDF indirectly will result in a no-operation (may affect status flags).

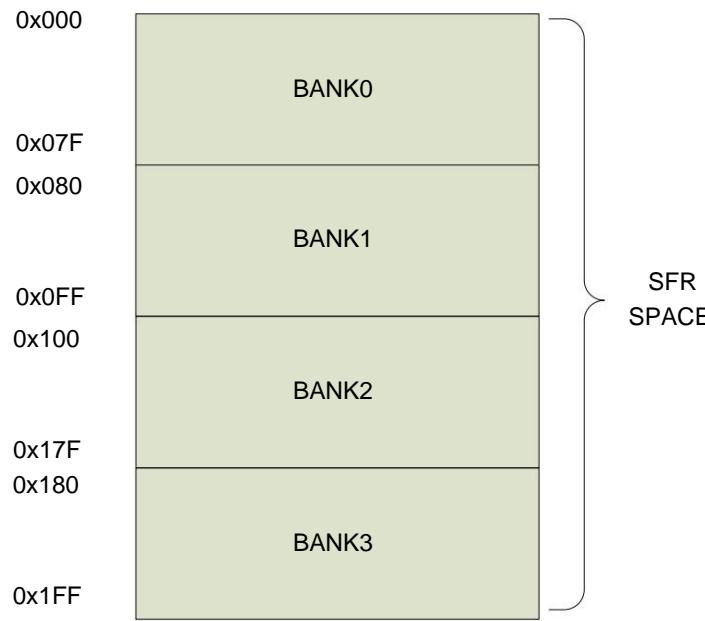


Figure 2.2 Indirect addressing

2.7. About register reserved bits

As shown in the table in Chapter 2.1/1.2, some registers or register bits in the SFR space are not implemented. The unimplemented register bits are reserved.

bit, the software returns 0 when reading, and writing is invalid.

It is not recommended that the program writes 1 to these reserved bits. This may cause problems in future program transplantation because subsequent chip products may use it.

This bit.

3. System clock source

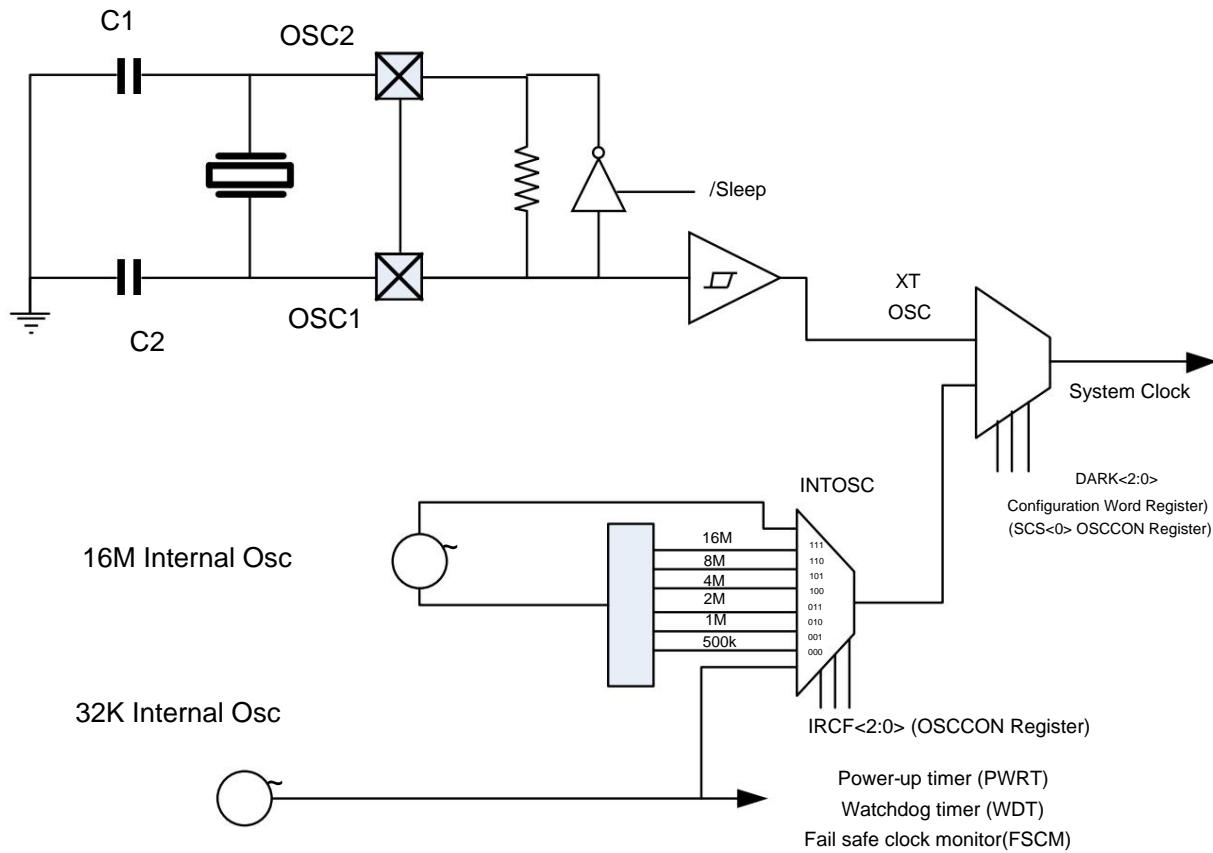


Figure 3.1 System clock source block diagram

This chip contains 4 clock sources: 2 built-in RC oscillators (high and low speed), 1 external crystal oscillator, and 1 external clock sink source.

The built-in oscillator includes an internal 16M high-speed precision oscillator (HIRC) and an internal 32k/256k (LIRC) low-speed and low-power oscillator. These clocks or oscillators combined with prescalers can provide clock sources of various frequencies to the system.

The prescaler ratio of the system clock source is controlled by the IRCF<2:0> bits in the OPTION register.

3.1. Clock source mode

Clock source modes are divided into external and internal modes.

External clock mode relies on an external circuit to provide a clock source, such as external clock EC mode, crystal resonator XT, and LP mode.

Internal clock mode is built into the oscillator module, which has a 16MHz high-frequency oscillator and a 32kHz low-frequency oscillator.

The internal or external clock source can be selected through the system clock select bit (SCS) of the OSCCON register.



3.2. External clock mode

3.2.1. Oscillator start-up timer (OST)

If the oscillator module is configured in LP, XT mode, the oscillator start-up timer (OST) will count oscillations from OSC1 1024 times. This occurs after a power-on reset (POR) and at the end of the Power-up Timer (PWRT) delay (if enabled), or after waking up from Sleep. During this time, the program counter is not incremented and program execution is suspended. OST ensures that the oscillator circuit using a quartz crystal resonator or ceramic resonator is started and provides a stable system clock signal to the oscillator module. When switching between clock sources, a certain delay is required to allow the new clock to stabilize.

Note: 1.

The OST reuses the WDT timer, so when the OST counts the crystal clock, the WDT function is blocked. After the OST overflows,

The WDT function is restored (if WDT was previously enabled).

2. Since OST and WDT share a timer, do not write to the WDTCON or OPTION register before the OST overflows.

device, otherwise unpredictable behavior may occur.

3.2.2. EC mode

External clock mode allows externally generated logic levels to be used as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 pin can be used as a general-purpose I/O. When EC mode is selected, the Oscillator Start-up Timer (OST) is disabled. Therefore, there is no delay in operations after power-on reset (POR) or wake-up from sleep. After the MCU wakes up, the external clock is started again, and the device resumes operation as if it had never stopped.

3.2.3. LP and XT modes

LP and XT modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2. Mode selects low or high gain settings for the internal inverting amplifier to support various resonator types and speeds.

LP oscillator mode selects the lowest gain setting of the internal inverting amplifier.

LP mode has the smallest current consumption of the two modes. This mode is designed only to drive 32.768 kHz tuning fork crystal oscillator (clock crystal oscillator). XT oscillator mode selects the high gain setting of the internal inverting amplifier.

3.3. Internal clock mode

The oscillator module has two independent internal oscillators that can be configured or selected as the system clock source.

1. HIRC (High Frequency Internal Oscillator) is factory calibrated and operates at 16MHz.

2. LIRC (Low Frequency Internal Oscillator) is uncalibrated and operates at 32 kHz. Software sets the internal oscillator frequency in the OSCCON register.

The system clock speed can be selected by operating the rate selection bits IRCF<2:0>.

The system clock can be selected between an external or internal clock source through the System Clock Select (SCS) bit of the OSCCON register.

3.3.1. Frequency selection bit (IRCF)

The outputs of the 16MHz HIRC and 32kHz LIRC are connected to the prescaler and multiplexer (see Figure 3.1). The internal oscillator frequency selection bits IRCF<2:0> of the OSCCON register are used to select the frequency output of the internal oscillator. One of the following 8 frequencies can be selected through software: 16MHz
 ÿ 8MHz
 ÿ 4MHz
 (default value)
 after reset) 2MHz
 ÿ 1MHz
 ÿ 500 kHz
 ÿ 250 kHz
 ÿ 32 kHz

3.3.2. HIRC and LIRC clock switching timing

When switching between LIRC and HIRC, the new oscillator may have been turned off to save power (see Figure 3.2 and Figure 3.3). In this case, there is a delay after the IRCF bit in the OSCCON register is modified before the frequency selection takes effect. The LTS and HTS bits of the OSCCON register will reflect the current active status of the LIRC and HIRC oscillators. The frequency selection timing is as follows: 1. The IRCF<2:0> bits of the OSCCON register are modified 2. If the new clock is turned off, a clock start delay is started 3. The clock switching circuit waits for the arrival of the falling edge of the current clock 4. CLKOUT is maintained low, the clock switching circuit waits for the arrival of two new clock falling edges 5. Now CLKOUT is connected to the new clock. The HTS and LTS bits of the OSCCON register are updated as required 6. Clock switching completed

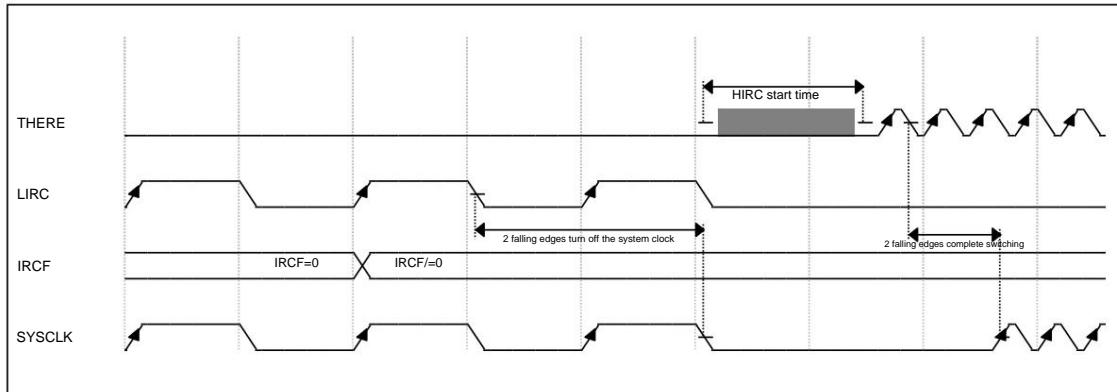


Figure 3.1 Switching from slow clock to fast clock

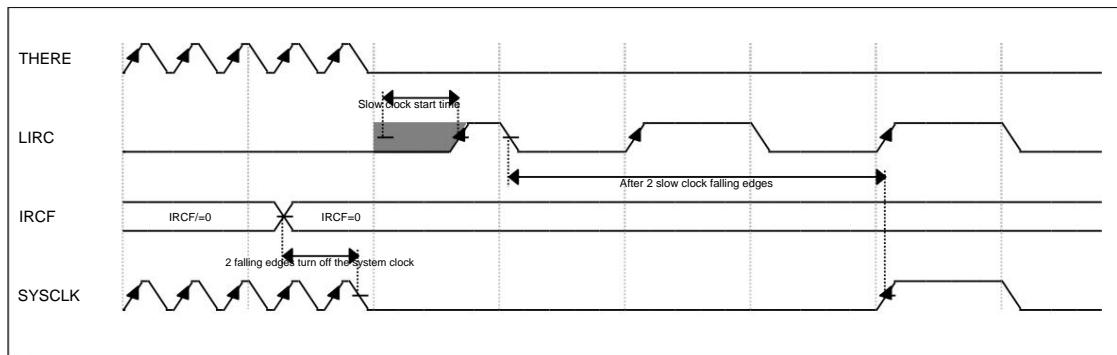


Figure 3.2 Switching from fast clock to slow clock

3.3.3. Relationship between frequency and minimum operating voltage

The higher the system clock frequency, the higher the MCU's requirements for the minimum operating voltage (safe operating voltage). For example, if you want to run 16M in 2T operating mode, VDD should be at least above 2.7V.

The power-on reset voltage VPOR of the FT62F13x series chips is around 1.6V. That is, when VDD exceeds VPOR during the power-on process, the reset is released. After a delay of about 8ms, the power-on configuration is completed, and then the program instructions begin to be executed. For some applications that are powered on slowly and need to run **16M/2T**, if the time for VDD to rise from VPOR to VDDmin of 2.7V is too long, and the program switches to the highest system clock of 16M during this "dead time", The MCU will likely run away.

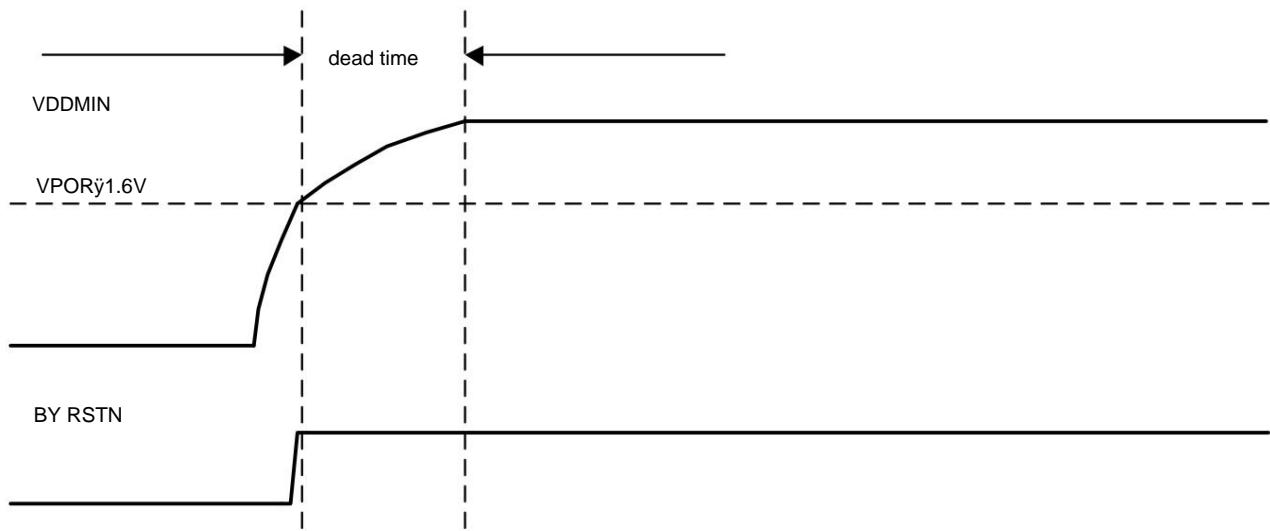


Figure 3.3 "Dead time" during power-on process

For slow power-on applications, there are several methods to avoid this situation: 1. The programming

option LVR must be enabled and set to an appropriate value. For example, **16M/2T** should set a reset voltage of **2.8V** ; 2. Power on After reset, the software can delay long enough for VDD to rise to a safe operating voltage before switching to the 16M system clock, that is

Delay for a period of time before initializing the clock;

3. Enable the PWRT option. The PWRT time is about 64ms. This extra reset time is beneficial to allowing VDD to climb to the minimum working value.

operating voltage;

Among the above three points, it is strongly recommended to use the first method, because it can not only solve the problem of slow power-on speed, but also monitor the unexpected drop of VDD during normal operation.

3.3.4. HIRC frequency fine-tuning

The built-in high-precision HIRC is factory calibrated to 16MHz @ 2.5V/25°C. The calibration process is to filter out the deviations in the manufacturing process that affect accuracy. This HIRC will also be affected by the working environment temperature and working voltage, and its frequency will drift to a certain extent.

In addition to factory calibration, a way for users to fine-tune HIRC is also provided: by rewriting the value of the FOSCCAL register.

The initial value of FOSCCAL ensures that HIRC operates at 16MHz after power-on. This value will vary on each IC. Let the initial value be FOSCCAL[s], at this time the chip is working at 16M, and the HIRC frequency changes by about 40kHz every time 1 LSb is changed. FOSCCAL[7:0]

The relationship with HIRC output is as follows:

FOSCCAL[7:0] value	HIRC actual output frequency (16M as an example)
FOSCCAL[s]-n	(16000-n*40)
.....
FOSCCAL[s]-2	16000-2*40=15920
FOSCCAL[s]-1	16000-1*40=15960
FOSCCAL[s]	16000
FOSCCAL[s]+1	16000+1*40=16040
FOSCCAL[s]+2	16000+2*40=16080
.....
FOSCCAL[s]+n	(16000+n*40)

3.4. Clock switching

By operating the System Clock Select (SCS) bit of the OSCCON register through software, the system clock source can be selected between the external and internal clocks.

Switch between sources.

3.4.1. System clock select (SCS) bit

The System Clock Select (SCS) bits of the OSCCON register select the system clock source for the CPU and peripherals.

When bit SCS of the OSCCON register = 0, the system clock source is configured by the FOSC<2:0> bits in the configuration word register (UCFG0).

placement decision.

When the bit SCS of the OSCCON register = 1, the internal oscillator frequency is selected according to the IRCF<2:0> bits of the OSCCON register.

Select the system clock source. After reset, the SCS bit in the OSCCON register is always cleared.

NOTE: Any hardware-induced clock switching (perhaps from two-speed boot or the failsafe clock monitor) will not update **OSCCON**

SCS bit of the register . The user should monitor the **OSTS** bit of the **OSCCON** register to determine the current system clock source.

3.4.2. Oscillator start-up timeout status (OSTS) bit

The Oscillator Start-Up Timeout Status (OSTS) bit of the OSCCON register indicates whether the system clock is coming from an external clock source or an internal clock source. external clock source. The external clock source is defined by FOSC<2:0> of the Configuration Word register (UCFG0). OSTS also specifically specifies that in LP or XT mode, whether the oscillator start-up timer (OST) has timed out.

3.5.Two -speed clock startup mode

Two-speed startup mode further saves power by minimizing the delay between external oscillator start-up and code execution. For applications that frequently use Sleep mode, Two-Speed Start-up mode will reduce the overall power consumption of the device by removing the external oscillator start-up time after the device wakes up. This mode enables an application to wake from Sleep, execute a few instructions using INTOSC as a clock source, and then return to Sleep without waiting for the main oscillator to stabilize.

Note: Executing the **SLEEP** instruction will terminate the oscillator start-up time and keep the **OSTS** bit in the **OSCCON** register clear.

When the oscillator module is configured in LP or XT mode, the Oscillator Start-up Timer (OST) is enabled (see Section 3.2.1 "Oscillator Start-up Timer"). The OST will pause program execution until 1024 oscillation counts are completed. Two-speed startup mode uses the internal oscillator to operate while the OST is counting, minimizing code execution latency. When the OST counts to 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

3.5.1.Double -speed startup mode configuration

Configure the two-speed startup mode through the following settings: \checkmark Bit IESO = 1 in the configuration word register (UCFG1); internal/external switch bit (enables the two-speed startup mode). \checkmark Bit SCS = 0 in the OSCCON register. \checkmark FOSC<2:0> in the configuration word register (CONFIG) is configured as LP or HS mode.

Enter the two-speed startup mode after the following operations: \checkmark Power-on reset (POR) and power-on delay timer (PWRT), after the delay ends (when enabled), or wakes up from sleep state.

If the external clock oscillator is configured in any mode other than LP or XT mode, Two-Speed Start-up is disabled. This is because The external clock oscillator does not require stabilization time after POR or when exiting from Sleep.

3.5.2. Two-speed starting sequence

1. Wake up from power-on reset or sleep 2. Use the internal oscillator to start executing instructions at the frequency set by the IRCF<2:0> bits of the OSCCON register 3. OST enabled, counting 1024 clock cycles
4. OST times out, waiting for the falling edge of the internal oscillator. 5. OSTS is set to 1. 6. The system clock remains low until the next falling edge of the new clock (LP or HS mode). 7. The system clock switches to the external clock source.

3.6. Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows continued operation of the device in the event of an external oscillator failure. FSCM can start the oscillator

An oscillator failure is detected at any time after the oscillation delay timer (OST) has expired. FSCM is configured by placing the configuration word register (UCFG1)

Set the FCMEN bit to 1 to enable. FSCM is available in all external oscillator modes (LP, HS and EC).

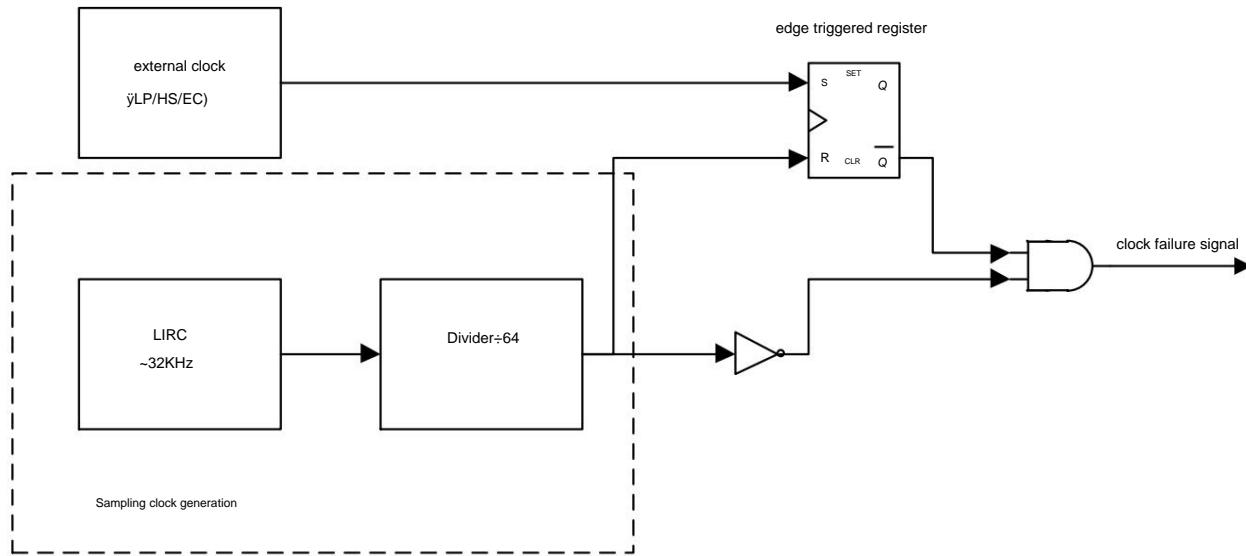


Figure 3.4 FSCM principle block diagram

3.6.1. Fault protection detection

The FSCM module detects oscillator failures by comparing the external oscillator to the FSCM sample clock. LIRC divided by 64 produces samples

clock. See Figure 3.4. There is a latch inside the fault detector. On each falling edge of the external clock, the latch is set. Sampling

On each rising edge of the clock, the latch is cleared. If a full half-cycle of the sample clock elapses without the master clock going low, a check

A fault was detected.

3.6.2. Failsafe operation

When the external clock fails, the FSCM switches the device clock to the internal clock source and sets the OSFIF flag bit in the PIR1 register.

If this flag is set at the same time as the OSFIE bit of the PIR1 register is set, an interrupt will be generated. The device firmware will then take steps to reduce

Minor problems that may be caused by a faulty clock. The system clock will continue to come from the internal clock source until the device firmware successfully restarts the external oscillator and switch back to external operation.

The internal clock source selected by FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to operate before a fault occurs can be configured.

3.6.3. Clearing fault protection conditions

The fault-safe condition is cleared after a reset, a SLEEP instruction, or toggling the SCS bit of the OSCCON register. After the SCS bit of the OSCCON register is modified, the OST will restart. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. After the OST times out, the fault-safe condition is cleared and the device will operate from the external clock source. The fault-safe condition must clear before the OSFIF flag can be cleared.

3.6.4. Reset or wake up from sleep

The FSCM is designed to detect an oscillator failure at any time after the Oscillator Start-Up Delay Timer (OST) has expired. The use cases for OST are after waking up from sleep and after any type of reset. OST cannot be used in EC clock mode, so once reset or wakeup is completed, FSCM is active.

Note: Due to the wide range of oscillator start-up times, the fault protection circuit is not active during oscillator start-up (when exiting reset or sleep). After an appropriate period of time, the user should check the **OSTS** bit of the **OSCCON** register to verify that the oscillator has started successfully and that the system clock has switched successfully.



3.7. Summary of registers related to clock source

Name	address	bit7		bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value
UCFG0	0x2000	CPDB		CPB	MCLRE	PWRTEB	WDTE	FOSC2		FOSC1	FOSC0
OSCCON	0x8F	LFMOD	IRCF2		IRCF1	IRCF0	OSTS	HTS	LTS	SCS	0101 x000
FOSCCAL	0x0D						HIRC trim bit				0110 1000
MSCON1	0x18	E				-			HIRCM		yyyy yyyy0

3.7.1. OSCCON register, address 0x8F

Bit	7	6	5	4	3	2	1	0
Name	LFMOD		IRCF[2:0]		OSTS	HTS	LTS	SCS
Reset	0		3'b100		x	0	0	0
TYPE	RW		RW		RO	RO	RO	RW

Bit	Name	Function																											
7	LFMOD	Frequency selection of LIRC (system clock is not affected by it) 0 = 32kHz 1 = 256kHz																											
6:4	IRCF[2:0]	Internal oscillator (system clock) frequency selection <table> <thead> <tr> <th>value</th> <th>2T mode</th> <th>4T mode</th> </tr> </thead> <tbody> <tr> <td>111</td> <td>16MHz</td> <td>8MHz</td> </tr> <tr> <td>110</td> <td>8MHz</td> <td>4MHz</td> </tr> <tr> <td>101</td> <td>4MHz</td> <td>2MHz</td> </tr> <tr> <td>100</td> <td>2MHz(default)</td> <td>1MHz(default)</td> </tr> <tr> <td>011</td> <td>1MHz</td> <td>500kHz</td> </tr> <tr> <td>010</td> <td>500kHz</td> <td>250kHz</td> </tr> <tr> <td>001</td> <td>250kHz</td> <td>125kHz</td> </tr> <tr> <td>000</td> <td>32kHz(LIRC)</td> <td>16kHz(LIRC/2)</td> </tr> </tbody> </table>	value	2T mode	4T mode	111	16MHz	8MHz	110	8MHz	4MHz	101	4MHz	2MHz	100	2MHz(default)	1MHz(default)	011	1MHz	500kHz	010	500kHz	250kHz	001	250kHz	125kHz	000	32kHz(LIRC)	16kHz(LIRC/2)
value	2T mode	4T mode																											
111	16MHz	8MHz																											
110	8MHz	4MHz																											
101	4MHz	2MHz																											
100	2MHz(default)	1MHz(default)																											
011	1MHz	500kHz																											
010	500kHz	250kHz																											
001	250kHz	125kHz																											
000	32kHz(LIRC)	16kHz(LIRC/2)																											
3	OSTS	Oscillator start-up timeout status bit 1 = The device is running on the external clock specified by FOSC<2:0> 0 = Device is running from the internal oscillator																											
2	HTS	High-speed internal clock status 1 = HIRC is ready 0 = HIRC is not ready																											
1	LTS	Low speed internal clock status 1 = LIRC is ready 0 = LIRC is not ready																											
0	SCS	System clock selection bit 1 = System clock selected is internal oscillator 0 = Clock source is determined by FOSC<2:0>																											



3.7.2. FOSCCAL register, address 0x0D

Bit	7	6	5	4	3	2	1	0
Name	FOSCCAL[7:0]							
Reset	0	1	1	0	1	0	0	0
TYPE	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	FOSCCAL on-chip HIRC clock calibration bit	

3.7.3. MSCON1 register, address 0x18E

Bit	7	6	5	4	3	2	1	0
Name	–							HIRC
Reset	–							0
TYPE	RO.0	RW						

Bit	Name	Function
7:1	N/A	Reserved bit, read 0
0	HIRC	<p>HIRC mode selection:</p> <p>0 = HIRC center frequency is 16MHz</p> <p>1 = HIRC center frequency is 13.5MHz</p> <p>Notice:</p> <p>When selecting the oscillation frequency of 13.5M, you need to save the value of FOSCCAL first, and then copy the value of SECCODE to FOSCCAL, to calibrate the 13.5M frequency;</p> <p>If you want to switch to the center frequency of 16M, you need to write the previously saved value back to FOSCCAL;</p>

4. Reset source

The FT62F13X has the following different resets:

- A) Power-on reset POR
- B) WDT (Watchdog) reset – during normal operation
- C) MCLRB pin reset – during normal operation
- D) MCLRB pin reset – during sleep
- E) Low voltage (BOR/LVR) reset
- F) Instruction error reset

Some registers are not affected by any reset; the status of these registers is unknown at power-on reset and is not affected by reset events.

Most other registers return to their "reset state" on a reset event, see the Register SFR table.

WDT (Watchdog) sleep wake-up will not cause the reset caused by WDT (Watchdog) timeout in normal operating state. Because sleep wakes up this book

Shen means continuation, not reset. Setting and clearing the /TF and /PF bits behave differently under different reset conditions. Tool

Please refer to Tables 4.1 and 4.2 for details.

The circuit of the MCLRB pin has an anti-shake function, which can filter out some sharp pulse signals caused by interference.

The figure below is a general overview block diagram of the reset circuit.

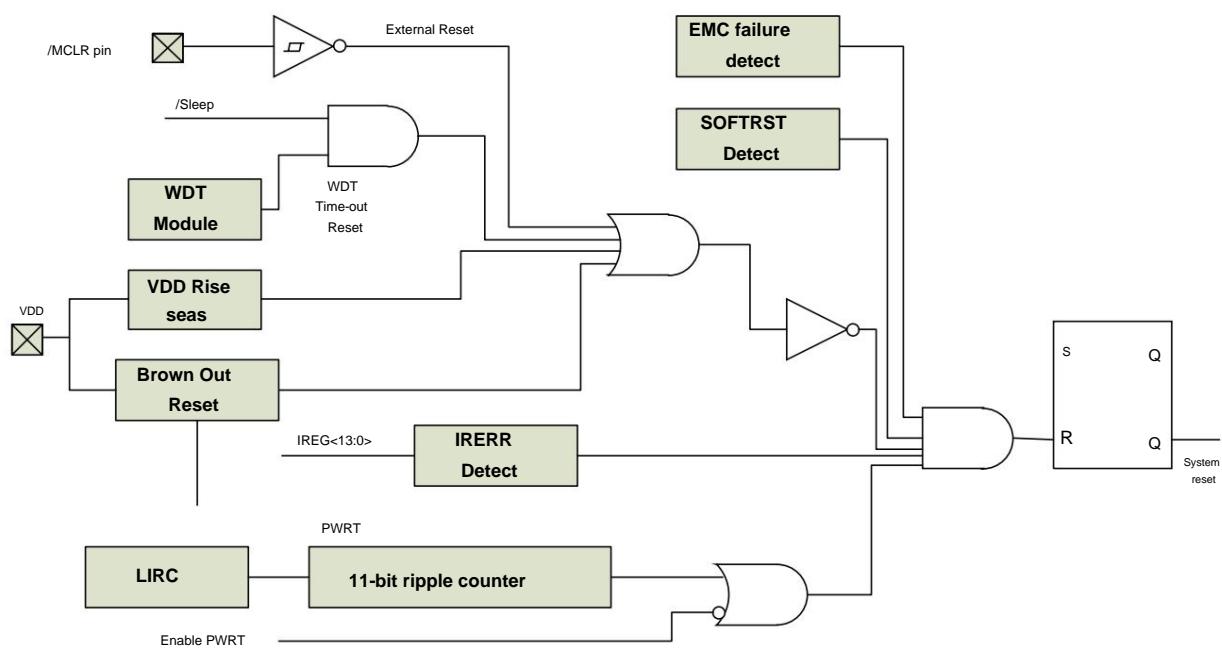


Figure 4.1 Reset block diagram

4.1. POR power-on reset

The on-chip POR circuit will keep the chip in reset until the VDD supply voltage reaches a high enough level. After power-on reset, the system reset will not be released immediately, and there will be a delay of about 8ms, during which the digital circuit remains in the reset state.

4.2. External reset MCLR

It should be noted that WDT reset will not pull the MCLRB pin low. Applying a voltage that exceeds the specification (such as an ESD event) on the MCLRB pin will cause an excessively large current to be generated on the pin. Therefore, we do not recommend that users directly connect MCLRB to VDD with a resistor. Instead, use the following circuit.

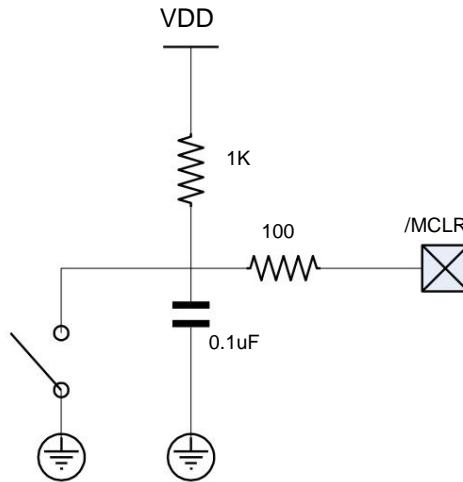


Figure 4.2 MCLRB reset circuit

There is a MCLRE enable bit in the chip's CONFIG OPTION register (UCFG0). Clearing this bit will cause the reset signal to be generated internally by the chip. When this bit is 1, the PB7/MCLRB pin of the chip becomes an external reset pin. In this mode, the MCLRB pin has a weak pull-up to VDD.

4.3. PWRT (power-on timer)

PWRT provides a fixed 64ms (under normal circumstances) timing for power-on reset and low-voltage reset. This timer is driven by the internal slow clock. The chip is held in reset until the timer expires. This period of time ensures that VDD rises to a high enough voltage for the system to operate normally. PWRT can also be enabled through the system CONFIG register (UCFG0). When turning on the low voltage reset function, the user should also turn on PWRT. The PWRT timing is initiated by an event where the VDD voltage exceeds the VBOR threshold. In addition, it should be noted that since it is driven by an internal slow clock, the actual length of timing changes with changes in temperature, voltage and other conditions. This time is not a precise parameter.

4.4. BOR low voltage reset

The low-voltage reset is controlled by the UCFG1<1:0> bits and the SLVREN bit of MSCON0. Low voltage reset refers to the reset generated when the power supply voltage is lower than the VBOR threshold voltage. However, when the VDD voltage is lower than VBOR for no more than TBOR time, the low voltage reset will not occur.

The VBOR voltage needs to be calibrated before the chip is shipped. The calibration can be completed by writing to the internal calibration register through the serial port.

If BOR (low voltage reset) is enabled (UCFG1<1:0>=00), then the maximum VDD voltage rise time requirement does not exist.

The BOR circuit will control the chip in the reset state until the VDD voltage reaches above the VBOR threshold voltage. It should be noted that when VDD is lower than the threshold for normal operation of the system, the POR circuit does not generate a reset signal.

When UCFG1<1:0>=10, the BOR circuit shutdown will be determined by the running status of the CPU: the BOR circuit works when the CPU is working normally, and the BOR circuit is shut down when the CPU is in sleep mode, which can conveniently reduce the system power consumption to a minimum. level.

4.5. LVD low voltage detection

In addition to the low voltage reset function, the chip also has a built-in low voltage detection function. When the power supply voltage is lower than the set voltage level (selected by LVDL<3:0> of PCON) for more than TBOR (3 to 4 slow clock cycles), the flag bit LVDW will be set to 1, and the software can use this bit to monitor the supply voltage. If the power supply voltage is greater than the voltage level set by LVDL, this flag will be automatically cleared. In other words, the LVDW bit does not have a latch function.

4.5.1. Detect external voltage

In addition to monitoring the on-chip VDD, the LVD module also has the function of detecting external voltage. The register bit LVDM determines whether the LVD acts on VDD or an external voltage. When EVLDx is selected to be detected, the Schmitt input of the corresponding pin is turned off to prevent leakage. Note: 1. The voltage of the ELVD pin cannot be higher than VDD.

4.6. Error command reset

When the CPU's instruction register fetches an illegal instruction, the system will be reset. Using this function can increase the system's anti-interference capability.

4.7. Timeout action

During the power-on process, the internal timeout action sequence of the chip is executed according to the following process: a) After the POR is completed, start the 8ms timing b) Start the chip configuration process (BOOT) c) Start the PWRT timing (if enabled)

4.7.1. PCON register

There are 2 bits in the PCON register indicating which reset occurred. Bit0 is the /BOR indication bit, which is in an unknown state during power-on reset. The software must be set to 1 and then checked to see if it is 0. Bit1 is the /POR indication bit, which is 0 after power-on reset, and the software must set it to 1.

4.8. Power-on configuration process

After a power-on reset or low-voltage reset occurs, in addition to the inherent 8ms reset delay, there is also an initialization configuration register UCFGx. This action reads the content from the reserved address of the PROM and writes it to UCFGx. The system can be released only after all configuration addresses have been read. System reset, as shown in Figure 4.2 and Figure 4.3, this process takes about 17us.

4.9. Power-on verification process

If UCFG1.6(CSUMENB) is 0, after the power-on configuration process is completed, the CPU will not execute the program immediately, but will start the PROM internal verification process. The hardware will read out the contents of the main program area of the PROM and add it automatically. After all 3k words have been accumulated, they will be summed up and stored in 0x2007. Comparing the values, if they are equal, it means the verification is successful, and the CPU will execute the program from address 0, as shown in Figure 4.4; if they are not equal, it means the verification failed. If it fails, the CPU will not execute the program. The verification process takes about 3ms.

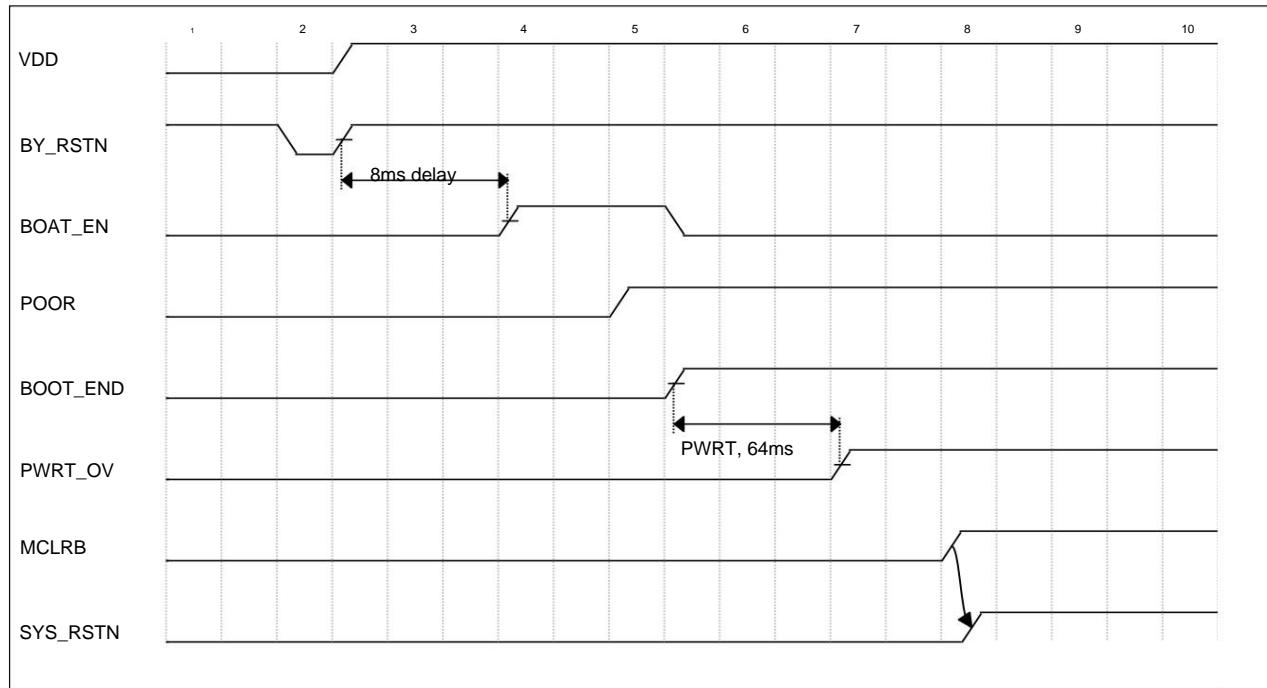


Figure 4.3 Power-on reset, using MCLRB

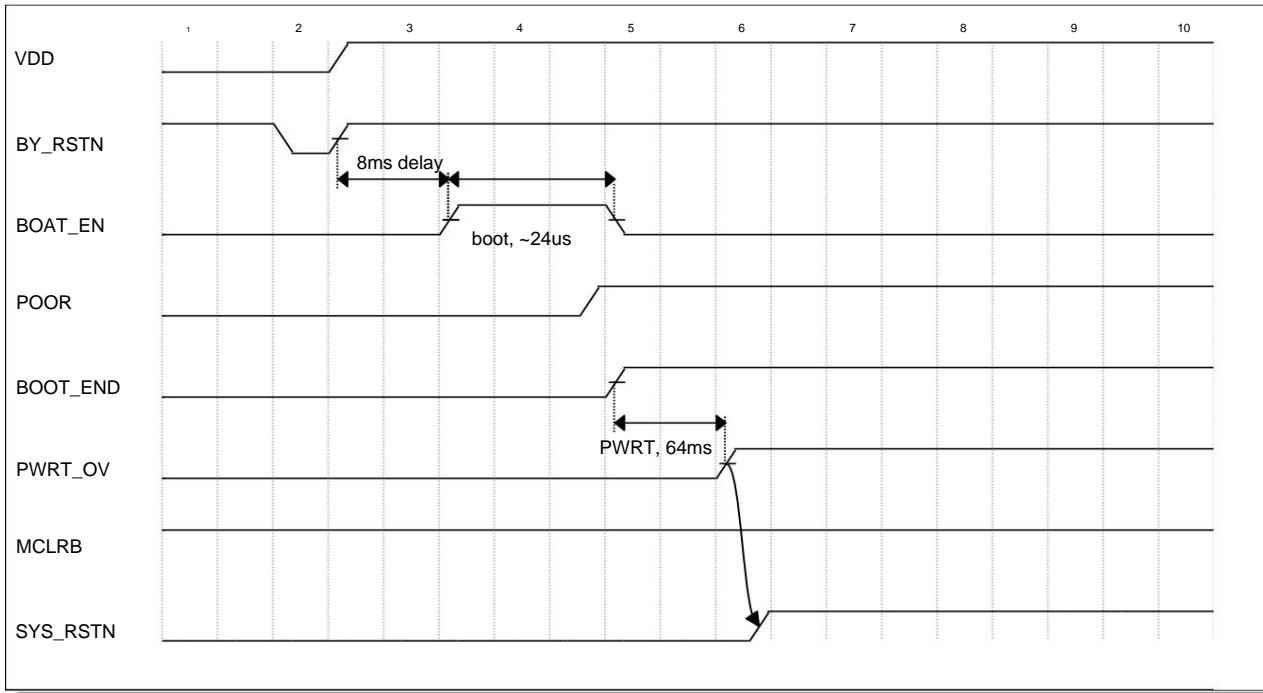


Figure 4.4 Power-on reset, MCLRB is not used

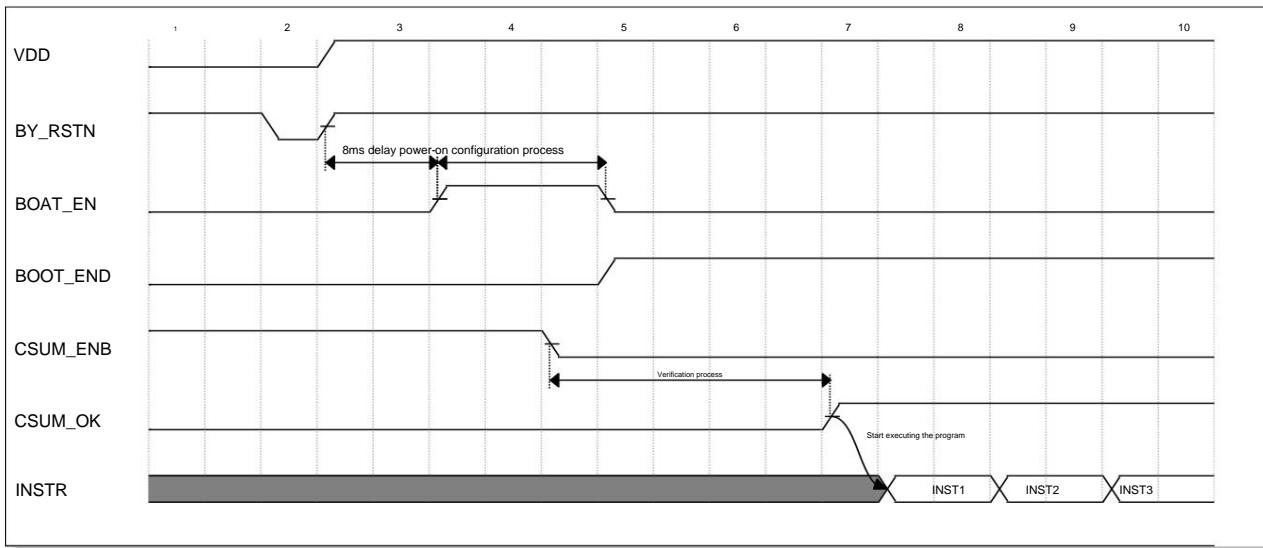


Figure 4.5 Verification process

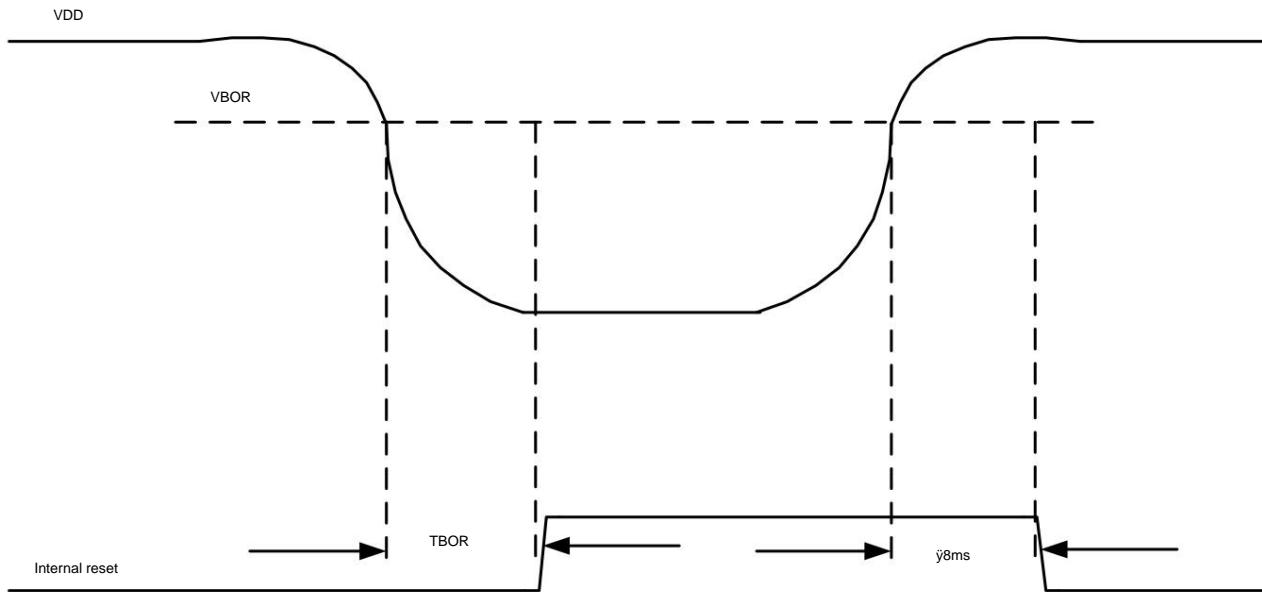


Figure 4.6 BOR reset

Notice:

1. After power-on reset or low-voltage reset, and when PWRTEB (UCFG0.4) is low, PWRT is valid. It is within 2048

The slow clock cycle is about 64ms;

2. TBOR time is about 122–152us;

3. After the voltage returns to normal, the internal reset will not be released immediately, but will have to wait for about 8ms .

Oscillator configuration	Power on reset		low voltage reset		wake up from sleep
	/PWRTEB=0	/PWRTEB=1	/PWRTEB=0	/PWRTEB=1	
INTOSC	TPWRT	—	TPWRT	—	—

Table 4.1 Timeout in various situations

/BY /BOR		/TF	/PF	condition
0	x	1	1	BY
in	0	1	1	There is
in	in	0	in	WDT reset
in	in	0	0	WDT wake up
in	in	in	in	MCLRB reset during normal operation
in	in	1	0	MCLRB reset during sleep

Table 4.2 STATUS/PCON bits and their meanings (u-no change x-unknown)

4.10. PCON register, address **0x8E**

Bit	7	6	5	4	3	2	1	0
Name	LVDL[3:0]				LVDEN	LVDW	/BY	/THERE IS
Reset	0	0	0	0	0	x	q	q
Type	RW	RW	RW	RW	RW	RO	RW	RW

Bit	Name	Function
7:4	LVDL	<p>Low voltage detection selection bit</p> <p>value detection voltage</p> <p>0000: Reserved</p> <p>0001: 2.0V</p> <p>0010: 2.4V</p> <p>0011: 2.7V</p> <p>0100: 3.0V</p> <p>0101: 3.3V</p> <p>0110: 3.6V</p> <p>0111: 4.0V</p> <p>1xxx: 1.2V</p>
3	LVDEN	<p>Low voltage detection enable</p> <p>1: Turn on LVD detection function</p> <p>0: Turn off LVD detection function</p>
2	LVDW	<p>Low voltage flag, read only</p> <p>When LVDP=0:</p> <p>1: VDD dropped to the voltage set by LVDL[2:0] for more than TBOR</p> <p>0: VDD is higher than the voltage set by LVDL[2:0]</p> <p>When LVDP=1:</p> <p>1: VDD is higher than the voltage set by LVDL[2:0], and the time exceeds TBOR</p> <p>0: VDD dropped to the voltage set by LVDL[2:0]</p> <p>Note: When LVDP and LVDEN are 1 at the same time, LVDW is fixed to 1 and LVDIF is also set to 1.</p>
1	/BY	<p>Power-on reset flag, active low</p> <p>0: A power-on reset occurred</p> <p>1: No power-on reset occurs or is set to 1 by software</p> <p>/POR has a value of 0 after power-on reset, and software should set it to 1 thereafter.</p>
0	/THERE IS	<p>Low voltage reset flag, active low</p> <p>0: A low voltage reset has occurred</p> <p>1: No low voltage reset occurs or is set to 1 by software</p> <p>/BOR has an undefined value after power-on reset and must be set to 1 by software. After a subsequent reset occurs, query this bit to determine if the battery is low pressure reset</p>

4.11. LVDCON register, address 0x110

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	LVDP	LVDDEB	LVDM[2:0]		
Reset	0	0	0	0	1	1	0	0
Type	RO.0	RO.0	RO.0	RW	RW	RW	RW	RW

Bit	Name	Function
7:5	N/A	Reserved bit, read 0
4	LVDP	<p>LVDW polarity selection, reset value is 0</p> <p>1: LVDW flag indicates that VDD is higher than the set threshold</p> <p>0: LVDW flag indicates that VDD is lower than the set threshold</p>
3	LVDDEB	<p>Whether the LVD level output passes through the debounce circuit</p> <p>1: After debounce circuit</p> <p>0: Without debounce circuit</p>
2:0	LVDM	<p>LVD detection source selection</p> <p>000:PB6</p> <p>001:PB5</p> <p>010:PA1</p> <p>011:PA0</p> <p>100:VDD</p> <p>101/110/111: Reserved</p>

4.12. LVDTRIM register, address 0x19F

Bit	7	6	5	4	3	2	1	0
Name	-	LVDADJ[3:0]				LVRADJ[2:0]		
Reset	0	1	0	0	0	0	1	1
Type	RO	RW	RW	RW	RW	RO	RO	RO

Bit	Name	Function
7	N/A	Reserved bit, read 0
6:3	LVDAJ	<p>LVD trimming position, power-on reset value 1000</p> <p>3% / step</p>
2:0	LVRADJ	Read only, LVR accuracy adjustment register, power-on reset value is 011



4.13. Configuration register summary

4.13.1. UCFG0, PROM address **0x2000**

Bit	7	6	5	4	3	2	1	0
Name	CPDB	CPB	MCLRE PWRTEB		WDTE	DARK[2:0]		
BY val.	1	1	0	1	0	111		

Bit	name	describe
7	CPDB	DROM code protection bit 1: DROM content is not protected 0: Enable DROM content protection, MCU can read, but serial port cannot read Notice: 1. This bit can only be rewritten from 1 to 0, but not from 0 to 1. The only way to rewrite from 0 to 1 is to include Chip erase operation including USER_OPT, and CPDB will not change to 1 until power is turned on again. 2. In the case of DROM protection, the DROM will be automatically erased after the full chip erase is completed.
6	CPB	Flash full area (4K words) protection settings 1: No full area protection for Flash 0: Enable Flash full area protection, except for CPU instruction fetch, CPU or external serial port reads return 0 Notice: This bit can only be rewritten from 1 to 0, but not from 0 to 1. The only way to rewrite from 0 to 1 is to include Chip erase operation including USER_OPT, and CPB will not change to 1 until power is turned on again.
5	MCLRE	1:PB7/MCLR is the reset pin function 0:PB7/MCLR pin is GPIO
4	PWRTEB	1:PWRTE prohibited 0:PWRTE enabled
3	WDTE	1: WDT is enabled and cannot be disabled by the program. 0: WDT is disabled, but the program can enable WDT by setting the SWDTEN bit of WDTCON
2:0	DARK	000: LP crystal oscillator mode, PC0/PC1 is connected to a low-speed crystal 001: HS crystal oscillator mode, PC0/PC1 connected to high-speed crystal 010: External clock mode, PC0 is the IO function, PC1 is connected to the clock input 011: INTOSC mode, PB0 (PA2) outputs the system clock divided by 2, PC1 is the IO pin 1xx:INTOSCIO mode, PC0 is IO pin, PC1 is IO



4.13.2. UCFG1, PROM address 0x2001

Bit	7	6	5	4	3	2	1	0
Name	— CSUMEB		TSEL	FCMEN	IESO	RDCTRL	LVREN[1:0]	
BY val.	RO.0	1	1	1	1	0	11	

Bit	name	describe
7	N/A	Reserved bit
6	CSUMEB	<p>Checksum enable 1: Disable checksum function 0: Enable the checksum function. After the boot is completed, the hardware automatically adds the contents of all units in the 2K PROM space, and the result is the same as 0x2007 Compare the unit contents. If they are equal, the verification is successful; if the verification fails, the CPU will not execute the program.</p>
5	TSEL	<p>Instruction cycle select bit 1: The instruction cycle is 2T 0: Instruction cycle is 4T</p>
4	FCMEN	<p>Clock failure monitoring enabled 1: Enable clock failure monitoring 0: Disable clock failure monitoring</p>
3	IESO	<p>Two-speed clock enable 1: Enable two-speed clock mode 0: Disable two-speed clock mode</p>
2	RDCTRL	<p>Read port control in output mode 1: Read the value on PAD returned by the data port 0: Read the value on the Latch returned by the data port</p>
1:0	LVREN	<p>Low voltage reset option 00: Enable low voltage reset 01:LVR is determined by SLVREN of MSCON0 10: The MCU turns on LVR in normal mode and turns off LVR in sleep mode. It has nothing to do with the SLVREN bit. 11: Disable low voltage reset</p>

4.13.3. UCFG2, PROM address 0x2002

Bit	7	6	5	4	3	2	1	0
Name	-	DRILL	MRBTE WDTBTE		LVRS[3:0]			
BY val.	1	0	0	0	4'b0000			

Bit	name	describe
7	N/A	Reserved bit
6	DRILL	IRERR reset BOOT enable bit 0 = Disable incorrect instruction reset to generate BOOT 1 = Allow error instruction reset to generate BOOT
5	MRBTE	MCLR reset BOOT enable bit 0 = Disable MCLR reset to generate BOOT 1 = Allow MCLR reset to generate BOOT
4	WDTBTE	WDT reset BOOT enable bit 0 = Disable WDT reset to generate BOOT 1 = Allow WDT reset to generate BOOT
3:0	LVDS	Low voltage reset threshold selection numerical voltage 1010: Reserved 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved 0000: Reserved 0001: Reserved 0010: Reserved 0011: 2.0V 0100: 2.2V 0101: 2.5V 0110: 2.8V 0111: 3.1V 1000: 3.6V 1001: 4.1V



4.13.4. UCFG3, PROM address 0x2003

Bit	7	6	5	4	3	2	1	0
Name	-					SECPB2	SECPB1	SECPB0
BY val.	RO.0	RO.0	RO.0	RO.0	RO.0	1	1	1

Bit	name	describe
7:3	N/A reserved bit, needs to be kept at 1	
2:0	SECP2/1/0	<p>PROM sector protection control bit, active low. 1 sector=1kW, each bit controls one sector</p> <p>SECPx value:</p> <p>0 = Sector x is protected, the serial port cannot read or program, only erase</p> <p>1 = Sector x is not protected</p>

4.13.5. MAINCSUM (Address: 0x2007)

Bit	7	6	5	4	3	2	1	0
Name	-					MAINCSUM[3:0]		
BY val.	RO.0	RO.0	RO.0	RO.0	x	x	x	x

Bit	name	describe
7:4	N/A	Reserved bit, read 0
3:0	MAINCSUM 4-digit checksum	of the 3K main program area, which is determined by the host computer when burning the program.

After the power-on configuration process (BOOT) is completed, when the CSUMEB of Config1 is 0, the hardware will enter all units in the 3K main program area.

Rows add up. After completing the addition operation of the last word (address 0xBFF), the accumulated result is compared with the value of MAINCSUM. If

If the two are equal, the verification is successful. Otherwise, the verification fails and the reset module will generate a reboot reset.

5.Watchdog timer

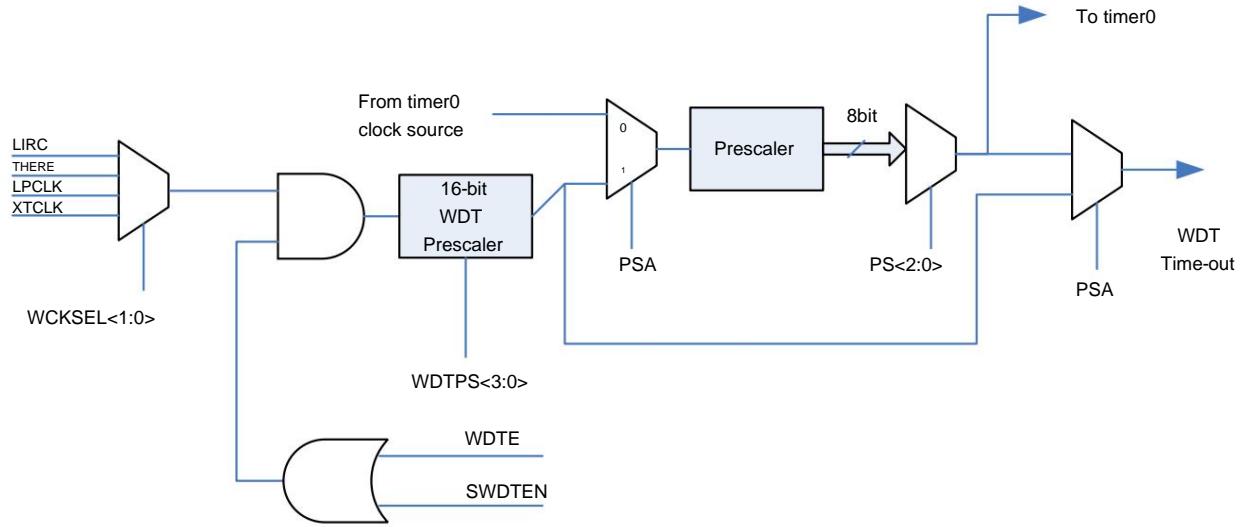


Figure 5.1 Watchdog and Timer 0 block diagram

5.1.Watchdog

The watchdog is a 16-bit counter that shares an 8-bit prescaler with timer 0. The hardware enable bit WDTEN is located in the configuration register.

Bit 3 of register UCFG0, software enable bit SWDTEN is located at bit 0 of WDTCON register. When it is 1, it means the watchdog is enabled.

Dog, disabled when 0.

Clear watchdog instructions CLRWDT and SLEEP will clear the watchdog counter.

When the watchdog is enabled, the watchdog overflow event can be used as a wake-up source when the MCU is sleeping, and as a wake-up source when the MCU is working normally.
a reset source.

condition	watchdog status
WDTEN and SWDTEN are 0 at the same time	
CLRWDT instruction	Clear
Enter SLEEP, exit SLEEP time	
When OST count overflows	
Write WDTCON	

5.2.Watchdog clock source

The watchdog clock sources include the following:

- ÿ LIRC
- ÿ HIRC
- ÿ LP crystal clock
- ÿ XT crystal clock

When the watchdog is enabled, the selected clock source will automatically turn on and will remain running in SLEEP mode.

Notice:

1. When selecting **LP** as the WDT clock source, the configuration option **FOSC** must be in **LP** or **INTOSCIO** mode. Otherwise, the LP crystal transistor

The road will not be open;

2. Similarly, when selecting **XT** as the WDT clock source, the configuration option **FOSC** must be **XT** or **INTOSCIO** mode, otherwise, XT

The crystal circuit will not open;

5.3. Summary of registers related to watchdog

name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value
WDTCON 0x18 —			WCKSRC[1:0]		WDTPS[3:0]			SWDTEN	ÿ000 1000	
UCFG0 0x2000 CPDB			CPB	MCLRE PW	RTEB WDTE		DARK[2:0]			1100 0111
OPTION	0x81	/PAPU	INTEDG T0GS		T0SE	PSA	PS[2:0]			1111 1111



5.3.1. WDTCON register, address 0x18

Bit	7	6	5	4	3	2	1	0
Name	Reserved	WCKSRC[1:0]		WDTPS[3:0]				SWDTEN
Reset	0	0	0	0	1	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function																																
7	Reserved	Reserved bit																																
6:5	WCKSRC	<p>Watchdog clock source selection 00 = LIRC(256k or 32k) 01 = HERE 10 = LP crystal clock, only meaningful when FOSC is configured in LP or INTOSCIO mode 11 = XT crystal clock, only meaningful when FOSC is configured in XT or INTOSCIO mode</p>																																
4:1	WDTPS	<p>WDTPS<3:0>: Watchdog timer period selection: Bit Value = Prescaler ratio of the watchdog timer driving clock</p> <table> <tr><td>0000</td><td>= 1:32</td></tr> <tr><td>0001</td><td>= 1:64</td></tr> <tr><td>0010</td><td>= 1:128</td></tr> <tr><td>0011</td><td>= 1:256</td></tr> <tr><td>0100</td><td>= 1:512 (reset value)</td></tr> <tr><td>0101</td><td>= 1:1024</td></tr> <tr><td>0110</td><td>= 1:2048</td></tr> <tr><td>0111</td><td>= 1:4096</td></tr> <tr><td>1000</td><td>= 1:8192</td></tr> <tr><td>1001</td><td>= 1:16384</td></tr> <tr><td>1010</td><td>= 1:32768</td></tr> <tr><td>1011</td><td>= 1:65536</td></tr> <tr><td>1100</td><td>= 1:65536</td></tr> <tr><td>1101</td><td>= 1:65536</td></tr> <tr><td>1110</td><td>= 1:65536</td></tr> <tr><td>1111</td><td>= 1:65536</td></tr> </table>	0000	= 1:32	0001	= 1:64	0010	= 1:128	0011	= 1:256	0100	= 1:512 (reset value)	0101	= 1:1024	0110	= 1:2048	0111	= 1:4096	1000	= 1:8192	1001	= 1:16384	1010	= 1:32768	1011	= 1:65536	1100	= 1:65536	1101	= 1:65536	1110	= 1:65536	1111	= 1:65536
0000	= 1:32																																	
0001	= 1:64																																	
0010	= 1:128																																	
0011	= 1:256																																	
0100	= 1:512 (reset value)																																	
0101	= 1:1024																																	
0110	= 1:2048																																	
0111	= 1:4096																																	
1000	= 1:8192																																	
1001	= 1:16384																																	
1010	= 1:32768																																	
1011	= 1:65536																																	
1100	= 1:65536																																	
1101	= 1:65536																																	
1110	= 1:65536																																	
1111	= 1:65536																																	
0	SWDTEN	<p>Software turns on/off the watchdog timer: 1 = open 0 = off</p>																																

6. Interruption

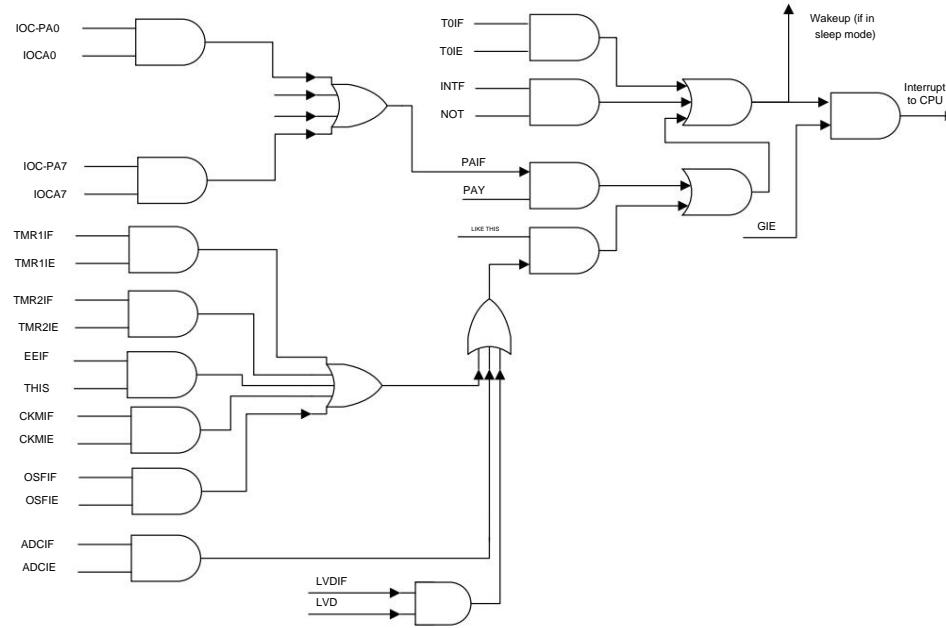


Figure 6.1 Interrupt logic block diagram

FT62F13x has the following interrupt sources, some of which can wake the CPU from sleep state:

- ÿ ADC interrupt
- ÿ External interrupt coming from PA4/INT pin
- ÿ Timer0 overflow interrupt
- ÿ PORTA level change interrupt
- ÿ Timer2 match equal interrupt
- ÿ Timer1 match equal interrupt
- ÿ EEPROM data write interrupt
- ÿ Clock missing interrupt
- ÿ LVD interrupt

The interrupt control register (INTCON) and the peripheral interrupt request register (PIR1) record the mid-end flag bit. INTCON also contains

Global interrupt enable bit GIE.

When the interrupt is serviced, the following actions occur automatically:

- ÿ GIE is cleared, thereby turning off interrupts
- ÿ The return address is pushed onto the stack
- ÿ The program pointer loads the 0004h address

Interrupt return instruction, RETI will set the GIE bit when exiting the interrupt function and re-enable unmasked interrupts. It should be noted that executing

The relevant interrupt flag bit should be cleared to 0 before the interrupt returns to RETI to avoid repeatedly entering the interrupt handler.

The INTCON register contains the following interrupt flag bits:

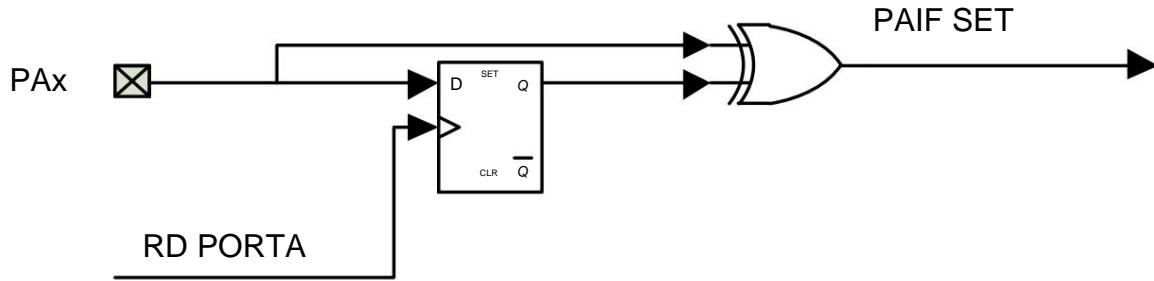
- ÿ INT pin interrupt
- ÿ PORTA change interrupt
- ÿ Timer0 overflow interrupt

PIR1 contains the peripheral interrupt flag bit, and PIE1 contains its corresponding interrupt enable bit. For details, please refer to the description of each register bit.

6.1. INT external interrupt

The external interrupt on the INT pin is edge-triggered: on the rising edge when the INTEDG bit of the OPTION register is set, and on the falling edge when the INTEDG bit is cleared. When a valid edge occurs on the INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the interrupt service routine before the interrupt can be re-enabled. If the INTE bit is set before entering Sleep state, the INT pin interrupt can wake the processor from Sleep state.

6.2. Port change interrupt



6.2 Principle block diagram of port change interrupt

A change in the PORTA input level sets the PAIF bit of the INTCON register to 1. This interrupt can be enabled/disabled by setting/clearing the PAIE bit of the INTCON register. In addition, individual pins of this port can be configured through the IOCA register.

Note:

1. When initializing the level change interrupt, you should first configure it as a digital input IO, set the corresponding **IOCA** to 1, and then read the **PORTA**;
2. When the I/O level changes, PAIF is set to 1;
- 3.

Before clearing the interrupt flag bit, PORTA should be read, and then **PAIF** should be cleared to 0;

6.2.1. Clearing the PAIF flag

The PAIF register bit is set asynchronously, that is, if the port mismatch event persists, software cannot complete its clearing operation. To clear it to 0, there are two methods: Method 1 a)

Wait for

the external pin to return to its original level b)

Software clears PAIF

Method

2 a) Read PORTA and actively clear mismatch events b)

Software clears PAIF

6.3. Interrupt response

The delay of external interrupts, including those from the INT pin or PORTA change interrupts, is generally 1 to 2 instruction cycles. It is related to when an interrupt occurs

The moment is related to the instruction being executed.

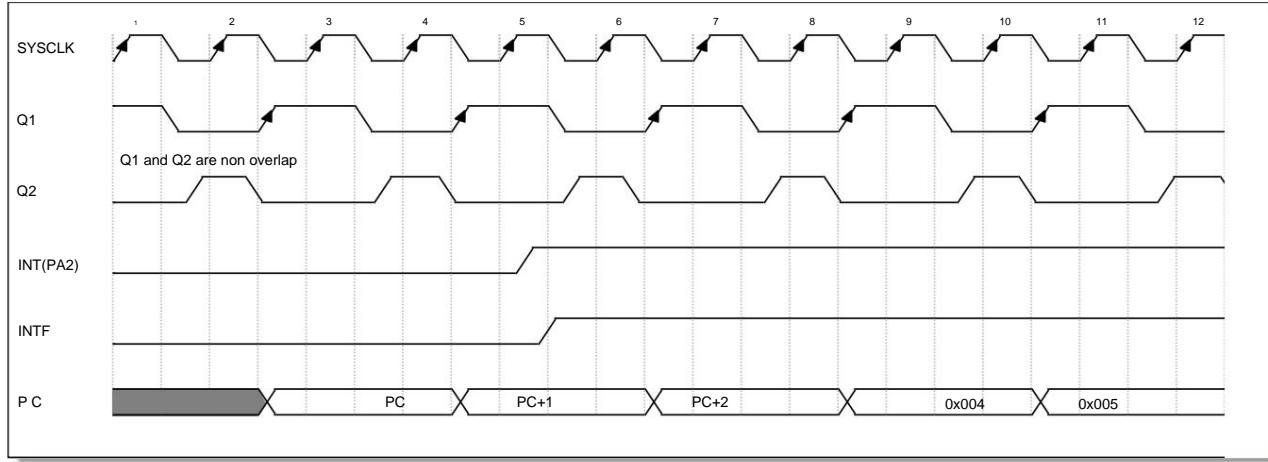


Figure 6.3 Interrupt response timing diagram

6.4. On-site saving during interruption

During an interrupt, only the return PC is automatically saved on the stack. Generally speaking, users may need to save important register values in the heap

On the stack, such as W, STATUS register, etc. These must be done by software. Temporary registers W_TEMP and STATUS_TEMP

Should be placed in the last 16bytes of the GPR. These 16 GPRs fall in various page intervals, so you can save a little code.

6.5. About interrupt flags

The interrupt flag bits of all peripherals are independent of their interrupt enable (enable) bits. Even if each interrupt enable bit is 0 and a related interrupt event occurs, its flag will still be set to 1.

6.6. Summary of interrupt-related registers

Name	Address	bit7		bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value
INTCON	0x0B	GIE	LIKE THIS	TOIE	NOT	PAY	TOIF	INTF	PAIF	0000 0000	
PIE1	0x8C	THIS	CKMIE	LVDIE	ACMPIE	TMR1IE	OSFIE	TMR2IE		ADCIE	0000 0000
PIR1	0x0C	EEIF	CKMIF	LVDIF	ACMPIF	TMR1IF		OSFIF	TMR2IF	ADCIF	0000 0000
TRISA	0x85			TRISA[7:0], PORTA direction control						1111 1111	
JOKE	0x96			IOCA[7:0], port change interrupt enable bit						0000 0000	

6.6.1. INTCON register, address 0x0B/0x8B

Bit	7	6	5	4	3	2	1	0
Name	GIE	LIKE THIS	TOIE	NOT	PAY	TOIF	INTF	PAIF
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	GIE	GIE: global interrupt enable 1 = Enable all unmasked interrupts 0 = disable all interrupts
6	LIKE THIS	PEIE: Peripheral interrupt enable 1 = Enable all unmasked peripheral interrupts 0 = Disable all peripheral interrupts
5	TOIE	TOIE: Timer 0 overflow interrupt enable 1 = Enable Timer0 interrupt 0 = disable Timer0 interrupt
4	NOT	INTE: External interrupt enable 1 = Enable PC1/INT external interrupt 0 = Disable PC1/INT external interrupt
3	PAY	PAIE: PORTA level interrupt enable bit 1 = Enable PORTA change interrupt 0 = Disable PORTA change interrupt
2	TOIF	TOIF: Timer 0 overflow interrupt flag bit 1 = Timer0 register has overflowed (must be cleared in software) 0 = Timer0 register did not overflow
1	INTF	INTF: PA4/INT external interrupt flag bit 1 = PA4/INT external interrupt occurred (must be cleared in software) 0 = PA4/INT external interrupt has not occurred
0	PAIF	PAIF: PORTA level change interrupt flag bit 1 = At least one PORTA<7:0> pin has changed state (must be cleared in software) 0 = None of the PORTA<7:0> pins changed state



6.6.2. PIR1 register, address 0x0C

Bit	7	6	5	4	3	2	1	0
Name	EEIF	CKMIF	LVDIF	ACMPIF	TMR1IF	OSFIF	TMR2IF	ADCIF
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	EEIF	EEIF: EE write interrupt flag bit 1 = EE write operation completed 0 = EE write operation is not completed or has been cleared by software
6	CKMIF	CKMIF: Fast clock measurement slow clock operation completion interrupt flag bit 1 = Fast clock measurement slow clock operation completed 0 = Fast clock measurement of slow clock has not completed, or has been cleared by software
5	LVDIF	LVDIF: LVD interrupt flag bit 1 = LVD detection voltage is below the set threshold 0 = LVD detection voltage is higher than the set threshold, or has been cleared by software.
4	ACMPIF	ADC threshold comparison interrupt flag bit 1 = ADC threshold comparison result is higher than preset value 0 = ADC threshold comparison result is lower than the preset value, or has been cleared by software.
3	TMR1IF	TMR1IF: Timer1 and PR1 compare equal interrupt flag bit 1 = The value of Timer1 is equal to PR1 0 = The value of Timer1 is not equal to PR1, or has been cleared by software.
2	OSFIF	Oscillator fault interrupt flag bit 1 = System oscillator failed, clock input switched to INTOSC 0 = The system clock is running normally or has been cleared by software.
1	TMR2IF	TMR2IF: Timer2 and PR2 compare equal interrupt flag bit 1 = The value of Timer2 is equal to PR2 0 = The value of Timer2 is not equal to PR2, or has been cleared by software.
0	ADCIF	ADC conversion complete interrupt flag bit 1 = ADC conversion completed 0 = ADC conversion is not complete or has been cleared by software

6.6.3. PIE1 register, address 0x8C

Bit	7	6	5	4	3	2	1	0
Name	THIS	CKMIE	LVD	ACMPIE	TMR1IE	OSFIE	TMR2IE	ADCIE
Reset	0	0	0	0	0	0	0	0
TYPE	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	THIS	EE write interrupt enable bit 1 = Enables EE write completion interrupt 0 = Turn off EE write operation complete interrupt
6	CKMIE	Fast clock measurement slow clock operation complete interrupt enable bit 1 = Enable fast clock measurement slow clock operation complete interrupt 0 = Turn off the fast clock measurement slow clock operation completion interrupt
5	LVD	Key interrupt enable bit 1 = Enable key interrupt 0 = disable key interrupt
4	ACMPIE	ADC threshold comparison result interrupt enable bit 1 = ADC threshold compare interrupt enabled 0 = Turn off ADC threshold compare interrupt
3	TMR1IE	Timer1 and PR1 compare equal interrupt enable bit 1 = Enable match interrupt for Timer1 0 = Turn off Timer1 match interrupt
2	OSFIE	Oscillator fault interrupt enable bit 1 = Oscillator fault interrupt enabled 0 = Oscillator fault interrupt disabled
1	TMR2IE	Timer2 and PR2 compare equal interrupt enable bit 1 = Enable match interrupt for Timer2 0 = Turn off Timer2 match interrupt
0	ADCIE	ADC conversion complete interrupt enable 1 = ADC conversion interrupt enabled 0 = ADC conversion interrupt disabled

6.6.4. IOCA register, address 0x96

Bit	7	6	5	4	3	2	1	0
Name	JOKE [7:0]							
Reset	0x00							
Type	RW							

Bit	Name	Function
7:0	JOKE	Port change interrupt setting 1 = Enable port change interrupt 0 = disable port change interrupt



7. Sleep mode

The device enters sleep mode by executing the SLEEP instruction.

When entering sleep mode, the state of the MCU is as

follows: 1. The WDT will be cleared but will keep running (if enabled to operate during sleep) 2.

The PD bit of the STATUS register is cleared 3. The

TO bit of the STATUS register is set to 1 4. CPU

clock Stop 5. The 32kHz LIRC

is not affected, and peripherals clocked by it can continue to operate in Sleep mode 6. The LP crystal oscillator is not affected

(when the TIMx uses it as the operating clock) 7. The ADC is not affected (If dedicated FRC clock is

selected) 8. The I/O port remains in the state before executing the SLEEP

instruction (driven to high level, low level or high impedance state) 9. Reset other than WDT is not affected by sleep mode

See the individual chapters for more details on peripheral operation during sleep.

To minimize current consumption, the following conditions should be

considered: 1. The I/O pin should not be left floating, and the internal pull-up or pull-down can be turned

on when the I/O is used as an input. 2. The

external circuit sinks current from the I/O pin. 3.

Internal circuitry sources current

from I/O pins 4. Internal weak pull-up pins

5. Module uses 31kHz LIRC 6. Module uses LP oscillator

7.1. Wake-up mode

The following events can wake up

the chip: ý External reset on MCLRB pin ý BOR

reset (if enabled) ý POR reset ý WDT

timeout ý Any external

interrupt ý Interrupt generated

by peripherals capable of

running during sleep (more information please See individual peripherals)

The first three events will reset the device, and the last three events are considered a continuation of program execution.

Clear watchdog instructions CLRWDT, SLEEP (enter sleep mode) or wake up from sleep mode will clear the watchdog counter.

7.2. Watchdog wake-up

The watchdog works on the internal slow clock (32kHz), which is a 16-bit counter and shares an 8-bit prescaler with timer 0.

The enable bit is located in bit 3 of the configuration register UCFG0, WDTEN. When it is 1, it means the watchdog is enabled. When it is 0, it will be set by the SWDTEN bit.

To determine whether to enable or not, SWDTEN is located in the WDTCON register.

Clear watchdog instructions CLRWDT and SLEEP will clear the watchdog counter.

When the watchdog is enabled, the watchdog overflow event can be used as a wake-up source when the MCU is sleeping, and as a wake-up source when the MCU is working normally. a reset source.

7.3. Interrupt wake-up

When waking up from an interrupt, the CPU first enters the interrupt handler, exits the interrupt, and then executes the next instruction of SLEEP.

7.4. About the first instruction after **SLEEP**

It is necessary to write the instruction immediately following SLEEP as NOP, because when using non-interrupt mode to wake up (such as WDT wake-up, GIE is not enabled) (wake up by an interrupt event), the instruction will be executed twice.

As shown in the following sample program:

<u>SLEEP</u>	// sleep
<u>NOP</u>	// When waking up without interrupt, this instruction will be executed twice.

8.Data EEPROM

There is 128 bytes of EEPROM integrated on the chip, which is addressed and accessed through EEADR. Software is available via EECON1 and EECON2. For programming EEPROM, the hardware implements the self-timing function of erasing and programming without software query, saving limited code space. time, and using this feature, you can enter sleep mode after starting the programming cycle to reduce power consumption.

Programming EEPROM requires following certain steps. This mechanism can prevent miswriting operations caused by program runaway or program loss.

8.1. Programming data EEPROM steps

- A. Clear the GIE bit of INTCON to 0;
- B. Determine whether GIE is 1, if so, repeat step A, otherwise proceed to the next step;
- C. Write the target address to EEADR;
- D. Write target data to EEDAT;
- E. Set all bits WREN3/WREN2/WREN1 to 1;
- F. Set bit WR to 1 (EECON2.0, WR will remain high thereafter);
- G. The value of WREN3/2/1 cannot be changed during the writing process, otherwise the programming will be terminated;
- H. After about 2ms, programming is automatically completed, WR is automatically cleared to 0, and WREN3, WREN2, and WREN1 are cleared to 0;
- I. If you want to program again, repeat steps C–H;

Example 1:

```
BCR INTCON, GIE
BTSC INTCON, GIE
LUMP $-2
BANKSEL EEADR
LDWI 55H
STR EEADR ;The address is 0x55
EEDAT STR ;The data is 0x55
LDWI 34H
STR EECON1 ;WREN3/2/1 is set to 1 at the same time
BSR EECON2, 0 ;Start writing
BSR INTCON, GIE ; Set GIE to 1
```

Example 2:

```

BCR INTCON, GIE
BTSC INTCON, GIE
LUMP $-2
BANKSEL EEADR
LDWI 55H
STR EEADR ;The address is 0x55
EEDAT STR ;The data is 0x55
LDWI 34H
STR EECON1 ;WREN3/2/1 is set to 1 at the same time
NOP ;Here NOP can be replaced by other instructions
BSR EECON2, 0 ;Start writing, the hardware will not actually start the programming EEPROM operation

```

BCR EECON1, WREN1; Clear WREN1 first so that WREN3/2/1 are not 1 at the same time

BSR EECON1, WREN1; Reset WREN1 so that WREN3/2/1 is 1 at the same time

BSR EECON2, 0 ;Start writing, this time the hardware will program the EEPROM

BSR INTCON, GIE

Notice:

1. Steps E and F of the above steps must be completed in two consecutive instruction cycles and cannot be staggered (such as example 2), otherwise the programming operation will not

Start, WREN3, WREN2 and **WREN1** may not be set to 1 by the same instruction . For example, the **BSR** instruction can be used to set them separately.

1 for each position ;

2. If steps E and F are executed in a staggered manner, if you want to start the next programming operation, you must add a step before E and F , and change **WREN3**,

Clear any bit of **WREN2** or **WREN1** to 0, as in example 2;

3. The read operation is invalid during programming;

4. If any bit of WREN3, WREN2 or **WREN1** is cleared to 0 before programming is completed, the **EEIF** flag must be cleared before the next programming .

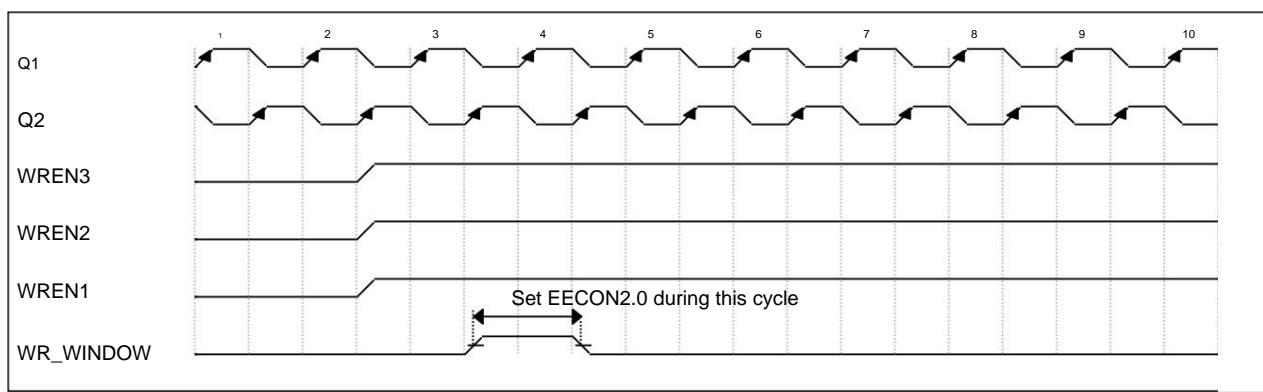


Figure 8.1 Software programming data EEPROM timing

8.2. Read data EEPROM

To read a data memory location, the user must write the address to the EEADR register and then set the control bit RD of the EECON1 register.

The EEPROM read cycle is 4 system clocks, so the EEDAT register is written with EEPROM data in the second instruction cycle after the read operation is initiated, that is, the data can be read by the next instruction. EEDAT will retain this value until the next time the user reads from or writes data to the unit (during a write operation).

The following is a sample program for reading EEPROM:

BANKSEL EEADR

LDWI dest_addr

STR EEADR

BSR EECON1, RD

NOP ; read wait

LDR EEDAT, W ; At this time, the data can be read by software

8.3. About the programming cycle

After starting the programming operation of the data EEPROM, the 2ms programming timer starts. During this time, the CPU will not pause, but will continue to execute the program.

8.4. Single programming mode of EEPROM

In addition to the normal self-erasing mode (programming operation includes automatic erasure), EEPROM also supports single programming mode. That is, after starting programming according to the steps described in Section 8.1, the selected address unit will not be automatically erased, but will only contain Programming, controlled through the PONLY register bit. Note that the single programming mode of **EEPROM** can only write data from 1 to 0, but not from 0 to 1. This is a bit like a "bitwise AND" operation.

For example, if the data 0xAA is stored at address 0, start the normal self-erasing mode (PONLY=0) and write 0x55. After the operation is completed, the data stored at address 0 becomes 0x55;

But if the single programming mode is set (PONLY=1) and the same data 0x55 is written, the final data stored at address 0 will be 0x00.



8.5. Summary of registers related to data EEPROM

Name	address	bit7		bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value
INTCON	0x0B/8B		GIE	LIKE THIS	TOIE	NOT	PAY	TOIF	INTF	PAIF	0000 0000
PIE1	0x8C	THIS	CKMIE	LVD	ACMPIE TMR1IE	OSFIE TMR2IE			ADCIE	0000 0000	
PIR1	0x0C	EEIF	CKMIF	LVDIF	ACMPIF TMR1IF	OSFIF TMR2IF			ADCIF	0000 0000	
EDTA	0x9A					EDTA[7:0]					0000 0000
EEADR	0x9B						EEADR[7:0]				0000 0000
EECON1	0x9C		— Reserved	WREN3 WR	EN2 WRERR	WREN1 PONLY				RD	ÿ000 x000
EECON2	0x9D		—	—	—	—	—	—	—	WR	ÿÿÿ ÿÿ0

8.5.1. EEDAT register, address 0x9A

Bit	7	6	5	4	3	2	1	0
Name	EDTA[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	EDTA	Data EEPROM Data Register

8.5.2. EEADR register, address 0x9B

Bit	7	6	5	4	3	2	1	0
Name	EEADR[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	EEADR	Data EEPROM address register

8.5.3. EECON1 register, address 0x9C

Bit	7	6	5	4	3	2	1	0
Name	-	Reserved	WREN3	WREN2	WRERR	WREN1	PONLY	RD
Reset	-	0	0	0	x	0	0	0
Type	RO-0	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	N/A	Reserved bit, read 0
6	Reserved reserved bits	
5	WREN3	Data EEPROM write enable 3 Used in conjunction with WREN2 and WREN1
4	WREN2	Data EEPROM write enable 2 Used in conjunction with WREN3 and WREN1
3	WRERR	Data EEPROM write error flag bit 1: A watchdog or external reset occurs during the EEPROM programming cycle and is aborted. 0: The EEPROM programming cycle is completed normally
2	WREN1	Data EEPROM write enable 1 WREN3-1=111: Allow software to program EEPROM. After programming is completed, each bit will be cleared to 0 automatically. WREN3-1=Other values: disable software programming of EEPROM
1	PONLY	Data EEPROM write programming mode 1: Only write but not erase 0: Erase first and then write
0	RD	Data EEPROM read control bit When RD is enabled, the high level of this bit only lasts for two instruction cycles, and then reading always returns 0. Write 1: Start a data EEPROM read cycle Write 0: do not start reading

8.5.4. EECON2 register, address 0x9D

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	WR
Reset	-	-	-	-	-	-	-	0
Type	RO-0	RW						

Bit	Name	Function
7:1	N/A	Reserved bit, read 0
0	WR	Data EEPROM write control bit Read operation: 1: Data EEPROM programming cycle in progress 0: Data EEPROM is not in programming cycle Write operation: 1: Start a data EEPROM programming cycle 0: meaningless

9. 12bit ADC module

Analog-to-digital Converter (ADC) can convert analog input signals into corresponding 12-bit binary representation values.

This family of devices uses multiple analog inputs multiplexed into a sample and hold circuit. The output of the sample and hold circuit is connected to the input of the converter.

The converter generates a 12-bit binary value through the successive approximation method and saves the conversion result in the ADC result register (ADRESL:ADRESH)

middle. The ADC reference voltage can be software selected as VDD, an external reference voltage, or an internally generated reference voltage. The ADC can be used when conversion is complete

Generate an interrupt. This interrupt can be used to wake the device from Sleep.

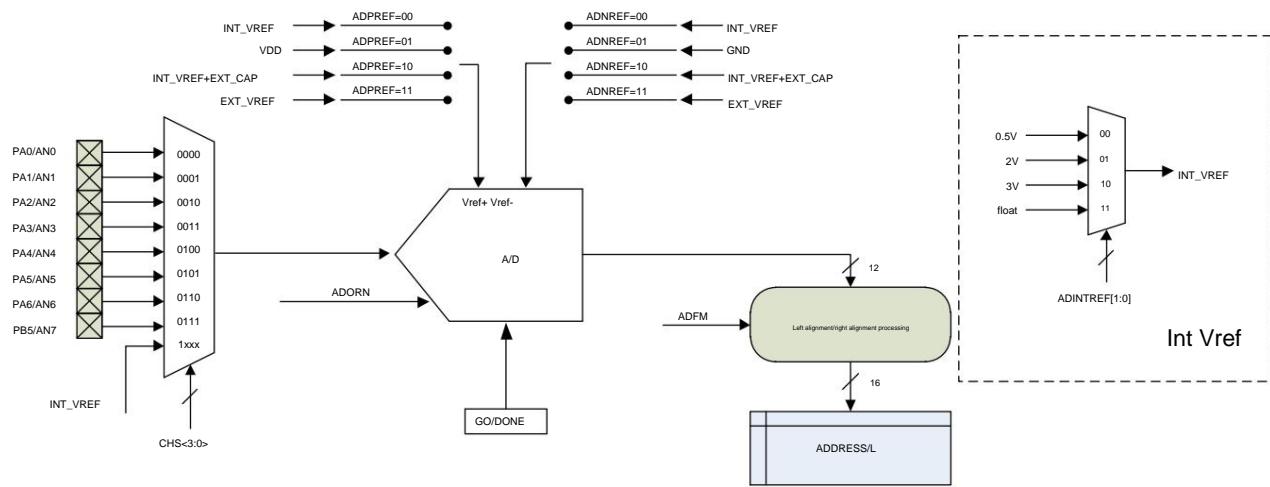


Figure 9.1 ADC principle block diagram

9.1 ADC configuration

When configuring and using the ADC, you must consider the following features:

- ÿ Calibrate ADC
- ÿ Port configuration
- ÿ Channel selection
- ÿ Trigger mode selection
- ÿ Trigger source selection
- ÿ Trigger type selection
- ÿ Trigger delay configuration
- ÿ ADC reference voltage selection
- ÿ ADC conversion clock source
- ÿ Interrupt control
- ÿ Format of conversion result
- ÿ Threshold comparison

Note: When making various configuration changes, you need to ensure that **AD** conversion is not in progress or the external trigger function is not turned on. It is recommended to

Changes are made when **ADON** is closed.



9.1.1 Port configuration

ADCs can be used to convert analog and digital signals. When converting analog signals, the relevant TRIS and ANSEL bits should be set and the I/O pin should be configured for analog functionality. See the corresponding port chapter for more information.

NOTE: The presence of analog voltages on pins defined as digital inputs can cause the input buffer to conduct excessive current.

9.1.2 Channel selection

The CHS bit of the ADCON0 register determines which channel is connected to the sample and hold circuit. When changing channels, a certain delay can be added before starting conversion according to the need for stable sampling. The hardware has a fixed sampling delay of 1.5TAD. See Section 9.2 "ADC Operation" for more information.

9.1.3 Trigger mode selection

The ADEX bit of the ADCON0 register determines whether to use an external trigger signal. If ADEX=0, ADGO can be set by the program and automatically cleared after AD conversion is completed. If ADEX=1, ADGO will be set by external hardware trigger and cleared after AD conversion is completed.

Note: If the leading edge blanking trigger **ADC** is selected , that is, when **LEBADT** is set to 1 , **ADEX** and **ADON** need to be set first .

9.1.4 Trigger source selection

After setting ADEX, the ETGSEL bit in the ADCON2 register determines which external trigger signal is used. The optional I/O pin trigger requires configuring the relevant registers. Please refer to the corresponding port chapter for details.

9.1.5 Trigger type selection

The ETGTYP bit of the ADCON2 register determines the trigger type of the external trigger signal.

9.1.6 Trigger delay configuration

The ADDLY:8 bit of the ADCON2 register and the ADDLY register form a 9-bit delay counter, which together determine the trigger delay time of the external trigger signal. Due to the need to synchronize asynchronous signals, the actual delay time is: (ADDLY+6)/FADC.

Note: If the leading edge blanking trigger function is selected, the actual delay time is: (ADDLY+3)/FT2CK + 3/FADC. T2CK is the Timer2 clock, selected by the T2CKSRC bit.

9.1.7 ADC reference voltage

The ADPREF bit of the ADCON1 register provides control of the positive reference voltage, and the ADNREF bit provides control of the negative reference voltage. Positive/negative parameters

The test voltage can be the internal reference voltage, VDD/GND, the internal reference voltage plus an external capacitor, or the external reference voltage. Positive/negative reference voltage available

There are various combinations, but the internal reference voltage cannot be selected at the same time. If this occurs it forces the negative reference voltage to be connected to GND.

The ADINTREF bit of the ADCON2 register provides control of the internal voltage reference. Internal reference voltage can be selected from 0.5V, 2V, 3V

Or left in the air.

9.1.8 Conversion clock

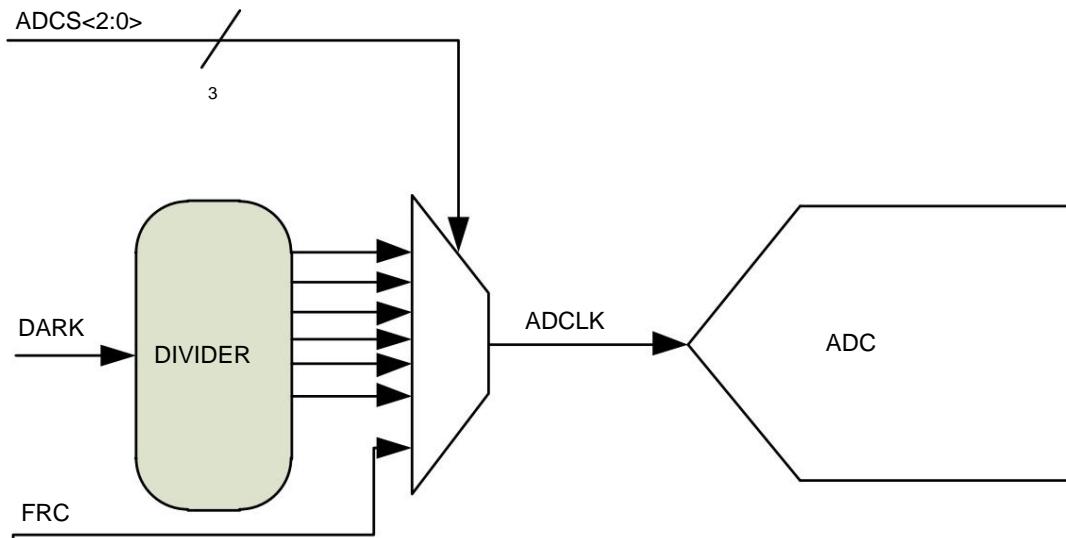


Figure 9.2 ADC clock configuration principle

The conversion clock source is software selectable via the ADCS bits of the ADCON1 register. There are 8 clock options:

- ÿ DARK
- ÿ DARK/2
- ÿ DARK /4
- ÿ DARK /8
- ÿ DARK /16
- ÿ DARK /32
- ÿ DARK /64
- ÿ FRC (internal slow clock oscillator)

The conversion time to complete one bit is defined as TAD. It takes 12 TAD cycles to complete a 12-bit conversion (including the 1.5TAD sampling time and 1TAD data transmission processing time), as shown in Figures 9.3 and 9.6.

Correct conversion must meet the corresponding TAD specifications. See A/D conversion requirements in Section 21 "Electrical Characteristics" for more information. Table 9.1

Shown is an example of correct selection of ADC clock.

Notice:

1. Unless FRC is used , any change in system clock frequency will change the **ADC** clock frequency, which will have a negative impact on **the ADC** results.

Negative impact:

2. FRC can be **256kHz or 32kHz**, depending on the value of **LFMOD** ;

3. The gray cells in the table below indicate unsupported frequencies;

ADC clock period (TAD)					
ADC clock source	ADCS<2:0>	16MHz	8MHz	4MHz	1MHz
DARK	011	62.5ns	125ns	250ns	1.0 μ s
DARK /2	000	125ns	250ns	500ns	2.0 μ s
DARK /4	100	250ns	500ns	1.0 μ s	4.0 μ s
DARK /8	001	0.5 μ s 1.0 μ s 1.0 μ s 2.0 μ s 2.0 μ s 4.0 μ s		2.0 μ s	8.0 μ s
DARK /16	101	4.0 μ s 8.0 μ s 4.0 μ s 4.0 μ s Table 9.1		4.0 μ s	16.0 μ s
DARK /32	010	ADC clock cycle and device		8.0 μ s	32.0 μ s
DARK /64	110	operating frequency		16.0 μ s	64.0 μ s
FRC	x11			4.0 μ s	4.0 μ s

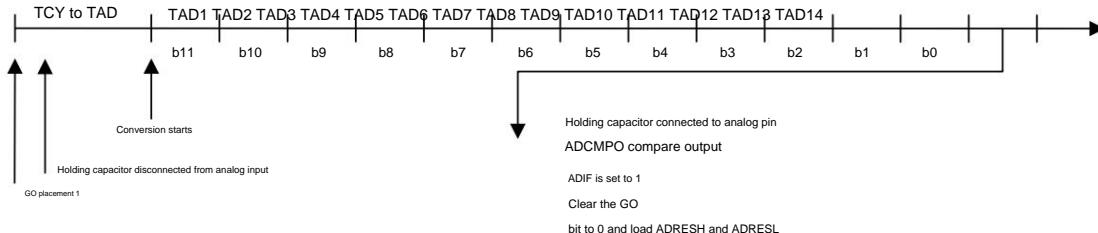


Figure 9.3 Analog-to-digital conversion TAD cycle

9.1.9 Interruption

The ADC module enables an interrupt to be generated upon completion of an analog-to-digital conversion or by a threshold comparison on completion of the conversion. The ADC conversion interrupt flag is ADIF bit in the PIR1 register. The ADC interrupt is enabled by the ADIE bit in the PIE1 register. The ADIF bit must be set and cleared by software.

The ADC threshold comparison interrupt location is ACMPIF in the PIR1 register. The ADC threshold compare interrupt is enabled in the PIE1 register ACMPIE bit.

- Note: 1. Regardless of whether **the ADC** interrupt is turned on or not, the ADIF bit is set to 1 when each normal conversion is completed .
 2. ADIF will not be set even when the software stops **AD** conversion .
 3. The ADC can work during sleep only when the FRC oscillator is selected.

Interrupts can be generated while the device is operating or in sleep state. If the device is in Sleep state, an interrupt can wake the device. When waking up from sleep, First enter the interrupt handler, exit the interrupt, and then execute the instruction after SLEEP. If the user attempts to wake up the device and resume sequential execution line of code, global interrupts must be disabled. If global interrupts are enabled, code execution will go to the interrupt service routine.

9.1.10 Format of conversion results

There are two formats for 12-bit A/D conversion results, namely left-justified and right-justified. The ADFM bit of the ADCON1 register controls the output format.

AD autocalibration values are also affected by the output format.

Figure 9.4 shows the two output formats.

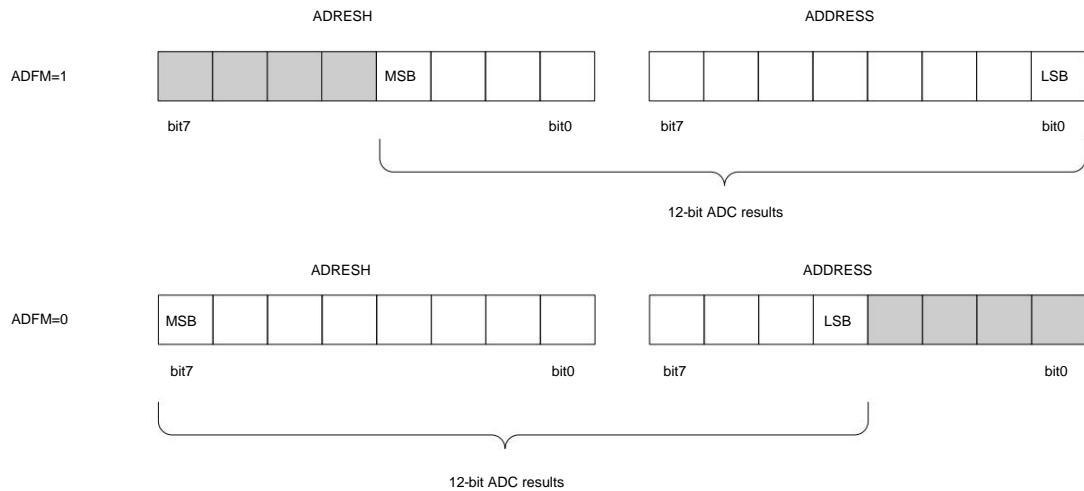


Figure 9.4 ADC conversion result format diagram

9.1.11 Threshold comparison

The ADCMPH register is the ADC result comparison threshold, and the ADCMPEN bit of the ADCON3 register controls the comparison function enable.

The ADCMPOP bit controls the comparison polarity and ADCMPO indicates the comparison result.

AD can be compared at the completion of each conversion. The comparison results will be maintained until the next conversion is completed and updated. ADCMPEN or

Clearing ADON can turn off the comparison function or AD module, and can clear ADCMPO at the same time. Entering sleep does not clear ADCMPO.

A fault brake event can be generated when each comparison is completed, controlled by ADFBEN in the ADCON3 register.

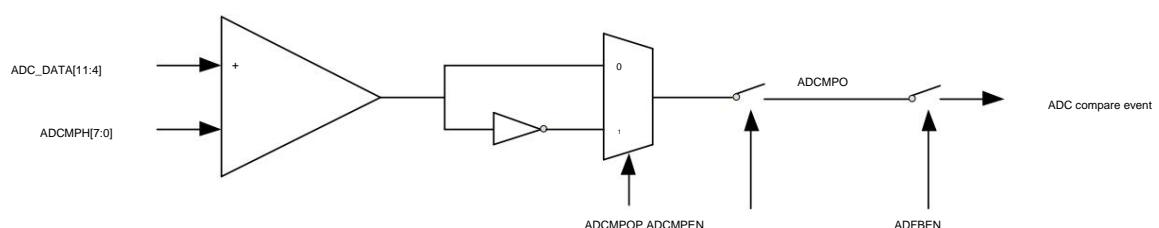


Figure 9.5 ADC threshold comparison function block diagram

Notice:

1. ADCMPO is an internal signal and is invisible to software, but software can indirectly determine the value of ADCMPO through the ADCMPIF bit .

The ADC control module determines the value of ADCMPO at the end of conversion . When ADCMPO is 1 , ADCMPIF is set to 1.



9.2 Working principle of ADC

9.2.1 Start conversion

To enable the ADC module, the ADON bit of the ADCON0 register must be set. If ADEX=0, setting the GO/DONE bit of the ADCON0 register to 1 will start AD conversion. If ADEX=1, an external trigger signal is required to start, and the hardware sets the GO/DONE bit, and the program sets the ADGO bit to be invalid.

Note: 1.

The GO/DONE bit should not be set to 1 in the instruction that turns on the ADC . See Section 9.2.7 “A/D Conversion Steps” 2. The AD configuration should not be changed after starting the ADC conversion or while waiting for an external trigger . 3.

After setting ADGO, you need to wait for one system cycle before reading back the ADGO flag.

9.2.2 Conversion completed

When the conversion is completed, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF flag bit to 1
- Update the ADRESH:ADRESL registers with the new conversion result

9.2.3 Terminating conversion

When ADEX=0, the ADC is in software trigger state. If the conversion must be terminated before completion, software can clear GO/DONE. Then ADC will not update this conversion data. When ADEX=1, ADC is in hardware trigger state. If you need to terminate the conversion, you need to set ADON to 0 and turn off the ADC enable switch.

NOTE: A device reset will force all registers back to their reset state. In this way, the ADC module is turned off and any pending conversions are terminated.

9.2.4 ADC operation in sleep mode

The ADC module can operate during sleep, which requires the ADC clock source to be placed in the FRC option.

ADC needs to wait 4*TAD before starting conversion. This allows software to execute a SLEEP instruction to put the MCU in SLEEP mode after setting ADGO, thereby reducing system noise during ADC conversion. System noise can be further reduced by configuring the ADC clock to be FRC. If the ADC interrupt is enabled, the device will wake from Sleep after the conversion is complete. If the ADC interrupt is disabled, the ADC module turns off after the conversion is complete, although the ADON bit remains set.

If the ADC clock source is not FRC, executing a SLEEP instruction will forcefully abort the current conversion and the ADC module will be shut down directly, although The ADON bit remains set.

9.2.5A/D conversion steps

The following is an example of steps for analog-to-digital conversion using an ADC:

1. Configure the port:

- ÿ Disable pin output driver (see TRIS register)
- ÿ Configure pins as analog

2. Configure the ADC module:

- ÿ Select ADC conversion clock
- ÿ Configure reference voltage
- ÿ Select ADC input channel
- ÿ Select the format of the conversion result
- ÿ Open the ADC module

3. Configure ADC interrupt (optional):

- ÿ Clear the ADC interrupt flag to zero
- ÿ Allow ADC interrupt
- ÿ Allow peripheral interrupts
- ÿ Allow global interrupts

4. Wait for the required stabilization time TST (1);

5. Wait for the required acquisition time TACQ (2);

6. Set GO/DONE to 1 to start conversion or wait for hardware trigger;

7. Wait for one system cycle before reading back GO/DONE;

8. Wait for the ADC conversion to complete via one of the following conditions:

- ÿ Query GO/DONE bit
- ÿ Wait for ADC interrupt (when interrupt is enabled)

9. Read ADC results;

10. Clear the ADC interrupt flag (required if interrupts are enabled).

Here is a sample code:

```

BANKSEL ADCON1
LDWI B'01110000' ;ADC Frc clock
STR ADCON1
TRISA BANKSEL
BSR TRISA,0 ;Set RA0 to input
BANKSEL ANSEL
BSR ANSEL,0 ;Set RA0 to analog
BANKSEL ADCONO
LDWI B'10000001' ;Right justify,
STR ADCONO ; Vdd Vref, AN0, On
LCALL StableTime ; ADC stable time
LCALL SampleTime ;Acquisition delay
BSR ADCONO,GO ;Start conversion
BTSC ADCONO,GO ;Is conversion done?
LUMP $-1 ;No, test again
BANKSEL ADDRESS;
LDR ADRESH,W ;Read upper 2 bits
STR RESULTHI ;Store in GPR space
BANKSEL ADDRESS ;
LDR ADRESL,W ;Read lower 8 bits
STR RESULTLO Note: ;Store in GPR space

```

1. TST time is the stabilization time of the ADC. When using the internal reference, the ADC needs to consider the stabilization time of the reference voltage when it is first started.

TVRINT, the waiting time should be the larger of the two, that is, **max(TVRINT, TST)**;

2. See Figure 9.6, ADC conversion timing;

3. You must wait for a long enough TACQ time after switching channels, that is, the SampleTime in the above example must meet the TACQ in Table 18.10

Time requirement, otherwise ADC accuracy and linearity will not be guaranteed;

9.2.6A/D acquisition time requirements

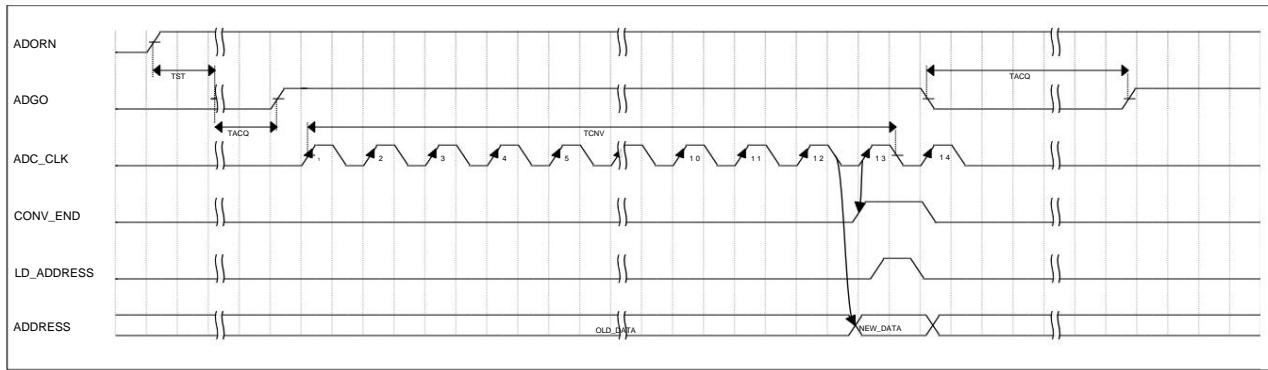


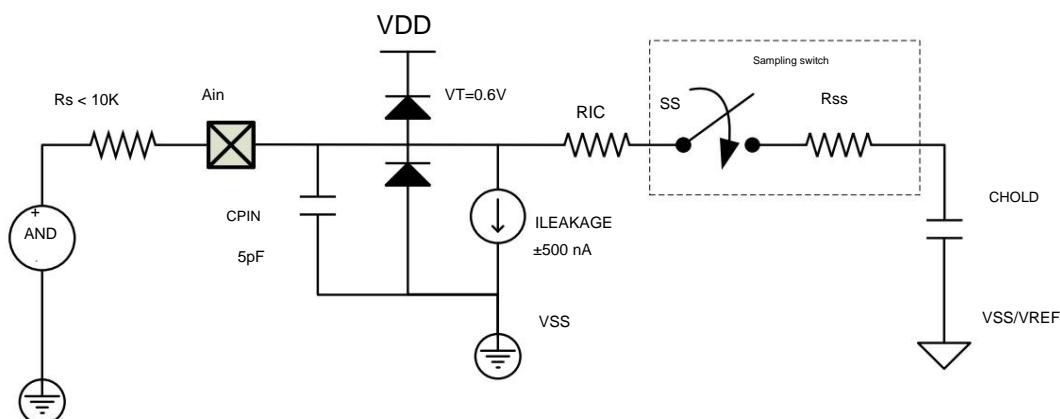
Figure 9.6 ADC software triggered conversion timing diagram

In order for the ADC to achieve the specified accuracy, the charge holding capacitor (CHOLD) must be filled to the level of the input channel. Simulation input model

See Figure 9.7. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the charging time of the capacitor CHOLD. Sampling on

The off (RSS) impedance changes as the device voltage (VDD) changes, see Figure 9.7. It is recommended that the maximum impedance of the analog signal source is 10k Ω .

Acquisition time decreases as source impedance decreases. After selecting (or changing) an analog input channel, acquisition must be completed before starting conversion.



Legend:

- CPIN = input capacitance
- VT = threshold voltage
- ILEAKAGE = Node leakage current =
- RIC = Interconnect
- SS = resistance = Sampling switch
- CHOLD = sample and hold capacitor

Figure 9.7 Simulation input model

9.3 Summary of registers related to ADC

Name	Address	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	reset value			
ADRESL 0x111				Low byte of A/D result register										
ADDRESS 0x112				High byte of A/D result register										
ADCON1 0x113	—			CHS<3:0>				ADEX GO	DONE ADON		ÿ000 0000			
ADCON1 0x114	ADFM			ADCS<2:0>			ADNREF<1:0>		ADPREF<1:0>		0000 0000			
ADCON2 0x115				ADINTREF<1:0>		ETGTYPE<1:0>		ADDLY.8	ETGSEL<2:0>		0000 0000			
ADDLY 0x186				ADDLY<7:0> / LEBPRL<7:0>										
ADCON3 0x186	ADFBEN	ADCMPOP	ADCMPEN	—	LEBADT						000ÿ 0ÿÿ			
ADCMPH 0x187				ADCMPH<7:0>										
LEBCON 0x185	LIVE			LEBCH		— EDGS					000ÿ 0ÿÿ			
VRP5VCAL 0x97				VRP5VCAL<7:0>										
VR2VCAL 0x108				VR2VCAL<7:0>										
VR3VCAL 0x11F				VR3VCAL<7:0>										

9.3.1 ADRESL, address 0x111

Bit	7	6	5	4	3	2	1	0
Name	ADDRESS<7:0>							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	ADDRESS	Low byte of ADC result register When ADFM=0, ADRESL[7:4] are the lower 4 bits of the 12-bit conversion result, and the rest are 0. When ADFM=1, ADRESL[7:0] are the lower 8 bits of the 12-bit conversion result.

9.3.2 ADRESH, address 0x112

Bit	7	6	5	4	3	2	1	0
Name	ADRESH<7:0>							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	ADRESH	High byte of ADC result register When ADFM=0, ADRESH[7:0] is the high 8 bits of the 12-bit conversion result. When ADFM=1, ADRESH[3:0] are the high 4 bits of the 12-bit conversion result, and the rest are 0.

9.3.3 ADCON0, address 0x113

Bit	7	6:3	2	1	0
Name	-	CHS<3:0>	ADEX	GO/DONE	ADORN
Reset	-	0	0	0	0
Type	RO.0	RW	RW	RW	RW

Bit	Name	Function
7	N/A	Reserved: Read as 0
6:3	CHS	<p>Analog channel selection bit</p> <p>0000 = AN0 0001 = AN1 0010 = AN2 0011 = AN3 0100 = AN4 0101 = AN5 0110 = AN6 0111 = AN7</p> <p>1xxx = Internal reference voltage channel, the specific voltage value is selected according to ADINTREF</p>
2	ADEX	<p>ADC trigger signal type selection</p> <p>This bit determines the trigger condition to start the ADC</p> <p>0 = When software sets the GO/DONE bit, AD conversion is started 1 = An external trigger signal is required to start AD conversion, and the trigger event sets the GO/DONE bit. The external trigger signal condition is determined by the registers ETGSEL<2:0> and ETGTYP<1:0>.</p>
1	GO/DONE	<p>AD conversion status bit (set directly by hardware trigger event)</p> <p>Setting this bit starts an A/D conversion cycle. When the A/D conversion is completed, this bit is automatically cleared by hardware.</p> <p>0 = A/D conversion completed/not in progress. 1 = A/D conversion is in progress or hardware trigger delay is counting.</p>
0	ADORN	<p>ADC enable bit</p> <p>0 = ADC is disabled and draws no operating current 1 = ADC is enabled</p>

9.3.4 ADCON1, address 0x114

Bit	7	6	5	4	3	2	1	0
Name	ADFM	ADCS<2:0>			ADNREF<1:0>		ADPREF<1:0>	
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	ADFM	ADC result format selection bit 1 = Right aligned. When loading the conversion result, the upper 4 bits of ADRESH are set to '0'. 0 = left aligned. When loading the conversion result, the lower 4 bits of ADRESL are set to '0'.
6:4	ADCS	ADC conversion clock selection bit 000 = DARK/2 001 = DARK/8 010 = DARK/32 011 = Dark 100 = DARK/4 101 = DARK/16 110 = DARK/64 111 = FRC (clocked from dedicated RC oscillator)
3:2	ADNREF	ADC negative reference voltage configuration bit (use PA5 to connect the external reference voltage or external capacitor) 00 = Int Vref (internal reference voltage) 01 = GND 10 = Int Vref + Ext Cap (internal reference voltage + external capacitor) 11 = Ext Vref (external reference voltage)
1:0	ADPREF	ADC positive reference voltage configuration bit (use PA4 to connect an external reference voltage or external capacitor) 00 = Int Vref (internal reference voltage) 01 = VDD 10 = Int Vref + Ext Cap (internal reference voltage + external capacitor) 11 = Ext Vref (external reference voltage)

9.3.5 ADCON2, address 0x115

Bit	7	6	5	4	3	2	1	0
Name	ADINTREF<1:0>		ETGTYPE<1:0>		ADDLY.8	ETGSEL<2:0>		
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:6	ADINTREF	<p>ADC internal reference voltage configuration bits</p> <p>00 = 0.5V</p> <p>01 = 2V</p> <p>10 = 3V</p> <p>11 = float</p>
5:4	ETC TYPE	<p>External trigger signal type selection</p> <p>When ADEX is set to 1, this bit determines the type of response to external trigger</p> <p>00 = falling edge of PWM or ADC_ETR pin</p> <p>01 = rising edge of PWM or ADC_ETR pin</p>
3	ADDLY.8 /LEBPR9	<p>ADC external trigger delay counter threshold bit 8</p> <p>See the ADDLY register description for details.</p>
2:0	ETGSEL	<p>External trigger source selection</p> <p>When ADEX is 1, this bit selects the source of external trigger ADC</p> <p>000 = P1A0</p> <p>001 = P1A0N</p> <p>010 = P1B</p> <p>011 = P1C</p> <p>100 = P1D</p> <p>101 = ADC_ETR</p> <p>Other bits are invalid</p>

9.3.6LEBCON register, address 0x185

Bit	7	6	5	4	3	2	1	0
Name	LIFE	LEBCH[1:0]			EDGS			
Reset	0	0	0		0			
Type	RW	RW	RW	RO-0	RW	RO-0	RO-0	RO-0

Bit	Name	Function
7	LIFE	Leading edge blanking enable bit (can only be switched when ADGO=0 , otherwise the ADC will work abnormally) 1 = enabled 0 = disabled
6:5	LEBCH	Leading edge blanking channel selection 00 = P1A0 01 = P1B 10 = P1C 11 = P1D
4	N/A	Reserved bit, read 0
3	EDGS	PWM blanking edge selection 0 = PWM rising edge 1 = PWM falling edge
2:0	N/A	Reserved bit, read 0

9.3.7ADCON3, address 0x186

Bit	7	6	5	4	3	2	1	0
Name	ADFBEN	ADCMPOP	ADCMPPEN	—		LEBADT	—	—
Reset	0	0	0	—	0	—	—	—
Type	RW	RW	RW	RO.0	RW	RO.0	RO.0	RO.0

Bit	Name	Function
7	ADFBEN	ADC comparison result responds to fault brake enable 0 = disabled 1 = ADC trigger fault brake function enabled
6	ADCMPOP	ADC comparator output polarity selection bit 0 = If the upper eight bits of the ADC result are greater than or equal to ADCMPH[7:0], ADCMPO is 1 1 = If the upper eight bits of the ADC result are less than ADCMPH[7:0], ADCMPO is 1
5	ADCMPPEN	ADC result comparison enable bit 0 = ADC result comparison function is turned off 1 = ADC result comparison function is on
4	N/A reserved bit,	read 0
3	LEBADT	After the leading edge blanking period ends, the ADC trigger is enabled 1 = trigger ADC conversion 0 = Do not trigger ADC conversion
2:0	N/A Reserved,	read as 0

9.3.8 ADCMPH, address 0x187

Bit	7	6	5	4	3	2	1	0
Name	ADCMPH<7:0>							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	ADCMPH	<p>ADC comparison threshold</p> <p>Only 8 bits are used for comparison of the upper 8 bits of the ADC result.</p>

9.3.9 ADDLY/LEBPRL, address 0x188

Bit	7	6	5	4	3	2	1	0
Name	ADDLY<7:0>							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	ADDLY	<p>ADC external trigger start delay counter threshold low</p> <p>This 8-bit register and ADCON2.7 form a 9-bit counter, which is used to add a delay before the external trigger starts the ADC. delay count</p> <p>The converter ends and then starts ADC conversion.</p> <p>External delay time = (ADDLY+6)/FADC</p> <p>Note that this delay is only effective when ADEX is set to 1. If the PWM output triggers the ADC function, it must not be changed during PWM operation.</p> <p>ADDLY count value. Simultaneously multiplexed as leading edge blanking count threshold</p>

9.3.10 VRP5VCAL, address 0x97

Bit	7	6	5	4	3	2	1	0
Name	VRP5VCAL<7:0>							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	VRP5VCAL ADC internal 0.5V reference voltage calibration bit	

9.3.11 VR2VCAL, address 0x108

Bit	7	6	5	4	3	2	1	0
Name	VR2VCAL<7:0>							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	VR2VCAL ADC internal 2V reference voltage calibration bit	

9.3.12 VR3VCAL, address 0x11F

Bit	7	6	5	4	3	2	1	0
Name	VR3VCAL<7:0>							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	VR3VCAL ADC internal 3V reference voltage calibration bit	

10.Timer 0

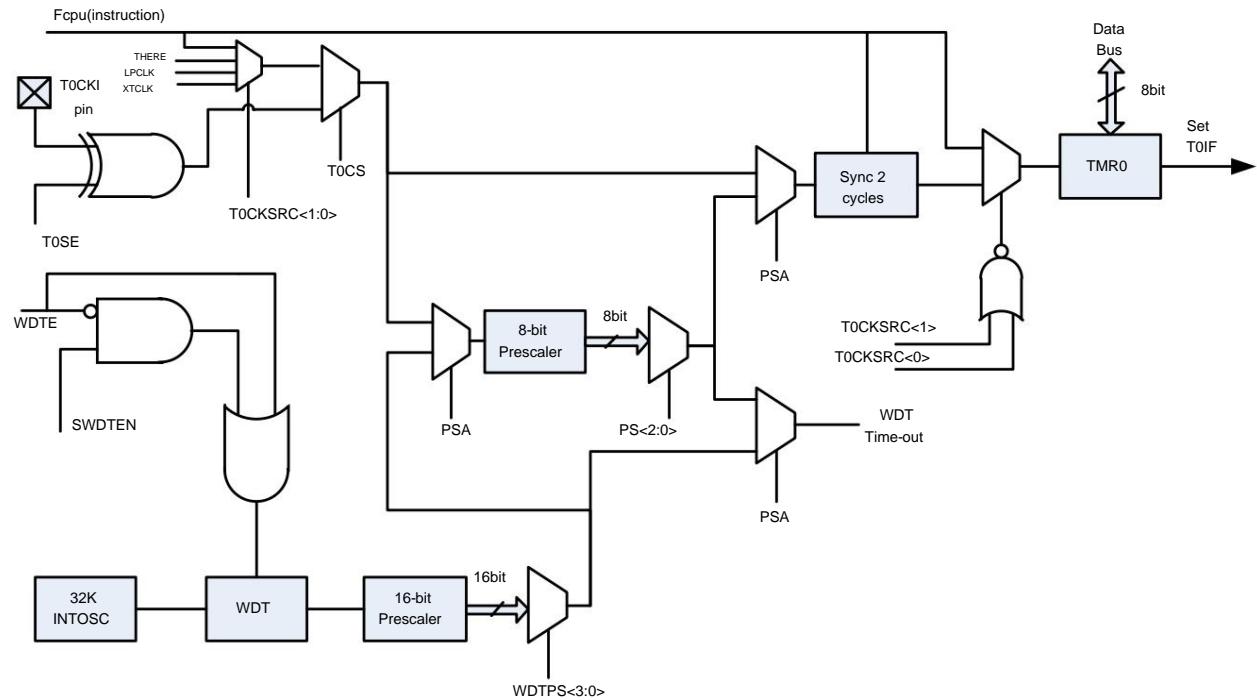


Figure 10.1 Watchdog and Timer 0 block diagram

Timer 0 is 8 bits and can be configured as a counter or timer. When used as an external event (T0CKI) counter, it can be configured as an upper Count rising or falling edges. When used as a timer, its counting clock source is selected by T0CKSRC, that is, it increments by one every clock cycle. Second-rate. There is an 8-bit prescaler shared with WDT. When PSA is 0, the prescaler is assigned to timer 0.

Notice:

- When changing the value of PSA, the hardware will automatically clear the prescaler to 0.

10.1. Timer0 timer mode

In this mode, Timer 0 is incremented by 1 (without prescaler) every clock cycle (clock source is optional). Software can clear the OPTION register T0CS bit inside to enter timer mode. When software writes to TMR0, the timer will not increment for 2 cycles after the write.



10.1.1. Timer0 clock source

The clock source of Timer0 is controlled by register bit T0CKSRC, and the instruction clock is selected by default.

Instruction clock → HIRC

internal high-speed clock → LP crystal

clock → XT crystal clock

Before changing the clock configuration of Timer0, it is recommended to clear T0ON to 0 to prevent glitches generated during clock switching from affecting Timer0.

In non-SLEEP mode and Timer0 is enabled (T0ON=1), the selected clock source will automatically turn on; Note: 1. When selecting **LP** as the **T0** clock source, the

configuration option **FOSC** must be **LP** or **INTOSCIO** mode. Otherwise, the LP crystal circuit

will not open;

2. Similarly, when selecting **XT** as the **T0** clock source, the configuration option **FOSC** must be **XT** or **INTOSCIO** mode. Otherwise, the XT crystal

The body circuit will not open.

In SLEEP mode, if you want Timer0 to continue counting, you need to set T0CKRUN to 1, and the clock source cannot select the instruction clock, because in SLEEP mode, the instruction clock is turned off.

10.1.2. Reading and writing of TMR0 register

When the Timer0 clock source is different from the CPU clock (such as configured in LP or XT mode), it is recommended that the software first clear **T0ON** to 0 when starting a read or write operation on TMR0 to avoid reading or writing errors.

10.2. Timer0 counter mode

In this mode, Timer 0 is incremented by 1 (without prescaler) triggered by the rising or falling edge of each T0CKI pin. The specific clock edge is determined by the T0SE bit in the OPTION register. Software can set the T0CS bit in the OPTION register to enter counter mode.

10.2.1. Software configurable prescaler circuit

The chip has a prescaler circuit in front of timer 0 and watchdog timer, which can be assigned to Timer0 or watchdog timer, but both cannot use this prescaler circuit at the same time. The specific allocation to Timer0 or watchdog is determined by the PSA bit in the OPTION register. When PSA is 0, the prescaler is allocated to Timer0. In Timer0 prescaler mode, a total of 8 prescaler ratios (1:2 to 1:256) can be set by the PS[2:0] bits in the OPTION register. The prescaler circuit is neither readable nor writable. Any write to the TMR0 register will clear the prescaler circuit.

When the prescaler circuit is assigned to the watchdog, a CLRWDT instruction clears the prescaler circuit.



10.2.1.1. Switching the prescaler circuit between timer and watchdog

Since the prescaler circuit can be assigned to Timer0 or watchdog timer, switching the prescaler between the two may cause false reset. Bit.

When switching the prescaler circuit from being assigned to TMR0 to being assigned to watchdog, be sure to execute the following sequence of instructions:

<u>BANKSEL TMR0</u>	:Clear WDT
<u>CLRWDT</u>	
<u>CLRR TMR0</u>	:Clear TMR0 and prescaler
<u>BANKSEL OPTION_REG</u>	
<u>BSR OPTION_REG.PSA</u>	:Select WDT
<u>CLRWDT</u>	
<u>LDWI b'11111000'</u>	:Mask prescaler bits
<u>ANDWR OPTION_REG.W</u>	
<u>IORWI b'00000101'</u>	:Set WDT prescaler bits to 1:32
<u>STR OPTION_REG</u>	

When switching the prescaler circuit from being assigned to watchdog to being assigned to TMR0, be sure to execute the following sequence of instructions:

<u>CLRWDT</u>	:Clear WDT and prescaler
<u>BANKSEL OPTION_REG</u>	
<u>LDWI b'11110000'</u>	:Mask TMR0 select and prescaler bits
<u>ANDWR OPTION_REG.W</u>	
<u>IORWI b'00000011'</u>	:Set prescale to 1:16
<u>STR OPTION_REG</u>	

10.2.2. Timer 0 interrupt

When register TMR0 (timer 0 count value) matches PR0, the T0IF flag will be set and an interrupt will be generated (if enabled).

Note that the Timer0 interrupt cannot wake up the CPU because the timer is frozen in the sleep state unless T0CKRUN is 1 and its

When the clock source is not the instruction clock.

10.2.3. Driving Timer 0 with an external clock

In counting mode, the synchronization between the T0CKI pin input and the Timer0 register is determined by the Timer0 clock source (clock source is optional)

The generated non-overlapping clock is sampled, so the high level time and low level time of the external clock source cycle must meet the relevant timing requirements. beg.

10.2.4. Status in sleep mode

When T0CKRUN=1 and the clock source of Timer0 is not the instruction clock, Timer0 will remain running after the MCU enters sleep.

status, the clock source selected by T0CKSRC will not be turned off. Otherwise, Timer0 will stop counting and maintain the count value before sleep.

10.3. Summary of registers related to Timer0

Name	address bit7		bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value
TMR0	0x01		Timer0 count value register							xxxx xxxx
INTCON 0x0B/8B		GIE	LIKE THIS	TOIE	NOT	PAY	TOIF	INTF	PAIF	0000 0000
OPTION	0x81	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
T0CON0 0x1F	—		—	—	—	TOON TOCKRUN	TOCKSRC[1:0]			ÿÿÿ 1000
TRISA	0x85	TRISA[7:0], PORTA direction control								1111 1111

10.3.1. OPTION register, address 0x81

Bit	7	6	5	4	3	2	1	0
Name	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	/PAPU	/PAPU: PORTA pull-up enable bit 1 = Disable PORTA pull-up 0 = PORTA pull-up is enabled by the respective port latch value
6	INTEDG	INTEDG: Interrupt edge selection bit 1 = Interrupt on rising edge of PC1/INT pin 0 = Interrupt on falling edge of PC1/INT pin
5	T0CS	T0CS: Timer0 clock source selection bit 1 = Transition on PA2/T0CKI pin 0 = Determined by T0CKSRC bit
4	T0SE	T0SE: Timer0 clock source edge selection bit 1 = Increments on the falling edge of PA2/T0CKI pin 0 = Increments on rising edge of PA2/T0CKI pin
3	PSA	PSA: prescaler allocation bit 1 = Prescaler assigned to WDT 0 = Prescaler assigned to Timer0 module
2	PS2	PS<2:0>: Prescaler ratio selection bits Bit value TIMER0 divider ratio WDT divider ratio 000 1 : 2 1 : 1 001 1 : 4 1 : 2 010 1 : 8 1 : 4 011 1 : 16 1 : 8 100 1 : 32 1 : 16 101 1 : 64 1 : 32 110 1 : 128 1 : 64 111 1 : 256 1 : 128
1	PS1	
0	PS0	

10.3.2. TMR0, address 0x01

Bit	7	6	5	4	3	2	1	0
Name	TMR0[7:0]							
Reset	xxxx xxxx							
Type	RW							

Bit	Name	Function
7:0	TMR0	Timer 0 count result register

10.3.3. T0CON0, address 0x1F

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	T0ON	T0CKRUN	T0CKSRC[1:0]	
Reset	-	-	-	-	1	0	0	0
Type	RO-0	RO-0	RO-0	RO-0	RW	RW	RW	RW

Bit	Name	Function
7:4	N/A	Reserved bit, read 0
3	T0ON	<p>Timer 0 enable bit</p> <p>1 = enabled (default value is 1, maintaining forward compatibility)</p> <p>0 = disabled</p>
2	T0CKRUN	<p>When the T0 clock is not the selected instruction clock, the operation control bit of the sleep state T0CK</p> <p>1 = T0CK keeps working while sleeping</p> <p>0 = T0CK stops working while sleeping</p>
1:0	T0CKSRC	<p>T0 clock source selection</p> <p>00 = instruction clock</p> <p>01 = HERE</p> <p>10 = LP crystal clock, only meaningful when FOSC is configured in LP or INTOSCIO mode</p> <p>11 = XT crystal clock, only meaningful when FOSC is configured in XT or INTOSCIO mode</p>

11. Timer 1

Timer 1 is a 12-bit timer and includes the following functions:

- ÿ 12-bit counting register
- ÿ 12-bit period register
- ÿ An interrupt is generated when the value of TMR1 is equal to PR1
- ÿ 1:1, 1:4, 1:16 prescaler ratio (shares the same divider with Timer2)

The clock source of Timer1 is controlled by register bit T1CKSRC, and the instruction clock is selected by default.

- ÿ Instruction clock
- ÿ HIRC internal high-speed clock
- ÿ LP crystal clock
- ÿ XT crystal clock

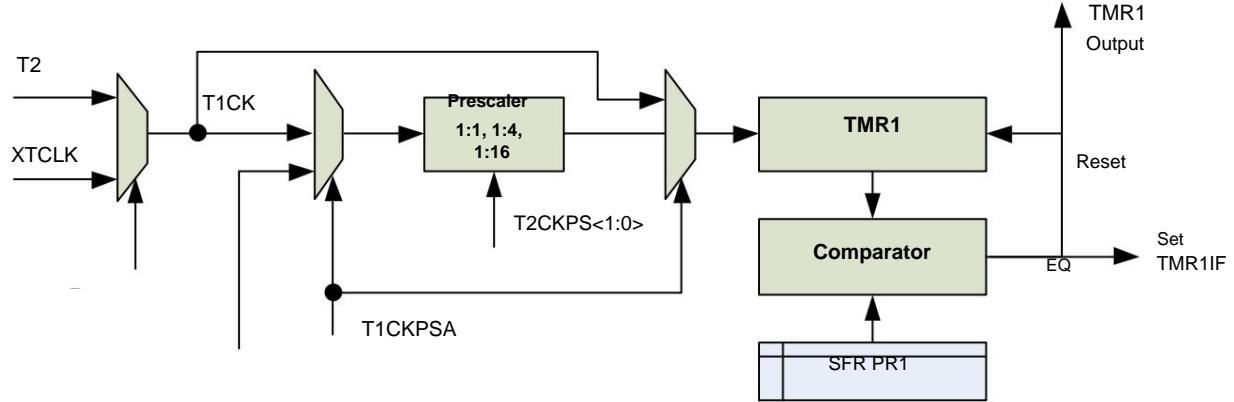


Figure 11.1 Timer 1 block diagram

11.1. Working principle of Timer1

The clock source of the Timer1 module is optional, and the default input is the system instruction clock (FOSC/2). This clock is used to increment the TMR1 register.

The values of {TMR1H, TMR1L} and {PR1H, PR1L} are continuously compared to determine when they match. {TMR1H,TMR1L} will start from 00h

Start incrementing until the value is the same as {PR1H, PR1L}. Two things will happen when matching:

{TMR1H, TMR1L} are reset to 00h in the next increment cycle;

The match output of the Timer1/PR1 comparator is used to set the TMR1IF interrupt flag in the PIR1 register.

{TMR1H, TMR1L} and {PR1H, PR1L} are both readable and writable registers. At reset, their values are 0 and 0xFF respectively. Will

Setting the T1ON bit in the T1CON0 register turns on Timer1, otherwise clearing the T1ON bit turns Timer1 off.



11.2. Reading and writing of Timer1 count value

For specific reading and writing operation steps, please refer to Section 12.3 Reading and Writing Timer2 Count Values.

Note: The write operation of Timer1 will affect the Timer2 prescaler (see section 12.4). In order to avoid affecting the Timer2 count, for Timer1

Clearing to 0 can be circumvented in the following ways:

Read TMR1L, read TMR1H, and get the current count value x;

Write x to PR1H:PR1L, that is, PR1= TMR1;

Write other values to PR1H:PR1L, such as the target matching value of Timer1. At this time, TMR1H:L will be automatically cleared to 0;

11.3. Summary of registers related to Timer1

Name	Address	Bit7		Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	reset value
PR1L	0x116										1111 1111
PR1H	0x117 —										yyyy 1111
TMR1L 0x118											0000 0000
TMR1H 0x119 —											yyyy 0000
T1CON0 0x11A —											yyyo 0000

11.3.1. PR1L register, address 0x116, 0x117

PR1L, address 0x116

Bit	7	6	5	4	3	2	1	0
Name	PR1L[7:0]							
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	PR1L[7:0]	PR1 period register lower 8 bits

PR1H, address 0x117

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	PR1H[3:0]			
Reset	—	—	—	—	1	1	1	1
Type	RO.0	RO.0	RO.0	RO.0	RW	RW	RW	RW

Bit	Name	Function
3:0	PR1H[3:0]	PR1 period register high 4 bits



11.3.2. TMR1 register, address 0x118, 0x119

TMR1L, address 0x118

Bit	7	6	5	4	3	2	1	0
Name	TMR1L[7:0]							
Reset	0000 0000							
Type	RW							

TMR1H, address 0x119

Bit	7	6	5	4	3	2	1	0				
Name	-	-	-	-	TMR1H[3:0]							
Reset	-	-	-	-	0	0	0	0				
Type	RO.0	RO.0	RO.0	RO.0	RW	RW	RW	RW				

Bit	Name	Function
11:0	TMR1	Timer 1 count result register

11.3.3. T1CON0 register, address 0x11A

Bit	7	6	5	4	3	2	1	0			
Name	-	-	-	T1CKPSA T1CKRUN							
Reset	-	-	-	0	0	0	0	0			
Type	RO-0	RO-0	RO-0	RW	RW	RW	RW	RW			

Bit	Name	Function
7:5	N/A	Not implemented, read 0
4	T1CKPSA	<p>Timer1 prescaler allocation bit</p> <p>1 = The prescaler is assigned to Timer1. At this time, regardless of the value of T2ON, Timer2 will start counting.</p> <p>0 = Prescaler assigned to Timer2 module</p>
3	T1CKRUN	<p>When the T1 clock is not the selected instruction clock, the operation control bit of the sleep state T1CK</p> <p>1 = T1CK keeps working while sleeping</p> <p>0 = T1CK stops working while sleeping</p>
2	T1ON	<p>Timer1 enable bit</p> <p>1 = Timer1 is on</p> <p>0 = Timer1 is off</p>
1:0	T1CKSRC	<p>T1 clock source selection</p> <p>00 = instruction clock</p> <p>01 = XT</p> <p>10 = LP crystal clock, only meaningful when FOSC is configured in LP or INTOSCIO mode</p> <p>11 = XT crystal clock, only meaningful when FOSC is configured in XT or INTOSCIO mode</p>

12. Timer 2

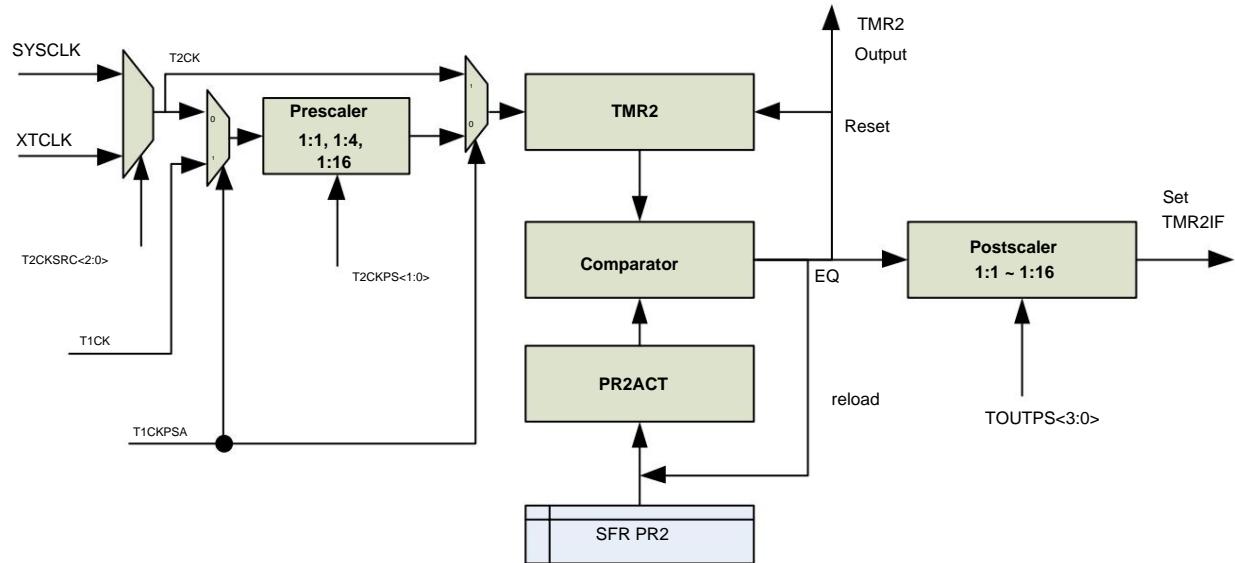


Figure 12.1 Timer 2 block diagram

Timer 2 is a 16-bit timer and includes the following functions:

- ÿ 16-bit counting register
- ÿ 16-bit period register, double buffered
- ÿ An interrupt is generated when the value of TMR2 is equal to PR2
- ÿ 1:1, 1:4, 1:16 prescaler ratio (Timer1 reuses the same prescaler)
- ÿ 1:1~1:16 post-scaler ratio
- ÿ Clock source optional: system clock or internal 32MHz clock (obtained from 2 times the frequency of the crystal) or LIRC



12.1. Working principle of Timer2

In non-PWM mode, the clock input to the Timer2 module is the system command clock. This clock is fed into the Timer2 prescaler, and its prescaler ratio has three options: 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are continuously compared to determine when they match. TMR2 will increment from 00h until it is the same value as PR2. The following two events will occur when

- matching: ý TMR2 is reset to 00h in the next increment
- cycle ý Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is fed into the Timer2 postscaler. Postscaler options range from 1:1 to 1:16. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag in the PIR1 register.

TMR2 and PR2 are both readable and writable registers. At reset, their values are 0 and 0xFFFF respectively.

Setting the TMR2ON bit in the T2CON0 register turns on Timer2, otherwise clearing the TMR2ON bit turns Timer2 off.

The Timer2 prescaler is controlled by the T2CKPS bits of the T2CON0 register.

The Timer2 postscaler is controlled by the TOUTPS bits of the T2CON0 register.

The prescaler and postscaler counters will be cleared when writing to the following registers:

- ý Write TMR2 ý Write
- T2CON0 ý Any reset action

Note:

1. Writing **T2CON0** will not clear the **TMR2** register; 2. The clock source of Timer2 is controlled by **T2CKSRC**. When **T2CKSRC**=000, if **T2CKRUN** is set to 1, Timer2

The clock continues to run during sleep state.

12.2. Updates about PR2

The period register PR2 of Timer2 has a double buffer structure, which are PR2ACT and PR2 inside the module. PR2ACT is the active register, which is the register to be compared by TMR2. Under normal circumstances, PR2ACT will be updated to the content of PR2 only when a matching event occurs in Timer2.

Software can also update PR2ACT after writing the PR2 register without waiting for a match event by writing a 1 to the PR2U bit.

Note: **PR2ACT** is not visible to the software.

12.3. Reading and writing of Timer2 count value

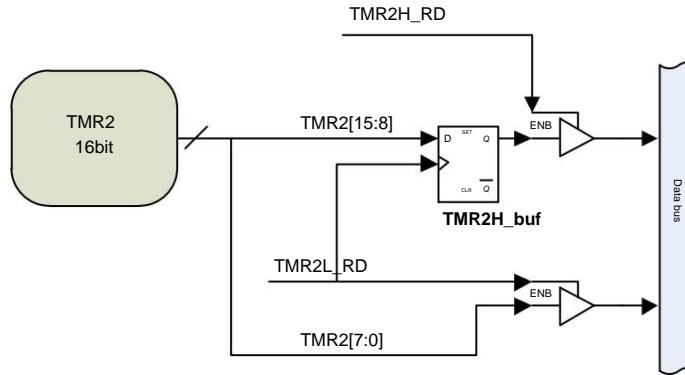


Figure 12.2 Principle block diagram of reading operation of Timer2 count value

Timer2 is a 16-bit timer. Since the internal data bus is limited to 8 bits, software needs to read the count value of Timer2 twice.

The lower 8 bits of the count value TMR2L can be accessed directly, and the upper 8 bits have an internal cache TMR2H_buf, which is read by software in TMR2L. are updated all the time. This mechanism ensures that even if Timer2 is counting, the software can always read a complete 16-bit count value to avoid This avoids situations such as Timer2 overflowing between two reads.

To sum up, read operations should be performed in the following order:

- ÿ Read TMR2L;
- ÿ Read TMR2H;

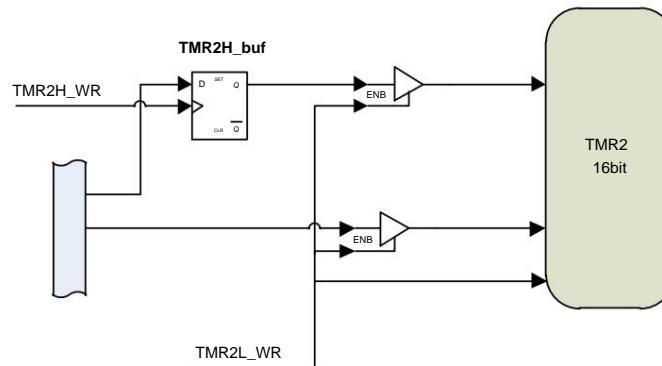


Figure 12.3 Principle block diagram of writing operation of Timer2 count value

Similar to the read operation, software writing to the TMR2H register does not immediately update the internal count value, but first writes to the cache TMR2H_buf. When the software writes TMR2L, the hardware automatically updates the high 8 bits of the cache to the count value.

Writing order:

- ÿ Write TMR2H;
- ÿ Write TMR2L;

Note: When Timer2 works on an asynchronous clock, it is recommended to clear the TMR2ON bit first to stop counting, and then wait for at least 1 count clock. Initiate the read of TMR2 again.

In addition, for write operations, it is recommended that the user directly stops the counter and then writes the desired value. If the register is counting up, the

Writing to the timer register may cause write contention, which may cause unpredictable events in the TMR2H:TMR2L register pair.

measured value.

12.4. Timer2 prescaler clearing

When the software performs the following actions, the prescaler is automatically cleared to 0, and Timer2 will stop counting one instruction
clock. ÿ Write TMR2H;
ÿ Write TMR2L; ÿ
Write TMR1H; ÿ Write
TMR1L; ÿ Write T2CON;

12.5. Timer2 clock source

Timer2 supports 6 different clock sources: ÿ
Instruction clock ÿ
System clock ÿ 2
times the frequency of HIRC
ÿ 2 times the frequency of the crystal/external clock (only valid when FOSC is configured in LP/XT or EC mode)
ÿ HIRC
ÿ LIRC
ÿ LP crystal clock (valid only when FOSC is configured as INTOSCIO, or LP mode) ÿ XT crystal
clock (valid only when FOSC is configured as INTOSCIO, or XT mode)

12.6. Working while sleeping

Timer2 will keep counting in SLEEP mode when the following conditions are true:
a) T2ON=1, T2CKRUN=1, T2CKSRC selects a non-instruction clock and is legal (see register description); or b)
T1CKPSA=1 and T2CKSRC selects a clock that is consistent with T1CKSRC. The selected clock is consistent, regardless of the value of T2ON, Timer2 will work;

12.7. Summary of registers related to Timer2

name	address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value
TMR2L	0x11									0000 0000
TMR2H	0x13									0000 0000
INTCON 0x0B/8B		GIE	LIKE THIS	T0IE	NOT	PAY	T0IF	INTF	PAIF	0000 0000
PIE1	0x8C	THIS	CKMIE LVDIE ACMPIE TMR1IE OSFIE				TMR2IE	ADCIE	0000 0000	
PIR1	0x0C	EEIF	CKMIF LVDIF ACMPIF TMR1IF OSFIF				TMR2IF	ADCIF	0000 0000	
MSCON0 0x1B	BGRBOE LVRoe ROMLPE CLKOS SLVREN CKMAVG CKCNTI T2CKRUN									0001 0000
PR2L	0x91									1111 1111
PR2H	0x92									1111 1111
T2CON0 0x12		PR2U		TOUTPS[3:0]			TMR2ON	T2CKPS[1:0]		0000 0000
T2CON1	0x9E		-		P1OS P1BZM			T2CKSRC[2:0]		ÿÿÿ0 0000

12.7.1. PR2 register, address 0x91, 0x92

See [PR2L register, address 0x91](#), [PR2H register, address 0x92](#).

12.7.2. TMR2 register, address 0x11, 0x13

TMR2L, address 0x11

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Reset	0000 0000							
Type	RW							

TMR2H, address 0x13

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Reset	0000 0000							
Type	RW							

Bit	Name	Function
15:0	TMR2	Timer 2 count result register

12.7.3. T2CON0 register, address 0x12

Bit	7	6	5	4	3	2	1	0
Name	PR2U	TOUTPS[3:0]					TMR2ON	T2CKPS[1:0]
Reset	0	0000					0	00
Type	WO-1	RW	RW	RW	RW	RW	RW	

Bit	Name	Function
7	PR2U	<p>Software update control bits of PR2 and P1xDTy registers, write only</p> <p>Write 1: Update the PR2/P1xDTy buffer value to the PR2 register and P1xDTy_ACT respectively</p> <p>Write 0: meaningless</p>
6:3	TOUTPS	<p>TOUTPS<3:0>: Timer2 Output Postscaler Select bits Timer 2 output postscaler selection</p> <p>0000 = 1:1 postscaler ratio 0001 = 1:2 postscaler ratio 0010 = 1:3 postscaler ratio 0011 = 1:4 postscaler ratio 0100 = 1:5 postscaler ratio 0101 = 1:6 postscaler ratio 0110 = 1:7 postscaler ratio 0111 = 1:8 postscaler ratio 1000 = 1:9 postscaler ratio 1001 = 1:10 postscaler ratio 1010 = 1:11 postscaler ratio 1011 = 1:12 postscaler ratio 1100 = 1:13 postscaler ratio 1101 = 1:14 postscaler ratio 1110 = 1:15 postscaler ratio 1111 = 1:16 postscaler ratio</p>
2	TMR2ON	<p>TMR2ON: Timer2 On bit Turn on timer 2</p> <p>1 = Timer2 is on 0 = Timer2 is off</p> <p>In PWM1 single pulse mode, this bit is automatically cleared to 0</p>
1:0	T2CKPS/T1CKPS	<p>T2CKPS<1:0>/T1CKPS<1:0>: Timer2/Timer1 Clock Prescale Select bits Timer2/Timer1</p> <p>Drive clock prescaler selection</p> <p>00 = Prescaler is 1 01 = Prescaler is 4 1x = Prescaler is 16</p>

12.7.4. T2CON1 register, address **0x9E**

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	P1OS	P1BZM	T2CKSRC[2:0]		
Reset	-	-	-	0	0	0	0	0
Type	RO-0	RO-0	RO-0	RW	RW	RW	RW	RW

Bit	Name	Function
7:5	N/A	Reserved bit, read 0
4	P1OS	<p>PWM1 single pulse mode selection</p> <p>0 = continuous mode</p> <p>1 = single pulse mode</p>
3	P1BZM	<p>PWM1 buzzer mode selection</p> <p>0 = PWM mode</p> <p>1 = buzzer mode</p>
2:0	T2CKSRC	<p>Timer2 clock source selection</p> <p>000 = instruction clock</p> <p>001 = system clock</p> <p>010 = 2 times HIRC</p> <p>011 = Crystal/External Clock Multiplier of 2 (valid only when FOSC is configured in LP/XT or EC mode)</p> <p>100 = HIRC</p> <p>101 = LIRC</p> <p>110 = LP crystal clock (valid only when FOSC is configured as INTOSCIO, or LP mode)</p> <p>111 = XT crystal clock (valid only when FOSC is configured as INTOSCIO, or XT mode)</p>

13.PWM module

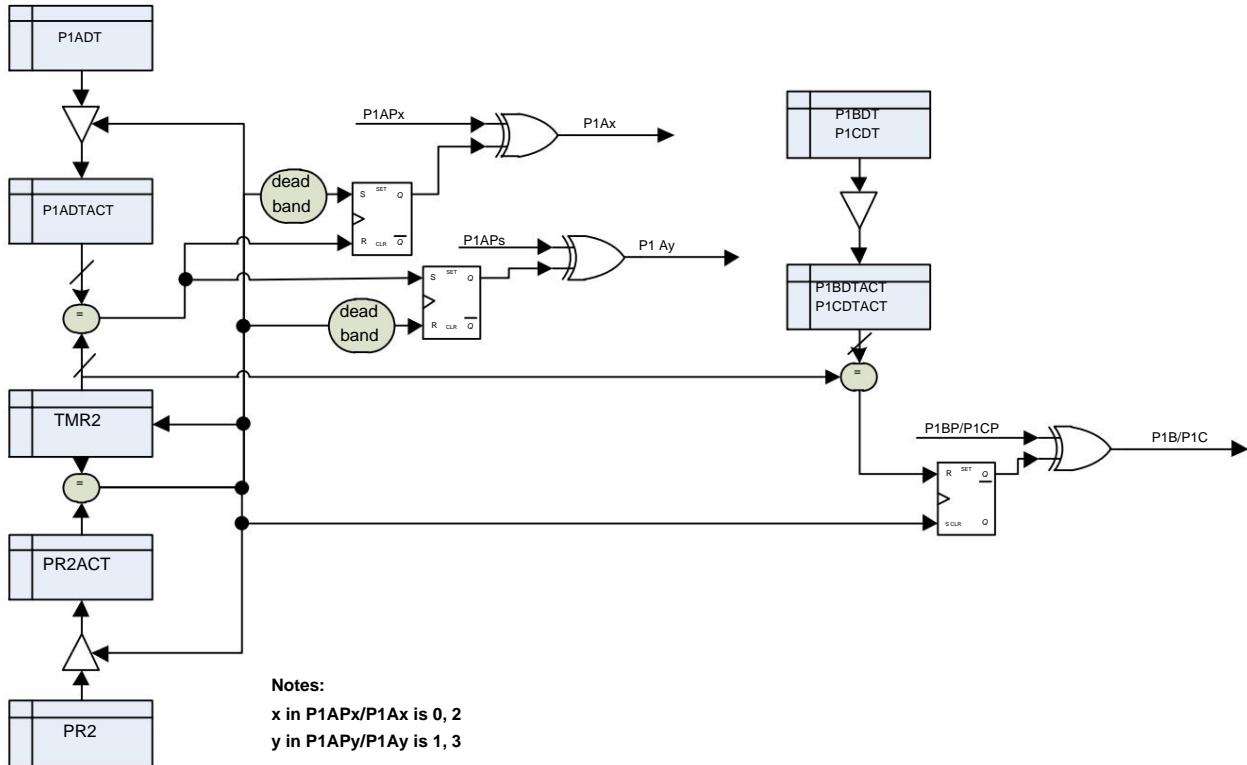


Figure 13.1 PWM structure block diagram

PWM supports the following features:

- ÿ 16bit resolution
- ÿ Cycle and duty cycle matching double buffer design
- ÿ 1 PWM output with dead zone control: P1A
- ÿ 4 channels of PWM output with independent duty cycle: P1A, P1B, P1C, P1D
- ÿ The polarity of each PWM output can be set independently
- ÿ Fault braking and automatic restart

13.1.Cycle

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using Equation 13.1.

$$\text{PWM period} = (\text{PR2} + 1) * \text{TT2CK} * (\text{TMR2 prescaler value}) \text{ When TMR2}$$

Official 13.1

equals PR2, the following three events will occur in the next increment cycle:

- ÿ TMR2 is cleared
- ÿ P1A0, [P1A0], P1B, P1C, P1D are set to 1 (when all 4 PWM channels are active high)
- ÿ The internal period register PR2ACT and duty cycle register P1xDTACT are updated

13.2.Duty cycle

The PWM duty cycle is specified by writing a 16-bit value to the following registers:

P1xDTL(x= A, B, C, D)

P1xDTH(x= A, B, C, D)

Among them, P1xDTH holds the 8-bit MSb of the 4-way PWM duty cycle register, and P1xDTL holds the lower 8 bits. Due to the internal double-buffering design, the duty cycle register is written at any time, which plays an important role in preventing PWM glitches when the software changes the duty cycle.

Equation 13.2 is used to calculate the PWM pulse width.

Equation 13.3 is used to calculate the PWM duty

cycle. Pulse width = P1xDT*TT2CK*(TMR2 prescaler value)

Official 13.2

Duty cycle = P1xDT/(PR2+1)

Official 13.3

13.3.Clock source selection

The time base timer used by PWM1 is Timer2. The clock source of Timer2 has the following

options:

- ÿ System

- clock
- ÿ Instruction clock (i.e. system clock divided by 2 or 4)
- ÿ HIRC

- multiplied by 2
- ÿ External

- clock multiplied by 2 (Only valid when FOSC is configured in EC mode)

- ÿ HIRC

- ÿ LIRC

13.4. PWM status during sleep

When T2CKRUN=1 and the clock source of Timer2 is not the selected instruction clock, after the MCU enters sleep, the PWM can remain in the running state, and the clock source selected by **T2CKSRC** will not be turned off. Otherwise, Timer2 will stop counting, and the levels of each PWM pin remain in the state after executing the SLEEP instruction.

13.5. P1A dead time

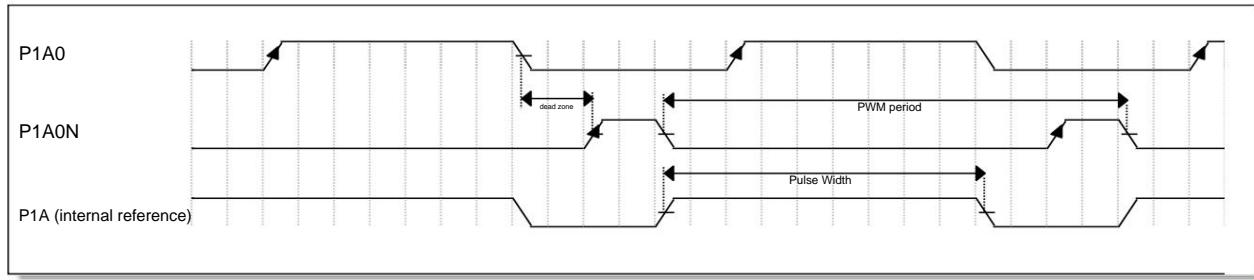


Figure 13.2 Dead zone PWM schematic

diagram has 1 PWM with complementary output, P1Ax. Among them, P1A0/[P1A1]/[P1A2] are defined as positive output, and [P1A0N]/[P1A1N]/[P1A2N] are defined as complementary output. The PWM of P1A has a dead-time insertion function, and its dead-time is controlled by P1DC[6:0]. The dead-time timer uses the Timer2 clock as the

counting clock source. Note: {P1A0, P1A0N}, {P1A1, P1A1N}, {P1A2, P1A2N}, these three pairs of complementary outputs share the same dead zone setting.

13.6. Failure brake

The PWM1 module supports fault braking mode, which disables PWM output when an external braking event occurs, while Timer2 and prescaler are in reset state. Brake mode puts the PWM output pins into a predetermined state and the module is used to prevent PWM damaging applications in the event of a fault condition.

Use the P1BKS bit of the P1BR0 register to select the fault source. The fault event can be the following:

ÿ BKIN pin is low level
ÿ BKIN pin is high level

LVDW is set to 1 by the LVD module

ÿ LVDW=1 or BKIN=0
ÿ LVDW=1 or

BKIN=1
ÿ ADC threshold comparison

is 1

The brake status is indicated by the P1BEVT bit of the P1BR0 register. If this bit is 0, the PWM1 pin operates normally. If this bit is 1, the PWM1 output is off.

Note: The braking source LVDW can choose to debounce, which is determined by the LVDDEB register bit.

13.6.1. Braking status

When a fault occurs, the level state of the PWM1 pin under the fault is selected by the register P1xSS bit, and has the following types:

- ÿ PWM1 is set to active level
- ÿ PWM1 is placed at an inactive level
- ÿ PWM1 is turned off and is in a floating high-impedance state.
- ÿ The TMR2 timer stops counting and the prescaler counter is reset.
- ÿ TMR2ON bit is not affected

The effective level is determined by each register bit of P1POL.

13.6.2. Fault clearing

The fault brake condition is a level-based signal, not an edge-based signal. As long as the fault condition is valid, the fault status remains and the soft

The software cannot be cleared; P1BEVT may be cleared to 0 only when the relevant fault input or LVD event is eliminated.

13.6.3. Automatic restart

PWM1 can be configured to automatically restart the PWM1 signal when the fault condition is cleared. By setting the P1AUE bit in the P1CON register

Enable automatic restart.

When auto-restart is enabled, the P1BEVT bit remains set as long as the fault condition is valid. When the fault condition is cleared, the P1BEVT flag

will be cleared by hardware and TMR2 resumes counting. When the next count overflows, the actual control signal P1BEVT is cleared and PWM1 returns to normal.

Normal output. .

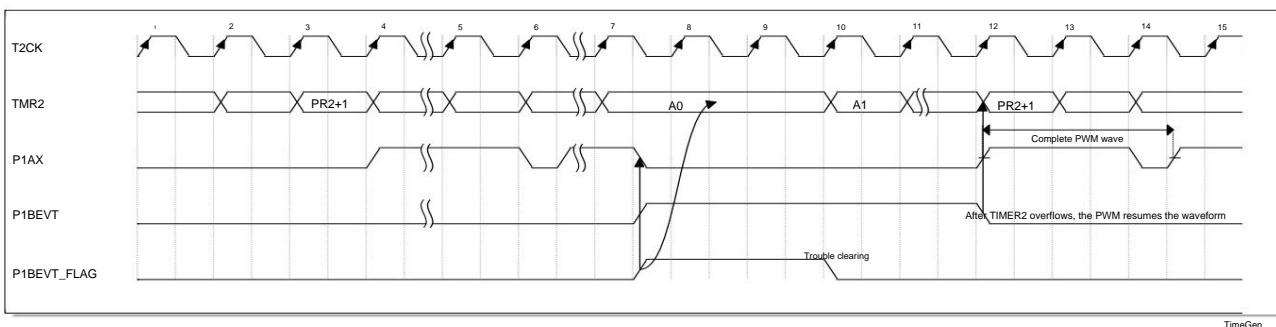


Figure 13.3 PWM automatic restart timing diagram

13.7. Updates on period and duty cycle registers

When Timer2 has been turned on, the update of the period and each duty cycle register requires matching events of TMR2 and PR2. If the user doesn't want to wait, you can update immediately by writing PR2U bit.

When TMR2ON is 0, software writes to the PR2, {P1xDTH, P1xDTL} registers will be immediately updated to the corresponding working registers.

When the PWM output maintains the old value, it will not change due to changes in the PR2 or P1xDT register.

Note: The working register **xxxACT** is not visible to the software, and the software can only read **PR2** and **P1xDTL**, **P1xDTH**.

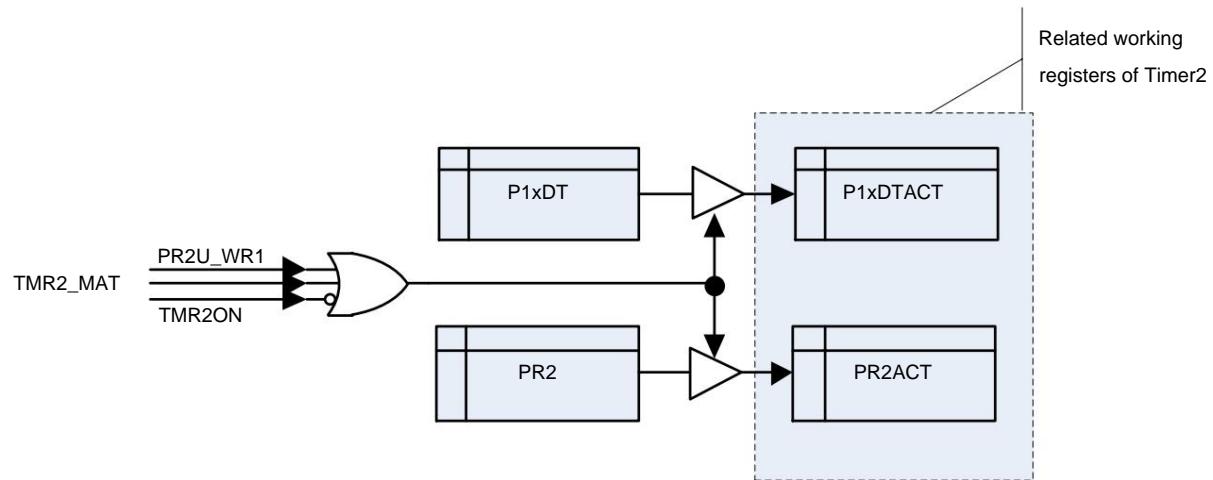


Figure 13.4 T2 working register update

Although the double buffering of period and duty cycle ensures that the PWM output will not cause glitches to a large extent, if the software is very close to the TMR2 match Always write to this register, especially when the T2 clock frequency is faster than the system clock frequency, unpredictable situations may occur.

As a result, the value of the working register group is not the expected value, see Figure 13.5 below.

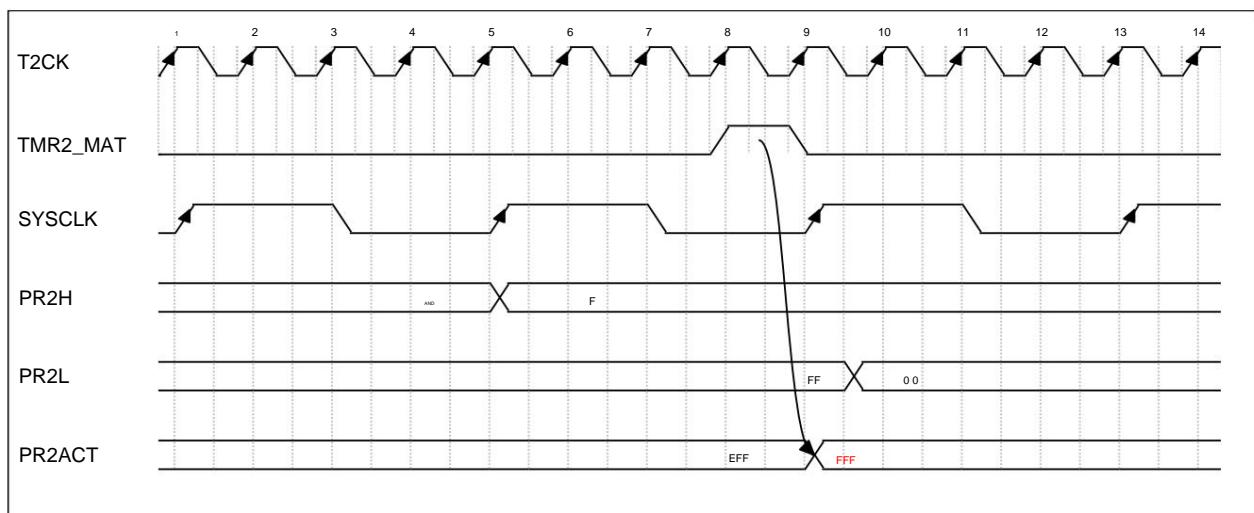


Figure 13.5 PR2ACT is updated to the unexpected value FFF (expected value is F00)

Therefore, it is strongly recommended to update **PR2** and **xxxDT** only in the **TMR2** matching interrupt.

13.8. Buzzer mode (Buzzer)

When T2CON1.P1BZM is set to 1, the PWM1 mode will be used as a buzzer output. In this mode, the duty cycle setting register does not

When activated, P1Ax, P1B, and P1C will output a square wave with a period of $(2 * (PR2+1) * TT2CK * TMR2 prescaler)$.

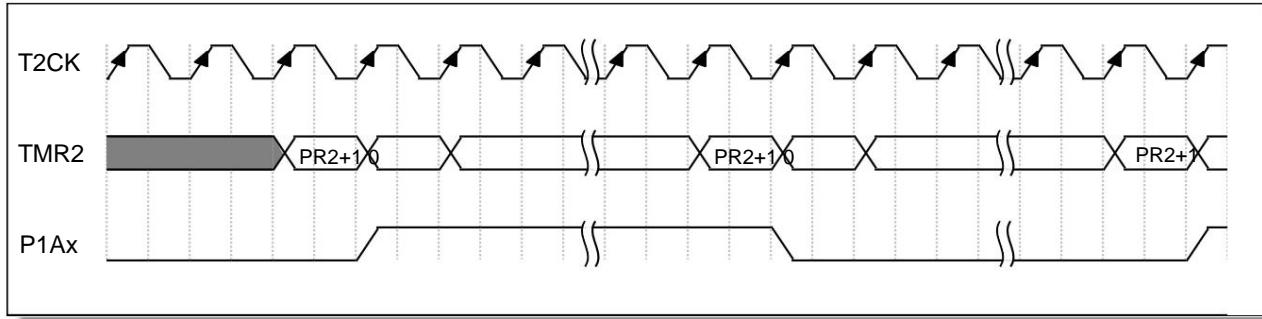


Figure 13.6 Buzzer mode output

13.9. Single pulse output

When P1OS is set to 1, PWM1 is in single pulse output mode. In this mode, the first match of TMR2 and (PR2+1)

Will cause P1Ax, P1B, P1C to output PWM pulses. At the next match, TMR2ON is turned off by hardware, and the P1XOE of the corresponding pin

Enable will also be turned off.

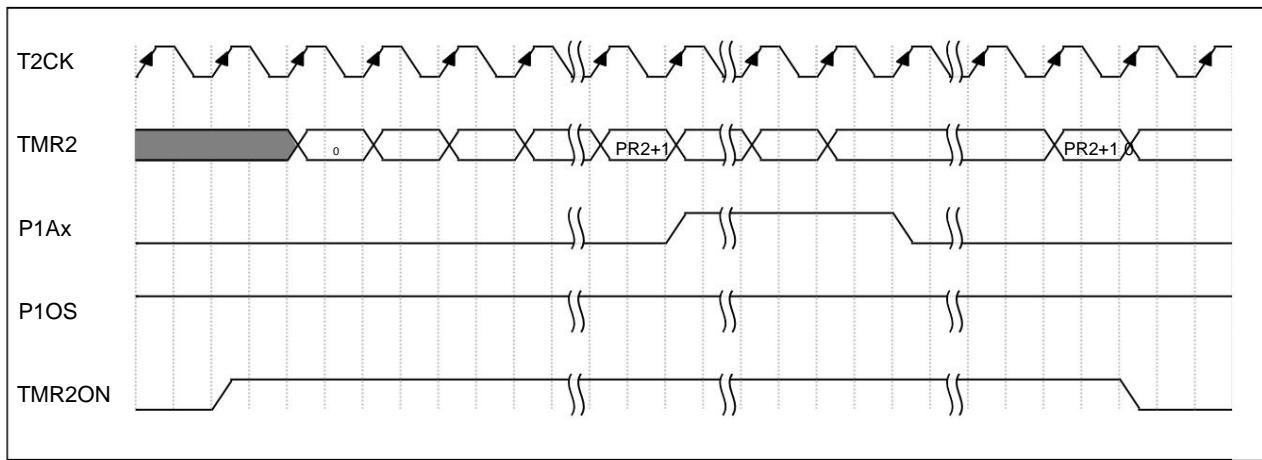


Figure 13.7 Single pulse mode output

13.10. PWM output remapping

The four PWM channels P1A, P1B, P1C and P1D can be mapped to different I/Os respectively and are controlled by registers P1OE0 and P1OE1.

Their reset value is 0, and the specific mapped I/O can be found in the pin diagrams and pin descriptions in Chapter 1 of this document.

This feature allows the same PWM output on two I/Os at the same time.

13.11. The second function output of P1C and P1D

In addition to the normal PWM waveform output, the remapping pin (PB0) of P1C can be configured to output the same or exclusive output between P1C and P1D, or result, controlled by registers P1CF2E and P1CF2. The remapping pins (PA3, PA2) of P1D can be configured to output P1B, The results of exclusive OR and exclusive OR between P1C are controlled by registers P1DF2E and P1DF2.

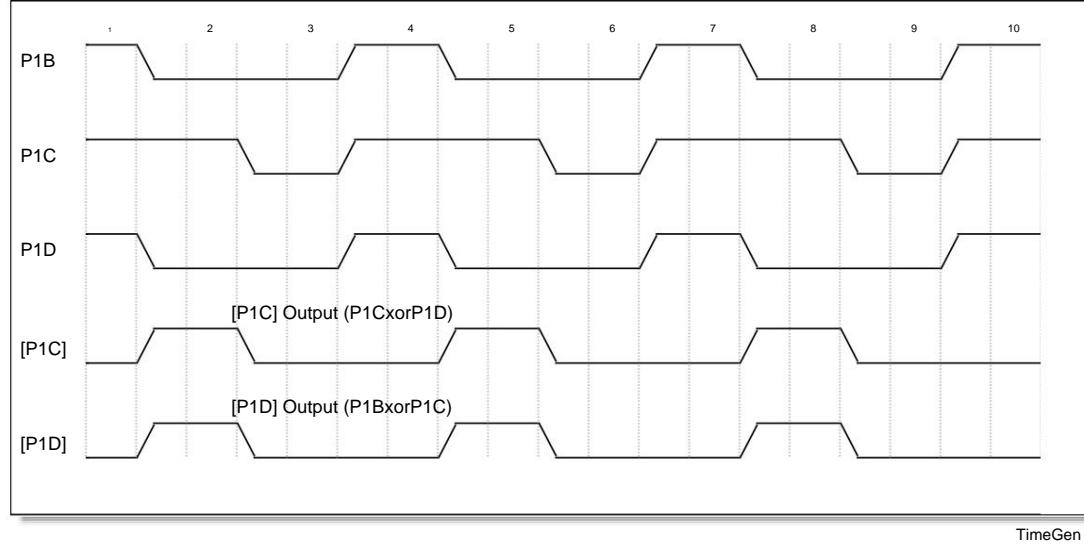


Figure 13.8 2nd function timing example of P1B and P1C

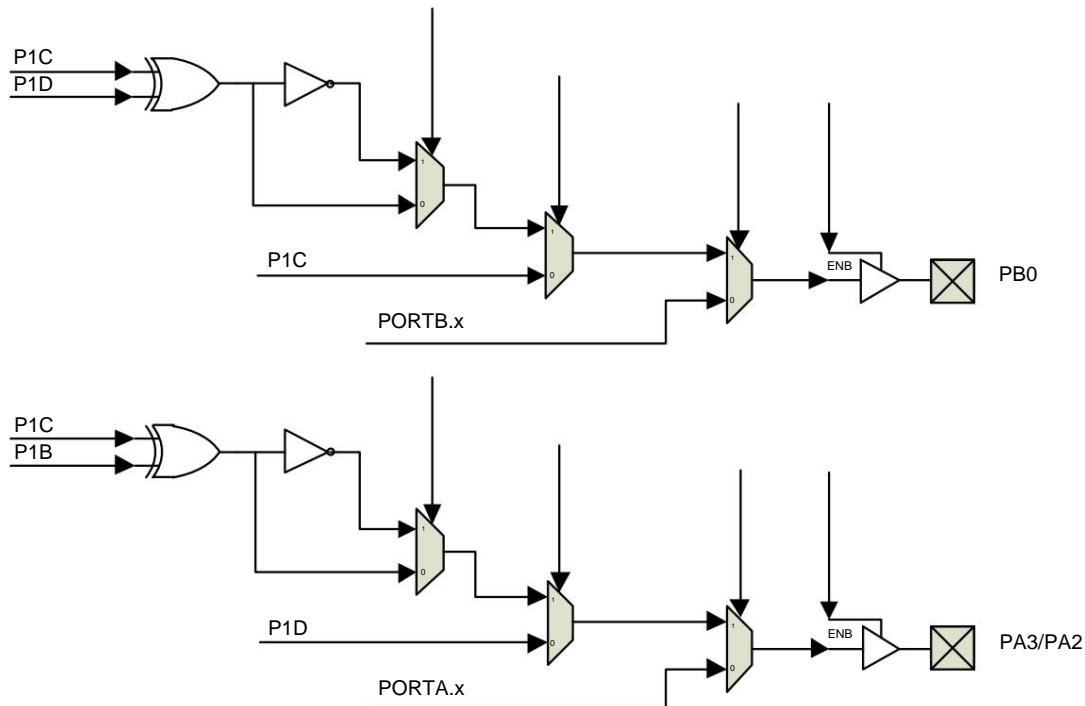


Figure 13.9 Second function output of P1C and P1D

13.12. Summary of registers related to PWM1

Name address bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value					
P1ADTL 0xE	P1A duty cycle lower 8 bits							0000 0000					
P1BDTL 0xF	P1B duty cycle lower 8 bits							0000 0000					
P1CDTL 0x10	P1C duty cycle lower 8 bits							0000 0000					
P1DDTL 0x08	P1D duty cycle lower 8 bits							0000 0000					
TMR2L 0x11	Timer2 counter low 8 bits							0000 0000					
TMR2H 0x13	Timer2 counter high 8 bits							0000 0000					
T2CON0 0x12	PR2U	TOUTPS			TMR2ON	T2CKPS		0000 0000					
T2CON1 0x9E	-		P1OS	P1BZM	T2CKSRC			ÿÿ0 0000					
P1ADTH 0x14	P1A duty cycle is 8 bits higher							0000 0000					
P1BDTH 0x15	P1B duty cycle is 8 bits higher							0000 0000					
P1CDTH 0x1A	P1C duty cycle high 8 bits							0000 0000					
P1DDTH 0x09	P1D duty cycle is 8 bits higher							0000 0000					
P1CON 0x16	P1AUE	P1DC						0000 0000					
P1BR0 0x17	P1BEVT	P1BKS		P1BSS		P1ASS		0000 0000					
P1BR1 0x19	P1D2SS		P1DSS		P1C2SS		P1CSS						
P1OE2 0x11	P1D2OE	P1D1OE	P1D0OE	-	-	P1C1OE	P1B1OE	- 000ÿ 000ÿ					
P1OE 0x90	P1C0OE	P1B0OE	P1A2NOE	P1A2OE	P1A1NOE	P1A1OE	P1A0NOE	P1A0OE 0000 0000					
PR2L 0x91	PR2[7:0]							1111 1111					
PR2H 0x92	PR2[15:8]							1111 1111					
P1POL 0x99	P1C0P	P1B0P	P1A2NP	P1A2P	P1A1NP	P1A1P	P1A0NP	P1A0P 0000 0000					
P1POL2 0x109	P1D2P	P1D1P	P1D0P	-	-	P1C1P	P1B1P	- 000ÿ 000ÿ					
P1AUX 0x1E	-	-	P1B2SS[1:0]		P1CF2E	P1CF2	P1DF2E	P1DF2 ÿ00 0000					

13.12.1. P1ADTL register, address 0x0E

Bit	7	6	5	4	3	2	1	0
Name	P1ADTL[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1ADTL	P1A duty cycle register lower 8 bits



13.12.2. P1BDTL register, address 0x0F

Bit	7	6	5	4	3	2	1	0
Name	P1BDTL[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1BDTL	P1B duty cycle register lower 8 bits

13.12.3. P1CDTL register, address 0x10

Bit	7	6	5	4	3	2	1	0
Name	P1CDTL[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1CDTL	P1C duty cycle register lower 8 bits

13.12.4. P1DDTL register, address 0x8

Bit	7	6	5	4	3	2	1	0
Name	P1DDTL[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
3:0	P1DDTL	P1D duty cycle register lower 8 bits

13.12.5. TMR2L register, address 0x11

Bit	7	6	5	4	3	2	1	0
Name	TMR2L[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	TMR2L	Timer2 counter low 8 bits

13.12.6. TMR2H register, address 0x13

Bit	7	6	5	4	3	2	1	0
Name	TMR2H[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
3:0	TMR2H	Timer2 counter high 8 bits

13.12.7. T2CON0 register, address 0x12

See [T2CON0 register, address 0x12](#).

13.12.8. P1ADTH register, address 0x14

Bit	7	6	5	4	3	2	1	0
Name	P1ADTH[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1ADTH	P1A duty cycle register high 8 bits

13.12.9. P1BDTH register, address 0x15

Bit	7	6	5	4	3	2	1	0
Name	P1BDTH[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1BDTH	P1B duty cycle register high 8 bits



13.12.10. P1CDTH register, address 0x1A

Bit	7	6	5	4	3	2	1	0
Name	P1CDTH[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1CDTH	P1C duty cycle register high 8 bits

13.12.11. P1DDTH register, address 0x9

Bit	7	6	5	4	3	2	1	0
Name	P1DDTH[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	P1DDTH	P1D duty cycle register high 8 bits

13.12.12. P1CON register, address 0x16

Bit	7	6	5	4	3	2	1	0	
Name	P1AUE	PDC[6:0]							
Reset	0	0	0	0	0	0	0	0	
Type	RW	RW	RW	RW	RW	RW	RW	RW	

Bit	Name	Function
7	P1AUE	PWM1 restart enable bit 1 = During fault braking, the P1BEVT bit is automatically cleared when exiting the shutdown event, and PWM1 automatically restarts 0 = During fault braking, P1BEVT must be cleared by software to restart PWM1
6:0	P1DC	PWM1 dead time setting P1DCn = Number of T2CK cycles between when the scheduled PWM signal should transition to active and when the PWM signal actually transitions to active

13.12.13. P1BR0 register, address 0x17

Bit	7	6	5	4	3	2	1	0
Name	P1BEVT	P1BKS[2:0]			P1BSS[1:0]		P1ASS[1:0]	
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	P1BEVT	<p>PWM1 fault event status bit</p> <p>1 = A fault event has occurred</p> <p>0 = No fault event has occurred, PWM1 output is operating normally</p>
6:4	P1BKS	<p>PWM1 fault source selection bit</p> <p>000 = Disable fault braking function</p> <p>001 = BKIN is low</p> <p>010 = BKIN is high</p> <p>011 = LVDW=1</p> <p>100 = BKIN is low or LVDW=1</p> <p>101 = BKIN is high or LVDW=1</p> <p>110 = ADC threshold comparison</p> <p>111 = Reserved (disable fault braking)</p>
3:2	P1BSS	<p>Under fault, the state of the P1B0 pin (the level polarity is determined by the P1POLx register)</p> <p>00 = high resistance</p> <p>01 = invalid level</p> <p>1x = active level</p>
1:0	P1ASS	<p>Under fault, the state of the P1A pin (the level polarity is determined by the P1POLx register)</p> <p>00 = high resistance</p> <p>01 = invalid level</p> <p>1x = active level</p>

13.12.14. P1BR1 register, address 0x19

Bit	7	6	5	4	3	2	1	0
Name	P1D2SS[1:0]		P1DSS[1:0]		P1C2SS[1:0]		P1CSS[1:0]	
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:6	P1D2SS	<p>Under a fault, the status of the [P1D1]/[P1D2] pins is only valid when P1D1OE/P1D2OE is 1.</p> <p>00 = high resistance 01 = output 0 1x = output 1</p>
5:4	P1DSS	<p>The state of the P1D0 pin under fault (the level polarity is determined by the P1POLx register)</p> <p>00 = high resistance 01 = invalid level 1x = active level</p>
3:2	P1C2SS	<p>Under a fault, the status of the [P1C1] pin is only valid when P1C1OE is 1</p> <p>00 = high resistance 01 = output 0 1x = output 1</p>
1:0	P1CSS	<p>The state of the P1C0 pin under fault (the level polarity is determined by the P1POLx register)</p> <p>00 = high resistance 01 = invalid level 1x = active level</p>

13.12.15. P1OE2 register, address 0x11B

Bit	7	6	5	4	3	2	1	0
Name	P1D2OE	P1D1OE	P1D0OE	-	-	P1C1OE	P1B1OE	-
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RO.0	RO.0	RW	RW	RO.0

Bit	Name	Function
7	P1D2OE	P1D2 output enable, high effective 1 = P1D2 output to associated pin 0 = P1D2 is not output to the relevant pin
6	P1D1OE	P1D1 output enable, high effective 1 = P1D1 output to associated pin 0 = P1D1 is not output to the relevant pin
5	P1D0OE	P1D0 output enable, high effective 1 = P1D0 output to relevant pin 0 = P1D0 is not output to the relevant pin
4:3	N/A	Reserved bit, read 0
2	P1C1OE	P1C1 output enable, high active 1 = P1C1 output to associated pin 0 = P1C1 is not output to the relevant pin
1	P1B1OE	P1B1 output enable, high effective 1 = P1B1 output to associated pin 0 = P1B1 is not output to the relevant pin
0	N/A	Reserved bit, read 0

13.12.16. P1OE register, address 0x90

Bit	7	6	5	4	3	2	1	0
Name	P1C0OE	P1B0OE	P1A2NOE	P1A2OE	P1A1NOE	P1A1OE	P1A0NOE	P1A0OE
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	P1C0OE	P1C0 output enable, high effective 1 = P1C0 output to associated pin 0 = P1C0 is not output to the relevant pin
6	P1B0OE	P1B0 output enable, high effective 1 = P1B0 output to relevant pin 0 = P1B0 is not output to the relevant pin
5	P1A2NOE	P1A2N output enable, high active 1 = P1A2N output to associated pin 0 = P1A2N does not output to the relevant pin
4	P1A2OE	P1A2 output enable, high effective 1 = P1A2 output to associated pin 0 = P1A2 is not output to the relevant pin
3	P1A1NOE	P1A1N output enable, high active 1 = P1A1N output to associated pin 0 = P1A1N does not output to the relevant pin
2	P1A1OE	P1A1 output enable, high effective 1 = P1A1 output to associated pin 0 = P1A1 is not output to the relevant pin
1	P1A0NOE	P1A0N output enable, high effective 1 = P1A0N output to relevant pin 0 = P1A0N is not output to the relevant pin
0	P1A0OE	P1A0 output enable, high effective 1 = P1A0 output to relevant pin 0 = P1A0 is not output to the relevant pin

13.12.17. PR2L register, address 0x91

Bit	7	6	5	4	3	2	1	0
Name	PR2L[7:0]							
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	PR2L	PR2 period register lower 8 bits

13.12.18. PR2H register, address 0x92

Bit	7	6	5	4	3	2	1	0
Name	PR2H[7:0]							
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	PR2H	PR2 period register high 8 bits

13.12.19. P1POL register, address 0x99

Bit	7	6	5	4	3	2	1	0
Name	P1C0P	P1B0P	P1A2NP	P1A2P	P1A1NP	P1A1P	P1A0NP	P1A0P
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7	P1C0P	P1C0 output polarity setting 1 = P1C0 active low 0 = P1C0 active high
6	P1B0P	P1B0 output polarity setting 1 = P1B0 active low 0 = P1B0 is active high
5	P1A2NP	P1A2N output polarity setting 1 = P1A2N active low 0 = P1A2N active high
4	P1A2P	P1A2 output polarity setting 1 = P1A2 active low 0 = P1A2 is active high
3	P1A1NP	P1A1N output polarity setting 1 = P1A1N active low 0 = P1A1N active high
2	P1A1P	P1A1 output polarity setting 1 = P1A1 active low 0 = P1A1 active high
1	P1A0NP	P1A0N output polarity setting 1 = P1A0N active low 0 = P1A0N is active high
0	P1A0P	P1A0 output polarity setting 1 = P1A0 active low 0 = P1A0 is active high

13.12.20. P1POL2 register, address 0x109

Bit	7	6	5	4	3	2	1	0
Name	P1D2P	P1D1P	P1D0P	-	-	P1C1P	P1B1P	-
Reset	0	0	0	-	-	0	0	-
Type	RW	RW	RW	RO.0	RO.0	RW	RW	RO.0

Bit	Name	Function
7	P1D2P	[P1D2] Output polarity setting When outputting P1D waveform 1 = [P1D2] active low 0 = [P1D2] active high When outputting the second function waveform 1 = Second function reverse waveform 0 = Second function waveform
6	P1D1P	[P1D1] Output polarity setting 1 = [P1D1] active low 0 = [P1D1] active high When outputting P1D second function waveform 1 = Second function reverse waveform 0 = Second function waveform
5	P1D0P	P1D output polarity setting 1 = P1D active low 0 = P1D active high
4:3	N/A	Reserved bit, read 0
2	P1C1P	[P1C1] Output polarity setting 1 = [P1C1] active low 0 = [P1C1] active high When outputting P1C second function waveform 1 = Second function reverse waveform 0 = Second function waveform
1	P1B1P	[P1B1] Output polarity setting 1 = [P1B1] active low 0 = [P1B1] active high
0	N/A	Reserved bit, read 0

13.12.21. P1AUX register, address 0x1E

Bit	7	6	5	4	3	2	1	0
Name	-	-	P1B2SS[1:0]		P1CF2E	P1CF2	P1DF2E	P1DF2
Reset	-	-	0	0	0	0	0	0
Type	RO-0	RO-0	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:6	N/A	Reserved bit, read 0
5:4	P1B2SS	<p>Under a fault, the status of the [P1B1] pin is only valid when P1B1OE is 1</p> <p>00 = high resistance 01 = output 0 1x = output 1</p>
3	P1CF2E	<p>When P1C1OE is 1, the second function of [P1C1] pin is enabled</p> <p>1 = Outputs the exclusive OR of P1C and P1D 0 = Output P1C</p>
2	P1CF2	<p>[P1C1] Pin 2 function selection</p> <p>1 = Outputs the exclusive OR of P1C and P1D 0 = Outputs the XOR of P1C and P1D</p>
1	P1DF2E	<p>When P1D1OE/P1D2OE is 1, the second function of [P1D1]/[P1D2] pin is enabled</p> <p>1 = Outputs the exclusive OR of P1B and P1C 0 = Output P1D</p>
0	P1DF2	<p>[P1D1]/[P1D2] pin 2nd function selection</p> <p>1 = Outputs the exclusive OR of P1B and P1C 0 = Outputs the XOR of P1B and P1C</p>

14.I/O end

This chip contains a total of 18 GPIOs. In addition to being ordinary input/output ports, these IOs usually have some connections with the core peripheral circuits.

The functions of messaging are detailed below.

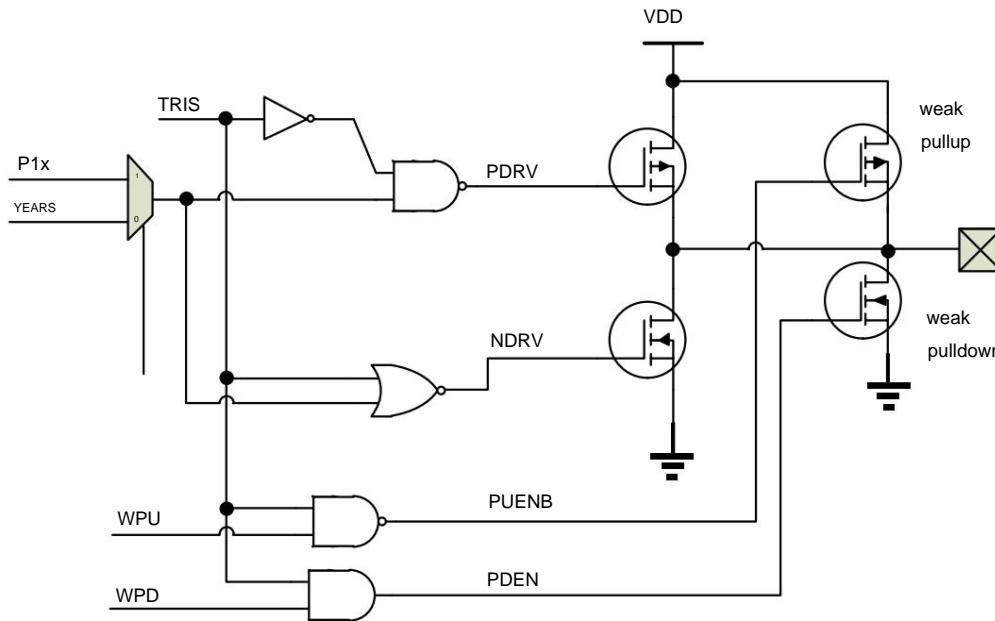


Figure 14.1 General structure of I/O

14.1. PORTx port and TRISx register

All pins on the chip are bidirectional ports, and the corresponding entry and exit direction control register is the TRISx register. If the bits of TRISx are 1, the pin will be used as an input pin, otherwise setting a certain bit to 0 will set the corresponding PORTx port as an output port. set as output

When the port is connected, the output driver circuit will be turned on and the data in the output register will be placed into the output port.

When the I/O is in the input state (TRISx=1), read PORTx, and the content of PORTx will reflect the status of the input port (also

Can be set to read output latch via programming options). When writing on PORTx, data is written to the output register. all

The write operations are all a micro-process of "read-change-write", that is, the process of data being read, then changed, and then written to the output data register.

When MCLRE is 1, the value read by PORTB[7] is 0, and it is used as an external reset pin at this time.

14.2. Other functions of the port

Each port of PORTA has a status change interrupt option and a weak pull-up option.

14.2.1. Weak pull-up

Each port of PORTA/B/C has an internal weak pull-up function that can be individually set. These weak pull-up circuits can be enabled or disabled by controlling bits in the WPUX register. When GPIO is set as output, these weak pull-up circuits will be automatically turned off. The weak pull-up circuit can be set off during power-on reset. This is determined by the /PAPU bit in the OPTION register. PORTB[7] also has a weak pull-up function internally, which is automatically enabled when PORTB[7] is set to the MCLRB function. When PORTB[7] is set to GPIO, this weak pull-up circuit is controlled by WPUB7.

14.2.2. Weak pull-down

All pins of PORTA/B/C have internal weak pull-down function when used as digital input pins, controlled by register WPDx.

When the weak pull-up and weak pull-down functions are non-mutually exclusive, that is, they can be turned on at the same time.

14.2.3. ANSEL register

The ANSEL register is used to control the digital-analog input of IO. When ANSEL.x is 1, the corresponding IO port is an analog pin. The input pull-up and pull-down of IO are automatically disabled, and the software returns 0 when reading the IO.

The ANSEL bit has no effect on the digital output driver. In other words, the TRIS bit has a higher priority, that is, when TRIS.x is 0, regardless of whether ANSEL.x is 0 or 1, the corresponding IO is the digital output IO. To configure a true analog pin, TRIS.x should be set to 1 to turn off the digital output driver.

14.3. Source current selection

I/O PC0-1 PB2-5 supports different source current drive capabilities. By configuring the corresponding selection register PSRCx, the specified I/O port can support 3 levels of source current drive capabilities. The source current selection bit is only valid when the corresponding pin is set as an output. Otherwise, these selection bits have no effect. Users can refer to the I/O Electrical Characteristics chapter to select the required source current for different applications.

14.4. Sink current selection

I/O PC0-1 PB2-5 supports 2 different sink current drive capabilities. The setting register is PSINKx. When the I/O is set to an output pin, its sink current setting bit is only valid.

14.5. Open drain function

Each I/O supports the IO open-drain function. The setting register is ODCON A/B/C. When the relevant bit is 1, the pin corresponding to the bit is configured.

Set to open drain.

14.6. Summary of registers related to GPIO

name	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	reset value
WPUA	0x95									1111 1111
WPUB	0x100									0000 0000
WPUC	0x93									yyyy yy00
TRISA	0x85									1111 1111
BRINGS	0x05									xxxx xxxx
TRISB	0x86									1111 1111
PORTB	0x06									xxxx xxxx
TRISC	0x87									yy11
PORTC	0x07									yyxx
JOKE	0x96									0000 0000
WPDA	0x89									0000 0000
WPDB	0x10E									0000 0000
WPDC	0x8D									yy00
OPTION	0x81	/PAPU	INTEDG	T0CS T0SE		PSA	PS2	PS1	PS0	1111 1111
PSRCB	0x10C									1111 1111
PSRCC	0x94									yy11
PSINKB	0x10F									0000 0000
PSINKC	0x9F									yy00
EDITION	0x105									0000 0000
ODCONB	0x106									0000 0000
ODCONC	0x107									yy00
ANSEL0	0x11E					ANSEL0[7:0]				0000 0000

14.6.1. WPUA, address 0x95

Bit	7	6	5	4	3	2	1	0
Name								
Reset	1	1	1	1	1	1	1	1
Type	RW							

Bit	Name	Function
7:0	WPUA	PORATA weak pull-up control register 1 = Enable weak pull-up 0 = disable weak pull-up

14.6.2. WPUB, address 0x10D

Bit	7	6	5	4	3	2	1	0
Name	WPUB[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	WPUB	PORTB weak pull-up control register 1 = Enable weak pull-up 0 = disable weak pull-up

14.6.3. WPUC, address 0x93

Bit	7	6	5	4	3	2	1	0
Name	WPUC[1:0]							
Reset	-	-	-	-	-	-	0	0
Type	RO.0	RO.0	RO.0	RO.0	RO.0	RO.0	RW	RW

Bit	Name	Function
7:2	N/A reserved bit, read 0	
1:0	WPUC	PORTC weak pull-up control register 1 = Enable weak pull-up 0 = disable weak pull-up

14.6.4. TRISA, address 0x85

Bit	7	6	5	4	3	2	1	0
Name	TRISA[7:0]							
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	TRISA	PORTA direction control register 1 = input 0 = output

14.6.5. TRISB, address 0x86

Bit	7	6	5	4	3	2	1	0
Name	TRISB[7:0]							
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	TRISB	PORTB direction control register 1 = input 0 = output

14.6.6. TRISC, address 0x87

Bit	7	6	5	4	3	2	1	0
Name	TRISC[1:0]							
Reset	—	—	—	—	—	—	1	1
Type	RO.0	RO.0	RO.0	RO.0	RO.0	RO.0	RW	RW

Bit	Name	Function
7:2	N/A reserved bit, read 0	
1:0	TRISC	PORTC direction control register 1 = input 0 = output

14.6.7. PORTA, address 0x05

Bit	7	6	5	4	3	2	1	0
Name	PORT[7:0]							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	BRINGS	PORTA data register

14.6.8. PORTB, address 0x06

Bit	7	6	5	4	3	2	1	0
Name	PORTB[7:0]							
Reset	x	x	x	x	x	x	x	x
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	PORTB	PORTB data register

14.6.9. PORTC, address 0x7

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PORTC[1:0]	
Reset	-	-	-	-	-	-	x	x
Type	RO.0	RO.0	RO.0	RO.0	RO.0	RO.0	RW	RW

Bit	Name	Function
7:2	N/A	Reserved bit, read 0
1:0	PORTC	PORTC data register

14.6.10. WPDA, address 0x89

Bit	7	6	5	4	3	2	1	0
Name	WPDA[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	WPDA	PORTA weak pull-down control register 1 = Enable weak pull-down 0 = disable weak pulldown



14.6.11. WPDB, address 0x10E

Bit	7	6	5	4	3	2	1	0
Name	WPDB[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	WPDB	PORPB weak pull-down control register 1 = Enable weak pull-down 0 = disable weak pulldown

14.6.12. WPDC, address 0x8D

Bit	7	6	5	4	3	2	1	0
Name	WPDC[1:0]							
Reset	-	-	-	-	-	-	0	0
Type	RO.0	RO.0	RO.0	RO.0	RO.0	RO.0	RW	RW

Bit	Name	Function
7:2	N/A reserved bit, read 0	
1:0	WPDC	PORTC weak pull-down control register 1 = Enable weak pull-down 0 = disable weak pulldown

14.6.13. PSRCB1, address 0x88

Bit	7	6	5	4	3	2	1	0
Name	PSRCB1[7:0]							
Reset	1	1	1	1	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW

PSRCB1 value/[2n+1:2n]	Source current capability
00	L0: 3mA
01/10	L1: 6mA
11	L3: 24mA

Bit	Name	Function
7:6	PSRCB1[7:6] PB5 source current setting bits	
5:4	PSRCB1[5:4] PB4 source current setting bits	
3:2	PSRCB1[3:2] PB3 source current setting bits	
1:0	PSRCB1[1:0] PB2 source current setting bits	

14.6.14. PSRCB2, address 0x10C

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PSRCB2[3:0]			
Reset	-	-	-	-	1	1	1	1
Type	RO.0	RO.0	RO.0	RO.0	RW	RW	RW	RW

PSRCB2 value/[2n+1:2n]	Source current capability
00	L0: 3mA
01/10	L1: 6mA
11	L3: 24mA

Bit	Name	Function
7:4	N/A	Reserved bit, read 0
3:2	PSRCB2[3:2] PB7 source	current setting bits
1:0	PSRCB2[1:0] Source current setting bits of PB6	

14.6.15. PSRCC, address 0x94

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	PSRCC[3:0]			
Reset	-	-	-	-	1	1	1	1
Type	RO.0	RO.0	RO.0	RO.0	RW	RW	RW	RW

PSRCC value/[2n+1:2n]	Source current capability
00	L0: 3mA
01/10	L1: 6mA
11	L3: 24mA

Bit	Name	Function
7:4	N/A	Reserved bit, read 0
3:2	PSRCC[3:2] PC1 source	current setting bits
1:0	PSRCC[1:0] PC0 source	current setting bits

14.6.16. PSINKB, address 0x10F

Bit	7	6	5	4	3	2	1	0
Name	PSINKB[7:2]						-	-
Reset	0	0	0	0	0	0	-	-
Type	RW	RW	RW	RW	RW	RW	RO.0	RW

Bit	Name	Function
7:2	PSINKB	Current sink capability setting of PORTB[7:2] 0: L0, 35mA 1: L2, 55mA
1:0	N/A reserved bit, read 0	

14.6.17. PSINKC, address 0x9F

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PSINKC[1:0]	
Reset	-	-	-	-	-	-	0	0
Type	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RW	RW

Bit	Name	Function
7:2	N/A reserved bit, read 0	
1:0	PSINKC	Current sink capability setting of PORTC[1:0] 0: L0, 35mA 1: L2, 55mA

14.6.18. ODCONA, address 0x105

Bit	7	6	5	4	3	2	1	0
Name	ODCON[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	DISCONNECTED	PORTE open drain output control 1 = Open-drain functionality enabled 0 = Turn off open drain function

14.6.19. ODCONB, address 0x106

Bit	7	6	5	4	3	2	1	0
Name	ODCONB[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	ODCONB	PORTB open drain output control 1 = Open-drain functionality enabled 0 = Turn off open drain function

14.6.20. ODCONC, address 0x107

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	ODCONC[1:0]	
Reset	—	—	—	—	—	—	0	0
Type	RO-0	RO-0	RO-0	RO-0	RO-0	RO-0	RW	RW

Bit	Name	Function
7:2	N/A reserved bit, read 0	
1:0	ODCONC	PORTC open drain output control 1 = Open-drain functionality enabled 0 = Turn off open drain function

14.6.21. ANSEL0, address 0x11E

Bit	7	6	5	4	3	2	1	0
Name	ANSEL0[7:0]							
Reset	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:0	ANSEL0	Analog selection bit Select analog or digital functions separately on AN<7:0> pins 1 = Analog input, pin is assigned as analog input 0 = Digital IO, pin assigned to port or special function

15. Slow clock measurement

The chip integrates two internal RC oscillators, one is a factory-calibrated high-speed and high-precision 16M fast clock HIRC, and the other is a low-speed

The low-power 32k clock LIRC uses the slow clock measurement function to calculate the LIRC period using the system clock.

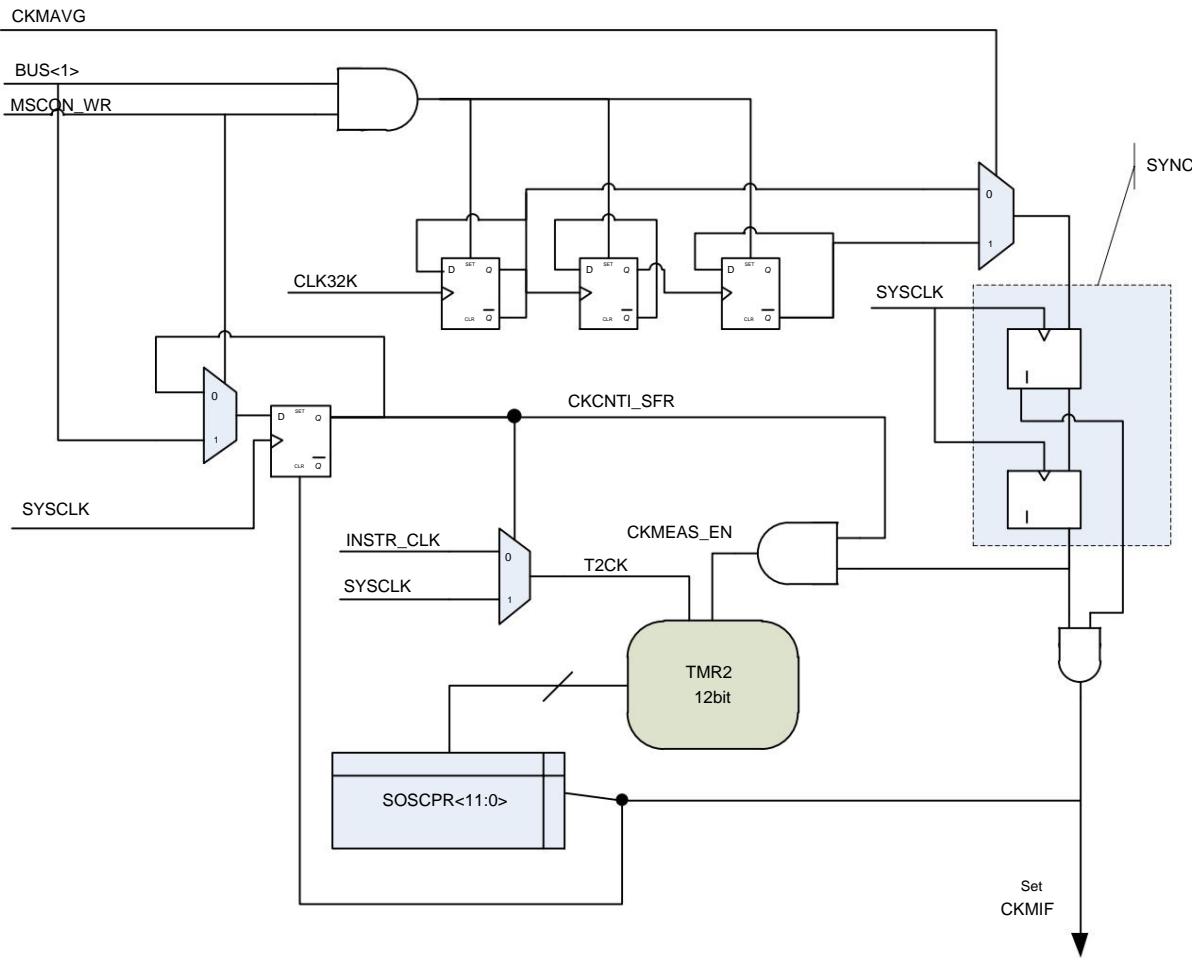


Figure 15.1 Slow clock measurement structure block diagram

15.1.Measurement principle

In the slow clock measurement mode, the prescaler and postscaler configuration of Timer2 automatically changes to 1:1, and the counting clock of Timer2 is the system clock FSYS.

Instead of the instruction clock FSYS/2 in normal mode . After the measurement is completed, the result is automatically stored in the SOSCPR register, and its unit is the system clock number.

15.2. Operation steps

1. To improve measurement accuracy, it is recommended to set IRCF to 111, SCS=1, and select a 16M system clock;
2. Set T2CON0.2 to 1 to enable Timer2;
3. If 4 times average is selected, set MSCON0.2 to 1, otherwise clear it to 0;
4. Set MSCON0.1 to start measurement;
5. After the measurement, MSCON0.1 is automatically cleared to 0 and the interrupt flag is set to 1;
6. You can wait for the end by querying or interrupting;
7. When the interrupt flag is found to be 1, the SOSCPR read is the final result.

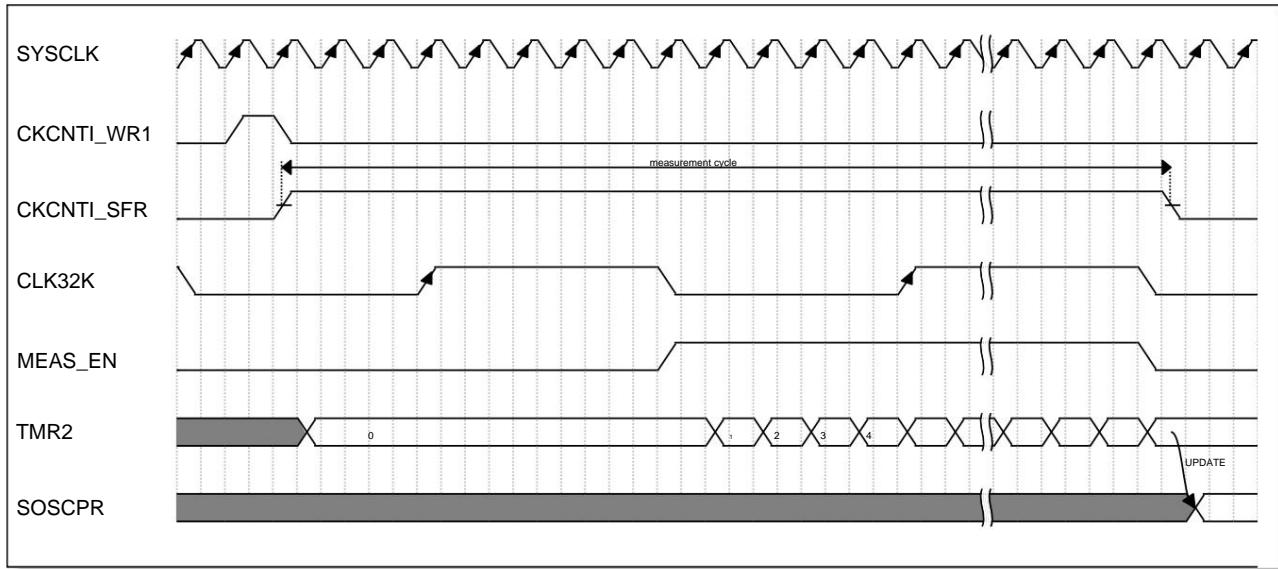


Figure 15.2 Single measurement timing diagram (CLK32K and SYSCLK are not drawn to real scale)

Notice:

1. Do not write **SOSCPRH/L** in the software during slow clock measurement ;
2. Do not perform slow clock measurements in single-step debugging, because **Timer2** is stopped in pause mode, which will cause incorrect measurement results;

15.3. Summary of registers related to slow clock measurement

Name	address	bit7		bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset value	
MSCON0	0x1B	BGRBOE	LVROE	ROMLPE	CLKOS	SLVREN	CKMAVG	CKCNTI	T2CKRUN		0001 0000	
SOSCPRL	0x1C	SOSCPR[7:0]										
SOSCPRH	0x1D						SOSCPR[11:8]					
INTCON	0x0B		GIE	LIKE THIS	T0IE	NOT	PAY	T0IF	INTF	PAIF	0000 0000	
PIE1	0x8C	THIS	CKMIE	LVD	ACMPIE	TMR1IE		OSFIE	TMR2IE	ADCIE	0000 0000	
PIR1	0x0C	EEIF	CKMIF	LVDIF	ACMPIF	TMR1IF		OSFIF	TMR2IF	ADCIF	0000 0000	

15.3.1. MSCON0 register, address 0x1B

Bit	7	6	5	4	3	2	1	0
Name	-	-	ROMLPE	CLKOS	SLVREN	CKMAVG	CKCNTI T2CKRUN	
Reset	-	-	0	1	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	Function
7:6	Reserved reserved bit, please do not write 1	
5	ROMLPE	<p>PROM low power mode selection 0 = normal power mode 1 = Enable low power mode</p> <p>Note: It can only be turned on if the PROM reading speed is below 250kHz , that is: in 2T mode, the system clock must be less than 500kHz; In 4T mode, the system clock must be less than 1MHz</p>
4	CLKOS	<p>CLKO signal mapping pin control 1 = CLKO function is mapped to PB0 0 = CLKO function mapped to PA2</p>
3	SLVREN	<p>Software controls the LVR enable bit, when UCFG1<1:0> is 01: 1 = Turn on LVR 0 = disable LVR</p> <p>When UCFG1<1:0> is not 01, this bit has no practical meaning.</p> <p>Note: This bit will not be cleared to 0 when a brown-out reset occurs . Any other reset clears it to 0</p>
2	CKMAVG	<p>Fast Clock Measurement Averaging Mode for Slow Clock Periods 1 = Turn on average mode (automatically measure and accumulate 4 times) 0 = turns off averaging mode</p>
1	CKCNTI	<p>Clock Count Init – enables fast clock measurement of slow clock periods 1 = Enables fast clock to measure slow clock periods 0 = Turn off fast clock to measure slow clock period</p> <p>Note: This bit will automatically return to zero after the measurement is completed.</p>
0	T2CKRUN	<p>When the T2 clock is not the selected instruction clock, the operation control bit of the sleep state T2CK 1 = T2CK keeps working while sleeping 0 = T2CK stops working while sleeping</p>

15.3.2. SOSCPR register, address **0x1C, 1D**

SOSCPRL, address 0x1C

Bit	7	6	5	4	3	2	1	0
Name	SOSCPR[7:0]							
Reset	0xFF							
Type	RW							

SOSCPRH, address 0x1D

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	SOSCPR[11:8]			
Reset	-	-	-	-	0xF			
Type	RO-0	RO-0	RO-0	RO-0	RW			

Bit	Name	Function
0x1D:3:0 0x1C:7:0	SOSCPR[11:0]	Low speed oscillator period (unit: number of fast clock cycles) For slow clock measurement function

16. Summary of instruction set

This chip uses a reduced instruction architecture with a total of 37 instructions. The following is a description of each instruction.

Assembly syntax	Function	Operation	status bit
BCR R, b	Clear the b bit of register R to 0.	0-> R(b)	
BSR R, b	Set the b position of register R to	1-> R(b)	
BTSC R, b	1 to test the bit. If it is 0, skip the	Skip if R(b)=0	
BTSS R, b	bit test. If it is 1, skip the no-	Skip if R(b)=1	
NOP	operation	None	
CLRWDT	and clear the watchdog	0-> WDT	/PF, /TF
SLEEP	(feed the dog). Enter	0-> WDT, STOP OSC	/PF, /TF
STTMD	sleep mode and save the W	W->TMODE1	
CTLIO R	content. Go to TMODE, set	W->TRISr	
STR R(MOVWF)	TRISr register,	W-> R	
LDR R, d(MOVF)	store W to R, store R to d.	R-> d	WITH
SWAPR R,d	R nibble swap	[R(0-3)R(4-7)]-> d	
INCR R, d	R+1	R+ 1-> d	WITH
INCRSZ R, d	R+1, skip if the result is 0	R+ 1-> d	
ADDRESS R, d	Add W and R	W+ R-> d	C, HC, Z
SUBWR R, d	R minus W	R- W-> d	C, HC, Z
		R+ /W+ 1-> d	
DEC R, d	R-1	R- 1-> d	WITH
DECRSZ R, d	R-1, skip if the result is 0	R- 1-> d	
ANDWR R, d	AND of W and R	R& W-> d	WITH
IORWR R, d	W is ORed with R	W R-> d	WITH
XORWR R, d	Exclusive OR of W and R	W^ R-> d	WITH
COMR R, d	to find the complement of R	/R-> d	WITH
RRR R, d	R rotate right with carry	R(n)-> R(n-1), C-> R(7), R(0)-> C	C
		R(n)-> R(n+1), C-> R(0), R(7)-> C	
RLR R, d	R rotate left with carry	R(n)-> R(n+1), C-> R(0), R(7)-> C	C
		R(n)-> R(n+1), C-> R(0), R(7)-> C	
CLRW	Clear W to 0.	0->W	WITH
CLRR R	Clear R to 0.	0-> R	WITH
RARELY	Return from	Stack-> PC,1-> GIE	
RIGHT	interrupt and return from subroutine.	Stack-> PC	
LCALL N	call subroutine	N-> PC, PC+1-> Stack	
		N-> PC	
LJUMP N	Unconditionally jumps to	N-> PC	
LDWI I(MOVLW)	immediate data and saves it to W	I->W	
WINDOW I	AND of W and immediate value I	W& I-> W	WITH
IORWI I	W is ORed with the immediate value I	W I-> W	WITH
XORWI I	W and immediate value I are XORed	W^ I-> W	WITH
RETW I	and returned with immediate value	Stack-> PC, I-> W	
ADDWI I	Add W to an immediate number and subtract	W+I-> W	C, HC, Z
SUBWI I	W from the immediate number.	IW->W	C, HC, Z

Opcode field description

Field	describe
R(F)	SFR address
IN	working register
b	register bit address
I/Imm(k)	immediate number
X	Don't care about the value, which can be 0 or 1
d	Target register selection
	0: The result is stored in W
	1: The result is stored in SFR
N	program absolute address
PC	program counter
TMODE	TMODE1 register
TRISr	TRISr register, r can be A, B, C
C	carry
HC	half carry
WTFH	0 flag
/PF	Power down flag
/TF	WDT overflow flag

Notice:

1. In the **FT62F13x** series chips, the TMODE register refers to **OPTION**, that is, the operation of the **STTMD** instruction is to store **W** in **OPTIONy**

17. Electrical characteristics of the chip

17.1. Limit parameters

Operating temperature.....	- 40 ~ + 85 °C
Storage temperature.....	- 40 ~ + 125 °C
Power supply voltage.....	V SS - 0.3 V ~ VS S + 6.0 V
Port input voltage.....	V SS - 0.3V ~ V DD + 0.3 V

Note: The above values are the limit parameter values of the chip working conditions. Exceeding the range specified by the limit parameters may cause permanent damage to the chip. Ruoxin
If the chip operates outside the extreme parameter range for a long time, its reliability may be affected.

17.2. Built-in high-frequency oscillator (HIRC)

Electrical parameter	minimum(1)	Typical value(1)	Maximum value	(1) unit conditions	s/remarks
parameter	15.84	16	16.16	MHz 25°C, VDD = 2.5V	
calibration range changes with temperature	-	±4.0%	-	-40~85°C, VDD = 2.5V	
Variation range with power supply voltage	-1.0%	-	1.0%	-25°C, VDD = 1.9~5.5V	
IIRC operating current	-	40	-	ȳA	25°C, VDD = 3.0V
Start Time	-	2.5	-	ȳs	25°C, VDD = 3.0V

(1) Data based on characteristic values and not production tested.

17.3. Built-in low-frequency oscillator (LIRC)

The low-frequency oscillator has a dual-mode mode, with a vibration frequency of 32kHz in one mode and a vibration frequency of 256kHz in the other mode. Oscillation frequency mode

The mode is controlled by the LFMOD bit in the OSCCON register, 0 is 32kHz mode, 1 is 256kHz mode.

Electrical parameters	minimum(1)	Typical value(1)	Maximum value	(1) unit conditions	s/remarks
Oscillation frequency	30.4	32	33.6	kHz	25°C, VDD = 2.5V
Variation range with temperature	-2.0%	-	2.0%	-40 ~ 85°C, VDD = 2.5V	
Variation range with power supply voltage	-1.0%	-	1.0%	-25°C, VDD = 1.9~5.5V	
ILIRC operating current	-	1.3	-	ȳA	25°C, VDD = 3.0V
Start Time	-	4.6	-	ȳs	25°C, VDD = 3.0V

(1) Data based on characteristic values and not production tested.

17.4. Low voltage reset circuit (LVR)

Electrical parameters	minimum(1)	Typical value(1)	Maximum value	(1) unit conditions	remarks
ILVR operating current	-	16.2	-	µA	25°C, VDD = 3.3V
VLVR, LVR threshold	1.94	2.0	2.06	IN	25°C
	2.13	2.2	2.27		
	2.42	2.5	2.58		
	2.72	2.8	2.88		
	3.01	3.1	3.19		
	3.49	3.6	3.71		
	3.98	4.1	4.22		
LVR delay	-	125	157	µs	25°C, VDD = 1.9~5.5V

(1) Data based on characteristic values and not production tested.

17.5. Low voltage detection circuit (LVD)

Electrical parameters	minimum(1)	Typical value(1)	Maximum value	(1) unit conditions	remarks
ILVD working current	-	21.4	-	µA	25°C, VDD = 3.3V
VLVD, LVD threshold	1.16	1.2	1.24	IN	25°C
	1.94	2.0	2.06		
	2.33	2.4	2.47		
	2.62	2.7	2.78		
	2.91	3.0	3.09		
	3.20	3.3	3.40		
	3.49	3.6	3.71		
	3.88	4.0	4.12		
LVD delay	-	125	157	µs	25°C, VDD = 1.9~5.5V

(1) Data based on characteristic values and not production tested.

17.6. Power-on reset circuit (POR)

Electrical parameters	Minimum value	Typical value (1)	Maximum value	Unit	conditions/remarks
IPOR operating current	-	140	-	nA	25°C VDD = 3.3V
VPOR	-	1.65	-	IN	25°C

(1) Data based on characteristic values and not production tested.

17.7. I/O PAD circuit

Electrical parameters			Minimum value (1)	Typical value (1)	Maximum value (1)	Unit	conditions/remarks
WILL			0	-	0.3* VDD	IN	
HIV			0.7* VDD —		VDD	IN	
Leakage current			-1	-	1	µA	VDD = 5V
Source current (source)	PB2~7 PC0~1	L0	-	-3	-	mA	25°C, VDD = 5V, VOH = 4.5V
	PB2~7 PC0~1	L1	-	-6	-		
	PA2 PB2~7 PC0~1	L2	-	-18	-		
	PA0~1 PA3~7 PB0~1	L3	-	-24	-		
	PB2~7 PC0~1	L0	-	35	-		
	PA2 PB2~7 PC0~1	L1	-	53	-		
sink current(sink)	PA0~1 PA3~7 PB0~1	L2	-	55	-	mA	25°C, VDD = 5V, VOL= 0.5V
	Pull-up resistor		-	20	-		k̄ Enable pull-up individually
	Pull-down resistor		-	20	-		k̄ individually enabled pull-down
Pull-up resistor			-	100	-	k̄ simultaneously enables pull-up and	
Pull-down resistor			-	100	-	k̄ pull down	

(1) Data based on characteristic values and not production tested.

17.8. Overall operating current (IDD)

Electrical parameters	Sysclk	(1) Typical value@VDD			unit
		2.0V	3.0V	5.5V	
Normal mode (2T), IDD	16MHz	—	1.244	1.320	mA
	8MHz	0.588	0.875	0.924	
	4MHz	0.463	0.687	0.706	
	2MHz	0.349	0.403	0.412	
	1MHz	0.220	0.256	0.260	
	32kHz	0.024	0.032	0.033	
Low power mode (2T), IDD	32kHz	0.007	0.008	0.009	
Sleep mode (Sleep, WDT OFF, LVR OFF), ISB	—	0.072	0.092	0.128	µA
Sleep mode (Sleep, WDT ON, LVR OFF)	—	1.077	1.468	1.582	
Sleep mode (Sleep, WDT OFF, LVR ON)	—	11.475	15.520	20.978	
Sleep mode (Sleep, WDT ON, LVR ON)	—	12.402	16.792	22.286	
Sleep mode (Sleep, WDT OFF, LVR OFF, LVD ON) — (1)	Data are	17.425	20.805	25.274	

based on characteristic values and are not production tested.

Note:

1. The test environment temperature is 25°C;
2. The test condition for sleep current is that the I/O is in input mode and externally pulled down to 0;

17.9. AC electrical parameters

Electrical parameters		minimum(1)	Typical value(1)	Maximum value	(1) unit conditions	remarks
Fsys (system clock frequency)	2T/4T	—	—	8	MHz -40~85°C, VDD = 1.9~5.5V	
		—	—	16	MHz -40~85°C, VDD = 2.7~5.5V	
Instruction cycles (Tins)	2T	—	125	—	ns	System clock HIRC
	4T	—	250	—	ns	
	2T	—	61	—	µs	System clock LIRC
	4T	—	122	—	µs	
T0CKI input cycle		(Tt0ck+40)/ N and 20 <small>Whichever is larger</small>	—	—	ns	N = prescaler value 2, 4, ..., 256
Power-on reset hold time (TDRH)		—	4.2	—	ms	25°C, PWRT disable
External reset pulse width (TMCLRB)		2000	—	—	ns	25°C
WDT period (TWDT)		—	—	—	ms without prescaler, WDTPS<3:0>=0000	

(1) Data based on characteristic values and not production tested.

Note 1: Tt0ck refers to the clock period selected by T0CKSRC.

Note 2: Unless otherwise specified, the characteristic test conditions are: T=25°C, VDD =1.9~5.5V.



17.10. 12bit ADC characteristics

ADC characteristic parameters

Electrical parameters	minimum(1)	Typical value(1)	Maximum value (1)	unit conditions/remarks
ADC operating voltage VDD	2.7	-	5.5	IN
ADC operating current IVDD	-	85	-	ÿA 25°C, VREFP = VDD = 2.7V, ADC conversion clock frequency is 250kHz
	-	95	-	ÿA 25°C, VREFP = VDD = 3.0V, ADC conversion clock frequency is 250kHz
	-	125	-	ÿA 25°C, VREFP = VDD = 5.5V, ADC conversion clock frequency is 250kHz
Analog input voltage VAIN	VREFN	-	VREFP	IN
External reference voltage VREF	-	-	VDD	IN
resolution	-	-	12	Bit
Integral error EIL	-	±2	-	LSB 25°C, VREFP = VDD = 5.0V, VREFN= GND, ADC conversion clock
Differential error E ^{DL}	-	±2	-	LSB Frequency is 250kHz
Offset error EOFF	-	±3	-	LSB 25°C, VREFP = VDD = 5.0V VREFN = GND
Gain error EGN	-	±5	-	LSB
Conversion clock period TAD	-	2	-	ÿs VREFP > 3.0V, VDD > 3.0V
Conversion clock	-	15	-	THEN
stabilization time (TST)	-	15	-	ÿs
Sampling time (TACQ)	-	1.5	-	THEN
Recommended analog voltage source impedance	-	-	10	kÿ —

(ZAI) (1) Data based on characterization values and not production tested.

ADC Vref characteristic parameters

Electrical parameters	minimum(1)	Typical value(1)	Maximum value (1)	unit conditions/remarks
Built-in reference voltage ADCVref	0.492	0.5	0.508	IN 25°C, VDD =5V
	1.992	2	2.008	IN 25°C, VDD =5V
	2.988	3	3.012	IN 25°C, VDD =5V
Built-in reference voltage 0.5V	-	400	-	ÿs 25°C, VDD =5V
	-	600	-	ÿs 25°C, VDD =5V, 1ÿF
Built-in reference voltage 2.0V	-	450	-	ÿs 25°C, VDD =5V
	-	800	-	ÿs 25°C, VDD =5V, 1ÿF
Built-in reference voltage 3.0V	-	450	-	ÿs 25°C, VDD =5V
	-	1200	-	ÿs 25°C, VDD =5V, 1ÿF

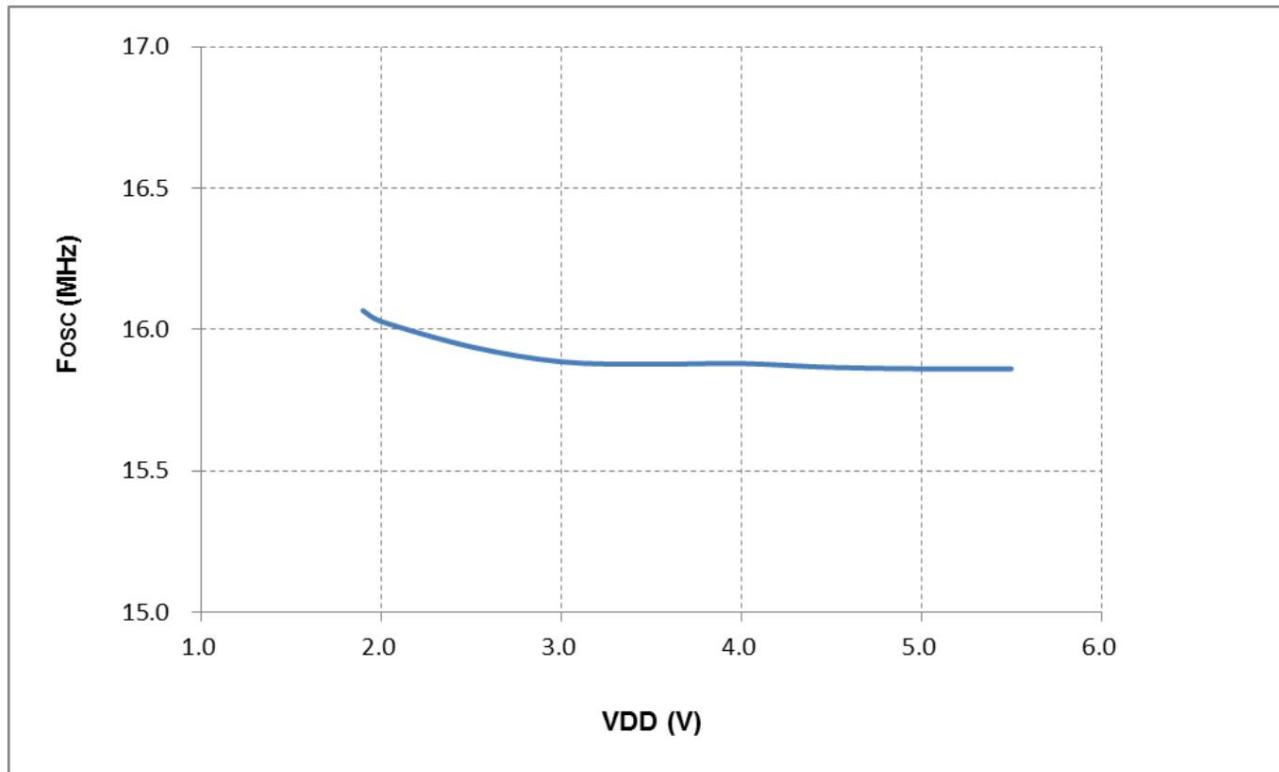
(1) Data based on characteristic values and not production tested.

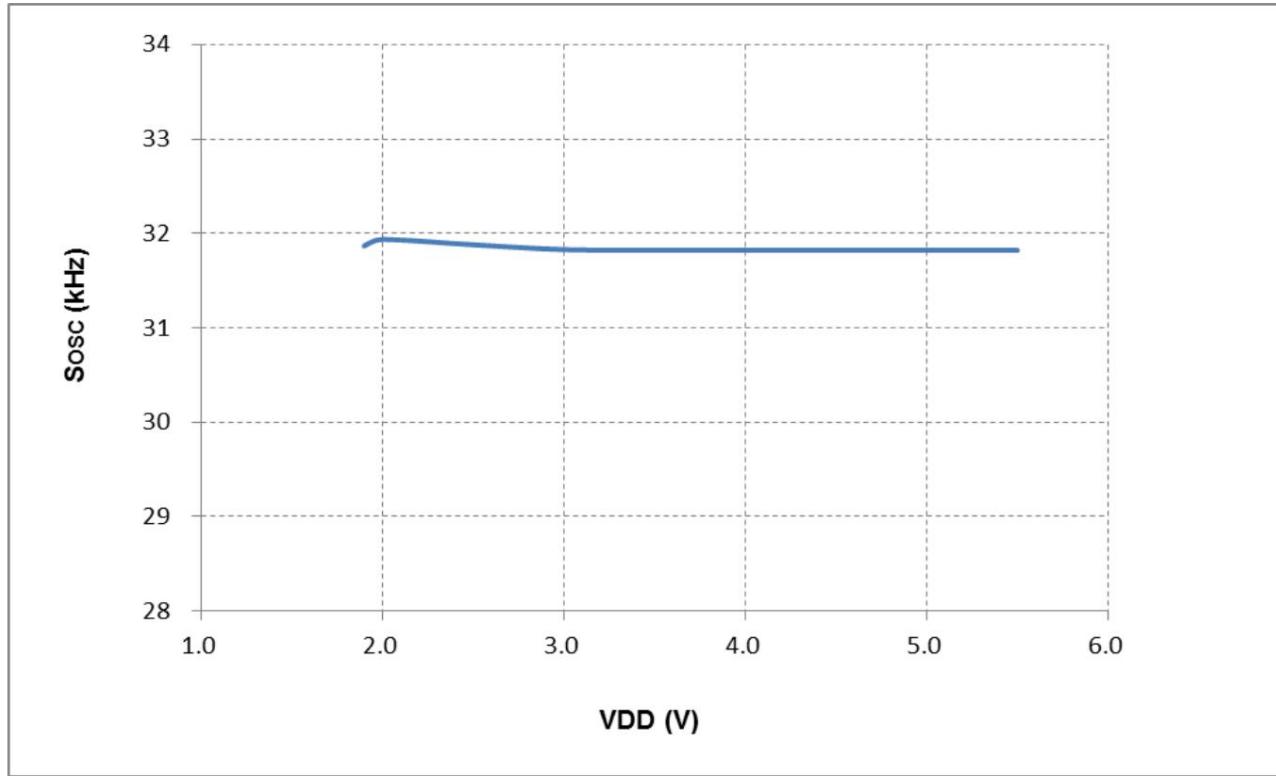
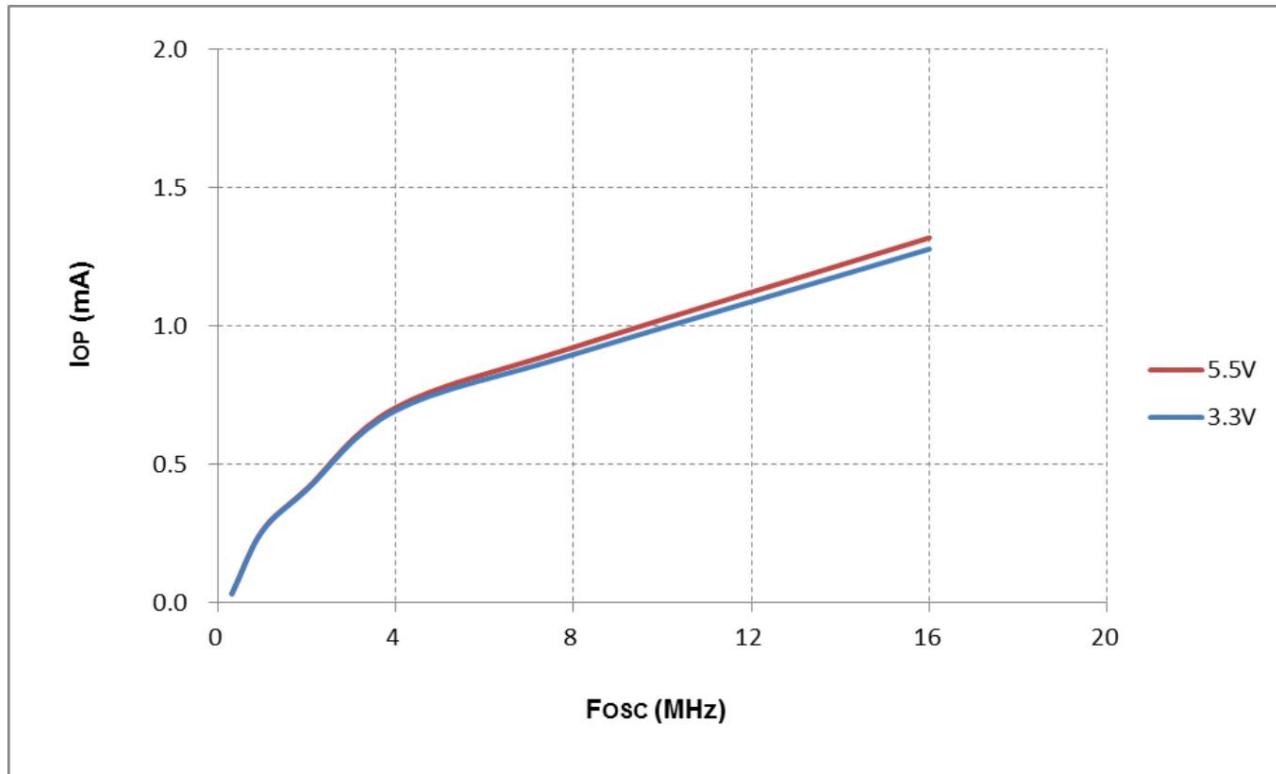
Note: Unless otherwise stated, the data in the "Typical Value" column are given under the conditions of 5.0V and 25°C.

17.11. DC and AC characteristic curves

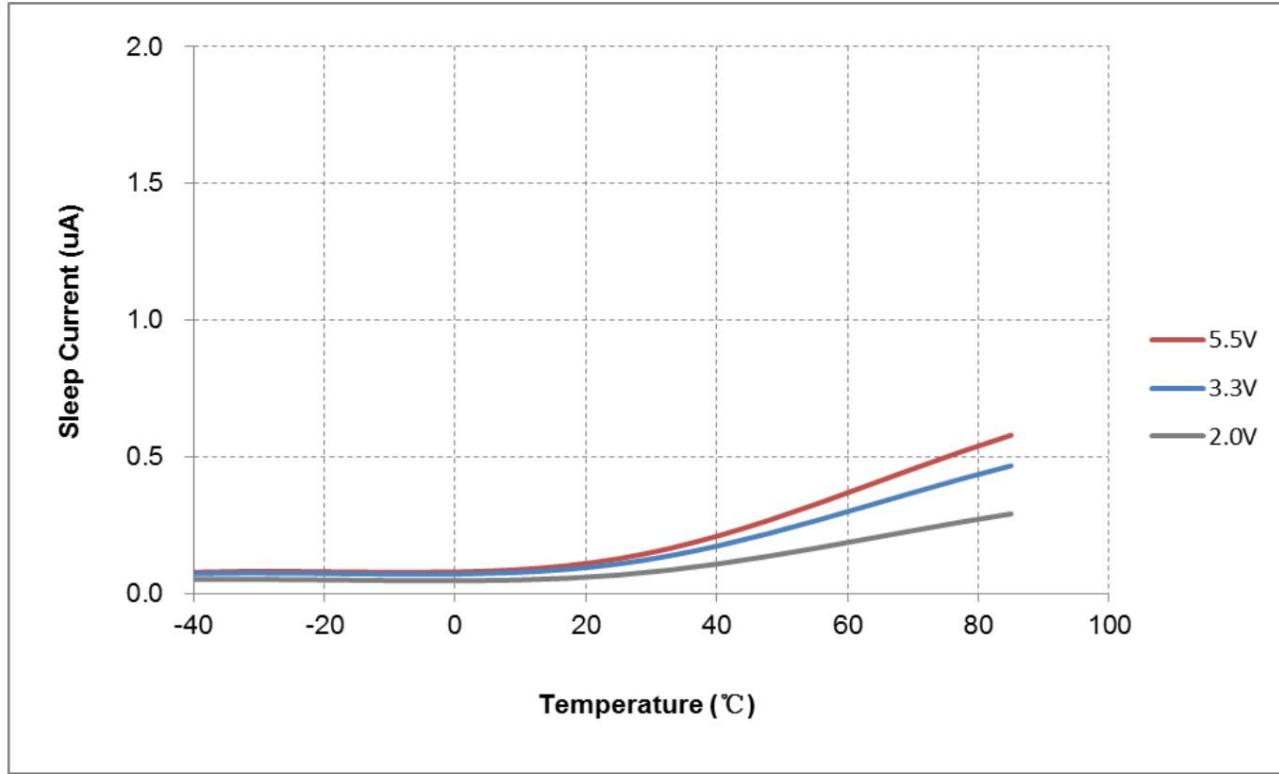
NOTE: The charts provided in this section are based on characteristic values and are for design reference only and have not been production tested.

17.11.1. HIRC vs VDD (TA=25°C)

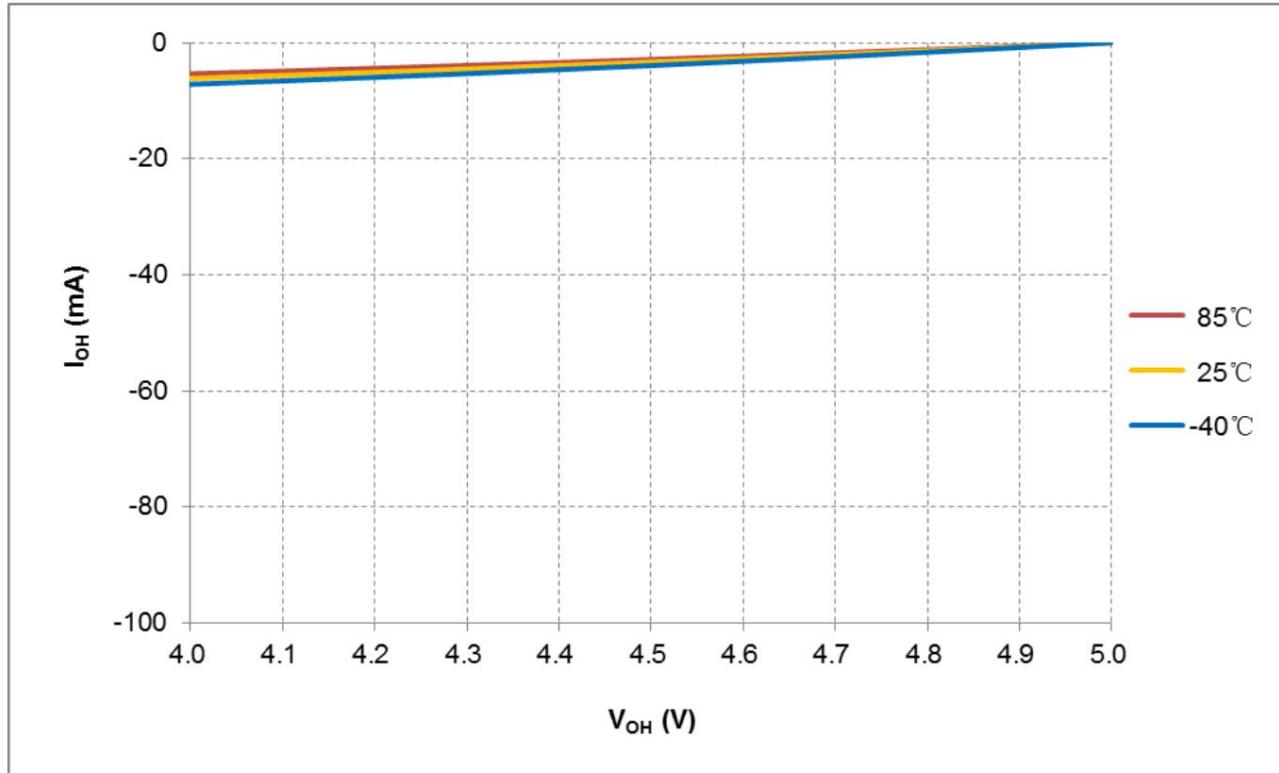


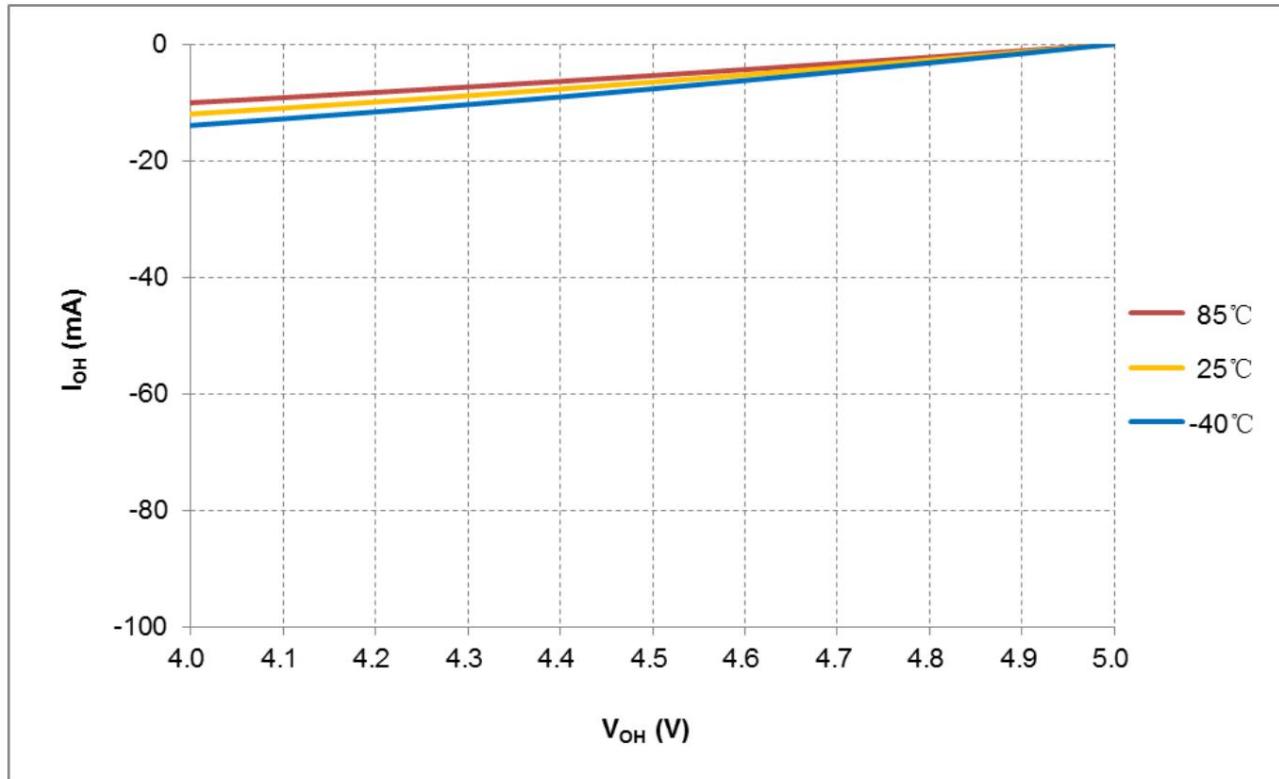
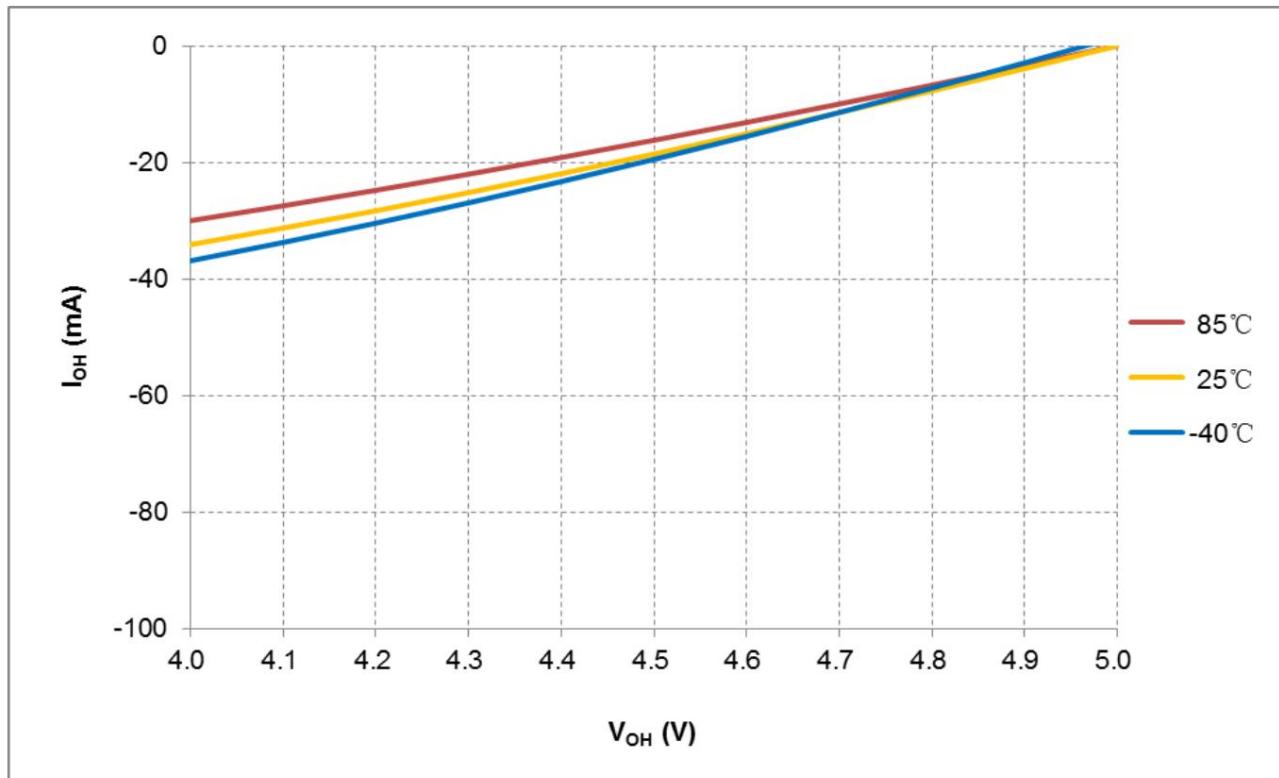
17.11.2. LIRC vs VDD (TA=25°C)**17.11.3. IDD vs Freq (2T, TA=25°C) under different VDD**

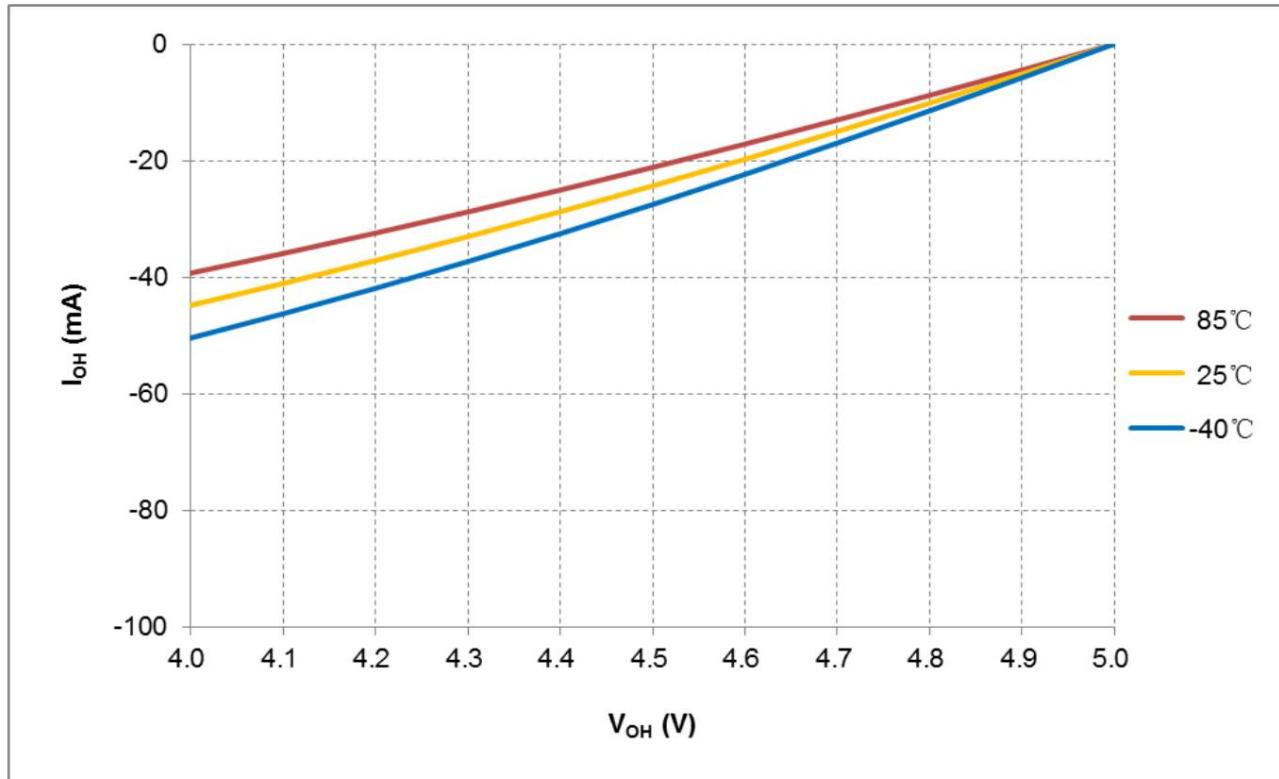
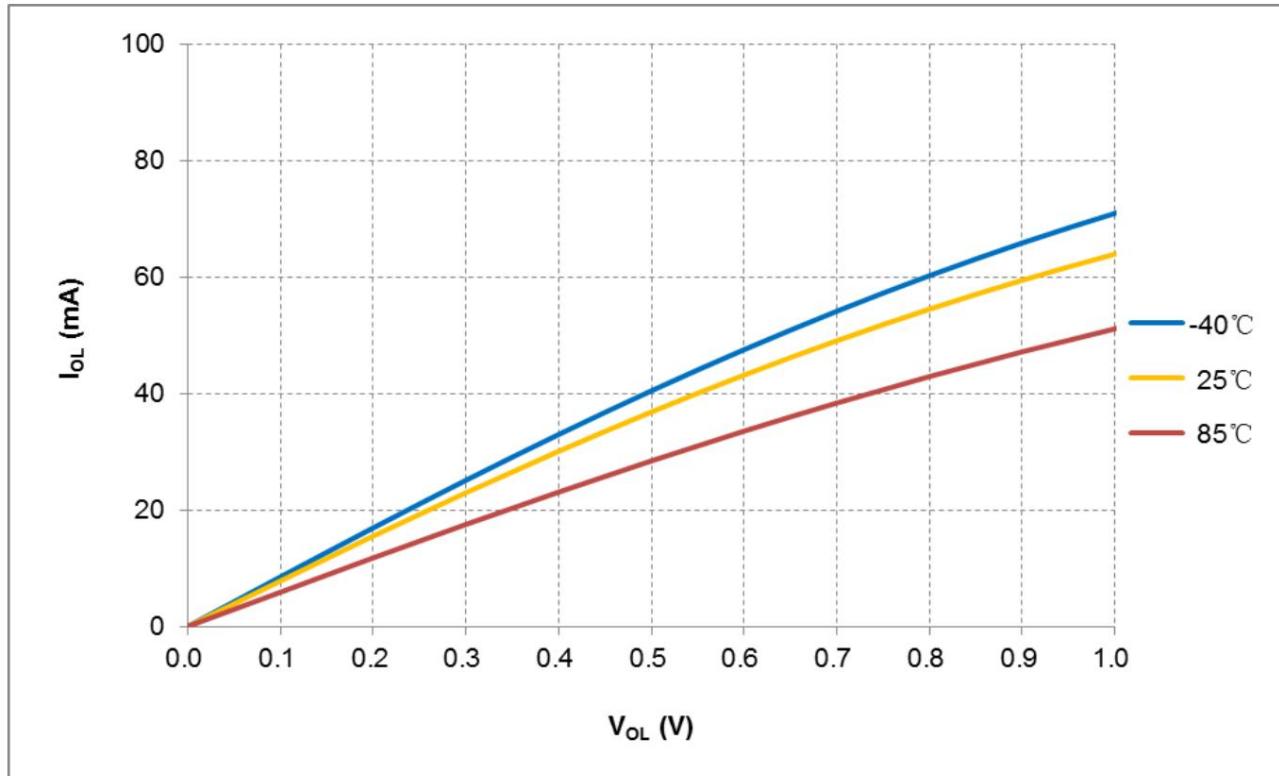
17.11.4. ISB (sleep current) changes curve with temperature under different VDD

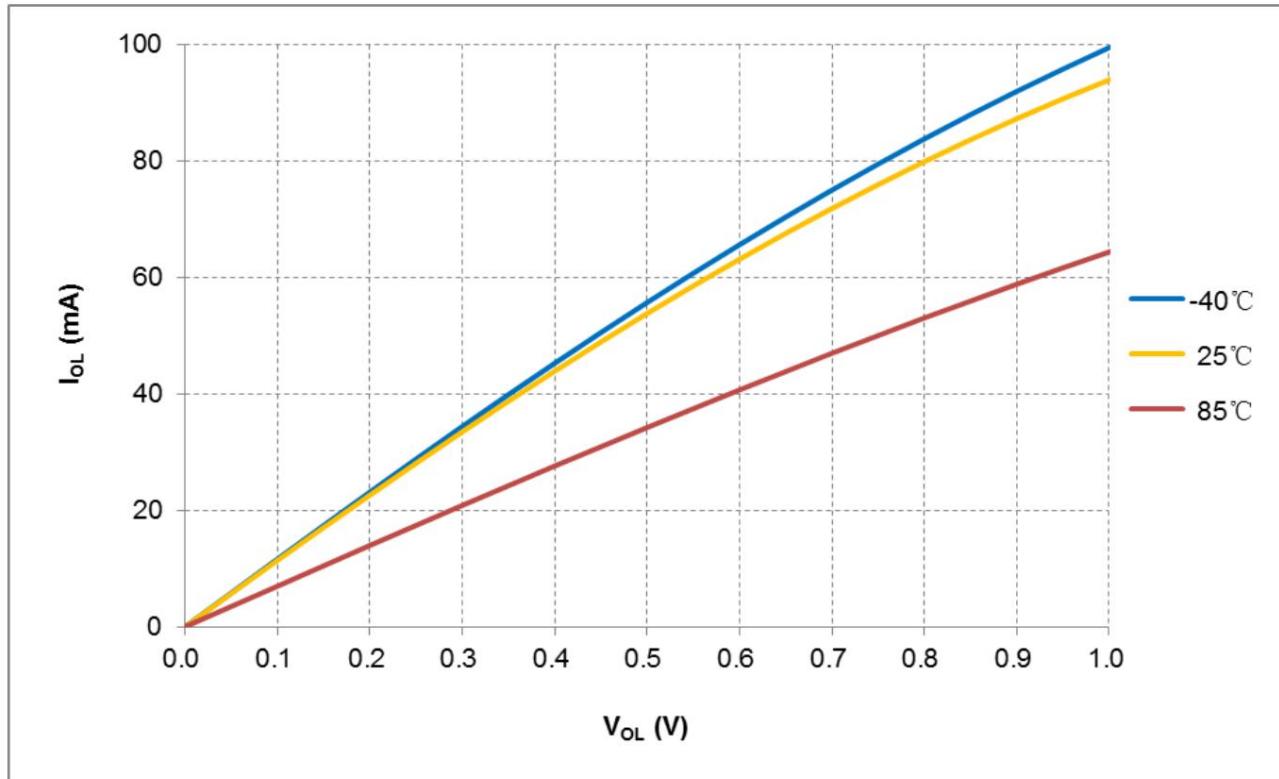
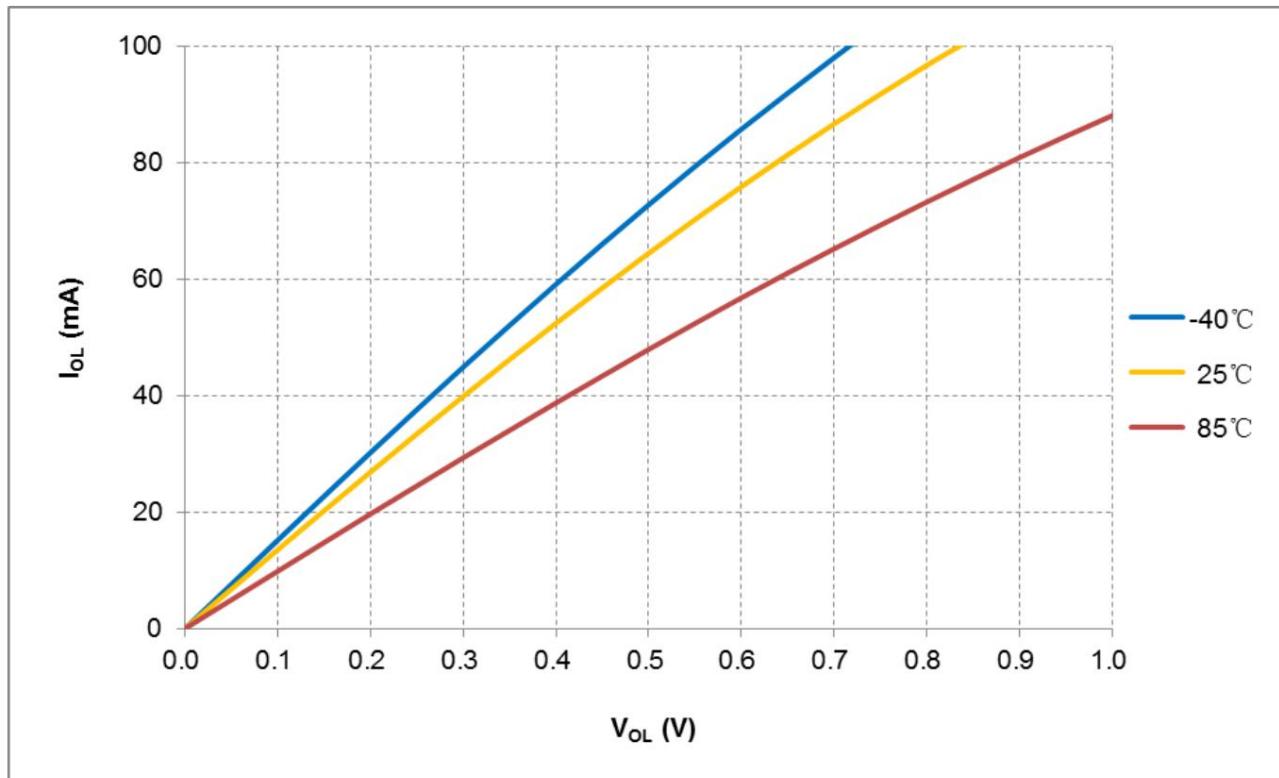


17.11.5. IOH (L0 -3mA) vs VOH @VDD=5V at different temperatures



17.11.6.IOH (L1 -6mA) vs VOH @VDD=5V at different temperatures**17.11.7.IOH (L2 -18mA) vs VOH @VDD=5V at different temperatures**

17.11.8.IOH (L3 -24mA) vs VOH @VDD=5V at different temperatures**17.11.9.IOL (L0 35mA) vs VOL @VDD=5V at different temperatures**

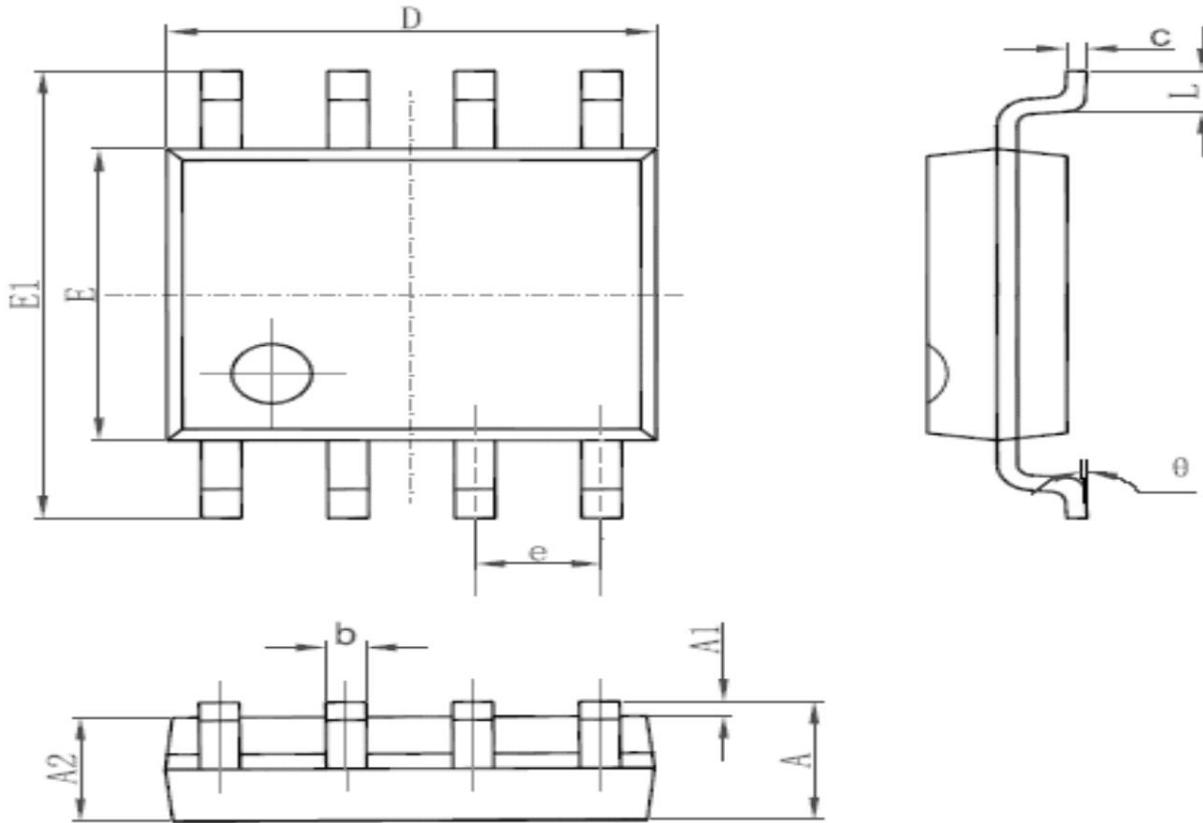
17.11.10.IOL (L1 53mA) vs VOL @VDD=5V at different temperatures**17.11.11.IOL (L2 55mA) vs VOL @VDD=5V at different temperatures**

18. Chip packaging information

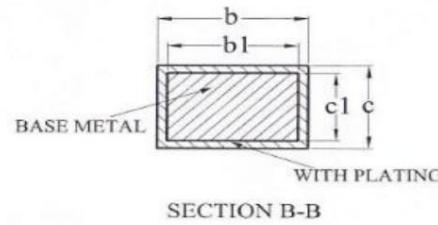
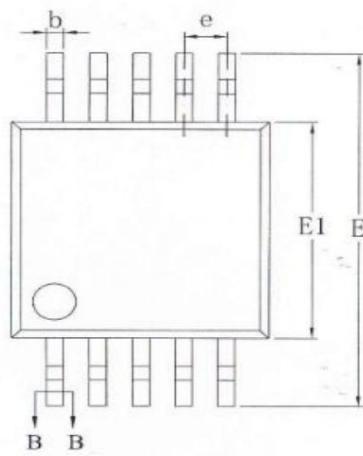
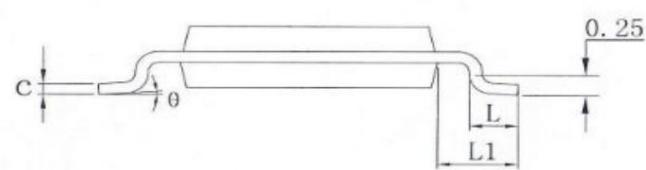
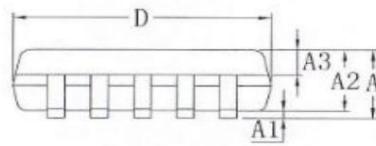
This chip is packaged in SOP8, MSOP10, SOP14, SOP16, SOP20, TSSOP20 and DIP20. The specific package size information

The information is as follows.

SOP8

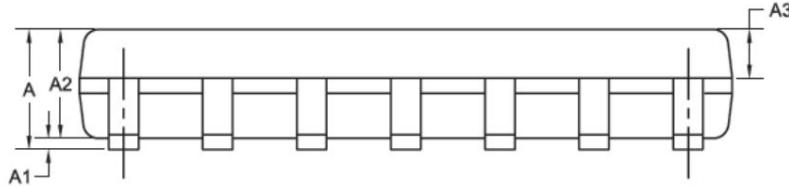
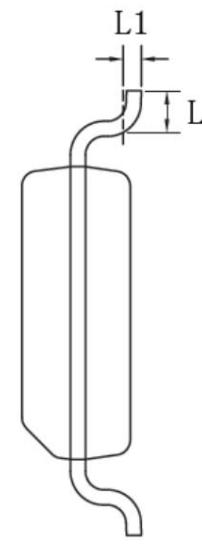
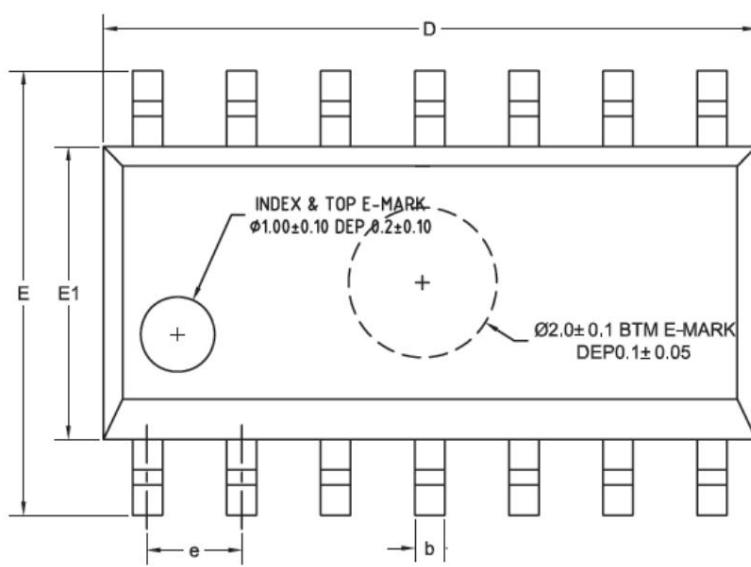


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E1	5.800	6.200	0.228	0.244
It is	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
i	0°	8°	0°	8°

MSOP10^y

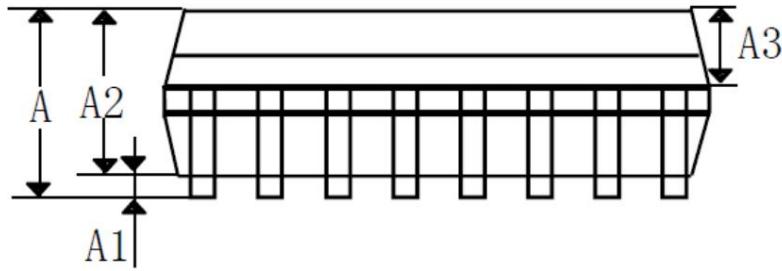
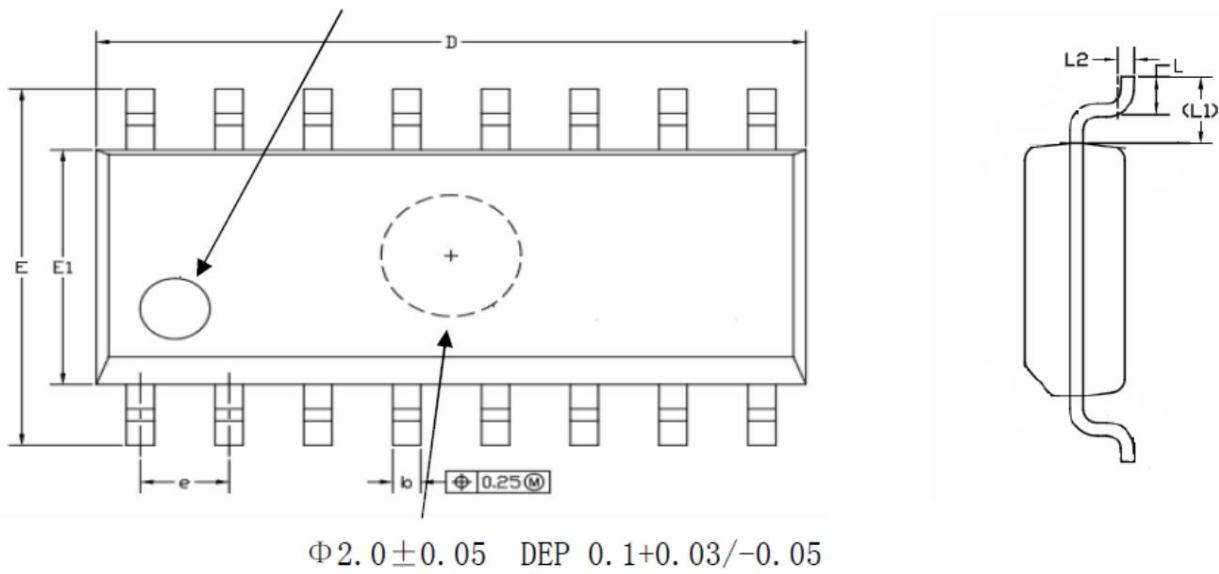
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
A3	0.300	0.400	0.012	0.016
b	0.180	0.260	0.007	0.010
b1	0.170	0.230	0.007	0.009
c	0.150	0.190	0.006	0.007
c1	0.140	0.160	0.006	0.006
D	2.900	3.100	0.114	0.122
AND	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
It is	0.500(BSC)		0.020(BSC)	
L	0.400	0.700	0.016	0.028
L1	0.950(REF)		0.037(REF)	
i	0	8°	0	8°

SOP14ÿ



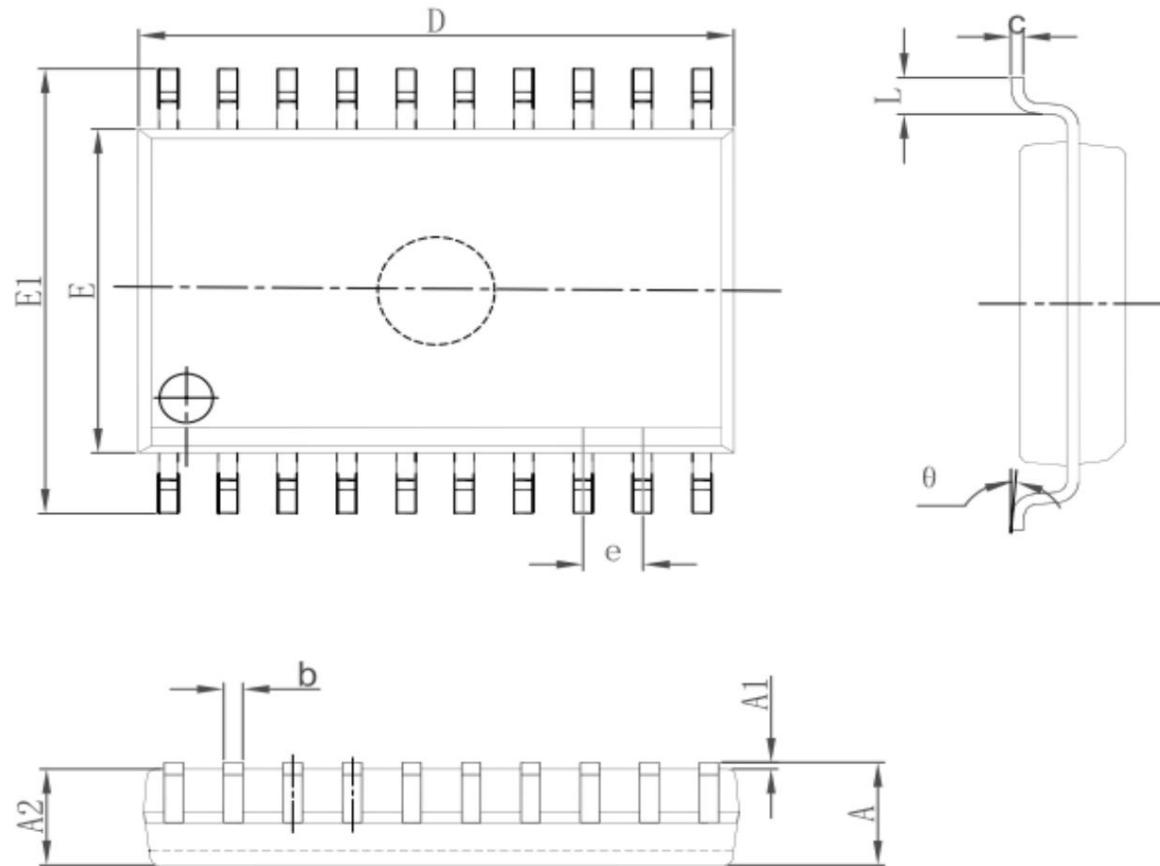
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.700		0.066
A1	0.100	0.200	0.004	0.008
A2	1.400	1.500	0.055	0.059
A3	0.620	0.680	0.024	0.027
b	0.370	0.420	0.015	0.016
D	8.710	8.910	0.343	0.347
AN	5.900	6.100	0.232	0.238
E1	3.800	3.950	0.150	0.156
It is	1.270(BSC)		0.050(BSC)	
L	0.500	0.700	0.020	0.027
L1	0.250(BSC)		0.010(BSC)	

SOP16ÿ



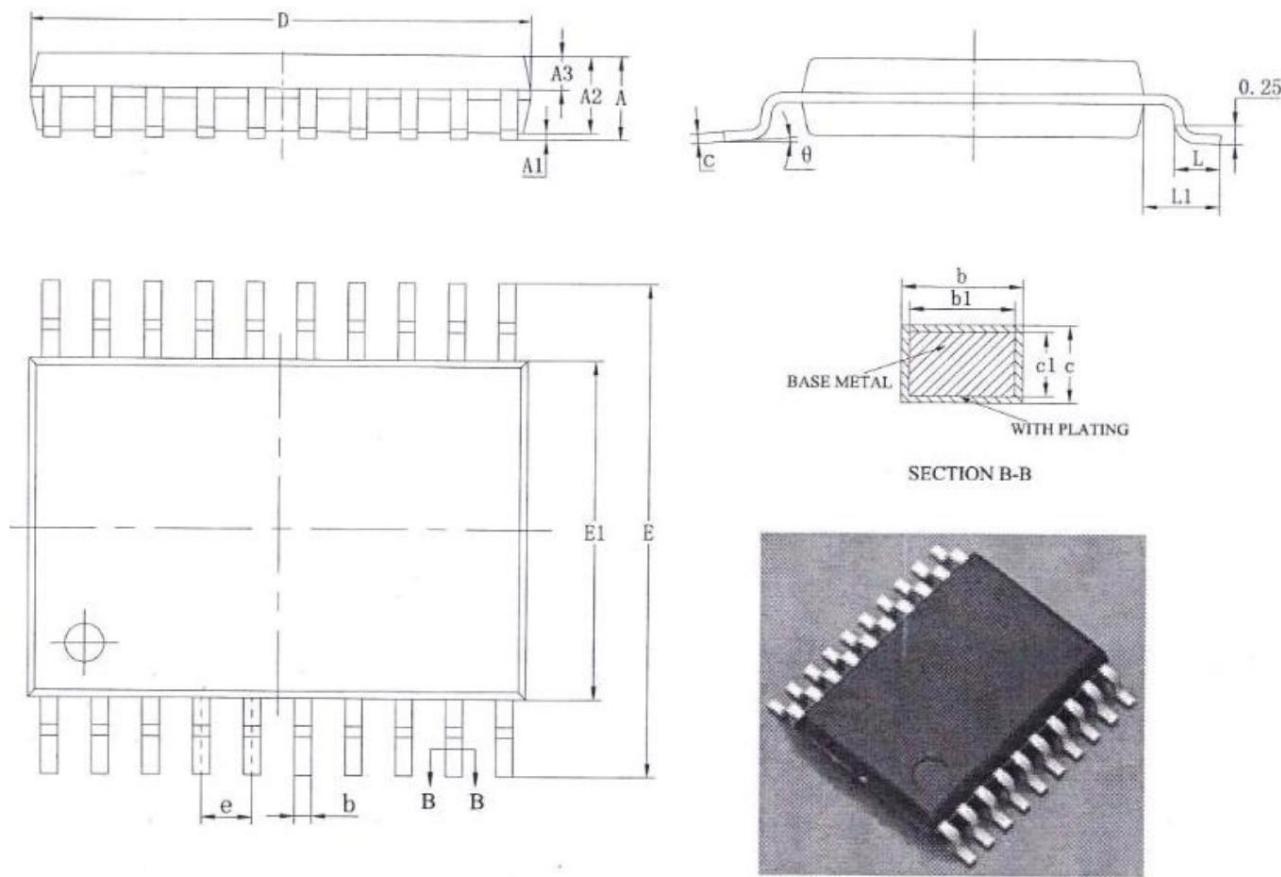
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.700		0.066
A1	0.100	0.200	0.004	0.008
A2	1.420	1.480	0.056	0.058
A3	0.620	0.680	0.024	0.027
D	9.960	10.160	0.392	0.396
ANd	5.900	6.100	0.232	0.238
E1	3.870	3.930	0.152	0.153
b	0.370	0.430	0.015	0.017
It is	1.240	1.300	0.048	0.051
L	0.500	0.700	0.020	0.027
L1	1.050(REF)		0.041(REF)	
L2	0.250(BSC)		0.010(BSC)	

SOP20ÿ



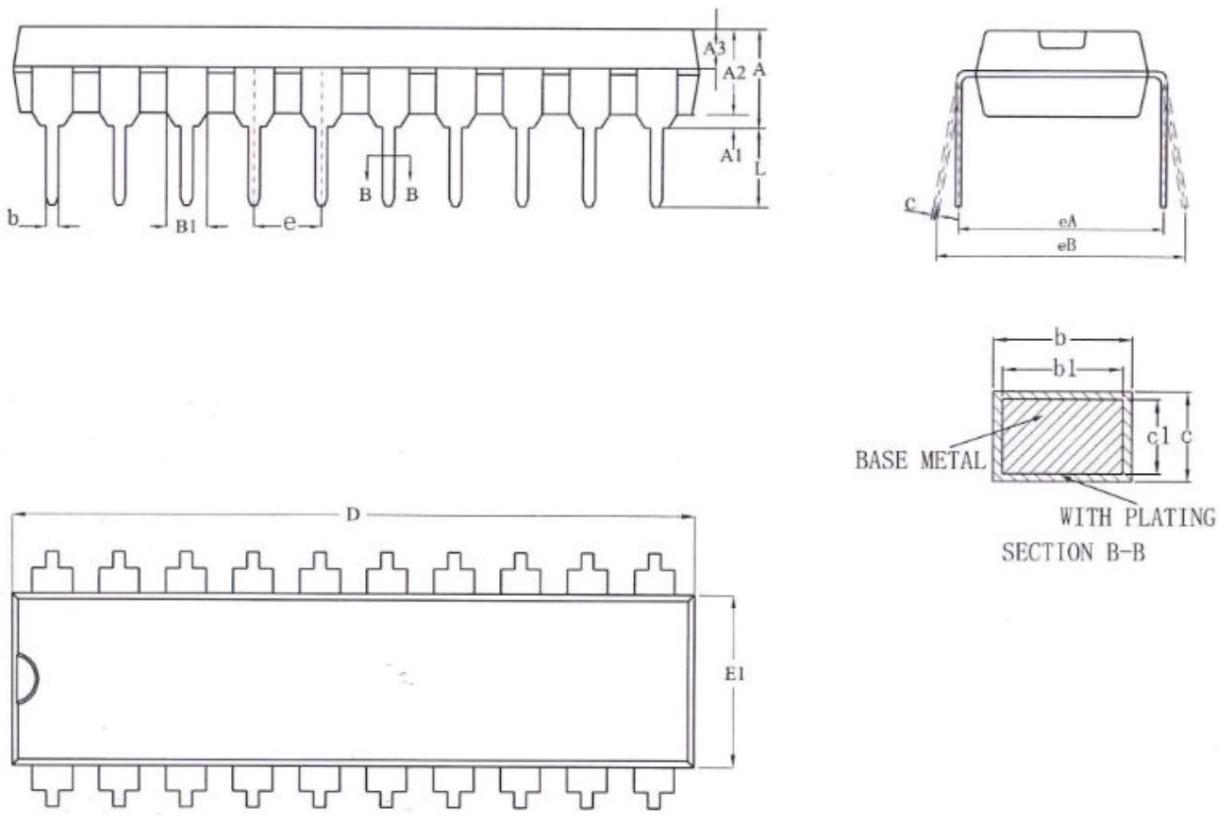
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
ÿ AND ÿ</td <td>7.400</td> <td>7.600</td> <td>0.291</td> <td>0.299</td>	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
It is	1.270ÿBSCÿ		0.050ÿBSCÿ	
L	0.400	1.270	0.016	0.050
i	0°	8°	0°	8°

TSSOP20Y



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
A3	0.39	0.49	0.015	0.019
b	0.20	0.28	0.008	0.011
b1	0.19	0.25	0.008	0.010
c	0.13	0.17	0.005	0.007
c1	0.12	0.14	0.005	0.006
D	6.40	6.60	0.252	0.260
E1	4.30	4.50	0.169	0.177
AND	6.20	6.60	0.244	0.260
It is	0.65(BSC)		0.026(BSC)	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.040REF	
i	0	8°	0	8°

DIP20:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.60	4.00	0.142	0.157
A1	0.51	-	0.020	-
A2	3.20	3.40	0.126	0.134
A3	1.47	1.57	0.058	0.062
b	0.44	0.52	0.017	0.020
b1	0.43	0.49	0.017	0.019
B1	1.52REF		0.060REF	
c	0.25	0.29	0.010	0.011
c1	0.24	0.26	0.009	0.010
D	25.80	26.00	1.016	1.024
E1	6.45	6.65	0.253	0.262
It is	2.54BSC		0.1BSC	
of A	7.62REF		0.3REF	
eB	7.62	9.30	0.3	0.366
eC	0	0.84	0	0.033
L	3.00	-	0.118	-



Appendix 1, Document Change History

date		content
2020-3-23	Version 1.00	First Edition