CDA 4213/CIS 6930 CMOS VLSI
Fall 2021

Final Project
Design Proposal (10%)

Due date
11:59PM, Monday, 8th November

Today's Date:	11/4/2021
Your Team Name:	*Team LGSB*
Team Members:	Josue U83997372, Patrick U76508800, Thomas U89246769
No. of Hours Spent:	Josue: 8Hrs, Patrick: 8Hrs, Thomas: 8Hrs
Exercise Difficulty: (Easy, Average, Hard)	Average
Any Other Feedback:	

(1) **(10 pts)** From the project description, write down the requirements in the form of R1, R2, etc…
Add as many bullets as you need below.

a) Requirement 1 (R1):

Implement a rectangular layout.

b) Requirement 2 (R2):

The inputs X and Y are fed serially to the multiplier.

c) Requirement 3 (R3):

Both X and Y should be registered.

d) Requirement 4 (R3):

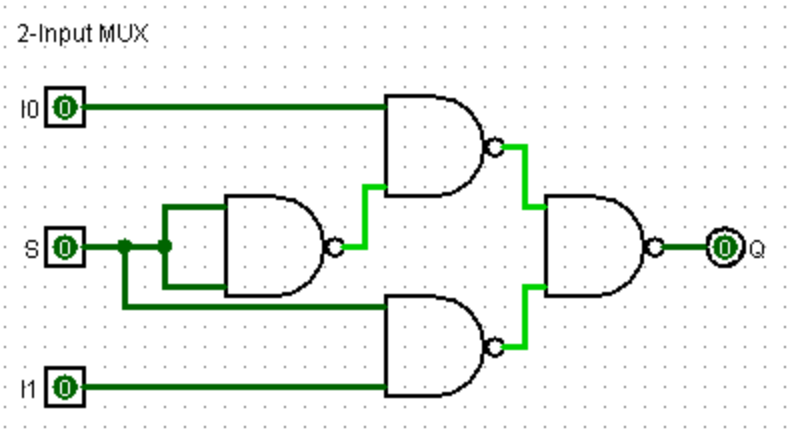
You need to maximize N.

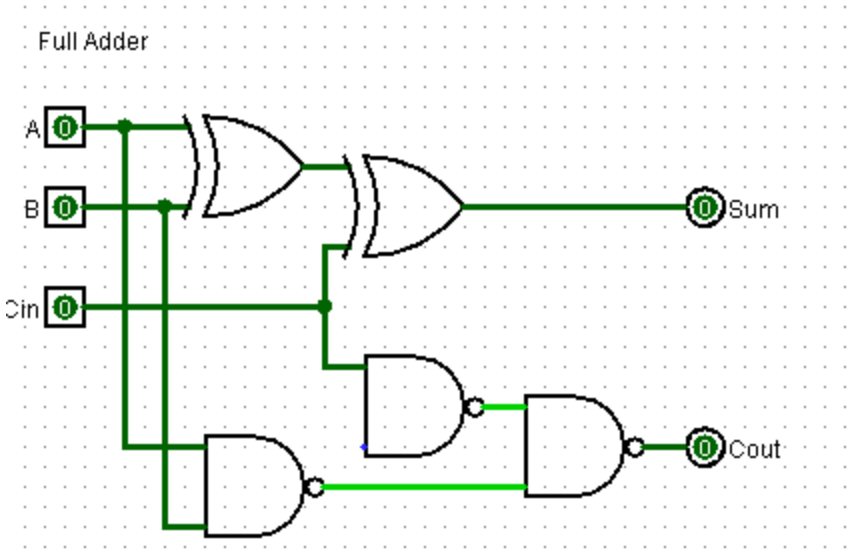
(2) **(50 pts.)** Proposed Design:

(a) List all module bit-slices you will need for your design.

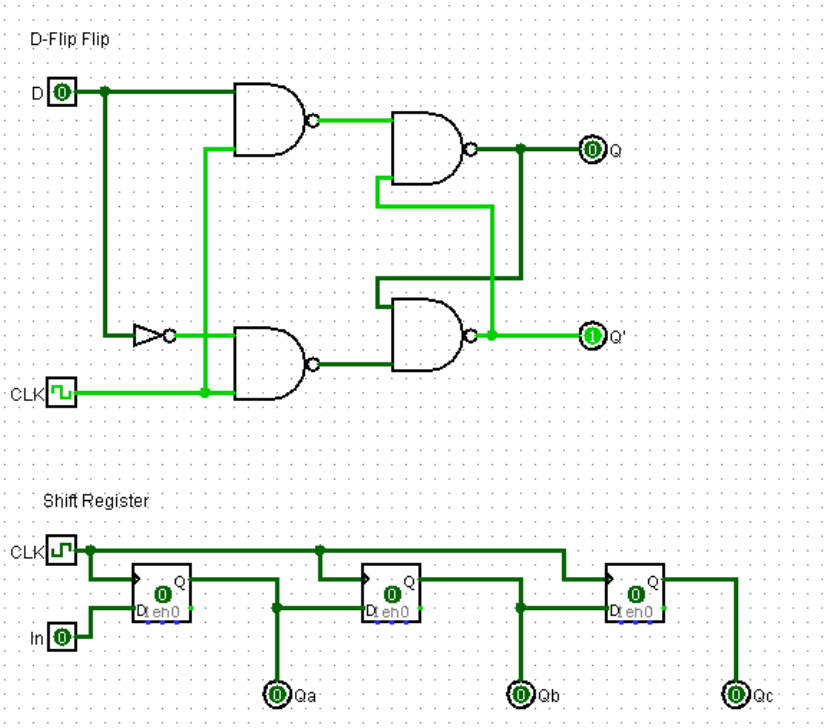
- 2-input MUX
- Shift register
- Full adder

(b) For each bit slice, show the gate-level design.



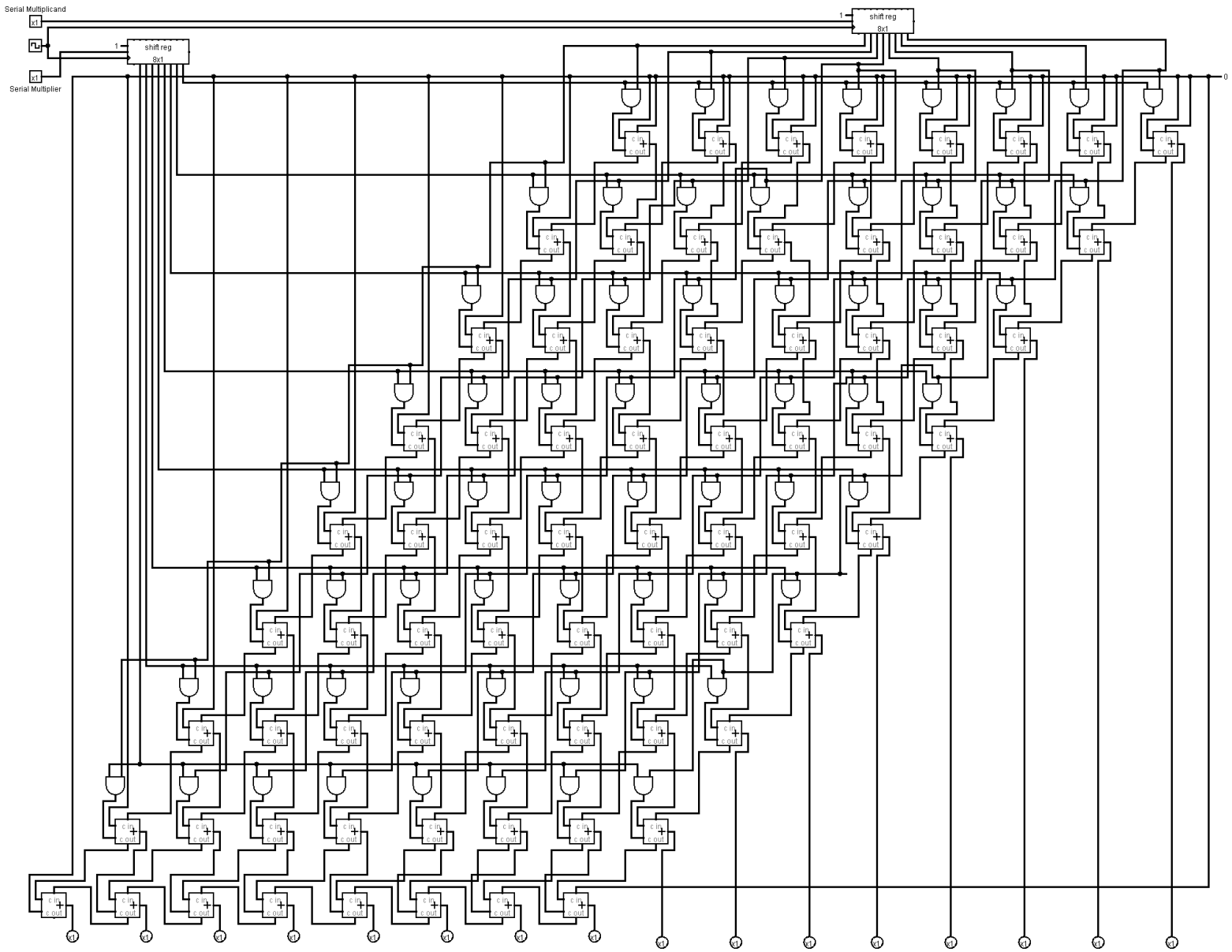


(c) Show the block level design of your register. NOTE: Use Flip-flops for your registers. Do not use Latches.



Note: Each "square" present in the above shift register is an individual representation of the displayed D Flip-Flop.

(d) Show an overall block-level diagram of your design. Briefly, explain how each of the above requirements will be met by your design.



The above block diagram showcases an 8 x 8 bit multiplier. The first requirement is satisfied since the design is roughly rectangular. The second requirement is satisfied by the two shift registers located at the top of the circuit and to the left near the inputs and clock signal being fed serially. The third requirement is met through keeping the inputs X and Y in the shift registers.

(3) **(10 pts)** *Area Estimation:*
(a) Estimate the area of your design. You already have the area numbers for the cells you have designed in lab assignments. Add more rows if needed.
Remember that you have to maximize N.

No.	Cell Name	Individual Cell Area (Sq. Micron)	No. of instances	Total Area	Remarks
1	Shift Register	5290.4	3	15,871.2	
2	Full Adder	768.195	64	49,164.48	
3	AND Gate	171.315	64	10,964.16	
4	2-input MUX	458.265	1	458.265	
Total Estimated Area				76,458.105	

(b) Estimate the size of the multiplier you can fit in a die area of approximately 900 um x 900 um. Total Area: ~100,000 *u*m^2

4.) (10 pts) Work Distribution:

Team Member:

- Josue - Optimizing size restrictions on individual slices.
- Patrick - Working on documentation.
- Tommy - Worked on theoretical layout of circuit in logisim.

5.) (10 pts) Project Schedule & Milestones. *Provide a weekly schedule with important milestones.*

Week 11/1 - 11/5 - Complete Design Proposal
Week 11/8 - 11/12 - Implement 8x8 Design
Week 11/15 - 11/19 - Prepare/Complete Partial Design Demo
Week 11/22 - 11/26 - Finalize 8x8 Design
Week 11/29 - 12/3 - Finalize 8x8 Design (Possibly 16x16 Design)
Week 12/6 - 12/10 - Final Design Demo + Report Submission

6.) (10 pts) Design Validation Plan:

Explain the plan for your design validation by simulation. Consider the following:

a) What input vectors will you test your design with?

Regular mode

1) 0 x 0 = 0
2) 0 x 255 = 0
3) 1 x 255 = 255 (00000001 x 11111111 = 0000000011111111)
4) 12 x 29 = 348 (00001100 x 00011101 = 0000000101011100)
5) 19 x 91 = 1729 (00010011 x 01011011 = 0000011011000001)
** Taxicab number
6) 83 x 97 = 8051 (01010011 x 01100001 = 0001111101110011)
7) 170 x 204 = 34680 (10101010 x 11001100 = 1000011101111000)
8) 255 x 255 = 65025 (11111111 x 11111111 = 1111111000000001)

Test mode

1) all 1's
2) alternating 0's and 1's i.e., 010101...

b) Which input vector(s) will exercise the critical path (longest path)?

7) 170 x 204 = 34680 (10101010 x 11001100 = 1000011101111000)
8) 255 x 255 = 65025 (11111111 x 11111111 = 1111111000000001)

c) How will you estimate the maximum clock speed?

To determine the maximum clock speed, we would have to first calculate the delay for each of our individual components, and find the total delay for all of the components in the layout.