



CC2630 SimpleLink™ 6LoWPAN, ZigBee® Wireless MCU

1 Device Overview

1.1 Features

- Microcontroller
 - Powerful ARM® Cortex®-M3
 - EEMBC CoreMark® Score: 142
 - Up to 48-MHz Clock Speed
 - 128KB of In-System Programmable Flash
 - 8KB of SRAM for Cache
 - 20KB of Ultralow-Leakage SRAM
 - 2-Pin cJTAG and JTAG Debugging
 - Supports Over-The-Air Upgrade (OTA)
- Ultralow-Power Sensor Controller
 - Can Run Autonomous From the Rest of the System
 - 16-Bit Architecture
 - 2KB of Ultralow-Leakage SRAM for Code and Data
- Efficient Code Size Architecture, Placing Drivers, IEEE 802.15.4 MAC, and Bootloader in ROM
- RoHS-Compliant Packages
 - 4-mm × 4-mm RSM VQFN32 (10 GPIOs)
 - 5-mm × 5-mm RHB VQFN32 (15 GPIOs)
 - 7-mm × 7-mm RGZ VQFN48 (31 GPIOs)
- Peripherals
 - All Digital Peripheral Pins Can Be Routed to Any GPIO
 - Four General-Purpose Timer Modules (Eight 16-Bit or Four 32-Bit Timers, PWM Each)
 - 12-Bit ADC, 200-ksamples/s, 8-Channel Analog MUX
 - Continuous Time Comparator
 - Ultralow-Power Analog Comparator
 - Programmable Current Source
 - UART
 - 2× SSI (SPI, MICROWIRE, TI)
 - I2C
 - I2S
 - Real-Time Clock (RTC)
 - AES-128 Security Module
 - True Random Number Generator (TRNG)
 - 10, 15, or 31 GPIOs, Depending on Package Option
 - Support for Eight Capacitive-Sensing Buttons
 - Integrated Temperature Sensor
- External System
 - On-Chip internal DC-DC Converter
 - Very Few External Components
 - Seamless Integration With the SimpleLink™ CC2590 and CC2592 Range Extenders
 - Pin Compatible With the SimpleLink CC13xx in 4-mm × 4-mm and 5-mm × 5-mm VQFN Packages
- Low Power
 - Wide Supply Voltage Range
 - Normal Operation: 1.8 to 3.8 V
 - External Regulator Mode: 1.7 to 1.95 V
 - Active-Mode RX: 5.9 mA
 - Active-Mode TX at 0 dBm: 6.1 mA
 - Active-Mode TX at +5 dBm: 9.1 mA
 - Active-Mode MCU: 61 µA/MHz
 - Active-Mode MCU: 48.5 CoreMark/mA
 - Active-Mode Sensor Controller: 8.2 µA/MHz
 - Standby: 1 µA (RTC Running and RAM/CPU Retention)
 - Shutdown: 100 nA (Wake Up on External Events)
- RF Section
 - 2.4-GHz RF Transceiver Compatible With IEEE 802.15.4 PHY and MAC
 - Excellent Receiver Sensitivity (–100 dBm), Selectivity, and Blocking Performance
 - Link budget of 105 dB
 - Programmable Output Power up to +5 dBm
 - Single-Ended or Differential RF Interface
 - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
 - ETSI EN 300 328 (Europe)
 - EN 300 440 Class 2 (Europe)
 - FCC CFR47 Part 15 (US)
 - ARIB STD-T66 (Japan)
- Tools and Development Environment
 - Full-Feature and Low-Cost Development Kits
 - Multiple Reference Designs for Different RF Configurations
 - Packet Sniffer PC Software
 - Sensor Controller Studio
 - SmartRF™ Studio
 - SmartRF Flash Programmer 2
 - IAR Embedded Workbench® for ARM
 - Code Composer Studio™



1.2 Applications

- Home and Building Automation
- Lighting Control
- Alarm and Security
- Electronic Shelf Labeling
- Proximity Tags
- Wireless Sensor Networks
- Energy Harvesting, Batteryless Sensors, and Actuators
- Smart Grid

1.3 Description

The CC2630 device is a wireless MCU targeting ZigBee® and 6LoWPAN applications.

The device is a member of the CC26xx family of cost-effective, ultralow power, 2.4-GHz RF devices. Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime and allow for operation on small coin cell batteries and in energy-harvesting applications.

The CC2630 device contains a 32-bit ARM Cortex-M3 processor that runs at 48 MHz as the main processor and a rich peripheral feature set that includes a unique ultralow power sensor controller. This sensor controller is ideal for interfacing external sensors and for collecting analog and digital data autonomously while the rest of the system is in sleep mode. Thus, the CC2630 device is ideal for battery-powered and energy harvesting end nodes in ZigBee and 6LoWPAN networks.

The IEEE 802.15.4 MAC is embedded into ROM and runs partly on an ARM Cortex-M0 processor. This architecture improves overall system performance and power consumption and frees up flash memory for the application.

The ZigBee stack is available free of charge from www.ti.com.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC2630F128RGZ	VQFN (48)	7.00 mm × 7.00 mm
CC2630F128RHB	VQFN (32)	5.00 mm × 5.00 mm
CC2630F128RSM	VQFN (32)	4.00 mm × 4.00 mm

(1) For more information, see [Section 9](#), *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 shows a block diagram for the CC2630.

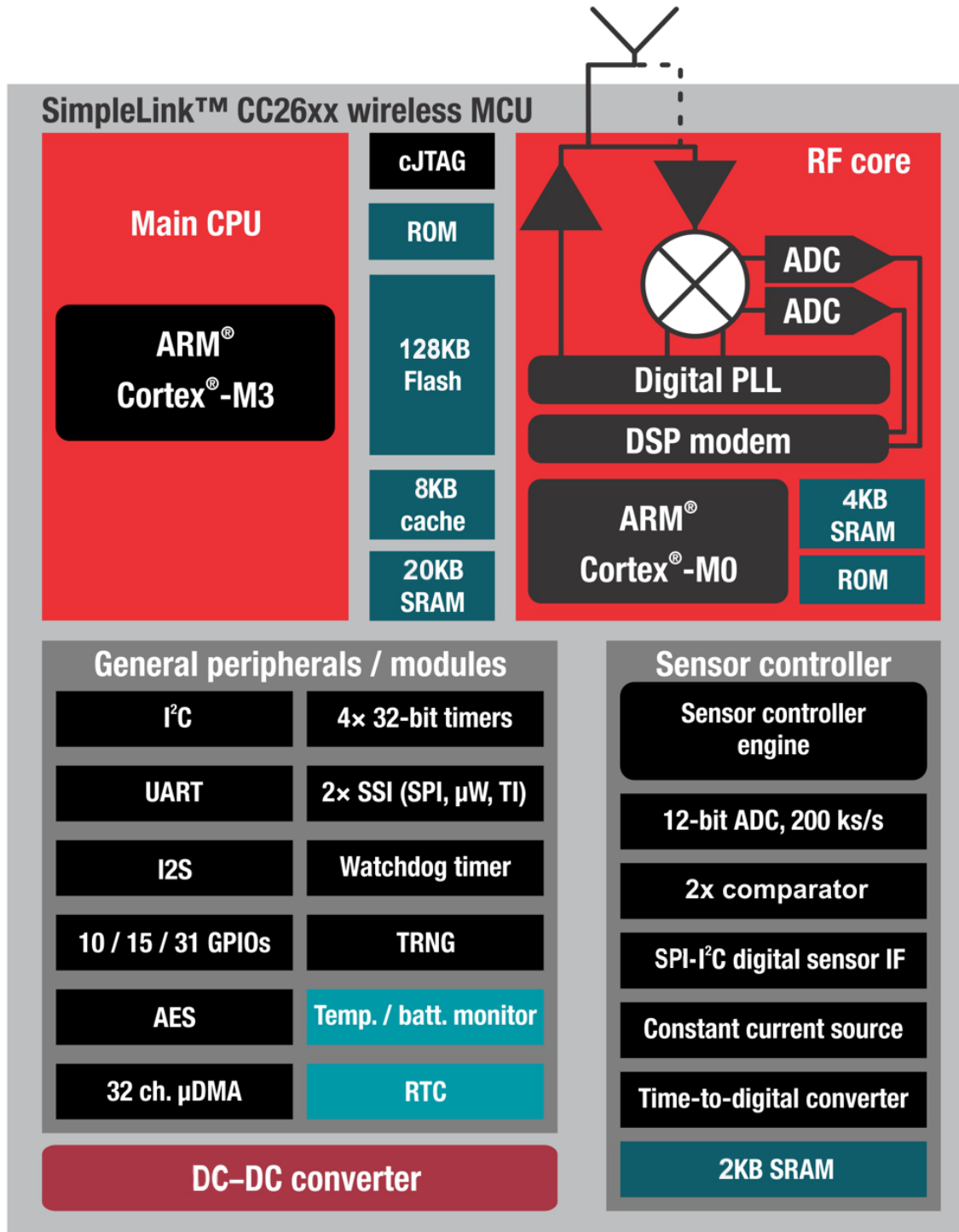


Figure 1-1. Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 21, 2015 to October 15, 2015	Page
<ul style="list-style-type: none"> Removed RHB package option from CC2620 Added motional inductance recommendation to the 24-MHz XOSC table Added VOH and VOL min and max values for 4-mA and 8-mA load Added min and max values for VIH and VIL Added SPI timing parameters Added <i>IEEE 802.15.4 Sensitivity vs Channel Frequency</i> Added <i>RF Output Power vs Channel Frequency</i> Added <i>Receive Mode Current vs Supply Voltage (VDDS)</i> graph Changed SoC ADC <i>ENOB vs Sampling Frequency (Input Frequency = FS / 10)</i> graph Clarified Brown Out Detector status and functionality in the <i>Power Modes</i> table. Added application circuit schematics and layout for 5XD and 4XS 	<ul style="list-style-type: none"> 6 16 19 20 21 23 23 23 24 31 34

3 Device Comparison

Table 3-1. Device Family Overview

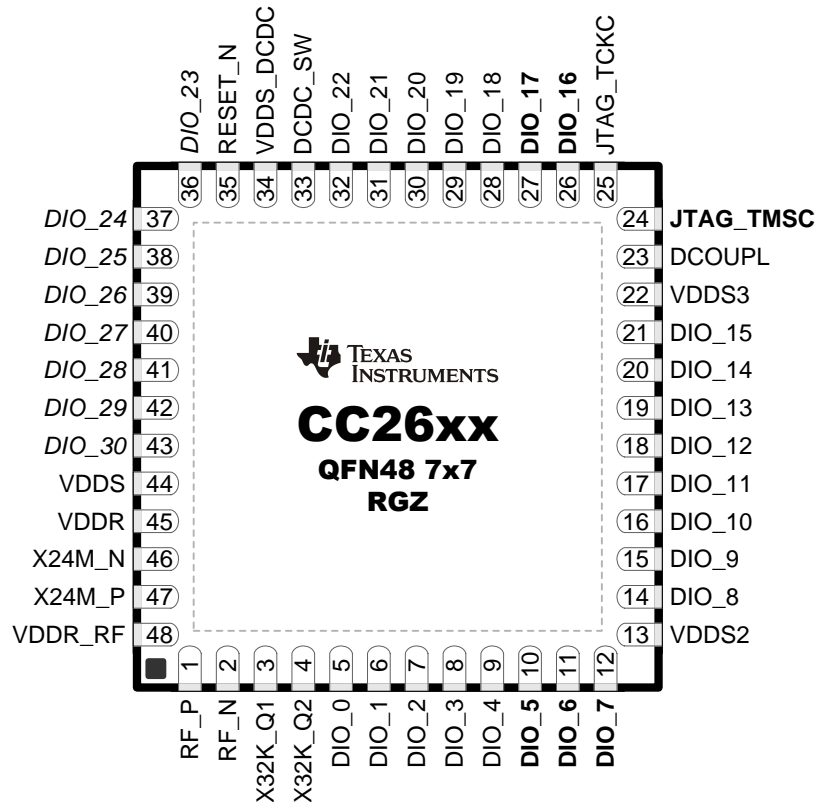
DEVICE	PHY SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE ⁽¹⁾
CC2650F128xxx	Multi-Protocol ⁽²⁾	128	20	31, 15, 10	RGZ, RHB, RSM
CC2640F128xxx	<i>Bluetooth</i> low energy	128	20	31, 15, 10	RGZ, RHB, RSM
CC2630F128xxx	IEEE 802.15.4 Zigbee(/6LoWPAN)	128	20	31, 15, 10	RGZ, RHB, RSM
CC2620F128xxx	IEEE 802.15.4 (RF4CE)	128	20	31, 10	RGZ, RSM

(1) Package designator replaces the xxx in device name to form a complete device name, RGZ is 7-mm × 7-mm VQFN48, RHB is 5-mm × 5-mm VQFN32, and RSM is 4-mm × 4-mm VQFN32.

(2) The CC2650 device supports all PHYs and can be reflashed to run all the supported standards.

4 Terminal Configuration and Functions

4.1 Pin Diagram – RGZ Package



Note: I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

Figure 4-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch

4.2 Signal Descriptions – RGZ Package

Table 4-1. Signal Descriptions – RGZ Package

NAME	NO.	TYPE	DESCRIPTION
DCDC_SW	33	Power	Output from internal DC-DC ⁽¹⁾
DCOUPL	23	Power	1.27-V regulated digital-supply decoupling capacitor ⁽²⁾
DIO_0	5	Digital I/O	GPIO, Sensor Controller
DIO_1	6	Digital I/O	GPIO, Sensor Controller
DIO_2	7	Digital I/O	GPIO, Sensor Controller
DIO_3	8	Digital I/O	GPIO, Sensor Controller
DIO_4	9	Digital I/O	GPIO, Sensor Controller
DIO_5	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_6	11	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_7	12	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO

(1) See [Section 8.2](#), technical reference manual for more details.

(2) Do not supply external circuitry from this pin.

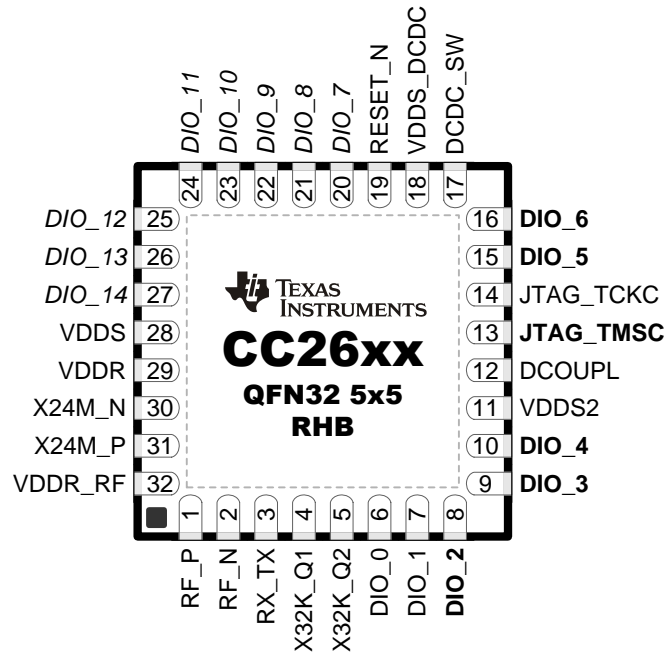
Table 4-1. Signal Descriptions – RGZ Package (continued)

NAME	NO.	TYPE	DESCRIPTION
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_24	37	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_25	38	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_26	39	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_27	40	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_28	41	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_29	42	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_30	43	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMSC	24	Digital I/O	JTAG TMS, high-drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCK
RESET_N	35	Digital input	Reset, active-low. No internal pullup.
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
VDDR	45	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC ⁽³⁾⁽²⁾
VDDR_RF	48	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC ⁽⁴⁾⁽²⁾
VDDS	44	Power	1.8-V to 3.8-V main chip supply ⁽¹⁾
VDDS2	13	Power	1.8-V to 3.8-V DIO supply ⁽¹⁾
VDDS3	22	Power	1.8-V to 3.8-V DIO supply ⁽¹⁾
VDDS_DCDC	34	Power	1.8-V to 3.8-V DC-DC supply
X32K_Q1	3	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	4	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2
EGP		Power	Ground – Exposed Ground Pad

(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.

(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.3 Pin Diagram – RHB Package



Note: I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

Figure 4-2. RHB (5-mm × 5-mm) Pinout, 0.5-mm Pitch

4.4 Signal Descriptions – RHB Package

Table 4-2. Signal Descriptions – RHB Package

NAME	NO.	TYPE	DESCRIPTION
DCDC_SW	17	Power	Output from internal DC-DC ⁽¹⁾
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling ⁽²⁾
DIO_0	6	Digital I/O	GPIO, Sensor Controller
DIO_1	7	Digital I/O	GPIO, Sensor Controller
DIO_2	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	9	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_4	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_5	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_6	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_7	20	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_8	21	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_9	22	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_10	23	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_11	24	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_12	25	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_13	26	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_14	27	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMSC	13	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	14	Digital I/O	JTAG TCKC
RESET_N	19	Digital input	Reset, active-low. No internal pullup.

(1) See [Section 8.2](#), technical reference manual for more details.

(2) Do not supply external circuitry from this pin.

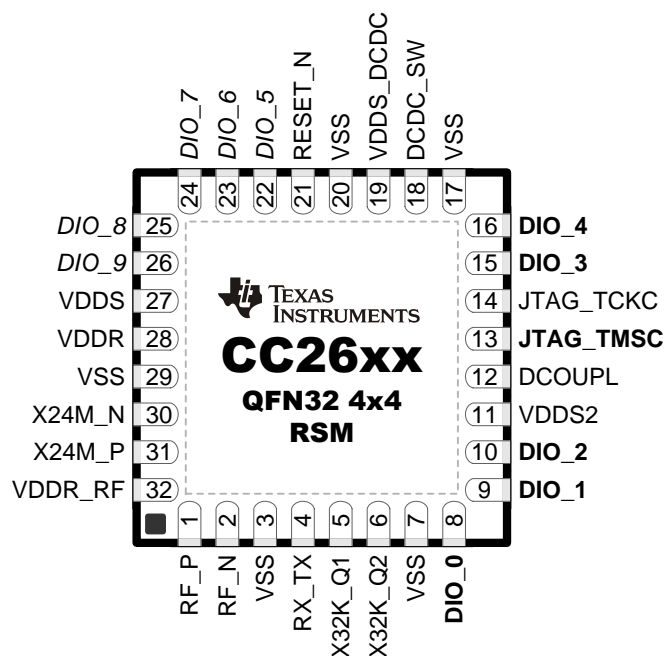
Table 4-2. Signal Descriptions – RHB Package (continued)

NAME	NO.	TYPE	DESCRIPTION
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
VDDR	29	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC ⁽³⁾⁽²⁾
VDDR_RF	32	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC ⁽⁴⁾⁽²⁾
VDDS	28	Power	1.8-V to 3.8-V main chip supply ⁽¹⁾
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply ⁽¹⁾
VDDS_DCDC	18	Power	1.8-V to 3.8-V DC-DC supply
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2
EGP		Power	Ground – Exposed Ground Pad

(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.

(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.5 Pin Diagram – RSM Package



Note: I/O pins marked in **bold** have high drive capabilities. I/O pins marked in *italics* have analog capabilities.

Figure 4-3. RSM (4-mm × 4-mm) Pinout, 0.4-mm Pitch

4.6 Signal Descriptions – RSM Package

Table 4-3. Signal Descriptions – RSM Package

NAME	NO.	TYPE	DESCRIPTION
DCDC_SW	18	Power	Output from internal DC-DC. ⁽¹⁾ Tie to ground for external regulator mode (1.7-V to 1.95-V operation)
DCOUPPL	12	Power	1.27-V regulated digital-supply decoupling capacitor ⁽²⁾
DIO_0	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_1	9	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_2	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	15	Digital I/O	GPIO, High drive capability, JTAG_TDO
DIO_4	16	Digital I/O	GPIO, High drive capability, JTAG_TDI
DIO_5	22	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_6	23	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_7	24	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_8	25	Digital/Analog I/O	GPIO, Sensor Controller, Analog
DIO_9	26	Digital/Analog I/O	GPIO, Sensor Controller, Analog
JTAG_TMISC	13	Digital I/O	JTAG TMISC
JTAG_TCKC	14	Digital I/O	JTAG TCKC
RESET_N	21	Digital Input	Reset, active-low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal to PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal to PA during TX
RX_TX	4	RF I/O	Optional bias pin for the RF LNA

(1) See [Section 8.2](#), technical reference manual for more details.

(2) Do not supply external circuitry from this pin.

Table 4-3. Signal Descriptions – RSM Package (continued)

NAME	NO.	TYPE	DESCRIPTION
VDDR	28	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC. ⁽³⁾⁽²⁾
VDDR_RF	32	Power	1.7-V to 1.95-V supply, typically connect to output of internal DC-DC ⁽⁴⁾⁽²⁾
VDDS	27	Power	1.8-V to 3.8-V main chip supply ⁽¹⁾
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply ⁽¹⁾
VDDS_DCDC	19	Power	1.8-V to 3.8-V DC-DC supply. Tie to ground for external regulator mode (1.7-V to 1.95-V operation).
VSS	3, 7, 17, 20, 29	Power	Ground
X32K_Q1	5	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	6	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2
EGP		Power	Ground – Exposed Ground Pad

(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.

(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Supply voltage, VDD _S ⁽³⁾	VDD _R supplied by internal DC-DC regulator or internal GLDO	−0.3	4.1	V
Supply voltage, VDD _S ⁽³⁾ and VDD _R	External regulator mode (VDD _S and VDD _R pins connected on PCB)	−0.3	2.25	V
Voltage on any digital pin ⁽⁴⁾		−0.3	VDD _S + 0.3, max 4.1	V
Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X24M_N and X24M_P		−0.3	VDD _R + 0.3, max 2.25	V
Voltage on ADC input (V _{in})	Voltage scaling enabled	−0.3	VDD _S	V
	Voltage scaling disabled, internal reference	−0.3	1.49	
	Voltage scaling disabled, VDD _S as reference	−0.3	VDD _S / 2.9	
Input RF level			5	dBm
T _{stg}	Storage temperature	−40	150	°C

(1) All voltage values are with respect to ground, unless otherwise noted.

(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(3) VDD_{S2} and VDD_{S3} must be at the same potential as VDD_S.

(4) Including analog-capable DIO.

5.2 ESD Ratings

			VALUE	UNIT
V _{ESD}	Electrostatic discharge (ESD) performance	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾	All pins	±2500
		Charged device model (CDM), per JESD22-C101 ⁽²⁾	RF pins	±750
			Non-RF pins	±750

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Ambient temperature range		−40	85	°C
Operating supply voltage (VDD _S and VDD _R), external regulator mode	For operation in 1.8-V systems (VDD _S and VDD _R pins connected on PCB, internal DC-DC cannot be used)	1.7	1.95	V
Operating supply voltage (VDD _S)	For operation in battery-powered and 3.3-V systems (internal DC-DC can be used to minimize power consumption)	1.8	3.8	V

5.4 Power Consumption Summary

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$ with internal DC-DC converter, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{core}	Core current consumption	Reset. RESET_N pin asserted or VDD5 below Power-on-Reset threshold		100		nA
		Shutdown. No clocks running, no retention		150		
		Standby. With RTC, CPU, RAM and (partial) register retention. RCOSC_LF		1		μA
		Standby. With RTC, CPU, RAM and (partial) register retention. XOSC_LF		1.2		
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. RCOSC_LF		2.5		
		Standby. With Cache, RTC, CPU, RAM and (partial) register retention. XOSC_LF		2.7		
		Idle. Supply Systems and RAM powered.		550		
		Active. Core running CoreMark		1.45 mA + 31 μA/MHz		
		Radio RX ⁽¹⁾		5.9		mA
		Radio RX ⁽²⁾		6.1		
		Radio TX, 0-dBm output power ⁽¹⁾		6.1		
		Radio TX, 5-dBm output power ⁽²⁾		9.1		
Peripheral Current Consumption (Adds to core current I _{core} for each peripheral unit activated) ⁽³⁾						
I _{peri}	Peripheral power domain	Delta current with domain enabled		20		μA
	Serial power domain	Delta current with domain enabled		13		μA
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle		237		μA
	μDMA	Delta current with clock enabled, module idle		130		μA
	Timers	Delta current with clock enabled, module idle		113		μA
	I ² C	Delta current with clock enabled, module idle		12		μA
	I2S	Delta current with clock enabled, module idle		36		μA
	SSI	Delta current with clock enabled, module idle		93		μA
	UART	Delta current with clock enabled, module idle		164		μA

(1) Single-ended RF mode is optimized for size and power consumption. Measured on CC2650EM-4XS.

(2) Differential RF mode is optimized for RF performance. Measured on CC2650EM-5XD.

(3) I_{peri} is not supported in Standby or Shutdown.

5.5 General Characteristics

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLASH MEMORY					
Supported flash erase cycles before failure		100			k Cycles
Flash page/sector erase current	Average delta current		12.6		mA
Flash page/sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash page/sector erase time ⁽¹⁾			8		ms
Flash write time ⁽¹⁾	4 bytes at a time		8		μs

(1) This number is dependent on Flash aging and will increase over time and erase cycles.

5.6 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – RX

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	Differential mode. Measured at the CC2650EM-5XD SMA connector, PER = 1%		–100		dBm
Receiver sensitivity	Single-ended mode. Measured on CC2650EM-4XS, at the SMA connector, PER = 1%		–97		dBm
Receiver saturation	Measured at the CC2650EM-5XD SMA connector, PER = 1%		+4		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at $\pm 5\text{ MHz}$, PER = 1%		39		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at $\pm 10\text{ MHz}$, PER = 1%		52		dB
Channel rejection, $\pm 15\text{ MHz}$ or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		57		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Spurious emissions, 30 MHz to 1000 MHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–71		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Conducted measurement in a 50 Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		–62		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		>200		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		>1000		ppm
RSSI dynamic range			100		dB
RSSI accuracy			± 4		dB

5.7 IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – TX

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power, highest setting	Delivered to a single-ended 50- Ω load through a balun		5		dBm
Output power, highest setting	Measured on CC2650EM-4XS, delivered to a single-ended 50- Ω load		2		dBm
Output power, lowest setting	Delivered to a single-ended 50- Ω load through a balun		–21		dBm
Error vector magnitude	At maximum output power		2%		

IEEE 802.15.4 (Offset Q-PSK DSSS, 250 kbps) – TX (continued)

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emission conducted measurement	f < 1 GHz, outside restricted bands		–43		dBm
	f < 1 GHz, restricted bands ETSI		–65		
	f < 1 GHz, restricted bands FCC		–76		
	f > 1 GHz, including harmonics		–46		
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				

5.8 24-MHz Crystal Oscillator (XOSC_HF)

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR Equivalent series resistance			20	60	Ω
L_M Motional inductance	Relates to load capacitance (C_L in Farads)		$< 1.6 \times 10^{-24} / C_L^2$		H
C_L Crystal load capacitance		5		9	pF
Crystal frequency			24		MHz
Crystal frequency tolerance ⁽²⁾		–40		40	ppm
Start-up time ⁽³⁾			150		μs

(1) Probing or otherwise stopping the XTAL while the DC-DC converter is enabled may cause permanent damage to the device.

(2) Includes initial tolerance of the crystal, drift over temperature, ageing and frequency pulling due to incorrect load capacitance. As per IEEE 802.15.4 specification.

(3) Kick-started based on a temperature and aging compensated RCOSC_HF using precharge injection.

5.9 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32.768		kHz
ESR Equivalent series resistance			30	100	k Ω
C_L Crystal load capacitance		6		12	pF

5.10 48-MHz RC Oscillator (RCOSC_HF)

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			48		MHz
Uncalibrated frequency accuracy			$\pm 1\%$		
Calibrated frequency accuracy ⁽¹⁾			$\pm 0.25\%$		
Start-up time			5		μs

(1) Accuracy relative to the calibration source (XOSC_HF).

5.11 32-kHz RC Oscillator (RCOSC_LF)

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency			32.8		kHz
Temperature coefficient			50		ppm/ $^\circ\text{C}$

5.12 ADC Characteristics

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range			0		VDD5	V
Resolution				12		Bits
Sample rate					200	ksps
Offset		Internal 4.3-V equivalent reference ⁽²⁾		2		LSB
Gain error		Internal 4.3-V equivalent reference ⁽²⁾		2.4		LSB
DNL ⁽³⁾	Differential nonlinearity			>−1		LSB
INL ⁽⁴⁾	Integral nonlinearity			±3		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		9.8		Bits
		VDD5 as reference, 200 ksps, 9.6-kHz input tone		10		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		−65		dB
		VDD5 as reference, 200 ksps, 9.6-kHz input tone		−69		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		−71		
SINAD, SNDR	Signal-to-noise and Distortion ratio	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		60		dB
		VDD5 as reference, 200 ksps, 9.6-kHz input tone		63		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		69		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference ⁽²⁾ , 200 ksps, 9.6-kHz input tone		67		dB
		VDD5 as reference, 200 ksps, 9.6-kHz input tone		72		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksps, 300-Hz input tone		73		
Conversion time		Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles
Current consumption		Internal 4.3-V equivalent reference ⁽²⁾		0.66		mA
Current consumption		VDD5 as reference		0.75		mA
Reference voltage		Equivalent fixed internal reference (input voltage scaling enabled)		4.3 ⁽²⁾⁽⁵⁾		V
Reference voltage		Fixed internal reference (input voltage scaling disabled)		1.44 ±1%		V
Reference voltage		VDD5 as reference (Also known as <i>RELATIVE</i>) (input voltage scaling enabled)		VDD5		V
Reference voltage		VDD5 as reference (Also known as <i>RELATIVE</i>) (input voltage scaling disabled)		VDD5 / 2.82 ⁽⁵⁾		V
Input Impedance		200 ksps, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241™-2010 for terminology and test methods.

(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.

(3) No missing codes. Positive DNL typically varies from +0.3 to +3.5, depending on device (see [Figure 5-21](#)).

(4) For a typical example, see [Figure 5-22](#).

(5) Applied voltage must be within absolute maximum ratings ([Section 5.1](#)) at all times.

5.13 Temperature Sensor

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		−40		85	°C

Temperature Sensor (*continued*)

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy			±5		°C
Supply voltage coefficient ⁽¹⁾			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

5.14 Battery Monitor

Measured on the TI CC2650EM-5XD reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV
Range		1.8		3.8	V
Accuracy			13		mV

5.15 Continuous Time Comparator

$T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		VDDS	V
External reference voltage		0		VDDS	V
Internal reference voltage	DCOUPPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from –10 mV to 10 mV		0.72		µs
Current consumption when enabled ⁽¹⁾			8.6		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.16 Low-Power Clocked Comparator

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DD5}	V
Clock frequency			32		kHz
Internal reference voltage, $V_{DD5} / 2$			1.49 – 1.51		V
Internal reference voltage, $V_{DD5} / 3$			1.01 – 1.03		V
Internal reference voltage, $V_{DD5} / 4$			0.78 – 0.79		V
Internal reference voltage, $DCOUP_L / 1$			1.25 – 1.28		V
Internal reference voltage, $DCOUP_L / 2$			0.63 – 0.65		V
Internal reference voltage, $DCOUP_L / 3$			0.42 – 0.44		V
Internal reference voltage, $DCOUP_L / 4$			0.33 – 0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from –50 mV to 50 mV		<1		clock-cycle
Current consumption when enabled			362		nA

5.17 Programmable Current Source

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25 – 20		μA
Resolution			0.25		μA
Current consumption ⁽¹⁾	Including current source at maximum programmable output		23		μA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.18 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_A = 25^\circ\text{C}$, $V_{DD5} = 1.8\text{ V}$					
GPIO VOH at 8-mA load	IOCURRE = 2, high-drive GPIOs only	1.32	1.54		V
GPIO VOL at 8-mA load	IOCURRE = 2, high-drive GPIOs only		0.26	0.32	V
GPIO VOH at 4-mA load	IOCURRE = 1	1.32	1.58		V
GPIO VOL at 4-mA load	IOCURRE = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, $V_{pad} = 0\text{ V}$		71.7		μA
GPIO pulldown current	Input mode, pulldown enabled, $V_{pad} = V_{DD5}$		21.1		μA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.33		V

DC Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_A = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR = 1		2.72		V
GPIO VOL at 4-mA load	IOCURR = 1		0.28		V
$T_A = 25^\circ\text{C}$, $V_{DD5} = 3.8\text{ V}$					
GPIO pullup current	Input mode, pullup enabled, $V_{pad} = 0\text{ V}$		277		μA
GPIO pulldown current	Input mode, pulldown enabled, $V_{pad} = V_{DD5}$		113		μA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 \rightarrow 1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 \rightarrow 0		1.54		V
GPIO input hysteresis	IH = 1, difference between 0 \rightarrow 1 and 1 \rightarrow 0 points		0.4		V
$T_A = 25^\circ\text{C}$					
VIH	Lowest GPIO input voltage reliably interpreted as a «High»			0.8	$V_{DD5}^{(1)}$
VIL	Highest GPIO input voltage reliably interpreted as a «Low»	0.2			$V_{DD5}^{(1)}$

(1) Each GPIO is referenced to a specific V_{DD5} pin. See the technical reference manual listed in [Section 8.2](#) for more details.

5.19 Thermal Characteristics

NAME	DESCRIPTION	RSM ($^\circ\text{C/W}$) ^{(1) (2)}	RHB ($^\circ\text{C/W}$) ^{(1) (2)}	RGZ ($^\circ\text{C/W}$) ^{(1) (2)}
R θ_{JA}	Junction-to-ambient thermal resistance	36.9	32.8	29.6
R $\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	30.3	24.0	15.7
R θ_{JB}	Junction-to-board thermal resistance	7.6	6.8	6.2
Psi $_{JT}$	Junction-to-top characterization parameter	0.4	0.3	0.3
Psi $_{JB}$	Junction-to-board characterization parameter	7.4	6.8	6.2
R $\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	1.9	1.9

(1) $^\circ\text{C/W}$ = degrees Celsius per watt.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*.
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*.

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

5.20 Timing Requirements

		MIN	NOM	MAX	UNIT
Rising supply-voltage slew rate		0		100	mV/μs
Falling supply-voltage slew rate		0		20	mV/μs
Falling supply-voltage slew rate, with low-power flash settings ⁽¹⁾				3	mV/μs
Positive temperature gradient in standby ⁽²⁾	No limitation for negative temperature gradient, or outside standby mode			5	°C/s
CONTROL INPUT AC CHARACTERISTICS⁽³⁾					
RESET_N low duration		1			μs
SYNCHRONOUS SERIAL INTERFACE (SSI)⁽⁴⁾					
S1 (SLAVE) ⁽⁵⁾	t _{clk_per}			65024	system clocks
S2 ⁽⁵⁾	t _{clk_high}		0.5		t _{clk_per}
S3 ⁽⁵⁾	t _{clk_low}		0.5		t _{clk_per}

- (1) For smaller coin cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-μF V_{DD}S input capacitor (see [Figure 7-1](#)) must be used to ensure compliance with this slew rate.
- (2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see [Section 5.11](#)).
- (3) T_A = –40°C to 85°C, V_{DD}S = 1.7 V to 3.8 V, unless otherwise noted.
- (4) T_C = 25°C, V_{DD}S = 3.0 V, unless otherwise noted. Device operating as SLAVE. For SSI MASTER operation, see [Section 5.21](#).
- (5) Refer to SSI timing diagrams [Figure 5-1](#), [Figure 5-2](#), and [Figure 5-3](#).

5.21 Switching Characteristics

Measured on the TI CC2650EM-5XD reference design with T_C = 25°C, V_{DD}S = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKEUP AND TIMING					
Idle → Active			14		μs
Standby → Active			151		μs
Shutdown → Active			1015		μs
SYNCHRONOUS SERIAL INTERFACE (SSI)⁽¹⁾					
S1 (TX only) ⁽²⁾ t _{clk_per} (SSIClk period)	One-way communication to SLAVE	4		65024	system clocks
S1 (TX and RX) ⁽²⁾ t _{clk_per} (SSIClk period)	Normal duplex operation	8		65024	system clocks
S2 ⁽²⁾ t _{clk_high} (SSIClk high time)			0.5		t _{clk_per}
S3 ⁽²⁾ t _{clk_low} (SSIClk low time)			0.5		t _{clk_per}

- (1) Device operating as MASTER. For SSI SLAVE operation, see [Section 5.20](#).
- (2) Refer to SSI timing diagrams [Figure 5-1](#), [Figure 5-2](#), and [Figure 5-3](#).

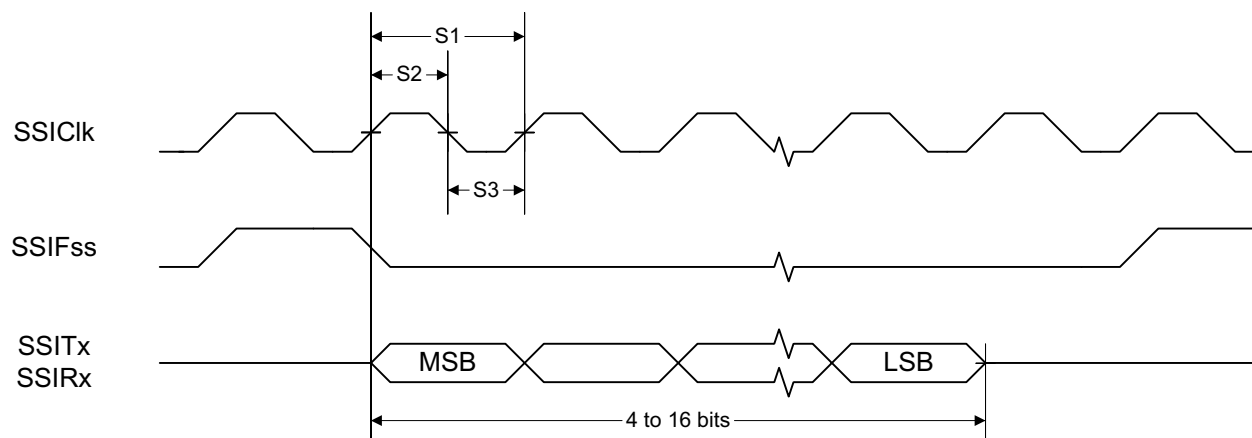


Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

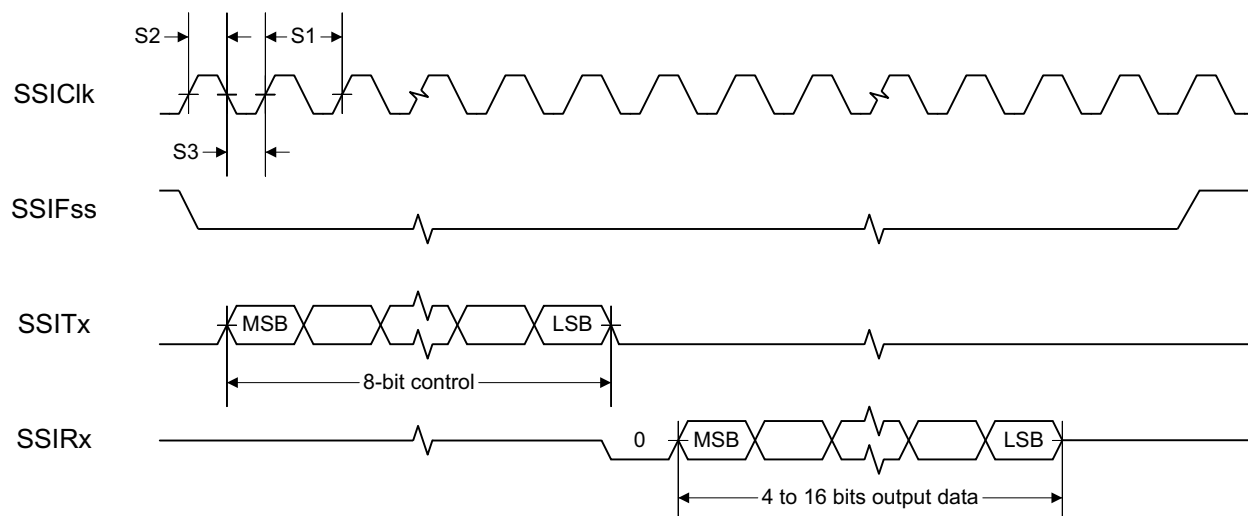


Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

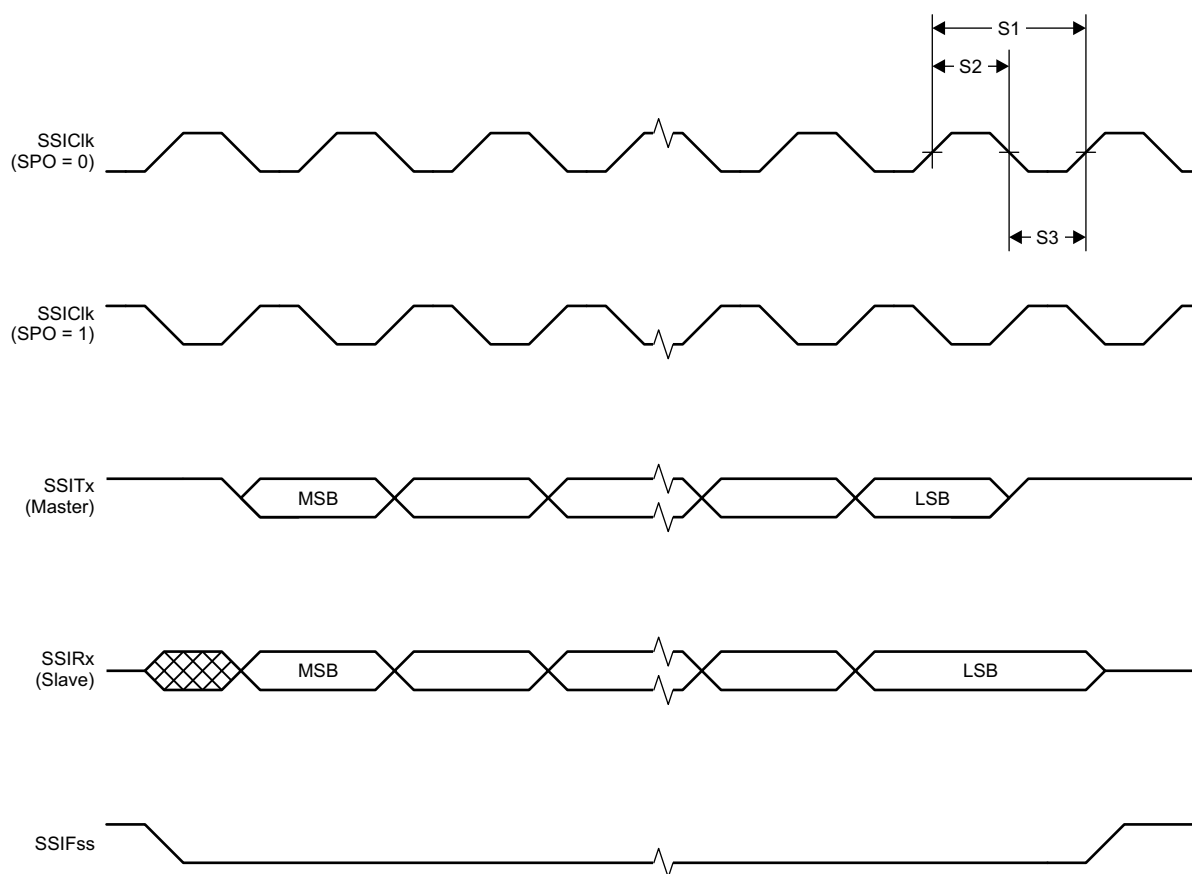


Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.22 Typical Characteristics

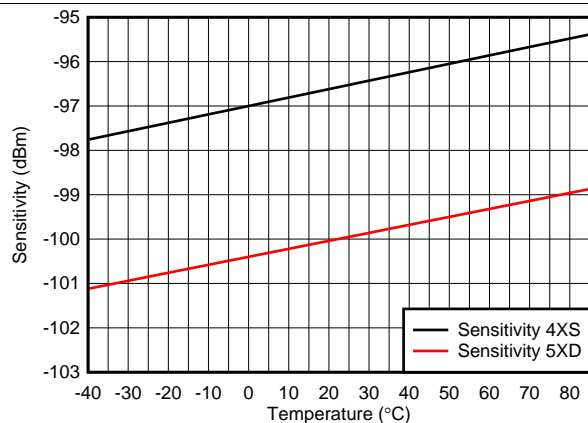


Figure 5-4. IEEE 802.15.4 Sensitivity vs Temperature

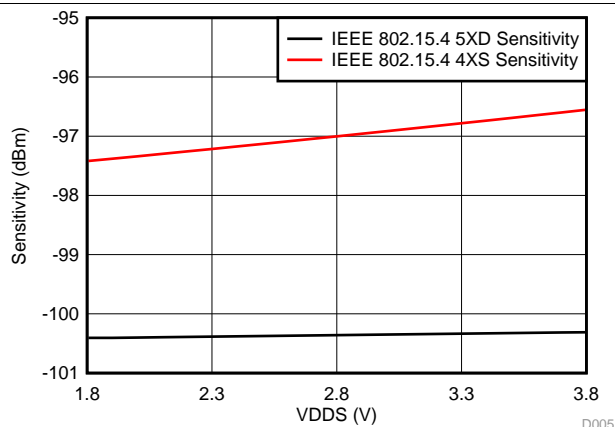


Figure 5-5. IEEE 802.15.4 Sensitivity vs Supply Voltage (VDD5)

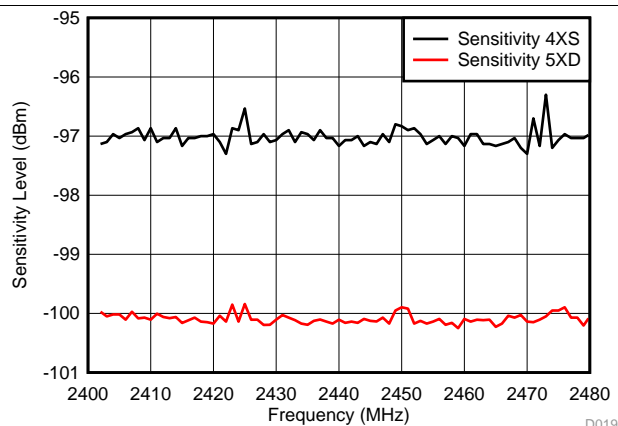


Figure 5-6. IEEE 802.15.4 Sensitivity vs Channel Frequency

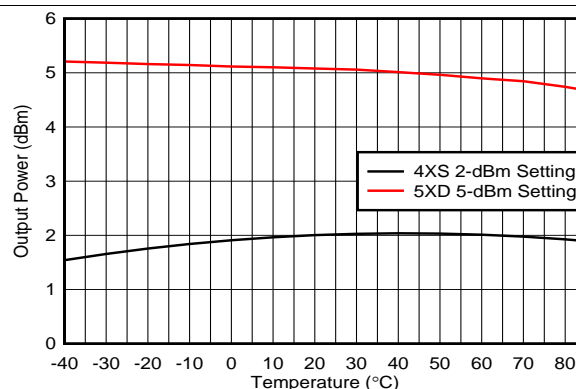


Figure 5-7. TX Output Power vs Temperature

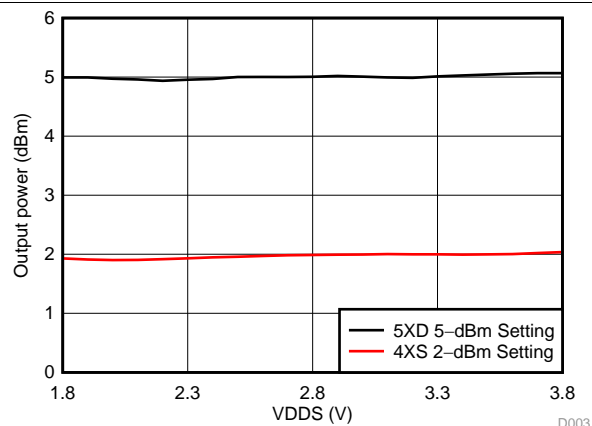


Figure 5-8. TX Output Power vs Supply Voltage (VDD5)

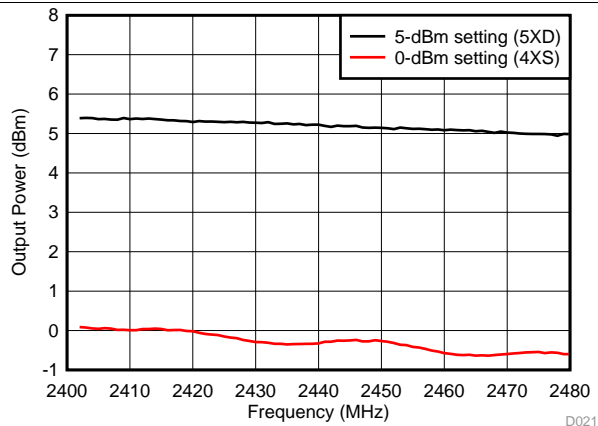


Figure 5-9. TX Output Power vs Channel Frequency

Typical Characteristics (continued)

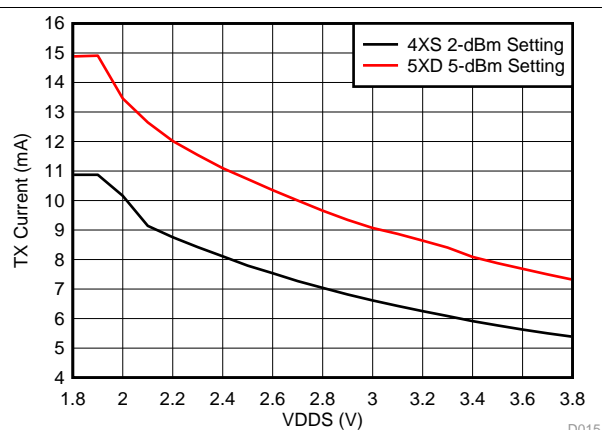


Figure 5-10. TX Current Consumption vs Supply Voltage (VDD5)

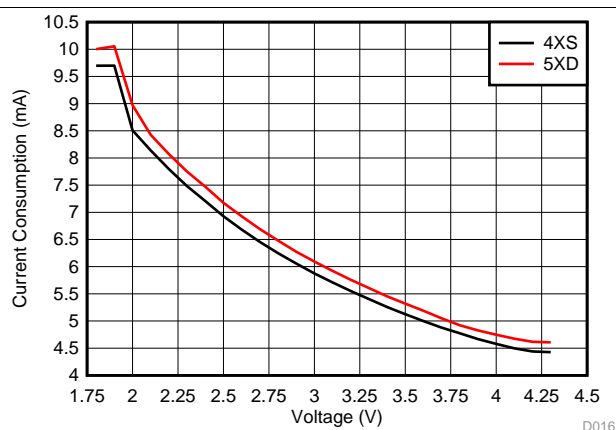


Figure 5-11. RX Mode Current vs Supply Voltage (VDD5)

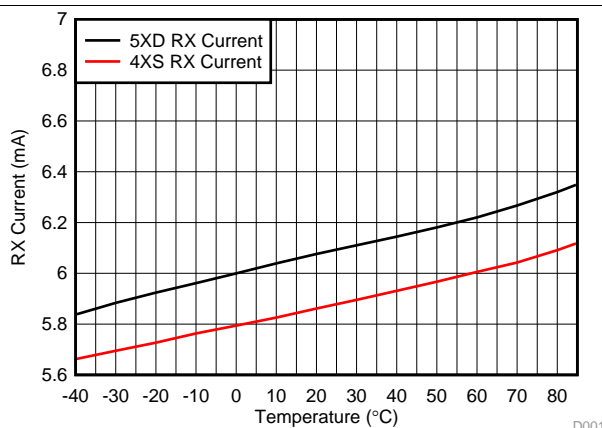


Figure 5-12. RX Mode Current Consumption vs Temperature

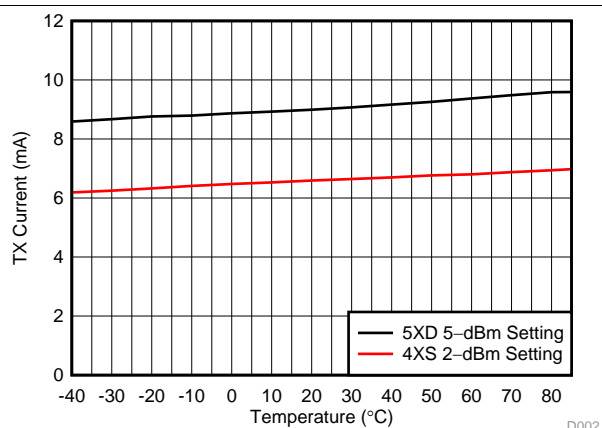


Figure 5-13. TX Mode Current Consumption vs Temperature

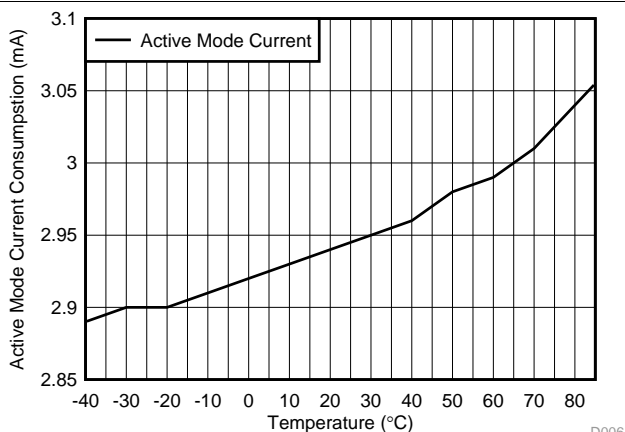


Figure 5-14. Active Mode (MCU Running, No Peripherals) Current Consumption vs Temperature

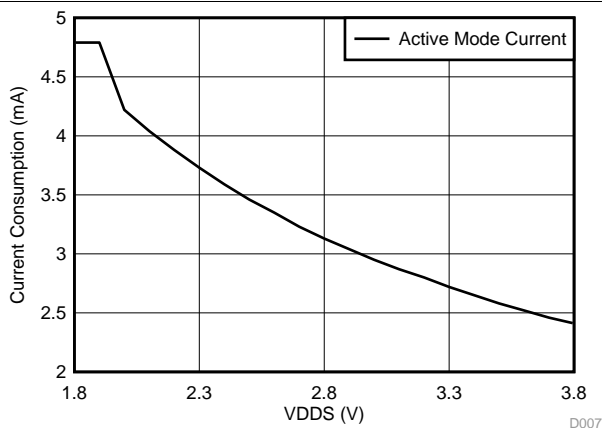


Figure 5-15. Active Mode (MCU Running, No Peripherals) Current Consumption vs Supply Voltage (VDD5)

Typical Characteristics (continued)

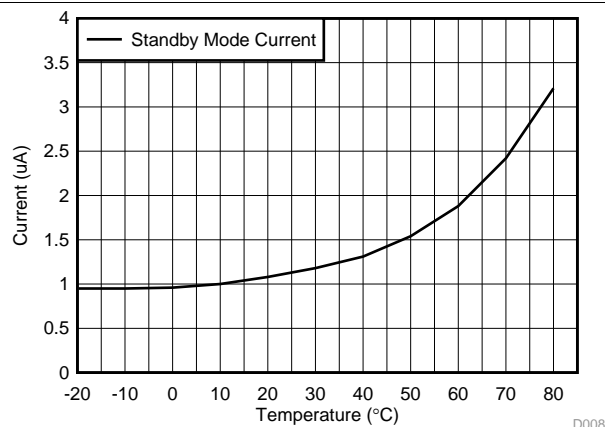


Figure 5-16. Standby Mode Current Consumption With RCOSC RTC vs Temperature

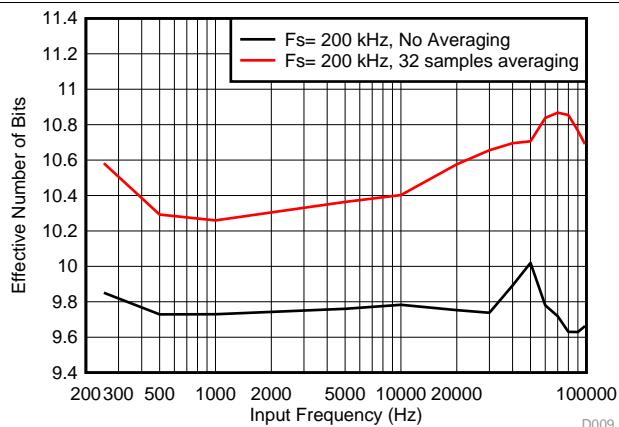


Figure 5-17. SoC ADC Effective Number of Bits vs Input Frequency (Internal Reference, No Scaling)

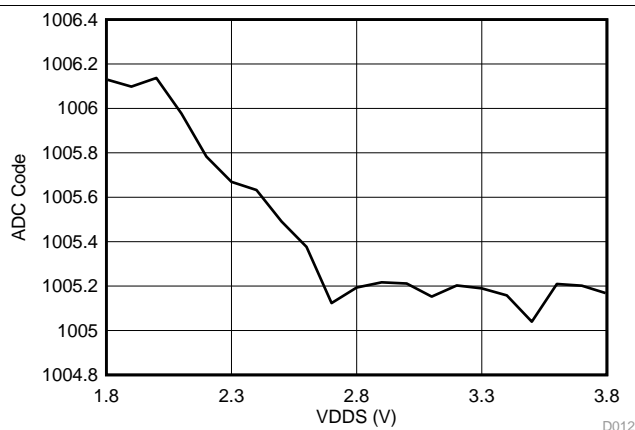


Figure 5-18. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

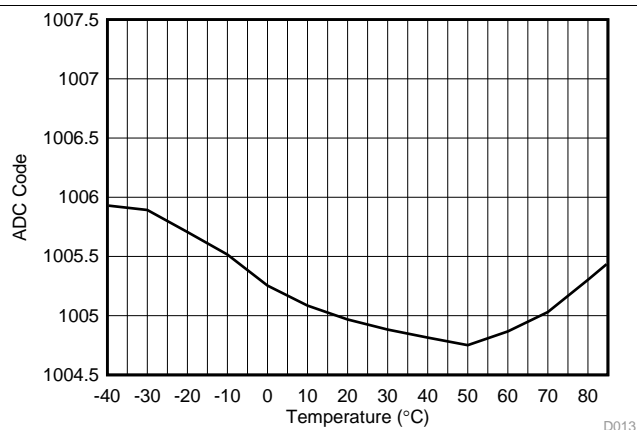


Figure 5-19. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)

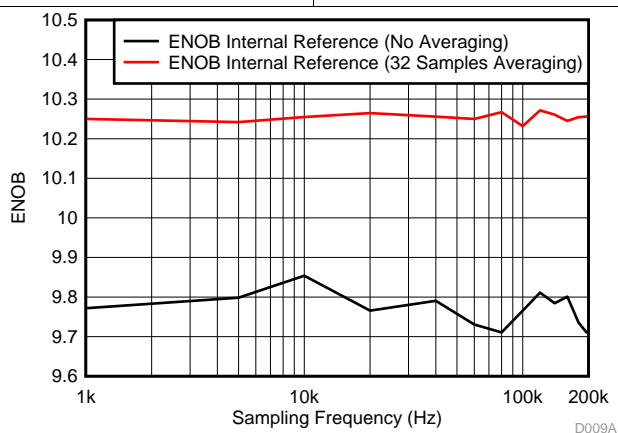
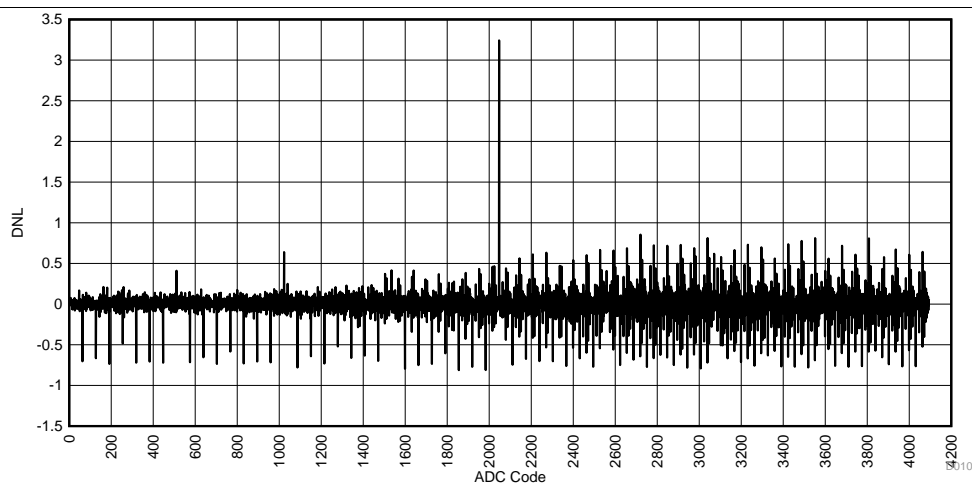
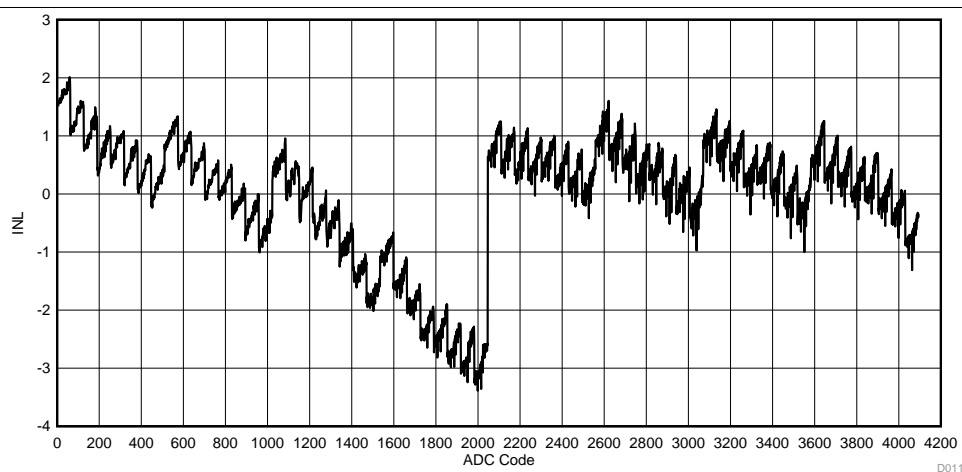


Figure 5-20. SoC ADC ENOB vs Sampling Frequency (Input Frequency = FS / 10)

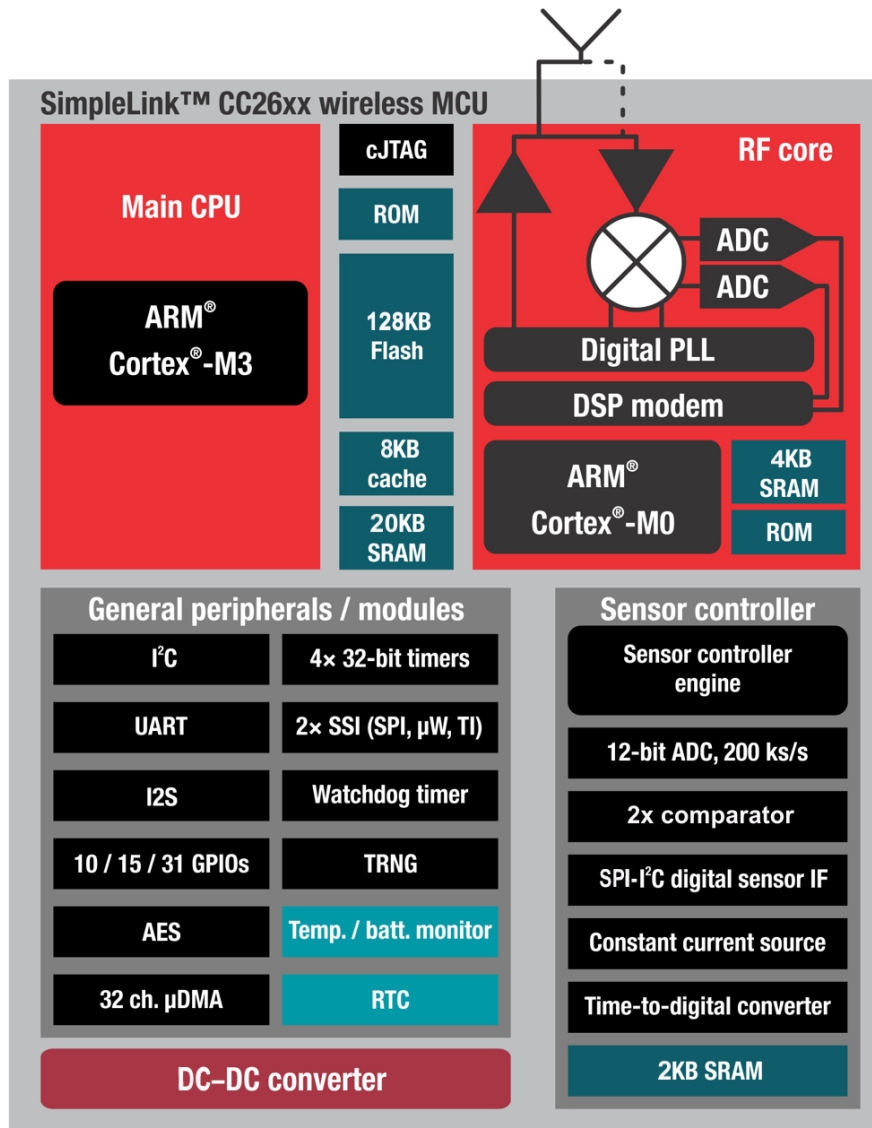
Typical Characteristics (continued)**Figure 5-21. SoC ADC DNL vs ADC Code (Internal Reference, No Scaling)****Figure 5-22. SoC ADC INL vs ADC Code (Internal Reference, No Scaling)**

6 Detailed Description

6.1 Overview

The core modules of the CC26xx product family are shown in the [Section 6.2](#).

6.2 Functional Block Diagram



6.3 Main CPU

The SimpleLink CC2630 Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

CM3 features include the following:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
 - Single-cycle multiply instruction and hardware divide
 - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
 - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultralow-power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.4 RF Core

The RF Core contains an ARM Cortex-M0 processor that interfaces the analog RF and base-band circuitries, handles data to and from the system side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU.

The RF core is capable of autonomously handling the time-critical aspects of the radio protocols (802.15.4 ZigBee) thus offloading the main CPU and leaving more resources for the user application.

The RF core has a dedicated 4-KB SRAM block and runs initially from separate ROM memory. The ARM Cortex-M0 processor is not programmable by customers.

6.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously, thereby significantly reducing power consumption and offloading the main CM3 CPU.

The Sensor Controller is set up using a PC-based configuration tool, called Sensor Controller Studio, and potential use cases may be (but are not limited to):

- Analog sensors using integrated ADC
- Digital sensors using GPIOs, bit-banged I²C, and SPI
- UART communication for sensor reading or debugging
- Capacitive sensing
- Waveform generation
- Pulse counting
- Keyboard scan
- Quadrature decoder for polling rotation sensors
- Oscillator calibration

NOTE

Texas Instruments provides application examples for some of these use cases, but not for all of them.

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller will take care of baseline tracking, hysteresis, filtering and other related functions.
- The ADC is a 12-bit, 200-kSamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The Sensor Controller also includes a SPI–I²C digital interface.
- The analog modules can be connected to up to eight different GPIOs.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1. GPIOs Connected to the Sensor Controller⁽¹⁾

ANALOG CAPABLE	7 × 7 RGZ DIO NUMBER	5 × 5 RHB DIO NUMBER	4 × 4 RSM DIO NUMBER
Y	30	14	
Y	29	13	
Y	28	12	
Y	27	11	9
Y	26	9	8
Y	25	10	7
Y	24	8	6
Y	23	7	5
N	7	4	2
N	6	3	1
N	5	2	0
N	4	1	
N	3	0	
N	2		
N	1		
N	0		

(1) Depending on the package size, up to 16 pins can be connected to the Sensor Controller. Up to 8 of these pins can be connected to analog modules.

6.6 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) can be used for both storage of data and execution of code and is split into two 4-KB blocks and two 6-KB blocks. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as a general-purpose RAM.

The ROM provides preprogrammed embedded TI RTOS kernel, Driverlib and lower layer protocol stack software (802.15.4 MAC). It also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.7 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.8 Power Management

To minimize power consumption, the CC2630 device supports a number of power modes and power management features (see [Table 6-2](#)).

Table 6-2. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.45 mA + 31 µA/MHz	550 µA	1 µA	0.15 µA	0.1 µA
Wake-up Time to CPU Active ⁽¹⁾	–	14 µs	151 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake up on RTC	Available	Available	Available	Off	Off
Wake up on Pin Edge	Available	Available	Available	Available	Off
Wake up on Reset Pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled ⁽²⁾	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead

(2) The Brown Out Detector is disabled between recharge periods in STANDBY. Lowering the supply voltage below the BOD threshold between two recharge periods while in STANDBY may cause the BOD to lock the device upon wake-up until a Reset/POR releases it. To avoid this, it is recommended that STANDBY mode is avoided if there is a risk that the supply voltage (VDD5) may drop below the specified operating voltage range. For the same reason, it is also good practice to ensure that a power cycling operation, such as a battery replacement, triggers a Power-on-reset by ensuring that the VDD5 decoupling network is fully depleted before applying supply voltage again (for example, inserting new batteries).

In active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [Table 6-2](#)).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event will bring the processor back into active mode.

In standby mode, only the always-on domain (AON) is active. An external wake event, RTC event, or sensor-controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is turned off entirely, including the AON domain and the Sensor Controller. The I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from Shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset in this way, a reset-by-reset pin, or a power-on-reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the Flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the main CPU, which means that the main CPU does not have to wake up, for example, to execute an ADC sample or poll a digital sensor over SPI. The main CPU saves both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio enables the user to configure the sensor controller and choose which peripherals are controlled and which conditions wake up the main CPU.

6.9 Clock Systems

The CC2630 supports two external and two internal clock sources.

A 24-MHz crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32-kHz crystal is optional. The low-speed crystal oscillator is designed for use with a 32-kHz watch-type crystal.

The internal high-speed oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed oscillator (32.768-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.10 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high drive capabilities (marked in **bold** in [Section 4](#)).

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver/transmitter function. It supports flexible baud-rate generation up to a maximum of 3 Mbps.

Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.

In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.

The I²C interface is used to communicate with devices compatible with the I²C standard. The I²C interface is capable of 100-kHz and 400-kHz operation, and can serve as both I²C master and I²C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (μ DMA) controller. The μ DMA controller provides a way to offload data transfer tasks from the CM3 CPU, allowing for more efficient use of the processor and the available bus bandwidth. The μ DMA controller can perform transfer between memory and peripherals. The μ DMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. Some features of the μ DMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory
 - Peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except for in Shutdown (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare and one capture registers. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and give a battery status indication as well as a coarse temperature measure.

6.11 System Architecture

Depending on the product configuration, CC26xx can function either as a Wireless Network Processor (WNP—an IC running the wireless protocol stack, with the application running on a separate MCU), or as a System-on-Chip (SoC), with the application and protocol stack running on the ARM CM3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

Very few external components are required for the operation of the CC2630 device. This section provides some general information about the various configuration options when using the CC2630 in an application, and then shows two examples of application circuits with schematics and layout. Complete reference designs are available in the product folder on www.ti.com. Figure 7-1 shows the various RF front-end configuration options. The RF front end can be used in differential- or single-ended configurations with the options of having internal or external biasing. These options allow for various trade-offs between cost, board space, and RF performance. Differential operation with external bias gives the best performance while single-ended operation with internal bias gives the least amount of external components and the lowest power consumption. Reference designs exist for each of these options.

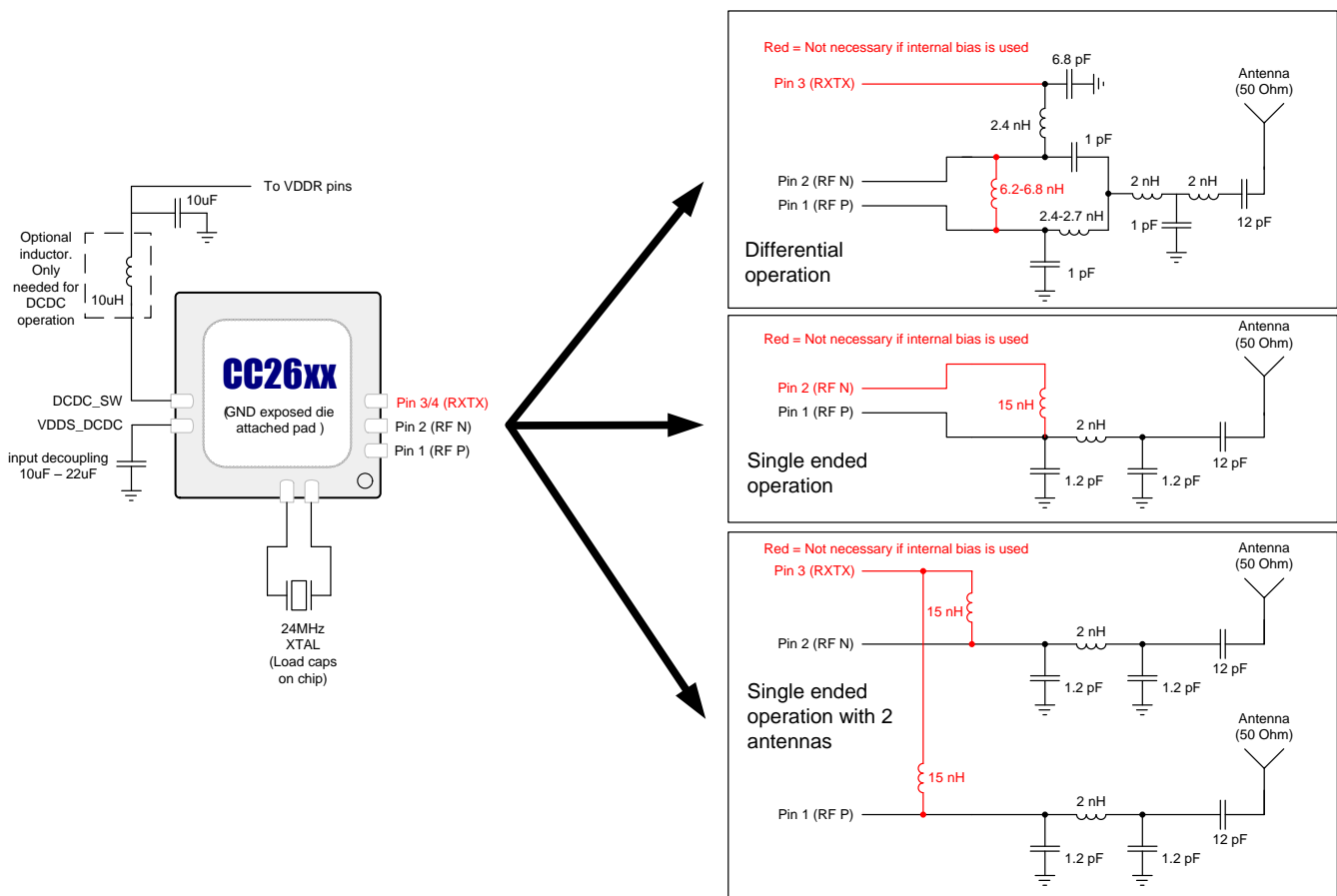


Figure 7-1. CC2630 Application Circuit

Figure 7-2 shows the various supply voltage configuration options. Not all power supply decoupling capacitors or digital I/Os are shown. Exact pin positions will vary between the different package options. For a detailed overview of power supply decoupling and wiring, see the TI reference designs and the CC26xx technical reference manual (Section 8.2).

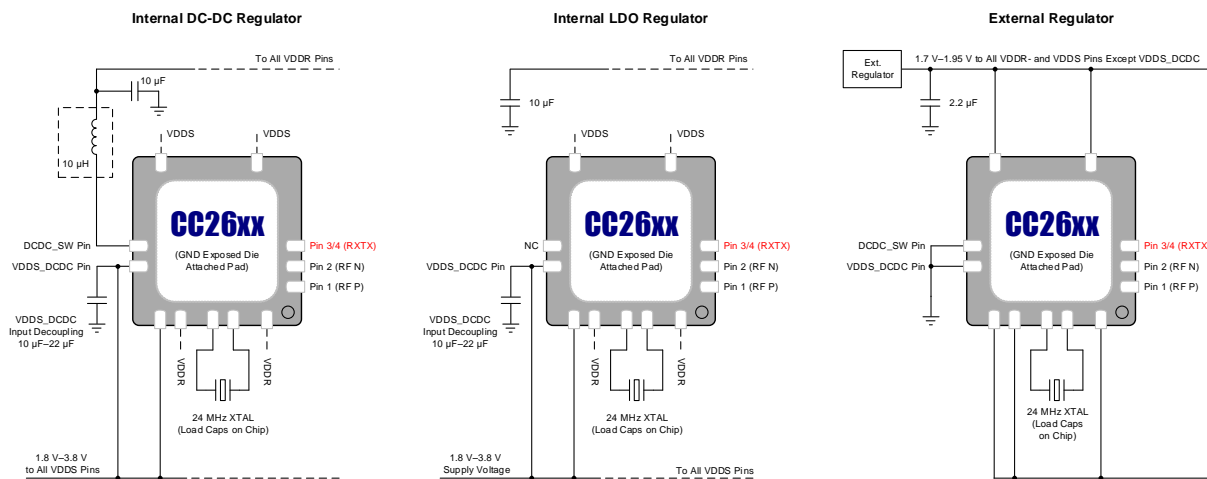


Figure 7-2. Supply Voltage Configurations

7.2 5 × 5 External Differential (5XD) Application Circuit

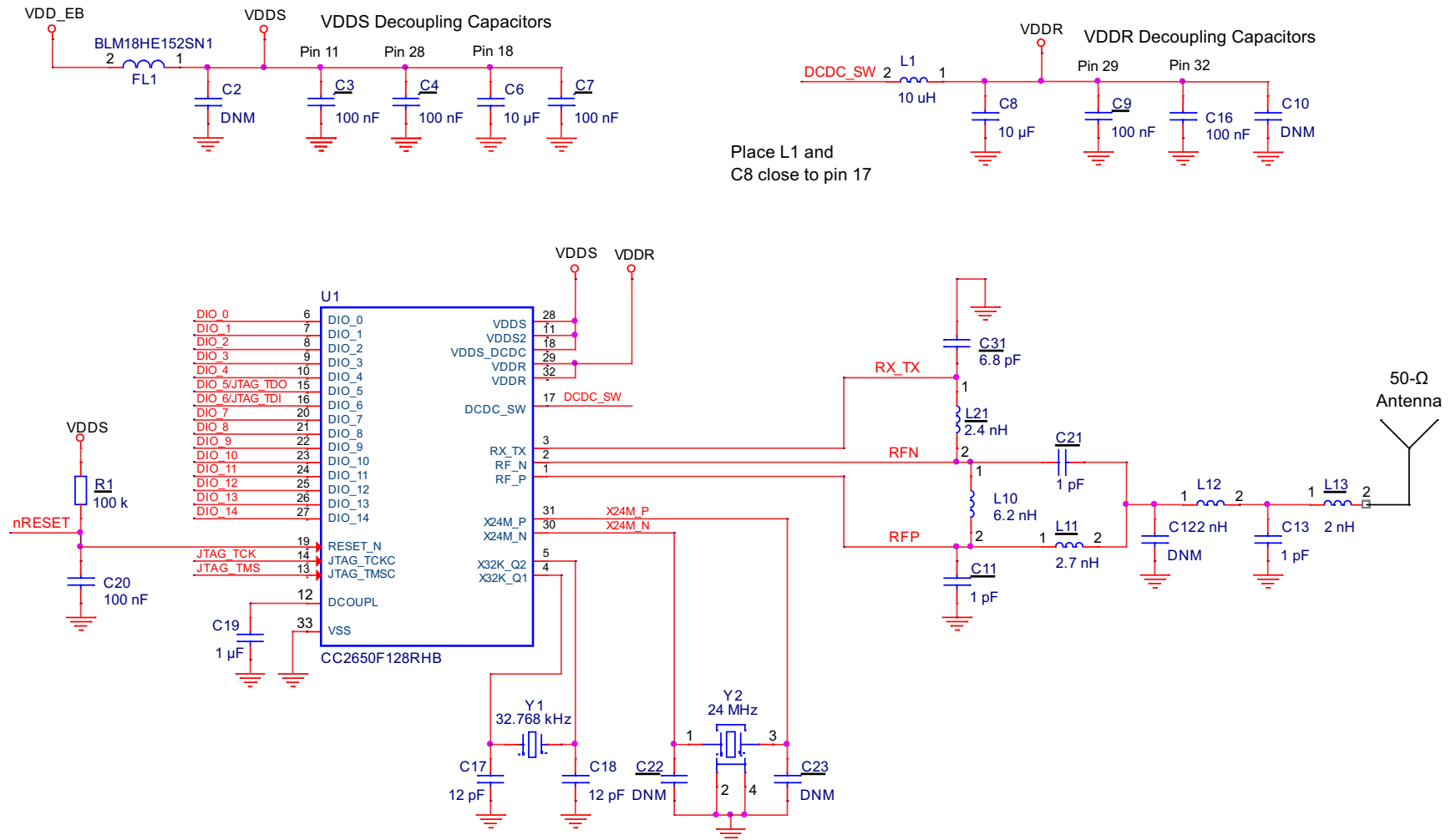


Figure 7-3. 5 × 5 External Differential (5XD) Application Circuit

7.2.1 Layout

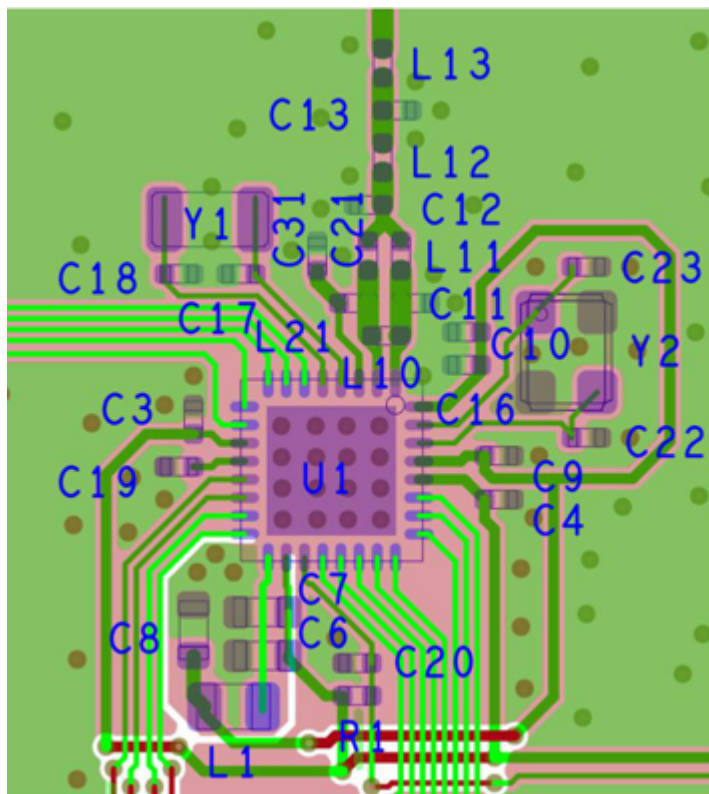


Figure 7-4. 5 × 5 External Differential (5XD) Layout

7.3 4 × 4 External Single-ended (4XS) Application Circuit

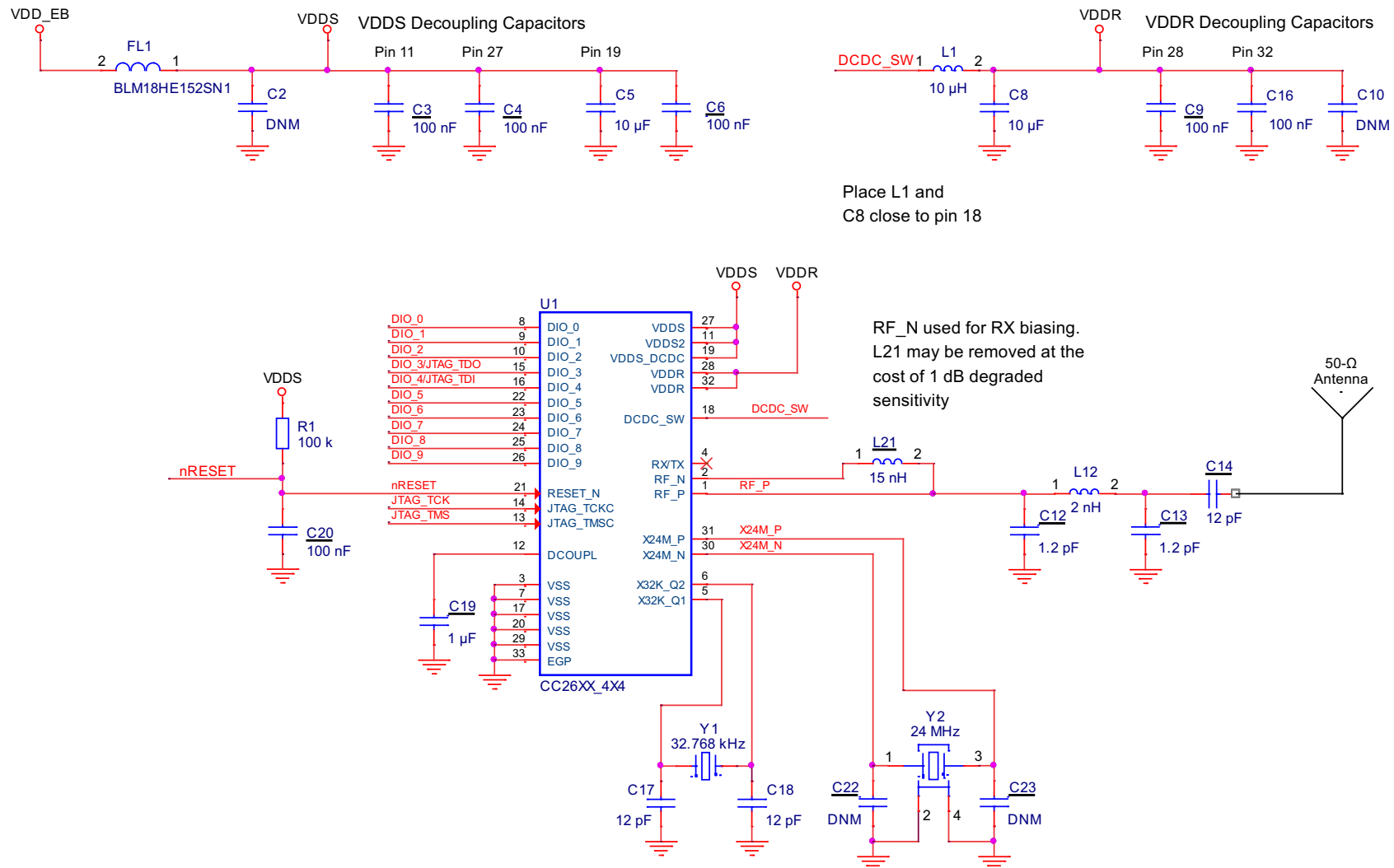


Figure 7-5. 4 × 4 External Single-ended (4XS) Application Circuit

7.3.1 Layout

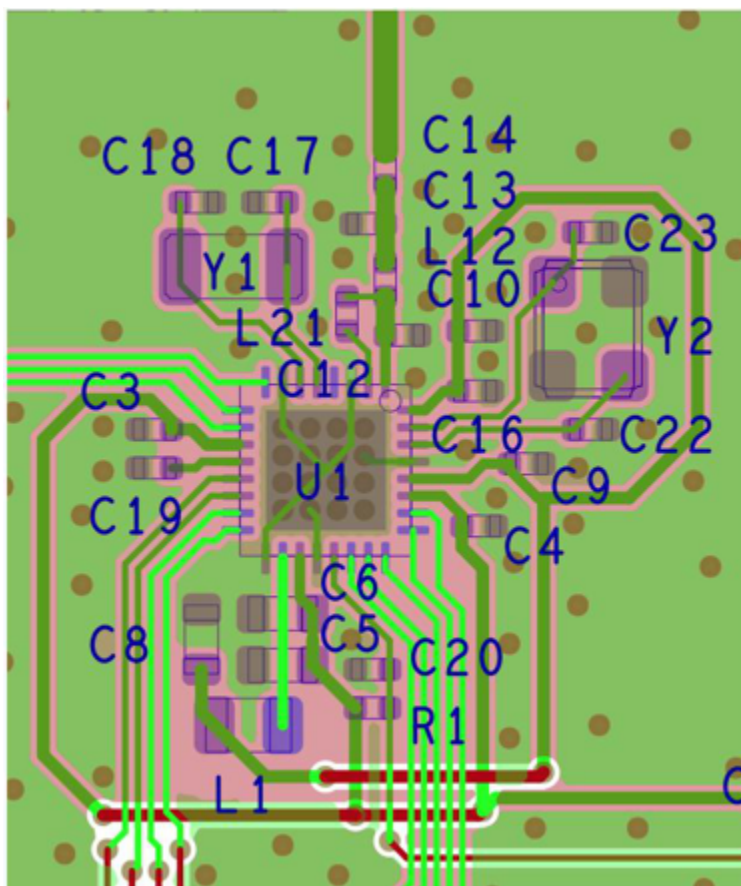


Figure 7-6. 4 x 4 External Single-ended (4XS) Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of the CC2630 device applications:

Software Tools:

SmartRF Studio 7:

SmartRF Studio is a PC application that helps designers of radio systems to easily evaluate the RF-IC at an early stage in the design process.

- Test functions for sending and receiving radio packets, continuous wave transmit and receive
- Evaluate RF performance on custom boards by wiring it to a supported evaluation board or debugger
- Can also be used without any hardware, but then only to generate, edit and export radio configuration settings
- Can be used in combination with several development kits for Texas Instruments' CCxxxx RF-ICs

Sensor Controller Studio:

Sensor Controller Studio provides a development environment for the CC26xx Sensor Controller. The Sensor Controller is a proprietary, power-optimized CPU in the CC26xx, which can perform simple background tasks autonomously and independent of the System CPU state.

- Allows for Sensor Controller task algorithms to be implemented using a C-like programming language
- Outputs a Sensor Controller Interface driver, which incorporates the generated Sensor Controller machine code and associated definitions
- Allows for rapid development by using the integrated Sensor Controller task testing and debugging functionality. This allows for live visualization of sensor data and algorithm verification.

IDEs and Compilers:

Code Composer Studio:

- Integrated development environment with project management tools and editor
- Code Composer Studio (CCS) 6.1 and later has built-in support for the CC26xx device family
- Best support for XDS debuggers; XDS100v3, XDS110 and XDS200
- High integration with TI-RTOS with support for TI-RTOS Object View

IAR Embedded Workbench for ARM

- Integrated development environment with project management tools and editor
- IAR EWARM 7.30.3 and later has built-in support for the CC26xx device family
- Broad debugger support, supporting XDS100v3, XDS200, IAR I-Jet and Segger J-Link
- Integrated development environment with project management tools and editor
- RTOS plugin available for [TI-RTOS](#)

For a complete listing of development-support tools for the CC2630 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, CC2630 is in production; therefore, no prefix/identification is assigned).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RSM*).

For orderable part numbers of the CC2630 device in the *RSM*, *RHB* or *RGZ* package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

8.2 Documentation Support

The following documents describe the CC2630. Copies of these documents are available on the Internet at www.ti.com.

SWCU117 *CC26xx SimpleLink™ Wireless MCU Technical Reference Manual*

SWRZ058 *CC26xx SimpleLink™ Wireless MCU Errata*

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.4 Texas Instruments Low-Power RF Website

Texas Instruments' Low-Power RF website has all the latest products, application and design notes, FAQ section, news and events updates. Go to www.ti.com/lprf.

8.5 Low-Power RF Online Community

- Forums, videos, and blogs
- RF design help
- E2E interaction

Join at: www.ti.com/lprf-forum.

8.6 Texas Instruments Low-Power RF Developer Network

Texas Instruments has launched an extensive network of low-power RF development partners to help customers speed up their application development. The network consists of recommended companies, RF consultants, and independent design houses that provide a series of hardware module products and design services, including:

- RF circuit, low-power RF, and ZigBee design services
- Low-power RF and ZigBee module solutions and development tools
- RF certification services and RF circuit manufacturing

For help with modules, engineering services or development tools:

Search the [Low-Power RF Developer Network](#) to find a suitable partner. www.ti.com/lprfnetwork

8.7 Low-Power RF eNewsletter

The Low-Power RF eNewsletter is up-to-date on new products, news releases, developers' news, and other news and events associated with low-power RF products from TI. The Low-Power RF eNewsletter articles include links to get more online information.

Sign up at: www.ti.com/lprfnewsletter

8.8 Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. The selection includes RF transceivers, RF transmitters, RF front ends, and Systems-on-Chips as well as various software solutions for the sub-1-GHz and 2.4-GHz frequency bands.

In addition, Texas Instruments provides a large selection of support collateral such as development tools, technical documentation, reference designs, application expertise, customer support, third-party and university programs.

The Low-Power RF E2E Online Community provides technical support forums, videos and blogs, and the chance to interact with engineers from all over the world.

With a broad selection of product solutions, end-application possibilities, and a range of technical support, Texas Instruments offers the broadest low-power RF portfolio.

8.9 Trademarks

SimpleLink, SmartRF, Code Composer Studio, E2E are trademarks of Texas Instruments.

ARM7 is a trademark of ARM Limited (or its subsidiaries).

ARM, Cortex, ARM Thumb are registered trademarks of ARM Limited (or its subsidiaries).

CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.

IAR Embedded Workbench is a registered trademark of IAR Systems AB.

IEEE Std 1241 is a trademark of Institute of Electrical and Electronics Engineers, Incorporated.

ZigBee is a registered trademark of ZigBee Alliance, Inc.

8.10 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.11 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.12 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical Packaging and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2630F128RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2630 F128	Samples
CC2630F128RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2630 F128	Samples
CC2630F128RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2630 F128	Samples
CC2630F128RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2630 F128	Samples
CC2630F128RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2630 F128	Samples
CC2630F128RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC2630 F128	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2630F128RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC2630F128RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC2630F128RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC2630F128RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC2630F128RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC2630F128RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

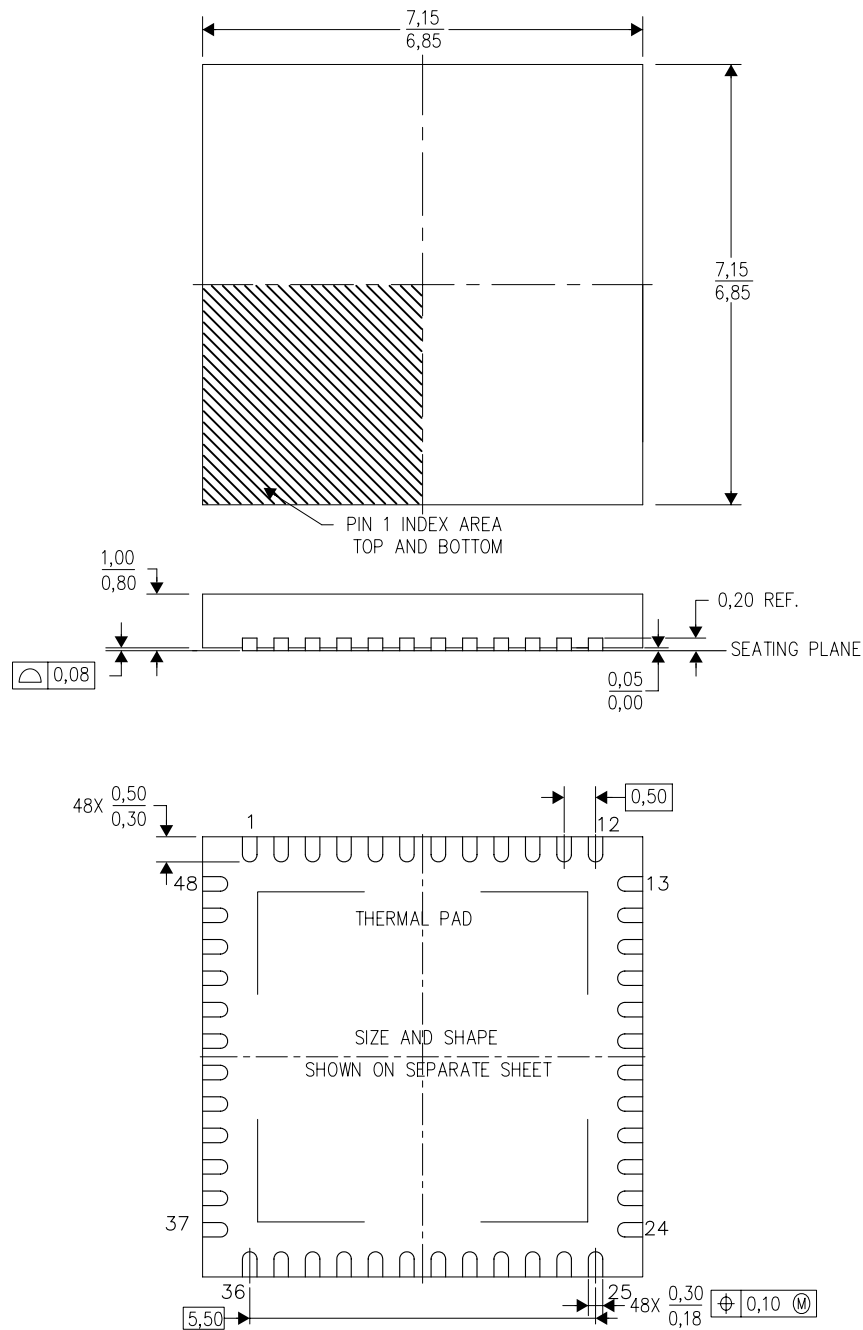


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2630F128RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC2630F128RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC2630F128RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC2630F128RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC2630F128RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
CC2630F128RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

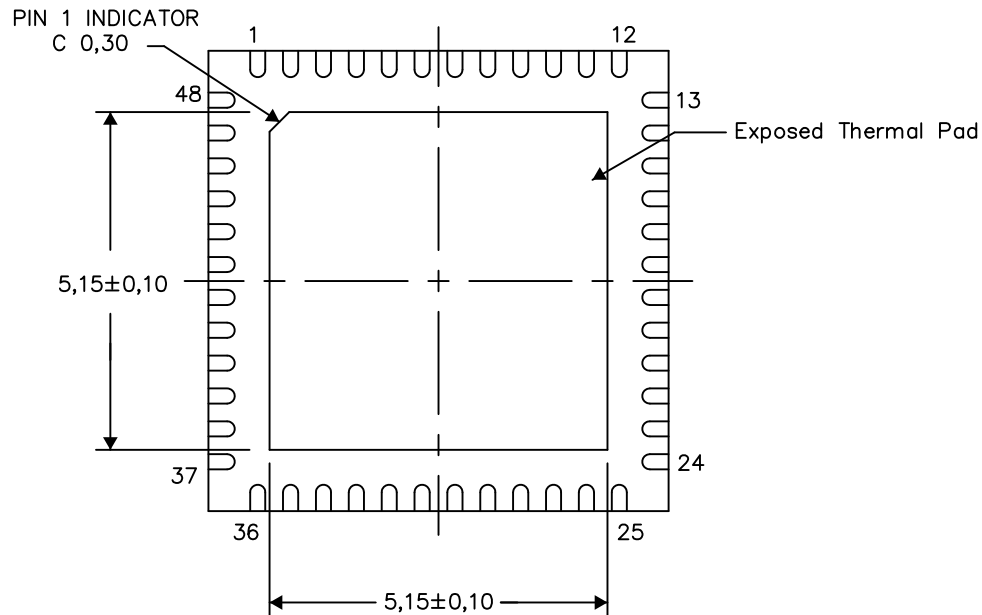
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

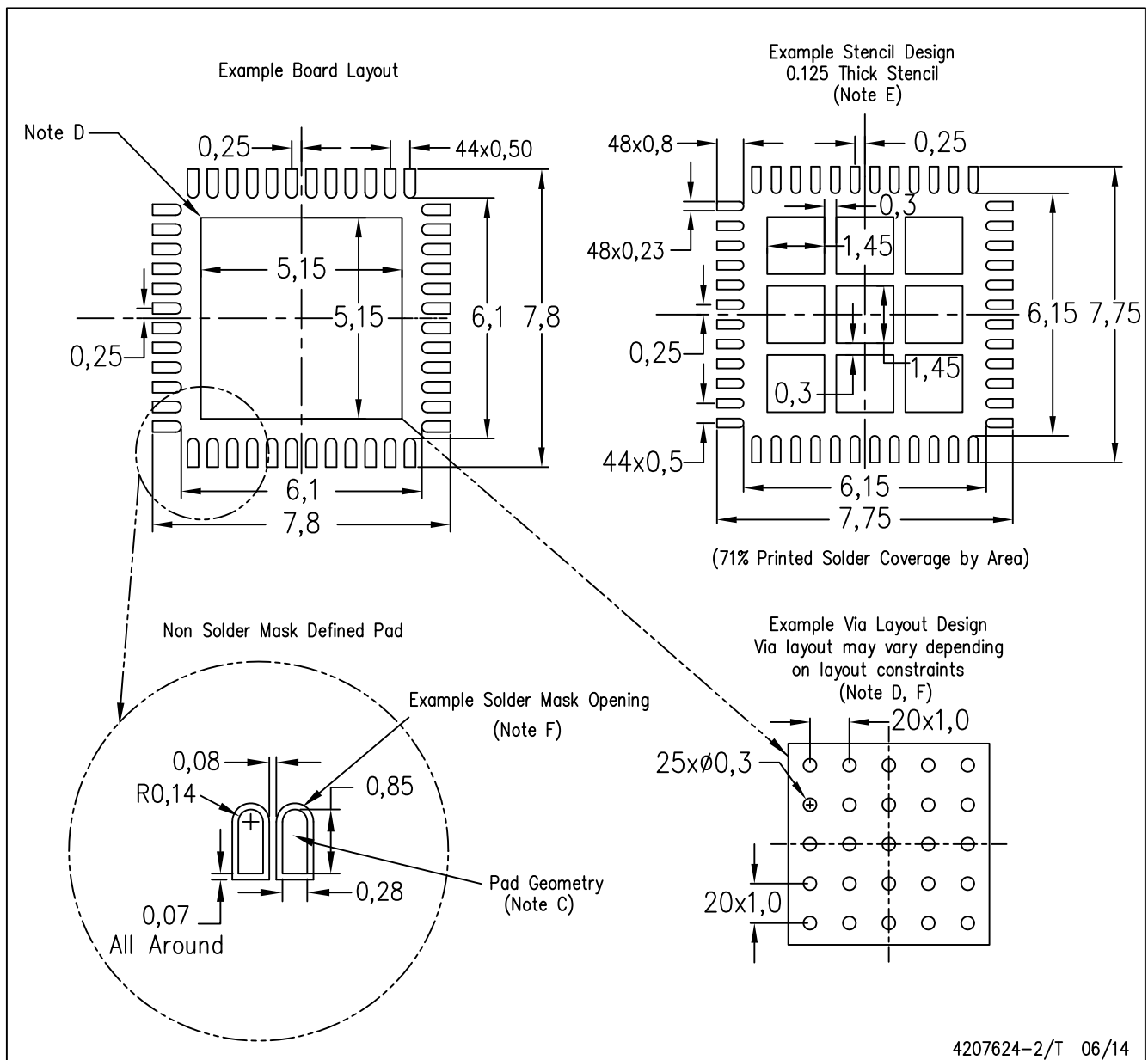
Exposed Thermal Pad Dimensions

4206354-2/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48)

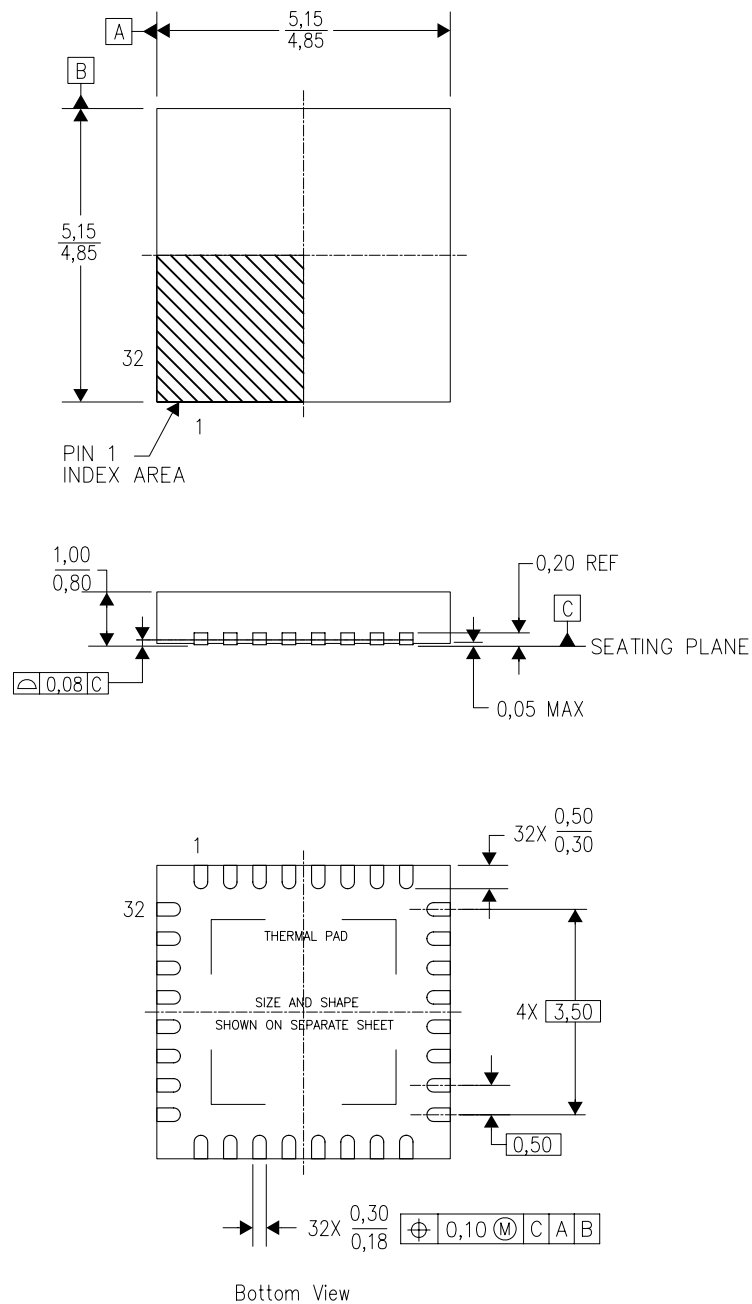
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD

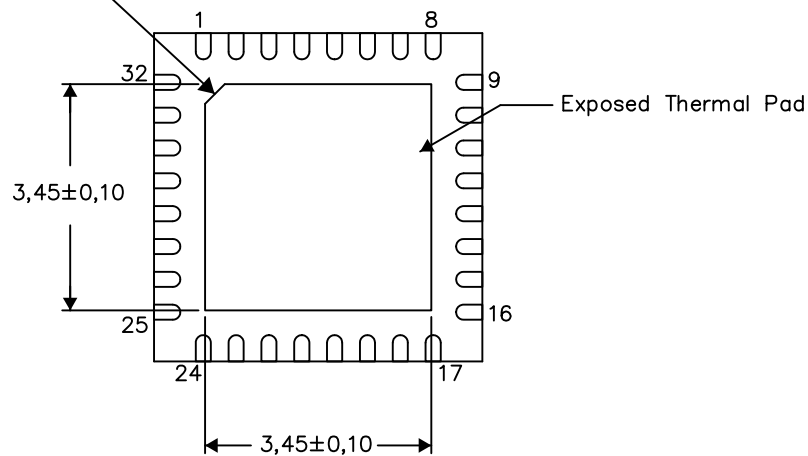
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
(OPTIONAL)



Bottom View

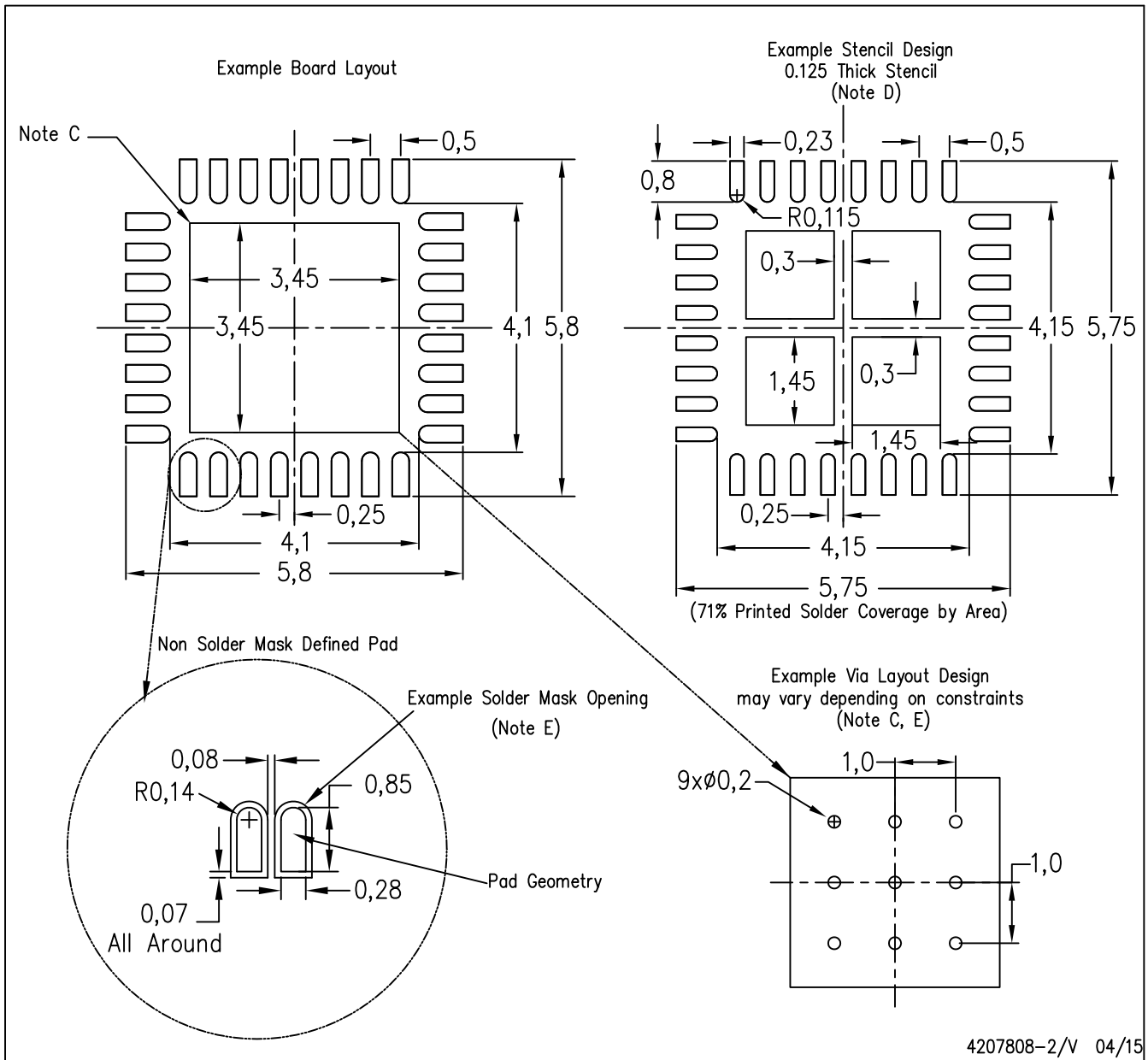
Exposed Thermal Pad Dimensions

4206356-2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

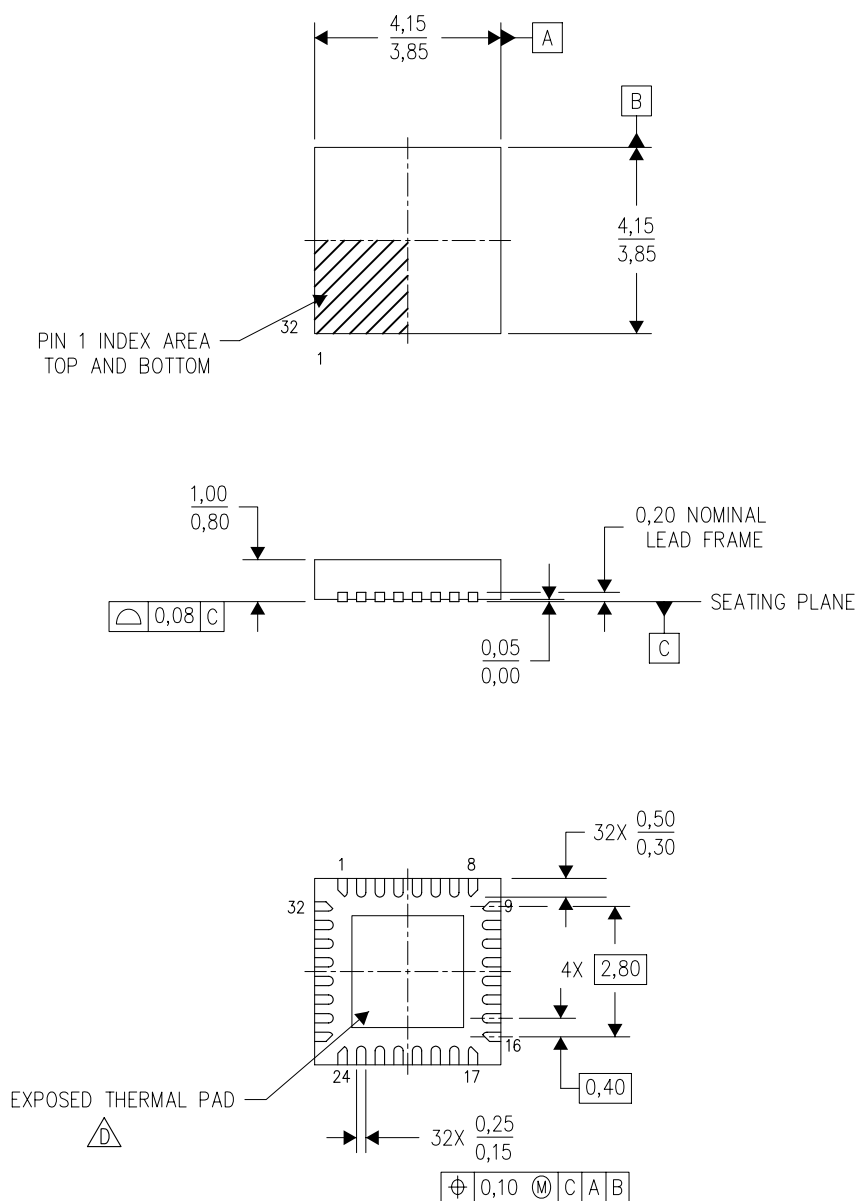
PLASTIC QUAD FLATPACK NO-LEAD




- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207560/B 03/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
-  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

RSM (S-PVQFN-N32)

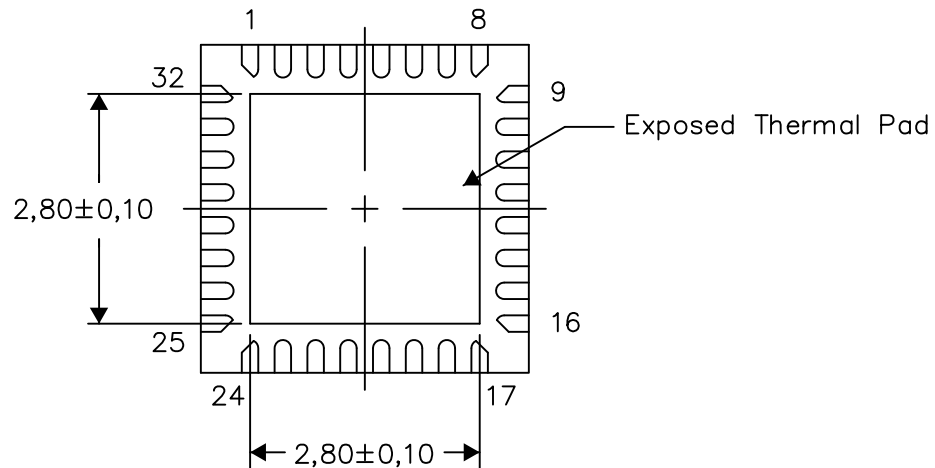
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

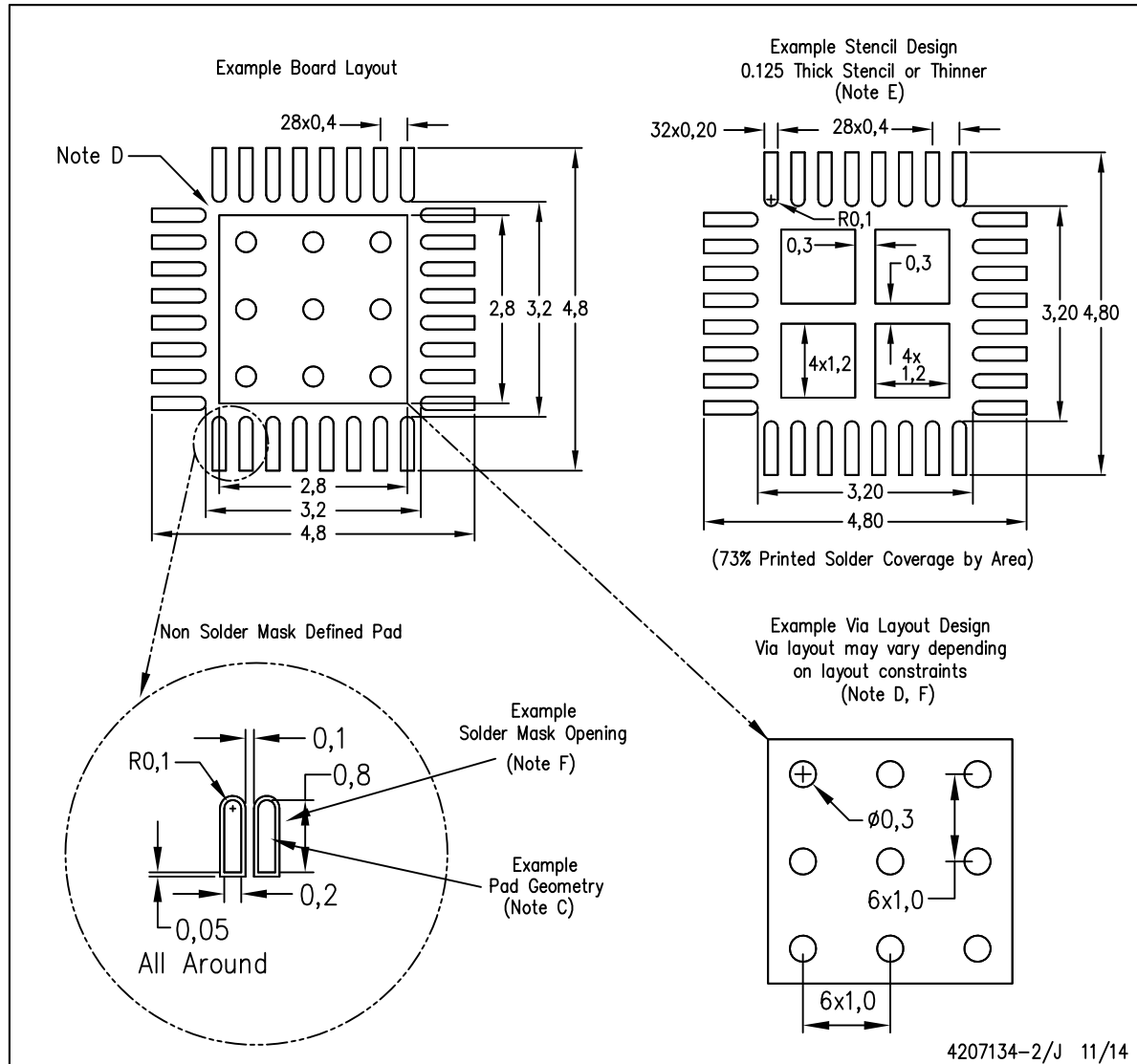
Exposed Thermal Pad Dimensions

4207868-2/1 07/14

NOTE: All linear dimensions are in millimeters

RSM (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



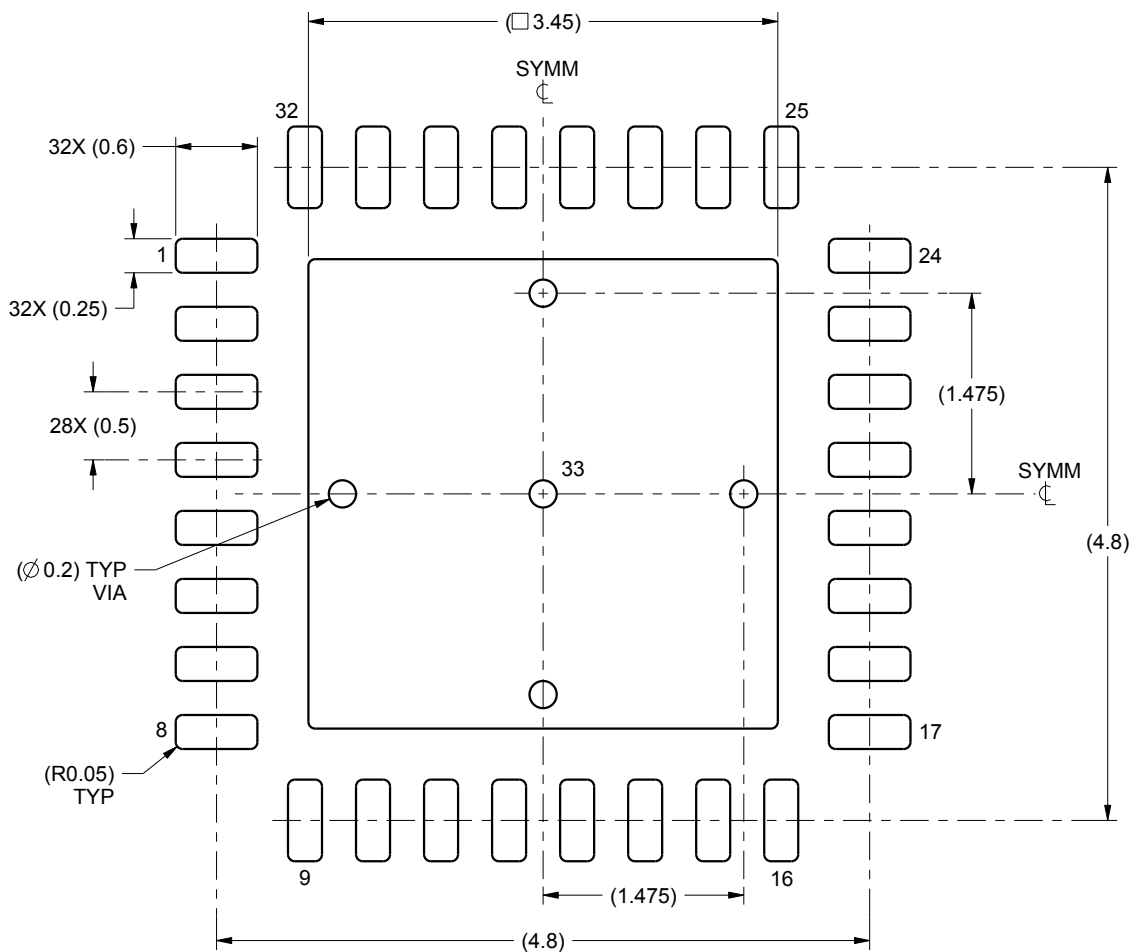
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

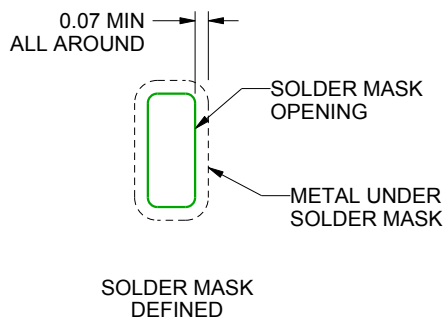
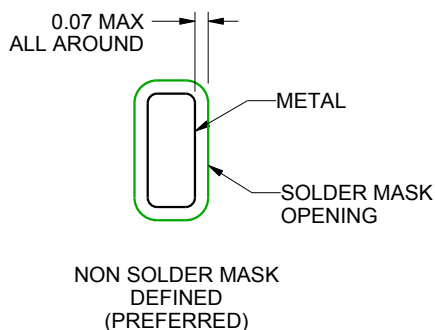
RHB0032N

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4222893/A 04/2016

NOTES: (continued)

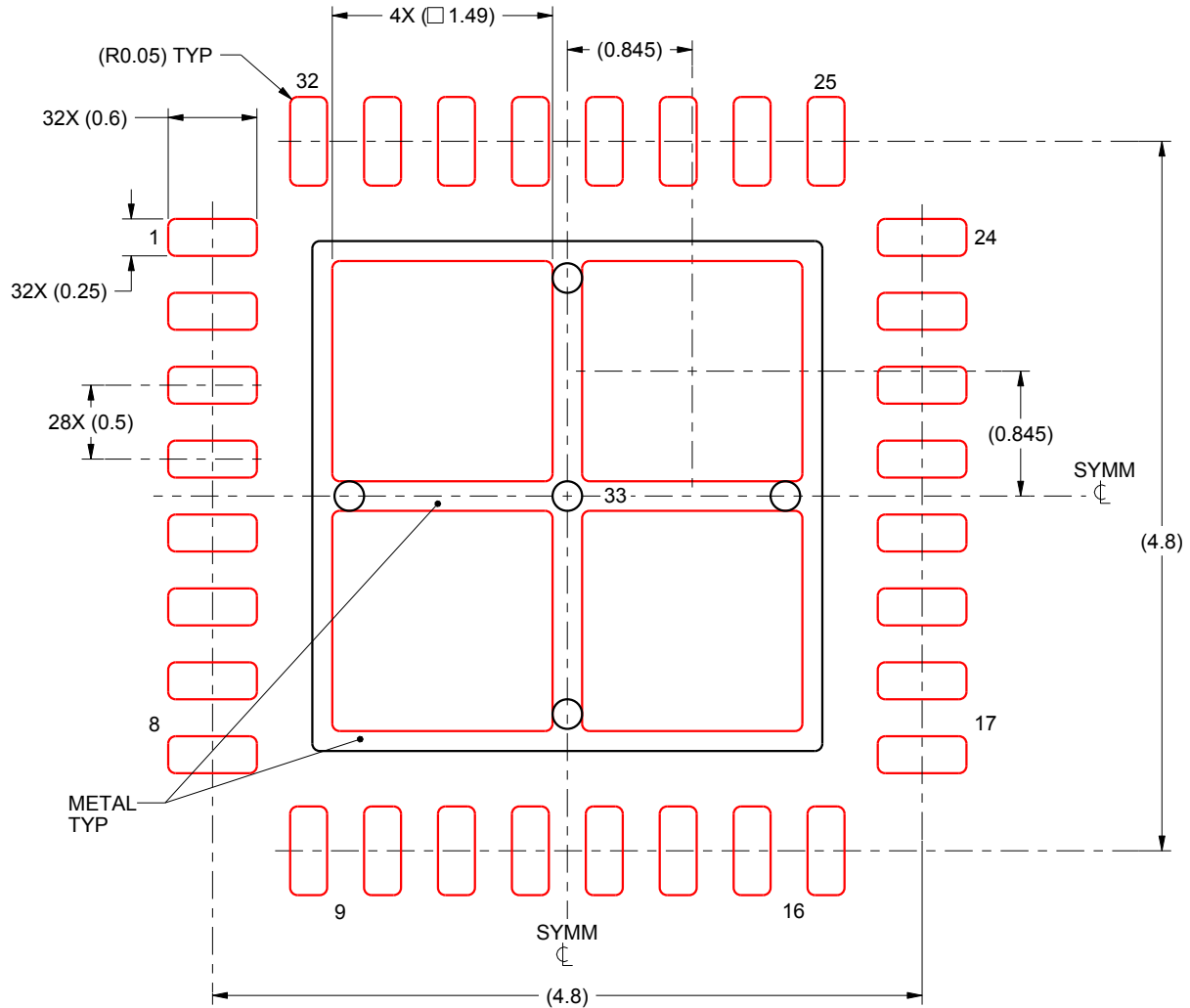
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032N

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222893/A 04/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD

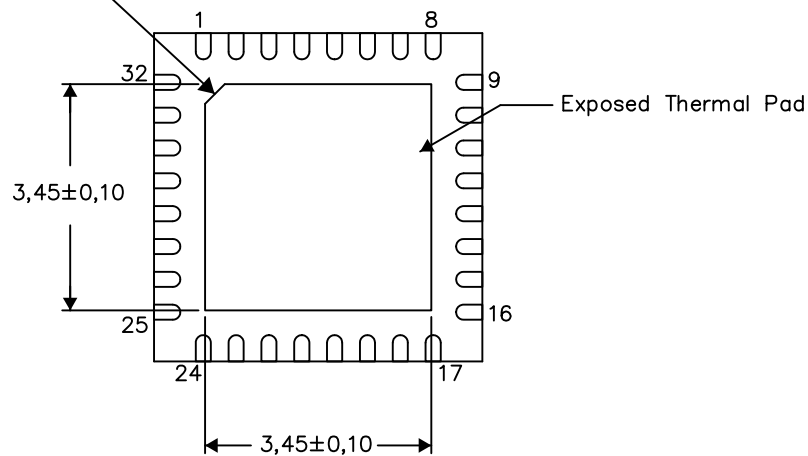
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
(OPTIONAL)



Bottom View

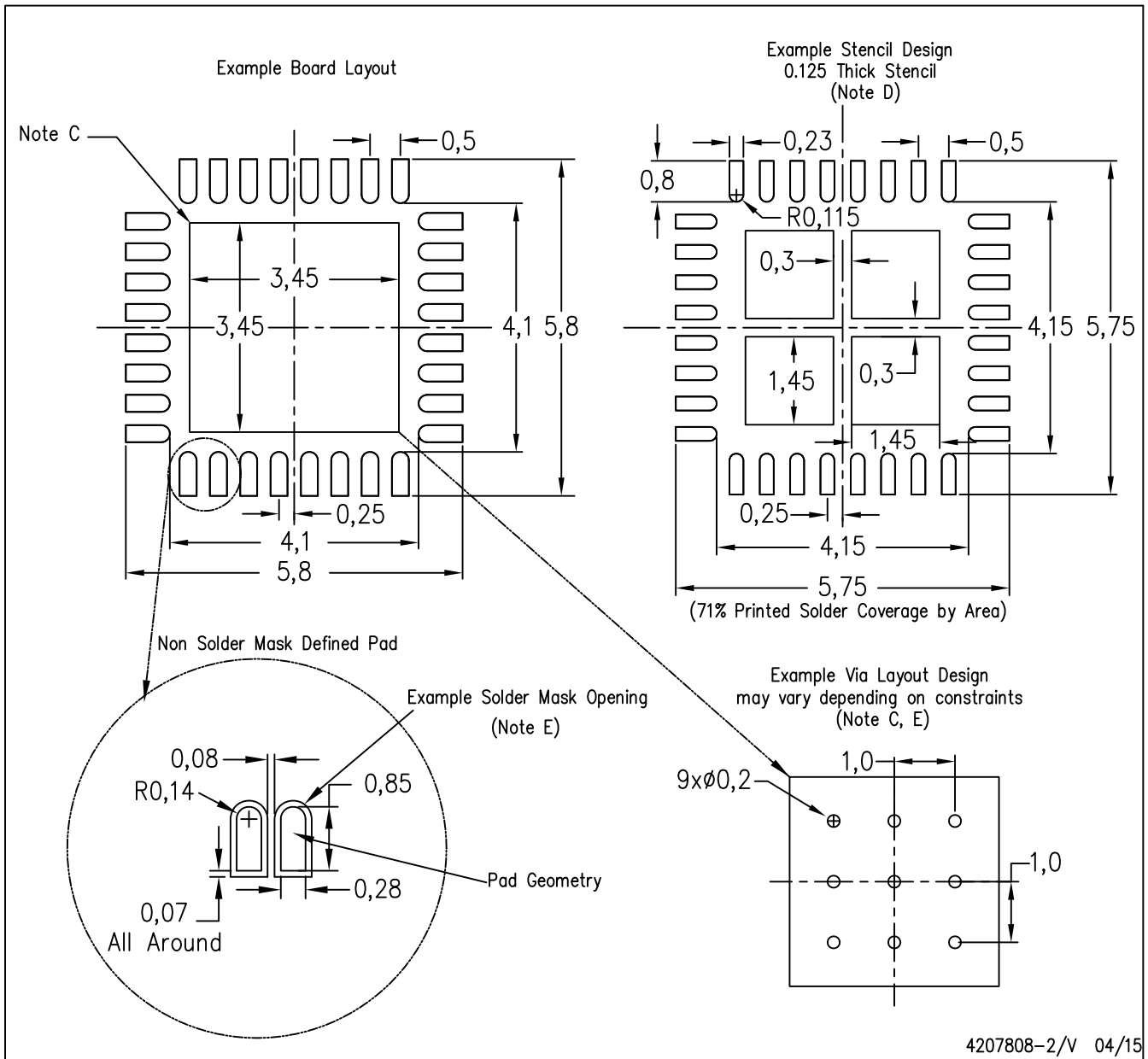
Exposed Thermal Pad Dimensions

4206356-2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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