190 PES Only

004773

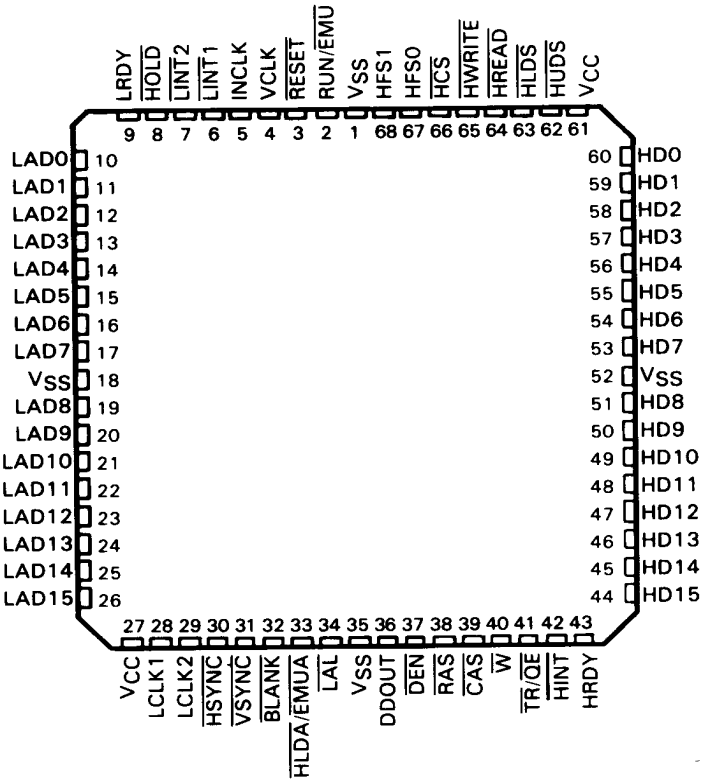
946 TI

TMS34010
GRAPHICS SYSTEM PROCESSOR

JANUARY 1986 – REVISED JULY 1987

- **Instruction Cycle Time:**
  - **160 ns . . . (TMS34010-50)**
  - **200 ns . . . (TMS34010-40)**
- **Fully Programmable 32-Bit General-Purpose Processor with 128-Megabyte Address Range**
- **Pixel Processing, XY Addressing, and Window Checking Built into the Instruction Set**
- **Programmable 1, 2, 4, 8, or 16-Bit Pixel Size with 16 Boolean and 6 Arithmetic Pixel Processing Options (Raster-Ops)**
- **30 General-Purpose 32-bit Registers and 32-bit Stack Pointer**
- **256-Byte LRU On-Chip Instruction Cache**
- **Direct Interfacing to Both Conventional DRAM and Multiport Video RAM**
- **Dedicated 8/16-Bit Host Processor Interface and HOLD/HLDA Interface**
- **Programmable CRT Control ($\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$)**
- **High-Level Language Support**
- **Full Line of Hardware and Software Development Tools Including a "C" Compiler**
- **68-Leaded Packaging (PLCC)**
- **5-Volt CMOS Technology**

FN PACKAGE
(TOP VIEW)



description

The TMS34010 Graphics System Processor (GSP) is an advanced high-performance CMOS 32-bit microprocessor optimized for graphics display systems. With a built-in instruction cache, the ability to simultaneously access memory and registers, and an instruction set designed specifically for raster graphics operation, the TMS34010 provides user-programmable control of the CRT interface as well as the memory interface (both standard DRAM and multiport video RAM). The 1-gigabit address space is completely bit-addressable on bit boundaries using variable width data fields (1 to 32 bits). Additional graphics addressing modes support 1, 2, 4, 8, and 16-bit wide pixels. The TMS34010 is exceptionally well-supported by graphics software interface standards such as CGI/VDI, DGIS, and MS-Windows, as well as a full line of hardware and software support tools.

architecture

The TMS34010 is a CMOS 32-bit processor with hardware support for graphics operations such as PixBlts (raster ops) and curve-drawing algorithms. Also included is a complete set of general-purpose instructions with addressing tuned to support high-level languages. In addition to its ability to address a large external memory range, the TMS34010 contains 30 general-purpose 32-bit registers, a hardware stack pointer and a 256-byte instruction cache. On-chip functions include 28 programmable I/O registers that contain CRT control, input/output control, and instruction parameters. The TMS34010 directly interfaces to dynamic

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

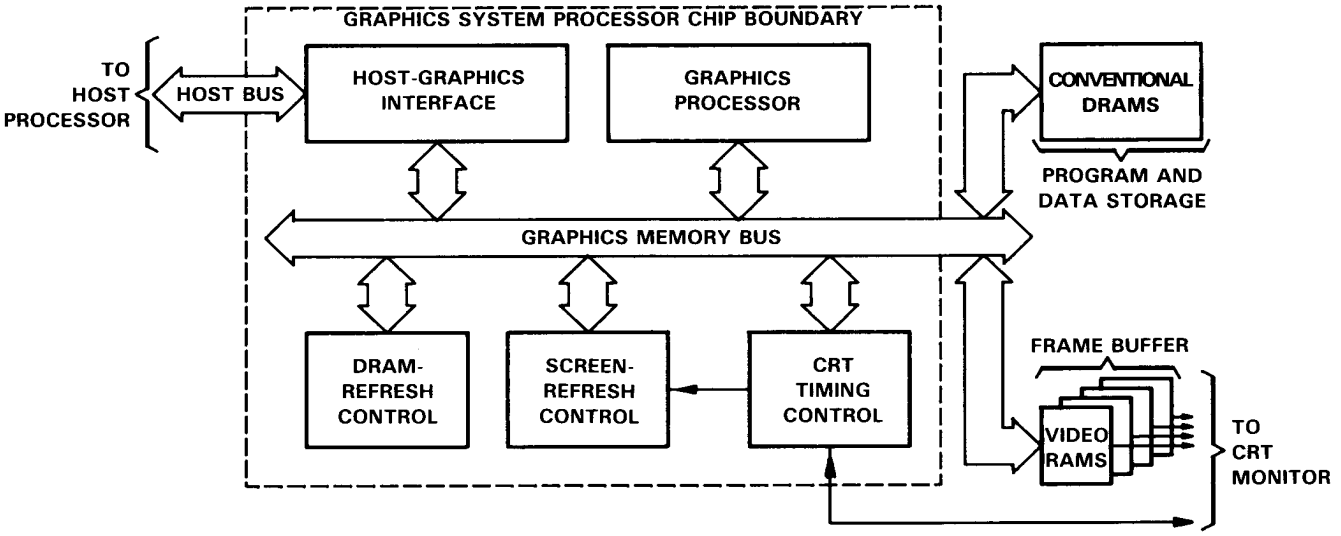
RAMs and video RAMs and generates video monitor control signals. It also accommodates a conventional HOLD/HLDA shared access as well as a separate, generalized interface for communicating with any standard host processor.

pin descriptions

PIN NAME	PIN NO.	I/O	DESCRIPTION
			Host Interface Bus Pins
$\overline{HCS}$	66	I	Host chip select
HD0-HD15	44-51, 53-60	I/O	Host bidirectional data bus
HFS0, HFS1	67, 68	I	Host function select
$\overline{HINT}$	42	O	Host interrupt request
$\overline{HLDS}$	63	I	Host lower data select
$\overline{HUDS}$	62	I	Host upper data select
HRDY	43	O	Host ready
$\overline{HREAD}$	64	I	Host read strobe
$\overline{HWRITE}$	65	I	Host write strobe
			Local Bus Interface Pins
$\overline{RAS}$	38	O	Local row-address strobe
$\overline{CAS}$	39	O	Local column-address strobe
DDOUT	36	O	Local data direction out
$\overline{DEN}$	37	O	Local data enable
LAD0-LAD15	10-17, 19-26	I/O	Local address/data bus
$\overline{LAL}$	34	O	Local address latched
LCLK1, LCLK2	28, 29	O	Local output clocks
$\overline{LINT1}$, $\overline{LINT2}$	6, 7	I	Local interrupt request pins
LRDY	9	I	Local ready
$\overline{TR/QE}$	41	O	Local shift register transfer or output enable
$\overline{W}$	40	O	Local write strobe
INCLK	5	I	Input clock
			Hold and Emulation
$\overline{HOLD}$	8	I	Hold request
RUN/$\overline{EMU}$	2	I	Run/Not emulate
$\overline{HLDA/EMUA}$	33	O	Hold acknowledge or emulate acknowledge
			Video Timing Signals
$\overline{BLANK}$	32	O	Blanking
$\overline{HSYNC}$	30	I/O	Horizontal sync
VCLK	4	I	Video clock
$\overline{VSYNC}$	31	I/O	Vertical sync
			Miscellaneous
$\overline{RESET}$	3	I	Reset
V_{CC}	27, 61	I	Nominal 5-volt power supply
V_{SS}	1, 18, 35, 52	I	Ground

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

system block diagram



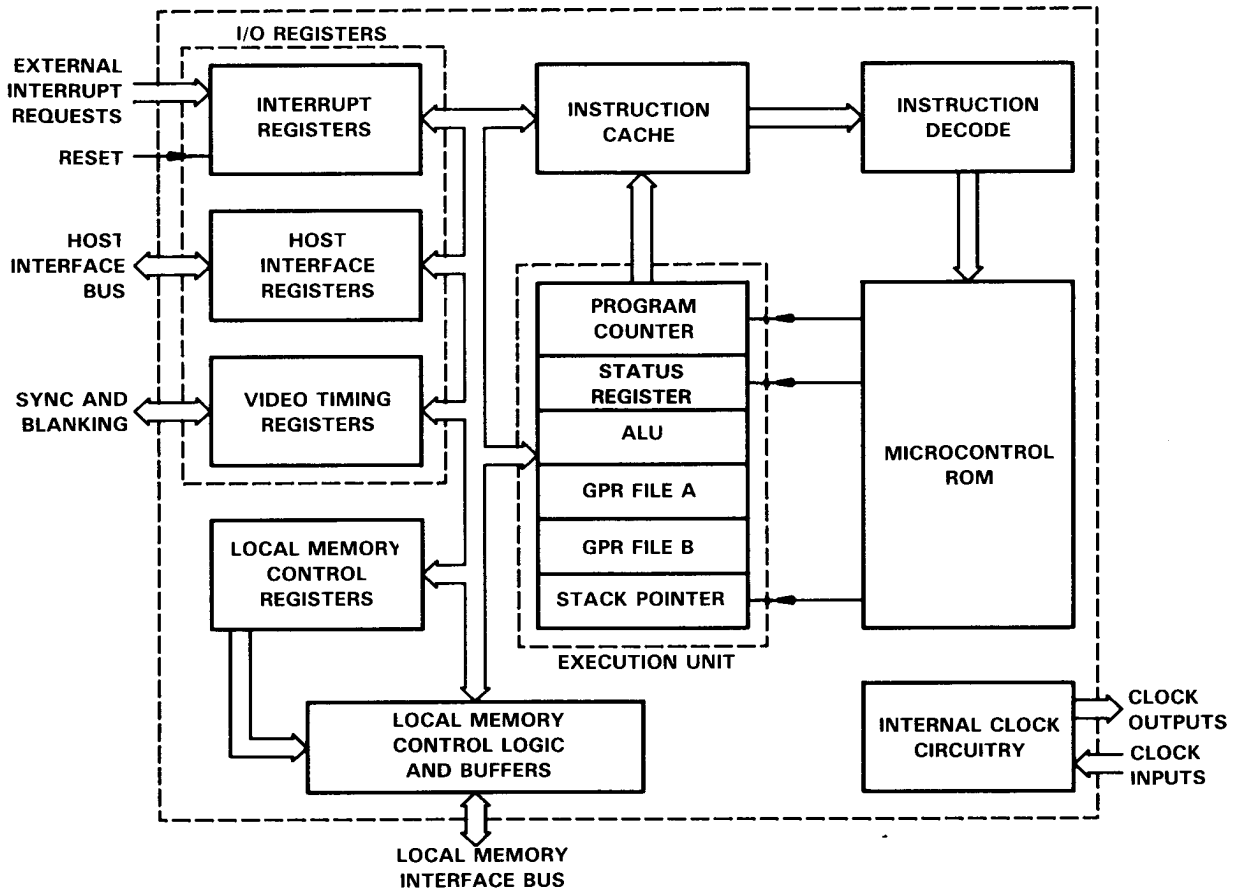


FIGURE 1. TMS34010 INTERNAL ARCHITECTURE

The TMS34010 provides single-cycle execution of most common integer arithmetic and Boolean operations from its instruction cache. Additionally, the TMS34010 incorporates a hardware barrel shifter that provides a single-state bidirectional shift and rotate function for 1 to 32 bits.

A microcoded local memory controller supports pipelined memory write operations of variable-size fields that can be performed in parallel with subsequent instruction execution.

TMS34010 graphics processing hardware supports pixel and pixel-array processing capabilities for both monochrome and color systems that have a variety of pixel sizes. The hardware incorporates two-operand raster operations with Boolean and arithmetic operations, XY addressing, window clipping, window checking operations, 1 to n bits per pixel transforms, transparency, and plane masking. The architecture further supports operations on single pixels (PIXT instructions) or on two-dimensional pixel arrays of arbitrary size (PixBlts).

The TMS34010's flexible graphics processing capabilities allow software-based graphics algorithms without sacrificing performance. These algorithms include: arbitrary window size, custom incremental curve drawing, and two-operand raster operations.

register files

Boolean, arithmetic, byte, and field move instructions operate on data within the GSP's general-purpose register files. The TMS34010 contains thirty-one 32-bit registers, including a system stack pointer (SP). The SP is accessible to both Register File A and B as the sixteenth register. Transfers between registers and memory are facilitated via a complete set of field MOVE instructions with selectable field sizes. Transfers between registers are facilitated via the MOVE instruction.

The fifteen general-purpose registers in Register File A are used for high-level language support and assembly language programming. The fifteen registers in Register File B are dedicated to special functions during PixBlts and other pixel operations, but can be used as general-purpose registers at other times.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

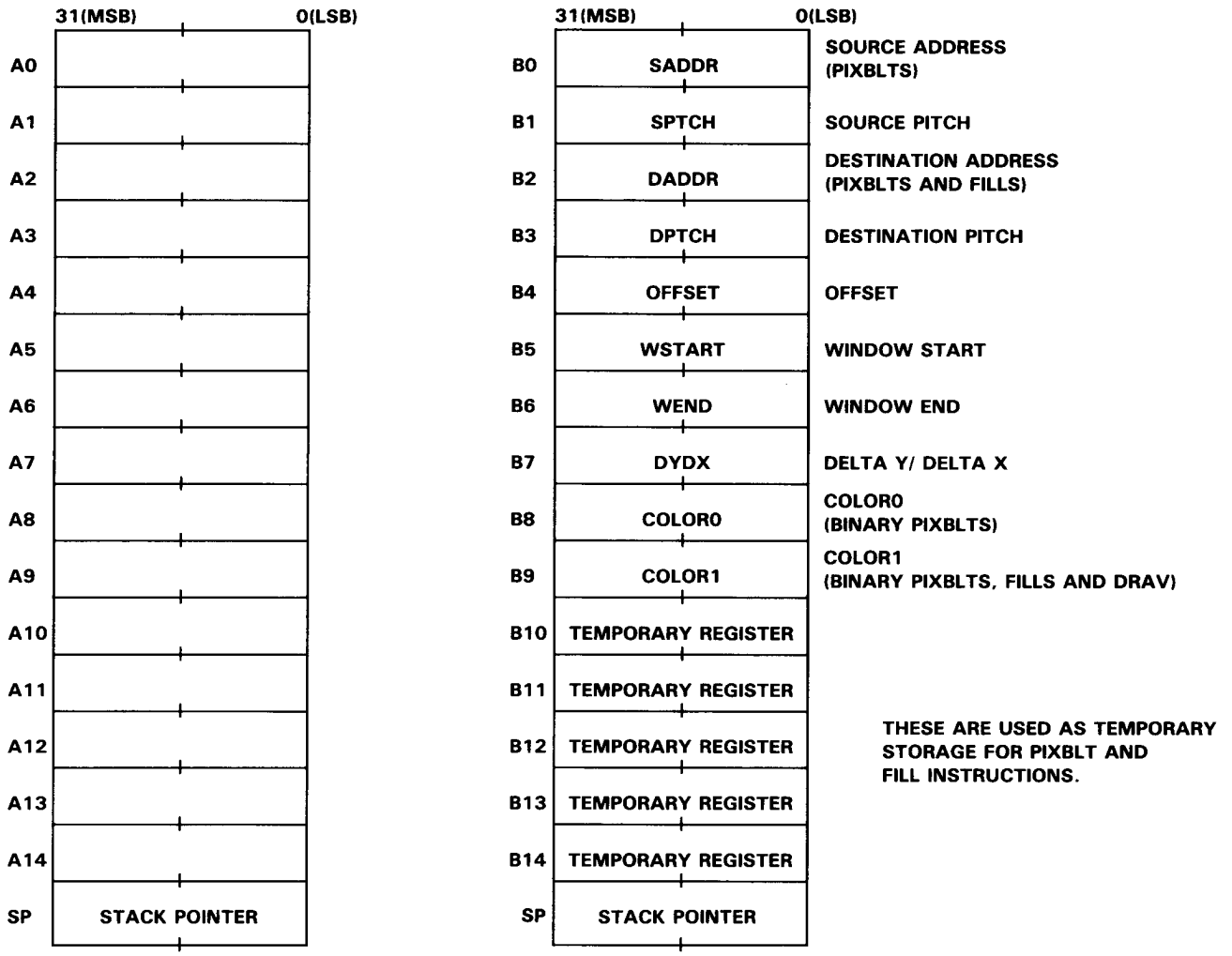


FIGURE 2. REGISTER FILES A AND B

program counter (PC)

The TMS34010's 32-bit program counter register points to the next instruction-stream word to be fetched. Since instruction words are aligned to 16-bit boundaries, the four LSBs of the PC are always zero.

instruction cache

An on-chip instruction cache contains 256 bytes of RAM and provides fast access to instructions. It operates automatically and is transparent to software. The cache is divided into four 64-byte segments. Associated with each segment is a 23-bit segment address register to identify the addresses in memory corresponding to the current contents of the cache segment. Each cache segment is further partitioned into eight subsegments of four words each. Each subsegment has associated with it a present flag to indicate whether the subsegment contains valid data.

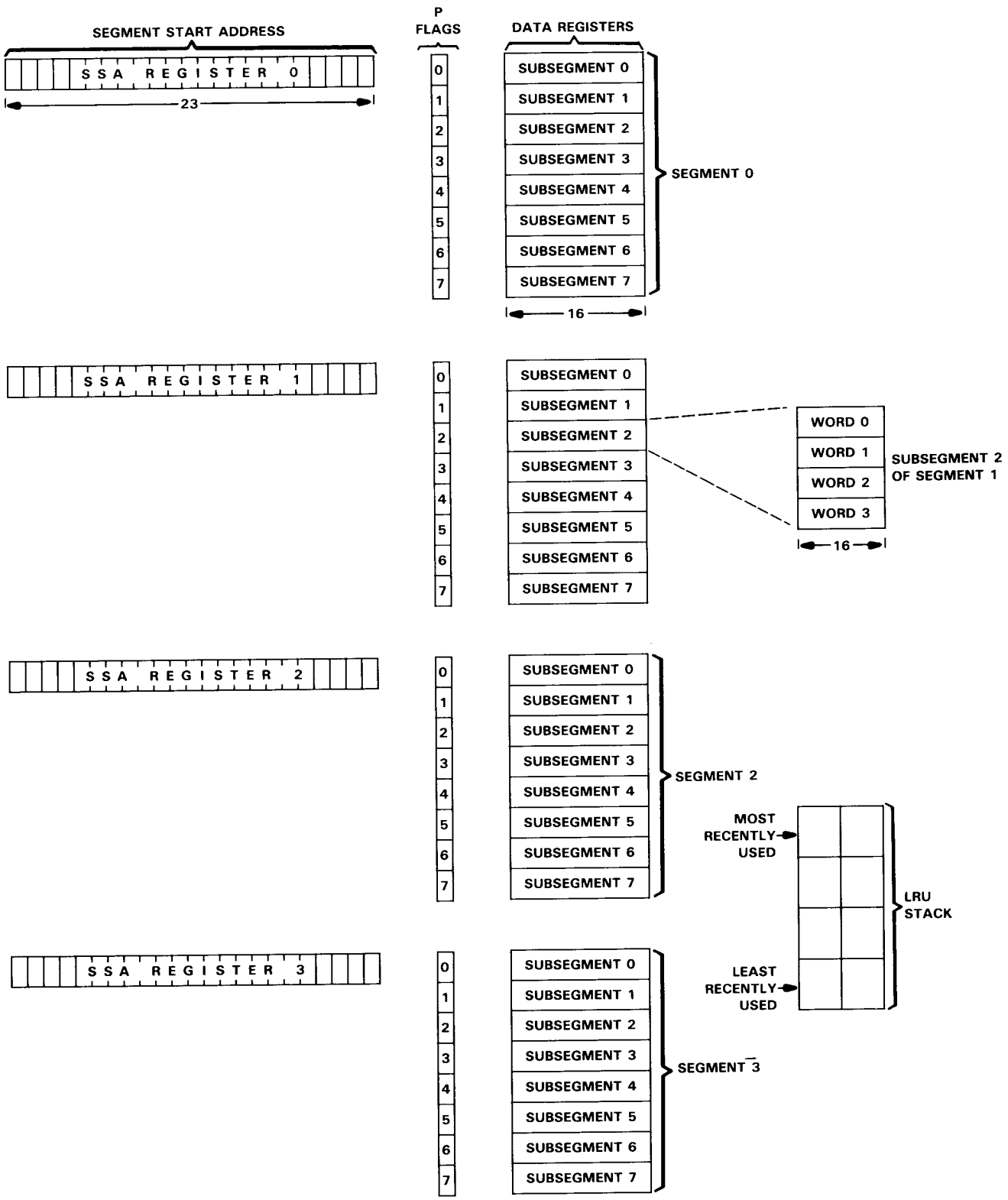


FIGURE 3. INSTRUCTION CACHE

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

The cache is loaded only when an instruction requested by the TMS34010 is not already contained within the cache. A least-recently-used (LRU) algorithm is used to determine which of the four segments of the cache is overwritten with the new data. For this purpose, an internal four-by-two LRU stack is used to keep track of cache usage.

status register

The status register (ST) is a special-purpose 32-bit register dedicated to status codes set by the results of implicit and explicit compare operations and parameters used to specify the length and behavior of fields 0 and 1.

N - Sign bit
C - Carry bit
Z - Zero bit
V - Overflow bit
PBX - PixBlt executing
IE - Interrupt enable bit
FE1 - Field extension bit 1
FS1 - Field size bit 1
FE0 - Field extension bit 0
FS0 - Field size bit 0

FIGURE 4. STATUS REGISTER

fields, bytes, pixels, and pixel arrays

A 26-bit address output by the TMS34010 selects a 16-bit word of physical memory; logically, however, the TMS34010 views memory data as fields addressable at the bit level. Primitive data types supported by the TMS34010 include: bytes, pixels, two 1- to 32-bit fields, and user-defined pixel arrays.

Fields 0 and 1 are specified independently to be from 1 to 32 bits in length. Bytes are special 8-bit cases of the field data type, while pixels are 1, 2, 4, 8 or 16 bits in length. In general, fields (including bytes) may start and terminate on arbitrary bit boundaries; pixels must pack evenly into 16-bit words.

pixel operations

Pixel arrays are two-dimensional data types of user-defined width, height, pixel depth (number of bits per pixel), and pitch (distance between rows). A pixel or pixel array may be accessed by means of either its memory address or its XY coordinates. Transfers of individual pixels or pixel blocks are influenced by the pixel processing, transparency, window checking, plane masking, or corner adjust operations selected.

I/O registers

The GSP contains an on-chip block of twenty-eight 16-bit I/O registers mapped into the TMS34010's memory address space. They can be accessed either by the TMS34010's CPU or by the host processor via the host interface. The I/O registers contain control parameters necessary to configure the operation of the following interfaces: interface to host processor (5 I/O registers), interface to local memory (6 registers), video timing and screen refresh functions (15 registers), and externally and internally generated interrupts (2 registers). The I/O registers also furnish status information on these interfaces.

ADDRESS	REGISTER	
>C000 01F0	REFCNT	DRAM REFRESH COUNT
>C000 01E0	DPYADR	DISPLAY ADDRESS
>C000 01D0	VCOUNT	VERTICAL COUNT
>C000 01C0	HCOUNT	HORIZONTAL COUNT
>C000 01B0	DPYTAP	DISPLAY TAP POINT
>C000 01A0	RESERVED	
>C000 0190		
>C000 0180		
>C000 0170		
>C000 0160	PMASK	PLANE MASK
>C000 0150	PSIZE	PIXEL SIZE
>C000 0140	CONVDP	CONVERSION (DESTINATION PITCH)
>C000 0130	CONVSP	CONVERSION (SOURCE PITCH)
>C000 0120	INTPEND	INTERRUPT PENDING
>C000 0110	INTENB	INTERRUPT ENABLE
>C000 0100	HSTCTLH	HOST CONTROL (8 MSB'S)
>C000 00F0	HSTCTLL	HOST CONTROL (8 LSB'S)
>C000 00E0	HSTADRH	HOST ADDRESS (16 MSB'S)
>C000 00D0	HSTADRL	HOST ADDRESS (16 LSB'S)
>C000 00C0	HSTDATA	HOST DATA
>C000 00B0	CONTROL	CONTROL
>C000 00A0	DPYINT	DISPLAY INTERRUPT
>C000 0090	DPYSTRT	DISPLAY START
>C000 0080	DPYCTL	DISPLAY CONTROL
>C000 0070	VTOTAL	VIDEO TOTAL
>C000 0060	VSBLNK	VERTICAL START BLANK
>C000 0050	VEBLNK	VERTICAL END BLANK
>C000 0040	VESYNC	VERTICAL END SYNC
>C000 0030	HTOTAL	HORIZONTAL TOTAL
>C000 0020	HSBLNK	HORIZONTAL START BLANK
>C000 0010	HEBLNK	HORIZONTAL END BLANK
>C000 0000	HESYNC	HORIZONTAL END SYNC

FIGURE 5. I/O REGISTERS

host interface registers

The host interface registers are provided for communications between the TMS34010 and the host processor. The registers are mapped into five of the I/O register locations accessible to the TMS34010. These same registers are mapped into four locations in the GSP interface to the host.

One of the registers is devoted to host interface control functions such as the passing of interrupt requests and 3-bit status codes from host to TMS34010 and from TMS34010 to host. Other control functions available to the host processor include flushing the instruction cache, halting the TMS34010, and transmitting a non-maskable interrupt request to the TMS34010.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

The remaining host registers are used for block transfers between the TMS34010 and host processor. The host uses these registers to indirectly access blocks within the TMS34010's local memory. Two of the 16-bit registers contain the 32-bit address of the current word location in memory. Another 16-bit register buffers data transferred to and from the memory by the host processor. The host interface can be programmed to automatically increment the pointer address following each transfer to provide the host with rapid access to a block of sequential addresses.

memory interface control registers

Six of the I/O registers are dedicated to various local memory interface functions including:

- Frequency and type of DRAM refresh cycles
- Pixel size
- Masking (write protection) of individual color planes
- Various pixel access control parameters
  - Window checking mode
  - Boolean or arithmetic pixel processing operation
  - Transparency
  - PixBlt direction control

video timing and screen refresh

Fourteen I/O registers are dedicated to video timing and screen refresh functions. The TMS34010 generates the horizontal sync ($\overline{\text{HSYNC}}$), vertical sync ($\overline{\text{VSYNC}}$), and blanking ($\overline{\text{BLANK}}$) signals used to drive a video monitor in a graphics system. These signals are controlled by means of a set of programmable video timing I/O registers and are based on the input video clock, VCLK. VCLK does not have to be synchronous with respect to INCLK, the TMS34010's CPU input clock.

The TMS34010 directly supports multiport video RAMs (VRAMs) by generating the shift-register-load cycles necessary to refresh the display being shown on the video monitor. The memory locations from which display information is taken, as well as the number of horizontal scan lines displayed between shift-register-load cycles, are programmable. VRAM tap point addresses are also fully programmable to support horizontal panning.

The TMS34010 supports various screen resolutions and either interlaced or noninterlaced video. The TMS34010 can optionally be programmed to synchronize to externally generated sync signals so that graphics images created by the TMS34010 can be superimposed upon images created externally. The external sync mode can also be used to synchronize the video signals generated by two or more TMS34010 chips in a multiple-TMS34010 graphics system.

interrupt interface registers

Two dedicated I/O registers monitor and mask interrupt requests to the TMS34010, including two externally generated interrupts and three internally generated interrupts. An internal interrupt request can be generated on one of the following conditions:

- Window violation: an attempt has been made to write a pixel to a location inside or outside a specified window boundary.
- Host interrupt: the host processor has set the interrupt request bit in the host control register.
- Display interrupt: a specified line number in the frame has been displayed on the screen.

A nonmaskable interrupt occurs when the host processor sets a particular control bit in the host interface registers. The TMS34010 reset function is controlled by a dedicated pin.

memory controller/local memory interface

The memory controller manages the TMS34010's interface to the local memory and automatically performs the bit alignment and masking necessary to access data located at arbitrary bit boundaries within memory. The memory controller operates autonomously with respect to the CPU. It has a ''write queue'' one field (1 to 32 bits) deep that permits it to complete the memory cycles necessary to insert the field into memory without delaying the execution of subsequent instructions. Only when a second memory operation is required before the memory controller has completed the first operation is the TMS34010 forced to defer instruction execution.

The TMS34010 directly interfaces to all standard dynamic RAMs and, in particular to JEDEC standard 64K and 256K video RAMs such as the TMS4161 and TMS4461 Multiport VRAMs. The TMS34010 memory interface consists of a triple-multiplexed address/data bus plus the associated control signals. Row address, column address, and data are multiplexed over the same address/data lines. DRAM refresh is supported with a variety of modes including $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh.

TMS34010 memory map

From the programmer's point of view, the TMS34010 treats data and instructions as residing in the same memory space.

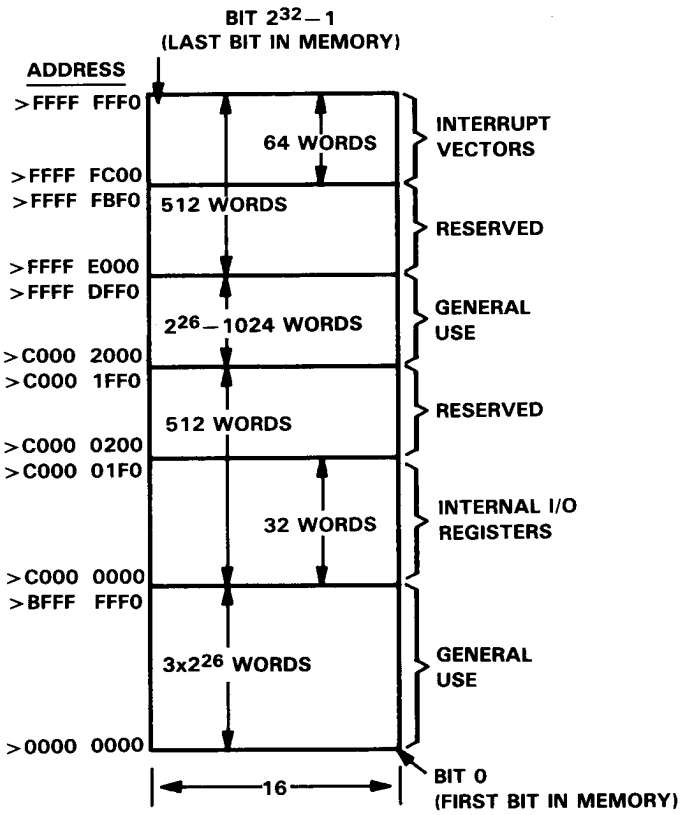


FIGURE 6. MEMORY MAP

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

instruction set

The TMS34010 instructions fall into three categories. The graphics instructions manipulate pixel data, accessed via memory addresses or XY coordinates. They provide support for graphics operations such as array and raster ops, pixel processing, windowing, plane masking, and transparency. The move instructions comprehend bit addressing and field operations; they manipulate fields of data using linear addressing for transfer to and from memory and the register file. The TMS34010 general-purpose instructions provide a complete set of arithmetic and Boolean operations on the register file as well as general program control and data processing. Partial timing information is provided in the table below. The two values given for jump instructions in the Minimum Cycles column indicate the jump and no-jump conditions, respectively. Full timing information can be obtained in the *TMS34010 User's Guide* (number SPVU001).

The following abbreviations are used below in the opcodes: S (source register), D (destination register), R (register file select), F (field select), K (constant), M (cross A/B file boundary), Z (draw option), code (jump select code), X (don't care), N (trap select and stack adjust), RS (source register), RD (destination register), xxxx (address displacement), IL (64-bit immediate operand), and IW(32-bit immediated operand).

GRAPHICS INSTRUCTIONS

SYNTAX	DESCRIPTION	NO. WORDS	MINIMUM CYCLES	16-BIT OPCODE MSB			LSB	STATUS BITS			
ADDXY RS, RD	Add Registers in XY Mode	1	1	1110	000S	SSSR	DDDD	N	C	Z	V
CMPXY RS, RD	Compare X and Y Halves of Registers	1	3	1110	010S	SSSR	DDDD	N	C	Z	V
CPW RS, RD	Compare Point to Window	1	1	1110	011S	SSSR	DDDD	–	–	–	V
CVXYL RS, RD	Convert XY Address to Linear Address	1	3	1110	100S	SSSR	DDDD	–	–	–	–
DRAV RS, RD	Draw and Advance	1	†	1111	011S	SSSR	DDDD	–	–	–	V
FILL L	Fill Array with Processed Pixels: Linear	1	†	0000	1111	1100	0000	–	–	–	–
FILL XY	Fill Array with Processed Pixels: XY	1	†	0000	1111	1110	0000	–	–	–	V
LINE Z	Line Draw	1	†	1111	1110	Z001	1010	–	–	–	V
MOVX RS, RD	Move X Half of Register	1	1	1110	110S	SSSR	DDDD	–	–	–	–
MOVY RS, RD	Move Y Half of Register	1	1	1110	111S	SSSR	DDDD	–	–	–	–
PIXBLT B,L	Pixel Block Transfer: Binary to Linear	1	†	0000	1111	1000	0000	–	–	–	–
PIXBLT B,XY	Pixel Block Transfer and Expand: Binary to XY	1	†	0000	1111	1010	0000	–	–	–	V
PIXBLT L,L	Pixel Block Transfer: Linear to Linear	1	†	0000	1111	0000	0000	–	–	–	–
PIXBLT L,XY	Pixel Block Transfer: Linear to XY	1	†	0000	1111	0010	0000	–	–	–	V
PIXBLT XY, L	Pixel Block Transfer: XY to Linear	1	†	0000	1111	0100	0000	–	–	–	–
PIXBLT XY,XY	Pixel Block Transfer: XY to XY	1	†	0000	1111	0110	0000	–	–	–	V
PIXT RS,*RD	Pixel Transfer: Register to Indirect	1	†	1111	100S	SSSR	DDDD	–	–	–	–
PIXT RS,*RD.XY	Pixel Transfer: Register to Indirect XY	1	†	1111	000S	SSSR	DDDD	–	–	–	V
PIXT *RS, RD	Pixel Transfer: Indirect to Register	1	4	1111	101S	SSSR	DDDD	–	–	–	–
PIXT *RS,*RD	Pixel Transfer: Indirect to Indirect	1	†	1111	110S	SSSR	DDDD	–	–	–	–
PIXT *RS.XY, RD	Pixel Transfer: Indirect XY to Register	1	6	1111	001S	SSSR	DDDD	–	–	–	–
PIXT *RS.XY,*RD.XY	Pixel Transfer: Indirect XY to Indirect XY	1	†	1111	010S	SSSR	DDDD	–	–	–	V
SUBXY RS,RD	Subtract Registers in XY Mode	1	1	1110	001S	SSSR	DDDD	N	C	Z	V

†Number of cycles depends on pixel size and/or pixel array size and graphics option selected. See TMS34010 User's Guide (SPVU001).

MOVE INSTRUCTIONS

SYNTAX	DESCRIPTION	NO. WORDS	MINIMUM CYCLES	16-BIT OPCODE MSB			LSB	STATUS BITS			
MOVB RS,*RD	Move Byte: Register to Indirect	1	†	1000	110S	SSSR	DDDD	–	–	–	–
MOVB *RS,RD	Move Byte: Indirect to Register	1	†	1000	111S	SSSR	DDDD	N	–	Z	O
MOVB *RS,*RD	Move Byte: Indirect to Indirect	1	†	1001	110S	SSSR	DDDD	–	–	–	–
MOVB RS,*RD(Disp)	Move Byte: Register to Indirect with Disp.	2	†	1010	110S	SSSR	DDDD	–	–	–	–
MOVB *RS(Disp),RD	Move Byte: Indirect with Disp. to Register	2	†	1010	111S	SSSR	DDDD	N	–	Z	O
MOVB *RS(Disp),*RD(Disp)	Move Byte: Ind. with Disp. to Ind. with Disp.	3	†	1011	110S	SSSR	DDDD	–	–	–	–
MOVB RS,@DADDR	Move Byte: Register to Absolute	3	†	0000	0101	111R	SSSS	–	–	–	–
MOVB @SADDR,RD	Move Byte: Absolute to Register	3	†	0000	0111	111R	DDDD	N	–	Z	O
MOVB @SADDR,@DADDR	Move Byte: Absolute to Absolute	5	†	0000	0011	0100	0000	–	–	–	–
MOVE RS,RD	Move Register to Register	1	1	0100	11MS	SSSR	DDDD	N	–	Z	O
MOVE RS,*RD,F	Move Field: Register to Indirect	1	†	1000	00FS	SSSR	DDDD	–	–	–	–
MOVE RS,–*RD,F	Move Field: Register to Indirect (pre-dec)	1	†	1010	00FS	SSSR	DDDD	–	–	–	–
MOVE RS,*RD+,F	Move Field: Register to Indirect (post-inc)	1	†	1001	00FS	SSSR	DDDD	–	–	–	–
MOVE *RS,RD,F	Move Field: Indirect to Register	1	†	1000	01FS	SSSR	DDDD	N	–	Z	O
MOVE –*RS,RD,F	Move Field: Indirect (pre-dec) to Register	1	†	1010	01FS	SSSR	DDDD	N	–	Z	O
MOVE *RS+,RD,F	Move Field: Indirect (post-inc) to Register	1	†	1001	01FS	SSSR	DDDD	N	–	Z	O
MOVE *RS,*RD,F	Move Field: Indirect to Indirect	1	†	1000	10FS	SSSR	DDDD	–	–	–	–
MOVE –*RD,–*RD,F	Move Field: Ind. (pre-dec) to Ind. (pre-dec)	1	†	1010	10FS	SSSR	DDDD	–	–	–	–
MOVE *RS+,*RD+,F	Move Field: Ind. (post-inc) to Ind. (post-inc)	1	†	1001	10FS	SSSR	DDDD	–	–	–	–
MOVE RS,*RD(Disp),F	Move Field: Register to Indirect with Disp.	2	†	1011	00FS	SSSR	DDDD	–	–	–	–
MOVE *RS(DISP),RD,F	Move Field: Indirect with Disp. to Register	2	†	1011	01FS	SSSR	DDDD	N	–	Z	O
MOVE *RS(Disp),*RD+,F	Move Field: Ind. with Disp. to Ind. (post-inc)	2	†	1101	00FS	SSSR	DDDD	–	–	–	–
MOVE *RS(Disp),*RD(Disp),F	Move Field: Ind. with Disp. to Ind. with Disp.	3	†	1011	10FS	SSSR	DDDD	–	–	–	–
MOVE RS,@DADDR,F	Move Field: Register to Absolute	3	†	0000	01F1	100R	SSSS	–	–	–	–
MOVE @SADDR,*RD,F	Move Field: Absolute to Register	3	†	0000	01F1	101R	DDDD	N	–	Z	O
MOVE @SADDR,*RD+,F	Move Field: Absolute to Indirect (post-inc)	3	†	1101	010F	000R	DDDD	–	–	–	–
MOVE @SADDR,@DADDR,F	Move Field: Absolute to Absolute	5	†	0000	01F1	1100	0000	–	–	–	–

†Number of cycles depends on field size and alignment. See TMS34010 User's Guide (SPVU001).

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

GENERAL INSTRUCTIONS

SYNTAX	DESCRIPTION	NO. WORDS	MINIMUM CYCLES	16-BIT OPCODE (MSB → LSB)	STATUS BITS
ABS RD	Store Absolute Value	1	1	0000 0011 100R DDDD	N – Z 0
ADD RS,RD	Add Registers	1	1	0100 000S SSSR DDDD	N C Z V
ADDC RS,RD	Add Register with Carry	1	1	0100 001S SSSR DDDD	N C Z V
ADDI IW,RD	Add Immediate (16 Bits)	2	2	0000 1011 000R DDDD	N C Z V
ADDI IL,RD	Add Immediate (32 Bits)	3	3	0000 1011 001R DDDD	N C Z V
ADDK K,RD	Add Constant (5 Bits)	1	1	0001 00KK KKKR DDDD	N C Z V
AND RS,RD	AND Registers	1	1	0101 000S SSSR DDDD	– – Z –
ANDI IL,RD	AND Immediate (32 Bits)	3	3	0000 1011 100R DDDD	– – Z –
ANDN RS,RD	AND Register with Complement	1	1	0101 001S SSSR DDDD	– – Z –
ANDNI IL,RD	AND Not Immediate (32 Bits)	3	3	0000 1011 100R DDDD	– – Z –
BTST K,RD	Test Register Bit - Constant	1	1	0001 11KK KKKR DDDD	– – Z –
BTST RS,RD	Test Register Bit - Register	1	2	0100 101S SSSR DDDD	– – Z –
CLR RD	Clear Register	1	1	0101 011D DDDR DDDD	– – – –
CLRC	Clear Carry	1	1	0000 0011 0010 0000	– 0 – –
CMP RS,RD	Compare Registers	1	1	0000 1011 010R DDDD	N C Z V
CMPI IW,RD	Compare Immediate (16 Bits)	2	2	0000 1011 010R DDDD	N C Z V
CMPI,IL,RD	Compare Immediate (32 Bits)	3	3	0000 1011 011R DDDD	N C Z V
DEC RD	Decrement Register	1	1	0001 0100 001R DDDD	– – – –
DINT	Disable Interrupts	1	3	0000 0011 0110 0000	– – – –
DIVS RS,RD	Divide Registers Signed	1	40	0101 100S SSSR DDDD	N – Z V
DIVU RS,RD	Divide Registers Unsigned	1	37	0101 101S SSSR DDDD	– – Z V
EINT	Enable Interrupts	1	3	0000 1101 0110 0000	– – – –
EXGF RD,F	Exchange Field Size	1	1	1101 01F1 000R DDDD	– – – –
LMO RS,RD	Leftmost One	1	1	0110 101S SSSR DDDD	– – Z –
MMFM RS,List	Move Multiple Registers from Memory	2	†	0000 1001 101R DDDD	– – – –
MMTM RD,List	Move Multiple Registers to Memory	2	†	0000 1001 100R DDDD	– – – –
MODS RS,RD	Modulus Signed	1	40	0110 110S SSSR DDDD	N – Z V
MODU RS,RD	Modulus Unsigned	1	35	0110 111S SSSR DDDD	– – Z V
MOVI IW,RD	Move Immediate (16 Bits)	2	2	0000 1001 110R DDDD	N – Z 0
MOVI IL,RD	Move Immediate (32 Bits)	3	3	0000 1001 111R DDDD	N – Z 0
MOVK K,RD	Move Constant (5 Bits)	1	1	0001 10KK KKKR DDDD	– – – –
MPYS RS,RD	Multiply Registers (Signed)	1	$5+\frac{FS1}{2}$	0101 110S SSSR DDDD	N – Z –
MPYU RS,RD	Multiply Registers (Unsigned)	1	$5+\frac{FS1}{2}$	0101 111S SSSR DDDD	– – Z –
NEG RD	Negate Register	1	1	0000 0011 101R DDDD	N C Z V
NEGB RD	Negate Register with Borrow	1	1	0000 0011 110R DDDD	N C Z V
NOP	No operation	1	1	0000 0011 0000 0000	– – – –
NOT RD	Complement Register	1	1	0000 0011 111R DDDD	– – Z –
OR RS,RD	OR Registers	1	1	0101 010S SSSR DDDD	– – Z –
ORI IL,RD	OR Immediate (32 bits)	3	3	0000 1011 101R DDDD	– – Z –
RL K,RD	Rotate Left - Constant	1	1	0011 00KK KKKR DDDD	– C Z –
RL RS,RD	Rotate Left - Register	1	1	0110 100S SSSR DDDD	– C Z –
SETC	Set Carry	1	1	0000 1101 1110 0000	– 1 – –
SETF FS,FE,F	Set Field Parameters	1	1,2	0000 01F1 01FS SSSS	– – – –
SEXT RD,F	Sign Extend to Long	1	3	0000 01F1 000R DDDD	N – Z –

†Number of cycles depends on number of registers in list and stack alignment. See TMS34010 User's Guide (SPVU001).

SYNTAX	DESCRIPTION	NO. WORDS	MINIMUM CYCLES	16-BIT OPCODE MSB			LSB	STATUS BITS			
SLA K,RD	Shift Left Arithmetic - Constant	1	3	0010	00KK	KKKR	DDDD	N	C	Z	V
SLA RS,RD	Shift Left Arithmetic - Register	1	3	0110	000S	SSSR	DDDD	N	C	Z	V
SLL K,RD	Shift Left Logical - Constant	1	1	0010	01KK	KKKR	DDDD	–	C	Z	–
SLL RS,RD	Shift Left Logical - Register	1	1	0110	001S	SSSR	DDDD	–	C	Z	–
SRA K,RD	Shift Right Arithmetic - Constant	1	1	0010	10KK	KKKR	DDDD	N	C	Z	–
SRA RS,RD	Shift Right Arithmetic - Register	1	1	0110	010S	SSSR	DDDD	N	C	Z	–
SRL K,RD	Shift Right Logical - Constant	1	1	0010	11KK	KKKR	DDDD	–	C	Z	–
SRL RS,RD	Shift Right Logical - Register	1	1	0110	011S	SSSR	DDDD	–	C	Z	–
SUB RS,RD	Subtract Registers	1	1	0100	010S	SSSR	DDDD	N	C	Z	V
SUBB RS,RD	Subtract Registers with Borrow	1	1	0100	011S	SSSR	DDDD	N	C	Z	V
SUBI IW,RD	Subtract Immediate (16 Bits)	2	2	0000	1011	111R	DDDD	N	C	Z	V
SUBI IL,RD	Subtract Immediate (32 Bits)	3	3	0000	1101	000R	DDDD	N	C	Z	V
SUBK K,RD	Subtract Immediate (5 Bits)	1	1	0001	01KK	KKKR	DDDD	N	C	Z	V
XOR RS,RD	Exclusively OR Registers	1	1	0101	011S	SSSR	DDDD	–	–	Z	–
XORI IL,RD	Exclusively OR Immediate Value (32 Bits)	3	3	0000	1011	110D	DDDD	–	–	Z	–
ZEXT RD,F	Zero Extend to Long	1	1	0000	01F1	001R	DDDD	–	–	Z	–

PROGRAM CONTROL AND CONTEXT SWITCHING

SYNTAX	DESCRIPTION	NO. WORDS	MINIMUM CYCLES	16-BIT OPCODE MSB			LSB	STATUS BITS			
CALL RS	Call Subroutine Indirect	1	6	0000	1001	001R	DDDD	–	–	–	–
CALLA ADDR	Call Subroutine Absolute	3	6	0000	1101	0101	1111	–	–	–	–
CALLR ADDR	Call Subroutine Relative	2	5	0000	1101	0011	1111	–	–	–	–
DSJ RD,ADDR	Decrement Register and Skip Jump	2	3,2	0000	1101	100R	DDDD	–	–	–	–
DSJEQ RD,ADDR	Conditionally Decrement Register and Skip Jump	2	3,2	0000	1101	101R	DDDD	–	–	–	–
DSJNE RD,ADDR	Conditionally Decrement Register and Skip Jump	2	3,2	0000	1101	110R	DDDD	–	–	–	–
DSJS RD,ADDR	Decrement Register and Skip Jump - Short	1	2,3	0011	1Dxx	xxxR	DDDD	–	–	–	–
EMU	Initiate Emulation	1	6	0000	0001	0000	0000	–	–	–	–
EXGPC RD	Exchange Program Counter with Register	1	2	0000	0001	001R	DDDD	–	–	–	–
GETPC RD	Get Program Counter into Register	1	1	0000	0001	010R	DDDD	–	–	–	–
GETST RD	Get Status Register into Register	1	1	0000	0001	100R	DDDD	–	–	–	–
JAcc ADDR	Jump Absolute Conditional	3	3,4	1100	code	1000	0000	–	–	–	–
JRcc ADDR	Jump Relative Conditional	2	3,2	1100	code	0000	0000	–	–	–	–
JRcc ADDR	Jump Relative Conditional - Short	1	2,1	1100	code	xxxx	xxxx	–	–	–	–
JUMP RS	Jump Indirect	1	2	0000	0001	011R	DDDD	–	–	–	–
POPST	Pop Status Register from Stack	1	8	0000	0001	1100	0000	–	–	–	–
PUSHST	Push Status Register onto Stack	1	2	0000	0001	1110	0000	–	–	–	–
PUTST RS	Copy Register into Status	1	3	0000	0001	101R	DDDD	N	C	Z	V
RETI	Return from Interrupt	1	11	0000	1001	0100	0000	N	C	Z	V
RETS (N)	Return from Subroutine	1	7	0000	1001	011N	NNNN	–	–	–	–
REV RD	Get Revision Number	1	1	0000	0000	001R	DDDD	–	–	–	–
TRAP N	Software Interrupt	1	16	0000	1001	000N	NNNN	0	0	0	0

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

development systems and software support

Texas Instruments, together with third party suppliers, offers a full range of hardware and software development tools for the TMS34010. The support environment is aimed at four areas of support with the key tools based on the IBM PC, DEC VAX, and TI Professional computers:

DESIGNER	TOOLS
Hardware	XDS-22 Real Time Emulator (with PC-based Debugger Interface)
	PC Software Development Board (with Debugger Interface)
Software	Assembly Language Package, including:
	Macro Assembler, Linker, Archiver, ROM Utility, Software Simulator (PC-only)
	Graphics/Math Function Library
	Bit-Mapped Font Library
Languages	"C" Compiler Package including:
	34010 "C" Compiler
	Run Time Support
Systems	Window Management Support
	Image Processing Support
	Graphics Interfaces and Standards
	Debugger Adaptation Software

Further support is provided through a network of Regional Technology Centers (RTCs).

TMS340 FAMILY HARDWARE AND SOFTWARE SUPPORT

SILICON	PART NUMBER
Graphics System Processor 68-Pin PLCC	TMS34010FNL
Video System Controller 68-Pin PLCC	TMS34061FNL
Color Palette 22-Pin DIP	TMS34070NL
64Kx1 Multiport Memory 22-Lead PLCC (120 and 150 ns)	TMS4161FML
64Kx1 Multiport Memory 22-Pin DIP (120 and 150 ns)	TMS4161NL
64Kx4 Multiport Memory 24-Pin DIP	TMS4461NL

SOFTWARE TOOLS	COMPUTER	OPERATING SYSTEM	PART NUMBER
TMS34010 Assembler Package:			
Assembler, Linker, Archiver,	IBM/TI PC	MS-DOS 2.11+	TMDS3440808002
Code Conversion Utility, Simulator			
TMS34010 Assembler Package:			
Assembler, Linker, Archiver,	VAX	VMS	TMDS3440200059
Code Conversion Utility (GSP)	VAX	ULTRIX	TMDS3440200069
	VAX	System V	TMDS3440200089
TMS34010 "C" Compiler Package	IBM/TI PC	MS-DOS 2.11+	TMDS3440805002
	VAX	VMS	TMDS3440205059
	VAX	ULTRIX	TMDS3440205069
	VAX	Systém V	TMDS3440205089
TMS34010 Graphics/Math			
Function Library	IBM/TI PC - Source		TMDS3440802202
	VAX - Source		TMDS3440802208
TMS34010 Bit-Mapped Font Library	IBM/TI PC	MS-DOS 2.11+	TMDS3440802302
	VAX	ALL	TMDS3440202308
TMS34010 PC Debugger Development Package (For Internal Use)	IBM/TI PC	MS-DOS 2.11+	TMDS3440806002
TMS34010 PC Debuffer Development Package (For Resale)	IBM/TI PC	MS-DOS 2.11+	TMDS3440806003

HARDWARE TOOLS	COMPUTER	VERSION	PART NUMBER
TMS34010 XDS-22 Real-Time Emulator with BT&T		U.S.	TMDS3469910000
		Europe	TMDS3469981000
Color Graphics Controller Board (TMS34061, TMS34070)	IBM/TI PC		TMDS3471804000
TMS34010 Software Development Board	IBM/TI PC		TMDS3411804420

DESIGN KITS	PART NUMBER
TMS340 Graphics Design Kit, including TMS34061, TMS34070, TMS4161s	TMS340GDK
TMS34010 Graphics Design Kit, including TMS34010, TMS34070, TMS4461s, PC Assembler	TMS34010GDK

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

reset

Reset puts the TMS34010 into a known initial state. It is entered when the input signal at the $\overline{\text{RESET}}$ pin is asserted low. $\overline{\text{RESET}}$ must remain active low for a minimum of 40 local clock (LCLK1 and LCLK2) periods to ensure that the TMS34010 has sufficient time to establish its initial internal state.

While $\overline{\text{RESET}}$ remains asserted, all outputs are in a known state, no DRAM-refresh cycles take place, and no screen-refresh cycles are performed.

At the low-to-high transition of the $\overline{\text{RESET}}$ signal, the state of the $\overline{\text{HCS}}$ input determines whether the GSP will be halted or begin executing instructions. The GSP may be in one of two modes, host-present or self-bootstrap mode.

1. Host-Present Mode

   If $\overline{\text{HCS}}$ is high at the end of reset, GSP instruction execution is halted and remains halted until the host clears the HLT (halt) bit in HSTCTL (host control register). Following reset, the eight $\overline{\text{RAS}}$-only refresh cycles required to initialize the dynamic RAMs are performed automatically by the GSP memory control logic. As soon as the eight $\overline{\text{RAS}}$-only cycles are completed, the host is allowed access to GSP memory. At this time, the GSP begins to automatically perform DRAM refresh cycles at regular intervals. The GSP remains halted until the host clears the HLT bit. Only then does the GSP fetch the level-0 vector address from location >FFFF FFE0 and begin executing its reset service routine.

2. Self-Bootstrap Mode

   If $\overline{\text{HCS}}$ is low at the end of reset, the GSP first performs the eight $\overline{\text{RAS}}$-only refresh cycles required to initialize the DRAMs. Immediately following the eight $\overline{\text{RAS}}$-only cycles, the GSP fetches the level-0 vector address from location >FFFF FFE0, and begins executing its reset service routine.

Unlike other interrupts and software traps, reset does not save previous ST or PC values. This is because the value of the stack pointer just before a reset is generally not valid, and saving its value on the stack is unnecessary. A TRAP 0 instruction, which uses the same vector address as reset, similarly does not save the ST or PC values.

asserting reset

A reset is initiated by asserting the $\overline{\text{RESET}}$ input pin at its active-low level. To reset the GSP at power up, $\overline{\text{RESET}}$ must remain active low for a minimum of 40 local clock periods after power levels have become stable. At times other than power up, the GSP is also reset by holding $\overline{\text{RESET}}$ low for a minimum of 40 clock periods. The 40-clock interval is required to bring GSP internal circuitry to a known initial state. While $\overline{\text{RESET}}$ remains asserted, the output and bidirectional signals are driven to a known state.

The GSP drives its $\overline{\text{RAS}}$ signal inactive high as long as $\overline{\text{RESET}}$ remains low. The specifications for certain DRAM and VRAM devices, including the TMS4161, TMS4164 and TMS4464 devices, require that the $\overline{\text{RAS}}$ signal be driven inactive-high for 100 microseconds during system reset. Holding $\overline{\text{RESET}}$ low for 150 microseconds will cause the $\overline{\text{RAS}}$ signal to remain high for the 100 microseconds required to bring the memory devices to their initial states. DRAMs such as the TMS4256 specify an initial $\overline{\text{RAS}}$ high time of 200 microseconds, requiring that $\overline{\text{RESET}}$ be held low for 250 microseconds. In general, holding $\overline{\text{RESET}}$ low for t microseconds ensures that $\overline{\text{RAS}}$ remains high initially for $t-50$ microseconds.

suspension of DRAM-refresh cycles during reset

An active-low level at the $\overline{\text{RESET}}$ pin is considered to be a power-up condition, and DRAM refresh is not performed until $\overline{\text{RESET}}$ goes inactive high. Consequently, the previous contents of the local memory may not be valid after a reset.

initial state following reset

While the $\overline{\text{RESET}}$ pin is asserted low, the GSP's output and bidirectional pins are forced to the states listed below.

INITIAL STATE OF PINS FOLLOWING A RESET

OUTPUTS DRIVEN TO HIGH LEVEL	OUTPUTS DRIVEN TO LOW LEVEL	BIDIRECTIONAL PINS DRIVEN TO HIGH IMPEDANCE
DDOUT	$\overline{\text{BLANK}}$	$\overline{\text{HSYNC}}$
HRDY		$\overline{\text{VSYNC}}$
$\overline{\text{DEN}}$		HD0-HD15
$\overline{\text{LAL}}$		LAD0-LAD15
$\overline{\text{TR/QE}}$		
$\overline{\text{RAS}}$		
$\overline{\text{CAS}}$		
$\overline{\text{W}}$		
$\overline{\text{HINT}}$		

Immediately following reset, all I/O registers are cleared (set to >0000), with the possible exception of the HLT bit in the HSTCTL register. The HLT bit is set to 1 if $\overline{\text{HCS}}$ is high just prior to the low-to-high transition of $\overline{\text{RESET}}$.

Just prior to execution of the first instruction in the reset routine, the TMS34010's internal registers are in the following state:

- General-purpose register files A and B are uninitialized.
- The ST is set to >0000 0010.
- The PC contains the 32-bit vector fetched from memory address >FFFF FFE0.

The state of the instruction cache at this time is as follows:

- The SSA (segment start address) registers are uninitialized.
- The LRU (least recently used) stack is set to the initial sequence 0,1,2,3, where 0 occupies the most-recently-used position, and 3 occupies the least-recently-used position.
- All P (present) flags are cleared to 0s.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TMS34010 local memory interface

The TMS34010 local memory interface consists of a triple-multiplexed address/data bus on which row addresses, column addresses, and data are transmitted. The associated memory control signals support direct interfacing to both DRAMs and VRAMs. At the beginning of a typical memory cycle, the address is output in multiplexed fashion as a row address followed by a column address. The remainder of the cycle is used to transfer data between the TMS34010 and memory.

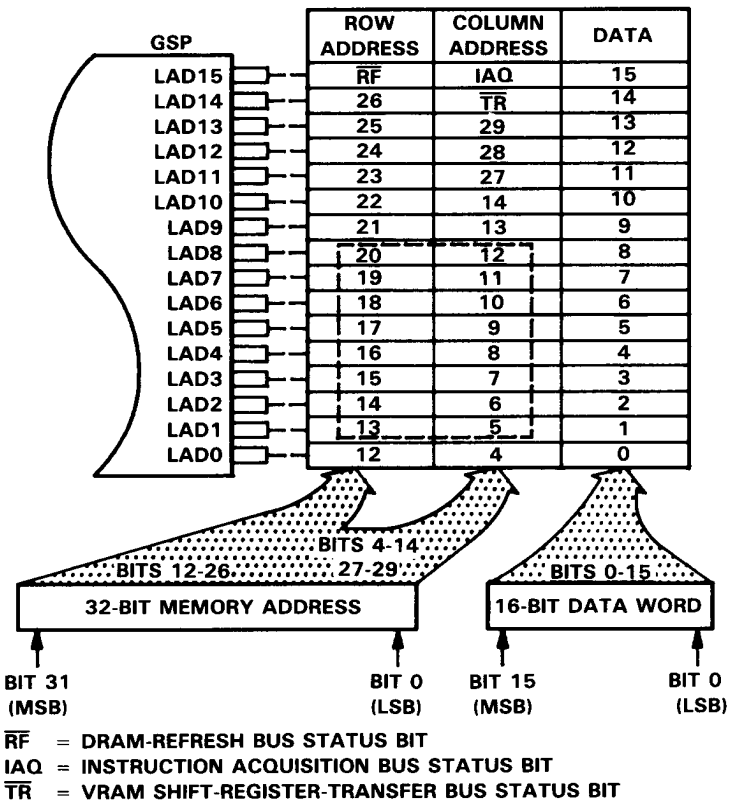


FIGURE 7. TRIPLE MULTIPLEXING OF ADDRESSES AND DATA

The following types of memory cycles are supported: read, write, VRAM memory-to-shift-register, VRAM shift-register-to-memory, $\overline{RAS}$-only DRAM refresh and $\overline{CAS}$-before-$\overline{RAS}$ DRAM refresh. The functional timing for these cycles is shown in the next six figures. The seventh figure indicates the timing signals output during an internal cycle, i.e., a cycle during which no memory access takes place.

During a memory cycle, the row address, column address, and data are transmitted over the same physical bus lines. The manner in which logical addresses are output at the memory interface makes external multiplexing hardware unnecessary, while supporting a wide variety of memory configurations. For example, in Figure 7, 16 consecutive address bits (5 through 20) are output on LAD1-LAD8 during the row and column address times. Output along with the address are bus status signals that indicate when DRAM refresh cycles, screen refresh (VRAM memory-to-shift-register) cycles, and instruction fetch cycles are occurring.

The following remarks apply to memory timing in general. A row address is output on LAD0-LAD15 at the start of the cycle, and is valid before and after the fall of $\overline{RAS}$. Next a column address is output on LAD0-LAD15. The column address is valid briefly before and after the falling edge of $\overline{LAL}$, but is not valid at the falling edge of $\overline{CAS}$. The column address is clocked into an external transparent latch (e.g., a 74AS373 octal latch) on the falling edge of $\overline{LAL}$ to provide the hold time on the column address required for dynamic RAMs and video RAMs. A transparent latch is required in order that the row address be available at the outputs of the latch during the start of the cycle.

Very large memory configurations may require external buffering of data lines. The $\overline{DEN}$ signal serves as the drive-enable signal to external bidirectional buffers, e.g., 74AS245 octal buffers. The DDOUT signal serves as the direction control for the buffers.

When an I/O register is addressed by the TMS34010, a special memory read or write cycle is performed. During this cycle, the external $\overline{RAS}$ signal falls, but the external $\overline{CAS}$ remains inactive-high for the duration of the cycle.

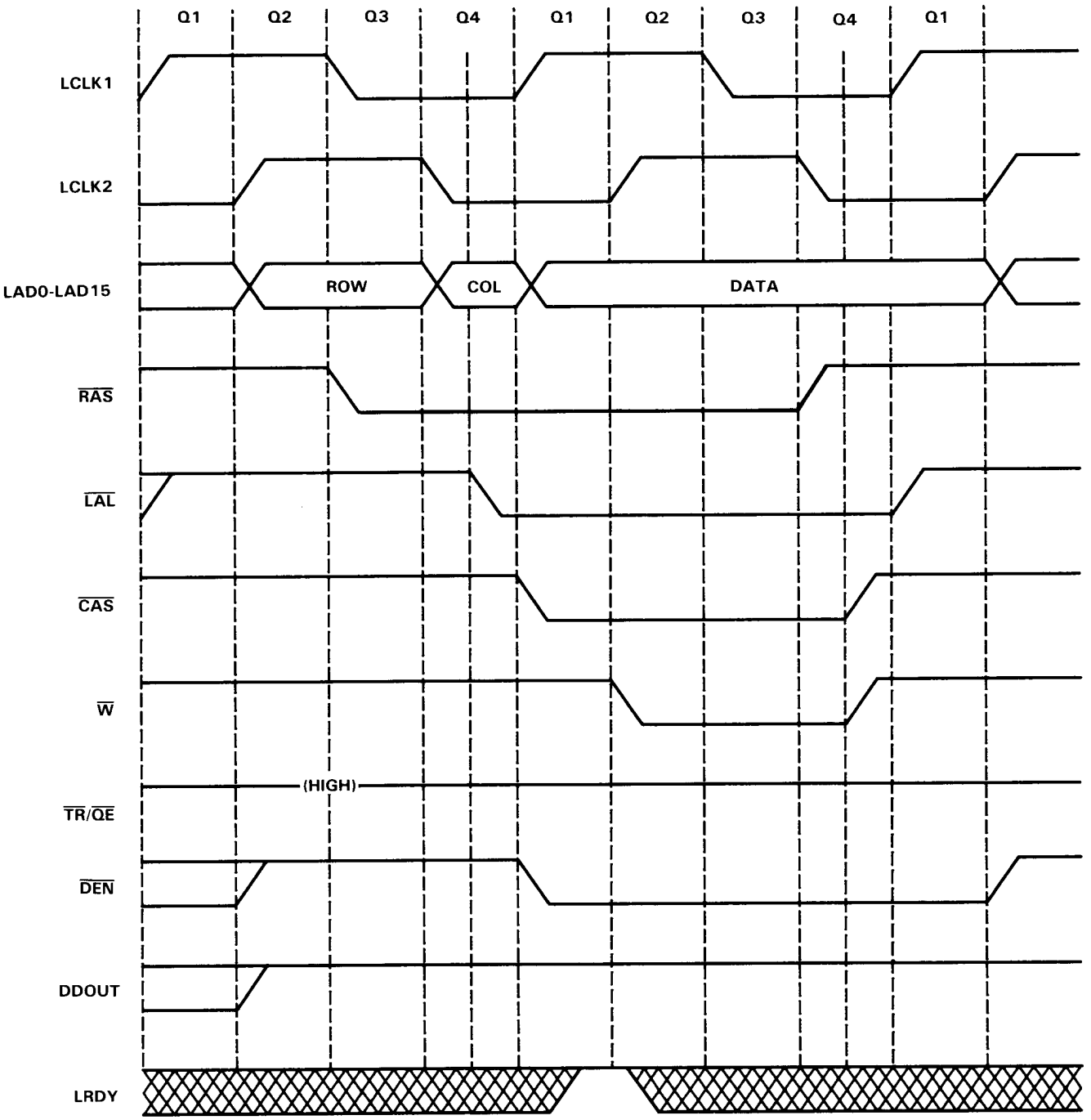
The timing shown in the first six functional timing diagrams assumes that the LRDY input remains high during the cycle. The LRDY pin is pulled low by slower memories requiring a longer cycle time. The TMS34010 samples the LRDY input at the end of Q1, as indicated in the figures. If LRDY is low, the TMS34010 inserts an additional state, called a "wait" state, into the cycle. Wait states continue to be inserted until LRDY is sampled at a high level. The cycle then completes in the manner indicated in the functional timing diagrams. A wait state is one local clock period in duration. Three additional timing diagrams provide examples of cycles extended by wait states.

The LRDY input is ignored by the TMS34010 during internal cycles.

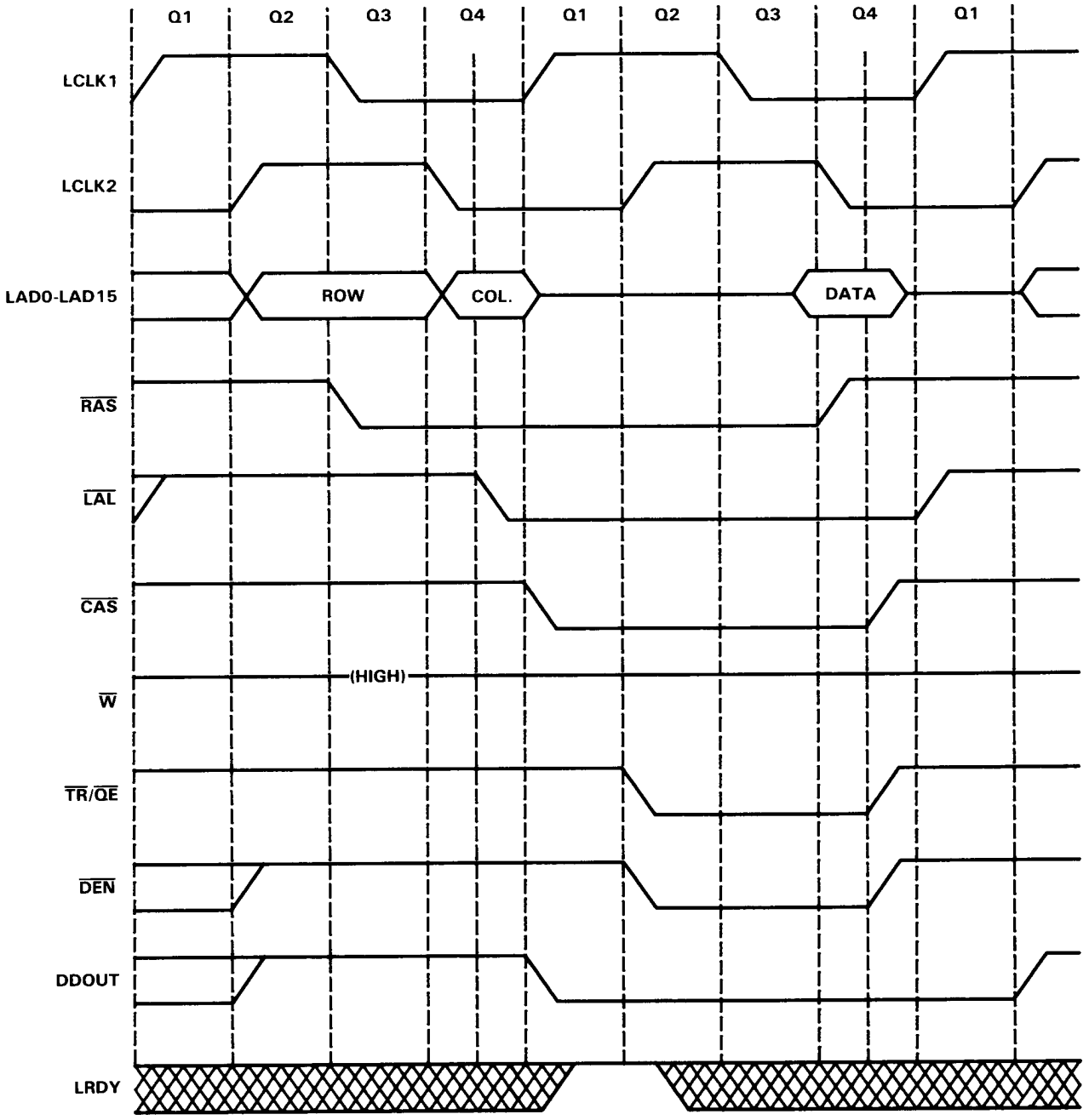
A hold/hold acknowledge capability is also built into the local memory interface to allow external devices to request control of the bus. After acknowledging a hold request, the TMS34010 releases the bus by driving its address/data bus and control outputs into high impedance.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

write cycle timing

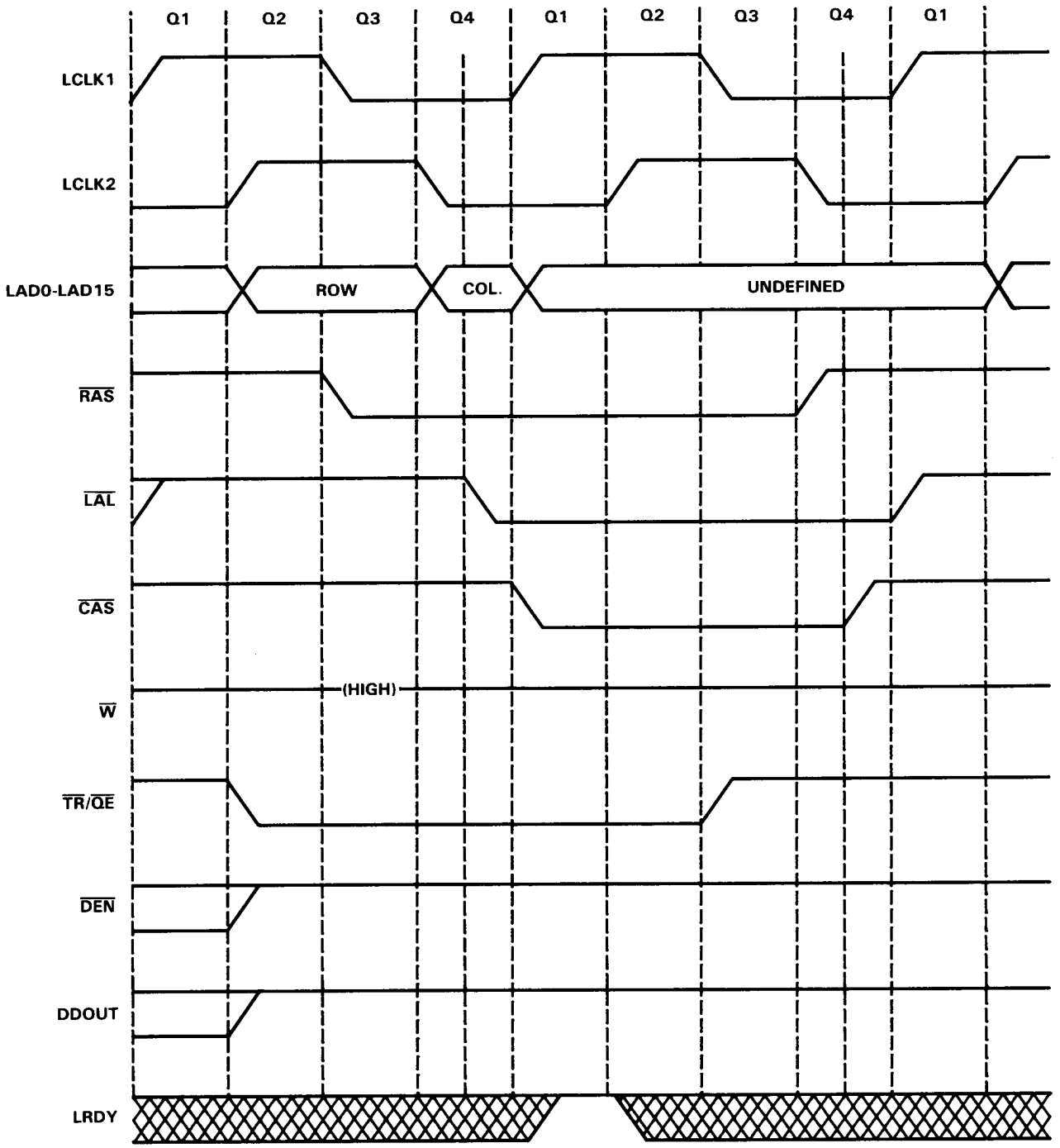


read cycle timing

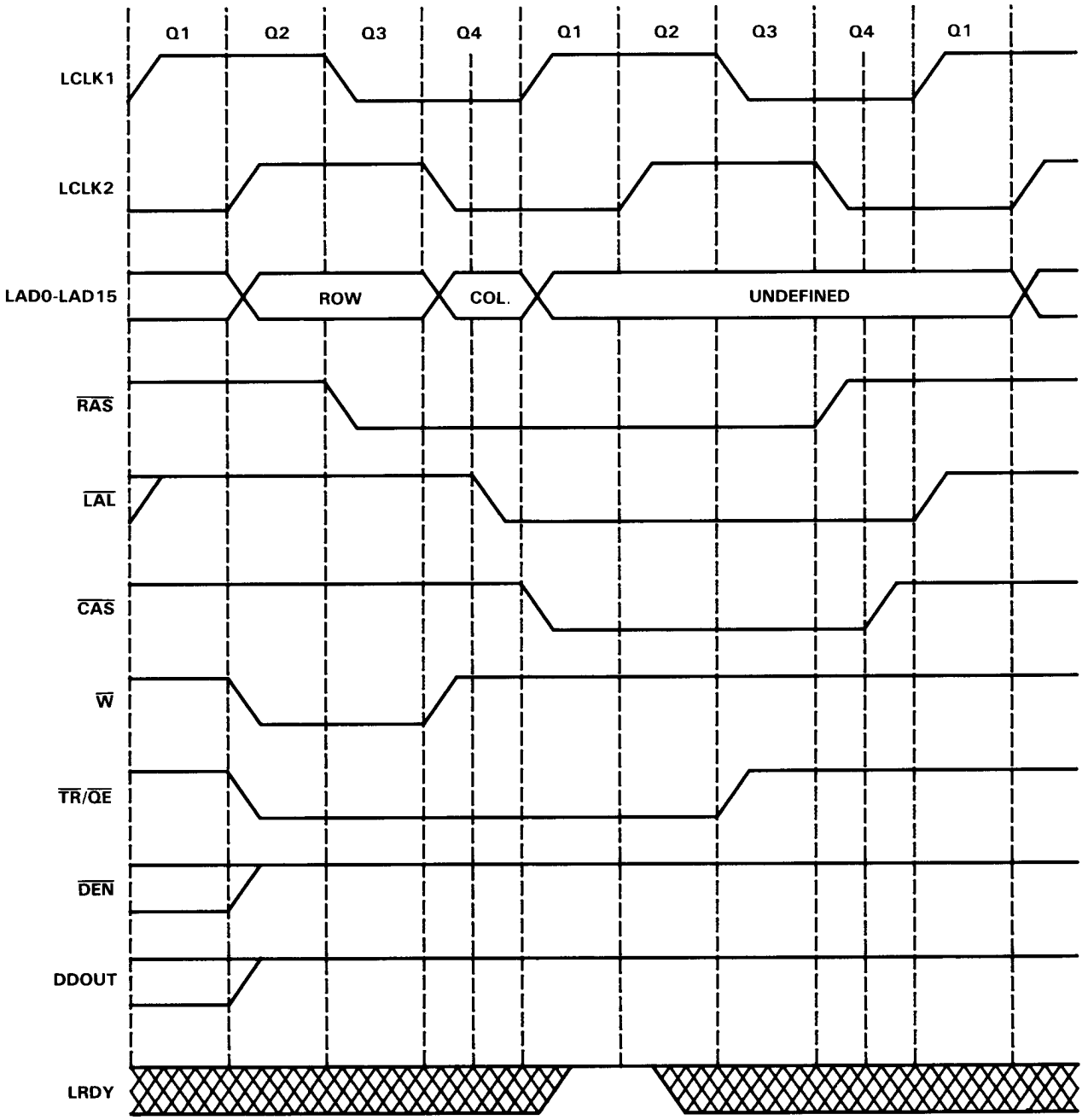


TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

memory to shift register timing

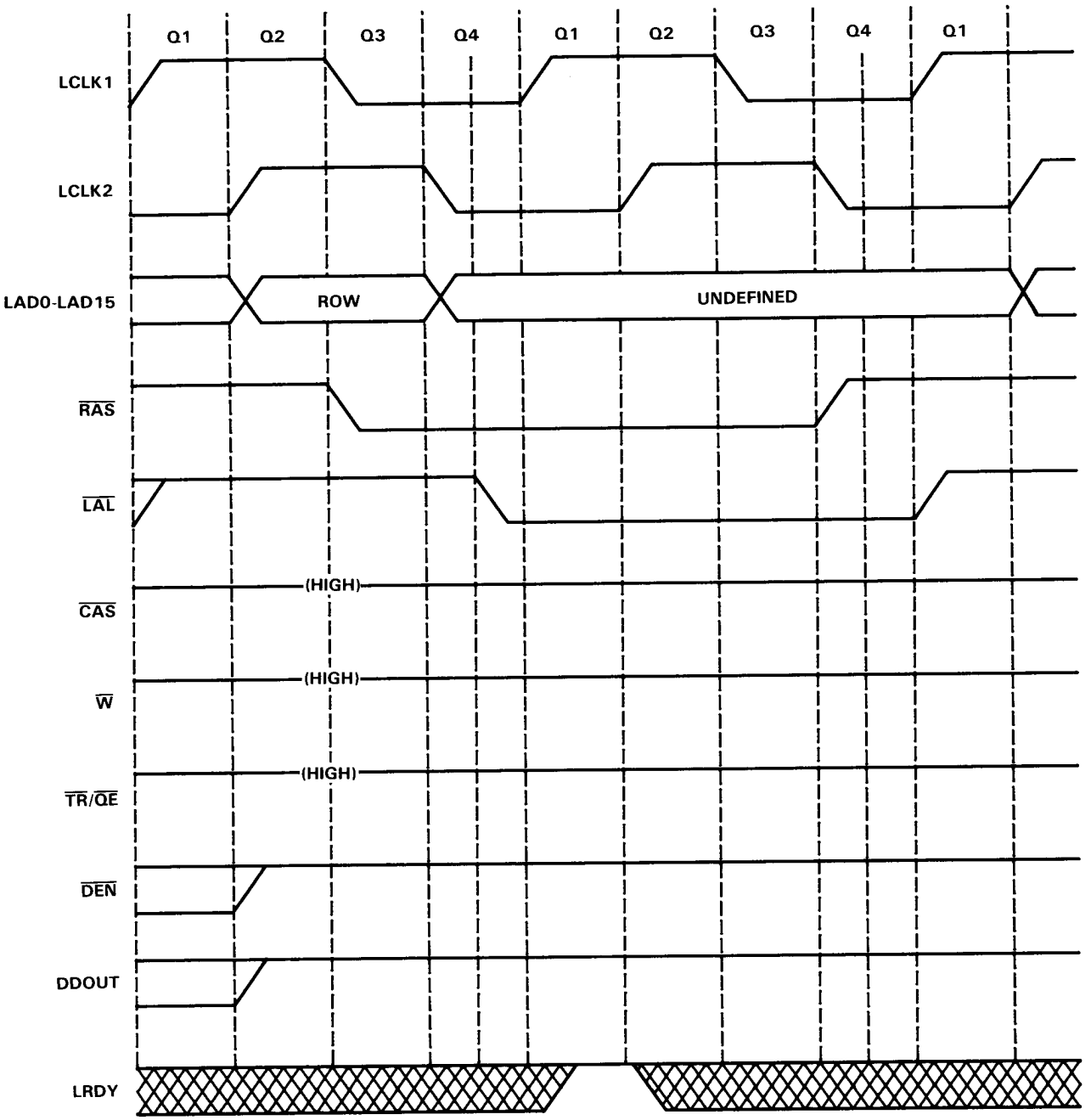


shift register to memory timing

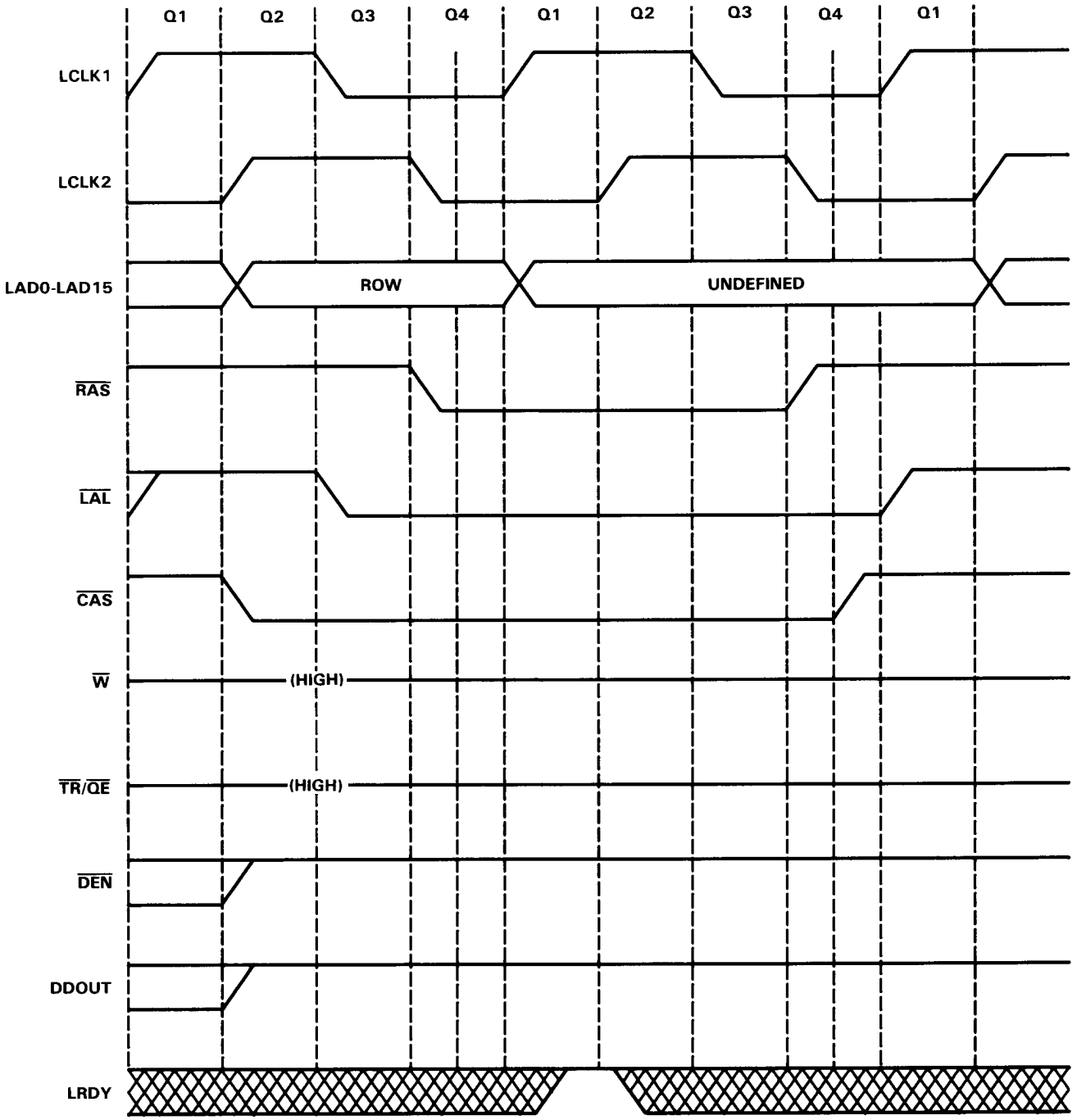


TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

$\overline{\text{RAS}}$-only DRAM refresh cycle timing

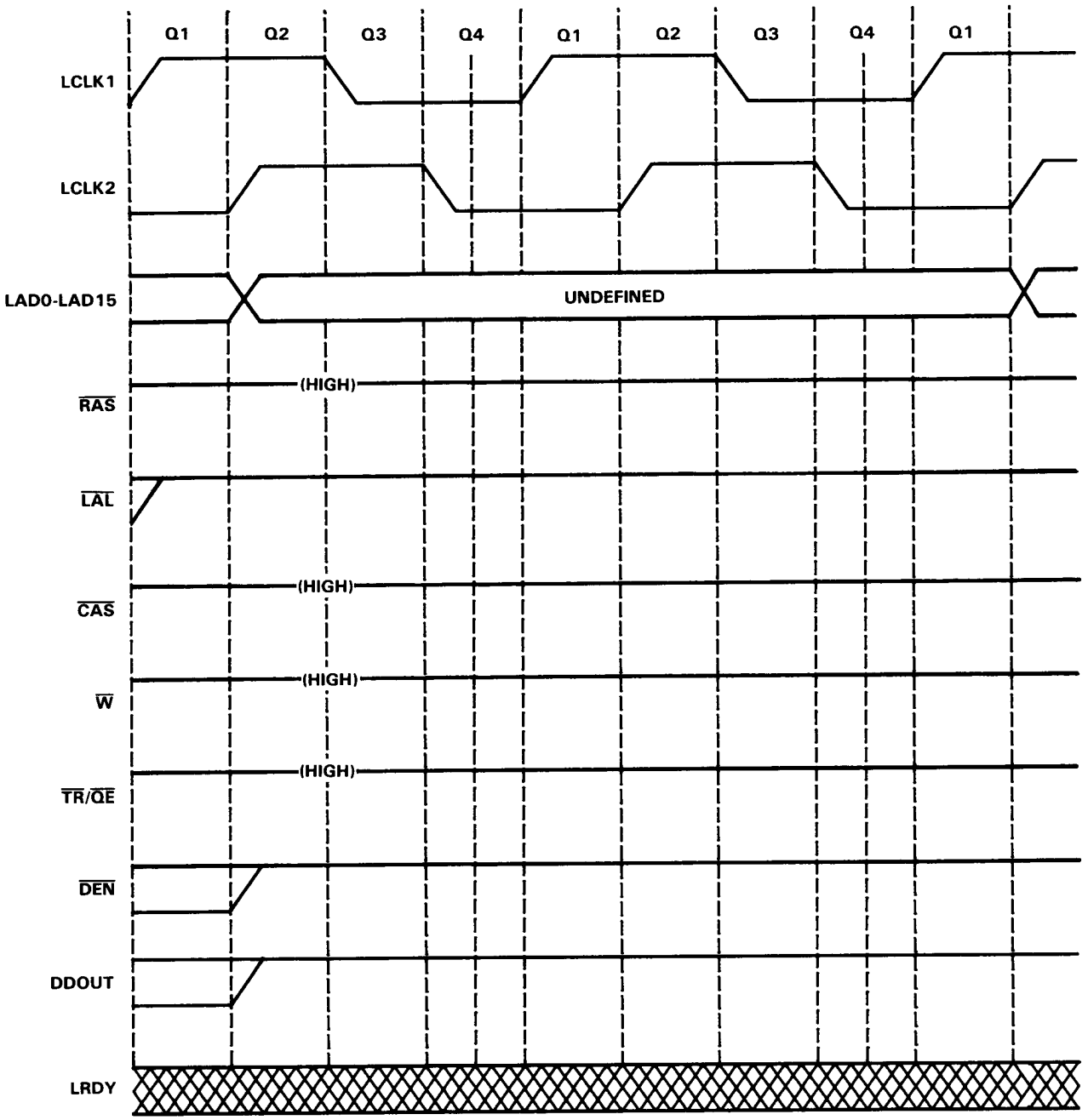


$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle timing

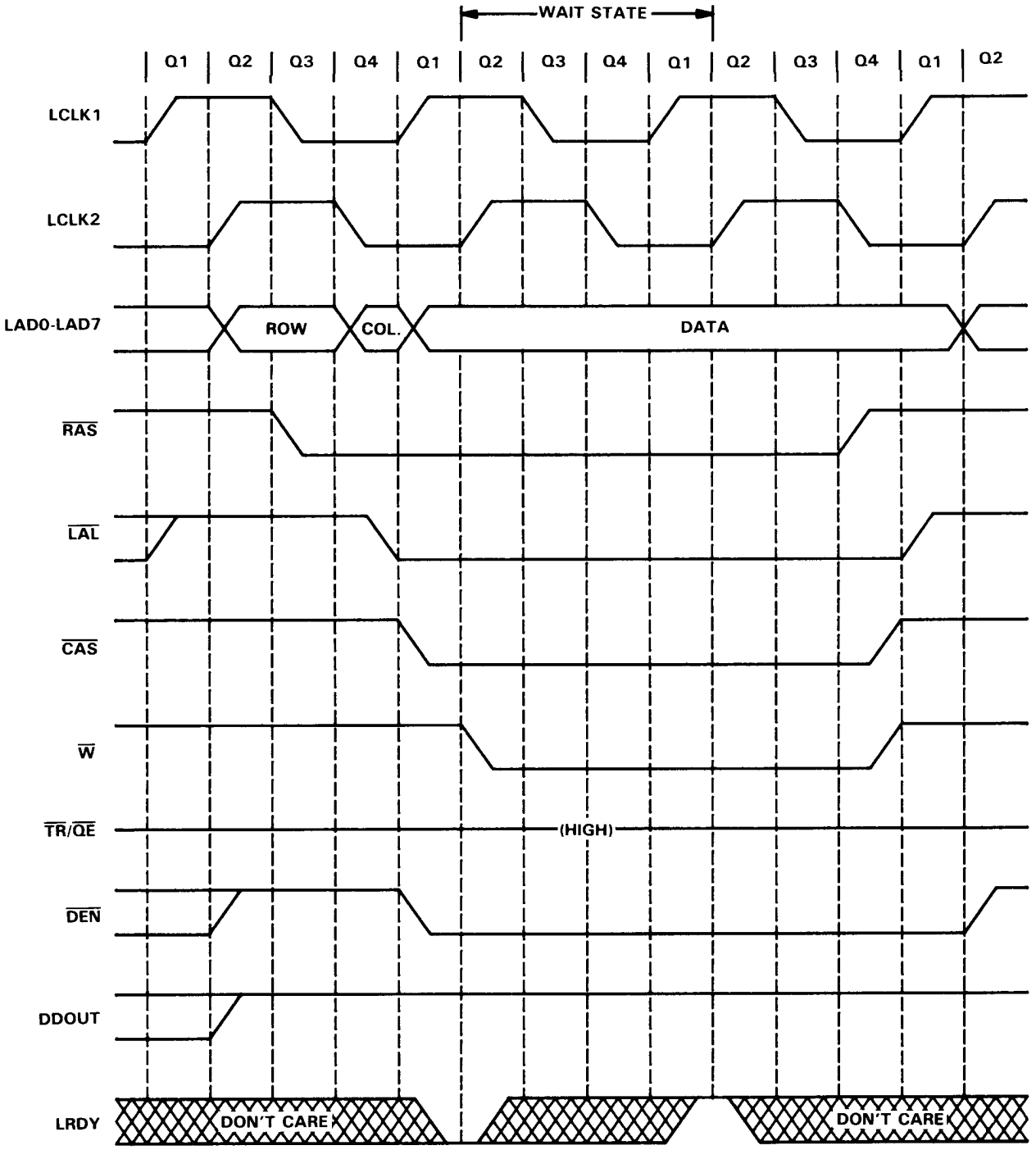


TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

internal cycles back to back

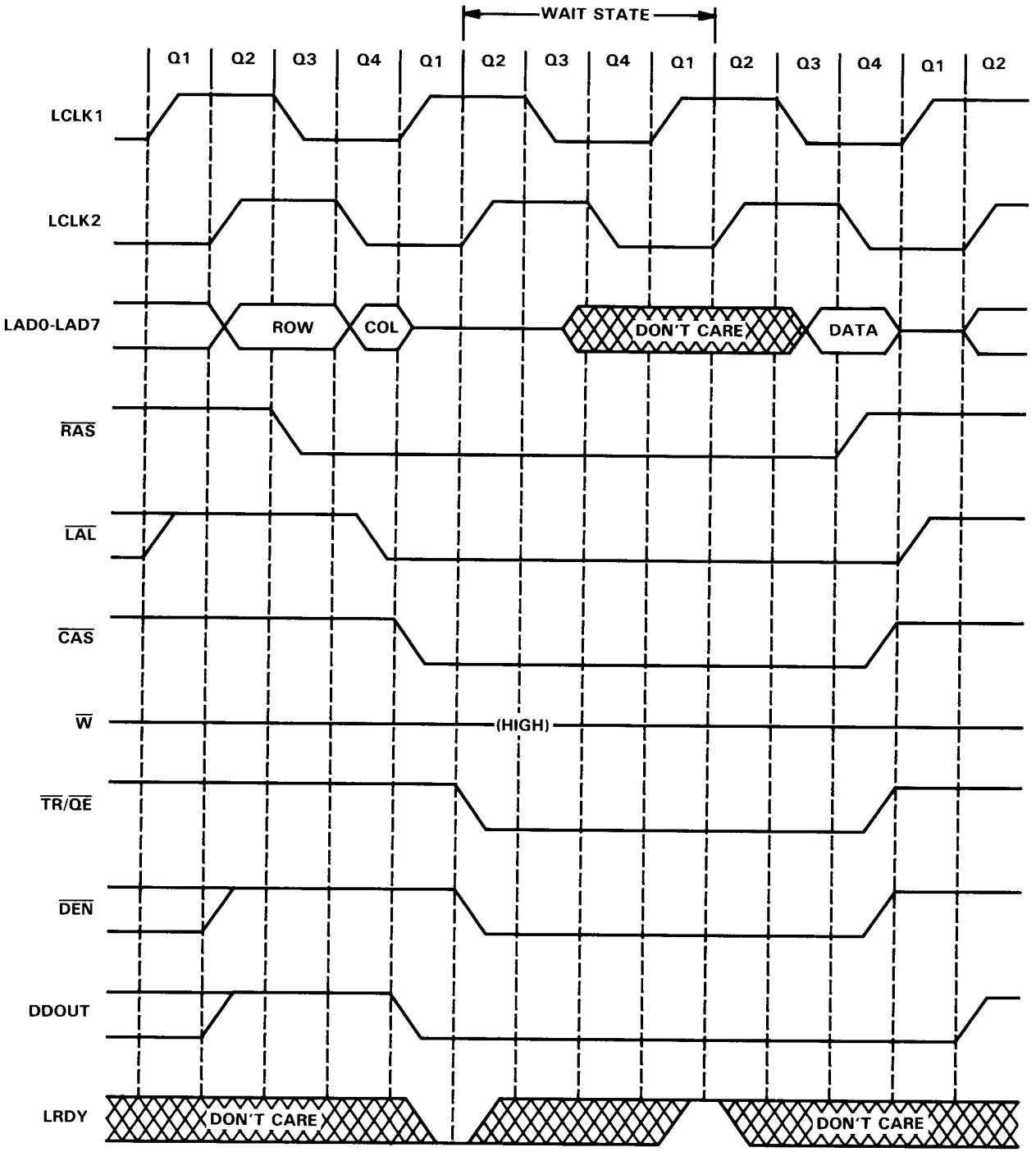


write cycle with one wait state

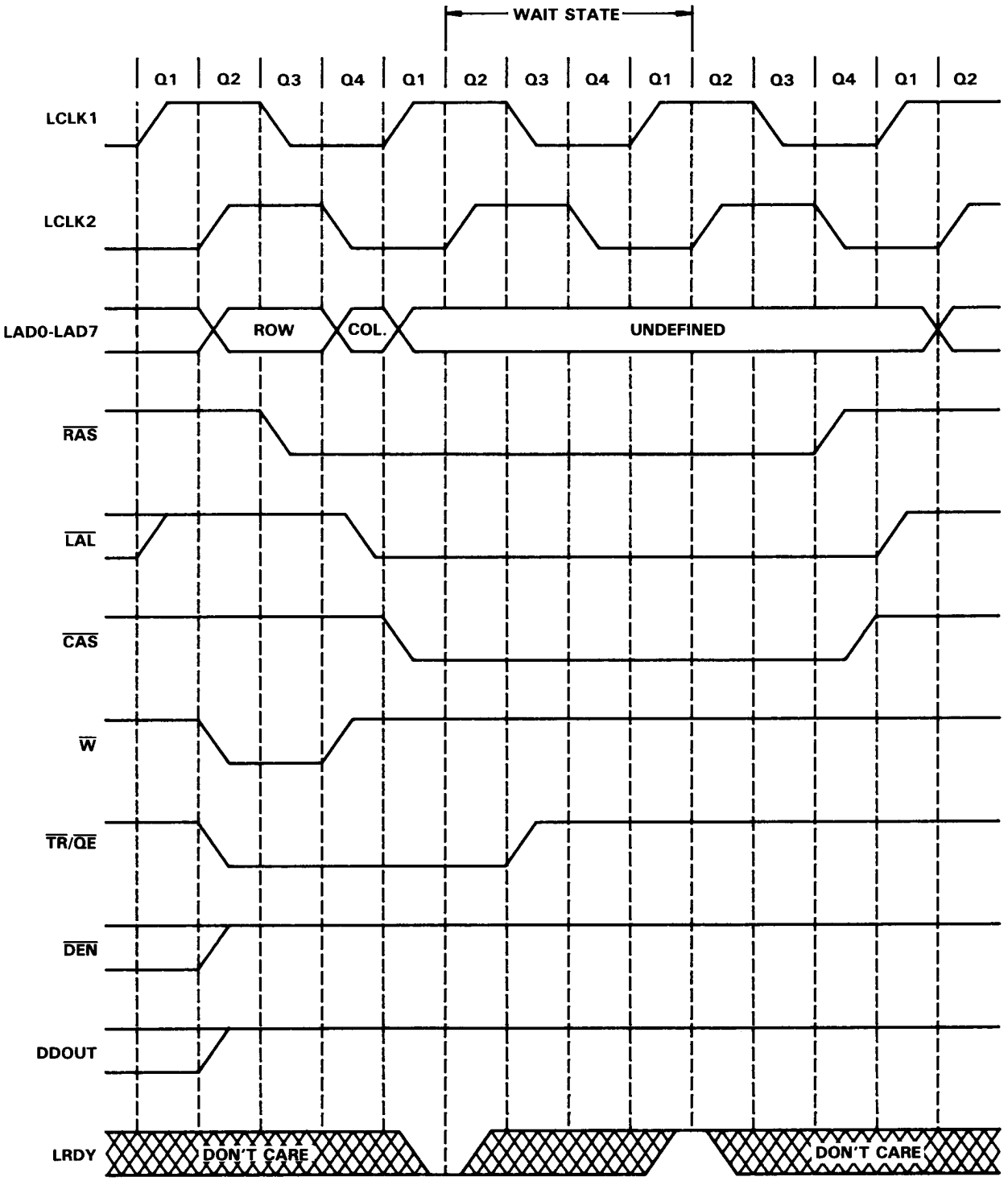


TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

read cycle with one wait state



shift-register-to-memory cycle with one wait state



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Off-state output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −10°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Voltage values are with respect to the V_{SS} pins of the chip.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{SS}	Supply voltage†	0	0	0	V
I_{OH}	High-level output current			400	μA
I_{OL}	Low-level output current			2.0‡	mA
T_A	Operating free-air temperature	0		70	°C

†Care should be taken by card designers to provide a minimum inductance path between the V_{SS} pins and system ground in order to minimize V_{SS} noise.
‡Output current of 2.0 mA is sufficient to drive five low-power Schottky TTL loads or 10 advanced low-power Schottky TTL loads (worst case).

DC electrical characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}§	High-level input voltage, TTL-level signal	All inputs except INCLK	V_{CC} = 5.0 V		2.2		V_{CC}+0.3	V
		INCLK			3.0		V_{CC}+0.3	
V_{IL}	Low-level output voltage, TTL-level signal	All inputs except INCLK			−0.3		0.8	V
		INCLK			−0.3		0.8	
V_{OH}	High-level output voltage, TTL-level signal		V_{CC} = min, I_{OH} = max,		2.6			V
V_{OL}	Low-level output voltage, TTL-level signal		V_{CC} = max, I_{OL} = min,				0.6	V
I_O	High-impedance leakage current, bidirectional pins		V_{CC} = max	V_O = 2.8 V			20	μA
				V_O = 0.6 V			−20	
I_I	Input current	All inputs except RUN/EMU§	V_I = V_{SS} to V_{CC}				20	μA
I_{CC}	Supply current		V_{CC} = max				125	mA
C_I	Input capacitance					10		pF
C_O	Output capacitance (except address/data lines)					10		pF

†For conditions shown as "min" or "max," use the appropriate value specified under "Recommended Operating Conditions."
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§RUN/EMU will be no-connected in a typical configuration. The nominal pull-up current will be 250 μA.

NOTE

Advance information notices apply only to the TMS34010-50.

ADVANCE INFORMATION

signal transition levels

FIGURE 8. TTL-LEVEL OUTPUTS

TTL-level outputs are driven to a minimum logic-high level of 2.6 volts and to a maximum logic-low level of 0.6 volts. Output transition times are specified as follows.

For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be "no longer high" is 2.0 volts, and the level at which the output is said to be "low" is 0.8 volts. For a low-to-high transition, the level at which the output is said to be "no longer low" is 0.8 volts, and the level at which the output is said to be "high" is 2.0 volts.

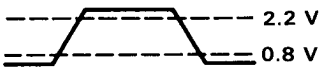


FIGURE 9. TTL-LEVEL INPUTS

Transition times for TTL-compatible inputs are specified as follows. For a high-to-low transition on an input signal, the level at which the input is said to be "no longer high" is 2.2 volts, and the level at which the input is said to be "low" is 0.8 volts. For a low-to-high transition on an input signal, the level at which the input is said to be "no longer low" is 0.8 volts, and the level at which the input is said to be "high" is 2.2 volts.

test measurement

Timing parameters for output signals are guaranteed for external capacitive loading of up to 100 pF per pin. The test load circuit shown in Figure 11 is used in measuring transition times of GSP output signals during test. The values of R_L and V_L are chosen to draw I_{OH} at V_{OH} and draw I_{OL} at V_{OL}.

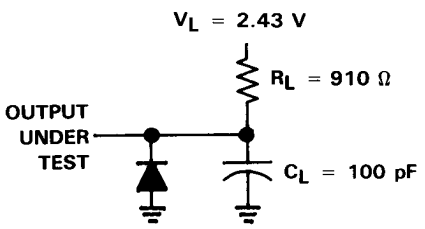


FIGURE 10. SWITCHING TIMES LOAD CIRCUIT

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

AL	$\overline{\text{LAL}}$
C	$\overline{\text{CAS}}$
CA	Column address
CK	LCLK1 and LCLK2
CK1	LCLK1
CK2	LCLK2
CS	$\overline{\text{HCS}}$
D	Data
DD	DDOUT
EN	$\overline{\text{DEN}}$
F	HFS0, HFS1
HK	$\overline{\text{HLDA}}$/$\overline{\text{EMUA}}$
HR	$\overline{\text{HOLD}}$
HS	$\overline{\text{HSYNC}}$ or $\overline{\text{VSYNC}}$
ICK	INCLK
LR	$\overline{\text{LRDY}}$
QE	$\overline{\text{TR}}$/$\overline{\text{QE}}$, when used as output enable
R	$\overline{\text{RAS}}$
RA	Row address
RS	$\overline{\text{HREAD}}$
RY	$\overline{\text{HRDY}}$
S	$\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}$
TR	$\overline{\text{TR}}$/$\overline{\text{QE}}$, when used as shift register enable
VCK	VCLK
W	$\overline{\text{W}}$
WS	$\overline{\text{HWRITE}}$

Lowercase subscripts and their meaning are:

a	access time
c	cycle time (period)
d	delay time
h	hold time
su	setup time
t	transition time
w	pulse duration (width)

The following additional letters and symbols and their meaning are:

H	High
L	Low
V	Valid
Z	High impedance
↑	No longer low
↓	No longer high

host interface timing parameters

The timing parameters for host interface signals are shown in the next four figures. The purpose of these figures and the accompanying table is to quantify the timing relationships among the various signals. The explanation of the logical relationships among signals will be found in the *TMS34010 User's Guide* (number SPVU001).

Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock period, or twice the input clock period, $t_{c(ICK)}$.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(FV-SL)}$	Setup time of $\overline{\text{HWRITE}}/\overline{\text{HREAD}}$ high or HFS0, HFS1 valid to $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}\downarrow$	10		10		ns
2	$t_{d(WSL-DV)}$	Delay from $\overline{\text{HWRITE}}\downarrow$ to data in valid, write cycle		$2t_Q$		$2t_Q$	ns
3	$t_{d(SL-SL)}$	Delay from $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}$ low to next $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}\downarrow$	$7t_Q+10$		$7t_Q+10$		ns
4	$t_{w(SL)}$	Duration of $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}$ low	80		80		ns
5	$t_{d(SH-SL)}$	Delay from $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}$ high to next $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}\downarrow$	60		60		ns
6	$t_{h(WSH-DV)}$	Hold time of data in valid after $\overline{\text{HWRITE}}$ high, write cycle	10		10		ns
7	$t_{h(SH-FV)}$	Hold time of $\overline{\text{HWRITE}}/\overline{\text{HREAD}}$ high or HFS0, HFS1 valid after $\overline{\text{HREAD}}$ or $\overline{\text{HWRITE}}$ high	10		10		ns
8	$t_{h(RSL-DZ)}$	Hold time of data high impedance after $\overline{\text{HREAD}}\downarrow$, read cycle	0		0		ns
9	$t_{d(RSL-DV)}$	Delay from $\overline{\text{HREAD}}$ low to data out valid, read cycle with no wait		90		90	ns
10	$t_{h(RSH-DV)}$	Hold time of data out valid after $\overline{\text{HREAD}}\uparrow$, read cycle	0		0		ns
11	$t_{d(RSH-DZ)}$	Delay from $\overline{\text{HREAD}}$ high to data out high impedance, read cycle		30		30	ns
12	$t_{h(CSL-RYH)}$	Hold time of HRDY high after $\overline{\text{HCS}}\downarrow$, cycle with wait	0		0		ns
13	$t_{d(CSL-RYL)}$	Delay from $\overline{\text{HCS}}$ low to HRDY low, cycle with wait		40		40	ns
14	$t_{w(RYL)}$	Pulse duration of HRDY low, cycle with wait		†		†	ns
15	$t_{d(RYL-RYH)}$	Delay from HRDY↓ to HRDY high, cycle with wait	0‡		0‡		ns
16	$t_{h(RYH-WSL)}$	Hold time of $\overline{\text{HWRITE}}$ low after HRDY↑, write cycle with wait	40		40		ns
17	$t_{d(RYH-DV)}$	Delay from HRDY↑ to data out valid, read cycle with wait		40		40	ns
18	$t_{h(RYH-RSL)}$	Hold time of $\overline{\text{HREAD}}$ low after HRDY↑, read cycle with wait	40		40		ns

NOTE: Advance information notices apply only to the TMS34010-50.
†Parameter 14 is a function of local bus memory contention. This parameter is not tested. Refer to the *TMS34010 User's Guide* for details.
‡Parameter 15 is specified as minimum 0 ns to indicate that a low-going pulse on HRDY can be arbitrarily narrow.

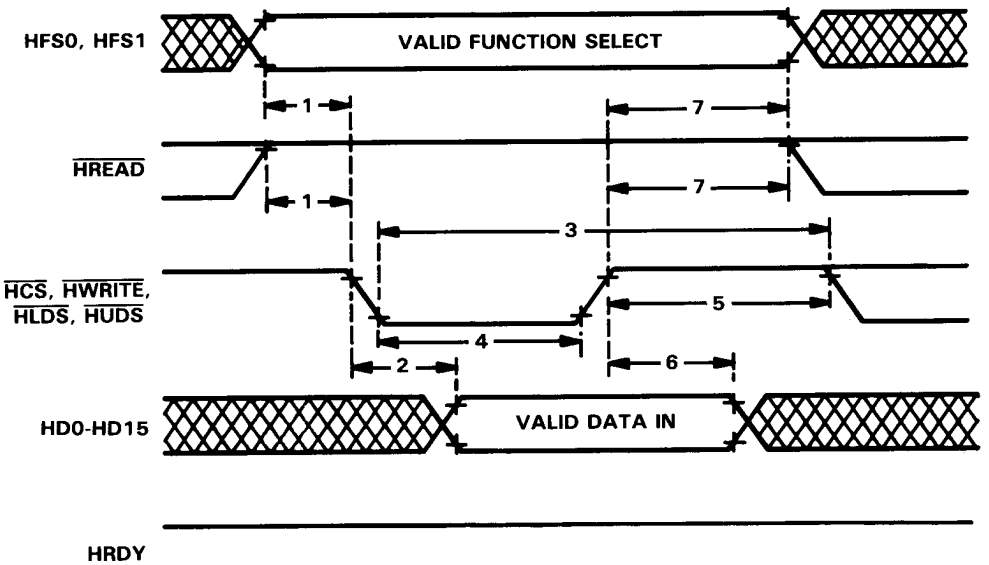
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

general comments on host interface timing

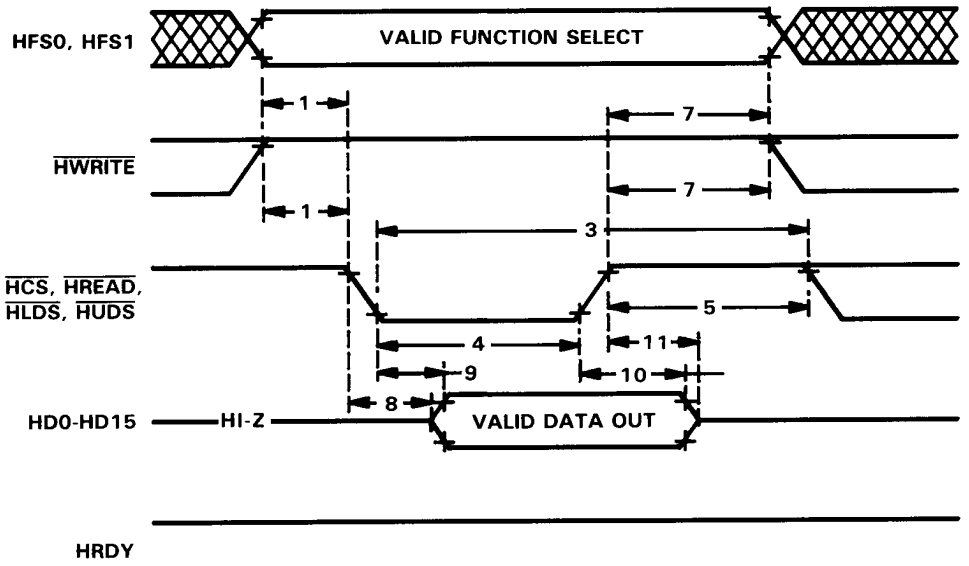
The following general comments apply to host interface timing:

1. The HRDY signal is enabled by an active-low level on the $\overline{\text{HCS}}$ input. When $\overline{\text{HCS}}$ is inactive-high, HRDY is forced high regardless of the internal state of the device. Low-going transient pulses on $\overline{\text{HCS}}$ may result in low-going transient pulses on HRDY, but otherwise have no effect unless accompanied by active levels on other control signals.
2. A host interface write cycle occurs when $\overline{\text{HCS}}$, $\overline{\text{HWRITE}}$, and $\overline{\text{HLDS}}$ are low, or when $\overline{\text{HCS}}$, $\overline{\text{HWRITE}}$, and $\overline{\text{HUDS}}$ are low. In either case, the last of the three signals to make the high-to-low transition is the strobe that begins the cycle. The first of the three signals to make the low-to-high transition ends the cycle. Similarly, a host interface read cycle occurs when $\overline{\text{HCS}}$, $\overline{\text{HREAD}}$, and $\overline{\text{HLDS}}$ are low, or when $\overline{\text{HCS}}$, $\overline{\text{HREAD}}$, and $\overline{\text{HUDS}}$ are low. In either case, the last of the three signals to make the high-to-low transition is the strobe that begins the cycle. The first of the three signals to make the low-to-high transition ends the cycle. All access times are specified with respect to the strobing edges that begin and end the cycle.
3. During a host interface read or write, $\overline{\text{HWRITE}}$ and $\overline{\text{HREAD}}$ must not be active-low simultaneously.

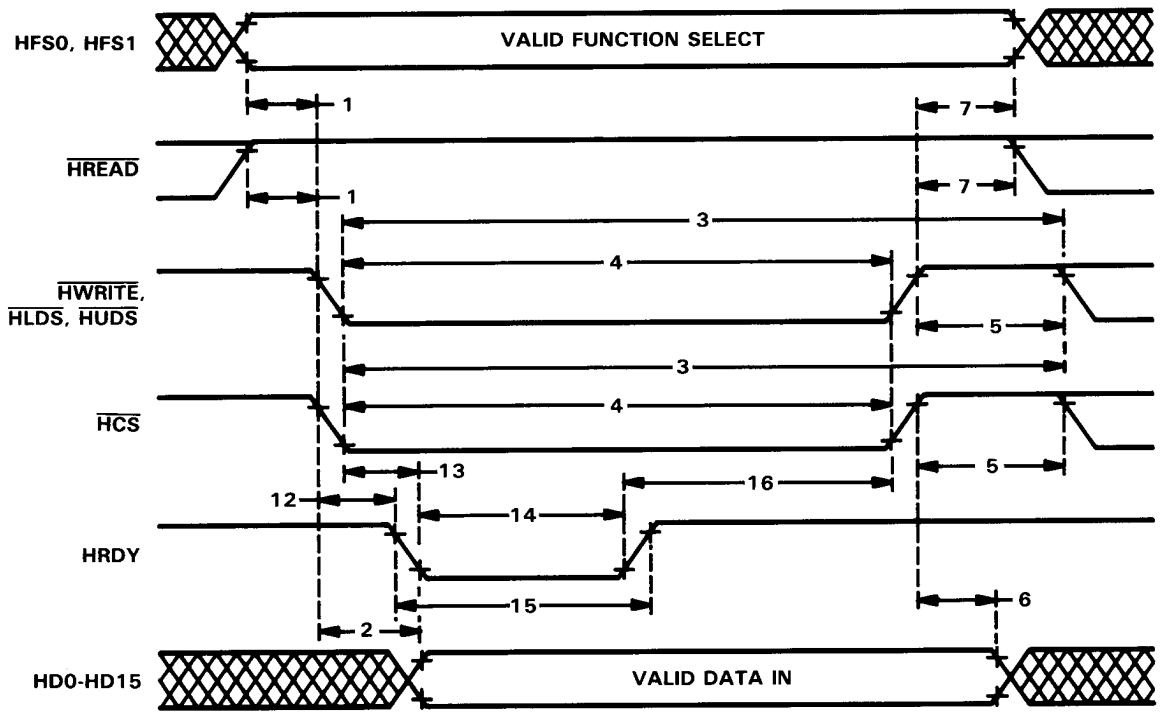
host interface timing: write cycle with no wait



host interface timing: read cycle with no wait

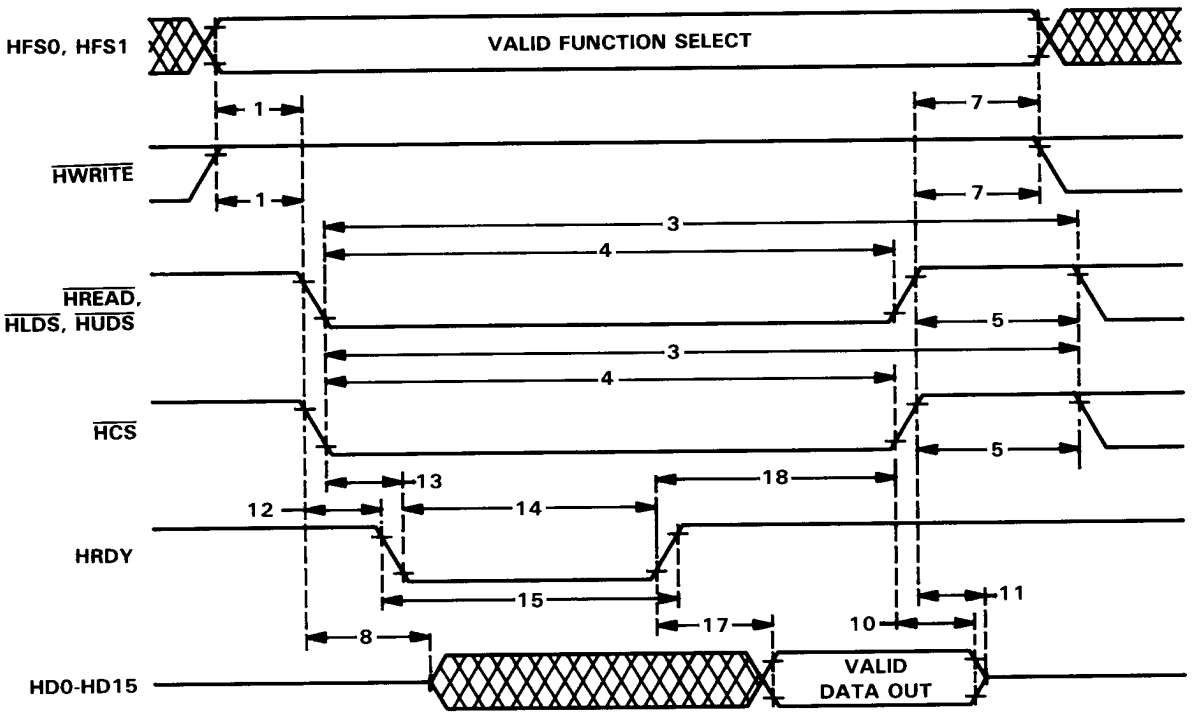


host interface timing: write cycle with wait



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

host interface timing: read cycle with wait



reset timing

The timing parameters for device reset are shown in the next two figures. The purpose of these figures is to quantify the timing relationships among the $\overline{\text{RESET}}$, $\overline{\text{HCS}}$, and LCLK1 signals. $\overline{\text{RESET}}$ and $\overline{\text{HCS}}$ are asynchronous inputs that are internally synchronized by latches internal to the GSP. The timing relationships specified for these signals relative to LCLK1 need be met only to guarantee recognition of a transition of one of these signals at a particular clock edge. The explanation of the logical relationships among signals will be found in the *TMS34010 User's Guide*.

Quarter clock time t_Q which appears in the following table, is one quarter of a local output clock period, or twice the input clock period, $t_{c(ICK)}$.

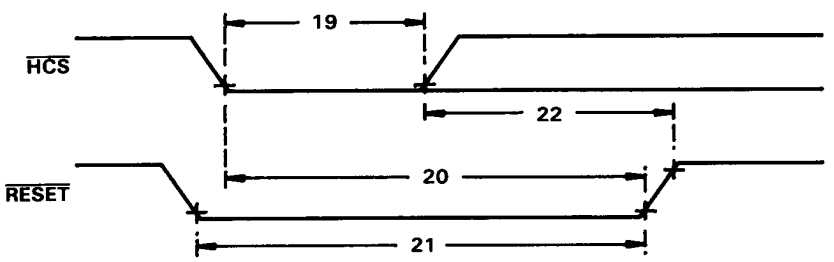
NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
19	$t_{w(CSL)}$	Duration of $\overline{\text{HCS}}$ low to configure GSP to run in self-bootstrap mode	$4t_Q+55$		$4t_Q+55$		ns
20	$t_{su(CSL-REH)}$	Setup time of $\overline{\text{HCS}}$ low to $\overline{\text{RESET}}\uparrow$ to configure the GSP to run in self-bootstrap mode	$8t_Q+55$		$8t_Q+55$		ns
21	$t_{w(REL)}$	Duration of $\overline{\text{RESET}}$ low to ensure that GSP is properly reset	$160t_Q-40$		$160t_Q-40$		ns
22	$t_{d(CSH-REH)}$	Delay from $\overline{\text{HCS}}\uparrow$ to $\overline{\text{RESET}}$ high, end of reset, to configure GSP to run in self-bootstrap mode		$4t_Q-50$†		$4t_Q-50$†	ns
23	$t_{su(REV-CK1L)}$	Setup time of $\overline{\text{RESET}}$ valid to LCLK1↓ to guarantee recognition at a particular clock edge	40‡		40‡		ns
24	$t_{h(CK1L-REV)}$	Hold time of $\overline{\text{RESET}}$ valid after LCLK1 low to guarantee recognition at a particular clock edge	10‡		10‡		ns
25	$t_{su(CSV-CK1L)}$	Setup time of $\overline{\text{HCS}}$ valid to LCLK1↓ to guarantee recognition at a particular clock edge	40‡		40‡		ns
26	$t_{h(CK1L-CSV)}$	Hold time of $\overline{\text{HCS}}$ valid after LCLK1 low to guarantee recognition at a particular clock edge	10‡		10‡		ns

NOTE: Advance information notices apply only to the TMS34010-50.

†Parameter 22 is the maximum amount by which the $\overline{\text{RESET}}$ low-to-high transition can be delayed after the $\overline{\text{HCS}}$ low-to-high transition and still guarantee that the GSP is configured to run in self-bootstrap mode (HLT bit = 0) following the end of reset. $\overline{\text{HCS}}$ may be held low for some time past the low-to-high $\overline{\text{RESET}}$ transition, and will be ignored by the GSP for 17 local clock periods following the clock edge at which the low-to-high $\overline{\text{RESET}}$ transition is detected. Following completion of the eight $\overline{\text{RAS}}$-only cycles that automatically follow reset, however, a low $\overline{\text{HCS}}$ level will be interpreted as a chip select.

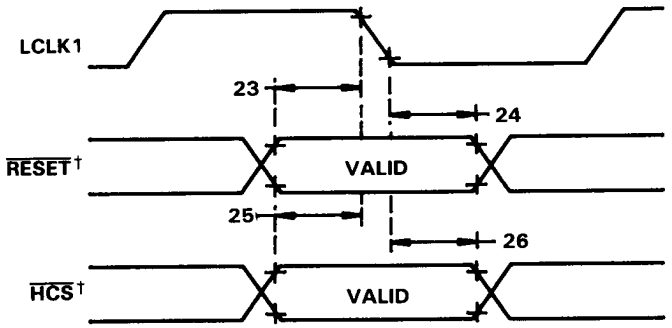
‡$\overline{\text{RESET}}$ and $\overline{\text{HCS}}$ are asynchronous inputs. The specified setup and hold times of these signals with respect to the high-to-low transition of LCLK1 need be met only to guarantee that a transition of $\overline{\text{RESET}}$ or $\overline{\text{HCS}}$ is detected by the device at a particular clock edge.

reset: asynchronous timing relationships



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

reset: synchronous timing relationships



†$\overline{\text{RESET}}$ and $\overline{\text{HCS}}$ are asynchronous inputs. The specified setup and hold times of $\overline{\text{RESET}}$ or $\overline{\text{HCS}}$ with respect to the high-to-low LCLK1 transition must be met only to guarantee that a $\overline{\text{RESET}}$ or $\overline{\text{HCS}}$ transition is detected by the device at a particular clock edge.

local bus timing parameters

The following six figures show the timing parameters for the signals of the local memory interface bus, often simply referred to as the local bus. The purpose of these figures and the accompanying tables is to quantify the timing relationships among the various signals. The explanation of the logical relationships among signals will be found in the *TMS34010 User's Guide* (number SPVU001).

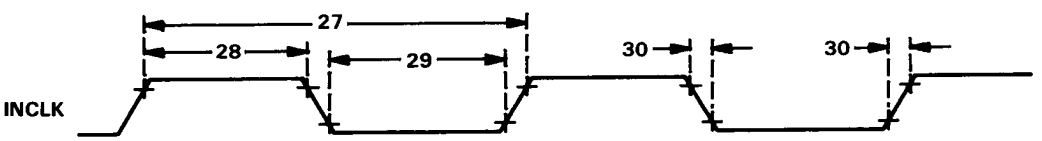
A number of parameter values are expressed in terms of quarter clock time t_Q, which is one quarter of a local clock period, or twice the input clock period, $t_{c(ICK)}$.

Input clock INCLK is divided internally by 8 to produce output clocks LCLK1 and LCLK2. Transitions of the other local interface output signals are also generated as delays from INCLK transitions. The divide-down logic that converts INCLK to the internal clocks used to generate LCLK1 and LCLK2 introduces significant propagation delays from the transitions of INCLK to the corresponding transitions of LCLK1 and LCLK2. While the frequency of INCLK is precisely eight times the frequency of LCLK1 or LCLK2, no timing relationship other than the frequency is specified between transitions of input clock INCLK and transitions of the output clocks LCLK1 and LCLK2.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
27	$t_{c(ICK)}$	Period of INCLK	25		20		ns
28	$t_{w(ICKH)}$	Pulse duration of INCLK high	8		6		ns
29	$t_{w(ICKL)}$	Pulse duration of INCLK low	8		6		ns
30	$t_{t(ICK)}$	Transition time (rise and fall) of INCLK	2†	8†	2†	8†	ns

NOTE: Advance information notices apply only to the TMS34010-50.
†These values are based on computer simulation, and are not tested.

local bus timing: input clock



ADVANCE INFORMATION

local bus timing parameters (continued)

Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock period, or $2t_{c(ICK)}$.

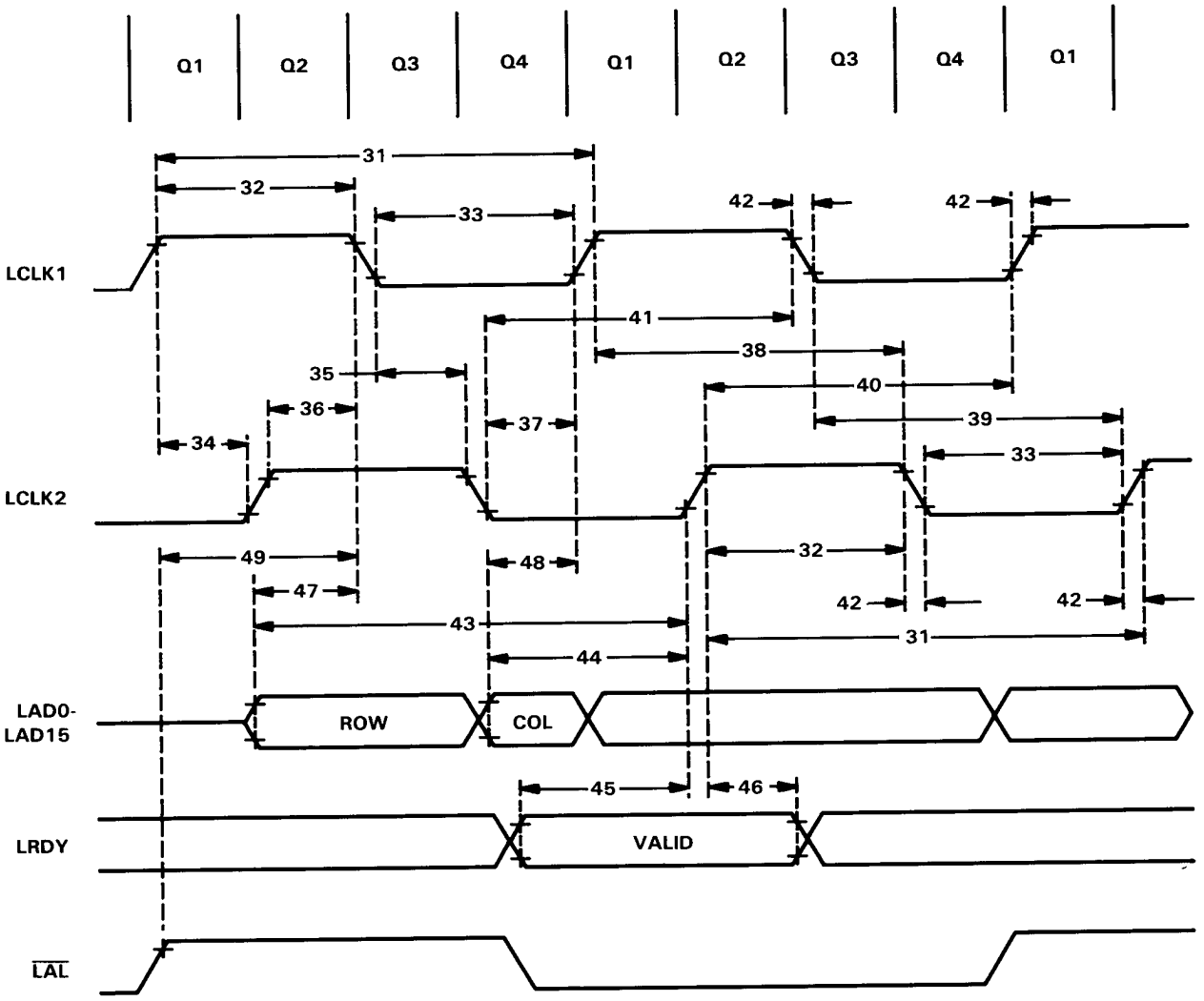
NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
31	$t_{c(CK)}$	Period of local clocks LCLK1 and LCLK2	$8t_{c(ICK)}$ †		$8t_{c(ICK)}$ †		ns
32	$t_{w(CKH)}$	Pulse duration of local clock high	$2t_Q-10$		$2t_Q-10$		ns
33	$t_{w(CKL)}$	Pulse duration of local clock low	$2t_Q-10$		$2t_Q-10$		ns
34	$t_{h(CK1H-CK2L)}$	Hold time of LCLK2 low after LCLK1 high	t_Q-10		t_Q-10		ns
35	$t_{h(CK1L-CK2H)}$	Hold time of LCLK2 high after LCLK1 low	t_Q-10		t_Q-10		ns
36	$t_{h(CK2H-CK1H)}$	Hold time of LCLK1 high after LCLK2 high	t_Q-10		t_Q-10		ns
37	$t_{h(CK2L-CK1L)}$	Hold time of LCLK1 low after LCLK2 low	t_Q-10		t_Q-10		ns
38	$t_{h(CK1H-CK2H)}$	Hold time of LCLK2 high after LCLK1 high	$3t_Q-10$		$3t_Q-10$		ns
39	$t_{h(CK1L-CK2L)}$	Hold time of LCLK2 low after LCLK1 low	$3t_Q-10$		$3t_Q-10$		ns
40	$t_{h(CK2H-CK1L)}$	Hold time of LCLK1 low after LCLK2 high	$3t_Q-10$		$3t_Q-10$		ns
41	$t_{h(CK2L-CK1H)}$	Hold time of LCLK1 high after LCLK2 low	$3t_Q-10$		$3t_Q-10$		ns
42	t_t	Transition time (rise and fall) of LCLK1 or LCLK2		10		10	ns
43	$t_{su(RAV-CK2H)}$	Setup time of row address valid to LCLK2↑	$4t_Q-25$		$4t_Q-10$		ns
44	$t_{su(CAV-CK2H)}$	Setup time of column address valid to LCLK2↑	$2t_Q-25$		$2t_Q-10$		ns
45	$t_{su(LRV-CK2H)}$	Setup time of LRDY valid to LCLK2↑	30		30		ns
46	$t_{h(CK2H-LRV)}$	Hold time of LRDY valid after LCLK2 high	0		0		ns
47	$t_{su(RAV-CK1L)}$	Setup time of row address valid to LCLK1↓	t_Q-25		t_Q-10		ns
48	$t_{su(CAV-CK1H)}$	Setup time of column address valid to LCLK1↑	t_Q-25		t_Q-10		ns
49	$t_{su(ALH-CK1L)}$	Setup time of $\overline{LAL}$ high to LCLK1↓	$2t_Q-20$		$2t_Q-10$		ns

NOTE: Advance information notices apply only to the TMS34010-50.
†This is a functional minimum and is not tested. This parameter can also be specified as $4t_Q$.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

local bus timing: output clock and LRDY signal



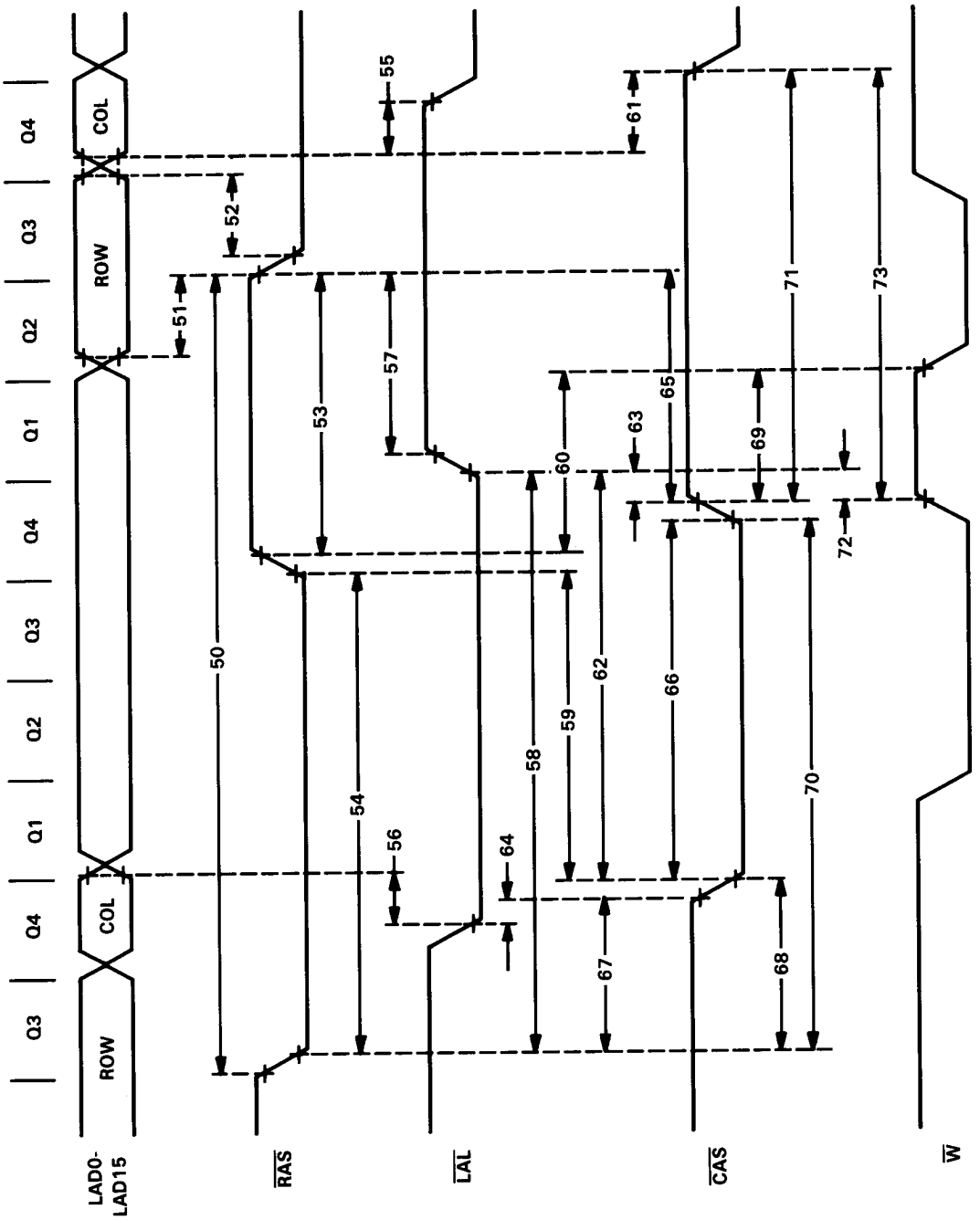
NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
50	$t_{d(RL-RL)}$	Delay from $\overline{RAS}\downarrow$ to $\overline{RAS}\downarrow$	$8t_Q$†		$8t_Q$†		ns
51	$t_{su(RAV-RL)}$	Setup time of row address valid to $\overline{RAS}\downarrow$	t_Q-20		t_Q-10		ns
52	$t_{h(RL-RAV)}$	Hold time of row address valid after $\overline{RAS}$ low	t_Q-20		t_Q-10		ns
53	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	$3t_Q-20$		$3t_Q-10$		ns
54	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	$5t_Q-20$		$5t_Q-10$		ns
55	$t_{su(CAV-ALL)}$	Setup time of column address valid to $\overline{LAL}\downarrow$	$0.5t_Q-20$		$0.5t_Q-10$		ns
56	$t_{h(ALL-CAV)}$	Hold time of column address valid after $\overline{LAL}$ low	$0.5t_Q-15$		$0.5t_Q-10$		ns
57	$t_{h(ALH-RH)}$	Hold time of $\overline{RAS}$ high after $\overline{LAL}$ high	$2t_Q-20$		$2t_Q-10$		ns
58	$t_{h(RL-ALL)}$	Hold time of $\overline{LAL}$ low after $\overline{RAS}$ low	$6t_Q-20$		$6t_Q-10$		ns
59	$t_{h(CL-RL)}$	Hold time of $\overline{RAS}$ low after $\overline{CAS}$ low	$3t_Q-20$		$3t_Q-10$		ns
60	$t_{h(RH-WH)}$	Hold time of $\overline{W}$ high after $\overline{RAS}$ high, shift register transfer follows read	$2t_Q-20$		$2t_Q-10$		ns
61	$t_{su(CAV-CL)}$	Setup time of column address valid to $\overline{CAS}\downarrow$	t_Q-20		t_Q-10		ns
62	$t_{h(CL-ALL)}$	Hold time of $\overline{LAL}$ low after $\overline{CAS}$ low	$4t_Q-20$		$4t_Q-10$		ns
63	$t_{h(CH-ALL)}$	Hold time of $\overline{LAL}$ low after $\overline{CAS}$ high, write cycle	$0.5t_Q-15$		$0.5t_Q-10$		ns
64	$t_{h(ALL-CH)}$	Hold time of $\overline{CAS}$ high after $\overline{LAL}$ low	$0.5t_Q-15$		$0.5t_Q-10$		ns
65	$t_{h(CH-RH)}$	Hold time of $\overline{RAS}$ high after $\overline{CAS}$ high	$2.5t_Q-15$		$2.5t_Q-10$		ns
66	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	$3.5t_Q-25$		$3.5t_Q-10$		ns
67	$t_{h(RL-CH)}$	Hold time of $\overline{CAS}$ high after $\overline{RAS}$ low	$2t_Q-20$		$2t_Q-10$		ns
68	$t_{d(RL-CL)}$	Delay time from $\overline{RAS}$ low to $\overline{CAS}$ low		$2t_Q+20$		$2t_Q+10$	ns
69	$t_{h(CH-WH)}$	Hold time of $\overline{W}$ high after $\overline{CAS}$ high, shift register transfer follows read	$1.5t_Q-15$		$1.5t_Q-10$		ns
70	$t_{h(RL-CL)}$	Hold time $\overline{CAS}$ low after $\overline{RAS}$ low	$5.5t_Q-25$		$5.5t_Q-10$		ns
71	$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	$4.5t_Q-15$		$4.5t_Q-10$		ns
72	$t_{h(WH-ALL)}$	Hold time of $\overline{LAL}$ low after $\overline{W}$ high, write cycle	$0.5t_Q-15$		$0.5t_Q-10$		ns
73	$t_{su(WH-CL)}$	Setup time of $\overline{W}$ high to $\overline{CAS}\downarrow$, end of write	$4.5t_Q-15$		$4.5t_Q-10$		ns

NOTE: Advance information notices apply only to the TMS34010-50.

†This is a functional minimum and is not tested.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

local bus timing: the $\overline{RAS}$, $\overline{CAS}$, and $\overline{LAL}$ outputs



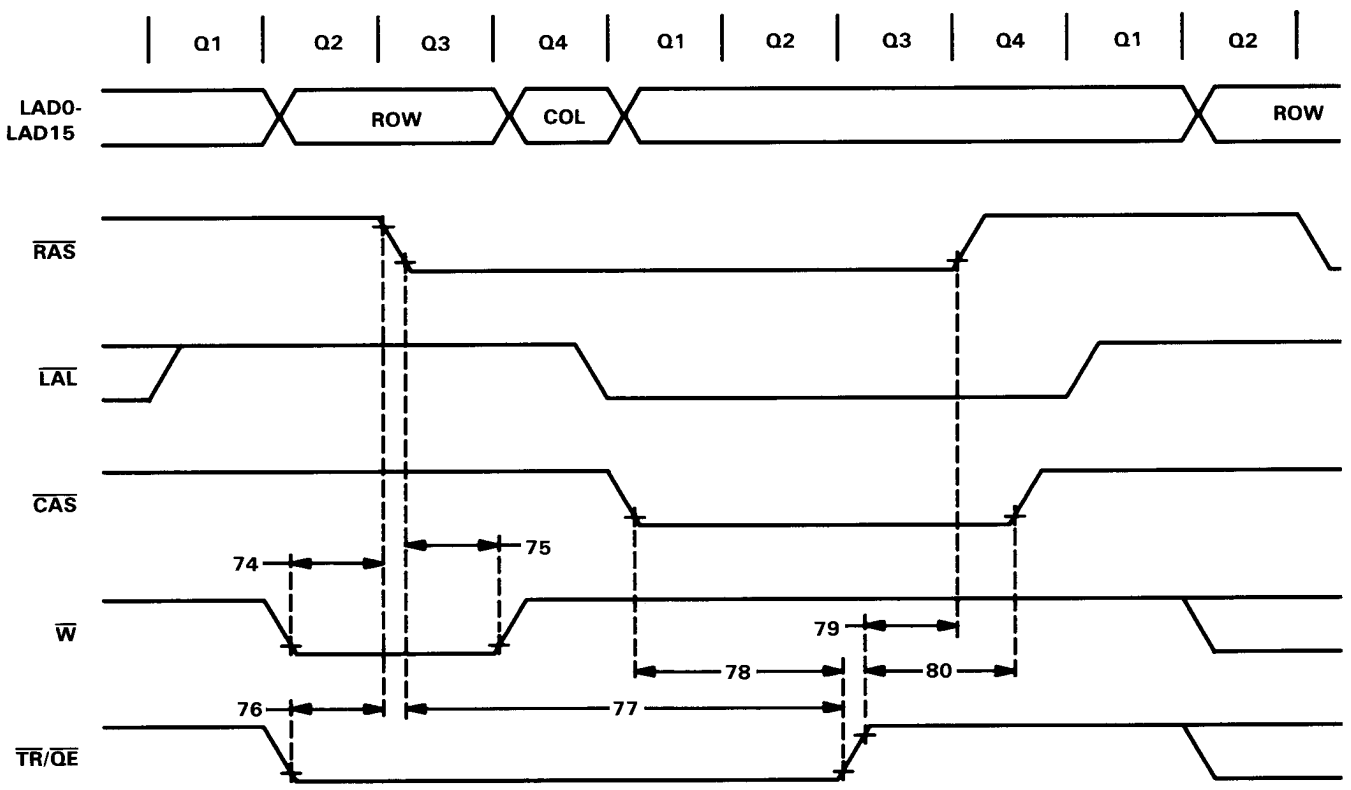
local bus timing parameters (continued)

Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock period, or $2t_{c(ICK)}$.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
74	$t_{su(WL-RL)}$	Setup time of $\overline{W}$ low to $\overline{RAS}\downarrow$, shift register transfer cycle	t_Q-20		t_Q-10		ns
75	$t_{h(RL-WL)}$	Hold time of $\overline{W}$ low after $\overline{RAS}$ low, shift register transfer cycle	t_Q-20		t_Q-10		ns
76	$t_{su(TRL-RL)}$	Setup time of $\overline{TR}/\overline{QE}$ low to $\overline{RAS}\downarrow$, shift register transfer cycle	t_Q-20		t_Q-10		ns
77	$t_{h(RL-TRL)}$	Hold time of $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ low, shift register transfer cycle	$4t_Q-20$		$4t_Q-10$		ns
78	$t_{h(CL-TRL)}$	Hold time of $\overline{TR}/\overline{QE}$ low after $\overline{CAS}$ low, shift register transfer cycle	$2t_Q-20$		$2t_Q-10$		ns
79	$t_{su(TRH-RH)}$	Setup time of $\overline{TR}/\overline{QE}$ high to $\overline{RAS}\uparrow$, shift register transfer cycle	t_Q-20		t_Q-10		ns
80	$t_{su(TRH-CH)}$	Setup time of $\overline{TR}/\overline{QE}$ high to $\overline{CAS}\uparrow$, shift register transfer cycle	$1.5t_Q-25$		$1.5t_Q-10$		ns

NOTES: 1. Advance information notices apply only to the TMS34010-50.
2. Parameters 81 and 82 intentionally omitted.

local bus timing parameters: shift register transfer cycle



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

local bus timing parameters (continued)

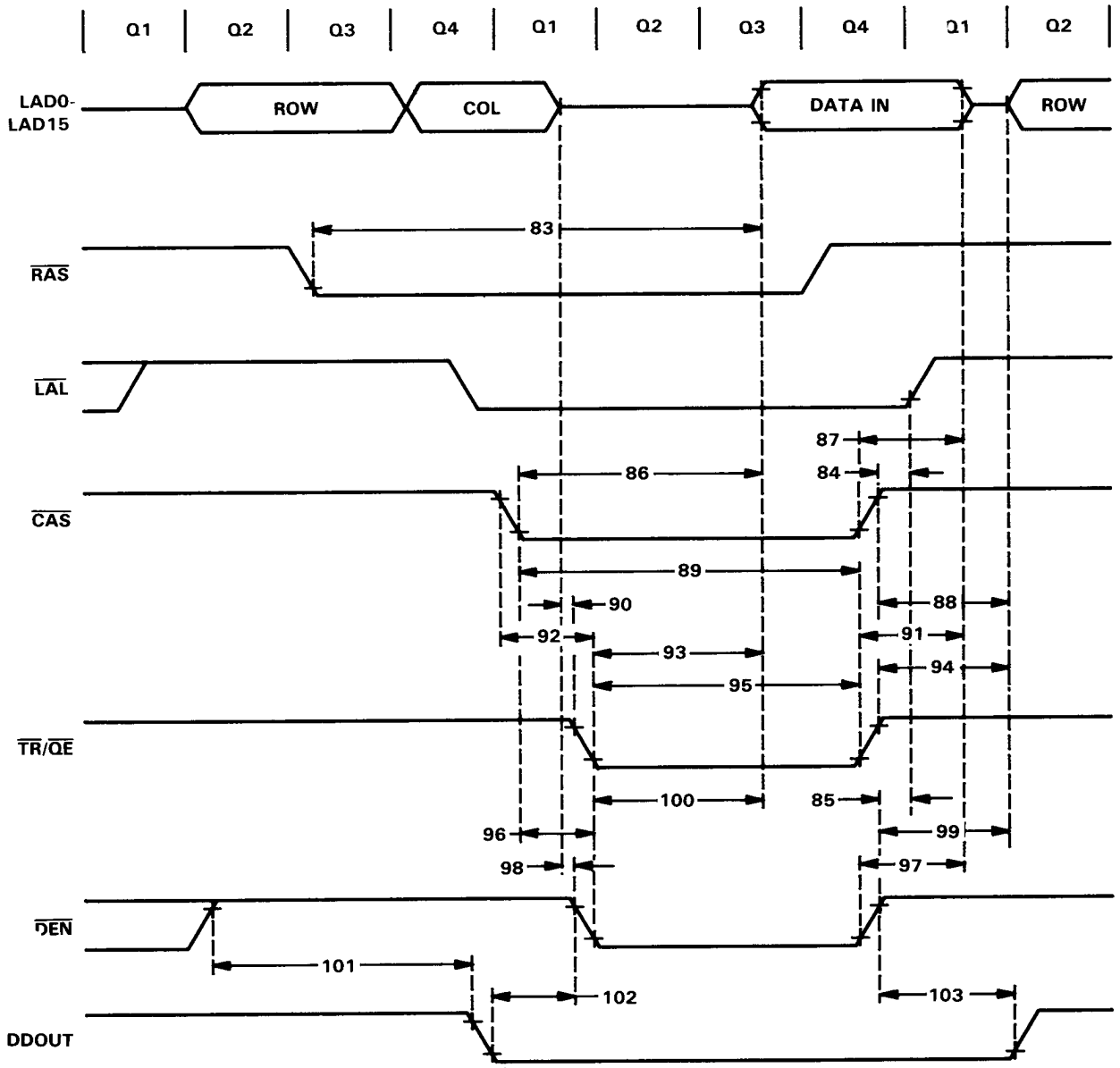
Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock period, or $2t_{c(ICK)}$.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
83	$t_{a(RL-DV)}$	Access time from $\overline{RAS}$ low to data in valid, read cycle		$5.5t_Q-40^\dagger$		$5.5t_Q-25^\dagger$	ns
84	$t_{su(CH-ALH)}$	Setup time of $\overline{CAS}$ high to $\overline{LAL}\uparrow$	$0.5t_Q-15$		$0.5t_Q-10$		ns
85	$t_{su(ENH-ALH)}$	Setup time of $\overline{DEN}$ high to $\overline{LAL}\uparrow$	$0.5t_Q-15$		$0.5t_Q-10$		ns
86	$t_{a(CL-DV)}$	Access time from $\overline{CAS}$ low to data in valid, read cycle		$3.5t_Q-40^\dagger$		$3.5t_Q-25^\dagger$	ns
87	$t_{h(CH-DV)}$	Hold time of data in valid after $\overline{CAS}\uparrow$, read cycle	0		0		ns
88	$t_{h(CH-RAZ)}$	Hold time of row address high impedance after $\overline{CAS}$ high, end of read cycle	$1.5t_Q-10^\ddagger$		$1.5t_Q-10^\ddagger$		ns
89	$t_{h(CL-QEL)}$	Hold time of $\overline{TR}/\overline{QE}$ low after $\overline{CAS}$ low, read cycle	$3.5t_Q-25$		$3.5t_Q-10$		ns
90	$t_{su(CAZ-QEL)}$	Setup time of column address high impedance to $\overline{TR}/\overline{QE}\downarrow$, read cycle	$t_Q-10^\ddagger$		$t_Q-10^\ddagger$		ns
91	$t_{h(QEH-DV)}$	Hold time of data in valid after $\overline{TR}/\overline{QE}\uparrow$, read cycle	0		0		ns
92	$t_{d(CL-QEL)}$	Delay time from $\overline{CAS}\downarrow$ to $\overline{TR}/\overline{QE}$ low, read cycle		t_Q+20		t_Q+10	ns
93	$t_{a(QEL-DV)}$	Access time from $\overline{TR}/\overline{QE}$ low to data in valid, read cycle		$2.5t_Q-40^\dagger$		$2.5t_Q-25^\dagger$	ns
94	$t_{h(QEH-RAZ)}$	Hold time of row address high impedance after $\overline{TR}/\overline{QE}$ high, end of read cycle	$1.5t_Q-10^\ddagger$		$1.5t_Q-10^\ddagger$		ns
95	$t_{w(QEL)}$	Pulse duration, $\overline{TR}/\overline{QE}$ low, read cycle	$2.5t_Q-10$		$2.5t_Q-10$		ns
96	$t_{d(CL-ENL)}$	Delay time from $\overline{CAS}$ low to $\overline{DEN}$ low, read cycle		t_Q+20		t_Q+10	ns
97	$t_{h(ENH-DV)}$	Hold time of data in valid after $\overline{DEN}\uparrow$, read cycle	0		0		ns
98	$t_{su(CAZ-ENL)}$	Setup time of column address high impedance to $\overline{DEN}\downarrow$, read cycle	$t_Q-10^\ddagger$		$t_Q-10^\ddagger$		ns
99	$t_{h(ENH-RAZ)}$	Hold time of next row address high impedance after $\overline{DEN}$ high, end of read cycle	$1.5t_Q-10^\ddagger$		$1.5t_Q-10^\ddagger$		ns
100	$t_{a(ENL-DV)}$	Access time from $\overline{DEN}$ low to data in valid, read cycle		$2.5t_Q-40^\dagger$		$2.5t_Q-25^\dagger$	ns
101	$t_{h(ENH-DDH)}$	Hold time of DDOUT high after $\overline{DEN}$ high, read follows write cycle	$3t_Q-20$		$3t_Q-10$		ns
102	$t_{su(DDL-ENL)}$	Setup time of DDOUT low to $\overline{DEN}\downarrow$, read cycle	t_Q-20		t_Q-10		ns
103	$t_{h(ENH-DDL)}$	Hold time of DDOUT low after $\overline{DEN}$ high, read cycle	$1.5t_Q-15$		$1.5t_Q-10$		ns

NOTE: Advance information notices apply only to the TMS34010-50.
$^\dagger 4t_Q$ is added to these values for each wait state inserted.
‡These values are derived from characterization and are not tested.

ADVANCE INFORMATION

local bus timing: read cycle



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

local bus timing parameters (continued)

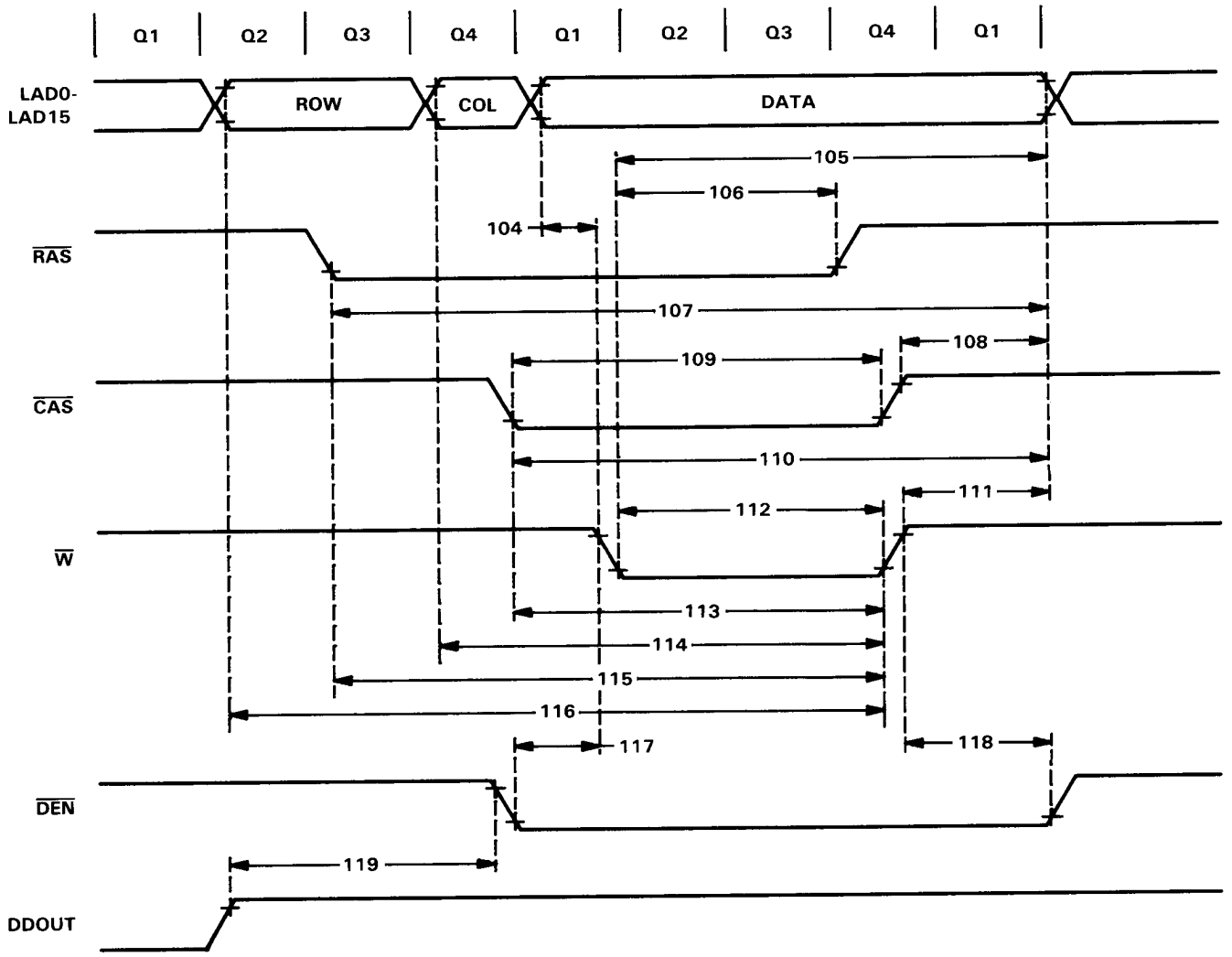
Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock period, or $2t_{c(ICK)}$.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
104	$t_{su(DV-WL)}$	Setup time of data out valid to $\overline{W}\downarrow$, write cycle	$t_Q - 20$		$t_Q - 10$		ns
105	$t_{h(WL-DV)}$	Hold time of data out valid after $\overline{W}$ low, write cycle	$4t_Q - 20$		$4t_Q - 10$		ns
106	$t_{su(WL-RH)}$	Setup time of $\overline{W}$ low to $\overline{RAS}\uparrow$, write cycle	$2t_Q - 20$		$2t_Q - 10$		ns
107	$t_{h(RL-DV)}$	Hold time of data out valid after $\overline{RAS}$ low, write cycle	$7t_Q - 20$		$7t_Q - 10$		ns
108	$t_{h(CH-DV)}$	Hold time of data out valid after $\overline{CAS}$ high, write cycle	$1.5t_Q - 15$		$1.5t_Q - 10$		ns
109	$t_{su(WL-CH)}$	Setup time of $\overline{W}$ low to $\overline{CAS}\uparrow$, write cycle	$2.5t_Q - 25$		$2.5t_Q - 10$		ns
110	$t_{h(CL-DV)}$	Hold time of data out valid after $\overline{CAS}$ low, write cycle	$5t_Q - 20$		$5t_Q - 10$		ns
111	$t_{h(WH-DV)}$	Hold time of data out valid after $\overline{W}$ high, write cycle	$1.5t_Q - 15$		$1.5t_Q - 10$		ns
112	$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	$2.5t_Q - 25$		$2.5t_Q - 10$		ns
113	$t_{h(CL-WL)}$	Hold time of $\overline{W}$ low after $\overline{CAS}$ low, write cycle	$3.5t_Q - 25$		$3.5t_Q - 10$		ns
114	$t_{su(CAV-WH)}$	Setup time of column address valid to $\overline{W}\uparrow$, write cycle	$4.5t_Q - 30$		$4.5t_Q - 10$		ns
115	$t_{h(RL-WL)}$	Hold time of $\overline{W}$ low after $\overline{RAS}$ low, write cycle	$5.5t_Q - 25$		$5.5t_Q - 10$		ns
116	$t_{su(RAV-WH)}$	Setup time of row address valid to $\overline{W}\uparrow$, write cycle	$6.5t_Q - 35$		$6.5t_Q - 15$		ns
117	$t_{su(ENL-WH)}$	Setup time of $\overline{DEN}$ low to $\overline{W}$ high, write cycle	$t_Q - 20$		$t_Q - 10$		ns
118	$t_{h(WH-ENL)}$	Hold time of $\overline{DEN}$ low after $\overline{W}$ high, write cycle	$1.5t_Q - 15$		$1.5t_Q - 10$		ns
119	$t_{su(DDH-ENL)}$	Setup time of DDOUT high to $\overline{DEN}\uparrow$, write follows read	$3t_Q - 20$		$3t_Q - 10$		ns

NOTE: Advance information notices apply only to the TMS34010-50.

ADVANCE INFORMATION

local bus timing: write cycle



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

local bus timing parameters (continued)

Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock period, or $2t_{c(ICK)}$.

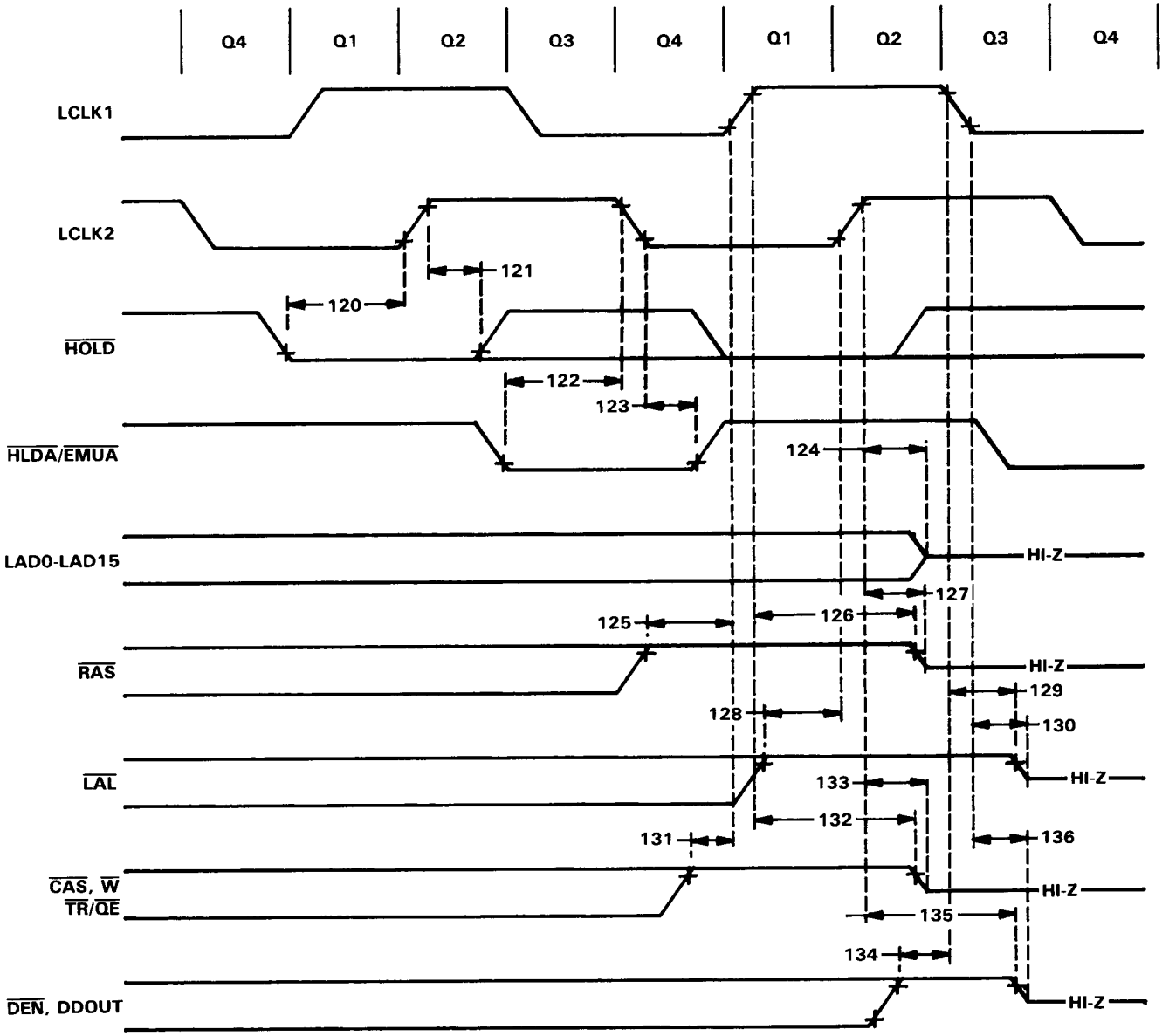
NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
120	$t_{su(HRV-CK2H)}$	Setup time of $\overline{HOLD}$ valid to LCLK2↑	50		50		ns
121	$t_{h(CK2H-HRV)}$	Hold time of $\overline{HOLD}$ valid after LCLK2 high	0		0		ns
122	$t_{su(HKV-CK2L)}$	Setup time of $\overline{HLDA}/\overline{EMUA}$ output valid before LCLK2↓	t_Q-20		t_Q-10		ns
123	$t_{h(CK2L-HKL)}$	Hold time of $\overline{HLDA}/\overline{EMUA}$ low, after LCLK2 low	t_Q-15		t_Q-10		ns
124	$t_{d(CK2H-DZ)}$	Delay from LCLK2 high to LAD pins high impedance, bus release		30†		30†	ns
125	$t_{su(RH-CK1H)}$	Setup time of $\overline{RAS}$ high to LCLK1↑	t_Q-20		t_Q-10		ns
126	$t_{h(CK1H-RH)}$	Hold time of $\overline{RAS}$ driven high after LCLK1 high, bus release	t_Q-10†		t_Q-10†		ns
127	$t_{d(CK2H-RZ)}$	Delay from LCLK2 high to $\overline{RAS}$ high impedance, bus release		30†		30†	ns
128	$t_{su(ALH-CK2H)}$	Setup time of $\overline{LAL}$ high to LCLK2↑	t_Q-20		t_Q-10		ns
129	$t_{h(CK1L-ALH)}$	Hold time of $\overline{LAL}$ driven high after LCLK1↓, bus release	0†		0†		ns
130	$t_{d(CK1L-ALZ)}$	Delay from LCLK1 low to $\overline{LAL}$ high impedance, bus release		30†		30†	ns
131	$t_{su(CH-CK1H)}$	Setup time of $\overline{CAS}$, $\overline{W}$, and $\overline{TR}/\overline{QE}$ high to LCLK↑	$0.5t_Q-15$		$0.5t_Q-10$		ns
132	$t_{h(CK1H-CH)}$	Hold time of $\overline{CAS}$, $\overline{W}$ and $\overline{TR}/\overline{QE}$ high after LCLK1 high, bus release	t_Q-10†		t_Q-10†		ns
133	$t_{d(CK2H-CZ)}$	Delay from LCLK2 high to $\overline{CAS}$, $\overline{W}$ and $\overline{TR}/\overline{QE}$ high impedance, bus release		30†		30†	ns
134	$t_{su(ENH-CK2H)}$	Setup time of $\overline{DEN}$ or DDOUT high to LCLK1↓	t_Q-20		t_Q-10		ns
135	$t_{h(CK2H-ENH)}$	Hold time of $\overline{DEN}$ and DDOUT high after LCLK1↓, bus release	t_Q-10†		t_Q-10†		ns
136	$t_{d(CK1L-ENZ)}$	Delay from LCLK1 low to $\overline{DEN}$ and DDOUT high impedance, bus release		30†		30†	ns
137	$t_{h(CK2H-DZ)}$	Hold time of LAD bus high impedance after LCLK2↑	0†		0†		ns
138	$t_{h(CK2H-RZ)}$	Hold time of $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{LAL}$, and $\overline{TR}/\overline{QE}$ high impedance after LCLK1↑	0†		0†		ns
139	$t_{d(CK1H-RH)}$	Delay from LCLK1 high to RAS, $\overline{CAS}$, $\overline{W}$, $\overline{LAL}$, and $\overline{TR}/\overline{QE}$ driven high, resume bus control		30		30	ns
140	$t_{h(CK2H-RH)}$	Hold time of $\overline{RAS}$ high after LCLK2 high, resumes bus control	t_Q-15		t_Q-10		ns
141	$t_{h(CK2H-CH)}$	Hold time of $\overline{CAS}$, $\overline{W}$, and $\overline{TR}/\overline{QE}$ high after LCLK2 high, resume bus control	0†		0†		ns
142	$t_{h(CK2H-ENZ)}$	Hold time of $\overline{DEN}$, DDOUT high impedance after LCLK2 high, resume bus control	0†		0†		ns

NOTE: Advance information notices apply only to the TMS34010-50.

†These values are derived from characterization and are not tested.

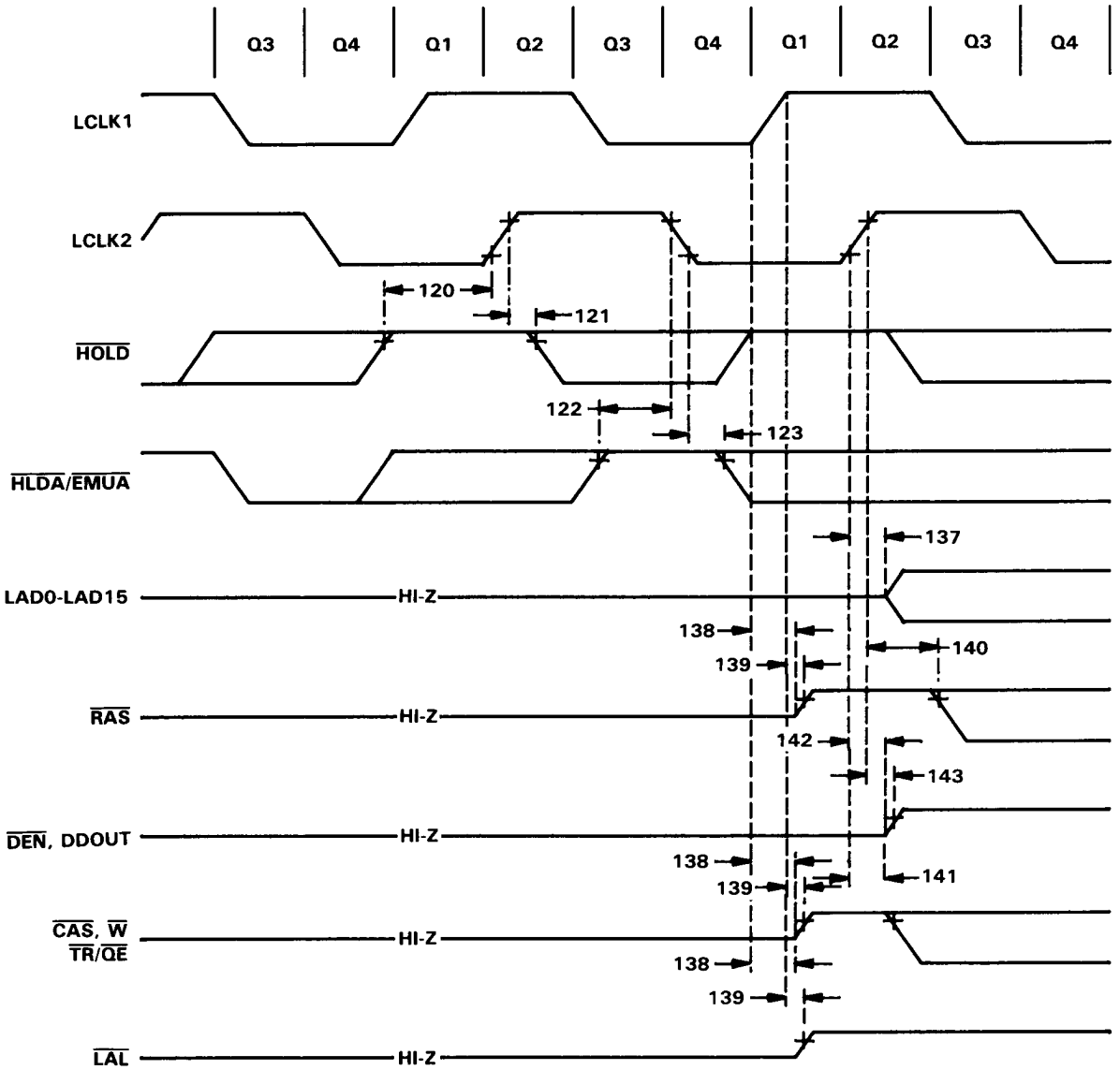
ADVANCE INFORMATION

GSP releases control of local bus



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

GSP resumes control of local bus



local bus timing parameters (continued)

Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock cycle, or $2t_{c(ICK)}$.

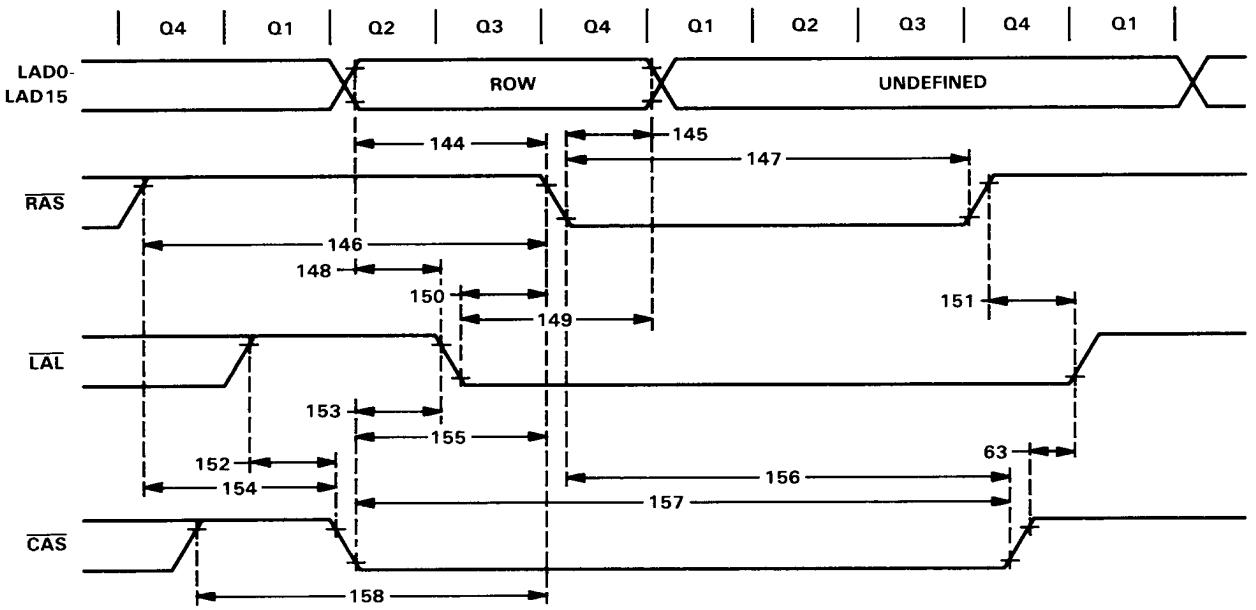
NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
143	$t_{d(CK2H-ENH)}$	Delay from LCLK2 high to $\overline{DEN}$, and DDOUT driven high, resume bus control		30		30	ns
144	$t_{su(RAV-RL)}$	Setup time of row address valid to $\overline{RAS}\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$2t_Q-25$		$2t_Q-10$		ns
145	$t_{h(RL-RAV)}$	Hold time of row address valid after $\overline{RAS}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
146	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high, start of $\overline{CAS}$-before-$\overline{RAS}$ refresh	$4t_Q-20$		$4t_Q-10$		ns
147	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$4t_Q-20$		$4t_Q-10$		ns
148	$t_{su(RAV-ALL)}$	Setup time of row address valid to LAL$\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
149	$t_{h(ALL-RAV)}$	Hold time of row address valid after $\overline{LAL}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$2t_Q-20$		$2t_Q-10$		ns
150	$t_{h(ALL-RH)}$	Hold time of $\overline{RAS}$ high after $\overline{LAL}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
151	$t_{su(RH-ALH)}$	Setup time of $\overline{RAS}$ high to $\overline{LAL}\uparrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
152	$t_{su(ALH-CL)}$	Setup time of $\overline{LAL}$ high to $\overline{CAS}\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
153	$t_{su(CL-ALL)}$	Setup time of $\overline{CAS}$ low to $\overline{LAL}\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
154	$t_{su(RH-CL)}$	Setup time of $\overline{RAS}$ high to $\overline{CAS}\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$2t_Q-20$		$2t_Q-10$		ns
155	$t_{su(CL-RL)}$	Setup time of $\overline{CAS}$ low to $\overline{RAS}\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$2t_Q-20$		$2t_Q-10$		ns
156	$t_{h(RL-CL)}$	Hold time of $\overline{CAS}$ low after $\overline{RAS}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$4.5t_Q-25$		$4.5t_Q-10$		ns
157	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$6.5t_Q-25$		$6.5t_Q-10$		ns
158	$t_{su(CH-RL)}$	Setup time of $\overline{CAS}$ high to $\overline{RAS}\downarrow$, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$3.5t_Q-15$		$3.5t_Q-10$		ns

NOTE: Advance information notices apply only to the TMS34010-50.

ADVANCE INFORMATION

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ DRAM refresh cycle timing



local bus timing parameters (continued)

Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock cycle, or $2t_{c(ICK)}$.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
159	$t_{h(CK2H-RH)}$	Hold time of $\overline{RAS}$ high after LCLK2 high, all cycles except internal and $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-15		t_Q-10		ns
160	$t_{su(RL-CK2L)}$	Setup time of $\overline{RAS}$ low to LCLK2↓, all cycles except internal and $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
161	$t_{h(CK1L-RH)}$	Hold time of $\overline{RAS}$ high after LCLK1 low, $\overline{RAS}$-before-$\overline{RAS}$ refresh	t_Q-15		t_Q-10		ns
162	$t_{su(RL-CK1H)}$	Setup time of $\overline{RAS}$ low to LCLK1↑, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
163	$t_{h(CK1L-RL)}$	Hold time of $\overline{RAS}$ low after LCLK1 low, all cycles except internal	t_Q-15		t_Q-10		ns
164	$t_{su(RH-CK1H)}$	Setup time of $\overline{RAS}$ high to LCLK1↑, all cycles except internal	t_Q-20		t_Q-10		ns
165	$t_{h(CK2L-ALH)}$	Hold time of $\overline{LAL}$ high after LCLK2 low, all cycles except internal	$0.5t_Q-15$		$0.5t_Q-10$		ns
166	$t_{su(ALL-CK1H)}$	Setup time of $\overline{LAL}$ low to LCLK1↑, all cycles except internal	$0.5t_Q-15$		$0.5t_Q-10$		ns
167	$t_{h(CK2L-ALL)}$	Hold time of $\overline{LAL}$ low after LCLK2 low, all cycles except internal	t_Q-15		t_Q-10		ns
168	$t_{su(ALH-CK2H)}$	Setup time of $\overline{LAL}$ high to LCLK2↑, all cycles except internal	t_Q-20		t_Q-10		ns
169	$t_{h(CK1H-CH)}$	Hold time of $\overline{CAS}$ high after LCLK1 high, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-15		t_Q-10		ns
170	$t_{su(CL-CK1L)}$	Setup time of $\overline{CAS}$ low to LCLK1↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
171	$t_{h(CK2L-CH)}$	Hold time of $\overline{CAS}$ high after LCLK2 low, all cycles except internal, DRAM refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-15		t_Q-10		ns
172	$t_{su(CL-CK2H)}$	Setup time of $\overline{CAS}$ low to LCLK2↑, all cycles except internal, DRAM refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns
173	$t_{h(CK2L-CL)}$	Hold time of $\overline{CAS}$ low after LCLK2 low, all cycles except internal and DRAM refresh	$0.5t_Q-15$		$0.5t_Q-10$		ns
174	$t_{su(CH-CK1H)}$	Setup time of $\overline{CAS}$ high to LCLK1↑, all cycles except internal and DRAM refresh	$0.5t_Q-15$		$0.5t_Q-10$		ns
175	$t_{h(CK1H-WH)TR}$	Hold time of $\overline{W}$ high after LCLK1 high, shift register transfer	t_Q-15		t_Q-10		ns
176	$t_{su(WL-CK1L)TR}$	Setup time of $\overline{W}$ low to LCLK1↓, shift register transfer	t_Q-20		t_Q-10		ns
177	$t_{h(CK1L-WL)}$	Hold time of $\overline{W}$ low after LCLK1 low, shift register transfer	t_Q-15		t_Q-10		ns

NOTE: Advance information notices apply only to the TMS34010-50.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

local bus timing parameters (concluded)

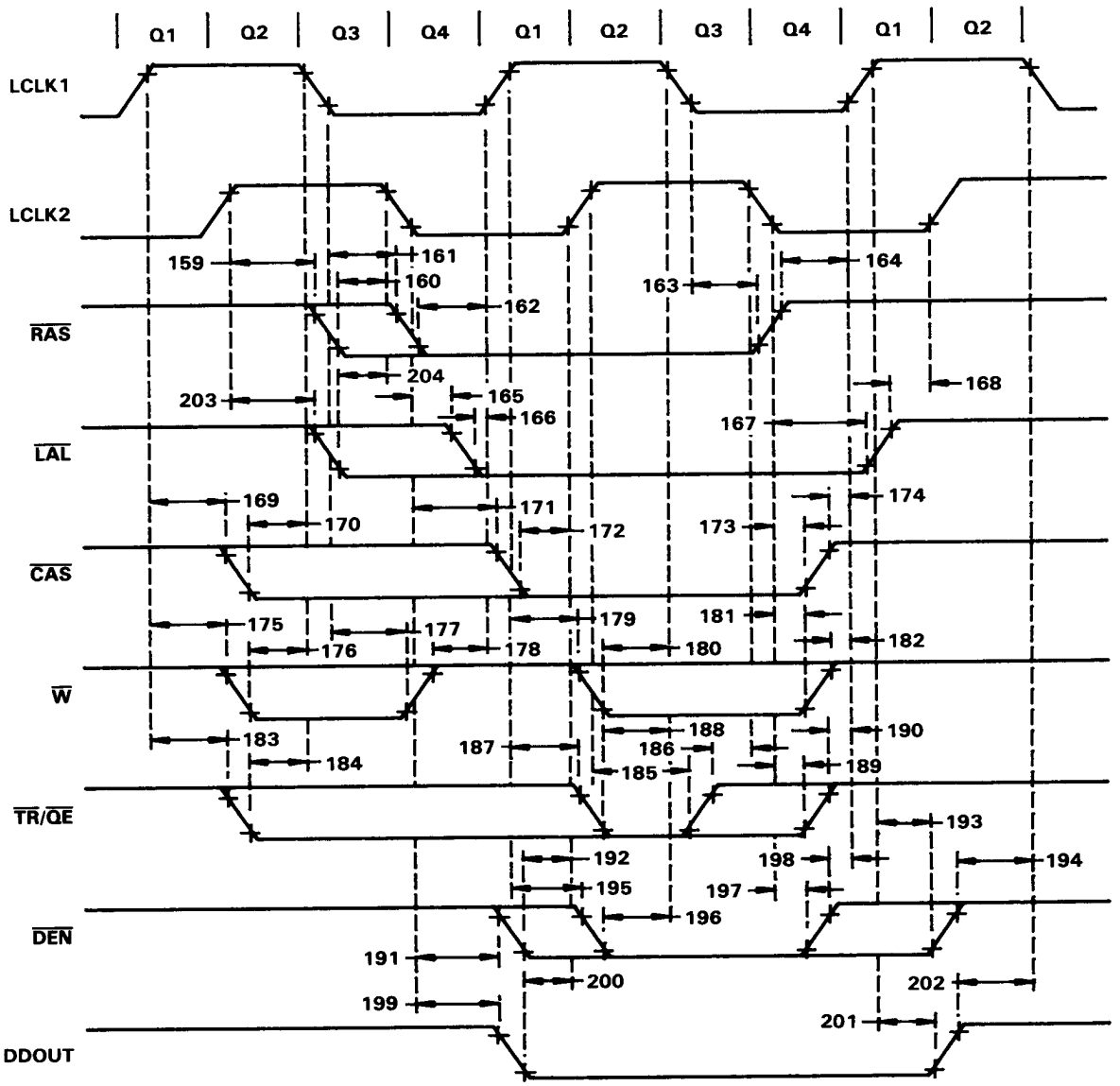
Quarter clock time t_Q, which appears in the following table, is one quarter of a local output clock cycle, or $2t_{c(ICK)}$.

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
178	$t_{su(WH-CK1H)}$	Setup time of $\overline{W}$ high to LCLK1↑, shift register transfer	t_Q-20		t_Q-10		ns
179	$t_{h(CK1H-WH)}$	Hold time of $\overline{W}$ high after LCLK1 high, write	t_Q-15		t_Q-10		ns
180	$t_{su(WL-CK1L)}$	Setup time of $\overline{W}$ low to LCLK1↓, write	t_Q-20		t_Q-10		ns
181	$t_{h(CK2L-WL)}$	Hold time of $\overline{W}$ low after LCLK2 low, write	$0.5t_Q-15$		$0.5t_Q-10$		ns
182	$t_{su(WH-CK1H)}$	Setup time of $\overline{W}$ high to LCLK1↑, write	$0.5t_Q-15$		$0.5t_Q-10$		ns
183	$t_{h(CK1L-TRH)}$	Hold time of $\overline{TR}/\overline{QE}$ high after LCLK1 high, shift register transfer	t_Q-15		t_Q-10		ns
184	$t_{su(TRL-CK1H)}$	Setup time of $\overline{TR}/\overline{QE}$ low to LCLK1↓, shift register transfer	t_Q-20		t_Q-10		ns
185	$t_{h(CK2H-TRL)}$	Hold time of $\overline{TR}/\overline{QE}$ low after LCLK2 high, shift register transfer	t_Q-15		t_Q-10		ns
186	$t_{su(TRH-CK2L)}$	Setup time of $\overline{TR}/\overline{QE}$ high to LCLK2↓, shift register transfer	t_Q-20		t_Q-10		ns
187	$t_{h(CK1H-QEH)}$	Hold time of $\overline{TR}/\overline{QE}$ high after LCLK1 high, read	t_Q-15		t_Q-10		ns
188	$t_{su(QEL-CK1L)}$	Setup time of $\overline{TR}/\overline{QE}$ low to LCLK1↓, read	t_Q-20		t_Q-10		ns
189	$t_{h(CK2L-QEL)}$	Hold time of $\overline{TR}/\overline{QE}$ low after LCLK2 low, read	$0.5t_Q-15$		$0.5t_Q-10$		ns
190	$t_{su(QEH-CK1H)}$	Setup time of $\overline{TR}/\overline{QE}$ high to LCLK1↑, read	$0.5t_Q-15$		$0.5t_Q-10$		ns
191	$t_{h(CK2L-ENH)}$	Hold time of $\overline{DEN}$ high after LCLK2 low, write	t_Q-15		t_Q-10		ns
192	$t_{su(ENL-CK2H)}$	Setup time of $\overline{DEN}$ low to LCLK2↑, read	t_Q-20		t_Q-10		ns
193	$t_{h(CK1H-ENL)}$	Hold time of $\overline{DEN}$ low after LCLK1 high, write	t_Q-15		t_Q-10		ns
194	$t_{su(ENH-CK1L)}$	Setup time of $\overline{DEN}$ high to LCLK1↓, write	t_Q-20		t_Q-10		ns
195	$t_{h(CK1H-ENH)}$	Hold time of $\overline{DEN}$ high after LCLK1 high, read	t_Q-15		t_Q-10		ns
196	$t_{su(ENL-CK1L)}$	Setup time of $\overline{DEN}$ low to LCLK1↓, read	t_Q-20		t_Q-10		ns
197	$t_{h(CK2L-ENL)}$	Hold time of $\overline{DEN}$ low after LCLK2 low, read	$0.5t_Q-15$		$0.5t_Q-10$		ns
198	$t_{su(ENH-CK1H)}$	Setup time of $\overline{DEN}$ high to LCLK1↑, read	$0.5t_Q-15$		$0.5t_Q-10$		ns
199	$t_{h(CK2L-DDH)}$	Hold time of DDOUT high after LCLK2 low, read	t_Q-15		t_Q-10		ns
200	$t_{su(DDL-CK2H)}$	Setup time of DDOUT low to LCLK2↑, read	t_Q-20		t_Q-10		ns
201	$t_{h(CK1H-DDL)}$	Hold time of DDOUT low after LCLK1 high, read	t_Q-15		t_Q-10		ns
202	$t_{su(DDH-CK1L)}$	Setup time of DDOUT high to LCLK1↓, read	t_Q-20		t_Q-10		ns
203	$t_{h(CK2H-ALH)}$	Hold time of $\overline{LAL}$ high after LCLK2 high, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-15		t_Q-10		ns
204	$t_{su(ALL-CK2L)}$	Setup time of $\overline{LAL}$ low to LCLK2↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_Q-20		t_Q-10		ns

NOTE: Advance information notices apply only to the TMS34010-50.

ADVANCE INFORMATION

local bus timing: relationship of control signals to clocks



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

video interface timing parameters

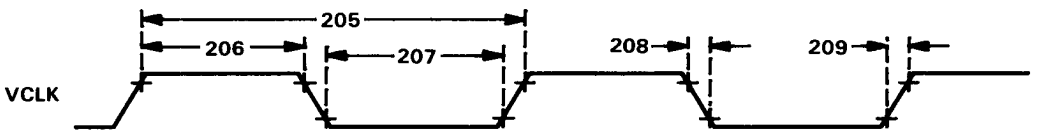
The timing parameters for TMS34010 video interface signals are shown in the next three tables and diagrams. The video interface includes the following TMS34010 pins: VCLK (video input clock), $\overline{\text{BLANK}}$ (blanking), $\overline{\text{HSYNC}}$ (horizontal sync, bidirectional), and $\overline{\text{VSYNC}}$ (vertical sync, bidirectional). $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are inputs if external sync mode is enabled; otherwise they are outputs.

video input clock timing parameters

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
205	$t_{c(VCK)}$	Period of video input clock VCLK	133		133		ns
206	$t_{w(VCKH)}$	Pulse duration of VCLK high	50		50		ns
207	$t_{w(VCKL)}$	Pulse duration of VCLK low	60		60		ns
208	$t_{t(VCK)}$	Transition time (rise and fall) of VCLK		5†		5†	ns

NOTE: Advance information notices apply only to the TMS34010-50.
†This value is determined through computer simulation.

video input clock timing

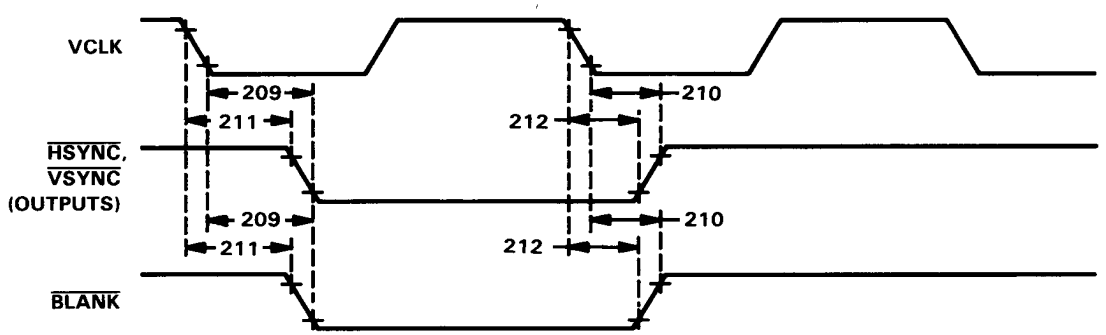


video interface timing parameters: outputs

NO.	PARAMETER		TMS34010-40		TMS34010-50		UNIT
			MIN	MAX	MIN	MAX	
209	$t_{d(VCKL-HSL)}$	Delay from VCLK low to $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, or $\overline{\text{BLANK}}$ low		55		55	ns
210	$t_{d(VCKL-HSH)}$	Delay from VCLK low to $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, or $\overline{\text{BLANK}}$ high		55		55	ns
211	$t_{h(VCKL-HSL)}$	Hold time of $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, or $\overline{\text{BLANK}}$ low after VCLK↓	0		0		ns
212	$t_{h(VCKL-HSH)}$	Hold time of $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, or $\overline{\text{BLANK}}$ high after VCLK↓	0		0		ns

NOTE: Advance information notices apply only to the TMS34010-50.

video output timing



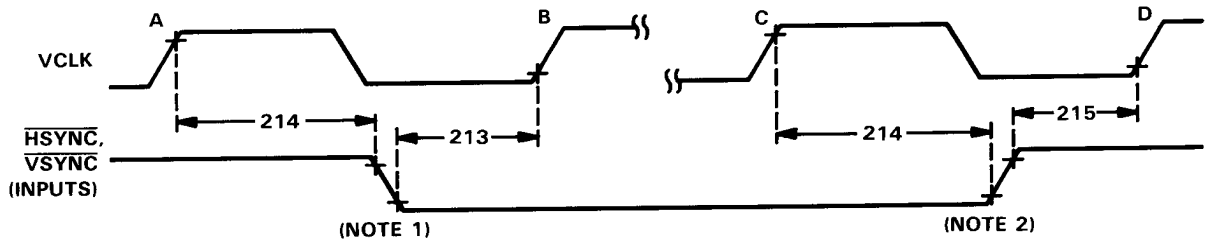
ADVANCE INFORMATION

video interface timing: external sync inputs

NO.	PARAMETER	TMS34010-40		TMS34010-50		UNIT
		MIN	MAX	MIN	MAX	
213	$t_{su(HSL-VCKH)}$ Setup time of $\overline{HSYNC}$, $\overline{VSYNC}$ low to VCLK↑	20†		20†		ns
214	$t_{h(VCKH-HSV)}$ Hold time of $\overline{HSYNC}$, $\overline{VSYNC}$ valid after VCLK high	20†		20†		ns
215	$t_{su(HSH-VCKH)}$ Setup time of $\overline{HSYNC}$, $\overline{VSYNC}$ high to VCLK↑	20‡		20‡		ns

NOTE: Advance information notices apply only to the TMS34010-50.
†Specified setup and hold times on asynchronous inputs are required only to guarantee recognition at indicated clock edge.
‡This value is determined through computer simulation.

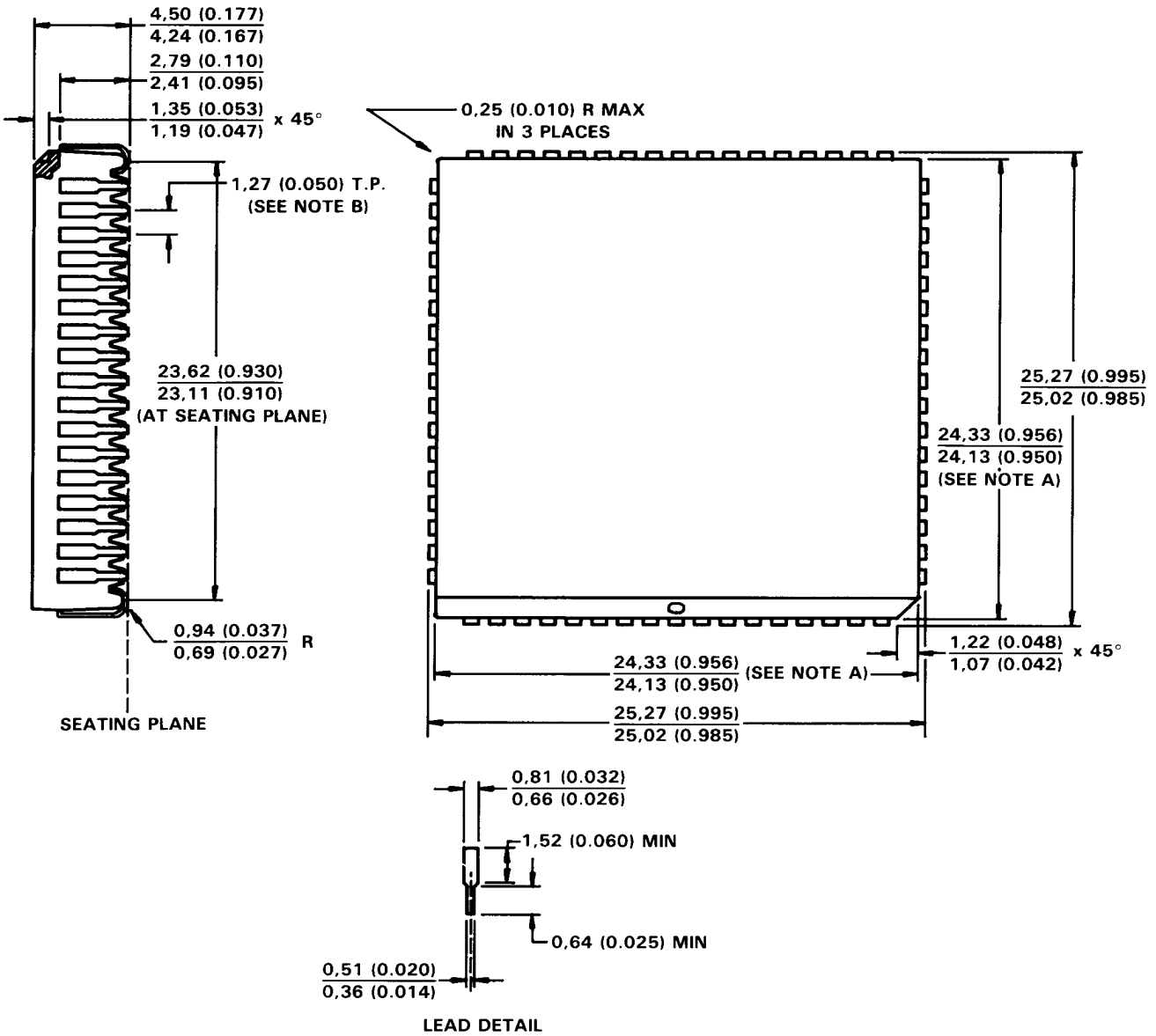
external sync input timing



NOTES: 1. If the falling edge of the sync signal occures more than $t_{h(SV-VCH)}$ past VCLK edge A, and at least $t_{su(SV-VCH)}$ before edge B, the transition will be detected at edge B instead of edge A.
2. If the rising edge of the sync signal occurs more than $t_{h(SV-VCH)}$ past VCLK edge C, and at least $t_{su(SV-VCH)}$ before edge D, the transition will be detected at edge D instead of edge C.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

MECHANICAL DATA



LEAD DETAIL

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by this dimension.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.