COSTGOLD RESEARCH LTD.

Cambridge
England

Technical Manual (Issue 4)

for the

CA856

80-Bus Compatible 8088 Card

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Section A General

1. Introduction

The CA856 card is a general purpose Intel 8088 based 16 bit processor card compatible with the Gemini 80-bus system. It offers a number of high performance features. When used in a system which contains another (Z80) based processor card, the CA856 may become the system master.

This manual describes all the features of the hardware together with a detailed description of circuit operation. For a description of the way in which the card may be used with disc operating systems please see the following manuals:

Costgold Research C-ROM Bios Operating Manual
Costgold Research CP/M-86 Impelmentation Guide

2. Facilities

* 8088 Card running at 8 MHz
* 16k Monitor EPROM space
* 256k of Dynamic Ram as standard
* Standard C-Rom Bios ROM operating system
* Optional CA856 Debug System Monitor
* Direct 80 bus IO interface with bus control
* Stand alone 80-bus operation is supported
* Full 8088 bus expansion provided on separate connector
* Asynchronous Serial Interface
* Crystal Controlled Real Time Clock

3. Installation and Operation

3.1 On Arrival of card

When the CA856 is delivered, the card should be carefully un-packed and examined for mechanical damage. Special attention should be paid to the gold plated bus connector, and care should be taken to avoid contamination with grease and dirt. The card has a polarising slot to ensure that it is correctly located in an 80-bus system. Power supplies required by the card are +5V at 0.5 A and +/-12V at 100mA (only needed where the RS232 option is to be used. Please check that each card is supplied with all the documentation as specified in the sales leaflet. If you are using the card with a GM813 card please read para 4.2 to determine where to place the CA856 - otherwise read 4.3

The card is provided with a number of link options. Cards are dispatched with these links in their standard operating mode for use as a second processor card in an existing Gemini system. For further information about these links, see Sect. A/8 "Summary of links".

3.2 Use in system with GM813 or GM811 card

The CA856 may be physically placed in the same rack frame as these cards. However, if it is intended to make full use of the dual processor facility, it is necessary to ensure that the CA856 is placed in the bus system such that it may take control of the bus when the system boot operation is performed. This is done by ensuring the Busreq signal of the CA856 is electrically connected to the Busreq signal of the GM813, and similarly for the Busak line. This may be achieved by placing the two cards adjacent, normally with the CA856 card to the right (when viewed from the front) of the GM813. However, it should be noted that a specific bus implementation may differ. Where there are other cards in the system, it is normal for these cards to loop the control lines through, and thus such cards may be interspersed between the CA856 and the GM813.

3.3 Use of the CA856 as the sole processor card.

In this case, the CA856 card may be inserted in any slot in the card frame in a typical GEMINI system, unless a peripheral card with Busreq/Busak logic is being used. Where the card is being used as a single board computer, it is not necessary to make any modifications, apart from directly connecting the supply rails if an edge connector is not to be used. Ensure correct connection by carefully consulting the circuit diagram.

The following points should be noted.

1. Processor clock as system clock.

Peripheral devices will need a system clock. The basic processor clock is 8 MHz (derived from a 24 MHz crystal). The FDCC card may be used with either 2 or 4 MHz clock - see Gemini Manual for link selection. The 8284 on the CA856 has a "PCLK" output, which is a 50% duty cycle 4 MHz clock. This may be connected to the system as follows:

On the 80-bus either Clock or AuxClock is used for the clock signal. Normally, Clock will be used, and this is connected to PCLK with Link j. Alternatively, AuxClock could be used (see connections on FDCC), and thus Link K should be connected.

2. Bus Control signals.

Pin 16 on the 80-bus is the NOT BAI (Not Bus acknowledge in) signal, which goes low to indicate that a peripheral may gain control of the system bus. On the CA856 this also directly enables the IO bus buffers A32, A46, A47.

In the standalone mode this pin must be held low. This is achieved by connecting links d and m on the CA856 (link m is normally shipped connected).

*** Note ****

Versions of the monitor earlier than 1.0 have a software problem when used in the standalone mode. This is connected with polling non-existent IO ports on the GM812 card. It may be overcome by connecting D0 on the 80-bus backplane to 0V with a 4k7 resistor. This prevents the D0 line from drifting up when the bus is tri-stated.

3. Reset Switch

The reset switch diode Z1 should be removed and replaced with a link if the RES SW line is used to indicate a reset.

4. IMPORTANT NOTES

Under no circumstances should the +5V rail exceed 5.5V in normal operation. Similarly, the +/- 12V rails must not exceed 12.5V in magnitude.

Polarity of all rails is vitally important, and application of incorrect voltages will cause damage which is not covered by the warranty.

Do not allow the card to operate with any line which is designated as an output connected to any damaging impedances. This is particularly important in respect of the bus control lines. (Normal Gemini systems do not provide any risk).

5. Selecting modes of operation

The CA856 card can operate in a wide variety of different ways. The system MODE links allows the selection of these modes of operation.

6. Other Facilities

The card can offer a number of other useful configuration options and facilities.

6.1 Interrupts

The CA856 supports the 8088 interrupt structure. Both the Real Time Clock and the 8250 Serial Link incorporate interrupts, which are fed to the Interrupt Control Register, and logically ORed to give a system INTR. This is acknowledged with an INTA, which strobes the Interrupt Control Register onto the data bus, providing an 8088 compatible Interrupt Vector. This may be used by an application program to provide interrupt driven facilities.

The interrupt vectors that will be jumped to are as follows:

2CH - 46818 Interrupt
2EH - 46818 Interrupt + 8250 Interrupt
2FH - 8250 Interrupt

For further details of the 8088 interrupt structure, and how to write programs to service it, consult the Intel Applications Handbook or contact Costgold Research Limited.

6.2 Reset Link Options

Normally, the 80-bus RESET SW line is connected to the 8284 Reset In pin via diode Z1, together with a power up capacitor/resistor circuit and the local Reset Switch. This diode may be removed to arrange that resetting the CA856 does not reset the whole system. This may be useful in applications where the user wishes to have the ability to reset programs running in the CA856 monitor, without affecting the rest of the system.

Alternatively, this diode may be reversed, allowing independent resets from the two reset switches with either as the master.

6.3 Other Options

6.3.1 Non-Maskable Interrupt (NMI)

Two possible options for the NMI interrupt exist:

a. Connected permanently low - disabled.

b. Connected to the front 8088 bus expansion connector.

Option b allows a switch and a monostable to be connected to the NMI which allows a monitor program execution to be terminated to aid software development.

6.3.2 TEST

This is selectable to 3 different positions:

a. Permanently low - disabled

b. Busak in - to allow high speed transfer

c. Spare line of 80-bus - to allow connection to high speed peripheral for WAIT loop controlled transfers.

7. IO Ports

7.1 80-bus IO Ports

80-bus io ports map with an offset of OFFOOH. This is because certain of the normal Gemini system ports conflict with Intel reserved values.

7.2 Local IO Ports

IO ports in the range of 0 - 0BFH are used for the onboard IO ports. The IO port range 0C0H to OFFOOH is not decoded, and so may be used by additional I/O devices connected via the front edge 64 way connector. The onboard IO ports are mapped as follows:

0	- 3FH	- Hitachi Real Time Clock 46818
40H	- 7FH	- Bus Status / Bus Control port
80H	- 0BFH	- National Semi. UART 8250.

8. Summary of Link Options

The CA866/CA856 has been designed to give a wide range of possible operational modes. These may be selected by a number of link options, some of which have been described above. This is a full summary of the links. The boards are shipped pre-configured to the dual-processor mode working with a Gemini GM813 or GM811 processor card. In most cases the links are set thus with a thin piece of track, which must be cut if an alternative mode is required.

Link	Made	Broken	Shipped
a	Connects 4250 READY to 8284 to enable wait state circuits.	Passes READY signal via front edge 64 way connector to allow ready arbitration off board.	MADE
b	NOT USED		OPEN
c	On board address buffers are always enabled.	Address buffer enable signal passed to 64 way connector for DMA operation etc.	MADE
d&m	d - Passes BAI* to TEST* input on processor. This allows high speed data transfer from a slave processor.	Disconnects BAI* to TEST* allowing link m to pull low or TEST* to be controlled off-board	OPEN
	m - Pulls TEST* low to ensure processor won't hang on a WAIT instruction.	TEST* may be controlled off-board	MADE
e	Pulls NMI low if this interrupt is not used.	NMI is available from the 64-way connector.	MADE
f	Allows INTA* to drive interrupt control port A52.	Allows off-board interrupt arbitration via 64-way connector.	MADE
ghi	Mode links to A59 - see C-Rom-Bios Manual or Debug/Monitor Manual.		OPEN
j	Connects 4MHz clock signal from 8284 (PCLK) to the 80-bus CLOCK LINE	Only one of j or k must be connected. If neither is connected then 4 MHz clock must come	OPEN

Link	Made	Broken	Shipped
k	Connects 4MHz clock signal from 8284 (PCLK) to the 80-bus AUXCLK line.	from other 80-bus card to provide system clock if required.	OPEN

l This comprises a four way link which is used to select the power up condition of BUSREQ.

a.

X----X

X----X

This will not assert BUSREQ

b.

X X
| |
X X

This will assert BUSREQ

Normal connection is as b., which asserts BUSREQ at power up or when the 8088 is RESET.

(N.B. - There is an error on the silkscreen of boards up to version -03 which show this link incorrectly as NOT ASSERTING BUSREQ but the boards are actually shipped connected in the opposite mode.)

m	(See link d. above)		
n	Ties HOLD to 8088 low if DMA is not used.	Allows off-board DMA controller to assert HOLD.	MADE

Also note that the diode Z1 connected with the reset switch may be replaced by a link, or removed, or connected in either direction to select how the two reset switches function when two processor cards are used.

Diode Z1

Removed	Both Reset switches operate independently, and link n will determine which processor obtains the bus.
Cathode to S1	Ca856 reset switch will reset both processors, but GM813 etc. reset switch will not reset CA856.
Anode to S1	GM813 reset switch will reset both processors, but CA856 reset will only locally reset CA856.
Short cct.	Not allowed, as the external impedance of the reset circuit on the GM813/811 interferes with the 8088 reset circuit.

Section B Hardware Description

Note *** In this text an active low signal is signified thus

1. Processor and associated control logic

1.1 Processor

The 16 bit processor used on the card is an Intel 8088-2 running minimum mode. In this mode the bus control lines closely resemble those of the 8 bit 8085 and hence the Z80 type control lines for feeding to the 80-bus can easily be synthesised.

Most signals from the processor connect into other circuit blocks on the board. The exceptions to this are HOLD and HLDA, which are the signals used to interface to a DMA (direct memory access) controller. When HOLD is driven to a logic 1 by an external DMA controller the 8088 finishes whatever it is doing , tri-states its address bus and control lines and then pulls HLDA to a logic 1, this signals the DMA controller that it has control of the address bus and control lines. When the DMA controller has finished its operation it releases HOLD, the processor will then release HLDA, re-enable the address bus and control lines and continue with its next operation.

1.1 Clock Generator, WAIT State Generator and RESET

All clock signals are generated from a 24MHz crystal oscillator in conjunction with the 8285 clock generator.

The 8284 has two independent sets of wait state generation logic, which are selected by AEN1* and AEN2*. The 74LS73 flip-flop, A51 is fed system CLK from the 8284, and ALE from the 8088. From these it generates a correctly timed input to RDY2 for the generation of one wait state on each bus access. To allow this to actually generate wait states, AEN2* must be held low, and AEN1* high. To achieve this, AEN1* is the inverse of AEN2*, from an invertor in A53. The two other conditions for WAIT state generation are:

1. An 80-bus access - 450 ns is the normal Z80 bus access time.

2. An autonomous refresh cycle in the 4500 DRAM controller.

An 80-bus access triggers the monostable A20 the output of which passes through the negative logic OR gate formed by A42, and makes AEN*1 active (that is, low) and AEN*2 inactive. Set up and hold times are observed. The monostable generates a pulse the width of which is controlled by the timing resistor and capacitor. This pulse is nominally 400ns long, to generate three wait states for IO access. In this case the 80-bus IO access signal will be 850 ns long. This value is quite

critical, as if it is any shorter, the WD1797 cannot provide data quickly enough, and if it is too long, other IO devices do not operate correctly. The RDY1,2* of the 8284 setup time is 35ns, and the AEN1,2* setup time is 15 ns. These timings must be observed, and are controlled by varying the value of the timing resistor.(There is a "window" of about 80 -90 ns as the hold times for these pins is 0ns).

Similarly, if the 4500 RDY pin becomes inactive, because it wishes to perform a refresh cycle, then AEN*1 becomes active and AEN*2 inactive.

These two devices correspond to "normally not ready" devices in the Intel applications note AP-67, and as RDY1 is tied low, for the duration of either the 80-bus access or the 4500 refresh, the 8284 inserts correctly timed Wait states.

The 24MHz OSC signal is fed along with the 8MHz CLK signal into an F74 D-type flip-flop to generate the 8MHz 4500CLK signal for the DRAM controller which is delayed from the 8MHz processor clock by the period of one 24MHz cycle - this provides the correct RDY1 set up time for wait state generation.

The 4MHz PCLK signal is divided by 2 with an LS73 flip-flop to generate a 2MHz clock signal for the baud rate generator in the 8250 UART. The reset input to the 8284 is driven from 3 different sources.

a) Power-up reset. This is achieved with an RC network.

b) On-board reset. This is a push button on the card which discharges the capacitor of the power-up reset circuit.

c) Off-board reset. If diode Z1 is fitted then a reset signal on the 80-bus will also reset the 8088 if the diode is fitted with anode to the CA856 Reset Switch. If Z1 is fitted in the opposite direction, then pressing the CA856 Reset Switch will reset both the 8088 and any cards on the 80-bus. If neither link nor diode is fitted then pressing the on-board button will reset the 8088 but will not affect the 80-bus, nor will a signal on the 80-bus affect the 8088.

1.3 Address Bus Buffers

Address lines A0 to A7 and A16 to A19 are latched into a pair of LS373s by the ALE (address latch enable) signal from the 8088. This is done because the 8088 time-multiplexes the data bus onto the same pins as A0 to A7 and the status bus onto the same pins as A16 to A19. A8 to A15 do not need to be latched as they remain valid throughout the whole of the processor cycle.

For use with a DMA controller the facility to tri-state the outputs of the LS373s is provided via the AEN signal. When this line, which comes from the 64 way expansion connector, goes to a logic 1 the address lines A0 to A7 and A16 to A19 out of the latches are tri-stated. A8 to A15 are tri-stated by the processor if DMA is in progress.

1.4 Data Bus Buffers

The data bus is buffered by an LS245 octal bi-directional buffer. The direction of the buffer is controlled by the DT/R* (data transmit/not receive) signal from the processor. This is a logic 1 when the processor is writing data onto the bus and a logic 0 when it is reading from it. This buffer is tri-stated when the DEN* (not data enable) signal is set to a logic 1 by the processor.

1.5 Control Signal Generation

The IO/M* (input & output/not memory) signal from the processor along with the RD* (not read) and WR* (not write) are fed into an LS257 which demultiplexes them into MEMR* (not memory read), MEMW* (not memory write), IOR* (not input and output read) IOW* (not input and output write).

1.6 Interrupt Generation

The two interrupt sources on the card are the 8250 UART and the 46818 RTC (real time clock). The interrupts from these two devices are logically 'ored' together and fed to the 8088 INTR input pin, and to a LS244 tri-state buffer. When the 8088 receives an interrupt on the INTR pin it takes the INTA* pin to a logic 0 level and then expects an 8 bit vector to be placed on the bus by the device generating the interrupt.

When an INTA* is generated the output of the LS244 is enabled onto the bus. The 6 other inputs to the LS244 are tied either to logic 0 level or logic 1 level to fix the range of vector numbers and the 2 inputs from the UART and the RTC determine exactly which vector is generated. For a more detailed description of how interrupts are handled the Intel 8086/8088 data book should be consulted.

2 Memory

2.1 Decoding

The generation of all memory chip selects is handled by a PLA which decodes address lines A8 through to A19 to give a resolution of 256 bytes to each of the memory boundaries. The PLA gives two memory chip selects, one for the on-board EPROM site which normally occupies a 16K area of memory right at the top of the memory map, the other handles the on-board RAM which normally occupies the bottom 256K of the map.

2.2 RAM

The on-board RAM is handled by a Texas Instruments TMS4500A DRAM Controller Chip. This chip handles all of the DRAM functions normally done in discrete logic i.e. address multiplexing, RAS* and CAS* generation, refresh generation, refresh arbitration and wait state generation.

The selection of the correct 64K bank of RAM is taken care of by an LS139 decoder fed with address lines A16 and A17. The gate input to the decoder is fed with the RAS0* signal from the controller to generate 4 bank RAS* signals. The bank RAS* signals from this chip are fed via an F08 quad and gate which generates a RAS* signal to all 4 banks simultaneously for refresh when the RAS1* signal from the controller goes low.

For further information on the DRAM controller see the Texas Instruments data sheet on that device.

2.3 EPROM

The EPROM site is a 28 pin socket which will accept either a 2764 or a 27128 without modification. This site is normally occupied by the monitor EPROM.

This site is mapped to absolute address OFC000H. If a 2764 is fitted, then two images will appear, one at OFC000H to OFDFFFH and one from OFE000H to OFFFFFH.

The device fitted must be 250 ns or better access time.

3 ON-BOARD I/O

3.3 Decoding

The chip select signals for the three on-board I/O ports are generated by one section of an LS139 fed by address lines A6 and A7, which are validated with a signal from the PLA. This signal places the on-board I/O in the 64K 8088 I/O address space in the bottom 256 bytes.

A7	A6	Chip Selected
0	0	real time clock
0	1	status and control port
1	0	serial interface
1	1	not used

3.2 Serial Port

This serial port is a National Semiconductors INS8250 which device has on-board baud rate generation facilities. The modem input and output lines from this device are buffered to voltage levels to suit normal RS232 operation by an MC1488 and MC1489.

3.3 Control Port

An LS74 D-type latch is connected as a 1 bit write only port and when written to the state of bit D0 is used to control the 80-bus request logic.

3.4 Status Port

An LS367 hex buffer is connected to the lower 6 bits of the data bus and is addressed as an on-board, read only, I/O port to provide a port through which the state of various on-board signals can be read.

Bit No.	Function.
0	- User defined link g
1	- User defined link h
2	- User defined link i
3	- BAI* in
4	- BUSRQ* in
5 to 7 are not used	

3.5 Real Time Clock

The real time clock is a Hitachi HD46818 RTC chip. It provides full time and date facilities and is provided with its own crystal oscillator to ensure accuracy.

4 80-BUS INTERFACE

4.1 Decoding

The select signal for the 80 bus I/O is the fourth select signal generated by the PLA and places the 80 bus I/O in the top 256 bytes of the 8088's I/O address space. When the 8088 accesses the 80-bus address spaces the address and the data bus buffers are enabled.

4.2 Data Bus Buffers

The 8088 data bus is buffered by an LS245 buffer. Its direction is controlled by DT/R* (see processor data bus buffer description for details of this signal) and it is enabled by a signal from the PLA which is conditioned with BUSEN* which comes from the bus arbitration section of the board.

4.3 Port Address Buffer

The low order 8 bit of the address bus, which determines which one of the 256 ports is being addressed, are fed to the 80-bus via a LS244 tri-state buffer. This buffer is enabled by BUSEN*.

4.4 Control signal generation

When the 8088 is driving the 80-bus lines RFSH*, M1* and MREQ* are set to a logic 1 level. Line RD* is fed with the 8088 IOR* signal and the WR* is fed with IOW*. IORQ* is generated by logically 'oring' IOR* and IOW*, conditioning this signal with the 80-bus chip select signal.

4.5 Bus Arbitration

When the on-board control port has a logic level 1 written to it the 80-bus open collector BUSRQ* line is pulled low. Upon BAI* going low a signal called BUSEN* for on-board use will be generated providing the BAI* was generated in response to a BUSRQ* signal from the card (this is done to allow for the possibility of multiple processor cards in a system). BAI* is may be read via the on-board status port. The state of BUSRQ* at power-up or reset is determined by the routing of the CA866/CA856 RESET signal via link 1 to the set or reset inputs of the controlling flip-flop. The connection of these links is more fully described in Section A parts 6 and 8.

APPENDIX A - 64 Way Connector Assignments

This connector is provided to allow full access to the 8088 internal circuitry.

1	-	Ground
2	-	Ground
3	-	Ground
4	-	Ground
5	-	Address A18
6	-	XRDY from Wait State Logic
7	-	Address A19
8	-	8284 Ready signal
9	-	Ground
10	-	Data Line D6
11	-	Data Direction Control DT/R*
12	-	Data Line D5
13	-	Ground
14	-	Data Line D4
15	-	Address A6
16	-	Data Line D0
17	-	Address A5
18	-	Data Line D1
19	-	* Not connected *
20	-	Data Line D2
21	-	Ground
22	-	Data Line D3
23	-	Address A4
24	-	Data Line D7
25	-	Address A3
26	-	Address A7
27	-	Address A2
28	-	Address A8
29	-	Address A1
30	-	Address A9
31	-	Address A0
32	-	Address A12
33	-	DEN* Not Data Enable
34	-	Address A13
35	-	* Not Used *
36	-	Address A14
37	-	* Not Used *
38	-	Address A10
39	-	TEST* Processor NOT TEST line.
40	-	Address A11
41	-	Ground
42	-	NMI Non Maskable Interrupt
43	-	Address A16
44	-	INTR Interrupt Request Line
45	-	Address A17
46	-	INTA* NOT Interrupt Acknowledge from 8088
47	-	Processor Clock
48	-	WR* Processor Not Write (un-buffered)
49	-	Address A15

50 - HOLD Processor Hold Request Line
51 - ALE Processor Address Latch Enable
52 - HLDA Processor Hold Acknowledge
53 - RESET System Reset line
54 - RD* Processor Not Read (un-buffered)
55 - AEN Address Enable of Address buffers for DMA
56 - IO/M* IO/NOT MEMORY select line (un-buffered)
57 - Address A19
58 - Ground
59 - Ground
60 - Ground

61 - Ground
62 - Ground
63 - Ground
64 - Ground

The main purpose of this 64-way connector is to allow the connection of user defined expansion hardware to the 8088 processor bus. This will allow DMA operation if the following points are observed.

1. Link n for HOLD must be removed on the CA856.
2. If external circuitry cannot meet 8088 bus access times then external wait circuitry must be incorporated between 6 & 8. In this case link a must be disconnected.
3. External decode of RD*, WR* and IO/M* must be incorporated.
4. AEN logic to disable CA856 address drivers must be provided.
5. DEN* and DT/R* logic must also be provided.

For further details see the Intel IAPX-88,86 System designers information, or contact Costgold Research for advice.

As a cheaper option it is possible to fit a 60 way connector, as pins 61 to 63 are solely reserved for GROUND connection.

APPENDIX B - 26 way RS232 connector.

Pin connections shown correspond to those for ribbon cable connectors. These have been chosen such that if the ribbon cable is connected to a 25 way D header, then they will directly correspond to the BELL modem configuration which are standard for modem connections, with pin 2 as transmit and pin 3 as receive.

1	Ground
2	* Not Used *
3	Transmitted Data
4	* Not Used *
5	Received Data
6	* Not Used *
7	RTS Request to Send
8	* Not Used *
9	CTS Clear to Send
10	* Not Used *
11	DSR Data Set Ready
12	* Not Used *
13	Ground
14	DTR Data Terminal Ready
15	* Not Used *

