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Programmers Reference Guide

Draft (001)

C O N T E N T S

1. Introduction

This manual is the Programmers Reference Manual for the Gemini Computer Systems GM886 CPU 80-bus card. This CPU uses the Intel 80286 processor to provide a very high performance bus-orientated system. The purpose of this manual is to explain the hardware interface incorporated within the GM886 in such a way that a programmer familiar with MS-DOS, the 80286 and 80-bus generally may produce software which exploits all the interface features provided.

This document is split into the following sections:

- Overview of facilities
- Description of Memory and I/O map
- Description of On-board peripherals
- Description of 80-Bus accesses
- Points arising from options
- Link settings

2. Overview of Features

Processor

The CPU is an Intel 80286 CPU. The design caters for both 8MHz and 12MHz clock options. There is one link required to select which clock is passed to the 80-bus. It should be noted that there is a conversion kit provided to convert from 8 to 12MHz operation.

Additionally, provision is made for two co-processors.

These are:

DMA Co-Processor Intel 82258
Numeric Co-Processor Intel 80287

It is recommended that the DMA Co-Processor option should be carefully studied before it is fitted, as the action of this device is extremely powerful. There is a link on the HOLD pin which must be removed if it is intended to run this device.

No special action is required if the Numeric Co-Processor option is installed.

Memory

One megabyte of high-speed dynamic RAM is provided on-board. This is implemented as 8 off 256k x 4 DRAMs. These may be changed to 1M x 4 DRAMs as these devices become available. Additionally, there is a connection point for the remaining multiplexed address line, and options are intended to allow memory expansion by means of a small daughter board.

Two EPROM sites are available. These are for the lower and higher order bytes of the 16 bit word access. The following options exist:

2 x 2764 - 16k EPROM
2 x 27128 - 32k EPROM
2 x 27256 - 64k EPROM

All EPROM devices must be 200 or 250 ns access times. It should be noted that for 12MHz operation only 200ns devices are acceptable. The access time is controlled by a PAL and so by special arrangement this could be extended if required.

Input/Output Devices

The following input/output devices are provided:

a. Serial Port INS8250

b. Parallel Port Intel 8255 (two 8-bit parallel I/O are made available for the user).

c. Real Time Clock HD146818

d. 80-BUS paging and control port.

e. Bus reset control.

f. Interrupt Controller PIC 8259.

g. 80-BUS semaphore port.

I/O Map

The I/O Map is as follows:

Start	Finish	Device
0020H	0027H	Interrupt Controller
0040H	0041H	80-BUS semaphore port
00F8H	00FFH	Numeric Co-Processor
0340H	0347H	Pluto 80-BUS access
03F8H	03FFH	Serial Port
0400H	043FH	Real Time Clock
0440H	0447H	Parallel Port (P8255)
0448H	044FH	80-BUS paging port

All other accesses are modulo-256 I/O accesses to the 80-bus.

3. Detailed description of memory map

Two bits of the Parallel Port may be used to control the memory map mode. The following memory map modes are supported:

Mode	RAM	EPROM	80-BUS	
0	0 0EFFFF	0F0000 0FFFFF	-	
1	0 09FFFF	0F0000 0FFFFF	0A0000 0EFFFF	*
2	0 09FFFF + 0C0000 0EFFFF	0F0000 0FFFFF	0A0000 0BFFFF	
3	0 0FFFFF	0FF000 0FFFFF	-	

Note: * In this mode the actual page addressed in the 80-bus space is controlled by the 80-bus control register. See the definition of the controls for this device.

The memory mode is controlled by Memory Mode 0 and Memory Mode 1 which are generated by the Intel 8255 parallel port. See the description of this device for details. Memory modes are defined thus:

Mode	MM0	MM1	
0	0	0	(MM0 is 8255 port PC4)
1	1	0	(MM1 is 8255 port PC5)
2	0	1	
3	1	1	

4. Detailed Description of Peripherals

Serial Port

There is one on-board serial port. This is an INS8250 UART. Full handshaking is provided. The address of this port is based at 03F8. This is the address of the COM1: port of an IBM PC. The registers for this port are at the following addresses:

Address	Register	
	DLAB 0	1
03F8		
03F9		
03FA		
03FB		
03FC		

The interrupt pin for this chip is connected to IR4 of the Interrupt Controller. No interrupt vector is programmed as default for this chip, so any software which requires to use the interrupt facility direct must set this device accordingly.

The serial port connector is PL1. The pinout of this connector is as follows:

Pin	Function
1, 13	GROUND
3	Serial Out
5	Serial IN
7	Request to send
8	Ring Indicate
9	Clear to Send
11	Data Set Ready
12	Data Terminal Ready
15	Received Line Signal Detect

This allows a full modem interface.

Interrupt Controller

The following interrupts are supported:

Interrupt	Function
0	Real Time Clock
1	80-Bus semaphore port
2	80-Bus Int 0
3	80-Bus Int 1
4	Serial Port (8250)
5	DMA controller/80-Bus Int 2 [JP8]
6	DMA controller/80-Bus Int 3 [JP7]
7	Parallel Port Interrupt

For programming details see the Intel 8259 PIC data sheet. Interrupt 4 is fully compatible with the IBM PC COM1: serial port interrupt.

The four interrupts from the 80-bus are polarity programmable by links JP4, JP2, JP1 and JP3. This allows full flexibility in interrupt sources. See the section on link configuration for details on how to set these links.

Real Time Clock

An Hitachi HD146818 R.T.C. is provided. This has a fully functioning calendar clock and also 64 bytes of battery backed up RAM which may be used for configuration information etc. Access to this device is not straightforward because of the non-multiplexed bus structure of the 80286. A PAL has been provided which generates addressing information for this device when accessed in the correct manner.

After reset the device will be in an Idle state. Any access to the R.T.C (I/O addresses 400 - 43FH) with A0 = 1 will cause the PAL to generate an ALE strobe into the R.T.C. and establish the R.T.C chip select. Thus if a write is performed to 401H the data value will be strobed into the R.T.C as a register address. The next access (either read or write) must be to a location with A0 = 0. This then generates the appropriate data read or write.

Prototype code to perform this access would be as follows:

FOR WRITE

```
    MOV     DX, 401H
    MOV     AL, 8           ; Register Number
    MOV     BL, 55H         ; Data value
    OUT     DX, AL          ; select register
    XCHG    AL, BL          ; swap data into AL
    DEC     DX              ; point to 400H
    OUT     DX, AL          ; write 55H to register 8
```

FOR READ

```
    MOV     DX, 401H
    MOV     AL, 9           ; Register Number
    OUT     AL, DX          ; select register
    DEC     DX              ; point to 400H
    IN      AL, DX          ; read register
```

With the above routines incorporated into a RTCREAD and RTCWRITE sub-routines accesses to the RTC are exactly as described in the relevant manufacturers data sheets.

Parallel Port

The parallel port is an Intel PPI 8255 which is a very powerful device. It is intended that one function of the parallel port should be to act as a printer port. To this end PL3 may be programmed as follows:

Input
Output
Bi-directional
Interrupt driven

PL2 is configured as a general purpose 8 bit I/O port. Additionally there are four general control signals from this device. They are as follows:

PC4	Memory Mode 0
PC5	Memory Mode 1
PC6	Reset for 80 Bus
PC7	External Reset Enable

All these signals are programmed as 0 when the chip is first initialised. This will be done as part of the ROM Bios initialisation sequence. Memory Mode 0 and 1 must be modified with the greatest of care. The Reset for 80 Bus and External Reset Enable are both "inactive" when 0. Their function is:

External Reset Enable.

0 - Allows only the on-board reset switch to reset the CPU.

1 - Allows the 80-bus /RESET SW line to reset the CPU.

Reset for 80-bus

0 - No reset

1 - Resets 80-bus (and 286 if External Reset Enable is active).

At power up the /RESET SW line may be used to reset the 80286. During initialisation it programs this port so that it may assert the 80-bus reset should it so desire but the 80-Bus cannot reset the 80286. This is intended to be part of a processor swapping protocol if required to act as a dual processor system.

80-Bus Semaphore Port

The purpose behind this port is to allow the exchange of bus mastership between two processors sharing the same 80-bus. The are two active bits which may be written/read. These are called Flag0 and Flag1. The device may be accessed in the following fashion:

Address	Function
0040H	Read - DB0 and DB1 reflect the setting of Flag0 and Flag1.
	Write - Flag0 and Flag1 are set with the values of DB0 and DB1. The Flag Interrupt will be set active.
0041H	A write of any data will clear the Flag Interrupt if it has been set.

An exchange protocol may therefore be arranged using these two flag bits. It should be noted that the exchange is not limited to an GM886 and a Z80 processor but may involve more than one GM886.

80-BUS paging and control port

This is used to control the higher order nibble of the 80-BUS address bus. It also has a number of control functions. Bit assignment is as follows:

Bit	Function
0	80-BUS A16 **
1	80-BUS A17
2	80-BUS A18
3	80-BUS A19 *
4	80-BUS /REFRESH pin
5	80-BUS /M1 pin
6	Bus Lock
7	80-BUS /NMI

* This is link selected to backplane
** This may not be operative in EGA mode

Bits 0-3 may be used to select a 64k page in 80-bus memory space. In future PCBs A16 (Bit 0) will be link selectable to a latched version of A16. This will allow the creation of a 128k byte image area in the backplane memory which may be used to directly interface to an IBM PC EGA card. Issue 1 pcbs may be easily modified to add this feature.

/REFRESH, /M1 and /NMI are provided for completeness. A mechanism for refreshing DRAM virtual discs may be provided which relies on a repetitive timer interrupt and generation of refresh cycles by setting /REFRESH active low.

Bus Lock is used in systems with only the GM886, or where it is required to completely disable the 80-bus. If it is active the 80-bus is continuously enabled.

5. Accessing the 80-BUS

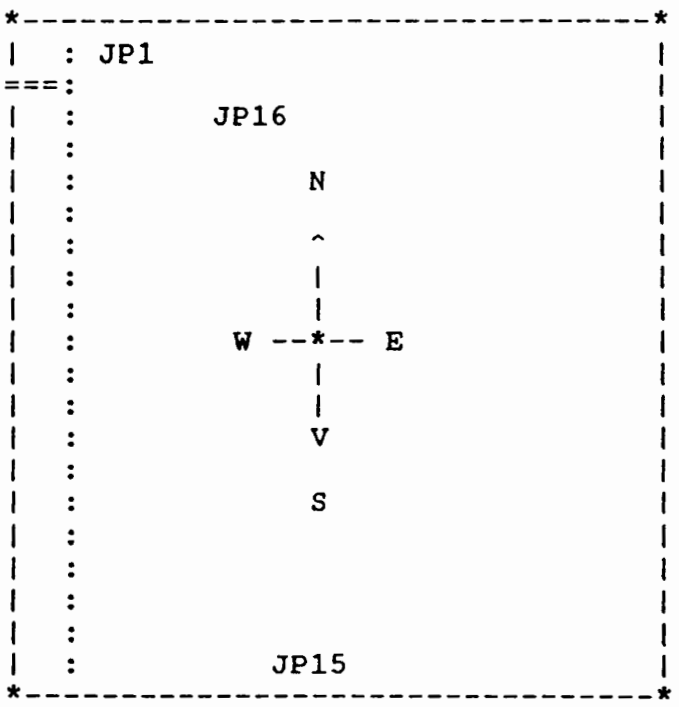
80-BUS access is reasonably straightforward but the following points should be considered.

There are two main modes of 80-bus access. These could be called "ARBITRATED" and "NON-ARBITRATED". In the "ARBITRATED" mode a full BUSREQ/BUSACK exchange occurs for every access to the 80-BUS. This allows multiple processors to exchange data via the backplane. In the "NON-ARBITRATED" mode, the Bus Lock signal is asserted and the GM886 has full control over the 80-BUS. It should be noted that unless a dynamic ram refresh operation is set up any data held in dynamic RAM will be lost.

6. Link settings

Link References and specification

The GM886 is provided with a large number of user-defined options which may be controlled by a number of links (or jumpers). All these are referenced as "JPnn" where nn is 1 -16. In many cases the link has only two pins. In these cases thelink is referred to as either "OPEN" where the two pins are not connected, or "CLOSED" where they are. In some cases the links have more than two positions. These links are specified by using an North-South-East-West terminology. With the GM886 held with the 80-BUS connector to the left, with component side uppermost and polarising key in the top left hand corner, then N-S-E-W are defined as follows:



These links are therefore specified by North Sout East or West where this corresponds to the part of the link which is made.

Location of links on the PCB

Links may be located on the PCB as follows:

JP1 - JP15 These links start in the top left hand corner of the PCB and work towards the bottom right in order. They may be found by first working to the right and then down.

JP16 This link is next to the DMA co-processor site, IC4 approximately in the position shown above.

Setting of Links

JP1 - Sets polarity of interrupt 2

OPEN - 80-Bus INT2 is inverted.
CLOSED - 80-Bus INT2 is NOT inverted.

JP2 - Sets polarity of interrupt 1

OPEN - 80-Bus INT1 is inverted.
CLOSED - 80-Bus INT1 is NOT inverted.

JP3 - Sets polarity of interrupt 3

OPEN - 80-Bus INT3 is inverted.
CLOSED - 80-Bus INT3 is NOT inverted.

JP4 - Sets polarity of interrupt 0

OPEN - 80-Bus INT0 is inverted.
CLOSED - 80-Bus INT0 is NOT inverted.

JP5 - NMI control for 286

1 - +5V
2 - 80286 NMI pin
3 - 0V
4 - 0V

normally 2 and 3 are connected to disable NMI, but an external switch could be connected for NMI operation.

JP6 - 80-Bus A19 connection

CLOSED - Connects A19 to 80-Bus pin 58
OPEN - A19 is not connected to the backplane

JP7 - Selects source of IR6.

NORTH - IR6 is INTDMA
SOUTH - IR6 is 80-Bus INT 3

JP8 - Selects source of IR5.

SOUTH - IR5 is INTDMA
NORTH - IR5 is 80-Bus INT 2

JP9 - Division ratio for 80-Bus clock prescaler

OPEN - 12 MHz CPU clock.
CLOSED - 8MHz CPU clock.

this link determines the division ratio required to give 4MHz for 80-Bus.

JP10 - Auxiliary outputs from 8250

1 - 0V
2 - /OUT1
3 - /OUT2
4 - 0V

JP11 - EPROM type selection

NORTH - 27128/2764 type of EPROMs
SOUTH - 27256 type of EPROMs.

JP12 - 80-Bus backplane clock selection

NORTH - Connects 4MHz to 80-Bus AUX CLK
SOUTH - Connects 4MHz to 80-Bus CLOCK
OPEN - 4MHz is not connected to 80-Bus

JP13 - 80-Bus /BAI

OPEN - /BAI comes from another CPU
CLOSED - /BAI permanently active - ie single CPU.

JP14 - Powerfail control

WEST - from /PWRF
EAST - from 7673 controller

JP15 - Real Time Clock

EAST - RTC standby power from VCC.
WEST - RTC standby power from 80-Bus AUX PWR line.

JP16 - CPU Hold Link

OPEN - No DMA co-processor
CLOSED - DMA co-processor operation ONLY