G E M I N I

M I C R O C O M P U T E R S

GM853/863

EPROM/RAM

BOARD

USER MANUAL

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1. INTRODUCTION

The Gemini GM853/863 is a reconfigurable "bytewide" memory board for use in 80-BUS systems. It will support 8K x 8 RAMs and 2764, 27128, 27256 and 27512 EPROMs. When used as a RAM board it will provide up to 64K of static RAM storage, and as an EPROM board it will provide up to 512K of EPROM.

The GM863 has all the features of the GM853 and in addition may be configured so that the RAM contents will be retained independent of system power, the backup power being provided by a Nicad battery which is recharged when system power is restored.

On both the GM853 and the GM863, the 80-BUS page mode scheme is supported together with extended addressing; page mode and extended addressing are the two methods of extending the amount of memory available to the Gemini CPU boards. The GM811 Z80 CPU board (and the Nascom 1 and 2) support only page mode, whereas the GM813 Z80 CPU/RAM board, and the GM888 8088 CPU board, support both page mode and extended addressing. On the GM853/863, address decoding and device type selection are performed using bipolar PROMs which may easily be changed to accommodate special or custom requirements.

Please take the time to read through this manual carefully, as there are a number of switch and link options that must be set correctly for the board to operate. For example, please note the following:

IMPORTANT

THE BATTERY BACK-UP OPTION OF THE GM863 WILL NORMALLY BE FACTORY SET IN THE `OFF' STATE IN ORDER TO CONSERVE THE ON-BOARD BATTERY.

2. DEFINITION OF TERMS

Device Refers to a memory device i.e. a RAM or EPROM.

Bank Row of four sockets capable of taking RAM or EPROM devices.

Socket The socket into which a memory device may be plugged.

Extended addressing
Some of the Gemini 80-BUS boards (GM813, GM888) support the use of three extra address lines (A16 - A18), these lines (in the case of a Z80 CPU) are generated using extra circuitry. For more information please see section 6.2.

Page mode
A technique for switching between one of four `pages´ of memory (provided by GM811, GM813 and GM888). For more information please see section 6.1.

DIL switch
Dual In Line switch, which on the GM853/863 has eight individual switches (poles) marked 1 to 8.

RAM-disk
An area of RAM memory can be configured to look and act like a disk drive (hence RAM-disk).

Where references are made to a position on the board, (e.g. upper left corner) it is assumed that the board is lying in front of you with the component side uppermost, and the 80-BUS edge connector nearest to you. In this orientation the board type number (GM853 or GM863) and IC numbering should be the correct way up.

3. SWITCH SETTINGS

3.1. Introduction

The GM853/863 has three DIL switches (SWa, SWb and SWc). SWa and SWb control the same functions, SWa for bank A (sockets A0-A3), SWb for bank B (sockets B0-B3). These switches are used to select the type of device to be used in each bank. In the configuration determined by the standard decode PROMs the two banks may contain different devices, however an individual bank may not have more that one type of device present. The switches also determine whether a particular device is enabled. This permits memory devices to be disabled without their removal from the board, or for memory on another board to be used at these addresses. It is also possible to prevent write cycles from affecting memory contents; this feature may be used to protect against memory corruption.

SWc is used for the functions which are common to both banks. It determines which page the board will respond to, the base Extended Address and the direction in which the 80-BUS RAMDIS signal will operate.

3.2. Switch Summary

The following tables give a brief description of the purpose of each switch.

Switch a

POLE	FUNCTION	OFF	ON
1	SOCKET A0 (IC12)	disabled	enabled
2	SOCKET A1 (IC14)	disabled	enabled
3	SOCKET A2 (IC19)	disabled	enabled
4	SOCKET A3 (IC24)	disabled	enabled
5	DEVICE TYPE 1)	these switches	
6	DEVICE TYPE 2)	determine the device	
7	DEVICE TYPE 3)	type to be used.	
8	WR ENABLE	disabled	enabled

Switch b

POLE	FUNCTION	OFF	ON
1	SOCKET B0 (IC11)	disabled	enabled
2	SOCKET B1 (IC13)	disabled	enabled
3	SOCKET B2 (IC18)	disabled	enabled
4	SOCKET B3 (IC23)	disabled	enabled
5	DEVICE TYPE 1)	these switches	
6	DEVICE TYPE 2)	determine the device	
7	DEVICE TYPE 3)	type to be used.	
8	WR ENABLE	disabled	enabled

Switch c

POLE	FUNCTION	OFF	ON
1	POWER FAIL	latched	non-latched
2	ADDRESS A18	inverted	true
3	ADDRESS A17	inverted	true
4	ADDRESS A16	inverted	true
5	PAGE LSB	high	low
6	PAGE MSB	high	low
7	RAMDIS	out(ROM)	in(RAM)
8	UNUSED	unused	unused

If you are installing your own memory devices in the board it is advisable NOT to insert them until all the switch options have been selected. The reason for this is that it is only possible to define specific memory addresses to devices if they are in specific sockets, and the correct socket positions will become apparent when working out the switch settings.

3.3. Page mode

There are four options for the memory `page' to which the entire board will respond, and these are selected by poles 5 and 6 of SWc. The Page Mode technique is supported by all 80-BUS CPU boards. In most applications page 0 will be chosen.

PAGE	SWc (5)	SWc (6)
0	on	on
1	off	on
2	on	off
3	off	off

For more information on the software implications of page mode please see section 6.1 or the manual for your CPU board.

3.4. Extended Addressing

The base Extended Address to which the board will respond is selected by poles 2, 3 and 4 of SWc, as detailed in the table below. To select the required decode, set SWc 2, 3 & 4 ON where a 0 is indicated, and OFF where a 1 is indicated. Also take note of the special cases.

A18	A17	A16	EX. ADD.	SWc(4)	SWc(3)	SWc(2)
L	L	L	0	on	on	on
L	L	H	1	on	on	off
L	H	L	2	on	off	on
L	H	H	3	on	off	off
H	L	L	4	off	on	on
H	L	H	5	off	on	off
H	H	L	6	off	off	on
H	H	H	7	off	off	off

3.4.1. Special cases

1) If the system Z80 CPU board does not support extended addressing, e.g. the Gemini GM811 and the Nascom 1 and 2, it is important that SWc 2, 3 and 4 are set to OFF. Note that in this instance the memory devices installed in the GM853/GM863 must not span more than 64K of address space.

2) If the system Z80 CPU board does not support extended addressing, but there is also a Gemini GM888 8088 CPU board in the system, then these switches may be set to any of the options above if access to the GM853/863 is required only from the GM888, but must be set to ON if access from the Z80 CPU board is also required.

3) If memory devices larger than 8K x 8 static RAMs or 2764s are used, then the GM853/863 will respond to more than one 64K Extended Address block, as detailed in the tables in this manual. Provided that the sockets selected are within a single 64K Extended Address block, then even if the system Z80 CPU board does not support extended addressing, all of the memory on the GM853/863 can be accessed, provided that the conditions in 1) and 2) above are noted.

3.5. RAMDIS selection

RAMDIS is normally generated by high priority memory (i.e. EPROM) and used to disable low priority memory (i.e. RAM), when RAM devices are in use set SWc pole 7 on. The RAMDIS signal is normally used to overlay low priority memory (e.g. RAM) with high priority memory (e.g. EPROM).

Normally if EPROMS are in use RAMDIS SWc (7) is set to OFF, which causes the generation of a RAMDIS signal when a read cycle access the board, for more information please see section 3.5.

3.6. Device type selection

For 8K X 8 Static RAM devices SWa/b 5, 6 & 7 should be set to ON, the other settings of these switches are for when EPROM devices are in use.

Five different types of memory devices may be selected with the appropriate setting of SWa/b 5, 6 & 7. The table below details the various options.

Pole	SWa/b 5	SWa/b 6	SWa/b 7
8K x 8 static RAM	on	on	on
2764 EPROM	on	on	off
27128 EPROM	on	off	off
27256 EPROM	off	on	off
27512 EPROM	off	off	off

If two different sizes of memory devices are used in the two banks, and bank A contains smaller devices than bank B, then it is possible for the two banks to overlap. One of each of any sockets that overlap should be disabled (see the following section). To determine the address at which each socket will be enabled please see the tables in the first Appendix.

It should be noted that the two banks of memory are independent, and information should be taken separately from the tables for the memory devices in use in each bank.

3.7. Socket enabling

If a memory socket is to be used it needs to be enabled. Set to ON the switches appropriate to the sockets that you wish to use; if you do not wish to use a particular socket set the switch to OFF.

Socket in use	Switch set to ON	Address (for 8K x 8 devices) from	to
A0 (IC12)	SWa (1)	0000	1FFF
A1 (IC14)	SWa (2)	2000	3FFF
A2 (IC19)	SWa (3)	4000	5FFF
A3 (IC24)	SWa (4)	6000	7FFF
B0 (IC11)	SWb (1)	8000	9FFF
B1 (IC13)	SWb (2)	A000	BFFF
B2 (IC18)	SWb (3)	C000	DFFF
B3 (IC23)	SWb (4)	E000	FFFF

It is possible to selectively enable different areas of memory. Only the sockets in use should be enabled, as all enabled sockets will enable the GM 853/863 and may, dependant upon the state of SWc (7), generate a RAMDIS signal which could disable external memory such as a RAM board.

3.8. Write enabling

It is possible for each of the two banks to be write enabled or write protected. To write enable block A set SWa (8) to on; to write enable block B SWb (8) to on.

If you are using battery backed up RAM and have placed your program in the RAM, the GM863/853 can be turned into the equivalent of a EPROM board by setting the banks to be write protected.

3.9. Power fail mode (GM863 only)

When the power supply on the GM863 falls below a preset level, the power-fail circuitry is triggered. It is possible to select one of two modes of operation for what happens next. In either case, the memory sockets will be disabled (from either read or write accesses) to protect their contents. However, if SWc (1) is set to UNLATCHED mode, then should the power supply rise back up above the preset level, the memory sockets will be enabled again.

If SWc (1) is set to LATCHED mode, then once a drop in the power supply level has triggered the power-fail circuitry, the memory sockets will NOT become enabled again unless two things occur. Firstly the power supply must rise back above the preset level, and then the software must do a WRITE to the Page Mode latch, at port OFFH. This WRITE need not correspond with the actual Page that has been selected by the switches on the GM863, but may be to any Page.

Note that the comments in the above paragraphs only apply to the bank(s) that are set to battery backup via the links on the 16 pin stripline connector.

4. INSTALLING MEMORY DEVICES

Once it has been determined what type of memory devices are to be installed in which socket on the GM853/863, it is important to ensure that they are inserted in the correct orientation. With the board positioned as described earlier, pin 1 of the socket is the bottom left hand pin. The end of the memory device indicating the pin 1 end normally has a small groove cut into it. Studying the other ICs on the GM853/863 will reveal the type of marking to look for.

ICs are normally shipped with their two rows of legs splayed slightly too far apart for them to be installed immediately. This can be rectified by holding the body of the IC between the thumb anf forefinger of each hand, with the IC legs pointing away from you, and pushing the row of legs gently against a hard surface, such as a desk, until they have bent slightly. Repeat this for the other row of legs.

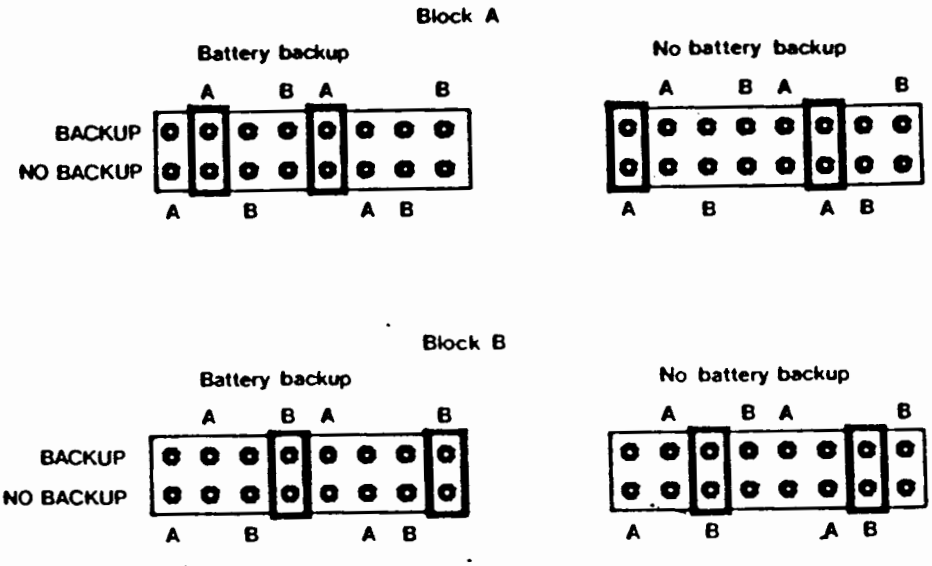
As each device is installed in its socket carefully look at it from all sides to ensure that all pins have gone into the corresponding receptacle in the socket.

5. BATTERY BACKUP (GM 863 only)

5.1. Battery backup links

IMPORTANT
Note that the GM863 is NOT normally shipped with the battery back-up links set for back-up operation. This is to conserve the battery life.

The GM 863 has provision for battery backup of one or both banks of memory, it is important that if EPROMs are used in one or both memory banks the links for battery backup are set to the correct position; if this is not done the high current consumption of the EPROMs will cause the battery to discharge in about half an hour. The link connections may easily be changed by moving the jumper blocks provided.



5.2. Further back-up information

The battery backup feature will retain the contents of the 8K X 8 static RAM devices for up to 45 days. It will take about six hours for the battery to become fully charged once system power is restored.

Care needs to taken when storing a GM863 to ensure that the backup power supply is not shorted, e.g. for example by the use of conductive foil to wrap the board.

5.3. Alternative battery types

Although the GM863 is normally shipped with a particular type of Nickel Cadmium cell, the board has been laid out so that other types may be used. For example, a circular cell carrier may be used, so that removable cells may be utilised. In addition certain types of non-rechargeable cells, such as Lithium cells, may be fitted.

If you wish to purchase further GM863 boards, manufactured with a different type of cell to that fitted as standard, then please contact your Gemini dealer.

IMPORTANT
Lithium cells, and certain other types of back-up power, do not need recharging. In fact to recharge them may result in them becoming damaged, or even exploding. If these types of cells are to be used in the GM863 you should ensure that the resistors R57 and R75 are removed from the board.

5.4. AUXPWR

The full 80-BUS specification specifies that bus line 64, AUXPWR, may be implemented in a system if required. This line is specified as an auxiliary +5 Volt supply for the use of back-up devices. Absolute maximum current that should be drawn from this line when the main supplies are off is given as 100mA.

The GM863 back-up circuit is connected to this line so that it may take its back-up power from the line, if it has been implemented in the host system. This means that back-up of the RAM contents will continue, even after GM863's own back-up cell has discharged.

5.5. /PWRF

The full 80-BUS specification specifies that bus line 63, /PWRF, may be implemented in a system if required. This is a power-fail warning line, and the host system should take this line low a minimum of 100mS before the power rails drop more than 5%, and hold it low until 100mS after the power-on reset.

The GM863 board is designed so that, in a system where this bus line is implemented, its change of state will take precedence over the GM863's own on-board power-fail detection circuitry.

5.6. Setting the threshold voltage

There is a small trimmer potentiometer, VR1, provided on the GM863 for setting the power-fail threshold voltage. The power supply level is constantly monitored by the GM863, and once it falls below the level determined by this potentiometer, the power-failure circuitry is activated, and the memory devices are disabled.

The level is factory set for 4.65 Volts, and it should not be necessary to change this. However, if your system is running at a particularly low voltage, or the power supply has an abnormal amount of ripple on its output, then the power fail detection circuitry may be spuriously triggered. Ideally this problem should be cured at source, by adjusting or replacing the power supply, but if this is not possible then the GM863 can be adjusted.

Set the power supply level to that at which the threshold voltage is to be set. Set switch SW c (1) to ON. With an oscilloscope on pin 8 of IC1 adjust VR1 until slight movements either way of VR1 cause the 'scope signal to switch between `0' and `1'. Seal the potentiometer to prevent further accidental movement, restore the power supply level to 5.00 Volts, and ensure that SW c (1) is set in the requiired position.

5.7. Battery backup

The battery backup feature has many diverse uses and in conjunction with the appropriate software will provide the system builder with a very powerful solution to particular problems.

One of the most useful applications for battery backed static RAM is as a "silicon" disk drive in situations where a single software package is used and the expense of a mechanical disk drive may be avoided. A good example of this is a data logger, data may be aquired and stored without concern for power failure and the mechanical problems associated with tape or disk drives.

It should be born in mind that when battery backup is used the memory contents will be retained as of the switching off of the system, a number of software packages use "scratchpad" areas, the contents of which change when the programme is run, a good example of this is BASIC, if the GM863 is used for the main system memory and the system is powered down, BASIC will be retained (along with the program) however it will probably not run as the "scratch pad" locations will not contain the correct values.

6. ON-BOARD LEDs

There are three LEDs that may be fitted to the top edge of the GM853/863. These indicate various accesses to the board, and can be useful in determining whether the controlling software is operating correctly.

6.1. RD

Whilst the GM853/863's selected Page is active, the LED D10 will indicate ANY READ cycle that occurs.

6.2. WR

Whilst the GM853/863's selected Page is active, the LED D11 will indicate ANY WRITE cycle that occurs.

6.3. ACCESS

The LED D12 illuminates when there is ANY access (memory or I/O, read or write) to the GM853/863 board.

7. SOFTWARE IMPLICATIONS

7.1. Page mode

With page-mode an entire memory board can be switched into or out of the memory map under software control. One particular IO port, port 0FFH, is reserved to control this function. The bits of the port are divided into two halves, the upper four bits are used to write-enable a board, and the lower four bits to read enable a board. To simplify the amount of logic necessary on the memory boards to implement this feature the four-bit fields are used directly and are not decoded further. The functions of the bits are shown below:

Bit	Function if set
7	Write enable page 3
6	" " " 2
5	" " " 1
4	" " " 0
3	Read enable page 3
2	" " " 2
1	" " " 1
0	" " " 0

The 64K of memory on GM813 is placed in page 0.

As there is no subsequent decoding of the data fields the onus lies on the programmer not to set up an invalid condition. For instance if the page-mode system is being used with all four pages in use, in general only one board can be read enabled at any one time. If a value such as 1FH is written into port 0FFH then when the Z80 attempts to read data from memory all four boards will attempt to put a byte on the data bus resulting in conflict between their data bus buffers and garbled data into the CPU. However it is perfectly possible to write-enable all of the boards simultaneously (by writing say 0F1H into port 0FFH) so that the same information can be written into each board.

In use the page-mode system requires a little thought to utilise in an application as the entire memory of the processor is switched. Either a common area of memory which is not switched has to be used to effect the transfer, or the identical program has to be written into the all the memory boards so that when the switch occurs the control program continues to run correctly.

7.2. Extended Addressing

GM813 supports an alternative method for extending the addressing capability of the Z80 - memory mapping. GM813 supplies 19 address lines to the 80-BUS rather than the 16 of the Z80. This means that the board can directly address 256K bytes of memory, although the Z80 can only "see" 64K of it at any one time. The extension in the addressing capability is achieved by putting mapping registers on the top four address lines. These registers are used to translate or "map" the top four address lines to seven address lines.

In GM813 the mapping is done by two 74LS189 TTL RAMs which are connected to give a 16 word x 8 bit register array. These RAMs, which are addressed by the top four address lines (A12-A15) of the Z80, supply the seven high address lines (A12-A19) to the 80-BUS from their data outputs. As any value may be written into the RAM registers it possible to arrange for any 4K segment of the Z80's 64K physical address space to access any 4K segment in the 256K address space of the 80-BUS.

On Reset the system monitor initialises each register of the 74LS189s with its own address, thus the 16 registers 0-F contain the data bytes 00-0F. This means that initially there is no difference between the Z80's output address, and the address put out on the 80-BUS. However if we program say 2E into mapping register 0, then whenever the Z80 accesses an address in the range 0XXX the actual physical address put onto the bus will be 2EXXX.

This approach has a distinct advantage over page mode in that the system's memory can be re-allocated in amounts of 4K at a time, not entire memory boards. In fact the mapping scheme can work quite successfully with just the standard 64K of memory. Consider a real-time task that has to handle say seven identical machines. Let us assume that the control program is contained in the bottom 12K of memory and requires additional workspace for each machine controlled. When switching tasks the program has to switch workspaces. Without memory mapping this would have to be done by either saving the current data and copying in the new, or by writing the program so that all data was accessed indirectly via one of the index registers which could then be changed to point to the new data area. However with memory mapping, the program can be written to use a fixed area of memory at say 3000H. The data areas for the tasks can then be allocated to 4000H, 5000H, 6000H, 7000H, and so on. Then to switch to task 3 it is only necessary to write a 6 into mapping register 3. Thereafter any memory reference in the range 3XXX will actually be mapped to a physical address of 6XXX. To switch to the next task it is only necessary to write a 7 into mapping register 3, and so on.

7.2.1. Writing to the mapping registers

To simplify the hardware required to implement the memory-mapping feature of GM813, use is made of the special Z80 OUT instruction "OUT r,(C)", where the output port is indirectly addressed by register C. When this instruction is executed, the port address (register C) is placed on the low address lines (A0-A7) of the address bus, and register B appears on the high address lines (A8-A15). This means that the four most significant bits of register B will address the memory-mapping RAMs. If an OUT instruction is performed to port 0FEH then a write strobe will be generated for the 74LS189s to latch whatever is on the data bus into the memory-mapping register selected by A12-A15. For example to write 2EH into memory mapping register 7 the following sequence of instructions should be executed:

```
LD   A,2EH          ;Data to be written
LD   B,70H          ;B high nibble = register address
LD   C,0FEH         ;C = memory-mapping port
OUT  (C),A          ;Write data into the selected register
```

The 74LS189s actually provide inverted data at their outputs, so an inverting buffer (IC45) is used for the 7 high address lines to correct for this. (It saves the programmer from some mental effort!)

8. TROUBLE SHOOTING

The first area to check when a problem occurs is the switch settings; it is easy for switches to inadvertently be moved when inserting or removing the board from the system. If you have a custom configuration it is suggested that the switch settings be noted down so that they may easily be checked.

Operation of the board may be effected by other boards in the system or the system itself. Noise is a problem with many older systems, the problem can be cured with thick ground wires.

If you think the board may be faulty, please note down in detail all the symptoms and return the unit to your Gemini dealer for repair. It is important that as much information as possible be provided particularly if the problem is intermittent.

A. MEMORY SOCKET ADDRESSES

The following tables give the address of each socket, different tables being given for the different possible sizes of memory devices used. Note that Block A (sockets A0-A3) and Block B (sockets B0-B3) are totally independant of each other, and so if there are different size devices in use in the two banks, care must be taken to ensure that the correct sections of the two relevant tables are used.

IMPORTANT. The setting of SWc is, 0 = ON, 1 = OFF.

A.1. 8K x 8 RAMs and 2764 EPROMs

SW c (extended address switch)			Socket number							
			Block A				Block B			
2	3	4	0	1	2	3	0	1	2	3
0	0	0	0 0000 - 1FFF	0 2000 - 3FFF	0 4000 - 5FFF	0 6000 - 7FFF	0 8000 - 9FFF	0 A000 - BFFF	0 C000 - DFFF	0 E000 - FFFF
1	0	0	1 0000 - 1FFF	1 2000 - 3FFF	1 4000 - 5FFF	1 6000 - 7FFF	1 8000 - 9FFF	1 A000 - BFFF	1 C000 - DFFF	1 E000 - FFFF
0	1	0	2 0000 - 1FFF	2 2000 - 3FFF	2 4000 - 5FFF	2 6000 - 7FFF	2 8000 - 9FFF	2 A000 - BFFF	2 C000 - DFFF	2 E000 - FFFF
1	1	0	3 0000 - 1FFF	3 2000 - 3FFF	3 4000 - 5FFF	3 6000 - 7FFF	3 8000 - 9FFF	3 A000 - BFFF	3 C000 - DFFF	3 E000 - FFFF
0	0	1	4 0000 - 1FFF	4 2000 - 3FFF	4 4000 - 5FFF	4 6000 - 7FFF	4 8000 - 9FFF	4 A000 - BFFF	4 C000 - DFFF	4 E000 - FFFF
1	0	1	5 8000 - 9FFF	5 A000 - BFFF	5 C000 - DFFF	5 E000 - FFFF	5 0000 - 1FFF	5 2000 - 3FFF	5 4000 - 5FFF	5 6000 - 7FFF
0	1	1	6 0000 - 1FFF	6 2000 - 3FFF	6 4000 - 5FFF	6 6000 - 7FFF	6 8000 - 9FFF	6 A000 - BFFF	6 C000 - DFFF	6 E000 - FFFF
1	1	1	7 0000 - 1FFF	7 2000 - 3FFF	7 4000 - 5FFF	7 6000 - 7FFF	7 8000 - 9FFF	7 A000 - BFFF	7 C000 - DFFF	7 E000 - FFFF

A.2. 27128 EPROMs

SW c (extended address switch) 2 3 4	Socket number: Block A 0	Block A 1	Block A 2	Block A 3	Block B 0	Block B 1	Block B 2	Block B 3
0 0 0	0 0000 - 3FFF	0 4000 - 7FFF	0 8000 - B000	0 C000 - FFFF	1 0000 - 3FFF	1 4000 - 7FFF	1 8000 - B000	1 C000 - FFFF
1 0 0	1 0000 - 3FFF	1 4000 - 7FFF	1 8000 - B000	1 C000 - FFFF	0 0000 - 3FFF	0 4000 - 7FFF	0 8000 - B000	0 C000 - FFFF
0 1 0	2 0000 - 3FFF	2 4000 - 7FFF	2 8000 - B000	2 C000 - FFFF	3 0000 - 3FFF	3 4000 - 7FFF	3 8000 - B000	3 C000 - FFFF
1 1 0	3 0000 - 3FFF	3 4000 - 7FFF	3 8000 - B000	3 C000 - FFFF	2 0000 - 3FFF	2 4000 - 7FFF	2 8000 - B000	2 C000 - FFFF
0 0 1	4 0000 - 3FFF	4 4000 - 7FFF	4 8000 - B000	4 C000 - FFFF	5 0000 - 3FFF	5 4000 - 7FFF	5 8000 - B000	5 C000 - FFFF
0 1 1	6 0000 - 3FFF	6 4000 - 7FFF	6 8000 - B000	6 C000 - FFFF	7 0000 - 3FFF	7 4000 - 7FFF	7 8000 - B000	7 C000 - FFFF
1 1 1	7 0000 - 3FFF	7 4000 - 7FFF	7 8000 - B000	7 C000 - FFFF	6 0000 - 3FFF	6 4000 - 7FFF	6 8000 - B000	6 C000 - FFFF

A.3. 27256 EPROMs

SW c (extended address switch) 2 3 4	Socket number: Block A 0	Block A 1	Block A 2	Block A 3	Block B 0	Block B 1	Block B 2	Block B 3
0 0 0	0 0000 - 7FFF	0 8000 - FFFF	1 0000 - 7FFF	1 8000 - FFFF	2 0000 - 7FFF	2 8000 - FFFF	3 0000 - 7FFF	3 8000 - FFFF
0 1 0	2 0000 - 7FFF	2 8000 - FFFF	3 0000 - 7FFF	3 8000 - FFFF	0 0000 - 7FFF	0 8000 - FFFF	1 0000 - 7FFF	1 8000 - FFFF
0 0 1	4 0000 - 7FFF	4 8000 - FFFF	5 0000 - 7FFF	5 8000 - FFFF	6 0000 - 7FFF	6 8000 - FFFF	7 0000 - 7FFF	7 8000 - FFFF
0 1 1	6 0000 - 7FFF	6 8000 - FFFF	7 0000 - 7FFF	7 8000 - FFFF	4 0000 - 7FFF	4 8000 - FFFF	5 0000 - 7FFF	5 8000 - FFFF

A.4. 27512 EPROMs

SW c (extended address switch)			Socket number								
			Block A				Block B				
2	3	4	0	1	2	3	0	1	2	3	
0	0	0	0 0000 - FFFF	1 0000 - FFFF	2 0000 - FFFF	3 0000 - FFFF	4 0000 - FFFF	5 0000 - FFFF	6 0000 - FFFF	7 0000 - FFFF	

B. EXAMPLE CONFIGURATION SETTINGS

Detailed below are some example settings of the switches, if you wish to have a custom configuration and are unsure as to how to work out the various switch setting you may find it instructive to work through an example setting.

B.1. 8 8k x 8 RAMs

Device type; 8K X 8 RAM

Socket(s) used; 0 - 7 Page number; 0

Start address; 0000 Extended address; not used

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X					X	X	X	X
off																	X	X	X	X				

B.2. 8 8K x 8 RAMs

Device type; 8K x 8 RAM

Socket(s) used; 0 - 7 Page number; 0

Start address; 0000 Extended address; 0 0000

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
off																								

B.3. 1 x 2764 EPROM

Device type; 2764

Socket used; 7 Page number; 0

Start address; E000 Extended address; 0

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on												X	X	X			X	X	X	X	X	X		
off	X	X	X	X	X	X	X	X	X	X	X				X	X							X	X

B.4. 1 x 2764 EPROM

Device type; 2764

Socket used; 0 Page number; 2

Start address; 0000 Extended address; not used

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on	X				X	X														X				
off		X	X	X			X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X

B.5. 1 x 2764 EPROM

Device type; 2764

Socket used; 5 Page number; 1

Start address; A000 Extended address; 0

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on										X			X	X			X	X	X	X		X		
off	X	X	X	X	X	X	X	X	X		X	X			X	X					X		X	X

B.6. 1 x 2764 EPROM

Device type; 2764

Socket used; 4 Page number; 0

Start address; 8000 Extended address; 0

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on									X				X	X			X	X	X	X	X	X		X
off	X	X	X	X	X	X	X	X		X	X	X			X	X							X	

B.7. 1 x 27128 EPROM

Device type; 27128

Socket used; 2 Page number; 3

Start address; 8000 Extended address; 4

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on			X		X												X	X	X					
off	X	X		X		X	X	X	X	X	X	X	X	X	X	X				X	X	X	X	X

B.8. 1 x 27128 EPROM

Device type; 27128

Socket used; 0 Page number; 0

Start address; 0000 Extended address; 0

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on	X				X												X	X	X	X	X			
off		X	X	X		X	X	X	X	X	X	X	X	X	X	X							X	X

B.9. 1 x 27256 EPROM

Device type; 27256

Socket used; 3 Page number; 1

Start address; 8000 Extended address; 3

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on				X		X												X		X		X		
off	X	X	X		X		X	X	X	X	X	X	X	X	X	X	X		X		X		X	X

B.10. 2 x 27128 EPROMs

Device type; 27128 x 2

Sockets used; 2, 3 Page number; 3

Start address; 8000 - B000 C000 - FFFF Extended address; 4

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on			X	X	X												X	X						
off	X	X				X	X	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X

B.11. 4 x 27128 EPROMs

Device type; 27128 X 4

Socket(s) used; 0, 1 2 3

Start address; 0000 - 3FFF 4000 - 7FFF 8000 - B000 C000 - FFFF

Page number; 0

Extended address; 0

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on	X	X	X	X	X												X	X	X	X	X	X		
off						X	X	X	X	X	X	X	X	X	X	X							X	X

B.12. 1 x 27512 EPROM

Device type; 27512

Socket used; 3 Page number; 1

Start address; 0000 Extended address; 3

	SW a								SW b								SW c							
	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
on				X														X	X	X		X		
off	X	X	X		X	X	X	X	X	X	X	X	X	X	X	X	X				X		X	X
