Work implemented :	Charge Pump Design	Date: 05-06/03/2020
Department where work will be implemented:	Research and Development	

Charge pump

There are some circuits which need a method to convert the width of input pulses into currents which can then be converted into voltages at subsequent stages. For this a Charge Pump (CP) block is utilized. CP, as the name suggests, acts like a pump which charges something. The conventional CP circuit is shown in Figure 1.

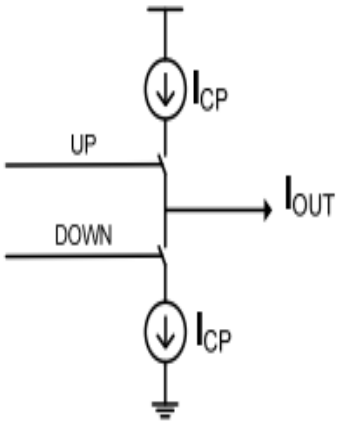


Figure 1

The CP circuit should ideally behave as described in Table 1.

UP	DOWN	IOUT
0	0	0
0	1	-ICP
1	0	+ICP
1	1	0

Table 1: Charge Pump Functionality

A conventional CP circuit is shown in Figure 2. The inverter just after the UP input in Figure 2 is added because of the technology being used. A high input to the transistor Q1 in Figure 2 turns the transistor off and thus the output node of CP will not be charged, but we need to pass current through Q1 when UP signal

is high. This is the reason for adding an inverter right after the UP signal. There will be a couple of more additions to this circuit because inverting the UP signal creates some delays. Thus, the proper UP and DOWN signals do not arrive at the same time at the inputs of the Q1 and Q2 transistors. For the solution of this problem there are different methods that can be used. The most usual solution is passing the DOWN signal through an always ON transmission gate that is able to produce almost the same delay the inverter is causing in the UP signal.

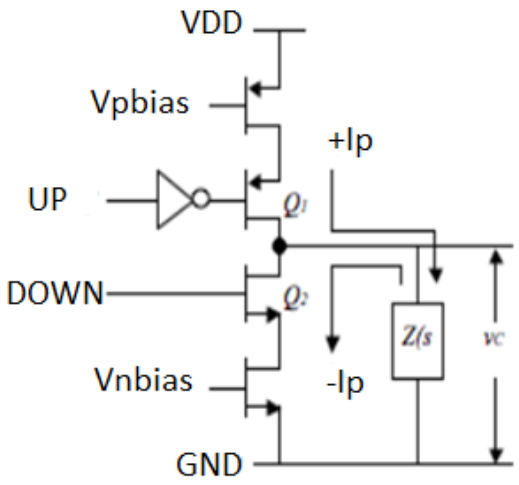


Figure 2

Having said that, the design of the CP circuit is very easy. For this block it will be necessary to know the unCox and upCox of nmos and pmos transistors as they will be used to produce the correct currents in the circuit. The TSMC0.18 transistors have the parameters shown in Figure 3.

Parameter	Symbol	N MOS	P MOS	Unit
Maximum supply voltage	$V_{DD,max}$	1.8		V
Zero-bias threshold voltage	V_{th0}	0.50	−0.48	V
Bulk effect parameter	γ	0.42	−0.67	$\sqrt{V}$
Twice Fermi potential	$2\phi_F$	0.87	−0.90	V
Zero-bias sub-threshold slope	n	1.31	−1.29	
Channel length modulation constant	k_2	0.041	−0.039	$\mu m/V$
Current factor	$K' = \mu C_{ox}$	316	−62	$\mu A/V^2$
Gate area capacitance	C_{ox}	8.4	8.4	$fF/\mu m^2$
Gate width overlap capacitance	C_{ov}	0.72	0.68	$fF/\mu m$
Junction area zero-bias capacitance	C_{j0}	1.0	1.2	$fF/\mu m^2$
Junction perimeter zero-bias capacitance	C_{jsw0}	0.25	0.20	$fF/\mu m$
Flicker noise coefficient (not KF)	K_f	$3.3 \cdot 10^{-25}$	$1.6 \cdot 10^{-25}$	J
Minimum channel length	L_{min}	0.18		μm
Typical source/drain length	ℓ_{SD}	0.6		μm
Mosis scalable design rules unit	λ_{SUBM}	0.1		μm
Thermal voltage (kT/q)	V_T	26		mV

Figure 3

Initially current mirrors which are supplying charging and discharging currents to the output node of the CP are designed. The first one to be built is the PMOS current mirror. Using the values in the Figure 3, it is calculated that for an Id = 250uA, the transistor W/L and R2 of Figure 4 should respectively be 2.5u/180n and 1.31 K ohms. For these values, the transistor stands in saturation with a Vov = 356.9mV and most

importantly it has 250uA of current flowing. This will create the appropriate VP_{BIAS} in Figure 2 as shown in Figure 4.

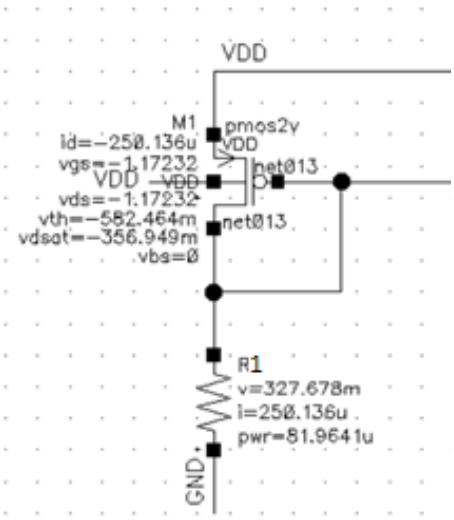


Figure 4

Using the same logic with the NMOS current mirror, we can have 250uA of current by having R_2=1.3k and W/L_2 = 1u/0.18u as shown in Figure 5.

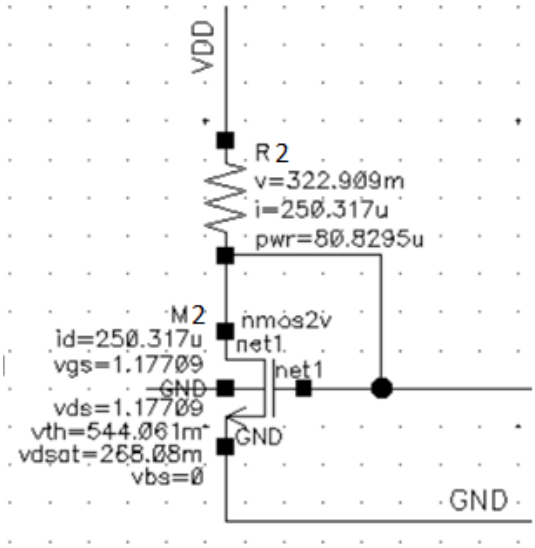


Figure 5

The complete circuit including the delay equalizing elements of the UP and DOWN inputs is shown in Figure 6.

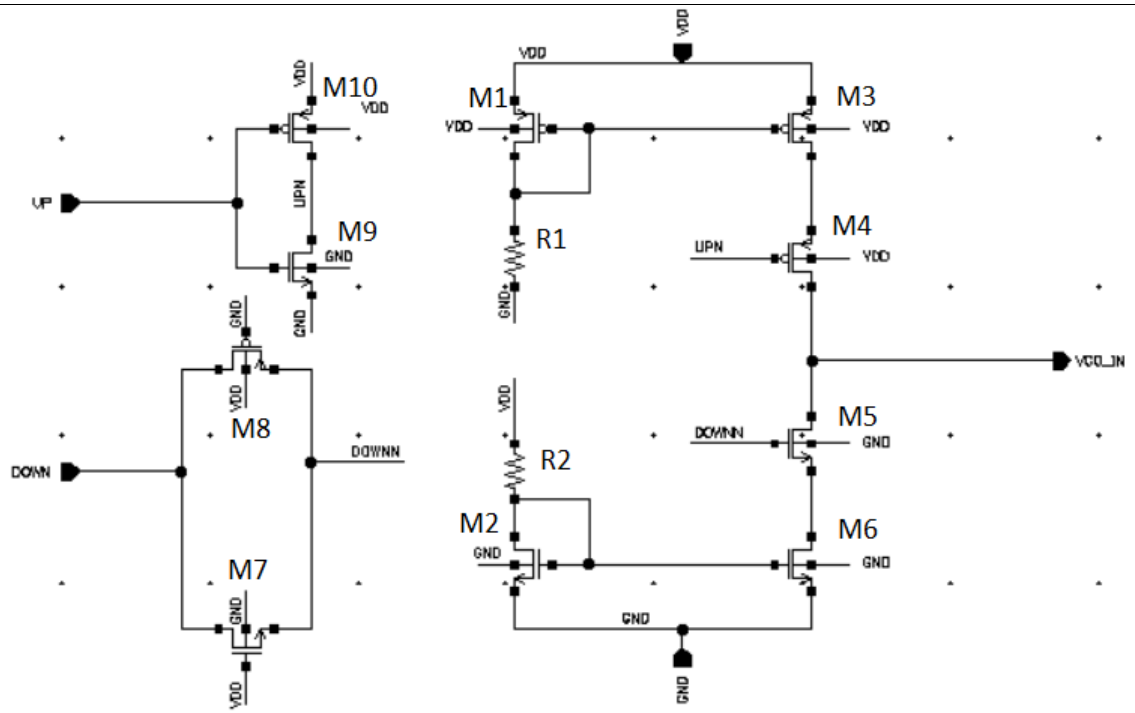


Figure 6

Transistor sizes M3 – M12 are shown in Table 2.

Transistor	M3	M4	M5	M6-M7	M8	M9	M10
W/L	2.5/0.18	20/0.18	10/0.18	1/0.18	2/0.18	0.45/0.18	0.9/0.18

Table 2: Transistor sizes for CP circuit

Figures 7 and 8 are the simulations of the CP circuit. In Figure 7, CP inputs are two square signals of the same frequency but out of phase. For the red signal, the phase difference is 2ns. For the blue signal, the phase difference is 6ns. Clearly, for greater phase differences, the output of the charge pump charges faster.

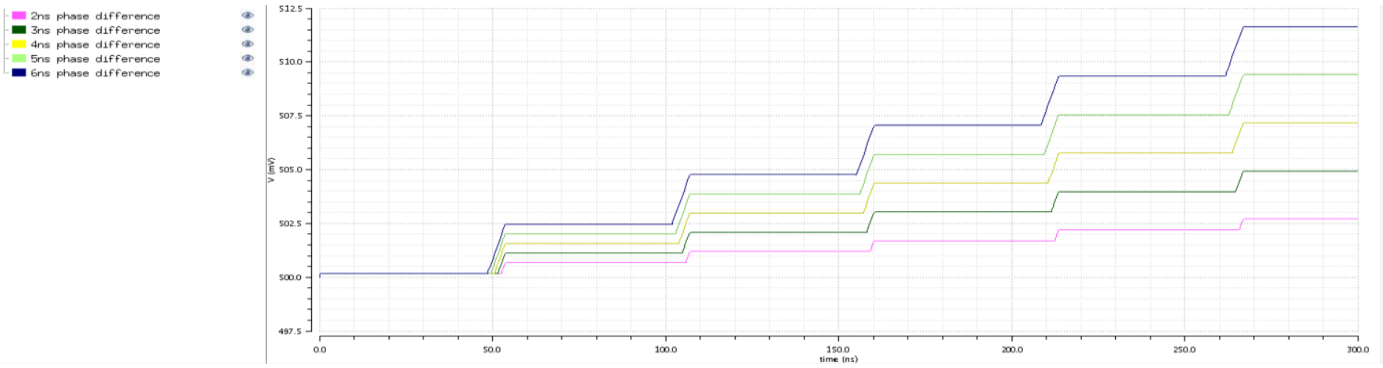


Figure 7

In Figure 8, CP inputs are two square signals of the same frequency but out of phase. For the red signal, the phase difference is 2ns. For the green signal, the phase difference is 6ns. Clearly, for greater phase differences, the output of the charge pump discharges charges faster.

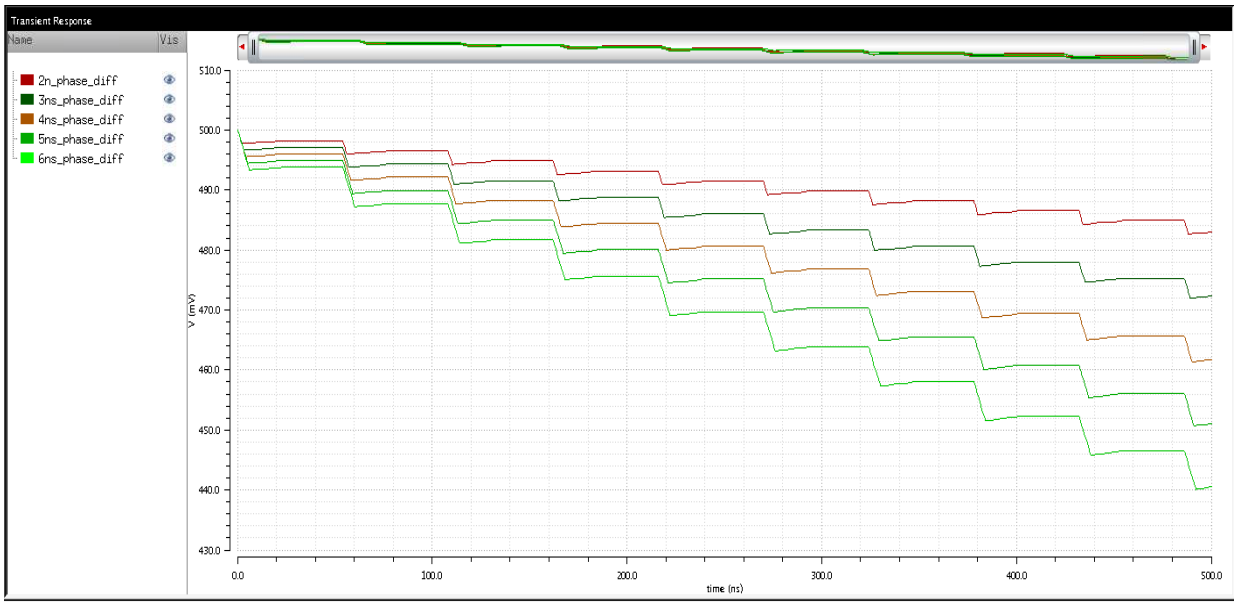


Figure 8

STUDENT Gerald Topalli	APPROVED	Company Authority Signature

Work implemented :	LC VCO Design	Date: 07,12/03/2020
Department where work will be implemented:	Research and Development	

The voltage-controlled oscillator (VCO) is a very important block in communication systems because it does not consume a lot of power, and it has a wide frequency range of operation. VCO-s use amplification, feedbacks and resonant circuits to generate a repeating voltage waveform at a particular frequency. VCO-s are important parts of phase-locked loops, clock recovery circuits and frequency synthesizers. The requirements of VCO include high frequency, low power consumption, phase stability, large linearity and large gain factor.

An ideal VCO is represented by the following equation:

$$\mathbf{fout = Kvco \cdot Vin + fmin}$$

Figure 1 shows the ideal VCO equation.

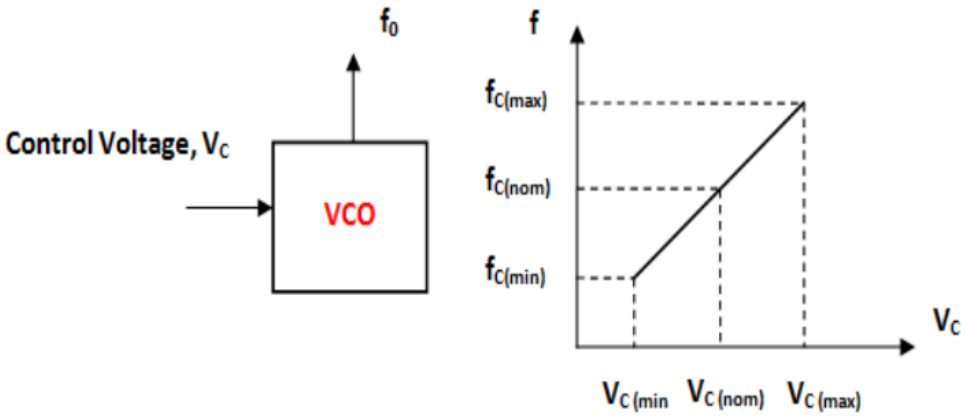


Figure 1

During these days the design of LC VCO was done. In theory, the frequency of the VCO should be linearly controlled by the input voltage but because of device parasitic and imperfections, the circuit will not have a perfect linear behavior. Usually the VCO is required to be linear over some specific region. For this internship, we will design a VCO whose center frequency is around 2.4GHz. Figure 2 shows the transistor level of an LC VCO.

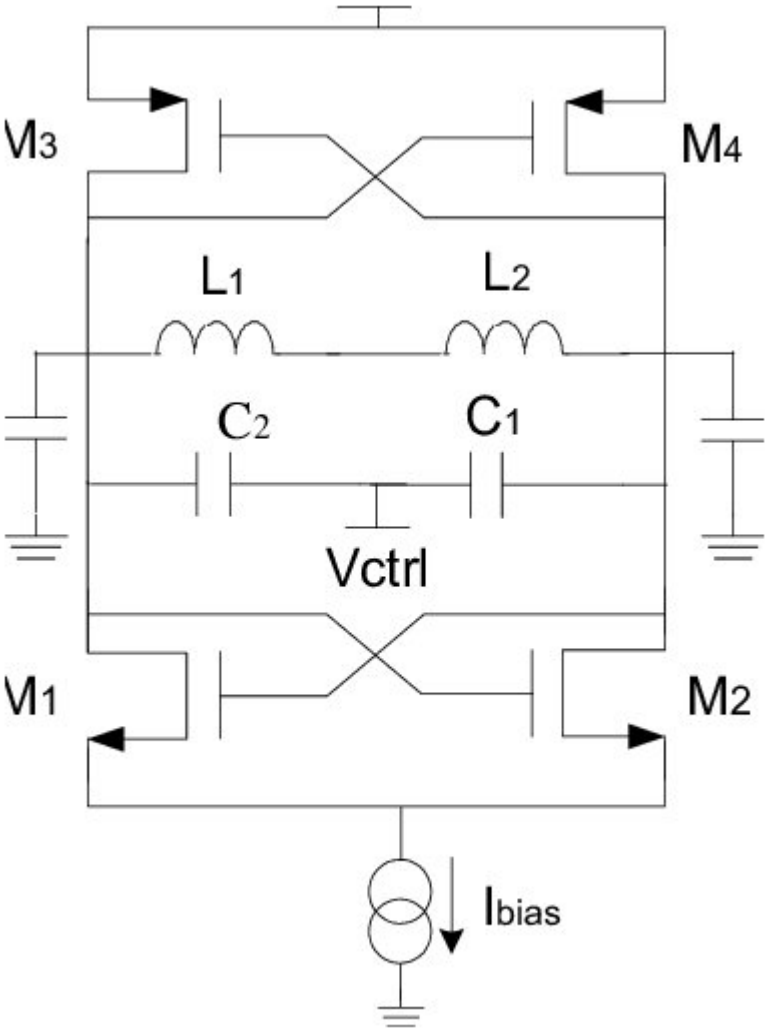


Figure 2

The C1 and C2 in Figure 2 are very important elements as they are used to alter the output frequency of the VCO. NMOS transistor-based varactors are used on this design to sweep the frequency of the output of VCO circuit.

At ω = 1 /√ ($L1 \cdot C1$), the LC tank completely resonates and the circuit starts to oscillate, filtering out most of the frequencies with exception to the resonating frequency. For this design $L1 = L2 = 1.75nF$.

In order to have the circuit oscillating at 2.4GHz, the total node capacitance should be: C1 = C2 = 2.51pF

if no virtual node capacitances are assumed. But since there are virtual capacitances coming from the $M_{1\text{-}4}$ transistors, we need to firstly determine how much node capacitance is present at the VCO output nodes. Only

then we will be able to determine how much capacitance is required by C_1 and C_2. Firstly, the oscillator part of the VCO is designed. This was preferable because the calculation of the capacitors of transistors $M_{1\text{-}4}$ in Figure 3 is quite difficult by hand calculations. Figure 3 shows the cross coupled oscillator and the varactors enclosed in the rectangle. M1-4 contain a lot of parasitic capacitors because they are big. They were intentionally selected big to satisfy the starting condition of the oscillator. Current mirror formed by transistors M5-6 is supplying current to the circuit. In order to have high gm transistors, high currents will be possible by means of the current mirror. The current mirror is supplying 3.5mA of current to the oscillator. By means of equations shown below, the sizes of M5-6 and resistor value were found.

$$\boldsymbol{\mu_n C_{ox} = 313 \frac{\mu A}{V^2}}$$

$$\boldsymbol{V_{ov\,5-6} = 0.2V}$$

$$\boldsymbol{\left(\frac{w}{L}\right)_n = \frac{2I_D}{\mu_n c_{ox}} \cdot (\frac{1}{v_{ov}})\text{^}2}$$

$$\boldsymbol{R = \frac{V_{DD} - (V_{ov} + V_{th})}{3.5mA}}$$

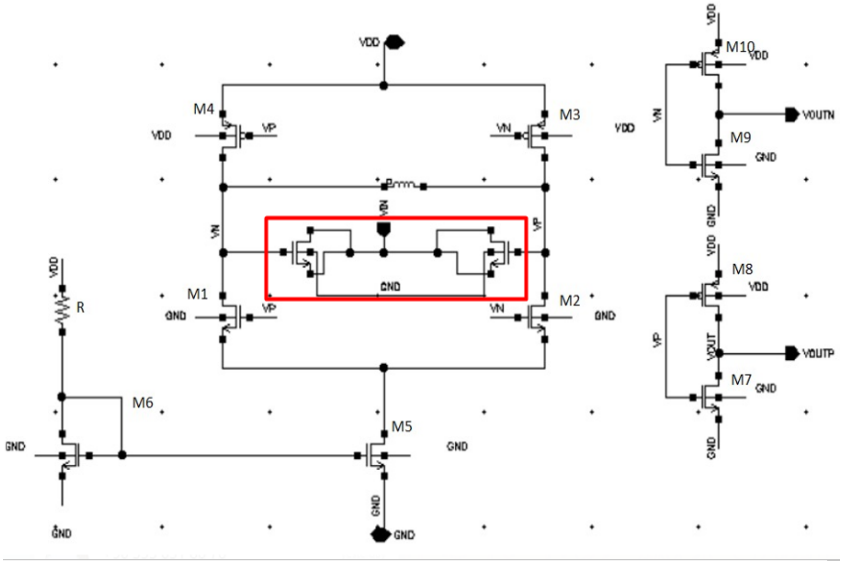


Figure 3

Table 1 shows the selected values for the oscillator in Figure 3. The resistance required is:

R = 234 ohms.

MOSFET	M1-M2	M3-M4	M5-6	M7 & M9	M8	M10
W/L	50/0.4	200/0.4	559/1	1/0.18	2/0.18	2/0.18

Table 1: Oscillator transistor sizes

Figure 4 shows the bias current of the current mirror used in Figure 3.

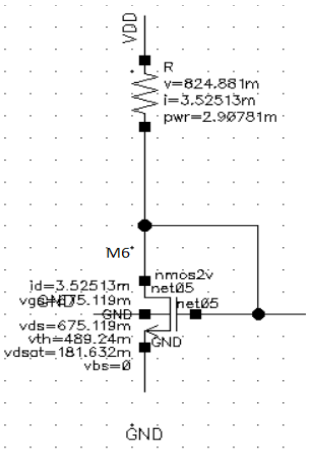


Figure 4

In Figure 5, the transient simulation of the oscillator in Figure 3.

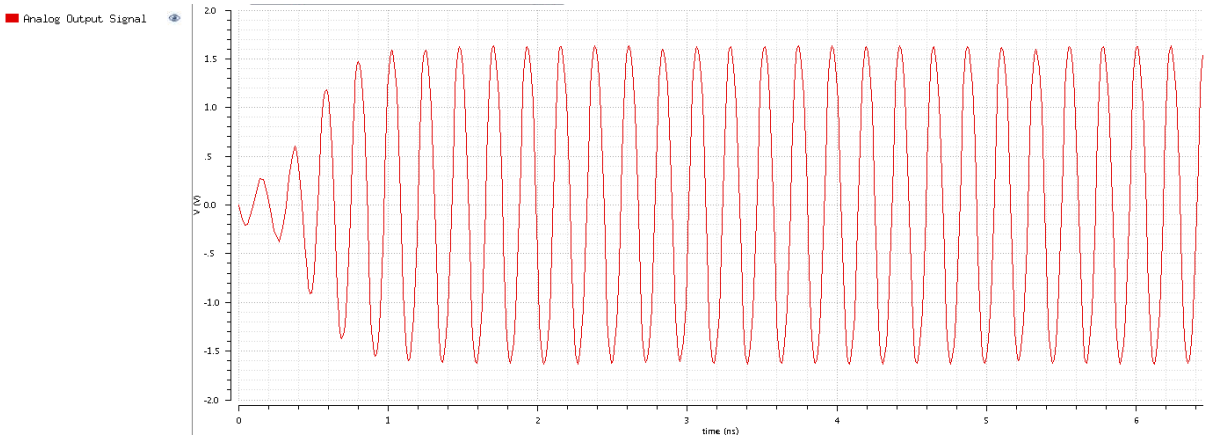


Figure 5

If the oscillator is not loaded with varactors, the oscillation frequency is 4.3 GHz. Based on calculations, the node to ground parasitic capacitance of both V_N and V_P is 0.753 pF. In order to make the oscillator work at 2.4GHz, the varactors should contribute with approximately 1.8 pF each. Using the TSMC transistor in the configuration shown in Figure 6 the behavior of NMOS

varactors can be analyzed as a function of V1. It would be great if we could make the varactor have parasitic capacitor values from 1pF to 2.6pF.

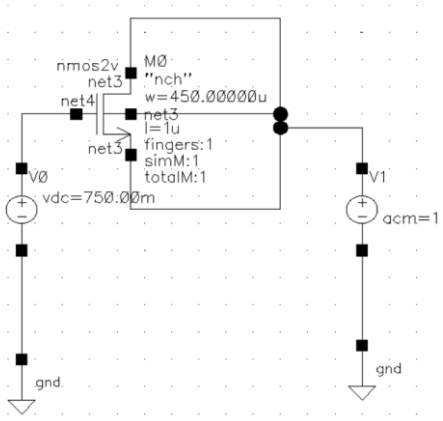


Figure 6

There is a way to measure the capacitance of a node. The equation that does that is shown in the following formula.

$$\boldsymbol{C(V) = \frac{I}{2\Pi f V}\Big|_{f=1}}$$

This equation can be implemented by means of an AC analysis in Cadence. Figure 7 shows how to configure the AC analysis in order to get the proper calculated value.

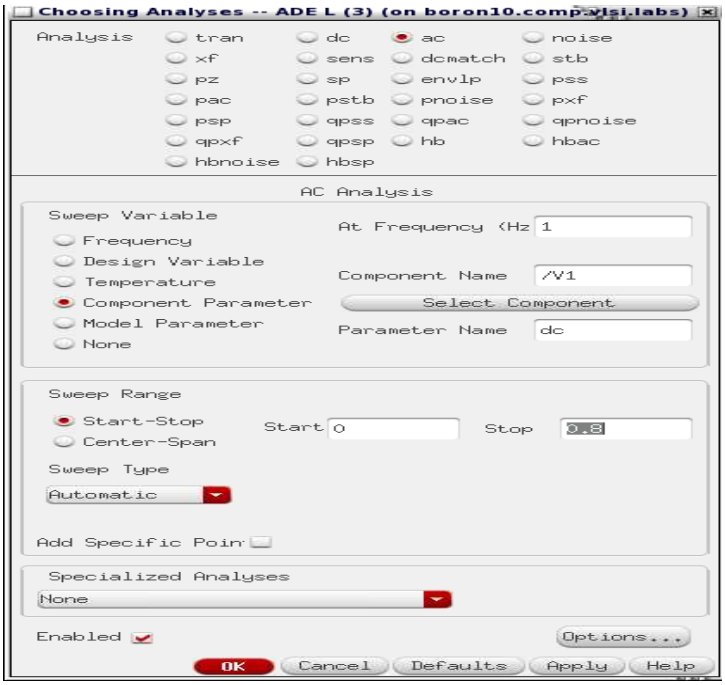


Figure 7

The selected W/L for the transistor in Figure 6 is 450um/1um. This value has been previously found by means of trial and error and parametric simulations of parasitic capacitances. This value provides 1pF to 4pF parasitic capacitance which can load the VCO and produce the correct range of frequencies. Figure 7 shows a plot of capacitance over a range of DC applied voltages.

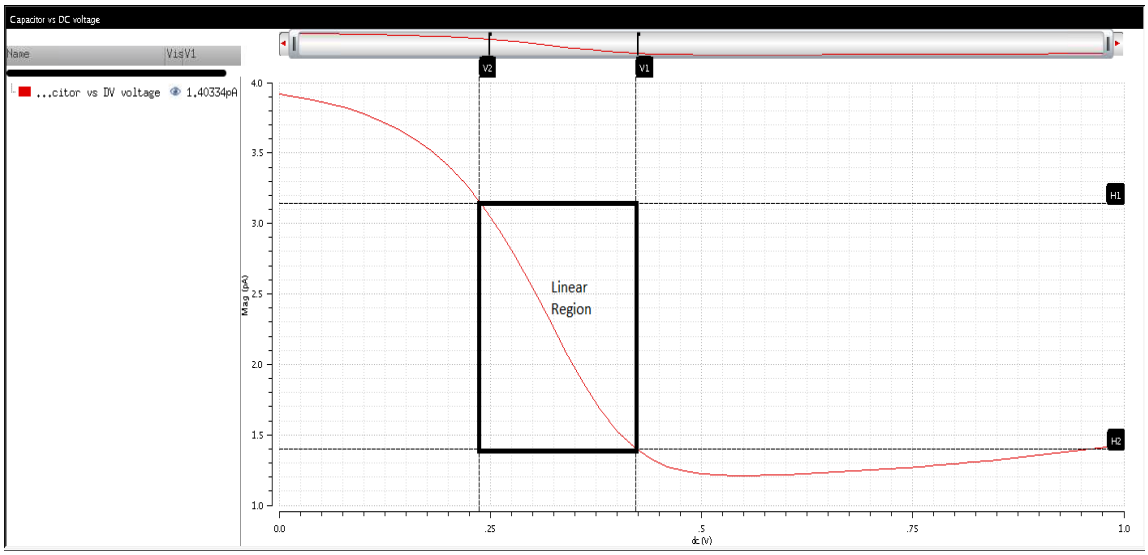


Figure 8

A PSS analysis can show the Frequency vs VCO_in plot as shown in Figure 9. The gain of VCO is:

K_{VCO} = 1.42 GHz/V

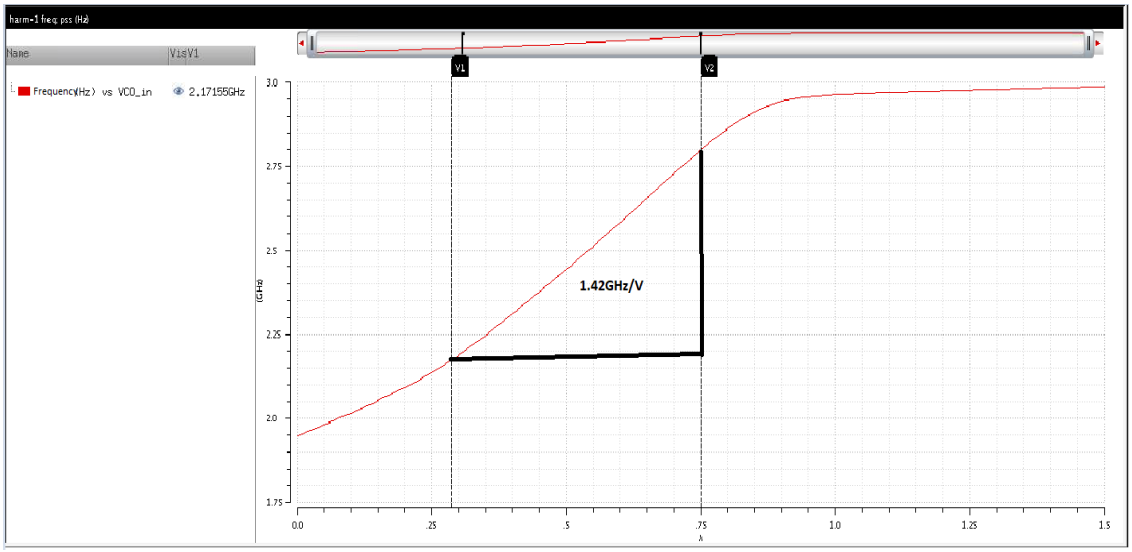


Figure 9

The phase noise of the VCO is shown in Figure 10. At 2.4GHz, the phase noise is: -155.89 dBc/Hz.

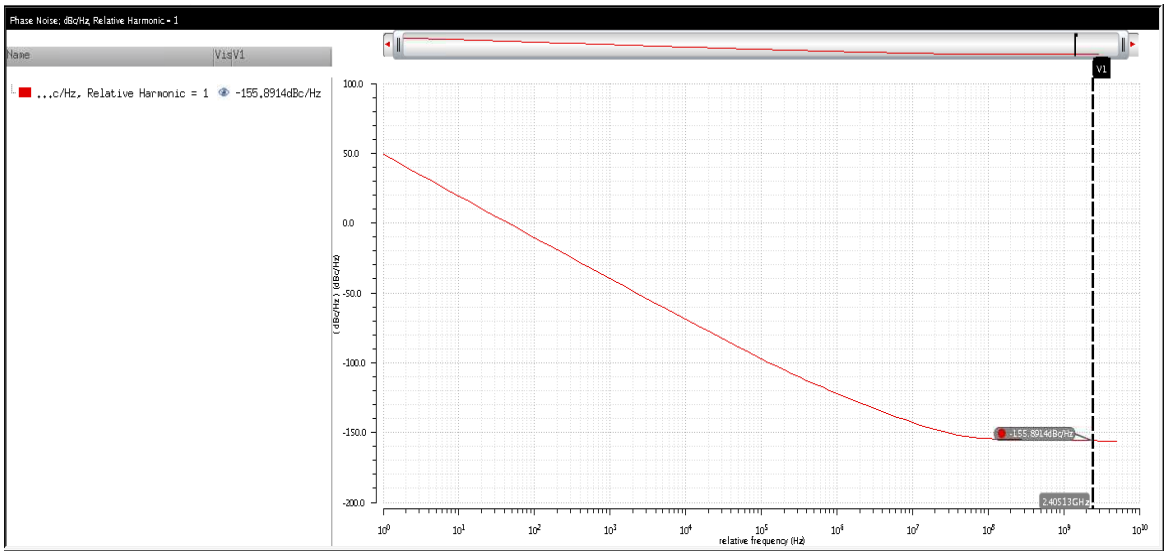


Figure 10

At 495mV, the VCO should oscillate at 2.4GHz. Figure 11 shows the transient simulation of the VCO.

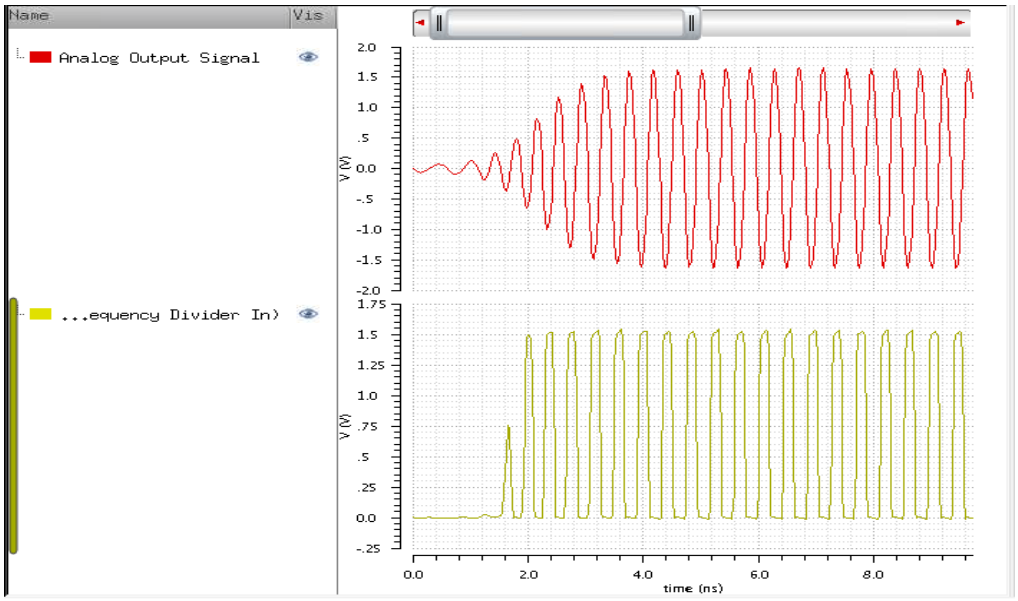


Figure 11

Figure 12 shows the DFT analysis for this input voltage. The output frequency is standing at 2.4 GHz but there are some other spikes at some very close frequencies which in fact are not dominant.

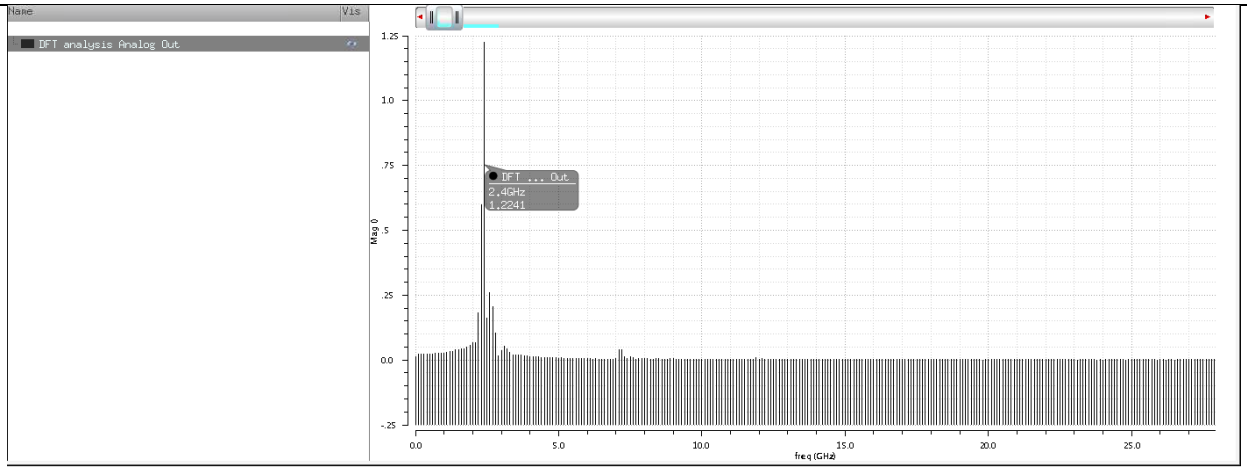


Figure 12

STUDENT Gerald Topalli	APPROVED	Company Authority Signature

Work implemented :	LC VCO Design	Date: 13,14/03/2020
Department where work will be implemented:	Research and Development	

Current Starved VCO is another very important voltage controll oscillator which is based on the ring oscillator. The current of each inverter in the ring oscillator is varied, making the nodes of the ring oscillator to charge and discharge faster or slower depending on the amount of current present. The schematic of the current starved VCO is shown in Figure 1.The current sources M1 and M4 control the current available to M2 and M3. The drain currents of M5 and M6 are the same and are determined by the input control voltage. The currents of M5 and M6 are mirrored to M4 and M5.

The total capacitance on the drains of M2 and M3 can be approximated like following:

$C_{tot} = C_{out} + C_{in}$

$C_{tot} = C_{ox} (W_p L_p + W_n L_n) + 3/2 * C_{ox} (W_p L_p + W_n L_n)$

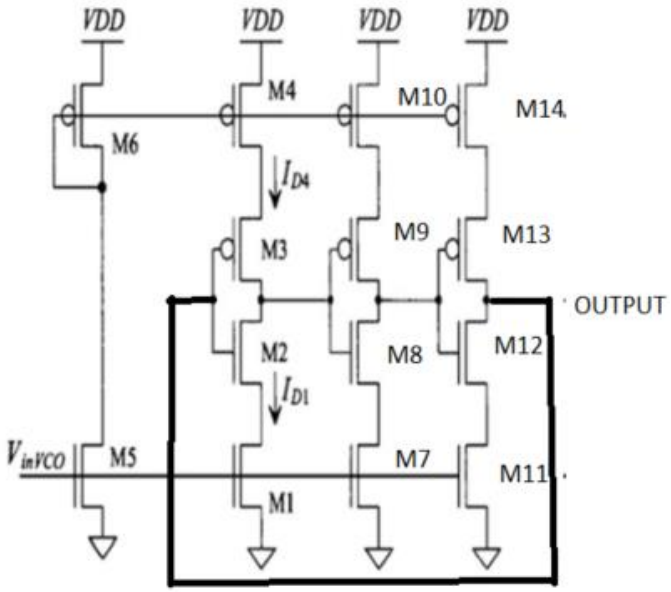


Figure 1

Knowing the parasistic capacitance at the nodes of ring oscillator cells, we can calculate the frequency of oscillation by means of the formula shown below:

$$f_{osc} = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}}$$

V_{DD} was selected to be 1.5 V whereas N = 3. The VCO should have a center frequency of 2.4 GHz. The first thing to do is to decide on the current biasing transistors of the VCO since they will be the ones controlling the I_D and thus the oscillation frequency. In Figure 1, the M5 drain current is shown with respect to the applied DC voltage. M6 is made a huge transistor compared to M5 in order to provide high current linearity as shown in Figure 2.

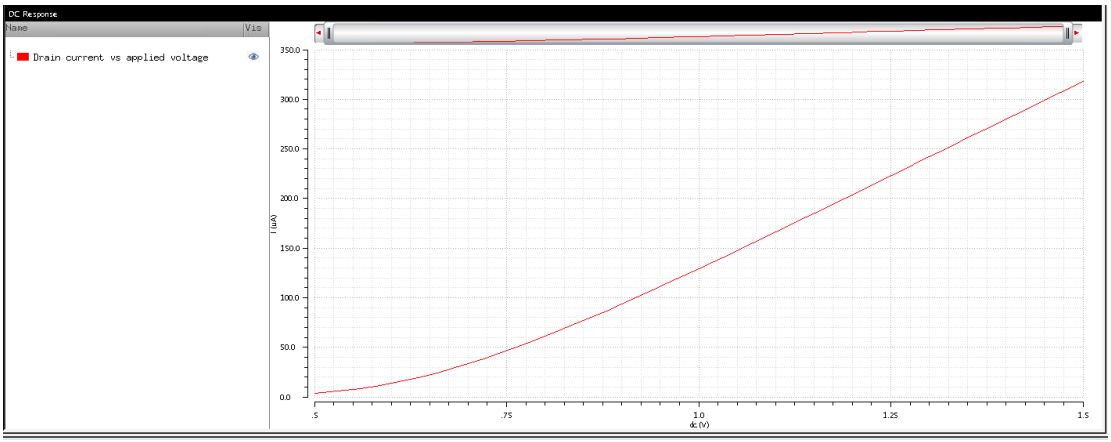


Figure 2

From the oscillation frequency formula and from trial and error, the appropriate sizes of the transistors in Figure 1 are as follows:

M6, M4, M10, M14 = 100u/0.18u

M1, M5, M7, M11 = 2u/0.18u

M2, M8, M12 = 1u/0.18u

M3, M9, M13 = 2u/0.18u

By doing a pss analysis to the final circuit the Frequency Gain of the Current Starved VCO is shown in Figure 3. The VCO gain is: 8.6 GHz / V

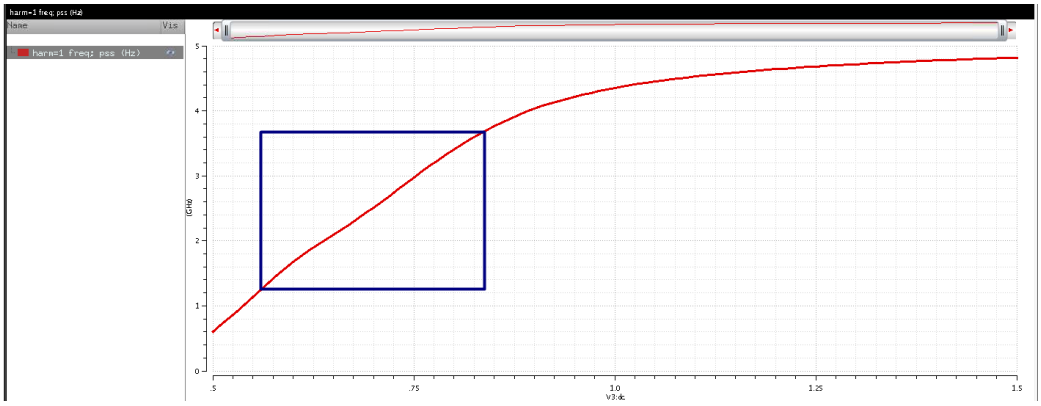


Figure 3

From Figure 3, 2.4 GHz is achieved for 687mV. Applying 687mV to the control voltage, the waveform shown in Figure 4 appears.

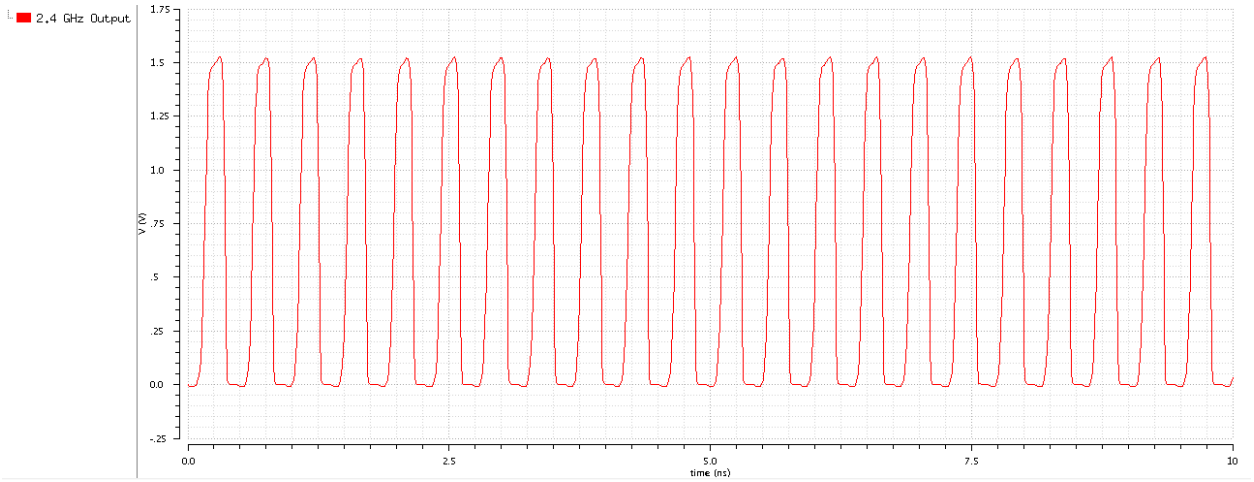
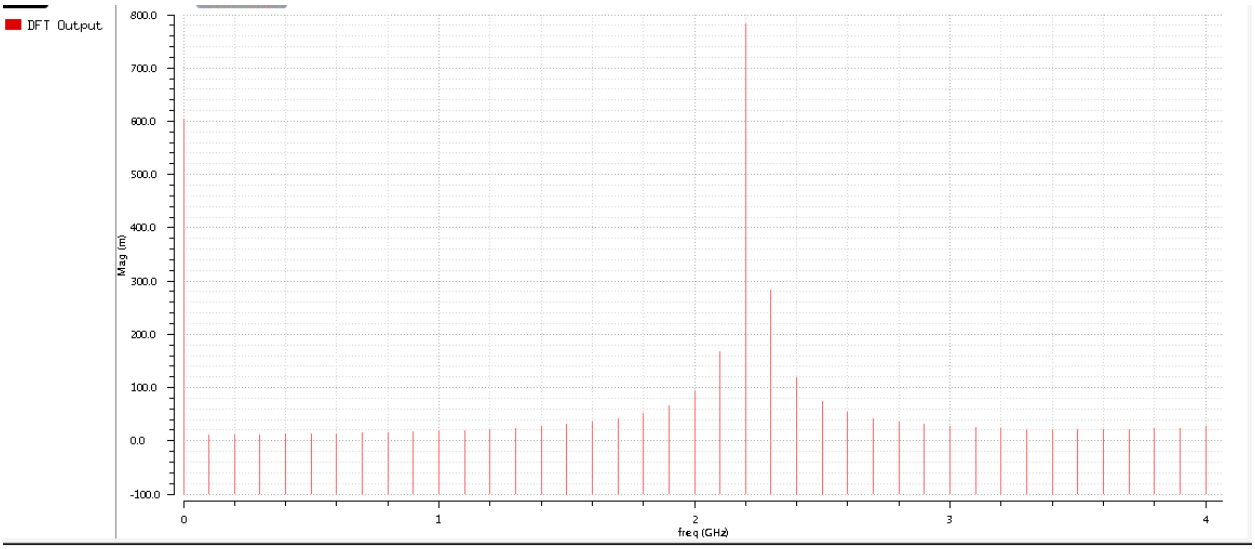


Figure 4

To confirm that the oscillating frequency is 2.4 GHz, I made a DFT analysis. According to the DFT analysis, the dominant harmonic is at 2.4 GHz.



This type of VCO is better than the LC VCO because it has a higher frequency gain and also its static power is minimal.

STUDENT Gerald Topalli	APPROVED	Company Authority Signature