Winner Micro 联盛德微电子

W801 Chip Specifications

V1.0

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1 Overview

The W801 chip is a secure IoT Wi-Fi/Bluetooth dual-mode SoC chip. The chip provides rich digital function interface. Support 2.4G IEEE802.11b/g/n Wi-Fi communication protocol; support BT/BLE dual-mode working mode, support BT/BLE4.2 protocol. Chip integrated 32-bit CPU processor with built-in UART, GPIO, SPI, I 2C, I 2S, 7816, SDIO, ADC, PSRAM, LCD, TouchSendor, etc. Digital interface; support TEE security engine, support a variety of hardware encryption and decryption algorithms, built-in DSP, floating-point arithmetic unit and security engine, support code Security permission setting, built-in 2MB Flash memory, support firmware encryption storage, firmware signature, security debugging, security upgrade and other security measures to ensure product safety features. Suitable for use in smart home appliances, smart homes, smart toys, wireless audio and video, industrial control, medical monitoring, etc. Broad IoT field.

2 Features

ÿ Chip appearance

- ÿ QFN56 package, 6mm x 6mm

ÿ MCU Features

- ÿ Integrated 32-bit XT804 processor, operating frequency 240MHz, built-in DSP, floating-point arithmetic unit and security engine
- ÿ Built-in 2MB Flash, 288KB RAM
- ÿ Integrated PSRAM interface, support up to 64MB external PSRAM memory
- ÿ Integrated 6-channel UART high-speed interface
- ÿ Integrate 4 channels of 16-bit ADC, the highest sampling rate is 1KHz
- ÿ Integrate 1 high-speed SPI interface, support up to 50MHz
- ÿ Integrate 1 master/slave SPI interface
- ÿ Integrate 1 SDIO_HOST interface, support SDIO2.0, SDHC, MMC4.2

ÿ Integrate 1 SDIO_DEVICE, support SDIO2.0, the maximum throughput rate is 200Mbps

ÿ Integrated PSRAM expansion interface, maximum support 64Mbyte

ÿ Integrate 1 I2C controller

ÿ Integrated GPIO controller, supports up to 44 GPIOs

ÿ Integrate 5 PWM interfaces

ÿ Integrated 1-way Duplex I 2S controller

ÿ Integrated LCD controller, support 4x32 interface

ÿ Integrate a 7816 interface

ÿ Integrate 15 Touch Sensors

ÿ Safety Features

ÿ The MCU has built-in Tee security engine, and the code can distinguish the secure world/non-secure world

ÿ Integrated SASC/TIPC, configurable security attributes of memory and internal modules/interfaces to prevent non-secure code access

ÿ Enable firmware signature mechanism for secure boot/upgrade

ÿ With firmware encryption function to enhance code security

ÿ Firmware encryption keys are distributed using asymmetric algorithms to enhance key security

ÿ Hardware encryption module: RC4256, AES128, DES/3DES, SHA1/MD5, CRC32, 2048 RSA, true random number

bionic device

ÿ Wi-Fi Features

ÿ Support GB15629.11-2006, IEEE802.11 b/g/n

ÿ Support Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS

ÿ Support EDCA channel access mode

ÿ Support 20/40M bandwidth working mode

ÿ Support STBC, GreenField, Short-GI, support reverse transmission

ÿ Support AMPDU, AMSDU

ÿ Support IEEE802.11n MCS 0~7, MCS32 physical layer transmission rate gear, transmission rate up to 150Mbps

ÿ Support Short Preamble when sending at 2/5.5/11Mbps

ÿ Support HT-immediate Compressed Block Ack, Normal Ack, No Ack response methods

ÿ Support CTS to self

ÿ Support Station, Soft-AP, Soft-AP/Station functions

ÿ Bluetooth Features

ÿ Integrated Bluetooth baseband processor/protocol processor, supports BT/BLE dual-mode working mode, supports BT/BLE4.2 protocol

ÿ Low Power Mode

ÿ 3.3V single power supply

ÿ Support Wi-Fi power saving mode power management

ÿ Support work, sleep, standby, shutdown working modes

ÿ Standby power consumption is less than 10uA

3 Chip structure

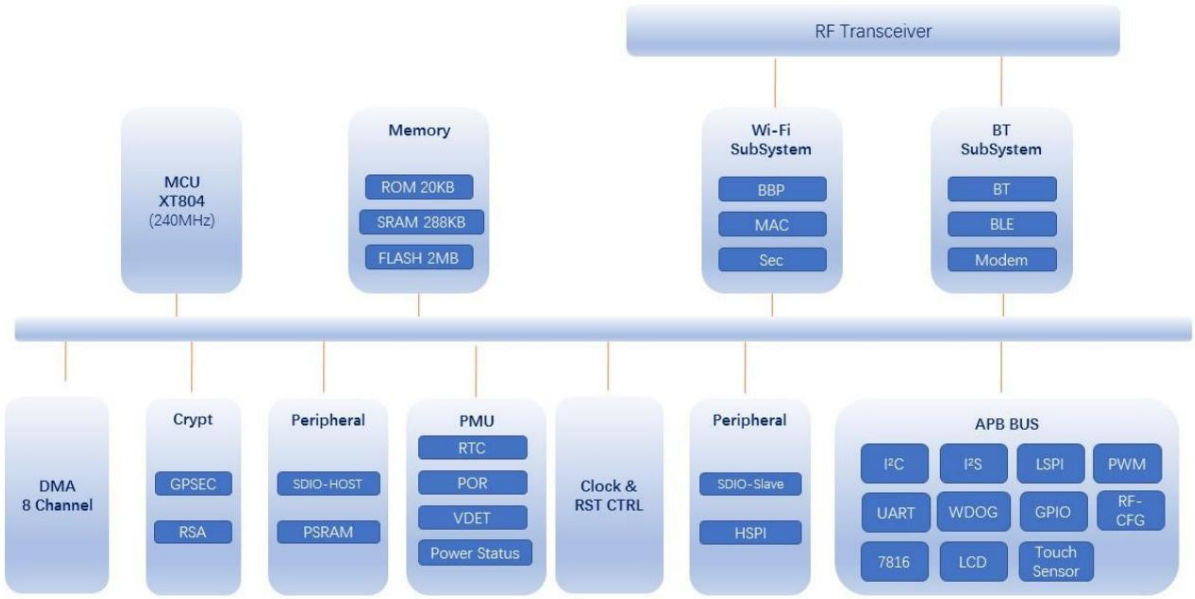

Figure 3-1 W801 chip structure

4 Address space division

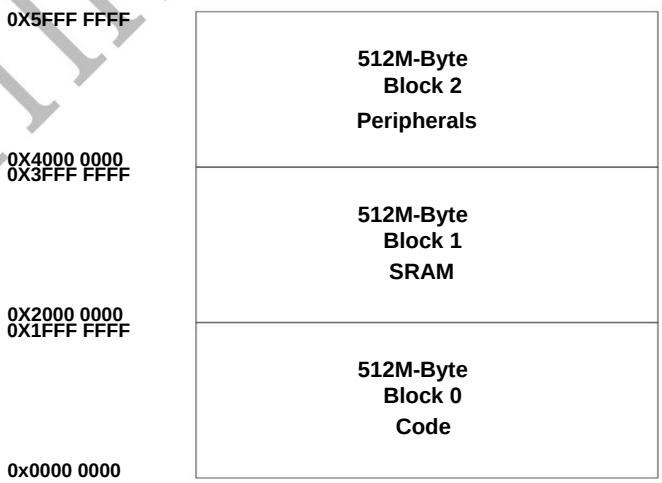

Figure 4-1 Address space mapping

Table 4-1 Detailed division of bus device address space

bus slave	BootMode=0	Address space breakdown	Remark
ROM	0x0000 0000 ~ 0x0004 FFFF		Store the solidified firmware code
FLASH	0x0800 0000 ~ 0x0FFF FFFF		as dedicated instruction memory.
SRAM	0x2000 0000 ~ 0x2002 7FFF		Firmware memory and instruction store
Mac RAM 0x2002 8000 ~ 0x2004 7FFF			SDIO/H-SPI/UART data buffer
PSRAM	0x3000 0000 ~ 0x30800000		Peripheral memory
CONFIG	0x4000 0000 ~ 0x4000 2FFF	0x4000 0000 ~ 0x4000 05FF RSA configuration space	
		0x4000 0600 ~ 0x4000 07FF GPSEC configuration space	
		0x4000 0800 ~ 0x4000 09FF DMA configuration space	
		0x4000 0A00 ~ 0x4000 0CFF SDIO_HOST configuration space	
		0x4000 0D00 ~ 0x4000 0DFF	PMU configuration space
		0x4000 0E00 ~ 0x4000 0EFF Clock and Reset configuration space	
		0x4000 0F00 ~ 0x4000 0FFF MacPHY Router configuration space	
		0x4000 1000 ~ 0x4000 13FF BBP configuration space	

		0x4000 1400 ~ 0x4000 17FF	MAC configuration space
		0x4000 1800 ~ 0x4000 1FFF	SEC configuration space
		0x4000 2000 ~ 0x4000 21FF	FLASH Controller configuration space
		0x4000 2200 ~ 0x4000 23FF	PSRAM_CTRL configuration space
		0x4000 2400 ~ 0x4000 25FF	SDIO Slave configuration space
		0x4000 2600 ~ 0x4000 27FF	H-SPI configuration space
		0x4000 2800 ~ 0x4000 29FF	SD Wrapper configuration space
		0x4000 2A00 ~ 0x4000 A9FF	BT Core configuration space
		0x4000 B000 ~ 0x4000 B0FF	SASC-B1 Level 1 bus memory security configuration module
		0x4000 B100 ~ 0x4000 B1FF	SASC-Flash Flash Security Configuration module
		0x4000 B200 ~ 0x4000 B2FF	SASC-B2 Level 2 bus memory security configuration module
APB	0x4001 0000 ~ 0x4001 C000	0x4001 0000 ~ 0x4001 01FF	I2C master
		0x4001 0200 ~ 0x4001 03FF	Sigma ADC
		0x4001 0400 ~ 0x4001 07FF	SPI master
		0x4001 0600 ~ 0x4001 07FF	UART0
		0x4001 0800 ~ 0x4001 09FF	UART1
		0x4001 0A00 ~ 0x4001 0BFF	UART2
		0x4001 0C00 ~ 0x4001 0DFF	UART3
		0x4001 0E00 ~ 0x4001 0FFF	UART4

		0x4001 1000 ~ 0x4001 11FF UART5	
		0x4001 1200 ~ 0x4001 13FF GPIO-A	
		0x4001 1400 ~ 0x4001 15FF GPIO-B	
		0x4001 1600 ~ 0x4001 17FF WatchDog	
		0x4001 1800 ~ 0x4001 19FF Timer	
		0x4001 1A00 ~ 0x4001 1BFF RF_Controller	
		0x4001 1C00 ~ 0x4001 1DFF LCD	
		0x4001 1E00 ~ 0x4001 1FFF PWM	
		0x4001 2000 ~ 0x4001 22FF I²S	
		0x4001 2200 ~ 0x4001 23FF BT-modem	
		0x4001 2400 ~ 0x4001 25FF Touch Sensor	
		0x4001 2600 ~ 0x4001 25FF TIPC Interface security settings	
		0x4001 4000 ~ 0x4000 BFFF RF_BIST DAC transmit memory	
		0x4001 C000 ~ 0x4003 BFFF RF_BIST ADC receive memory	
		0x4001 3C00 ~ 0x5FFF FFFF RSV	

5 Function description

5.1 SDIO HOST Controller

The SDIO HOST device controller provides a digital interface capable of accessing Secure Digital Input Output (SDIO) and MMC cards. were able

Access SDIO devices and SD card devices that are compatible with the SDIO 2.0 protocol. The main interfaces are CK, CMD and 4 data lines.

ÿ Compatible with SD Card Specification 1.0/1.1/2.0(SDHC)

ÿ Compatible with SDIO memory card specification 1.1.0

ÿ Compatible with MMC specification 2.0~4.2

ÿ Configurable interface clock rate, support host rate 0~50MHz

ÿ Support standard MMC interface

ÿ Support blocks up to 1024 bytes

ÿ Support soft reset function

ÿ Automatic Command/Response CRC generation/check

ÿ Automatic data CRC generation/check

ÿ Configurable timeout detection

ÿ Supports SPI, 1-bit SD and 4-bit SD modes

ÿ Support DMA data transfer

5.2 SDIO Device Controller

SDIO2.0 device interface to complete the interaction with the host data. Internally integrated 1024Byte asynchronous FIFO to complete the data between the host and the chip interact.

ÿ Compatible with SDIO Card Specification 2.0

ÿ Support host rate 0~50MHz

ÿ Support blocks up to 1024 bytes

ÿ Support soft reset function

ÿ Supports SPI, 1-bit SD and 4-bit SD modes

5.3 High Speed SPI Device Controller

Compatible with the general SPI physical layer protocol, through the agreed data format for interaction with the host, the host can access the device at high speed, and the maximum supported operating frequency is 50Mbps.

- ÿ Compatible with general SPI protocol
- ÿ Selectable level interrupt signal
- ÿ Support up to 50Mbps rate
- ÿ Simple frame format, full hardware parsing and DMA

5.4 DMA Controller

It supports up to 8 channels, 16 DMA request sources, and supports linked list structure and register control.

- ÿ Amba2.0 standard bus interface, 8 DMA channels
- ÿ Support DMA operation based on memory linked list structure
- ÿ Software configures 16 hardware request sources
- ÿ Support 1, 4-burst operation mode
- ÿ Support byte, half-word, word operations
- ÿ The source and destination addresses are unchanged or sequentially incremented, configurable or cyclic operation within a predefined address range
- ÿ Synchronous DMA request and DMA response hardware interface timing

5.5 Clock and Reset

Support the control of chip clock and reset system, clock control includes clock frequency conversion, clock shutdown and adaptive gating; reset control includes system and soft reset control of sub-modules.

5.6 Memory Manager

Supports the configuration of sending and receiving buffer size, as well as control information such as the base address of the MAC access buffer, the number of buffers, and the upper limit of frame aggregation.

5.7 Digital Baseband

Support IEEE802.11a/b/g/e/n (1T1R) transmitter and receiver algorithm implementation, main parameters:

- ÿ Data rate: 1~54Mpbs(802.11a/b/g), 6.5~150Mbps(802.11n)
- ÿ MCS format: MCS0~MCS7, MCS32 (40MHz HT Duplicate mode)
- ÿ Support 40MHz bandwidth non-HT Duplicate mode, 6Mÿ54M
- ÿ Signal bandwidth: 20MHz, 40MHz
- ÿ Modulation method: DSSS (DBPSK, DQPSK, CCK) and OFDM (BPSK, QPSK, 16QAM, 64QAM)
- ÿ Realize 1T1R MIMO-OFDM spatial multiplexing
- ÿ Support Short GI mode
- ÿ Support legacy mode and Mixed mode
- ÿ Support the transmission and reception of 20M upper and lower sideband signals under 40MHz bandwidth
- ÿ Support STBC reception of MCS0ÿ7,32
- ÿ Support Green Field mode

5.8 MAC Controller

Support the protocol control of the IEEE802.11a/b/g/e/n MAC sublayer, the specific specifications include:

- ÿ Support EDCA channel access mode
- ÿ Support CSMA/CA, NAV and TXOP protection mechanism
- ÿ Beacon, Mng, VO, VI, BE, BK five-way send queue and QoS
- ÿ Support single and wide group wave frame receiving and sending
- ÿ Support RTS/CTS, CTS2SELF, Normal ACK, No ACK frame sequence
- ÿ Support retransmission mechanism and retransmission rate and power control
- ÿ Support MPDU hardware aggregation and de-aggregation and Immediate BlockAck mode

ÿ Support RIFS, SIFS, AIFS

ÿ Support reverse transfer mechanism

ÿ Supports TSF timing and is software configurable

ÿ Support MIB statistics

5.9 Safety system

Support the security algorithm specified by the IEEE802.11a/b/g/e/n protocol, and cooperate to complete the encryption and decryption of the transmitted and received data frames.

ÿ Satisfy the encryption and decryption throughput rate greater than 150Mbps

ÿ Amba2.0 standard bus interface

ÿ Support WAPI security mode 2.0

ÿ Support WEP security mode - 64-bit encryption

ÿ Support WEP security mode - 128-bit encryption

ÿ Support TKIP security mode

ÿ Support CCMP safe mode

5.10 FLASH Controller

ÿ Provide bus access FLASH interface

ÿ Provide system bus and data bus access arbitration

ÿ Implement CACHE cache system to improve FLASH interface access speed

ÿ Provide compatibility with different QFlash

5.11 RSA encryption module

RSA operation hardware coprocessor, providing Montgomery (FIOS algorithm) modular multiplication function. Cooperate with RSA software library to realize RSA algorithm.

128-bit to 2048-bit modulo multiplication is supported.

5.12 General hardware encryption module

The encryption module automatically completes the encryption of the source address space data of the specified length, and automatically writes the encrypted data back to the specified destination address space after completion;

Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG.

- ÿ Support SHA1/MD5/RC4/DES/3DES/AES/CRC/TRNG encryption algorithm
- ÿ DES/3DES supports ECB and CBC modes
- ÿ AES supports ECB, CBC and CTR modes
- ÿ CRC supports four modes: CRC8, CRC16_MODBUS, CRC16_CCITT and CRC32
- ÿ CRC supports input/output reverse
- ÿ SHA1/MD5/CRC supports continuous multi-packet encryption
- ÿ Built-in true random number generator, also supports seed to generate pseudo-random numbers

5.13 I2C Controller

APB bus protocol standard interface, only supports master device controller, I²C operating frequency support can be configured, 100K-400K.

5.14 Master/Slave SPI Controller

Supports synchronous SPI master-slave function. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

- ÿ Transmit and receive paths each have 8-word deep FIFOs
- ÿ The master supports 4 formats of Motorola SPI (CPOL, CPHA), TI timing, macrowire time
- ÿ slave supports 4 formats of Motorola SPI (CPOL, CPHA);
- ÿ Supports full duplex and half duplex
- ÿ The main device supports bit transmission, the maximum supports 65535bit transmission
- ÿ The slave device supports transmission modes of various length bytes
- ÿ The maximum clock frequency of SPI_Clk input from the slave device is 1/6 of the system clock

5.15 UART Controller

ÿ The device side complies with the APB bus interface protocol

ÿ Support interrupt or polling working mode

ÿ Support DMA transfer mode, there are 32-byte FIFOs for sending and receiving

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity can be configured

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt indication

ÿ Maximum 16-burst byte DMA operation

5.16 GPIO Controller

Configurable GPIO, software-controlled input and output, hardware-controlled input and output, and configurable interrupt mode.

The GPIOA and GPIOB registers have different starting addresses, but the functions are the same.

5.17 Timer

Microsecond and millisecond timing (the number of counts is configured according to the clock frequency), and six configurable 32-bit counters are implemented.

When successful, a corresponding interrupt is generated.

5.18 Watchdog Controller

Support "Watchdog" function. Observe the correctness of software behavior and allow global reset after system crash. "Watchdog" generates a periodic

The system software must respond to this interrupt and clear the interrupt flag; if the interrupt flag has not been cleared for a long time due to a system crash, the

Generate a hard reset to perform a global reset of the system.

5.19 RF Configurator

A synchronized SPI master function is implemented. Its working clock is the internal bus clock of the system. Its characteristics are as follows:

ÿ Transmit and receive paths each have 1 word deep FIFO

5.20 RF Transceivers

ÿ The RF transceiver part includes modules including power amplifier, transmit path, receive path, phase-locked loop and SPI. By adjusting the control
control port SHDN, RXEN and TXEN to change the working state of the chip

ÿ The receiving channel adopts a zero-IF structure, which directly converts the RF signal into baseband I and Q outputs. The RF front end works at 2.4GHz,
Contains low noise amplifier and quadrature mixer; baseband consists of low pass filter and variable gain amplifier to realize channel filtering and gain control;
Driver amplifiers provide different DC outputs for ADC interface

ÿ The transmit path includes: programmable control filters, up-conversion mixers, variable gain amplifiers and power amplifiers. The transmit path also uses direct
Frequency conversion structure. The output signal of the DAC is passed through a low-pass filter to filter out the image frequency and out-of-band noise. PA outputs are differential output drivers
off-chip antenna

5.21 PWM Controller

ÿ 5-channel PWM signal generation function

ÿ 2-channel input signal capture function (two channels of PWM0 and PWM4)

ÿ Frequency range: 3Hz~160KHz

ÿ The maximum precision of the duty cycle: 1/256, the width of the counter inserted in the dead zone: 8bit

5.22 I²S Controller

ÿ Support AMBA APB bus interface, 32bit single read and write operations

ÿ Support master, slave mode, can work in duplex

ÿ Support 8/16/24/32 bit width, the highest sampling frequency is 128KHz

ÿ Support mono and stereo mode

ÿ Compatible with I²S and MSB justified data format, compatible with PCM A/B format

ÿ Support DMA request for read and write operations. Only supports word-by-word operations

5.23 7816/UART Controller

ÿ The device side complies with the APB bus interface protocol

ÿ Support interrupt or polling working mode

ÿ Support DMA transfer mode, there are 32-byte FIFOs for sending and receiving

ÿ DMA can only operate by byte, the maximum 16-burst byte DMA operation

Compatible with UART and 7816 interface functions:

Serial port function:

ÿ Programmable baud rate

ÿ 5-8bit data length, and parity polarity can be configured

ÿ 1 or 2 stop bits configurable

ÿ Support RTS/CTS flow control

ÿ Support Break frame sending and receiving

ÿ Overrun, parity error, frame error, rx break frame interrupt indication

7816 interface function:

ÿ Compatible with ISO-7816-3 T=0.T=1 mode

ÿ Compatible with EVM2000 protocol

ÿ Configurable guard time (11 ETU-267 ETU)

ÿ Forward/reverse convention is software configurable

ÿ Support send/receive parity check and retransmission function

ÿ Support 0.5 and 1.5 stop bit configuration

5.24 PSRAM Interface Controller

W800 has a built-in PSRAM controller with SPI/QSPI interface, supports external PSRAM device access, and provides bus-based PSRAM read, write, and erase operate. The maximum read and write speed is 80MHz.

ÿ Support read and write access to external PSRAM

ÿ Configurable as SPI and QSPI

ÿ SPI/QSPI clock frequency can be configured

ÿ Support BURST INC mode access

ÿ Support half sleep mode of PSRAM

5.25 ADC

The acquisition module based on Sigma-Delta ADC completes the acquisition of up to 4 channels of analog signals. The sampling rate is controlled by the external input clock. It can collect input voltage and also collect chip temperature, and support input calibration and temperature compensation calibration.

5.26 Touch key controller

The basic functions of the module are as follows:

ÿ Supports up to 15 Touch Sensor scans

ÿ Record the scanning result of each Touch Sensor

ÿ Report scan results by interrupt

6 Pin Definition

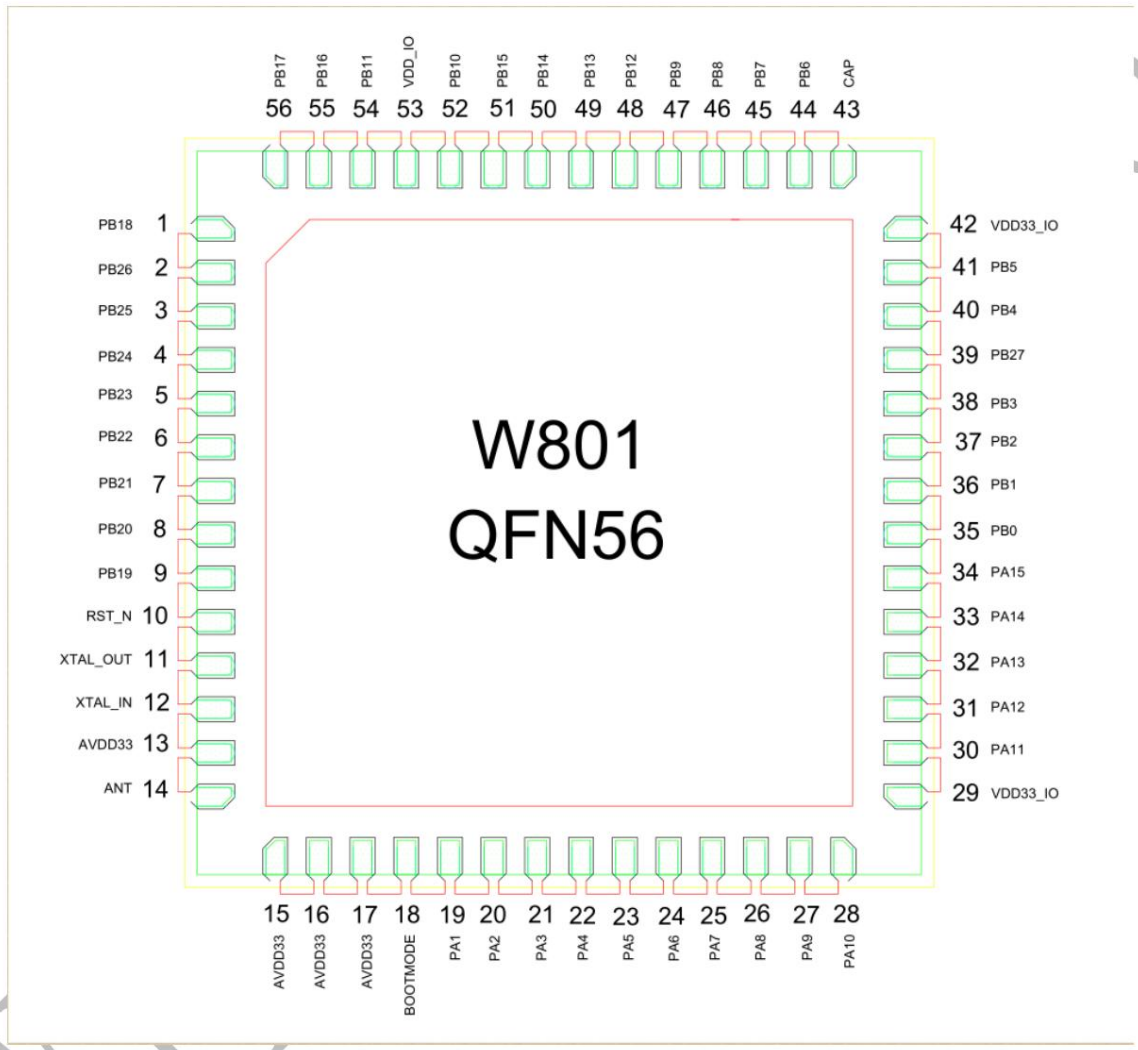

Figure 6-1 W801 pin layout (QFN56)

Table 6-1 W801 pin assignment definition (QFN56)

Number	Name	Type	Pin Function After Reset	Multiplexing function	Maximum frequency	pull-up and pull-down capability	drive capability
1	PB_18	I/O	GPIO, input, high impedance	UART5_TX/LCD_SEG30	10MHz	UP/DOWN	12mA
2	PB_26	I/O	GPIO, input, high impedance	LSPI_MOSI/PWM4/LCD_SEG1	20MHz	UP/DOWN	12mA
3	PB_25	I/O	GPIO, input, high impedance	LSPI_MISO/PWM3/LCD_COM0	20MHz	UP/DOWN	12mA
4	PB_24	I/O	GPIO, input, high impedance	LSPI_CK/PWM2/LCD_SEG2	20MHz	UP/DOWN	12mA
5	PB_23	I/O	GPIO, input, high impedance	LSPI_CS/PCM_DATA/LCD_SEG0	20MHz	UP/DOWN	12mA
6	PB_22	I/O	GPIO, input, high impedance	UART0_CTS/PCM_CK/LCD_COM2	10MHz	UP/DOWN	12mA
7	PB_21	I/O	GPIO, input, high impedance	UART0_RTS/PCM_SYNC/LCD_COM1	10MHz	UP/DOWN	12mA
8	PB_20	I/O	UART_RX	UART0_RX/PWM1/UART1_CTS/I2C_SCL	10MHz	UP/DOWN	12mA
9	PB_19	I/O	UART_TX	UART0_TX/PWM0/UART1_RTS/I2C_SDA	10MHz	UP/DOWN	12mA
10	RESET	I	RESET reset			UP	
11	XTAL_OUT	O	External crystal oscillator output				
12	XTAL_IN	I	External crystal input				
13	AVDD33	P	chip power supply, 3.3V				
4	ANT	I/O	RF Antenna				
15	AVDD33	P	chip power supply, 3.3V				
16	AVDD33	P	chip power supply, 3.3V				
17	AVDD33_AUX	P	chip power supply, 3.3V				
18	BOOTMODE	I/O	BOOTMODE	I2S_MCLK/LSPI_CS/PWM2/I2S_DO	20MHz	UP/DOWN	12mA
19	PA_1	I/O	JTAG_CK	JTAG_CK/I2C_SCL/PWM3/I2S_LRCK/ADC_1	20MHz	UP/DOWN	12mA
20	PA_2	I/O	GPIO, input, high impedance	UART1_RTS/UART2_TX/PWM0/UART3_RTS/ADC_4	20MHz	UP/DOWN	12mA
twenty one	PA_3	I/O	GPIO, input, high impedance	UART1_CTS/UART2_RX/PWM1/UART3_CTS/ADC_3	20MHz	UP/DOWN	12mA
twenty two	PA_4	I/O	JTAG_SWO	JTAG_SWO/I2C_SDA/PWM4/I2S_BCK/ADC_2	20MHz	UP/DOWN	12mA
twenty three	PA_5	I/O	GPIO, input, high impedance	UART3_TX/UART2_RTS/PWM_BREAK/UART4_RTS/VRP_EXT	20MHz	UP/DOWN	12mA
twenty four	PA_6	I/O	GPIO, input, high impedance	UART3_RX/UART2_CTS/NULL/UART4_CTS/LCD_SEG31/VRP_EXT	20MHz	UP/DOWN	12mA
25	PA_7	I/O	GPIO, input, high impedance	PWM4/LSPI_MOSI/I2S_MCK/I2S_DI/LCD_SEG3/Touch_1	20MHz	UP/DOWN	12mA
26	PA_8	I/O	GPIO, input, high impedance	PWM_BREAK/UART4_TX/UART5_TX/I2S_BCLK/LCD_SEG4	20MHz	UP/DOWN	12mA

27	PA_9	I/O GPIO, input, high impedance	MMC_CLK/UART4_RX/UART5_RX/I2S_LR CLK/LCD_SEG5/TOUCH_2	50MHz	UP/DOWN	12mA
28	PA_10	I/O GPIO, input, high impedance	MMC_CMD/UART4_RTS/PWM0/I2S_DO/LC D_SEG6/TOUCH_3	50MHz	UP/DOWN	12mA
29	VDD33IO	P IO power supply, 3.3V				
30	PA_11	I/O GPIO, input, high impedance	MMC_DAT0/UART4_CTS/PWM1/I2S_DI/L CD_SEG7	50MHz	UP/DOWN	12mA
31	PA_12	I/O GPIO, input, high impedance	MMC_DAT1/UART5_TX/PWM2/LCD_SEG8/ TOUCH_14	50MHz	UP/DOWN	12mA
32	PA_13	I/O GPIO, input, high impedance	MMC_DAT2/UART5_RX/PWM3/LCD_SEG9	50MHz	UP/DOWN	12mA
33	PA_14	I/O GPIO, input, high impedance	MMC_DAT3/UART5_CTS/PWM4/LCD_SEG1 0/TOUCH_15	50MHz	UP/DOWN	12mA
34	PA_15	I/O GPIO, input, high impedance	PSRAM_CK/UART5_RTS/PWM_BREAK/LCD _SEG11	50MHz	UP/DOWN	12mA
35	PB_0	I/O GPIO, input, high impedance	PWM0/LSPI_MISO/UART3_TX/PSRAM_CK /LCD_SEG12/Touch_4	80MHz	UP/DOWN	12mA
36	PB_1	I/O GPIO, input, high impedance	PWM1/LSPI_CK/UART3_RX/PSRAM_CS/L CD_SEG13/Touch_5	80MHz	UP/DOWN	12mA
37	PB_2	I/O GPIO, input, high impedance	PWM2/LSPI_CK/UART2_TX/PSRAM_D0/L CD_SEG14/Touch_6	80MHz	UP/DOWN	12mA
38	PB_3	I/O GPIO, input, high impedance	PWM3/LSPI_MISO/UART2_RX/PSRAM_D1 /LCD_SEG15/Touch_7	80MHz	UP/DOWN	12mA
39	PB_27	I/O GPIO, input, high impedance	PSRAM_CS/UART0_TX/LCD_COM3	80MHz	UP/DOWN	12mA
40	PB_4	I/O GPIO, input, high impedance	LSPI_CS/UART2_RTS/UART4_TX/PSRAM _D2/LCD_SEG16/Touch_8	80MHz	UP/DOWN	12mA
41	PB_5	I/O GPIO, input, high impedance	LSPI_MOSI/UART2_CTS/UART4_RX/PSA RM_D3/LCD_SEG17/Touch_9	80MHz	UP/DOWN	12mA
42	VDD33IO	P IO power supply, 3.3V				
43	CAP	I External capacitor, 1μF			-	
44	PB_6	I/O GPIO, input, high impedance	UART1_TX/MMC_CLK/HSPI_CK/SDIO_CK /LCD_SEG18/Touch_10	50MHz	UP/DOWN	12mA
45	PB_7	I/O GPIO, input, high impedance	UART1_RX/MMC_CMD/HSPI_INT/SDIO_C MD/LCD_SEG19/Touch_11	50MHz	UP/DOWN	12mA
46	PB_8	I/O GPIO, input, high impedance	I2S_BCK/MMC_D0/PWM_BREAK/SDIO_D0 /LCD_SEG20/Touch_12	50MHz	UP/DOWN	12mA
47	PB_9	I/O GPIO, input, high impedance	I2S_LRCK/MMC_D1/HSPI_CS/SDIO_D1/ LCD_SEG21/Touch_13	50MHz	UP/DOWN	12mA
48	PB_12	I/O GPIO, input, high impedance	HSPI_CK/PWM0/UART5_CTS/I2S_BCLK/ LCD_SEG24	50MHz	UP/DOWN	12mA
49	PB_13	I/O GPIO, input, high impedance	HSPI_INT/PWM1/UART5_RTS/I2S_LRCL K/LCD_SEG25	50MHz	UP/DOWN	12mA

50	PB_14	I/O	GPIO, input, high impedance	HSPI_CS/PWM2/LSPI_CS/I2S_DO/LCD_SEG26	50MHz	UP/DOWN	12mA
51	PB_15	I/O	GPIO, input, high impedance	HSPI_DI/PWM3/LSPI_CK/I2S_DI/LCD_SEG27	50MHz	UP/DOWN	12mA
52	PB_10	I/O	GPIO, input, high impedance	I2S_DI/MMC_D2/HSPI_DI/SDIO_D2/LCD_SEG22	50MHz	UP/DOWN	12mA
53	VDD33IO	P	IO power supply, 3.3V				
54	PB_11	I/O	GPIO, input, high impedance	I2S_DO/MMC_D3/HSPI_DO/SDIO_D3/LCD_SEG23	50MHz	UP/DOWN	12mA
55	PB_16	I/O	GPIO, input, high impedance	HSPI_DO/PWM4/LSPI_MISO/UART1_RX/LCD_SEG28	50MHz	UP/DOWN	12mA
56	PB_17	I/O	GPIO, input, high impedance	UART5_RX/PWM_BREAK/LSPI_MOSI/I2S_MCLK/LCD_SEG29	20MHz	UP/DOWN	12mA

Notes: 1. I = Input, O = Output, P = Power

7 Electrical Characteristics

7.1 Limit parameters

Table 7-1 Limit parameters

parameter	name	minimum	Typical value	maximum value	unit
Supply voltage	VDD	3.0	3.3	3.6	V
Input logic level low	VIL	-0.3		0.8	V
Input logic level high	VIH	2.0		VDD+0.3	V
Input pin capacitance	Cpad			2	pF
output logic level low	VOL			0.4	V
output logic level high	VOH	2.4			V
Output maximum drive capability	IMAX			twenty four	mA
Storage temperature range	TSTR	-40ÿ		+125ÿ	°C
range of working temperature	TOPR	-40ÿ		+85ÿ	°C

7.2 RF Power Consumption Parameters

Test conditions: 3.3V power supply, the emission is tested according to the 50% duty cycle.

Table 7-2 RF power consumption parameters

model	Typical value	unit
Transmit IEEE802.11b 1Mbps POUT = +19.4dBm	240	mA
Transmit IEEE802.11b 11Mbps	240	

POUT = +19.3dBm		
Transmit IEEE802.11g 54Mbps POUT = +14.7dBm	190	mA
Send IEEE802.11n MCS7 POUT = +12dBm	180	mA
Receive IEEE802.11b/g/n	95	mA

7.3 Wi-Fi Radio

Table 7-3 Wi-Fi RF parameters

parameter	Typical value	unit
input frequency	2.4~2.4835	GHz
transmit power		
IEEE802.11b 11Mbps	19±2	dBm
IEEE802.11g 54Mbps	16±2	dBm
IEEE802.11n MCS7 HT20	13±2	dBm
Receive sensitivity		
IEEE802.11b 1Mbps	-96	dBm
IEEE802.11b 11Mbps	-86	dBm
IEEE802.11g 54Mbps	-73	dBm
IEEE802.11g MCS7 HT20	-71	dBm

Adjacent channel suppression		
IEEE802.11b 6Mbps	32	dB
IEEE802.11g 54Mbps	16	dB
IEEE802.11n HT20, MCS0	31	dB
IEEE802.11n HT20, MCS7	12	dB

7.4 Bluetooth RF

7.4.1 Traditional Bluetooth RF

Receiver - Base Rate (BR)

parameter	condition	Min	Typ	Max	Units
Sensitivity@0.1% BER			-91		dBm
Maximum received signal@0.1% BER			0		dBm
Co-channel rejection ratio C/I			9		dB
out-of-band blocking	30MHz ~ 2000MHz		-10		dBm
	2000 MHz ~ 2400 MHz		-27		dBm
	2500 MHz ~ 3000 MHz		-27		dBm
	3000 MHz ~ 12.5 GHz		-10		dBm
intermodulation			-39		dB

Emitter - Base Rate (BR)

parameter	condition	Min Typ Max Units			
RF transmit power			6		dBm
Gain control step size			3		db
RF power control range		-10		12	dBm
20 dB bandwidth		0.918 0.923			
ÿ f1avg			159.8		
ÿ f2max			142.8		
ÿf2avg/ÿf1avg			0.89		
ICFT			0		
Drift rate		-2.25 -2.08 2.23			kHz
Offset (DH1)		-4		-1	kHz
Offset (DH5)			0	twenty one	kHz

Receiver - Enhanced Rate (EDR)

parameter	condition	Min Typ Max Units			
ÿ/4 DQPSK					
Sensitivity@0.01% BER			-88		dBm
Maximum received signal@0.01% BER			0		dBm

8DPSK					
Sensitivity@0.01% BER			-81		dBm
Maximum received signal@0.01% BER			0		dBm

Transmitter - Enhanced Data Rate (EDR)

parameter	condition	Min Typ Max Units			
RF transmit power			0		dBm
Gain control step size			3		db
RF power control range		-10		8	dBm
ÿ/4 DQPSK max w0		-3.2		2.6	KHz
ÿ/4 DQPSK max wi		-5.3		-2.4 KHz	
ÿ/4 DQPSK max |wi + w0|		-4.8		-3.9 KHz	
8DPSK max w0		-1.4		1.5	KHz
8DPSK max wi		-4.1		-2.9 KHz	
8DPSK max |wi + w0|		-4.8		-4.1	KHz
ÿ/4 DQPSK modulation accuracy	RMS DEVM		6.7		%
	99% DEVM		100		%
	Peak DEVM		14.1		%
8 DPSK modulation accuracy	RMS DEVM		6.8		%

	99% DEVM		99.99		%
	Peak DEVM		15.3		%
EDR Differential Phase Encoding			100		%

7.4.2 Bluetooth Low Energy RF

receiver

parameter	condition	Min	Typ	Max	Units
Sensitivity@30.8% PER			-94		dBm
Maximum received signal@30.8% PER				0	dBm
out-of-band blocking	30MHz~2000MHz		-30		dBm
	2003MHz~2399MHz		-35		dBm
	2484MHz~3000MHz		-35		dBm
	3000MHz~12.5GHz		-30		dBm
intermodulation			-47		dBm

launcher

parameter	condition	Min	Typ	Max	Units
RF transmit power			6		dBm
Gain control step size			2		db
RF power control range		-10		12	dBm

ÿ f1avg		240.8	241.2 242		kHz
ÿ f2max		175.7	182.7 183.9 kHz		
Drift rate			1.5		kHz
offset			-4.3		kHz

8 Package Information

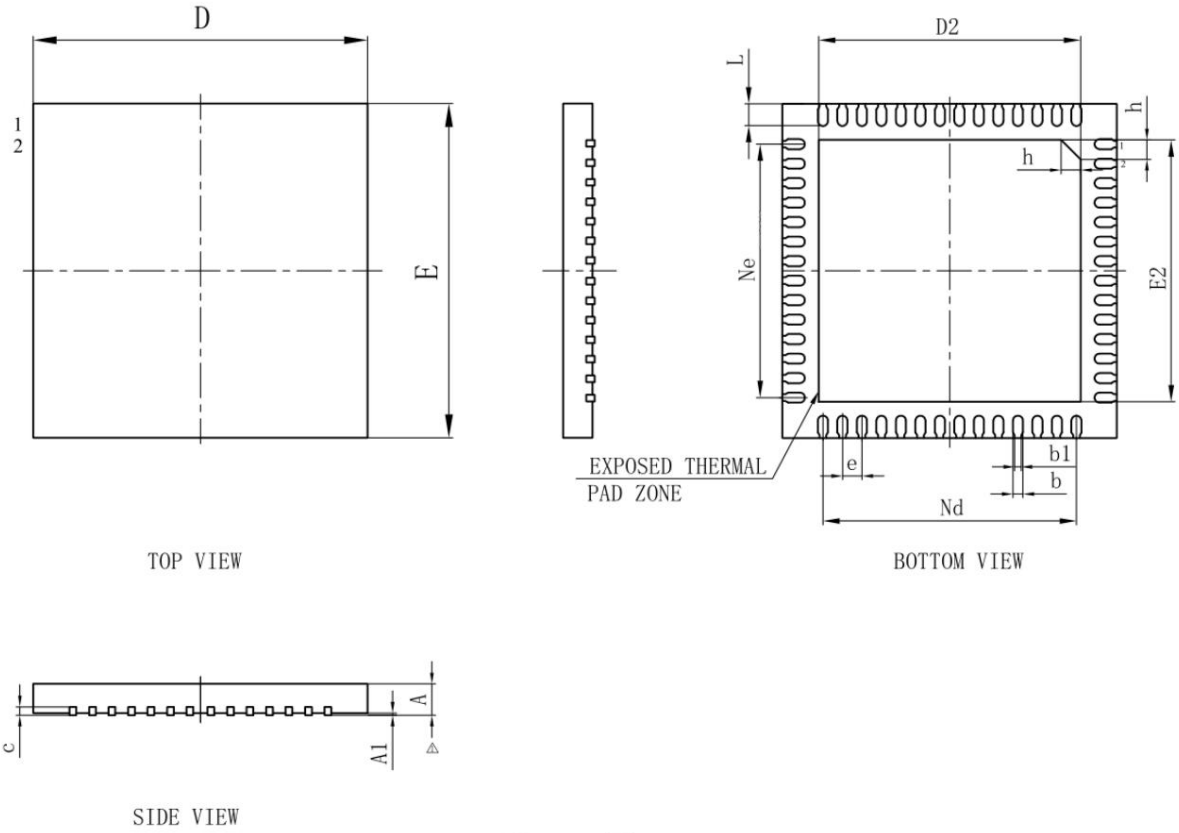

Figure 8-1 W801 Package Parameters

Table 8-1 W800 Package Parameters

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		

c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.60	4.70	4.80
e	0.35BSC		
Ne	4.55BSC		
Nd	4.55BSC		
E	5.90	6.00	6.10
E2	4.60	4.70	4.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F carrier size	193x193		