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LED Pulser FPGA Register Map (word addresses)

0x00: Control and status register

Bit 0: Enable Test Pulser. 1: Enabled, 0: Disabled.

Bit 1: Test Pulser Single Step/ Free Run 1: One Spill. 0: Free Run

15:2	1	0
Not Used	Single Step/Free Run	Test Pulser Enable

0x01: Read/Write word 0 of test pulser RAM

A Write to this address define bits 27..12 of the time at which an LED flasher pulse is issued.

0x02: Read/Write word 1 of test pulser RAM

A write to this address defines bits 11..0 of the time at which an LED flasher pulse is issued and bits 35..32 of the LED output map.

0x03: Read/Write word 2 of test pulser RAM

A write to this address defines bits 31..16 of the LED output map..

0x04: Read/Write word 3 of test pulser RAM

A write to this address defines bits 15..0 of the LED output map..

0x05: Read/Write test pulser RAM address

A write to this address defines the test pulse ram address. Data bits 7..0 are significant. A 28 bit, 100MHz time counter is compared to bits 63..36 of the RAM entry. When there is a match, a pulse to those outputs specified by test pulser RAM bits 35..0 is issued and the RAM pointer is incremented. A time value of 0 is used as end list. If the run mode is single step, the pulse sequence stops. If the mode is free run, the address pointer is reset to 0 and the sequence is repeated.

0x06: Read/Write gate delay address

A write to this address defines the eight bit delay in steps of 10ns between the time of a trigger and the sending of a gate on the GPO 1 (P6) LEMO.

0x07: Read/Write trigger delay address

A write to this address defines the eight bit delay in steps of 10ns between the time of an input trigger and the sending of a pulse to the LED array.

0x08: Not Used

0x09: LED Trigger pulse width

A write to this address defines the four bit width in steps of 10ns of the trigger pulse sent to the LED driver board. A width of 2 seems to be appropriate.

0x0A: Read/Write gate width address

A write to this address defines the eight bit width in steps of 10ns of the gate pulse on GPO 1.

0x0C: Uptime Counter bits 31...16

0x0D: Uptime Counter bits 15...0

A counter showing the number of seconds since the last FPGA reset

0x0E: Read/Write test Counter Bits 31...16

A write to this address defines the upper 16 bits of the 32 bit test counter. A read returns the present value of the upper bits.

0x0F: Read/Write test Counter Bits 15...0

A write to this address defines the lower 16 bits of the 32 bit test counter. A read from this address displays the value of the lower order bits and increments all 32 bits of the counter after the read.

0x10..0x33: Read/Write LED pulse magnitude DACs.

A write to these addresses define the 12 bit LED flasher DAC magnitudes with a span of 0..14V.