Available online at www.sciencedirect.com

ScienceDirect

Current Opinion in Neurobiology

Neuromorphic sensory systems

Shih-Chii Liu and Tobi Delbruck

Biology provides examples of efficient machines which greatly outperform conventional technology. Designers in neuromorphic engineering aim to construct electronic systems with the same efficient style of computation. This task requires a melding of novel engineering principles with knowledge gleaned from neuroscience. We discuss recent progress in realizing neuromorphic sensory systems which mimic the biological retina and cochlea, and subsequent sensor processing. The main trends are the increasing number of sensors and sensory systems that communicate through asynchronous digital signals analogous to neural spikes; the improved performance and usability of these sensors; and novel sensory processing methods which capitalize on the timing of spikes from these sensors. Experiments using these sensors can impact how we think the brain processes sensory information.

Address
Institute of Neuroinformatics, University of Zurich and ETH Zurich, Winterthurerstrasse 190, CH-8057, Zurich, Switzerland

Corresponding author: Liu, Shih-Chii (shih@ini.phys.ethz.ch) and Delbruck, Tobi (tobi@ini.phys.ethz.ch)

Current Opinion in Neurobiology 2010, **20**:288–295

This review comes from a themed issue on
Sensory systems
Edited by Kevan Martin and Kristin Scott

Available online 20th May 2010

0959-4388/$ – see front matter

DOI 10.1016/j.conb.2010.03.007

Introduction

Nature offers many examples of compact, energy-efficient, adaptable, and intelligent systems. Even a simple animal like the bee displays exquisite flight motor skills and cognitive behaviors, with a body weight of less than a gram and a brain that dissipates only on the order of 10 μW. Yet we are not able to construct an artificial system that displays even a subset of this creature's abilities using the latest technology; see for example, the performance of the state-of-art robotic vehicles in the recent DARPA Desert and Urban Challenges which relied heavily on absolute positioning via GPS and carried roughly 1 kW of computing power [1•].

To identify the factors contributing to nature's computational efficiency in dealing with its uncontrolled environment, many researchers rely on simulations of brain networks using supercomputers [2•] which are constructed from fast, high-precision digital hardware with high power dissipation. However, brains are composed of slow asynchronous neural components which use a combination of both analog and digital signal representations. Although computers are valuable for detailed simulation of biophysics, they are not physical emulations of biological neural computation.

A small number of labs in the field of *neuromorphic engineering* are actively pursuing a different approach towards understanding the architecture of brains. By emulating the neuronal organization and function of nervous systems in electronic devices, neuromorphic engineers hope to harness the brain's efficient and powerful style of physical computation for future artificial systems [3–5]. The fruits of this effort are illustrated in neuromorphic microchips that emulate biological sensing and spike-based neuronal processing.

Neuromorphic sensors and sensory systems have made the greatest strides in recent years with many designs using a new form of asynchronous output representation which carries timing information similar to spikes in the nervous systems. This representation has led to novel systems where computing occurs in an event-driven manner similar to that of nervous systems [6].

Artificial technology: similarities between biology and silicon

Neuromorphic electronic devices are constructed primarily on silicon, the same technology used for fabricating the majority of analog and digital computing chips. The primary silicon primitive is the transistor where current flows through this device as a function of the voltage at its four terminals. It shares much of the same physics of neurons thus making it an ideal device for emulating the circuitry of nervous systems [4,7]. In the ''subthreshold'' region of operation, the transistor current is exponentially dependent on its terminal voltages analogous to the exponential dependence of active populations of voltage-sensitive ionic channels as a function of the potential across the membrane of a neuron. This similarity allows us to construct using a small number of transistors, compact circuits that implement electronic models of voltage-controlled conductance-based neurons and conductance-based synapses [8,9] and useful computational biological primitives such as phototransduction, logarithmic functions, amplification, multiplication, inhibition, correlation, thresholding, and winner-take-all selection [7].

Communicating spikes by using the address-event representation

Building large arrays of interconnected neurons on a silicon chip can pose a challenge. Unlike the 3D world of neurons, transistors are permanently patterned on a 2D substrate with only a few layers of wiring. Point-to-point dedicated wiring is expensive and is restricted to local neighborhoods. Wiring and transistor circuits on a chip are also fixed after chip fabrication, restricting the range of possible neuronal architectures that can be expressed on one chip. However, the mobility of current flow (electrons) in a transistor is 10^7 times higher than the mobility of ions in biology. This huge difference in speed is used to make up for the fixed circuitry, as we will now discuss.

We use the higher speed of electronics to our advantage by devising a different signal transmission scheme than that of real neurons. Connections in real neurons are built by synapses which connect an axon to a dendrite. In electronics, we simply confer an address to every neuron and synapse on-chip. We transmit spikes off-chip as a *spike address* that carries the ''what'' (which neuron) and ''when'' (when it spiked) information. These addresses are transmitted within a few nanoseconds to another external device. For example, one 16-bit address bus can carry spikes from up to $2^{16} = 65,536$ neurons. Since the on-chip neurons are designed to have low firing rates of about 100 Hz or less, multiple spike addresses can be transmitted off-chip on the shared address bus before a neuron makes the next spike. The availability of ''what'' and ''when'' information allows great flexibility for subsequent processing. For example, digital memory chips can store a routing table which describes how a spike address is routed to other neurons through their pre-specified spike addresses, thus emulating a soft configurable connectivity scheme for multiple neuron on-chip. This scheme is called the *address-event representation* (AER) and is the de facto signal transmission scheme used in most recent neuromorphic sensors and multi-chip systems [10•].

Event-driven computing with spike-timing

What are the advantages of using AER? Conventional sensors and AER systems differ in who is the master of the communication. In conventional sensors, an external process regularly polls the sensor array at sufficiently high rate to capture all frequencies of interest. AER sensors, like their biological counterparts, make the sensor the master: Each retina pixel or cochlea channel autonomously decides when it should transmit events that carry useful information about the world. This form of event coding has two advantages: first, these sensors transmit only informative non-redundant events, thus reducing power dissipation both for communication and for subsequent processing. Second, because the pixels initiate their own communication, output events are transmitted with very short latencies. These spikes initiate computation in the post-processing network, which we call *event-driven computation*. A recipient network can, for example, use the timing information of the events to configure the connections between neurons [3,11•], to initiate synaptic plasticity in a network [12,13]; or to drive the motor output of a visual-motor system with low-latency [14••,15].

Emulation of biological sensing

Neuromorphic engineers have focused significant effort on mimicking the retina and cochlea. The primary reasons for this focus are that these sensors have immediate applications in artificial vision and audition, and they allow the exploration of neural-like architectures for sensory processing in the brain.

Silicon retinas

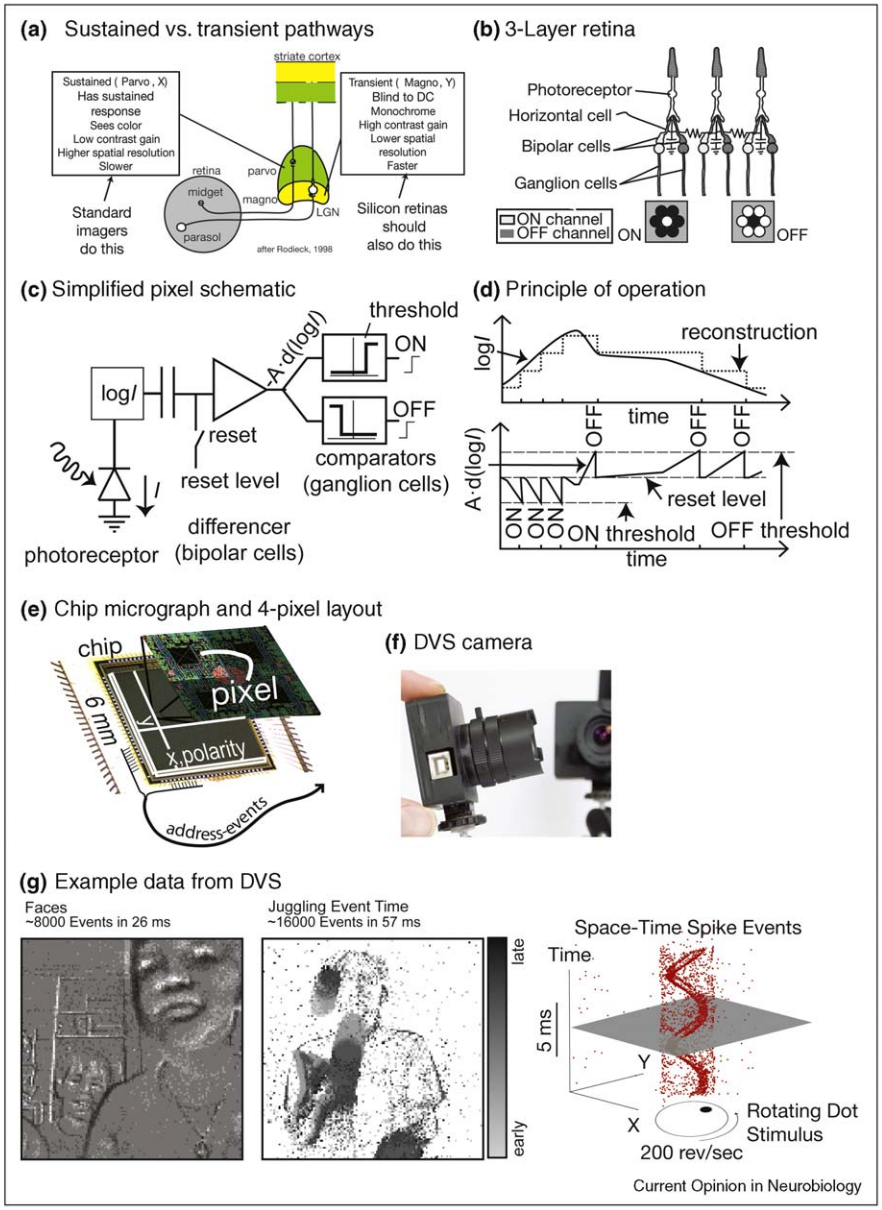
Conventional imagers like our digital cameras create sequences of highly redundant pictures. However, retinas serve a different function; they asynchronously transmit relevant information about the world, thus reducing redundancy and increasing efficiency in power dissipation and information transfer [16]. Neuromorphic designers have made significant strides in copying the functionality of the retina based on the wealth of knowledge from neuroscientists [17]. The earliest silicon retina by Mahowald and Mead [18] illustrated the functionality of major retinal cells and demonstrated useful properties of biological retinas, for example, the local gain control of photoreceptors over many decades of background intensity, and the reduction of redundant spatial and temporal information. The majority of recent silicon retina designs transmit their outputs as AER spikes. Improvement in the silicon analog circuit design techniques has led to recent useable designs with varieties of cell types and functionality [19,20•,21–25,26•] (see Figure 1).

Unlike conventional imagers that generate frame-sampled intensity values, silicon retinas emulate the local processing, local gain control, and asynchronous spike transmission properties of biological retinas. From an engineering perspective, silicon retinas offer advantages of increased dynamic range in illumination ($>10^5$) and higher effective sampling rates (several kHz) over conventional cameras, which have typical dynamic range of a factor of 300 in illumination and sampling rates of under 60 Hz. The cost of processing the sparse output of silicon retinas can be reduced by a factor of 100 compared to the cost of processing the outputs of conventional cameras [26•].

Silicon cochleas

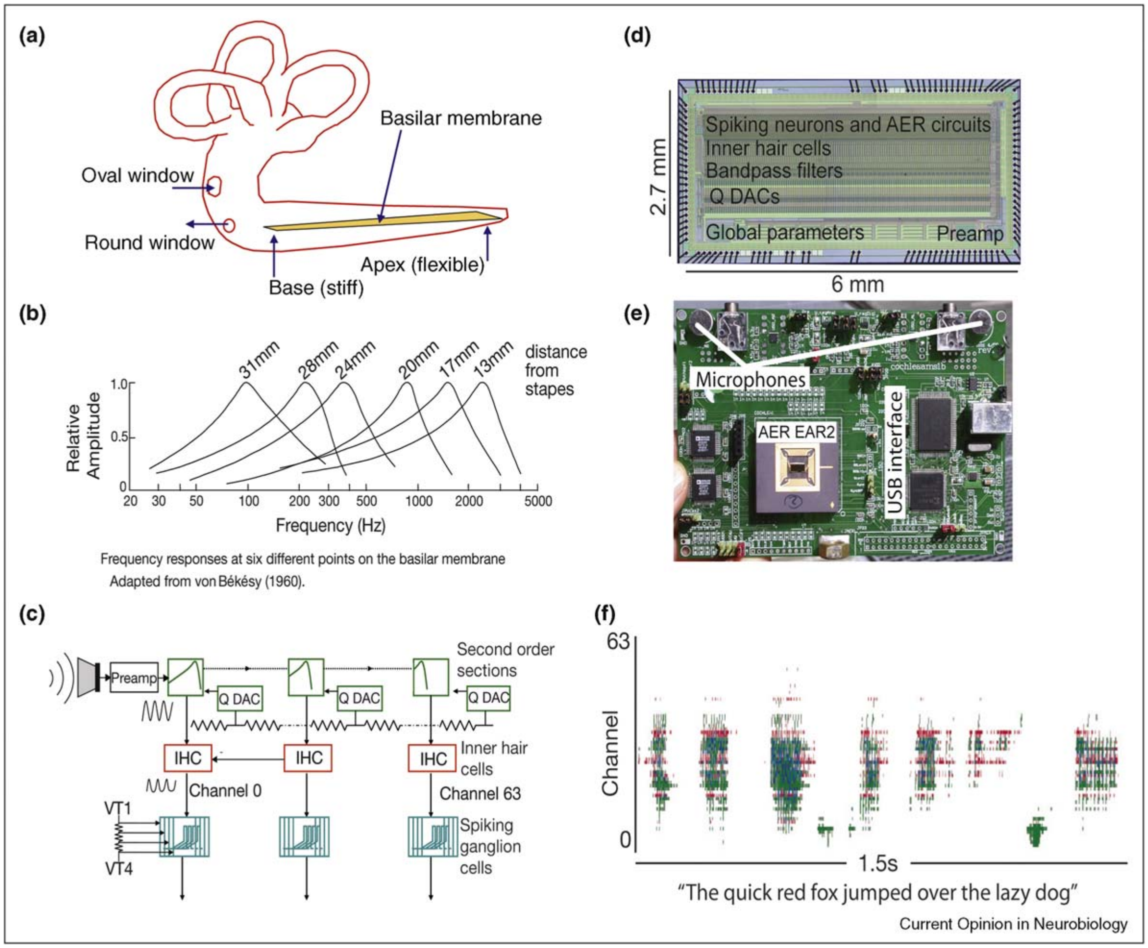
Silicon cochleas model the functionality of the biological counterpart, in particular the traveling wave responses of the basilar membrane (BM) as a result of incoming sound waves. The transport of energy along the BM is modeled by an electronic filter bank consisting of multiple filters

Figure 1



Example of silicon retina system [24]. **(a)** The sensor emulates a part of the retina pathway that is not well served by conventional image sensors. We made the analogy between the sustained pathway of the biological retina and conventional cameras, as opposed to the transient pathway of the biological retina, which we model with the so-called Dynamic Vision Sensor (DVS). **(b)** The DVS pixel models a simplified 3-layer retina, where individual pixels are decoupled spatially but still use a temporal ''surround'' computed by each pixel independently. **(c)** The DVS pixel forms an abstraction of the photoreceptor-bipolar-ganglion cell information flow. It consists of three parts: a logarithmic photoreceptor, a differencing amplifier (bipolar cells), and two decision units (ganglion cells). The pixel output consists of asynchronous ON and OFF address-events that signal scene reflectance changes. **(d)** The spike events are computed by the pixel as illustrated. The continuous-time photoreceptor output, which encodes intensity logarithmically, is constantly monitored for changes since the last event was emitted by the pixel. A detected change in log intensity which exceeds a threshold value results in the emission of an ON or OFF event. The threshold is typically set to about 10% contrast. Communication of the event to the periphery resets the pixel, which causes the pixel to memorize the new log intensity value. **(e)** The pixels are arranged in an array and fabricated in a standard chip-making process. AER circuits along the periphery of the chip handle the access to the shared AER bus and ensure that all events are transmitted, even if there are collisions. Colliding pixels must wait for their turn for access to the AER bus. **(f)** The chips are integrated into a camera, interfaced either to a computer by USB, directly to a microcontroller, or to another neuromorphic chip via its AER interface. **(g)** Data collected from the DVS shows its characteristics: the events can be histogrammed in 2D-space over a certain time window to form an image which displays either the ON and OFF events as contrast (Faces), or as a gray scale showing the relative event time (Juggling event time), or they can be viewed in space-time to see the spatiotemporal structure (space-time spike events).

Figure 2



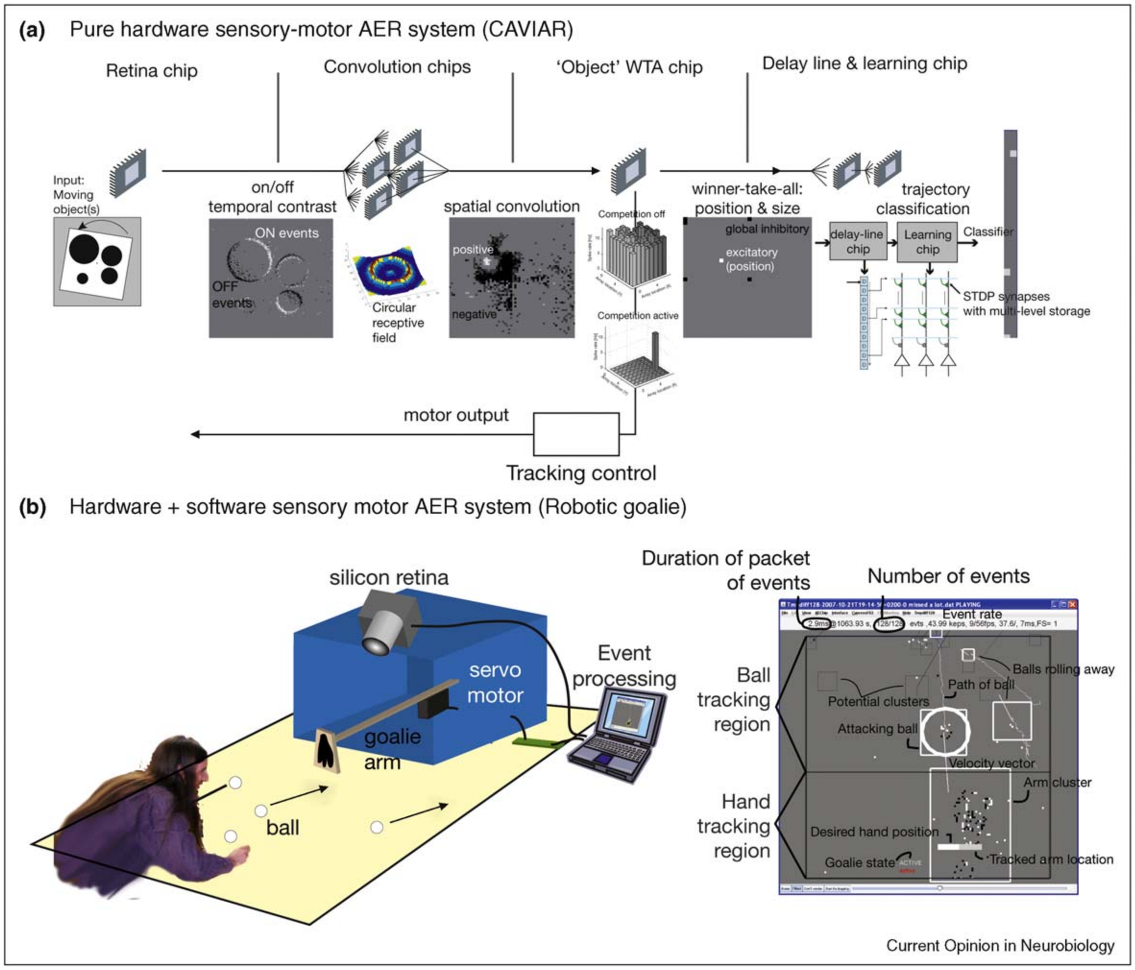
Example of silicon cochlea system [36]. **(a)** Simplified view of unrolled cochlea. **(b)** Responses of basilar membrane to different frequencies (adapted from von Békésy [59]). Depending on the frequency of an input tone, the frequency component of the pressure wave generated in the fluid leads to a maximum displacement at some place along the BM. The place depends on its characteristic frequency (CF). The CF has an exponentially decreasing value from the base to the apex of the BM. **(c)** Cascaded bank of second-order filter sections represents basilar membrane model, along with circuit blocks to model the half-wave rectification of the inner hair cells and multiple spiral ganglion cells with different thresholds (VT1–VT4). Digital to analog converters (Q DACs) in each channel allow adjustment of resonance properties. **(d)** Chip microphotograph of AER EAR2, a 64-stage binaural system where each ear is implemented as in (c). **(e)** User-friendly printed circuit board to hold the chip along with digital chips for USB interface to a laptop, microphones, and preamplifiers. **(f)** Spike raster response to speech ''The quick red fox jumped over the lazy dog''. The colors correspond to channels of the two ears.

which are arranged to model the physical properties of the BM. Initial prototypes used a 1D cascaded filter bank to model the response of the BM [27] (Figure 2b). Subsequent designs use filter banks with a cascaded or parallel architecture; or include circuits modeling the role of the fluid coupling between cochlea stages [28,29,30•]; and the local gain control in the biological cochlea [30•,31–33]. The latest designs also include circuits after the BM that emulate the hair cells and spiral ganglion cells [30•,34–36] and transmit asynchronous AER spikes like the silicon retina (see Figure 2). The timing information from the AER cochleas can be used for inferring the location of an acoustic source, for example, from the interaural time differences between sounds arriving to the two ears [37] or by emulating the echolocalization mechanism of bats [38]. The spike outputs can also be used to extract higher level auditory features suitable for tasks such as speaker identification [39]. The commonality of output representation in the retina and cochlea should open up a fruitful area in sensory fusion which exploits timing information for a coherent bimodal representation.

Neuromorphic sensory systems

In neuromorphic multi-chip sensory systems, AER sensor spikes travel in real-time to multi-neuron processors implementing neuron and synaptic circuit models of varying details [40,41,42•,43•]. Through the AER infrastructure, configuration of the network connectivity

Figure 3



Using events in AER systems. **(a)** The CAVIAR system [49••] used four different types of AER processing chips to continuously fixate a moving circular object of a certain size on a cluttered background. It had a total of 45,000 spiking neurons and could compute up to 12G synaptic connections per second. The output of the retina chip drove spike-based convolution chips which computed the responses of the circular receptive fields illustrated. An ''object'' winner-take-all chip then selected the peak of this filtered output. The location of this peak activity was used to continuously fixate the circular object that the system was configured to track. The delay line and learning chip components were used to learn common classes of trajectories. **(b)** The robotic goalie [15] also tracked circular objects (in this case balls shot at the goal), but in software rather than hardware. Multiple balls were simultaneously tracked and the one predicted by its position and velocity to first cross the goal line was blocked by moving the arm. To learn how to map motor commands to visual space, the goalie also tracked its own hand (unpublished result). Several behavioral states (blocking, actively waiting, and sleeping) were chosen based on a simple state machine with transitions that depended on past state and sensory input. The right panel shows a snapshot of 128 spike events from 2.4 ms of retina activity during the tracking of several balls and the goalie hand. Each retina event updates the putative location of a moving object (rectangles); events seed potential object locations (thin rectangles), and objects are discarded when they are no longer supported by events.

on-chip and across chips allows the expression of various network and system architectures. Multi-neuron chip systems are increasing in scale [42•,44] with as many as 65,000 neurons on a single chip (unpublished working system). Multi-chip sensory systems can demonstrate cortical visual properties such as orientation selectivity [45–47], stereopsis [48], and motion sensing with tracking [49••]. Cortical-like multi-layered AER systems which can implement neuroscience models of visual processing are also being realized [47,49••] along with sensory-motor AER systems [14••,49••] (see Figure 3 for two examples).

Challenges to application

Like every area in electronics, neuromorphic chip designers ultimately face the challenge of validating their approach by implementing commercially viable silicon designs. Transistor current variability is one of the main challenges because it severely limits precision, especially across an array of nominally identical circuits [50]. Silicon circuits cannot easily imitate the complex, rich molecular machinery of cells which enable the latter to continuously adapt their operating parameters to changes in their environment. Synchronous digital logic circuits are partially so successful because they deal with this transistor variability by simply restoring every logic circuit output to one of two possible voltage values. However, clever circuit and system design can be used to mimic biology's adaptation schemes and to reduce unwanted response variances across pixels in the chips. This understanding has led to recent neuromorphic sensors with performance that can exceed conventional technology, especially in applications like low power, high speed, or wide dynamic range vision [20–25,26•], and neural prosthetics [51•,52•]. A small number of studies have exploited transistor variability for computation. For example, an orientation-selective network refines its local orientation preference starting from the intrinsic preference embodied by the built-in variability of transistors [53] and a network of spiking neurons refines its synchronicity using relative spike-timing [12].

Future neuromorphic computation

For much of its history, neuromorphic engineers have aimed to build ''pure'' neuromorphic AER systems consisting of multiple interconnected, mostly feed-forward neuromorphic chips. These hardware systems have proved to be more difficult to configure than software, in large part because of the general lack of understanding of how we can compose real-time behaving systems out of independent modules. Although we understand something about building hierarchical networks for feature extraction and classification (e.g. [54,55]), little is known about building systems that express a suite of behaviors using these generic modules.

However, we have started to make some inroads into event-driven sensory and sensory-motor algorithms by combining AER sensors with conventional computers. An open-source software project (jaer.wiki.sourceforge.net) provides the possibility of processing AER sensor events using software algorithms. The software infrastructure is optimized for using the event timing. For example, local features like orientation and motion can be extracted using temporal coherence and relative timing of events [56]. The main practical application area so far has been fast object tracking using the temporal clustering of events [57] (see Figure 3b for an example). These developments show advantages gained from the reduction in latency and processor load with event-driven sensor representations [14,15,57].

Just as large microprocessor companies support open-source computer vision and machine learning software projects to understand the required features of future generations of processors, software processing of AER data will suggest neuromorphic hardware that needs to be developed. Future advances in neuromorphic sensory systems will also depend on ongoing work of how we can systematically combine modules to produce a desired function [58], on understanding probabilistic inference methods in nervous systems, and on the evolution of algorithms into hardware.

Acknowledgements

We thank members and former members of the Institute of Neuroinformatics; in particular RJ Douglas and K Martin, and the hardware group; the following readers for useful comments on the articles, U Rutishauser, A Benucci, N. da Costa, P. Baker; and the NSF Telluride Neuromorphic Cognitive Engineering Workshop.

References and recommended reading

Papers of particular interest, published within the period of review, have been highlighted as:

- • of special interest
- •• of outstanding interest

1. • Thrun S, Montemerlo M, Dahlkamp H, Stavens D, Aron A, Diebel J, Fong P, Gale J, Halpenny M, Hoffmann G: **Stanley: the robot that won the DARPA Grand Challenge**. *J Field Robot* 2006, **23**:661-692.

These cars were utterly dependent on Global Positioning System (GPS) for navigation, hardly used vision, and carried on the order of 1 kW of conventional computing power.

2. • Ananthanarayanan R, Esser SK, Simon HD, Modha DS: **The cat is out of the bag: cortical simulations with 109 neurons, 1013 synapses**. In *Proceedings of the Conference on High Performance Computing Networking, Storage and Analysis; ACM, Portland, Oregon: 2009:1-12*.

This ''cat scale'' brain simulation requires a 1.4 MW supercomputer with 147,000 processors which weighs 28,000 kg, requires 500 tons of air conditioning, and runs simplified point neurons about 700 times slower than real time.

3. Boahen K: **Neuromorphic microchips**. *Sci Am* 2005, **292**:56-63.

4. Mead C: **Neuromorphic electronic systems**. *Proc IEEE* 1990, **78**:1629-1636.

5. Douglas R, Mahowald MA, Mead C: **Neuromorphic Analog VLSI**. *Annu Rev Neurosci* 1995, **18**:255-281.

6. Laughlin S, Sejnowski T: **Communication in neuronal networks**. *Science* 2003, **301**:1870-1874.

7. Mead C: *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley; 1989.

8. Cole KS, Curtis HJ: **Electrical impedance of nerve during activity**. *Nature* 1938, **142**:209-210.

9. Hodgkin AL, Huxley AF: **A quantitative description of membrane current and its application to conduction and excitation in nerve**. *J Physiol* 1952, **117**:500-544.

10. • Merolla P, Arthur J, Shi BE, Boahen K: **Expandable networks for neuromorphic chips**. *IEEE Trans Circuits Syst I* 2007, **54**:301-311.

The authors describe an AER infrastructure for connecting multiple chips in a daisy-chain which allows for system scalability. Systems that consist of multiple chips speaking the same AER language can then be composed out of single chip modules almost like LEGO blocks. Because of the similarity with biology of the spike transmission process in the neuromorphic circuits, neuromorphic engineering is in a good position to look at event-driven computation in natural systems and event-driven coding schemes. Continual discussions of rate coding and temporal coding schemes pervade the neuroscience field and similar questions can be asked of the neuromorphic hardware.

11. • Boerlin M, Delbruck T, Eng K: **Getting to know your neighbors: unsupervised learning of topography from real-world, event-based input**. *Neural Comput* 2009, **21**:216-238.

This work shows how the timing of spikes can be used to develop topographical connections between layers when the cells in both input and output layers have only local knowledge of spike activity.

12. Arthur JV, Boahen K: **Learning in silicon: timing is everything**. In *Advances in Neural Information Processing Systems*, vol. 18. Edited by Sholkopf B, Weiss Y. MIT Press; 2006:75-82.

13. Mitra S, Fusi S, Indiveri G: **Real-time classification of complex patterns using spike-based learning in neuromorphic VLSI**. *IEEE Trans Biomed Circuits Syst* 2009, **3**:32-42.

14. •• Conradt JC, Berner R, Cook M, Delbruck T: **An embedded AER dynamic vision sensor for low-latency pole balancing**. *5th IEEE Workshop on Embedded Computer Vision*; *Kyoto, Japan: 2009*.

By using the output from two AER silicon retinas, this pencil balancing robot can be built using only simple microcontrollers burning a total of less than a watt of power. Using conventional high-frame-rate cameras for the same robot would require an entire state-of-the-art PC which burns more than a hundred times the power.

15. Delbruck T, Lichtsteiner P: **Fast sensory motor control based on event-based hybrid neuromorphic-procedural system**. *IEEE Int Symp Circuits Syst* 2007:845-848.

16. Barlow HB: **Possible principles underlying the transformation of sensory messages**. In *Sensory Communication.* Edited by Rosenblith WA. Cambridge, MA: MIT Press; 1961:217-234.

17. Sterling P, Demb J: **Retina**. In *The Synaptic Organization of the Brain,* 5th ed.. Edited by Shepherd GM. New York: Oxford University Press; 2004.

18. Mahowald MA, Mead C: **The silicon retina**. *Sci Am* 1991, **264**:76-82.

19. Zaghloul KA, Boahen K: **A silicon retina that reproduces signals in the optic nerve**. *J Neural Eng* 2006, **3**:257-267.

20. • Shimonomura K, Kushima T, Yagi T: **Binocular robot vision emulating disparity computation in the primary visual cortex**. *Neural Networks* 2008, **21**:331-340.

A high-performance sustained-pathway retina system which uses a conventional frame-sampled image sensor pixel which is then coupled to a lateral resistive network which models the horizontal cell network. The difference between the local intensity value and the spatially low-pass filtered image is output from the sensor.

21. Ruedi PF, Heim P, Kaess F, Grenet E, Heitger F, Burgi PY, Gyger S, Nussbaum P: **A 128 $\times$ 128 pixel 120-dB dynamic-range vision-sensor chip for image contrast and orientation extraction**. *IEEE J Solid-State Circuits* 2003, **38**:2325-2333.

22. Costas-Santos J, Serrano-Gotarredona T, Serrano-Gotarredona R, Linares-Barranco B: **A spatial contrast retina with on-chip Calibration for Neuromorphic spike-based AER vision systems**. *IEEE Trans Circuits Syst I: Regular Papers* 2007, **54**:1444-1458.

23. Culurciello E, Etienne-Cummings R, Boahen KA: **A biomorphic digital image sensor**. *IEEE J Solid-State Circuits* 2003, **38**:281-294.

24. Lichtsteiner P, Posch C, Delbruck T: **A 128 $\times$ 128 120 dB 15us latency asynchronous temporal contrast vision sensor**. *IEEE J Solid-State Circuits* 2008, **43**:566-576.

25. Posch C, Matolin D, Wohlgenannt R: **A QVGA 143 dB DR asynchronous address-event PWM dynamic image sensor with lossless pixel-level video compression**. *ISSCC Dig. of Tech. Papers* 2010:400-401.

26. • Delbruck T, Linares-Barranco B, Culurciello E, Posch C: **Activity-driven, event-based vision sensors**. *IEEE Intl Symp Circuits Syst Paris* 2010:2426-2429.

This review of recent advances in event-based vision sensor design covers technical advances in sensor architectures.

27. Lyon RF, Mead C: **An analog electronic cochlea**. *IEEE Trans Acoust Speech Signal Process* 1988, **36**:1119-1134.

28. Fragniere E: **A 100-channel analog CMOS auditory filter bank for speech recognition**. *ISSCC Dig. of Tech. Papers* 2005, 140–589.

29. Hamilton T, Tapson J, Jin C, van Schaik A: **An active 2-D silicon cochlea**. *IEEE Trans Biomed Circuits Syst* 2008, **2**:30-43.

30. • Wen B, Boahen K: **A silicon cochlea with active coupling**. *IEEE Trans Biomed Circuits Syst* 2009, **3**:444-455.

Active basilar control in this bidirectional fluid coupled silicon cochlea argues for a specific role of the outer hair cells.

31. Katsiamis A, Drakakis E, Lyon R: **A 4.5 μW, 120 + dB, log-domain cochlea channel with AGC**. *IEEE J Solid-State Circuits* 2009, **44**:1006-1022.

32. Martignoli S, van der Vyver JJ, Kern A, Uwate Y, Stoop R: **Analog electronic cochlea with mammalian hearing characteristics**. *Appl Phys Lett* 2007, **91**:064108.

33. Mandal S, Zhak SM, Sarpeshkar R: **A bio-inspired active radio-frequency silicon cochlea**. *IEEE J Solid-State Circuits* 2009, **44**:1814-1828.

34. Lazzaro J, Wawrzynek J, Mahowald M, Sivilotti M, Gillespie D: **Silicon auditory processors as computer peripherals**. *IEEE Trans Neural Networks* 1993, **4**:523-528.

35. Abdalla H, Horiuchi T: **An ultrasonic filterbank with spiking neurons**. *Proc IEEE Int Circuits Syst* 2005, **5**:4201-4204.

36. Liu S-C, van Schaik A, Minch B, Delbruck T: **Event-based 64-channel binaural silicon cochlea with Q enhancement mechanisms**. *IEEE Int Symp Circuits Syst* 2010:2027-2030.

37. Chan V, Liu S-C, van Schaik A: **AER EAR: a matched silicon cochlea pair with address event representation interface**. *IEEE Trans Circuits Syst I (Special Issue on Smart Sensors)* 2007, **54**:48-59.

38. Horiuchi TK: **A spike-latency model for sonar-based navigation in obstacle field**. *IEEE Trans Circuits Syst I* 2009, **56**:2393-2401.

39. Liu S-C, Mesgarani N, Harris J, Hermansky H: **The use of spike-based representations for hardware audition systems**. *IEEE Intl Symp Circuits Syst* 2010:505-508.

40. Liu S-C, Kramer J, Indiveri G, Douglas RJ: *Analog VLSI: Circuits and principles.* MIT Press; 2002.

41. Hynna KM, Boahen K: **Thermodynamically-equivalent silicon models of ion channels**. *Neural Comput* 2007, **19**:327-350.

42. • Silver R, Boahen K, Grillner S, Kopell N, Olsen KL: **Neurotech for neuroscience: unifying concepts, organizing principles, and emerging tools**. *J Neurosci* 2007, **27**:11807-11819.

Highlights state-of-the-art work in developing high-density arrays of biophysical models of neurons and synapses. The latest system has 61 graded and 18 binary programmable parameters allowing Neurocore to model a wide variety of spiking and connectivity patterns. Each neuron has a soma, a dendrite, four synapse populations, and four ion-channel populations. Circuits implement pairs of gating variables to model ion-channel populations. The synaptic circuits that consist of low-pass filters can be configured to drive the soma, dendrite, or to see an ion-channel population's maximum conductance. The same type of gating-variable circuits are used to model different synapses and receptors and cholinergic modulation.

43. • Indiveri G, Liu S-C, Delbruck T, Douglas RJ: **Neuromorphic systems**. In *Encyclopedia of Neuroscience.* Edited by Squire L. Academic Press; 2009:521-528.

This review focuses on silicon neurons, synapses, and communication technology.

44. Schemmel J, Fieres J, Meier K: **Wafer-scale integration of analog neural networks**. *IEEE Int Joint Conf Neural Networks* 2008:431-438.

45. Choi TYW, Merolla P, Arthur J, Boahen K, Shi BE: **Neuromorphic implementation of orientation hypercolumns**. *IEEE Trans Circuits Syst I: Regular Papers* 2005, **52**:1049-1060.

46. Chicca E, Whatley AM, Lichtsteiner P, Dante V, Delbruck T, Del Giudice P, Douglas RJ, Indiveri G: **A multi-chip pulse-based neuromorphic infrastructure and its application to a model of orientation selectivity**. *IEEE Trans Circuits Syst I: Regular Papers* 2007, **54**:981-993.

47. Vogelstein RJ, Mallik U, Culurciello E, Cauwenberghs G, Etienne-Cummings R: **A multi-chip neuromorphic system for spike-based visual information processing**. *Neural Comput* 2007, **19**:2281-2300.

48. Mahowald MA: *An Analog VLSI System for Stereoscopic Vision*. Boston: Kluwer; 1994.

49. •• Serrano-Gotarredona R, Oster M, Lichtsteiner P, Linares-Barranco A, Paz-Vicente R, Gomez-Rodriguez F, Camunas-Mesa L, Berner R, Rivas M, Delbruck T *et al.*: **CAVIAR: A 45k-**

neuron, 5M-synapse, 12G-connects/sec AER hardware sensory-processing-learning-actuating system for high speed visual object recognition and tracking. *IEEE Trans Neural Networks* 2009, **20**:1417-1438.
The largest scale multi-chip AER sensory processing system to date. This project integrated neuromorphic AER chips designed by four groups from different countries.

50. Sarpeshkar R: **Analog versus digital: extrapolating from electronics to neurobiology**. *Neural Comput* 1998, **10**:1601-1638.

51. • Rothermel A, Liu L, Pour-Aryan N, Fischer M, Wünschmann J, Kibbel S, Harscher A: **A CMOS chip with active pixel array and specific test features for subretinal implantation**. *IEEE J Solid-State Circuits* 2009, **44**:290-300 (Special Issue on ISSCC 2008).
Although it would seem that neuromorphic sensors would serve as ideal front ends for neural prosthetics, in practice developers of prosthetics are concerned mostly with issues of neural interfacing, long-term stability, power supply, device control, and clinical trials. As a result, recent advances in vision prosthetics such as this one focus on device fabrication and neural stimulation.

52. • Sit J, Sarpeshkar R: **A cochlear-implant processor for encoding music and lowering stimulation power**. *IEEE Pervasive Comput* 2008, **1**:40-48 (Special Issue on Implantable Electronics).
This paper describes state-of-the-art work in preprocessing audio for implants using a bio-inspired approach. State-of-the-art hearing aids burn only about 1mW and do a substantial amount of digital signal processing. Cochlear implants put most of the computation external to the body; the implant itself is a stimulator which provides pulses to stimulate the spiral ganglion cells. For this auditory prosthetics, power consumption is dominated by stimulation and communication, so there has not been a strong industrial drive for the reduced power consumption that a neuromorphic auditory front end could offer.

53. Merolla P, Boahen K: **A recurrent model of orientation maps with simple and complex cells**. In *Advances in Neural Information Processing Systems*, vol. 16. Edited by Thrun S, Saul L. MIT Press; 2004:995-1002.

54. Serre T, Oliva A, Poggio T: **A feedforward architecture accounts for rapid categorization**. *Proc Natl Acad Sci* 2007, **104**:6424-6429.

55. Riesenhuber M, Poggio T: **Neural mechanisms of object recognition**. *Curr Opin Neurobiol* 2002, **12**:162-168.

56. Delbruck T: **Frame-free dynamic digital vision**. In *Proceedings of Intl. Symp. on Secure-Life Electronics, Advanced Electronics for Quality Life and Society*; *Tokyo, University of Tokyo: 2008*.

57. Litzenberger M, Posch C, Bauer D, Schön P, Kohn B, Garn H, Belbachir A: **Embedded vision system for real-time object tracking using an asynchronous transient vision sensor**. *IEEE Digital Signal Processing Workshop 2006*; *Grand Teton, Wyoming: 2006:173-178*.

58. Rutishauser U, Douglas R: **State-dependent computation using coupled recurrent networks**. *Neural Comput* 2009, **21**:478-509.

59. von Békésy G: *Experiments in Hearing*. New York: McGraw-Hill; 1960.