377 Operating Systems

Paging Smaller Tables

Question?

If you have a 32 bit virtual address space and 4kB pages and each PTE in a linear page table is 4 bytes and you have 256 processes, how much space do all of the page tables take up?

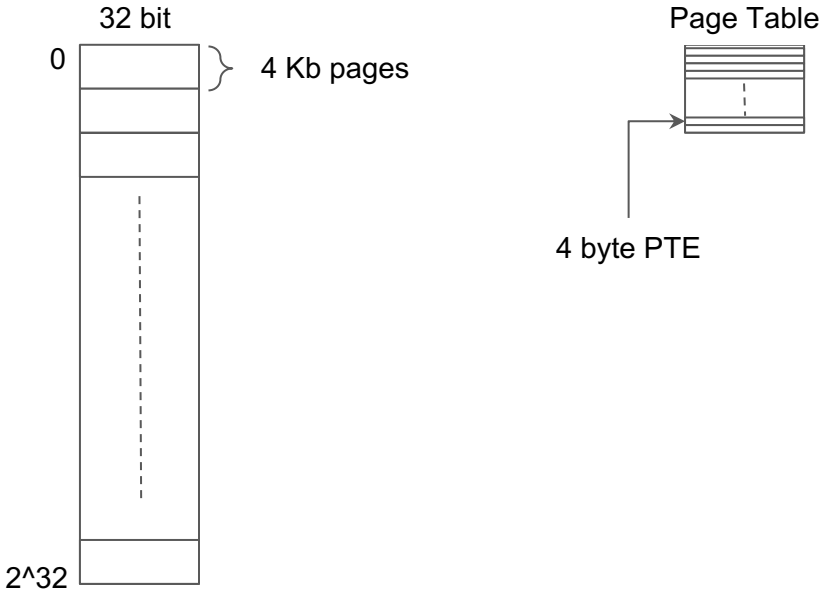
(A) 2^12 bytes

(B) 2^20 bytes

(C) 2^22 bytes

(D) 2^24 bytes

(E) 2^30 bytes



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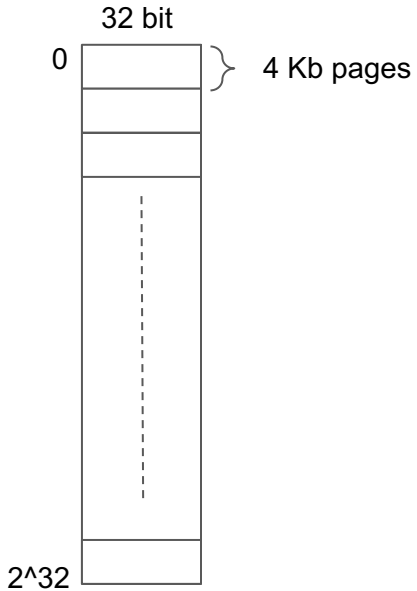
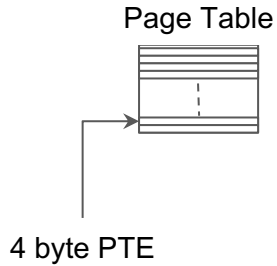
First, we need to figure out how many pages in a 32-bit address space.

2^12 = 4 Kb

2^32 / 2^12 = 2^20

So, 2^20 pages.





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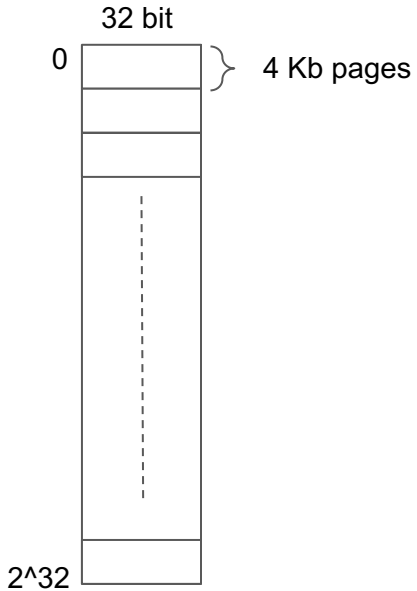
If we have 2^20 pages, we need to have a PTE for each.

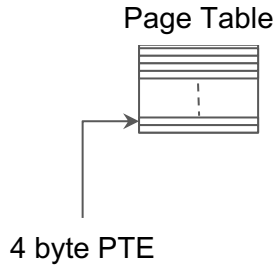
This means, 2^20 PTEs.

If each PTE is 4 bytes, we have:

2^2 * 2^20 = 2^22

2^22 bytes (4 MB)





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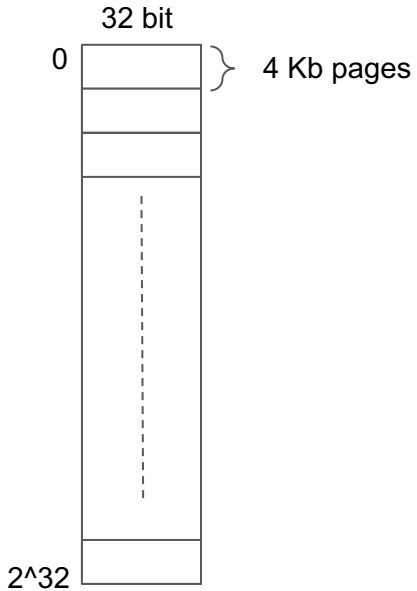
If we have 4 MB page tables and 256 processes, then we have

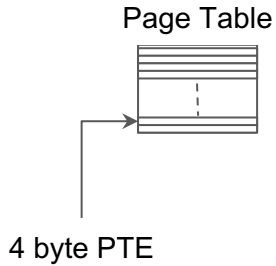
4 * 256 = 1024 MB

Or, 1 GB

2^22*2^2*2^8 = 2^30 bytes

Way too much!





From Before…

A page table contains a mapping from virtual pages to physical page frames

There is one page table per process

Two Problems

Page tables are slow:

Address translation requires looking for the PFN in the page tables' PTEs.

This adds one memory access per memory access…

Fix with a cache: The TLB

But, we have another problem…

Two Problems

Linear page tables are big

If there are many pages :

(2^32/2^12 = 2^20)

and page table entries are 4 bytes, then each page table is 2^22 bytes! (4MB)

We will fix that today…

Simple Solution

Bigger Pages!

Example:

Take our 32-bit address space:

Use 16KB pages, PTE=18-bit VPN,14-bit offset

Assuming 4-byte PTE, 2^18 or 1MB Page Table

Not surprising, factor of 4 reduction

Problem?

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Example:

Take our 32-bit address space:

Use 16KB pages, PTE=18-bit VPN,14-bit offset

Assuming 4-byte PTE, 2^18 or 1MB Page Table

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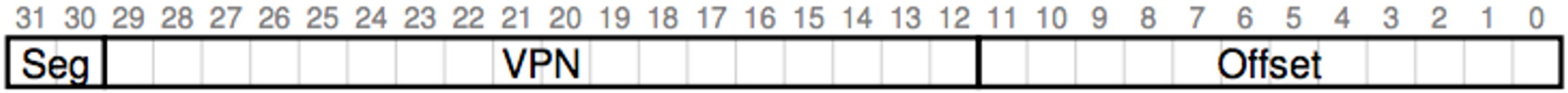
Problem? **Wasted space in pages!**

Hybrid: Segmentation + Paging



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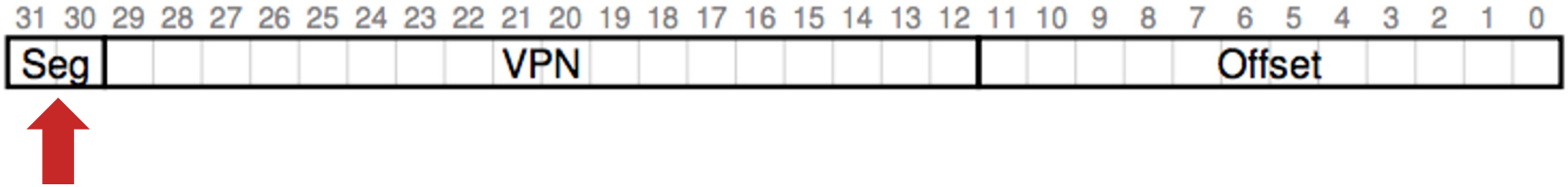
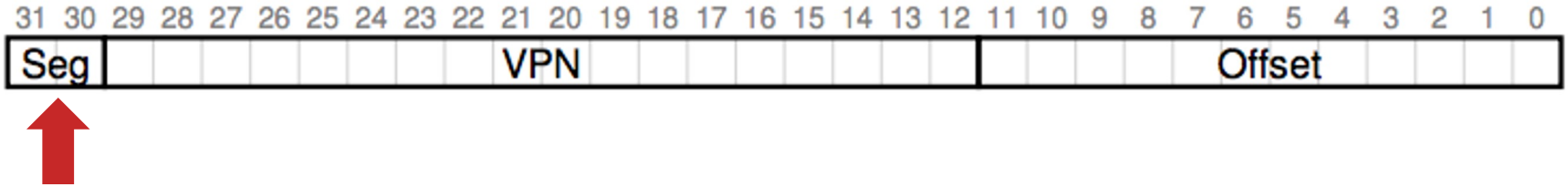


- Segment tells us: code, stack, or heap

Hybrid: Segmentation + Paging



- Segment tells us: code, stack, or heap
- That gives us which page table

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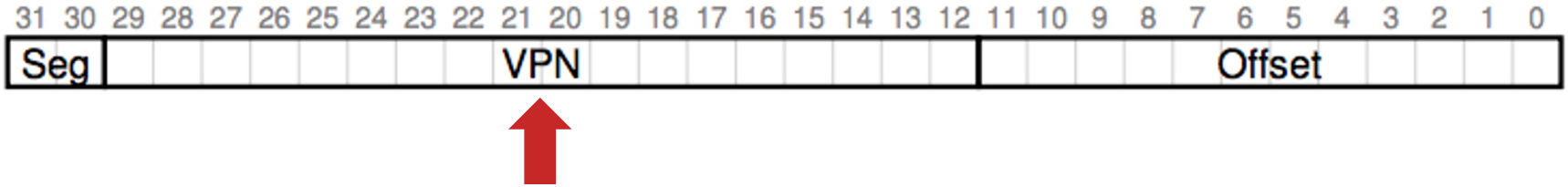


- Segment tells us: code, stack, or heap
- That gives us which page table
- The Virtual page number tells us which entry in that table

Ok, so why not?

- This is actually pretty complicated..
- Page tables are now variable sizes and we have to put them into memory, which leads to an allocator/fragmentation problem
- If the heap is large, but much of it unused in the middle, we still have to have a page table for the whole bound.
- Segments mean we are dictating to programs that they have to have three segments…

Ok, what does work?

Multi-level page tables

- This is used in the x86 processor
- Instead of one linear array, we will make page tables into a tree
- Chunk the page table up into pages and introduce a higher level table called a Page Directory

How does the CPU know where the page tables are?

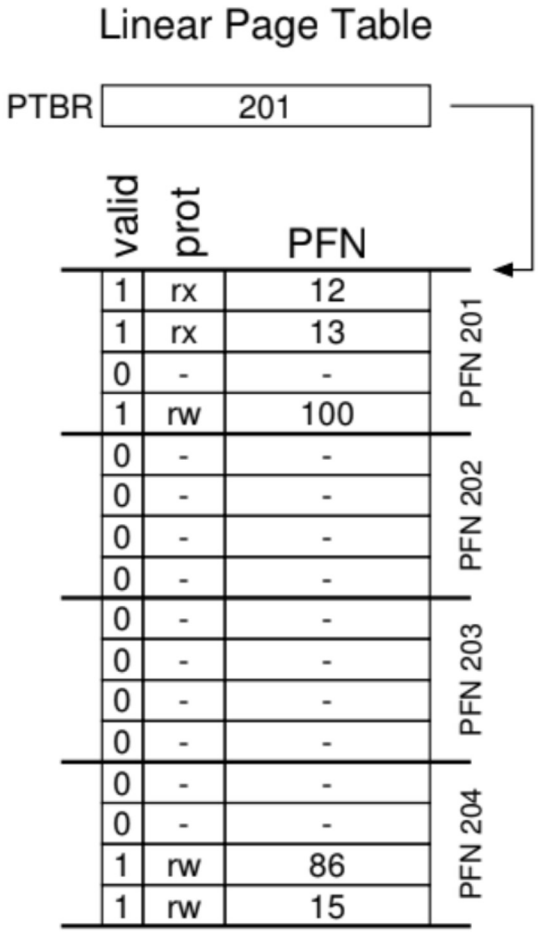
- On a context switch, we have to invalidate the TLB
- We also have to load a value for the process into a register called the Page Directory Base Register (PDBR)
- The MMU uses this register to find the page table

Linear Page Table Structure

This is the structure of a basic linear page table.

The PTBR holds an address that points to the start of the page table in memory.

Each entry in the table has a PFN referencing the page in physical memory.

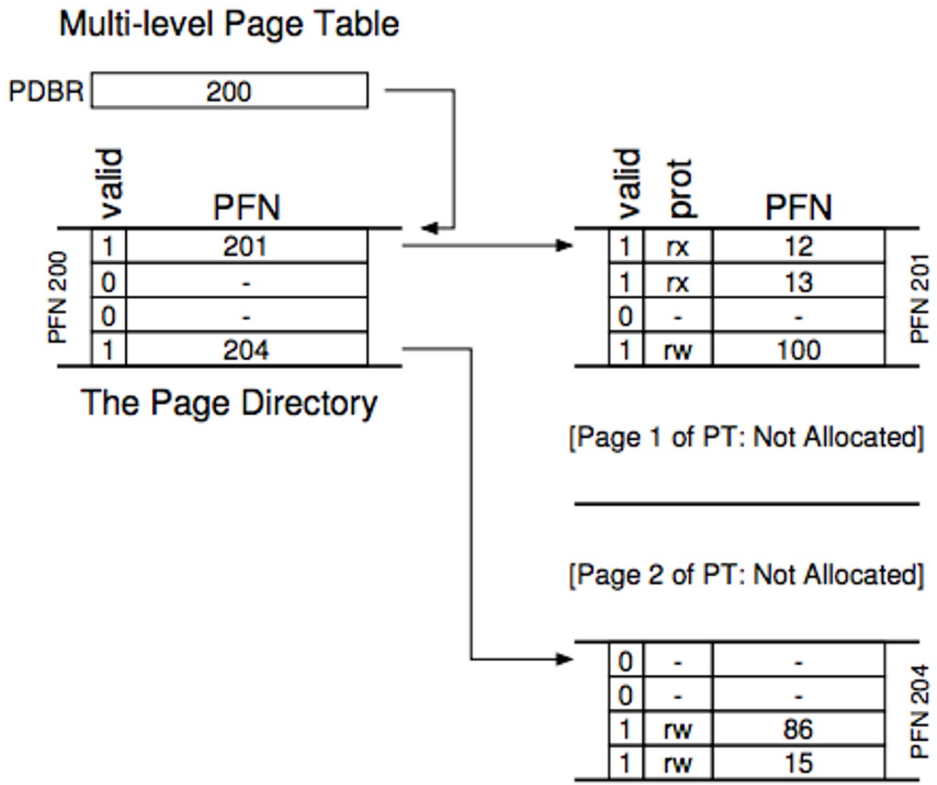


Multi-Level Page Table Structure

This is the structure of a 2-level page table.

The PTBR holds an address that points to the start of the page table directory in memory.

Each entry in the table has a PFN referencing a page table (also in memory).



Linear PT Example

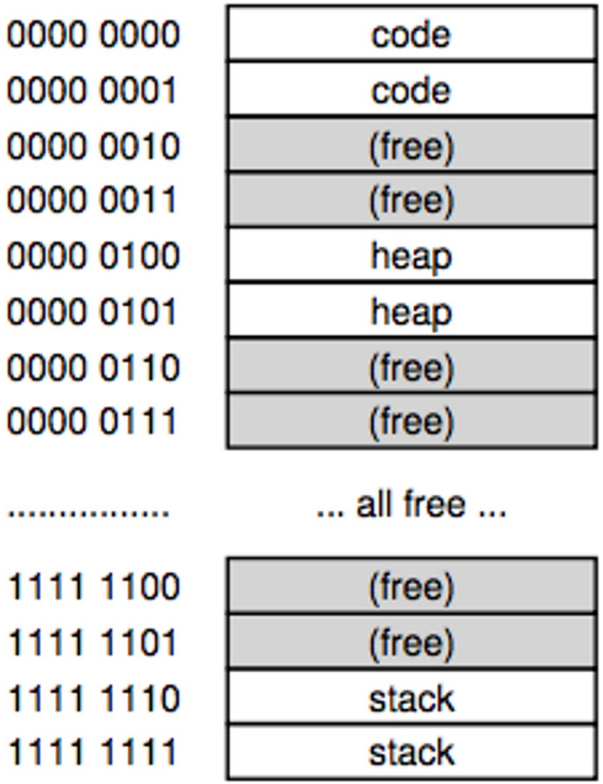
Start with a small address space:

16kB with 64 byte pages

So 14 bit addresses (8 bits for the VPN and 6 bits for the offset)

A linear (one level) page table has 256 entries

If each PTE is 4 bytes: **size = 1kB**



Linear PT Example

(16*1024)/64 = 256 pages
8 bits for VPN, 2^8 = 256
256 entries * 4 bytes =
1024 bytes or
1kB

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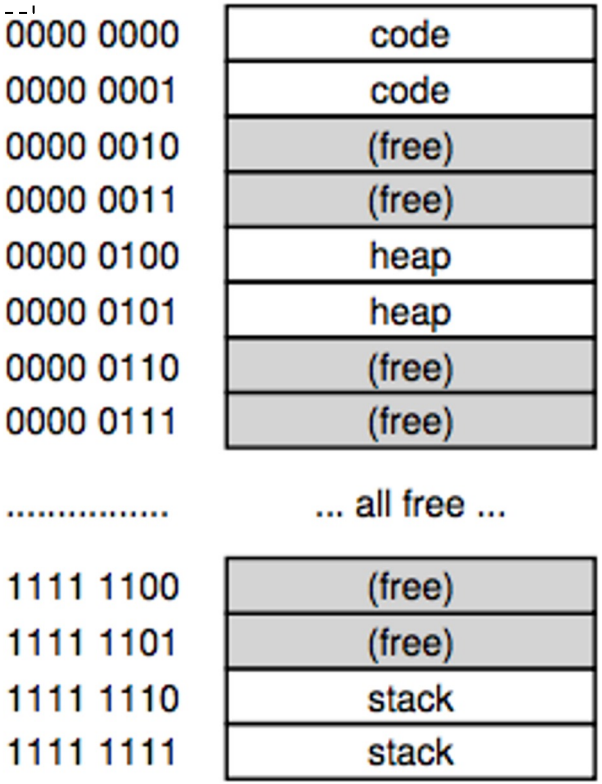
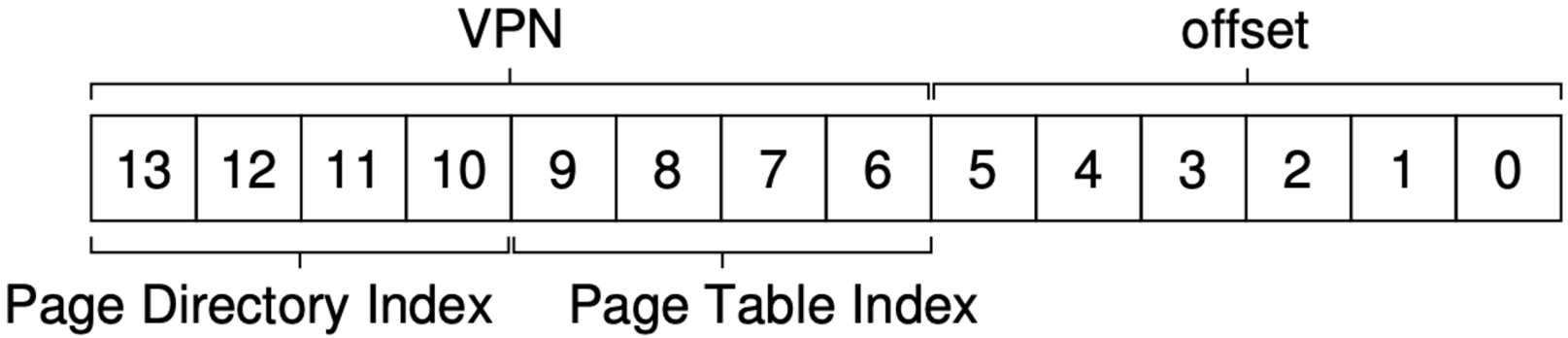


2-Level Page Table Example

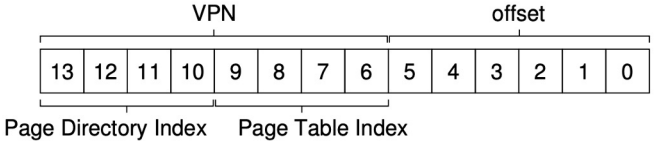
Take the 1kB Page table and divide it into 16, 64 byte pages

A 64 byte page can hold 16 4 byte PTEs

To index into the 16 pages of the page table, we need 4 bits



Example



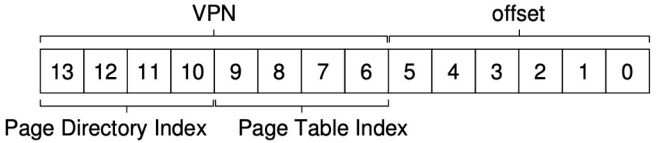
ignores offset

0000 0000	code
0000 0001	code
0000 0010	(free)
0000 0011	(free)
0000 0100	heap
0000 0101	heap
0000 0110	(free)
0000 0111	(free)
.....	... all free ...
1111 1100	(free)
1111 1101	(free)
1111 1110	stack
1111 1111	stack

Page Directory		Page of PT (@PFN:100)			Page of PT (@PFN:101)		
PFN	valid?	PFN	valid	prot	PFN	valid	prot
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0000



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100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

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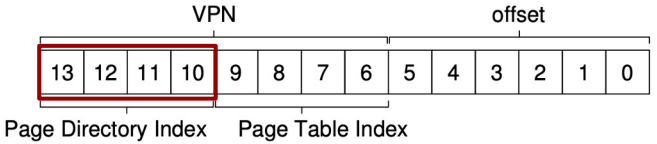

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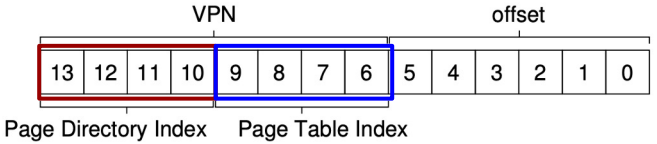
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0000



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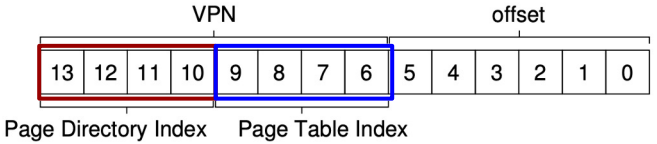
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0001



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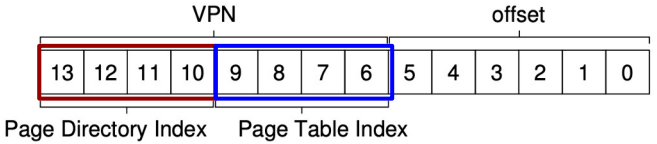
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0010



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0000 0000	code
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0000 0010	(free)
0000 0011	(free)
0000 0100	heap
0000 0101	heap
0000 0110	(free)
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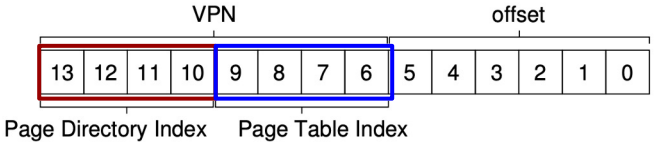
PFN	valid?	PFN	valid	prot	PFN	valid	prot
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0011



ignores offset

0000 0000	code
0000 0001	code
0000 0010	(free)
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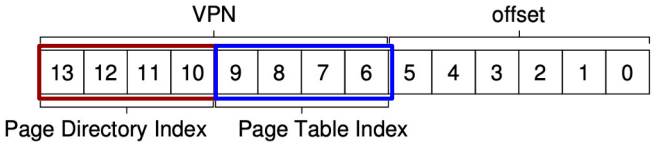
PFN	valid?	PFN	valid	prot	PFN	valid	prot
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0100



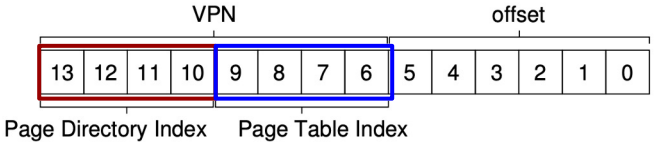
ignores offset

0000 0000	code
0000 0001	code
0000 0010	(free)
0000 0011	(free)
0000 0100	heap
0000 0101	heap
0000 0110	(free)
0000 0111	(free)
.....	... all free ...
1111 1100	(free)
1111 1101	(free)
1111 1110	stack
1111 1111	stack

Page Directory		Page of PT (@PFN:100)			Page of PT (@PFN:101)		
PFN	valid?	PFN	valid	prot	PFN	valid	prot
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 0000 0101

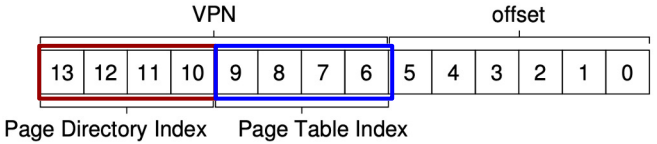


ignores offset	
0000 0000	code
0000 0001	code
0000 0010	(free)
0000 0011	(free)
0000 0100	heap
0000 0101	heap
0000 0110	(free)
0000 0111	(free)
.....	... all free ...
1111 1100	(free)
1111 1101	(free)
1111 1110	stack
1111 1111	stack

Page Directory		Page of PT (@PFN:100)			Page of PT (@PFN:101)		
PFN	valid?	PFN	valid	prot	PFN	valid	prot
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 1111 1110



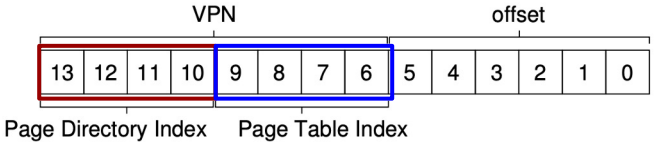
ignores offset

0000 0000	code
0000 0001	code
0000 0010	(free)
0000 0011	(free)
0000 0100	heap
0000 0101	heap
0000 0110	(free)
0000 0111	(free)
.....	... all free ...
1111 1100	(free)
1111 1101	(free)
1111 1110	stack
1111 1111	stack

Page Directory		Page of PT (@PFN:100)			Page of PT (@PFN:101)		
PFN	valid?	PFN	valid	prot	PFN	valid	prot
100	1	10	1	r-x	—	0	—
—	0	23	1	r-x	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

Example

0x00 = 1111 1111



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1111 1110	stack
1111 1111	stack

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—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	80	1	rw-	—	0	—
—	0	59	1	rw-	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	—	0	—
—	0	—	0	—	55	1	rw-
101	1	—	0	—	45	1	rw-

```
VPN = (VirtualAddress & VPN_MASK) >> SHIFT
(Success, TlbEntry) = TLB_Lookup(VPN)
if (Success == True)   // TLB Hit
  if (CanAccess(TlbEntry.ProtectBits) == True)
    Offset   = VirtualAddress & OFFSET_MASK
    PhysAddr = (TlbEntry.PFN << SHIFT) | Offset
    Register = AccessMemory(PhysAddr)
  else
    RaiseException(PROTECTION_FAULT)
else                   // TLB Miss
  // first, get page directory entry
  PDIndex = (VPN & PD_MASK) >> PD_SHIFT
  PDEAddr = PDBR + (PDIndex * sizeof(PDE))
  PDE     = AccessMemory(PDEAddr)
  if (PDE.Valid == False)
    RaiseException(SEGMENTATION_FAULT)
  else
    // PDE is valid: now fetch PTE from page table
    PTIndex = (VPN & PT_MASK) >> PT_SHIFT
    PTEAddr = (PDE.PFN << SHIFT) + (PTIndex * sizeof(PTE))
    PTE     = AccessMemory(PTEAddr)
    if (PTE.Valid == False)
      RaiseException(SEGMENTATION_FAULT)
    else if (CanAccess(PTE.ProtectBits) == False)
      RaiseException(PROTECTION_FAULT)
    else
      TLB_Insert(VPN, PTE.PFN, PTE.ProtectBits)
      RetryInstruction()
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```

So, what?

We save a bunch of space:

We went from a 1kB linear page table, to three pages (one for the directory and two for page tables)

3 * 64bytes = 192 bytes!

The **magic** is that each page table *fits in one page*.

So we can easily allocate page tables.

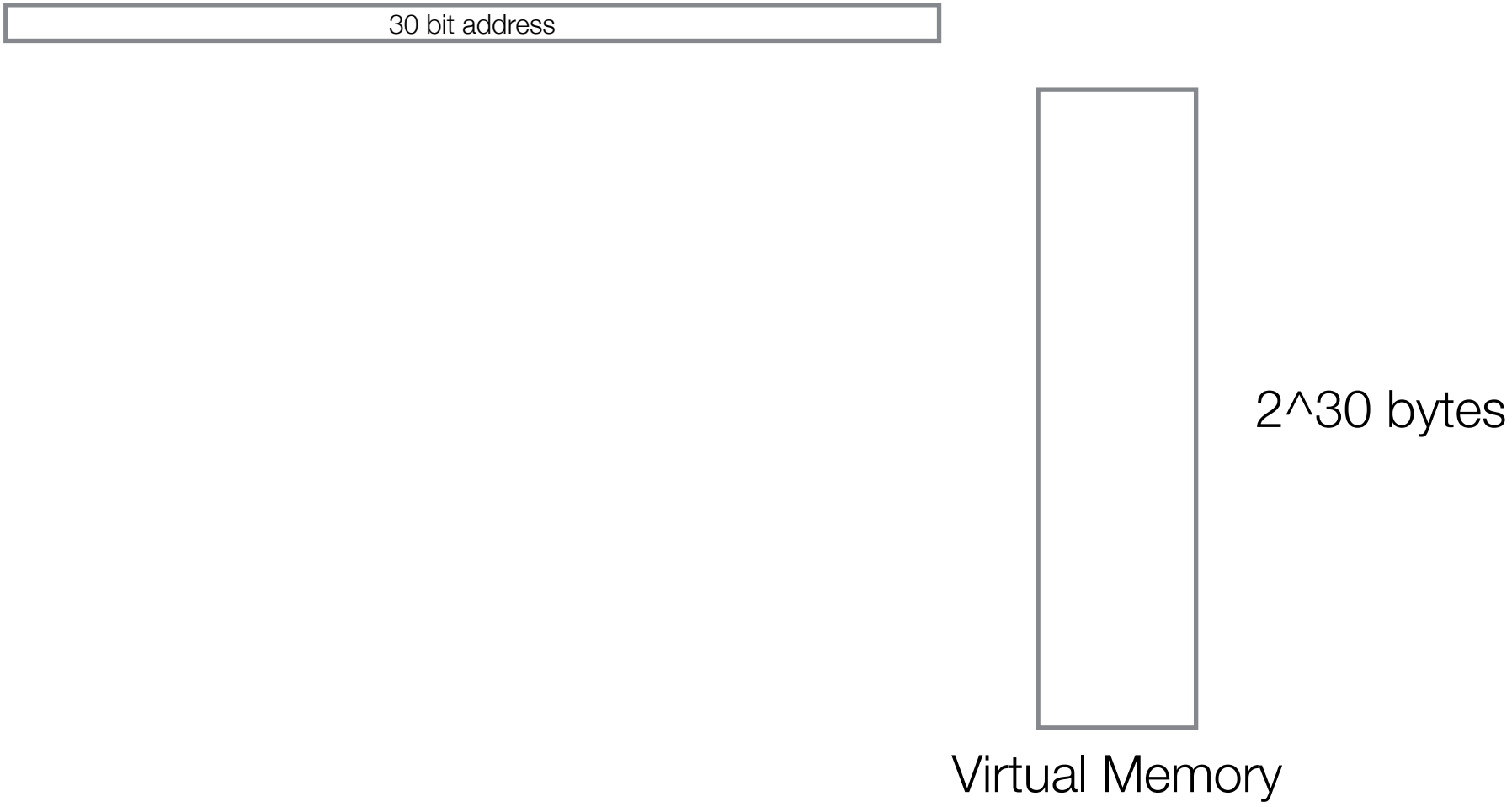
But we cooked the books on this example

Everything is small.

What about a real system?

What about more bits?

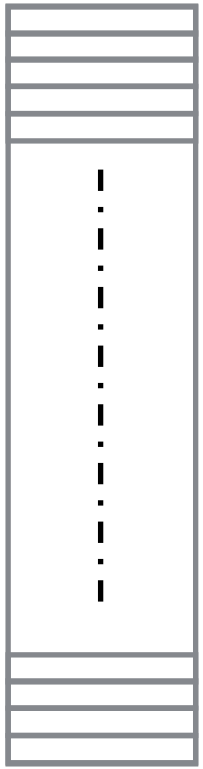
Let’s look at something more realistic, a 30 bit virtual address space with a page size of 512 bytes


30 bit address
2^30 bytes
Virtual Memory

30 bit address

Pages are 512 bytes

How many pages do we have?

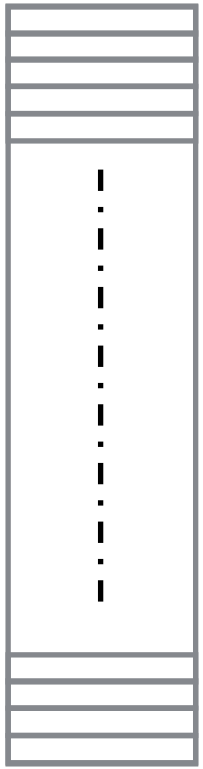


2^30 bytes

Virtual Memory

30 bit address

Pages are 512 bytes
We have 2^30/512 pages,
or 2^30/2^9 = 2^21
or 2,097,152 pages.



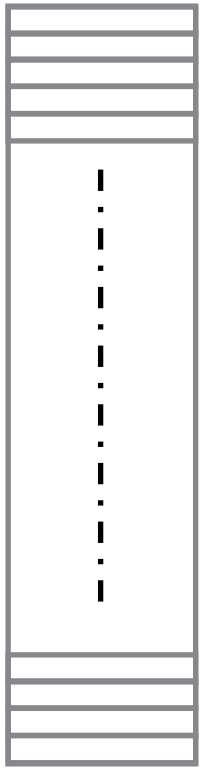
2^30 bytes

Virtual Memory

30 bit address

Pages are 512 bytes
We have 2^30/512 pages,
or 2^30/2^9 = 2^21
or 2,097,152 pages.

How many bits do we need for our offset if we have 512 byte pages?

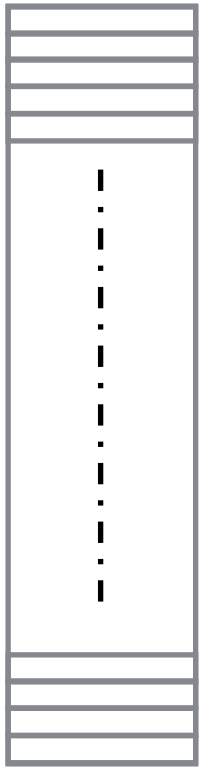


2^30 bytes

Virtual Memory

Pages are 512 bytes
We have 2^30/512 pages,
or 2^30/2^9 = 2^21
or 2,097,152 pages.

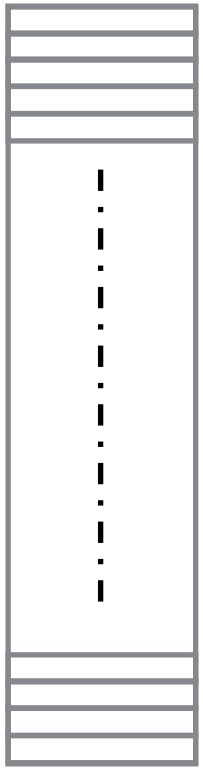
How many bits do we need for our offset if we have 512 byte pages?
Right, 9 bits: 2^9 = 512



2^30 bytes

Virtual Memory

So, if a page table fits into 1 page and each page is 512 bytes, how many 4 byte PTEs do we have in a page?

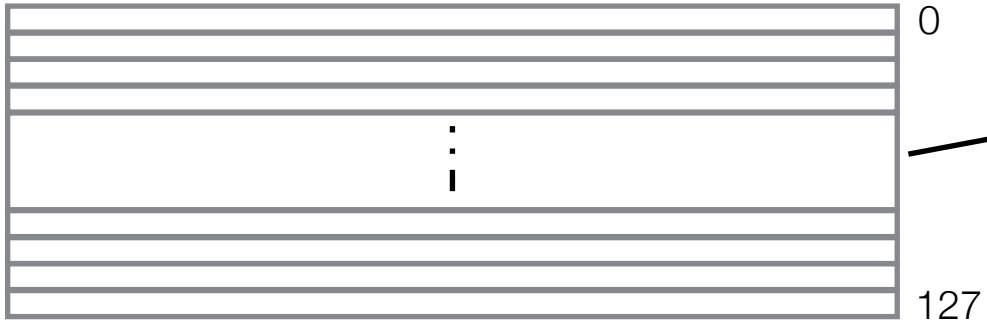


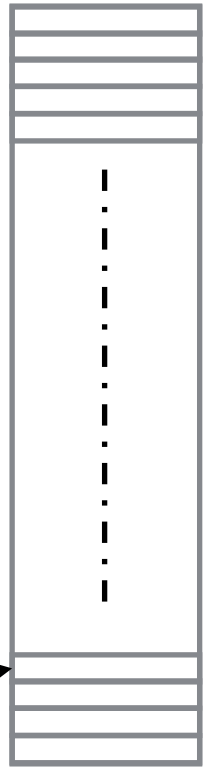
2^30 bytes

Virtual Memory

So, if a page table fits into 1 page and each page is 512 bytes, how many 4 byte PTEs do we have in a page?

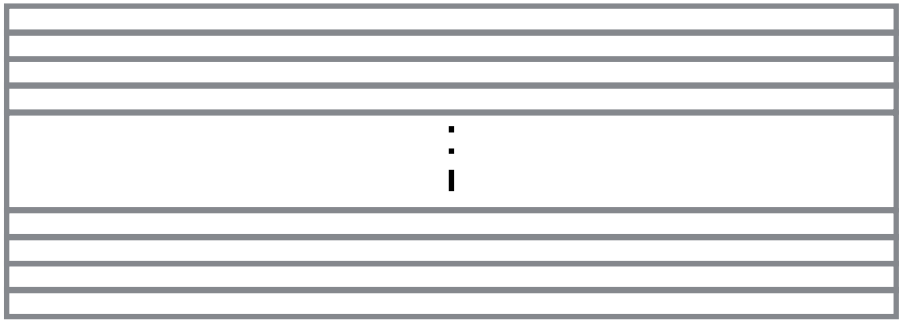
512/4 = 128 = 2^7, so 7 bits are needed for a page table index (PTI)

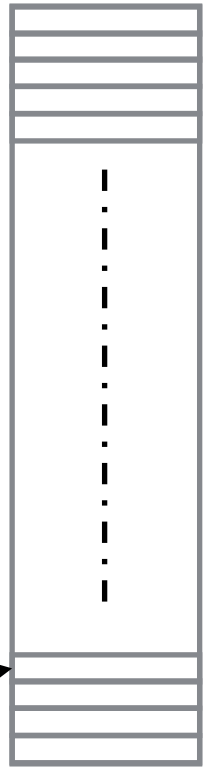




2^30 bytes

Ok, if each page table holds 128 PTEs then how many bits do we need to reference the Page Tables for 2,097,152 pages?



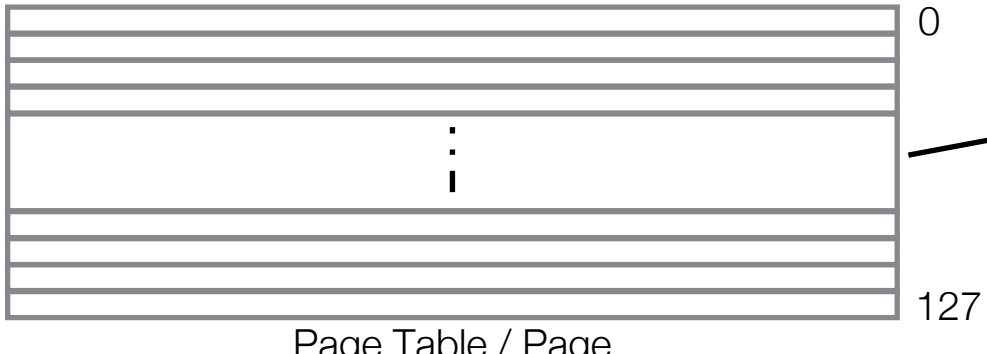


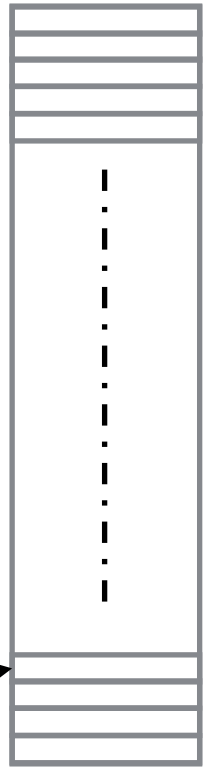
2^30 bytes

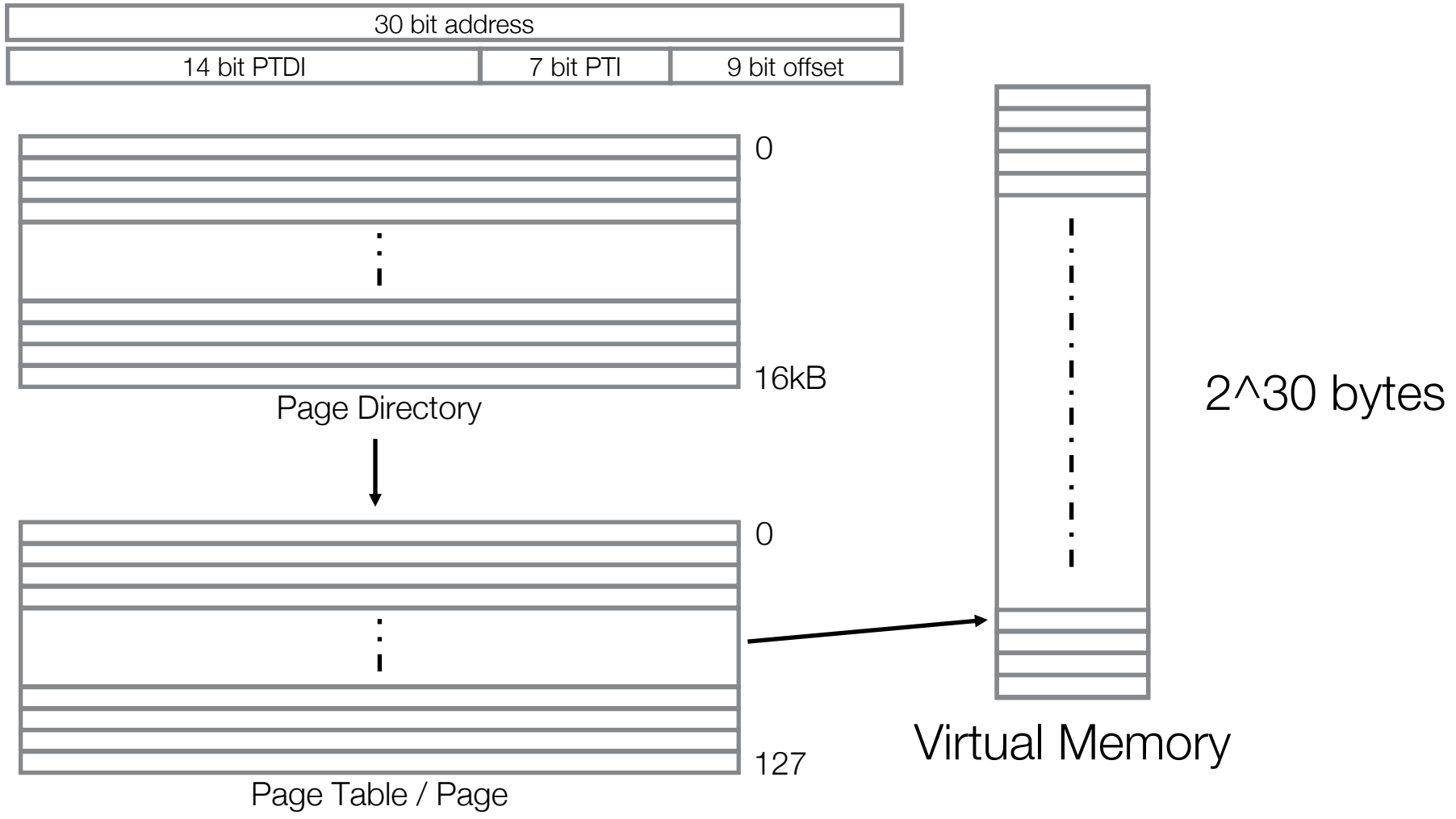
Virtual Memory

Ok, if each page table holds 128 PTEs then how many bits do we need to reference the Page Tables for 2,097,152 pages?

(2^30/512)/128 = 16,384 or 2^14
So, 14 bits



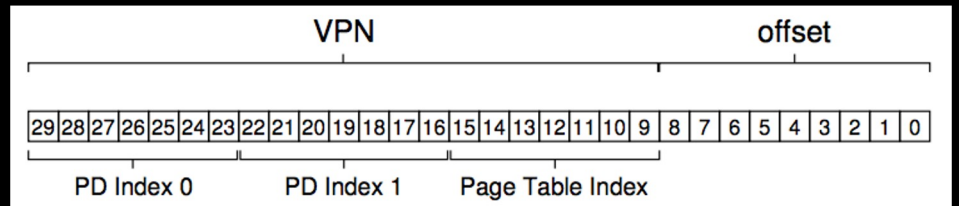



30 bit address
14 bit PTDI
7 bit PTI
9 bit offset
0
16kB
Page Directory
0
127
Page Table / Page
Virtual Memory
2^30 bytes

14 bits for the page table directory?

But if it is 14 bits, then the size of the page table directory is 2^14 = 16kB. This is way bigger than our page…

Add more levels! (2 Levels, 7 bits each)



Question?

If we have 32 bit addresses, a page size of 4kB, and 4 byte PTEs. We want page tables to fit in one page each. How many bits do we need for the page table directory, page table index, and offset?

(A)14, 7, 9

(B) 10, 10, 10

(C) 14, 8, 8

(D) 10, 10, 12

Question?

If we have 32 bit addresses, a page size of 4kB, and 4 byte PTEs. We want page tables to fit in one page each. How many bits do we need for the page table directory, page table index, and offset?

(A)14, 7, 9

(B) 10, 10, 10

(C) 14, 8, 8

(D) 10, 10, 12

2^32/2^12 = 2^20 pages

4kB (2^12) bytes/page, so offset is 12 bits.

4kB/4 bytes = 2^12/2^2 = 2^10, 10 bits PTI.

2^32 bytes/2^12 bytes /2^10 bytes = 2^10 PTD

ory	Page of PT (@PFN:100)			Page of P
d?	PFN	valid	prot	PFN va
	10	1	r-x	—
	23	1	r-x	—
	—	0	—	—
	—	0	—	—
	80	1	rw-	—
	59	1	rw-	—
	—	0	—	—
	—	0	—	—
	—	0	—	—
	—	0	—	—
	—	0	—	—
	—	0	—	—
	—	0	—	—
	—	0	—	—
	—	0	—	55
	—	0	—	45

Ok…what about 64 bits!

Yeah, we will cheat.

First, you don't need 64 bits (not yet). So we reduce the virtual address space to 48 bits

4kb page: 3 levels of page tables, 12 bits each, 12 bits for offset

Fine, but I am poor

All of this translation doesn’t create RAM out of thin air, all the virtual pages still need to be stored in physical RAM

And your processes actually want lots of virtual pages, and thus physical pages

More than you can afford.

But, I can't afford disk

~2021:

- **RAM:** ~$3 / GB
- **Disk:** ~1.5 cents/GB

So let's put some of our pages on disk

This area of the disk is called "swap space"

In each PTE we keep a bit for "present"

If the present bit is 0 during translation, then this causes a "page fault"

Question?

Who would raise this “page fault”?

(A) The CPU/MMU

(B) The user program

(C) The OS kernel

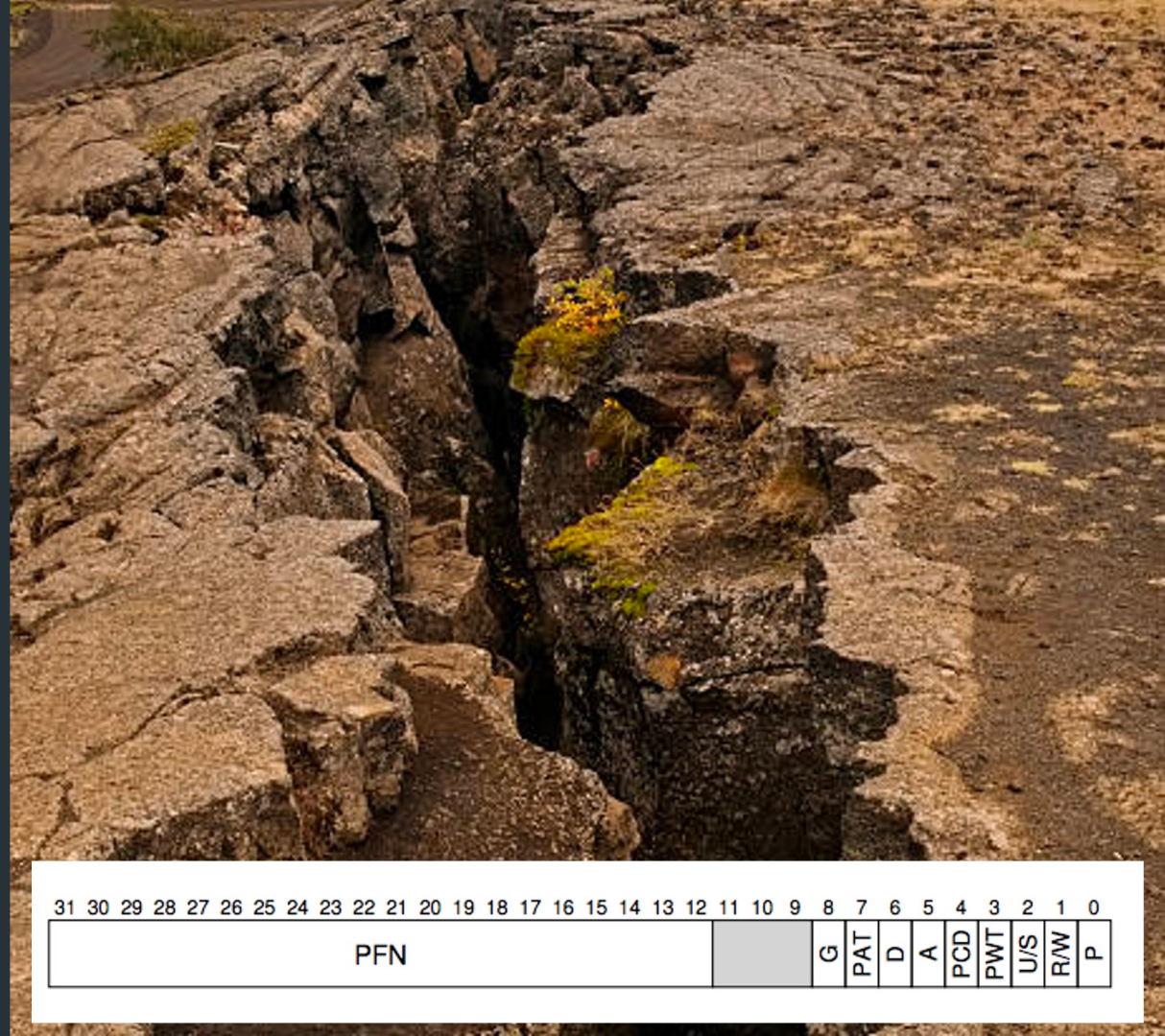
(D) The tubes

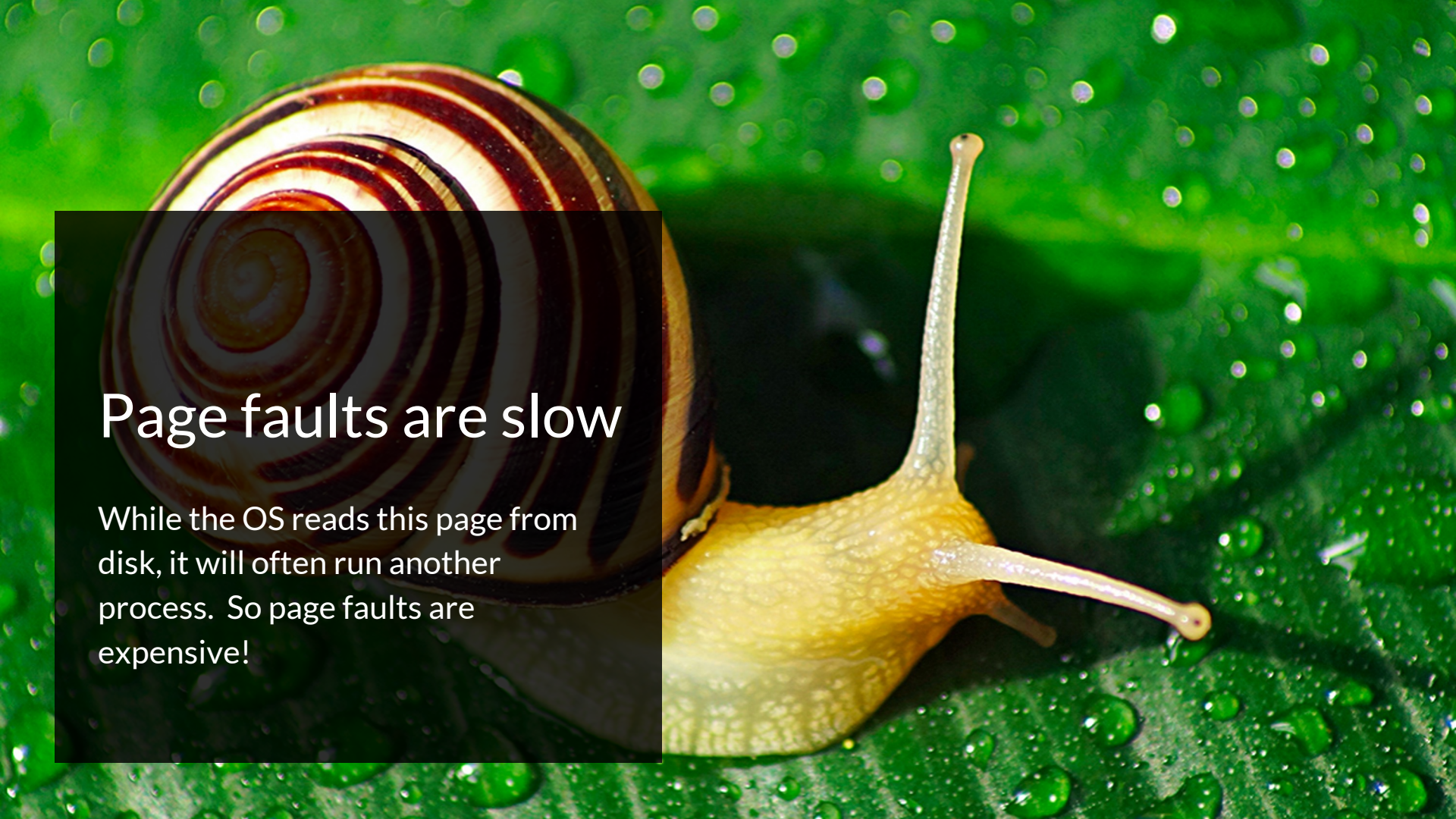
Page Fault

The page fault is an exception raised by the CPU which invokes the page fault handler of the OS

The OS then reads the page from disk into a physical page

Recall that the page table entry (~4 bytes..) contains the physical page number. But if it isn't present, it isn't in a physical page. So this number is usually reused as the place on disk





Page faults are slow

While the OS reads this page from disk, it will often run another process. So page faults are expensive!

What if memory if full?

Eventually we run out of physical pages.

What if memory if full?

When we read in a page from disk we may have to “evict” or “page out” a page

What if memory if full?

Which one to evict? The one you don’t need!


The End