Modular SGDMA Write Master Core

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Core Overview

The modular scatter-gather direct memory access (SGDMA) write master module is responsible for receiving data from an Avalon-Streaming (ST) port and writing the data to memory. The write master module is designed to be connected to the modular SGDMA dispatcher module but you can supply your own controller as well. The write master module is controlled by a ST command port and optional response data is sent via a ST response port.

There are various options that can be enabled to add functionality to the write master module. The write master module supports the following options:

- 8 to 1024 bit data width
- Up to 4 GB transfer lengths
- Unaligned accesses
- Burst transactions
- Stride addressing
- ST packet support
- ST error support
- Early termination support

Block Diagram

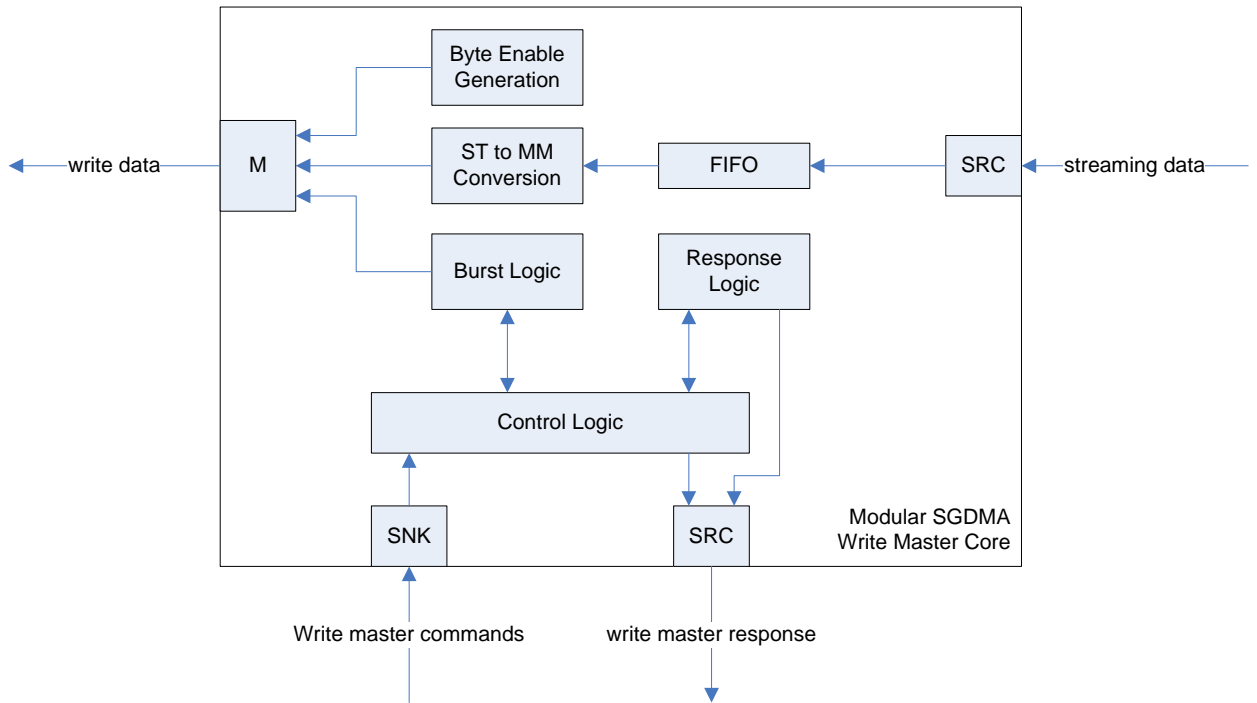Figure 1 shows the significant blocks that make up the write master core.

Figure 1. Modular SGDMA Write Master Core

Write Master Port Listing

This section will discuss the various Avalon-MM and ST ports that are exposed by the modular SGDMA write master module. Some of the signals that are exposed are optionally used by the dispatcher module depending on the transfer type.

Write Commands Sink Port

Bits	Signal Information
31-0	Write Address [31:0]
63-32	Length [31:0]
64	End on EOP
65	\<reserved\>
66	Stop[1]
67	Reset[1]
75-68	Write Burst Count [7:0]
91-76	Write Stride [15:0]
255-92	\<reserved\>

Table 1. Write Commands Sink Port Bitfields

[1] Combinational signals that don't obey flow control
[2] Reserved bits driven to ground

Write Response Source Port

Bits	Signal Information
31-0	Actual Bytes Transferred [31:0]
32	Reset Delayed[1]
33	Stop State[1]
41-34	Error [7:0]
42	Early Termination
43	Done Strobe
255-44	\<reserved\>

Table 2. Write Response Source Port Bitfields

[1] Combinational signals that don't obey flow control

Data Master Port

The data master port is responsible for writing data to memory buffered by the data streaming port. The data master port supports optional burst transactions. You are provided options for configuring the data width, burst length, and memory alignment. To learn more about the configuration options refer to the configuration options section of this document.

Data Sink Port

The data sink port is responsible for receiving data from the read master module or any component that contains a streaming source port. The port includes support for packets and errors. To learn more about the configuration options refer to the configuration options section of this document.

Configuration Options

The modular SGDMA has numerous configuration options to enable various functional units. Unnecessary functionality can be disabled to save resources and increase the frequency of the write master module. This section will discuss the various options for the write master module. Important to note are the options that require that the modular SGDMA dispatcher module to have the extended features support enabled.

Transfer Options

Parameter	Legal Values	Description
Data Width	8, 16, 32, 64, 128, 256, 512, 1024	Data width of the master and streaming ports.
Length Width	10-32	Transfer length in bytes. The transfer length is also used to limit the number of bytes sent during a packet transfer. If you do not wish to limit packet transfer lengths set this field to the maximum amount of `0xFFFFFFFF` and adjust the length width setting accordingly.
FIFO Depth	16, 32, 64, 128, 256, 512, 1024, 2048, 4096	The FIFO depth setting must be at least twice the maximum burst count setting. To maximize the read master module efficiency you should set the FIFO depth to be at least twice the maximum read latency of all the memories connected to the data master.
Stride Addressing Enable[1]	On/Off	Enable stride addressing if you want the read master module to perform fixed or non-sequential memory accesses. This feature is not supported when burst or unaligned accesses support is enabled.
Stride Width[1]	1-16	Stride width is specified in words. The following are examples of various stride addressing: 0 – Fixed read address 1 – Sequential read address 2 – Read every other word The stride width must be set to at least `floor(log2(maximum stride)) + 1`.
Burst Enable	On/Off	Enable burst support when you connect the read master module to burst capable slave ports.
Maximum Burst Count	2, 4, 8, 16, 32, 64, 128, 256, 512, 1024	The maximum burst count must be less than or equal to half of the FIFO depth setting.
Programmable Burst Enable[1]	On/Off	Programmable burst support allows you to program on a per descriptor basis a burst count of 1, 2, 4, 8, 16, 32, 64, or 128. The burst count that is programmed must be less than or equal to the maximum burst count.
Force Burst Alignment Enable	On/Off	When connecting the read master module to burst wrapping slave ports (SDRAM) you must enable this setting. This setting will force the master to post single beat burst transactions until the next burst boundary has been reached to avoid memory corruption.

Parameter	Legal Values	Description
Programmable Burst Enable[1]	On/Off	Programmable burst support allows you to program on a per descriptor basis a burst count of 1, 2, 4, 8, 16, 32, 64, or 128. The burst count that is programmed must be less than or equal to the maximum burst count.
Force Burst Alignment Enable	On/Off	When connecting the read master module to burst wrapping slave ports (SDRAM) you must enable this setting. This setting will force the master to post single beat burst transactions until the next burst boundary has been reached to avoid memory corruption.

Table 3. Transfer Options

[1] Modular SGDMA dispatcher module must have extended features enabled

Memory Access Options

Parameter	Legal Values	Description
Full Word Accesses Only	On/Off	When full word accesses only is enabled you must provide a read address that is aligned. You must also provide a transfer length is that is a multiple of the data width. This memory access mode results in the smallest hardware footprint and highest frequency.
Aligned Accesses	On/Off	When aligned accesses is enabled you must provide a read address that is aligned. You can provide any transfer length.
Unaligned Accesses	On/Off	When unaligned accesses is enabled you can provide any read address or transfer length. This memory access mode results in the largest hardware footprint and lowest frequency.

Table 4. Memory Access Options

Streaming Options

Parameter	Legal Values	Description
Packet Support Enable	On/Off	When packet support is enabled the data streaming port will include the start of packet (SOP), end of packet (EOP), and empty signals.
Error Enable	On/Off	When error support is enabled the data streaming port will include the error signal.
Error Width	1-8	This setting will adjust the width of the error signal. The error width must be set to at least `floor(log2(maximum error)) + 1`.

Table 5. Streaming Options