CE203/SC301 Tutorial 3: Computerised Data Acquisition

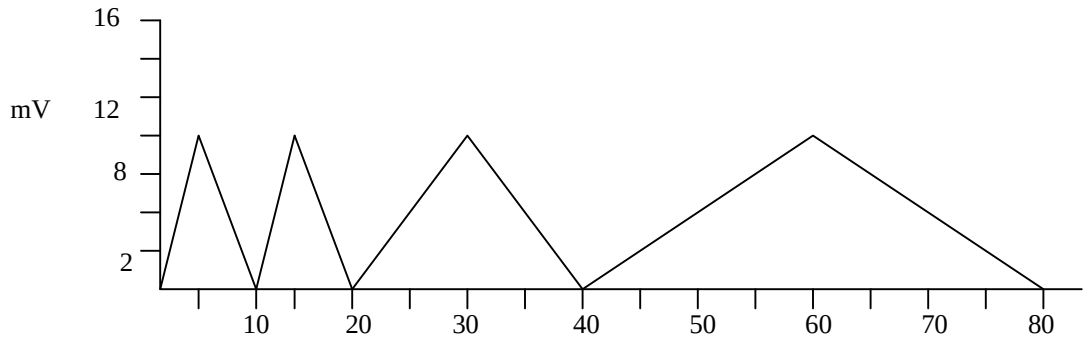

Figure Q1

1. Figure Q1 shows a signal to be sampled. The Y-axis is the signal voltage in mV and the X-axis is the time in milliseconds.

   (a) Identify the waveform components present in the signal, hence, calculate their signal frequencies.

   (b) What is the lowest theoretical sampling frequency usable in order to sample the signal such that no signal aliasing occurs?

   (c) Carefully draw the signal on a graph paper. Construct the sampled signal at the following sampling points: {0, 20, 40, 60, 80 ms} What is the sampling frequency used? Use linear interpolation to join the sampled points.

   (d) Construct the sampled signals at the following sampling points, Determine the sampling frequencies used in each case:
   (i) {0, 10, 20, 30, 40, …., 80 ms}
   (ii) {0, 5, 10, 15, 20, …..., 80 ms}
   (iii) {0, 2.5, 5, 7.5, 10, …, 80 ms}

   (e) Contrast the 4 reconstructed sampled signals. Is there any signal aliasing? Compare the calculated sampling frequencies with that in Q(1b).

   (f) Repeat the sampling at {2.5, 7.5, 12.5, 17.5ms …} at 5ms intervals. Compare the recontructed sampled signal against the four. Can the 100Hz signal be recovered?

2. Recommend the most suitable ADC type for the following computerised data acquisition applications. In the absence of actual product data sheet, there may not be a definite answer.

   (a) In the study into an improved spark plug for an internal combustion engine used in automobiles, the research engineers find that they need to acquire the rapid pressure profile within the combustion cylinder. Subtle pressure changes in the range of 10-20μs are of interest.

   (b) In a hi-tech durian farm producing D2 high-yield durian fruit, the chief agricultural scientist conjectured that the premium grade durian were highly sensitive to the level of the PH value in the soil. In general, soil PH level is a very slowly changing parameter unless chemical is used.

   (c) In order to ensure the structural safety for the container cranes in the Singapore Port. The chief port engineer is interested in a system which can monitor the structural stress level in the crane. Strain gauges are used as stress sensors. These sensors are to be read at 5 mins interval. In a preliminary study, it is found that the signals generated by the strain gauges are corrupted by high frequency noise from a nearby switching station.

3. Vibration in a motor is monitored for observation using the following measurement and data acquisition system shown in Figure 3. The vibration sensor produces a peak voltage of 3V with a frequency range from DC level to 600Hz. Noise is present and is dominated by a 2.4KHz noise signal with a peak voltage of 0.2V.

   (a) Given that the signal to noise ratio of the system must be at least 65db, specify the type and the order of the filter needed to condition the signal by attenuating the noise.
   (b) How many bit must the ADC have?
   (c) Suppose that the ADC chosen has a conversion time of 5μs, analyse if a SHA is needed in order that the conversion accuracy is not less than 0.5LSB.
   (d) Determine the range of sampling frequencies usable for this system.

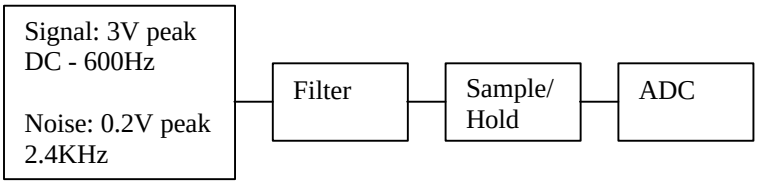

Figure Q3

4. A four channels data acquisition system is to be designed. The channels are to be sampled as simultaneously as possible so that phase relationship between channels is maintained to a high degree. A microcontroller (MCU) with seven built-in ports is avaliable. The machine cycle of the MCU is 1s and most instructions (sg move to port and counter increment) are executed in a single cycle. Some of the two cycle instructions are: moving data to external RAM, and subroutine branching. Two of the ports (port 0 & 1) are reserved for memory circuit; the others are free. In port 2, the input pins can also function as interrupt pins. Interrupt signals are received and acted on within one cycle.

   ADC:
   The ADC available is a 8-bit successive approximation, **50μs**, converter. It starts conversion on receiving a rising edge at its **SC** pin. When data conversion is done, it output a 3μs pulse on its **DR** pin.

   S/H and AMUX:
   The sample and hold amplifier (SHA) takes **2μs** to sample (wrt a sample signal) and settles within 0.4s on receiving a hold signal. One-of-four analogue multiplexer (AMUX) with **880ns** channel switching time is available.

   The final system should be able to acquire signals up to a maximum of **3000Hz** without signal aliasing.

   (a) Design the data acquisition system based on the devices available.
   (b) Design the firmware at pseudo-code or flow-chart level. The design should show the sequence of execution so that subsequent timing analysis can be performed/
   (c) Show the timing relationship of the key signales in the system.
   (d) Determine the throughput of the system. Hence, specify the theoretical maximum inout signal frequency so that signal aliasing will not occur. What is the most likely practical restriction on the input frequency.