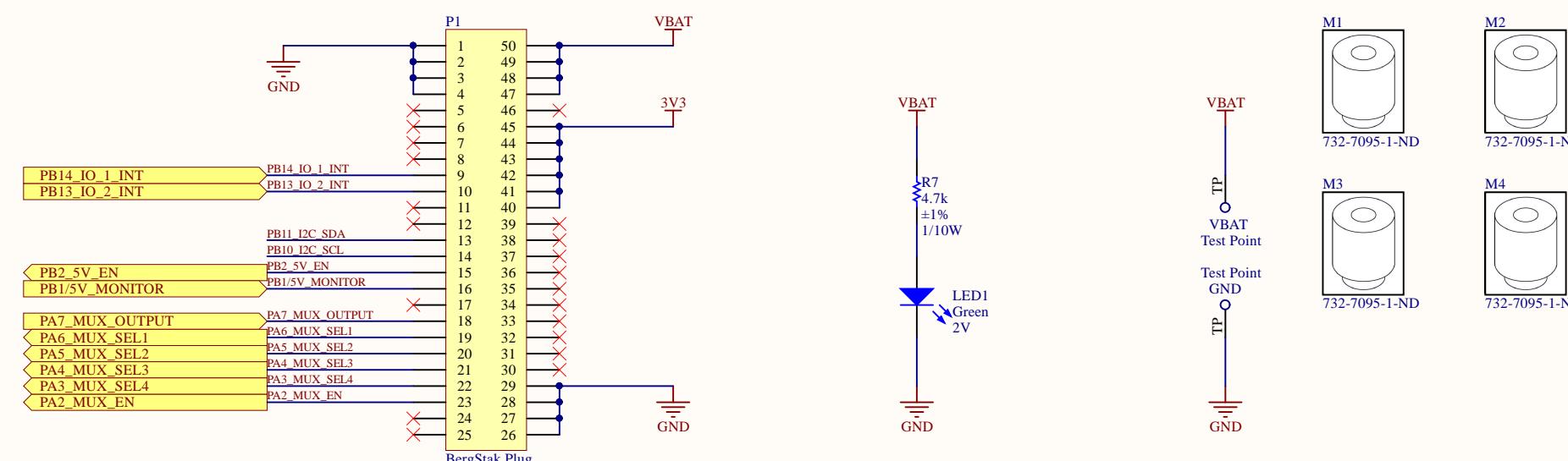
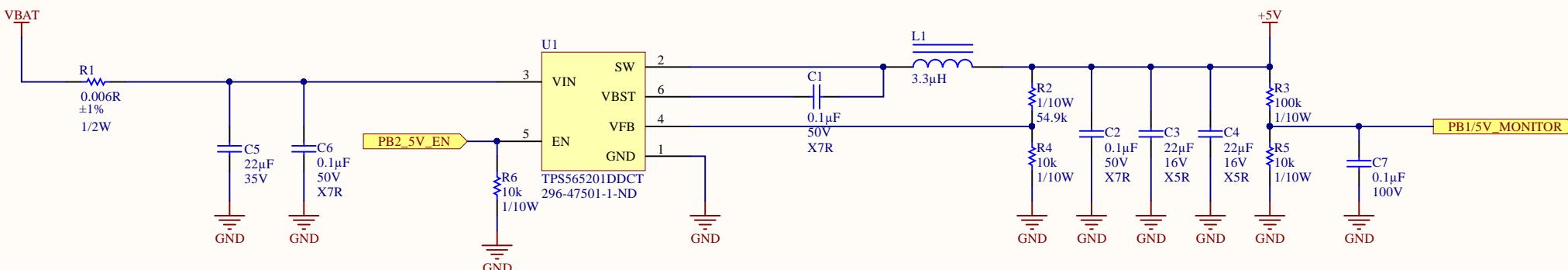
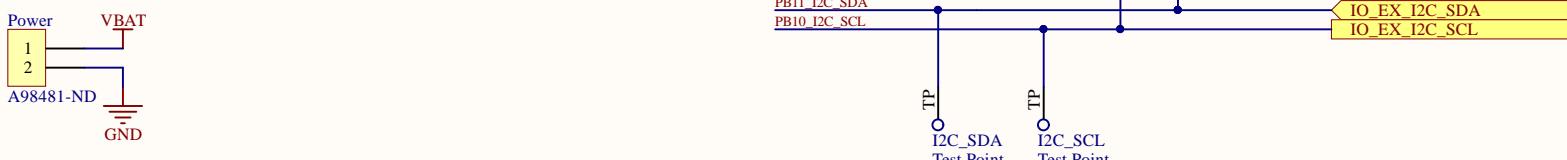


Regulator



12V Power Connector



PROJECT MSXIV_Front_Power_Distribution.PnjPcb

DOCUMENT Controller Board Interface

PART NUMBER

VARIANT [No Variations]

DRAWN BY

REVISION

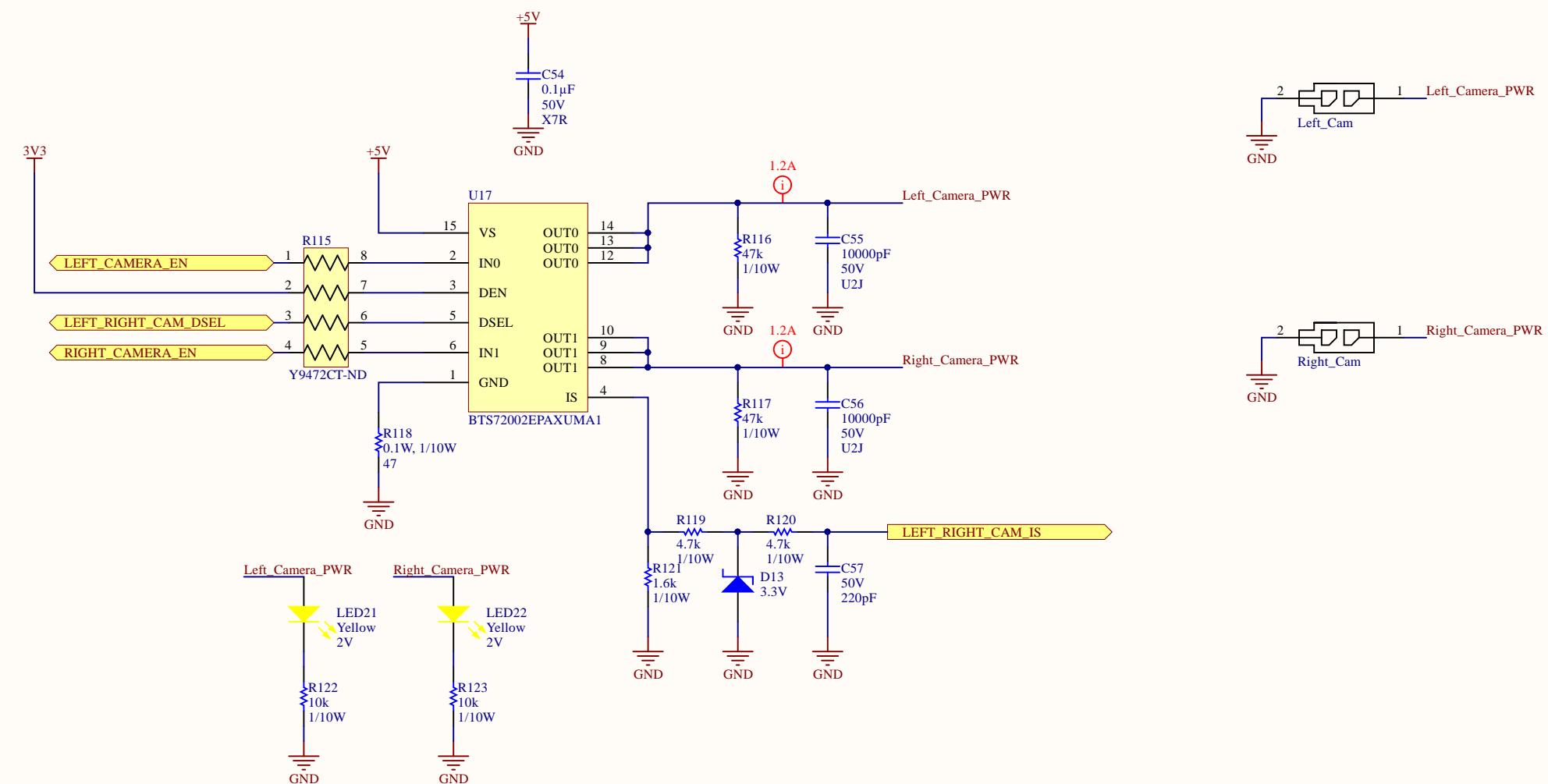
LAST MODIFIED 2020-02-26

SHEET * OF *

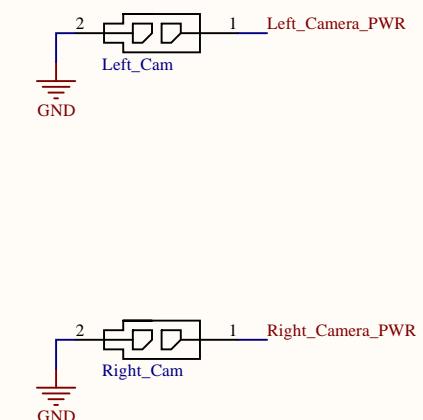


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hardware@uwmidsun.com

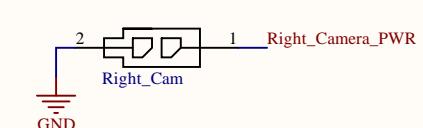
A



B



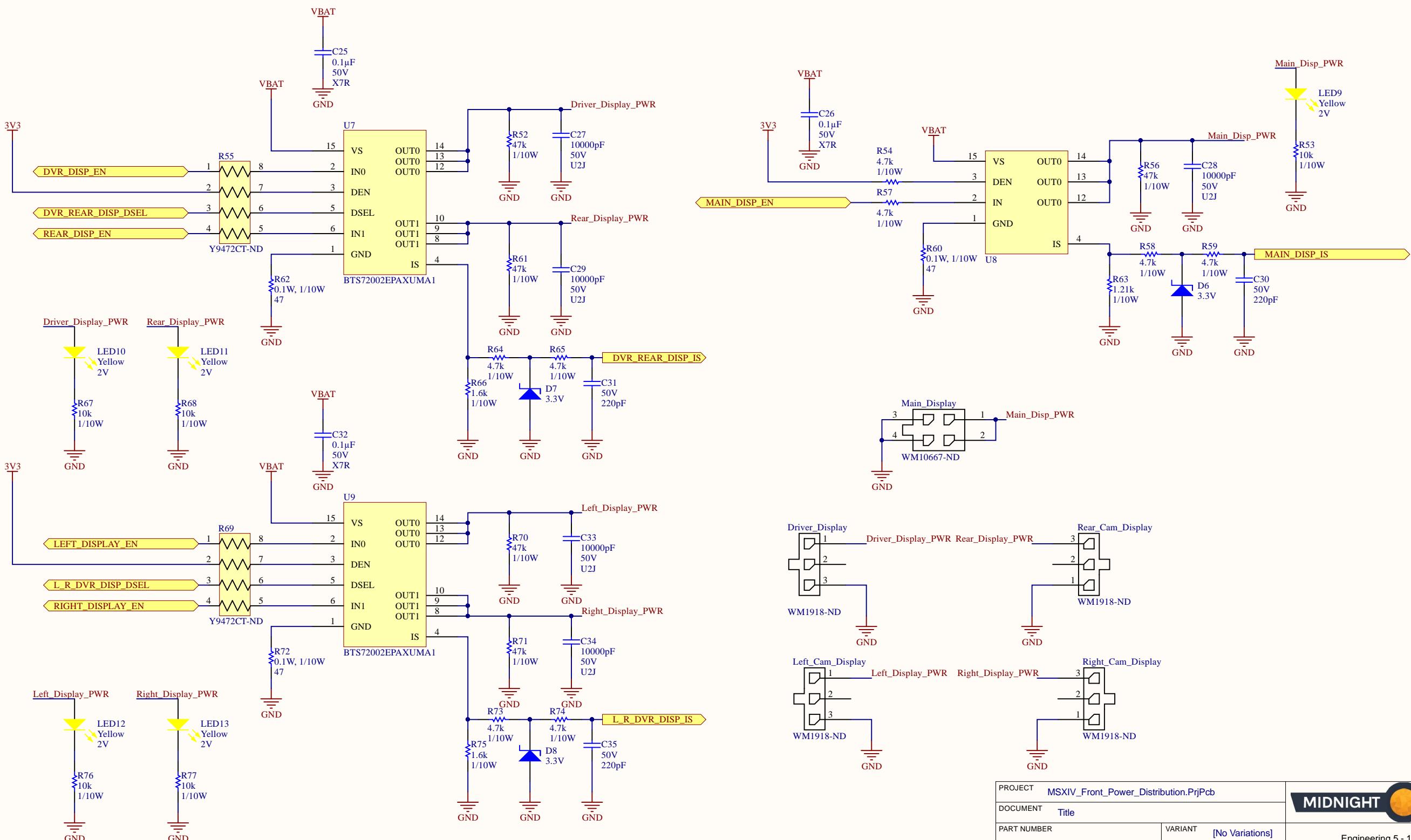
C



D

PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-26	SHEET * OF *

A



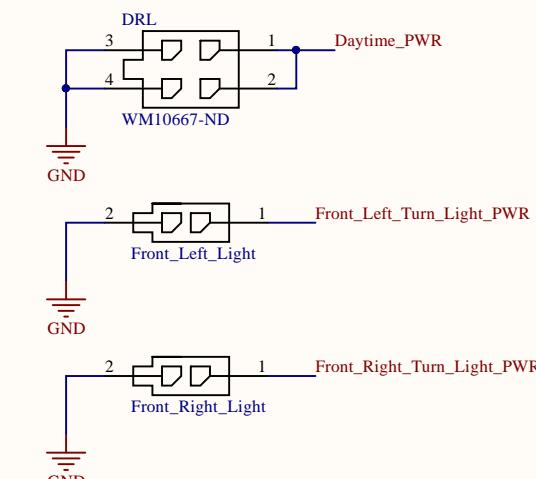
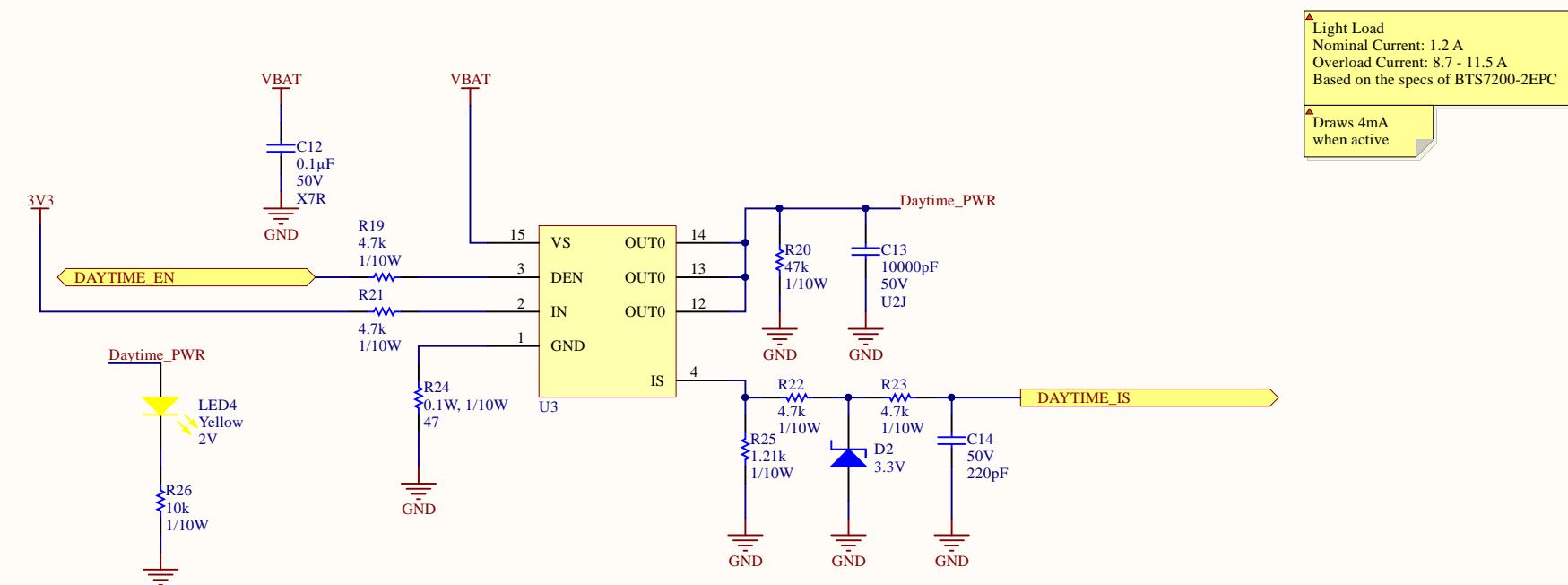
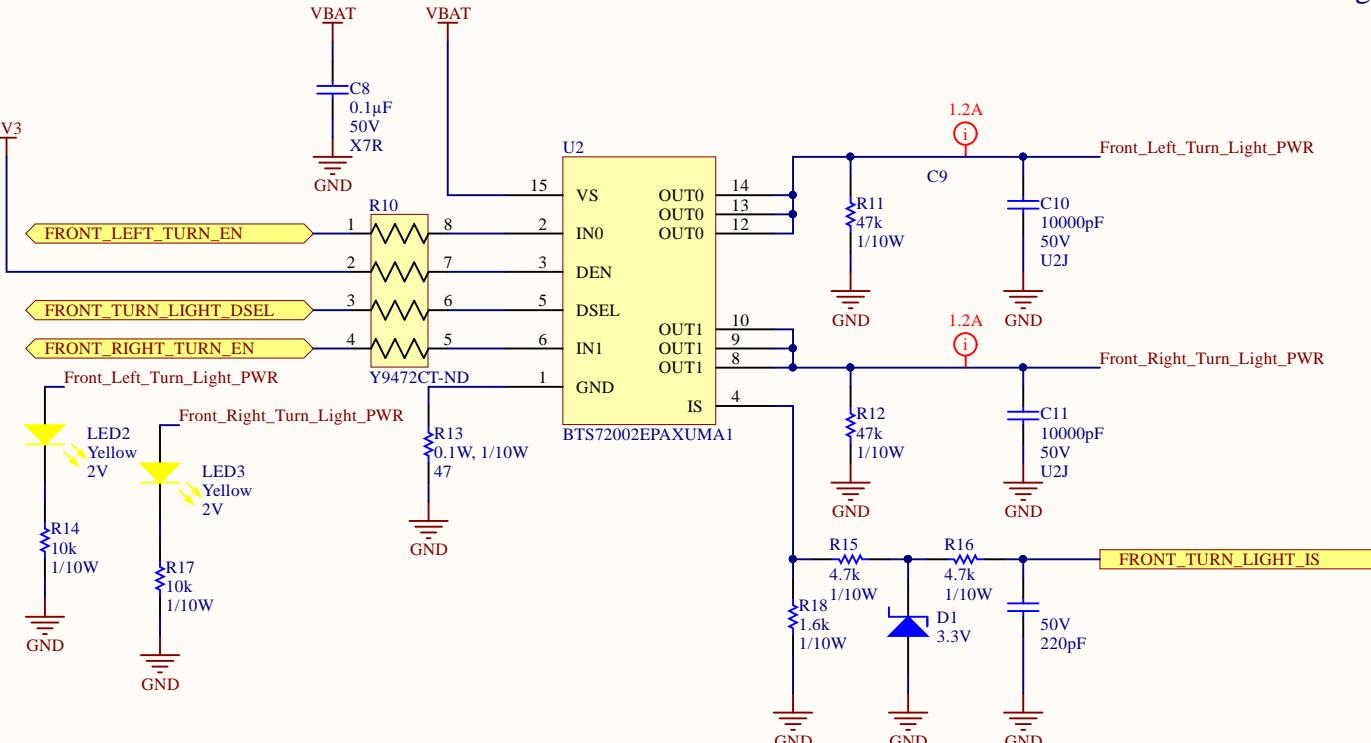
A

B

C

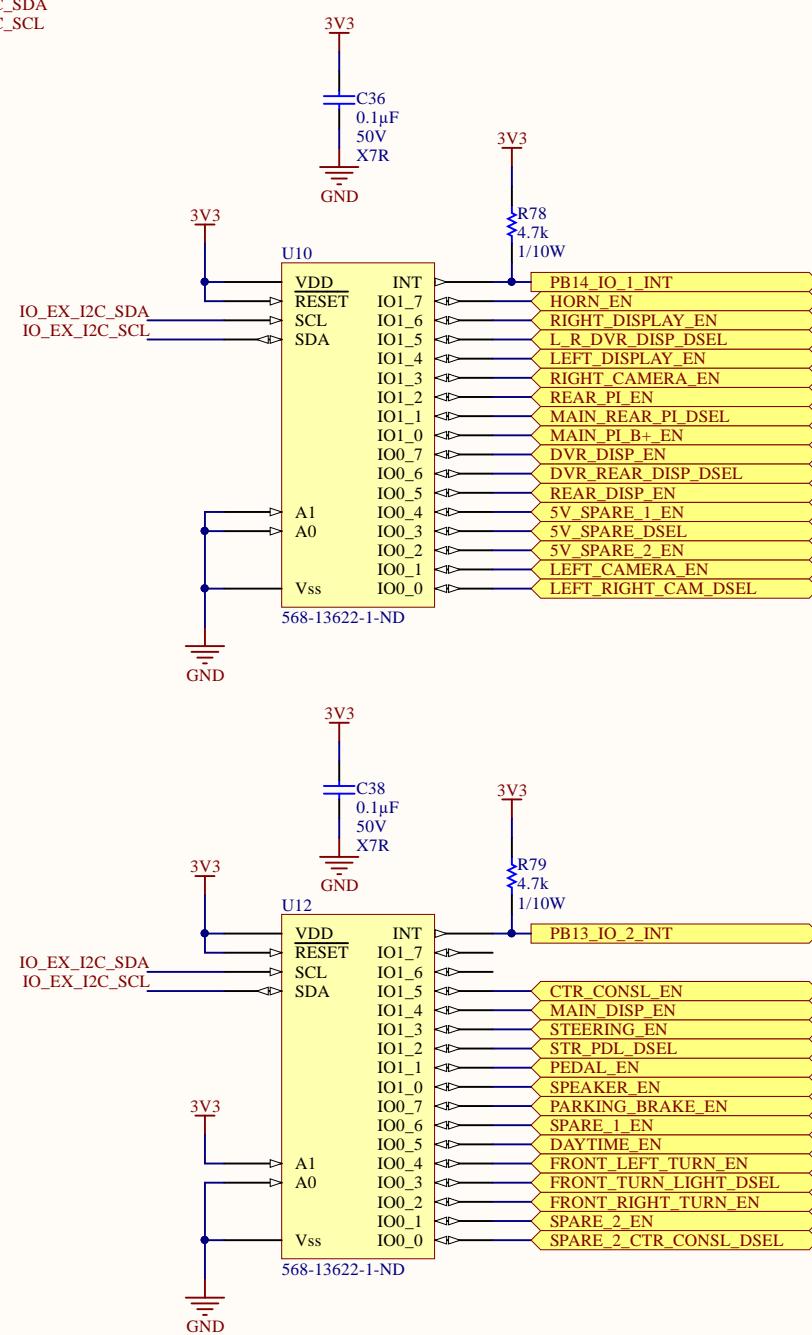
D

Front light



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
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IO_EX_I2C_SDA
IO_EX_I2C_SCL



PROJECT MSXIV_Front_Power_Distribution.PrjPcb

DOCUMENT Title

PART NUMBER VARIANT [No Variations]

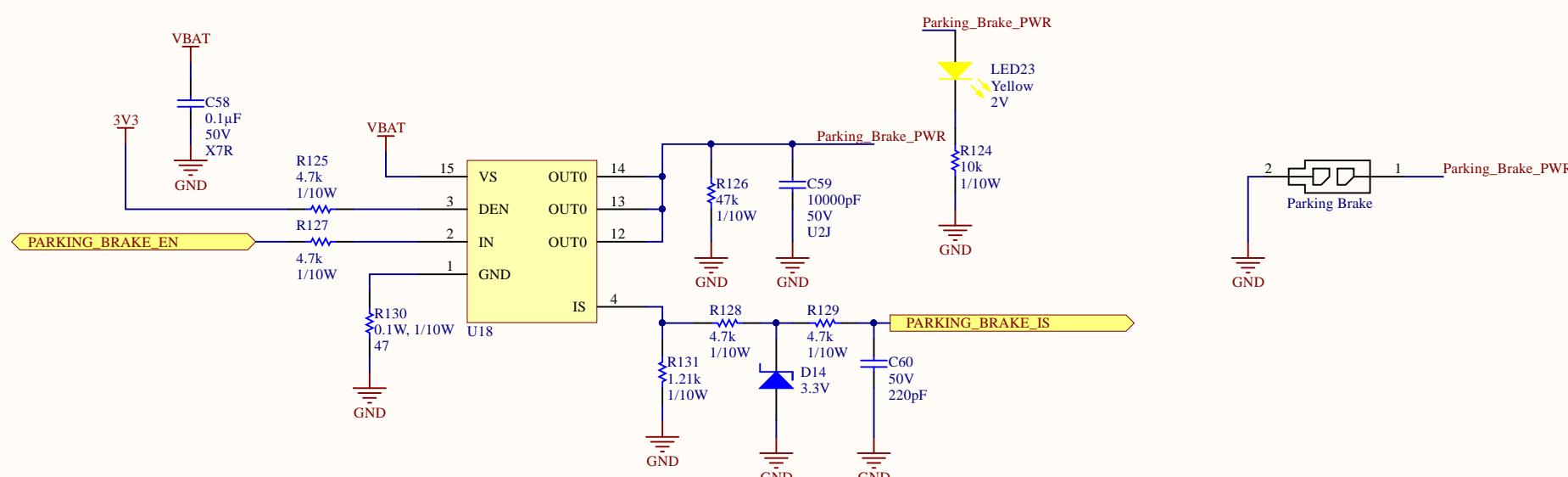
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A



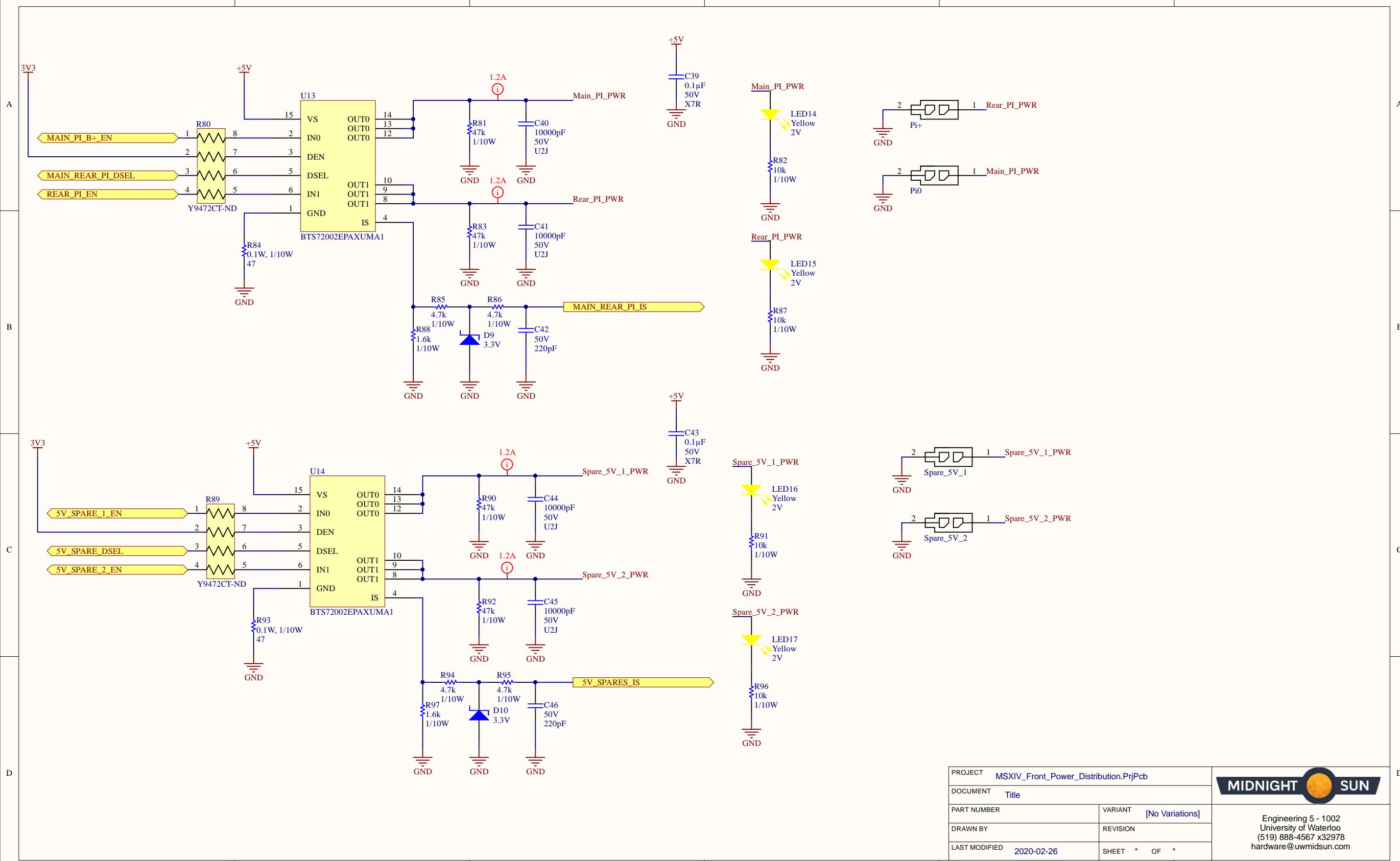
B

C

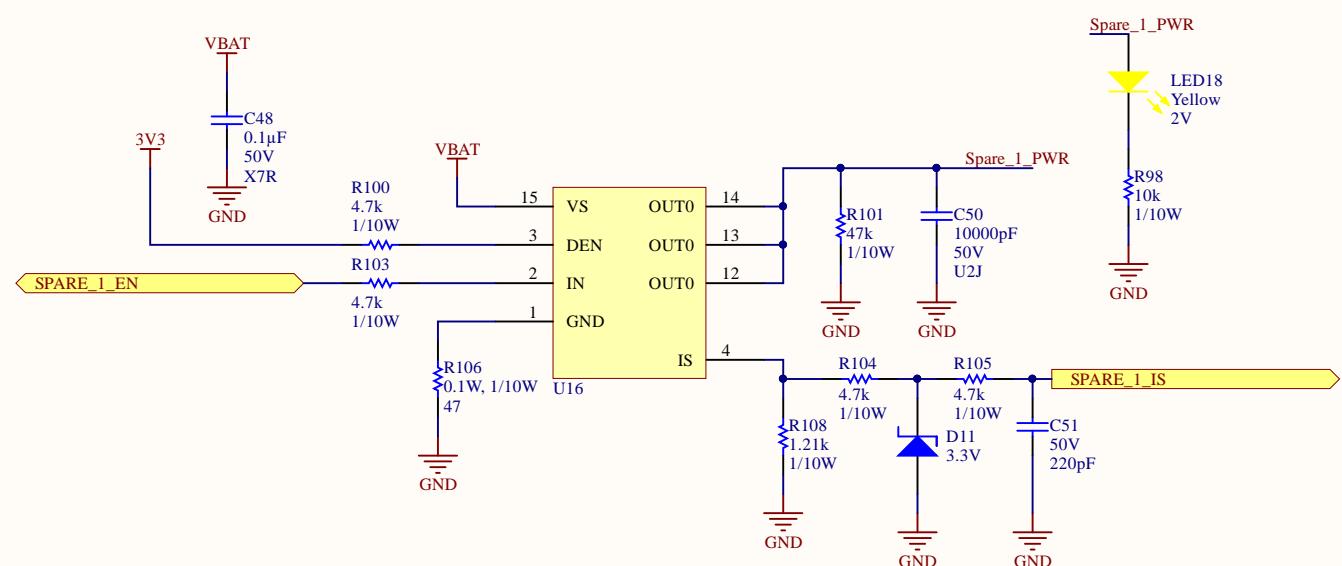
D

PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-26	SHEET * OF *

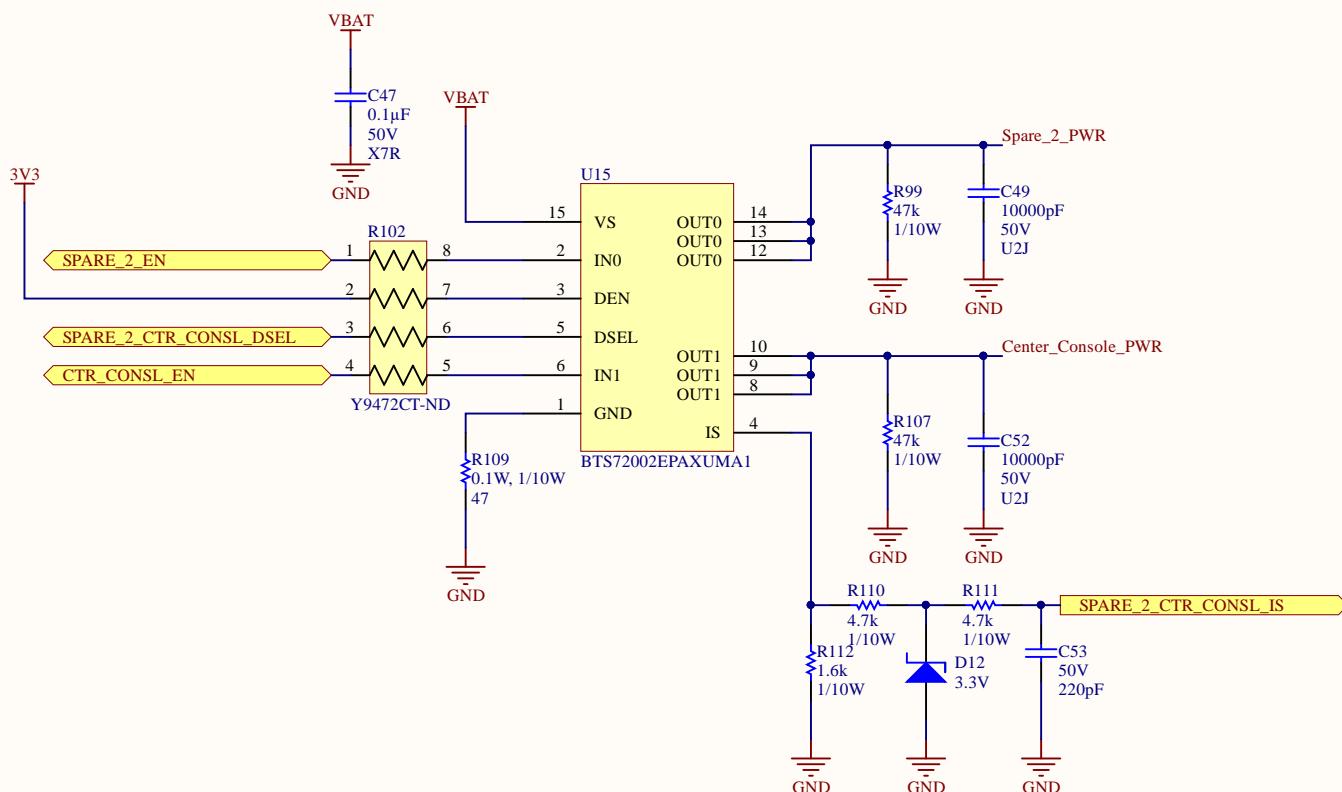
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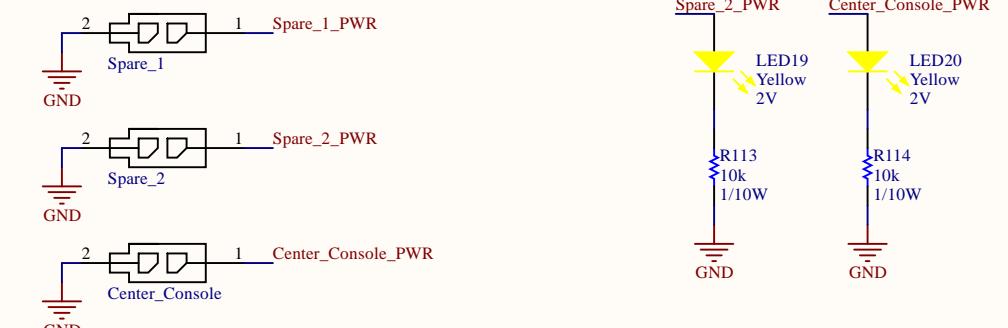
A



B



C



PROJECT MSXIV_Front_Power_Distribution.PrjPcb

DOCUMENT Title

PART NUMBER

VARIANT [No Variations]

DRAWN BY

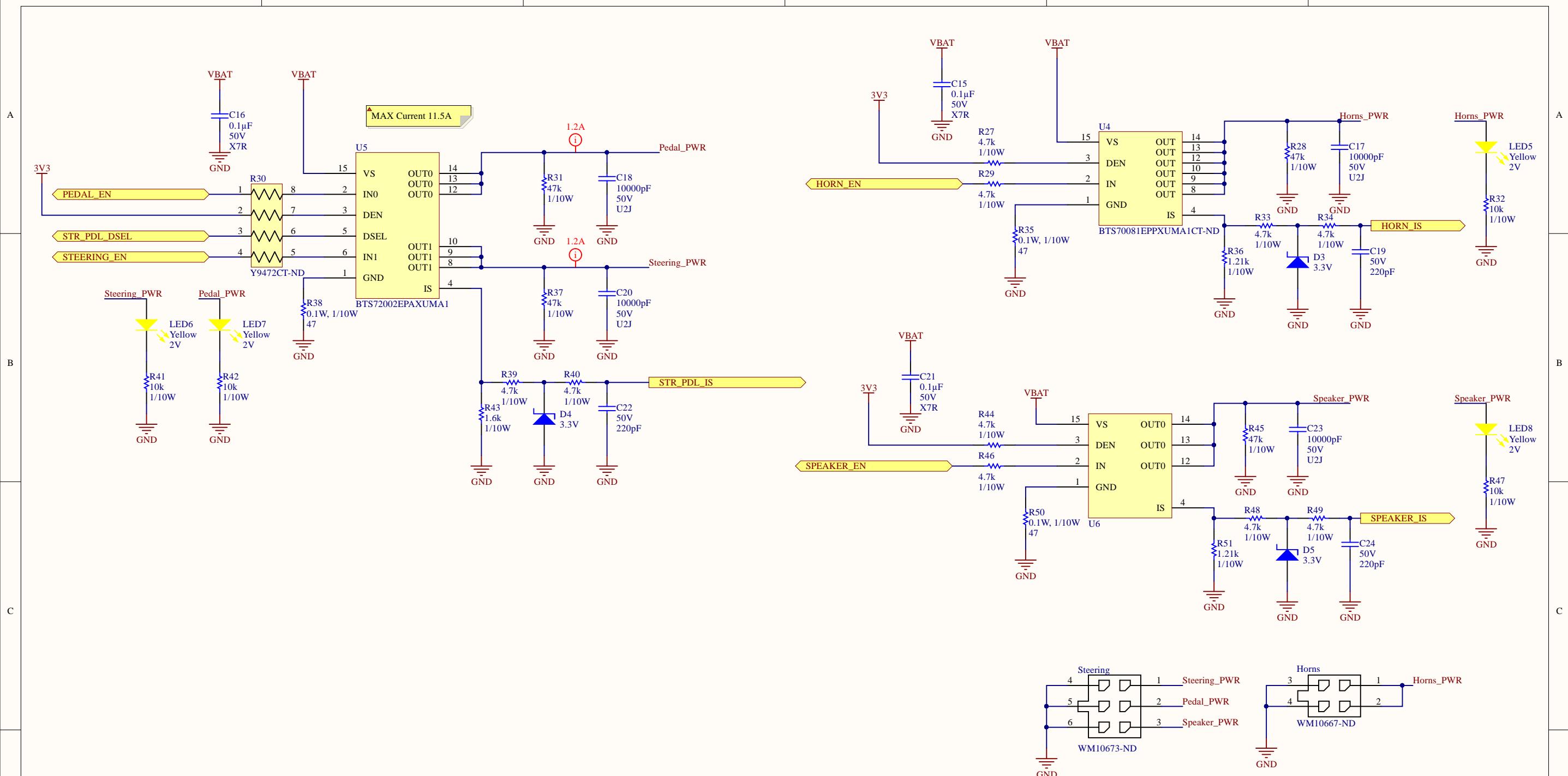
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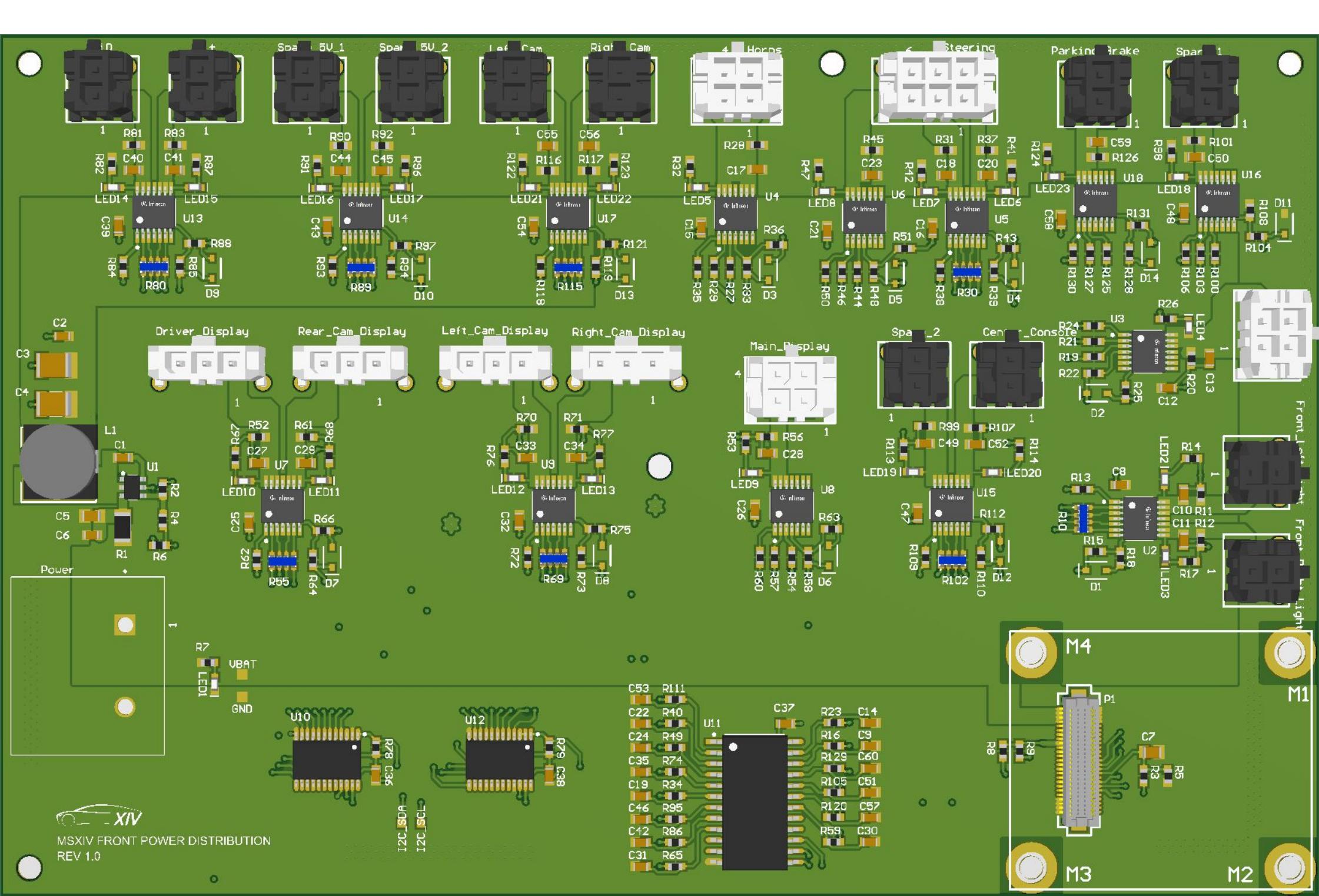
LAST MODIFIED 2020-02-26

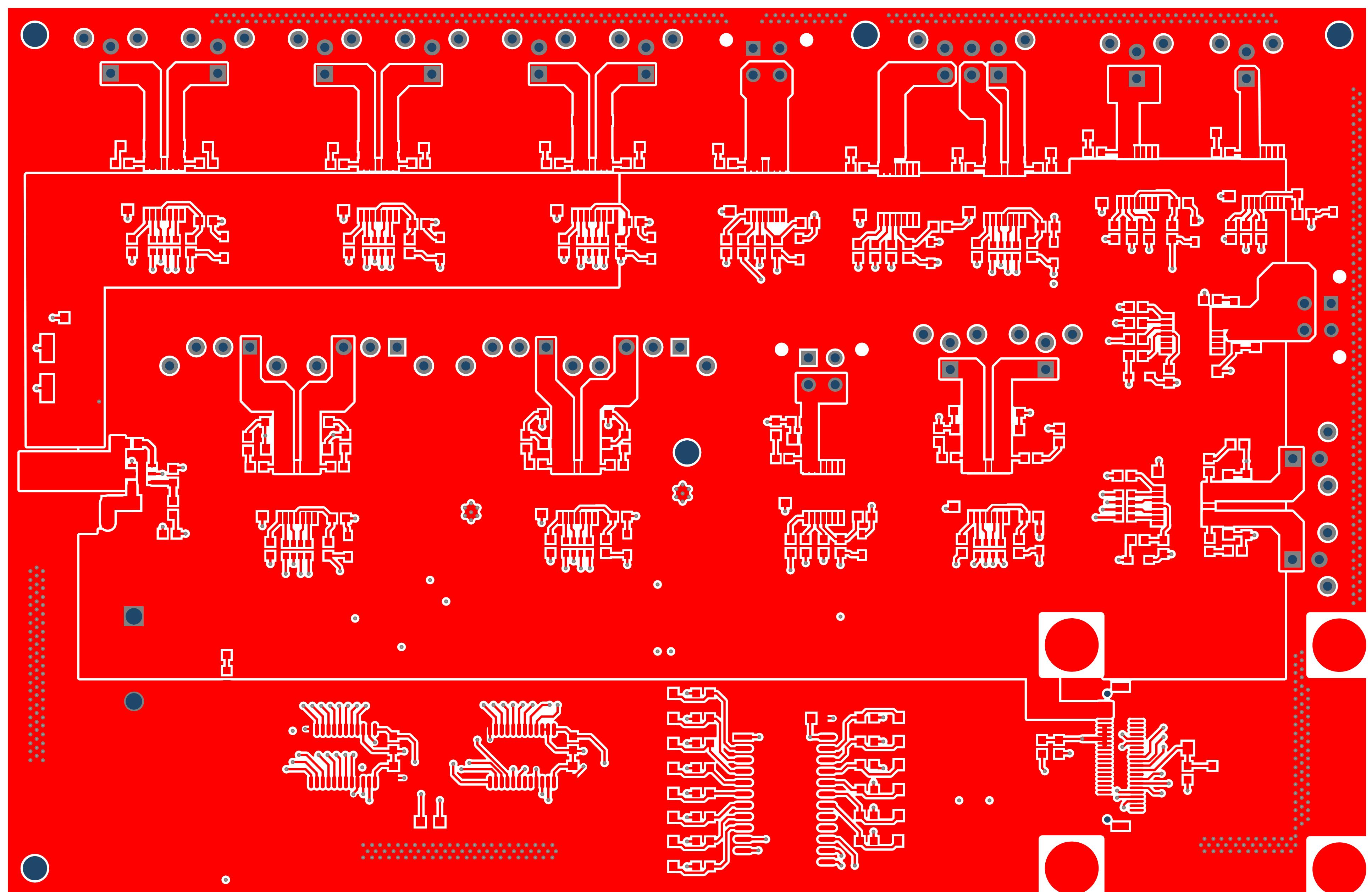
SHEET * OF *

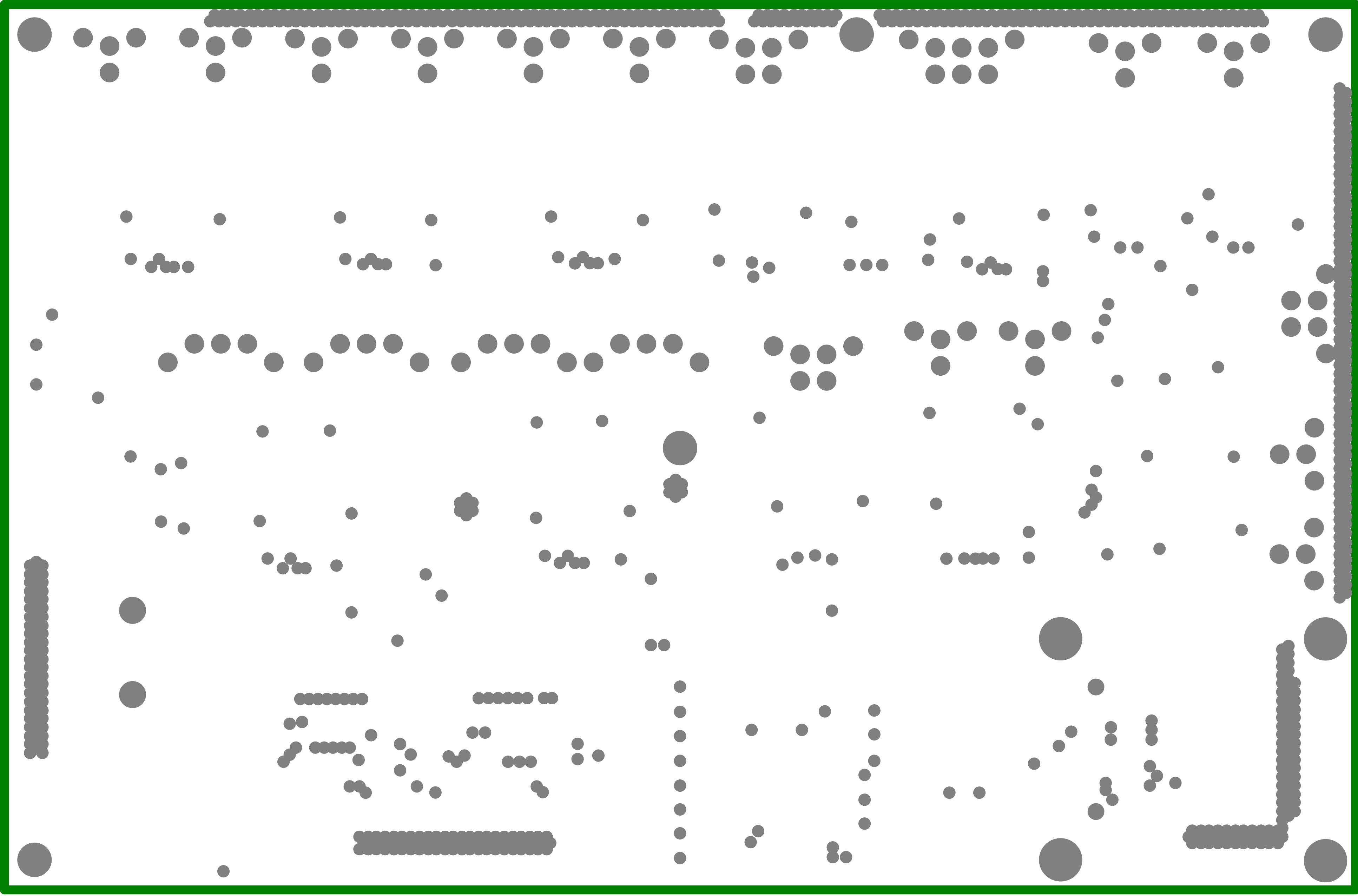
MIDNIGHT SUN

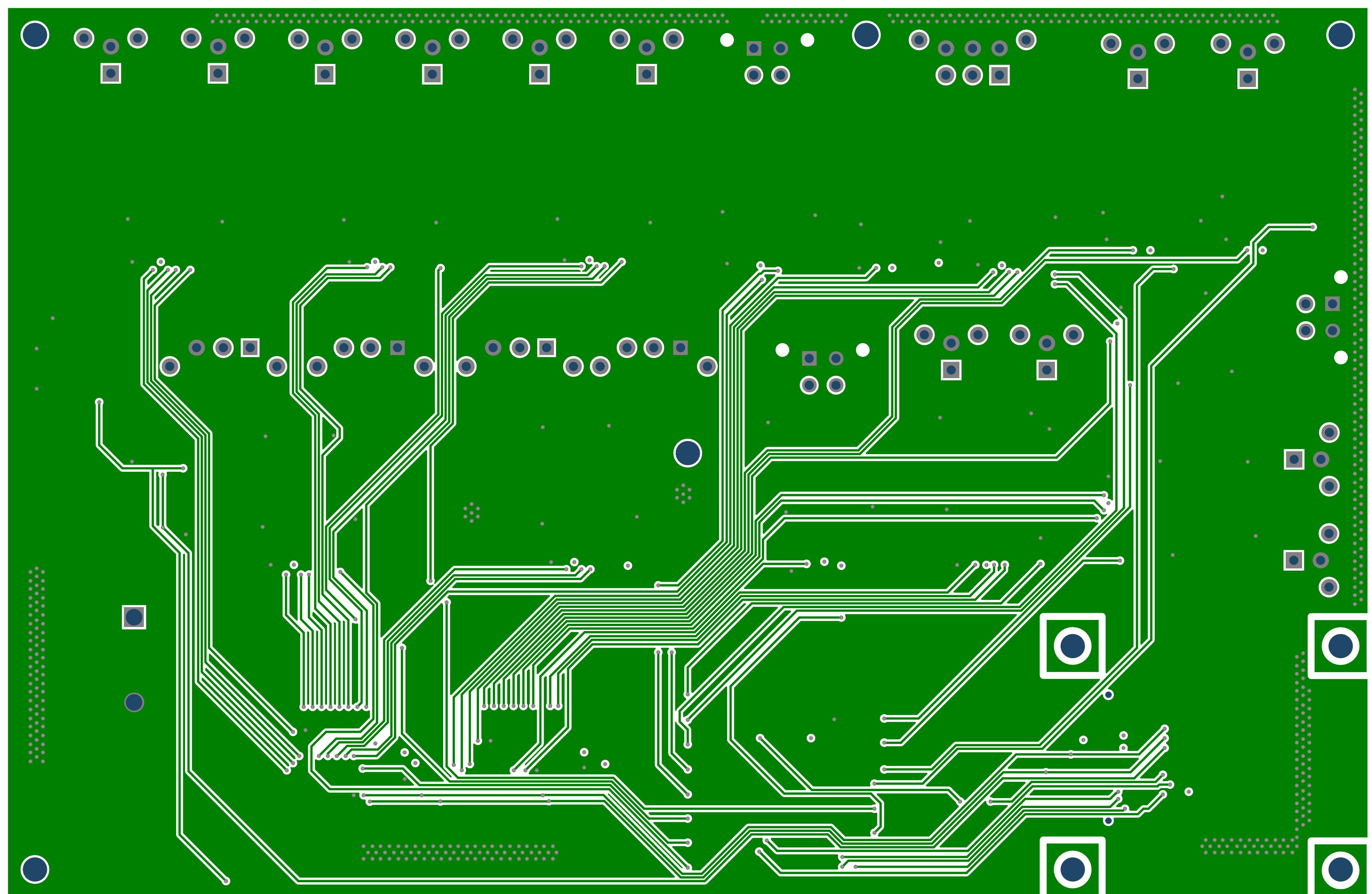
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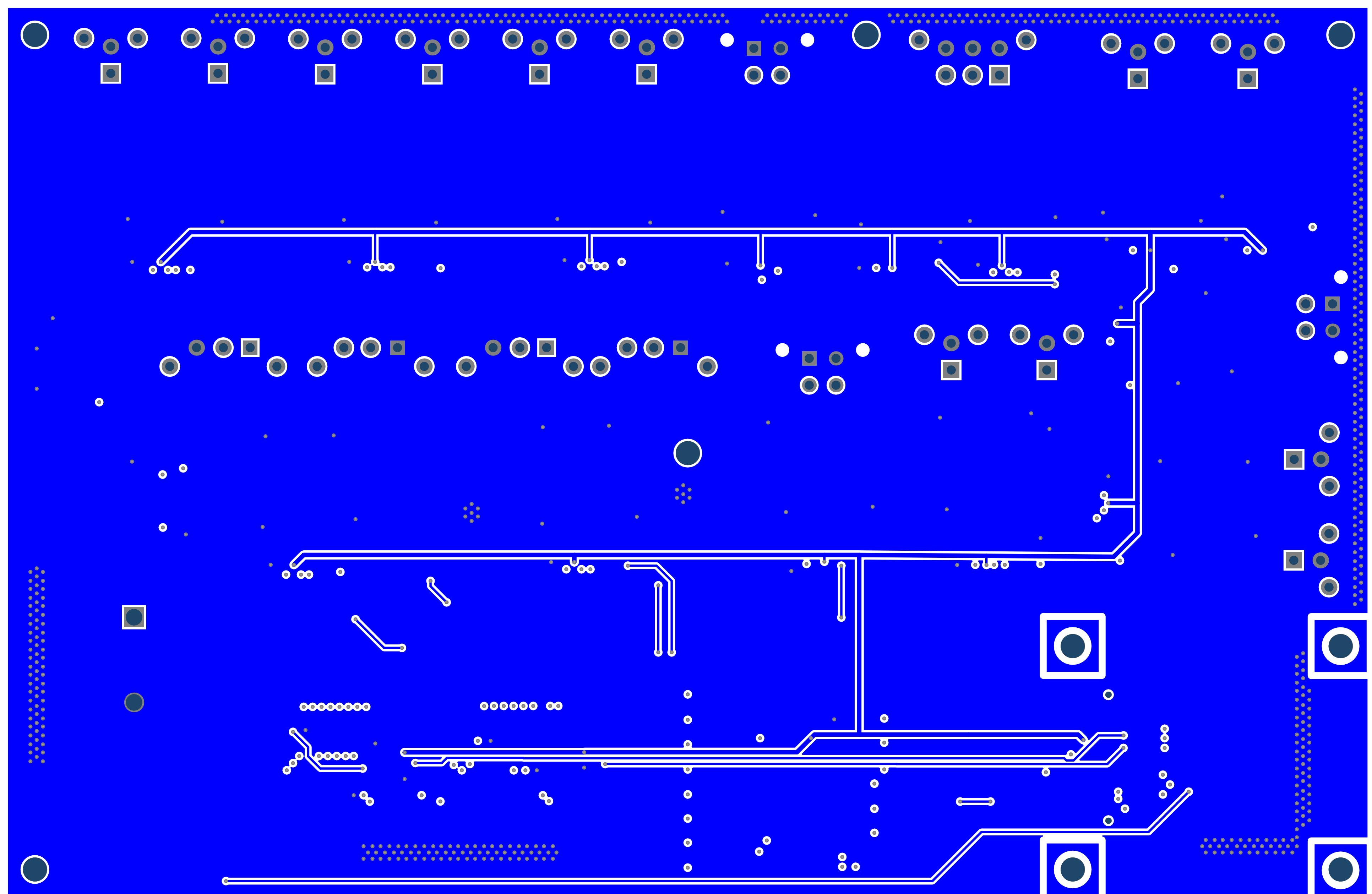


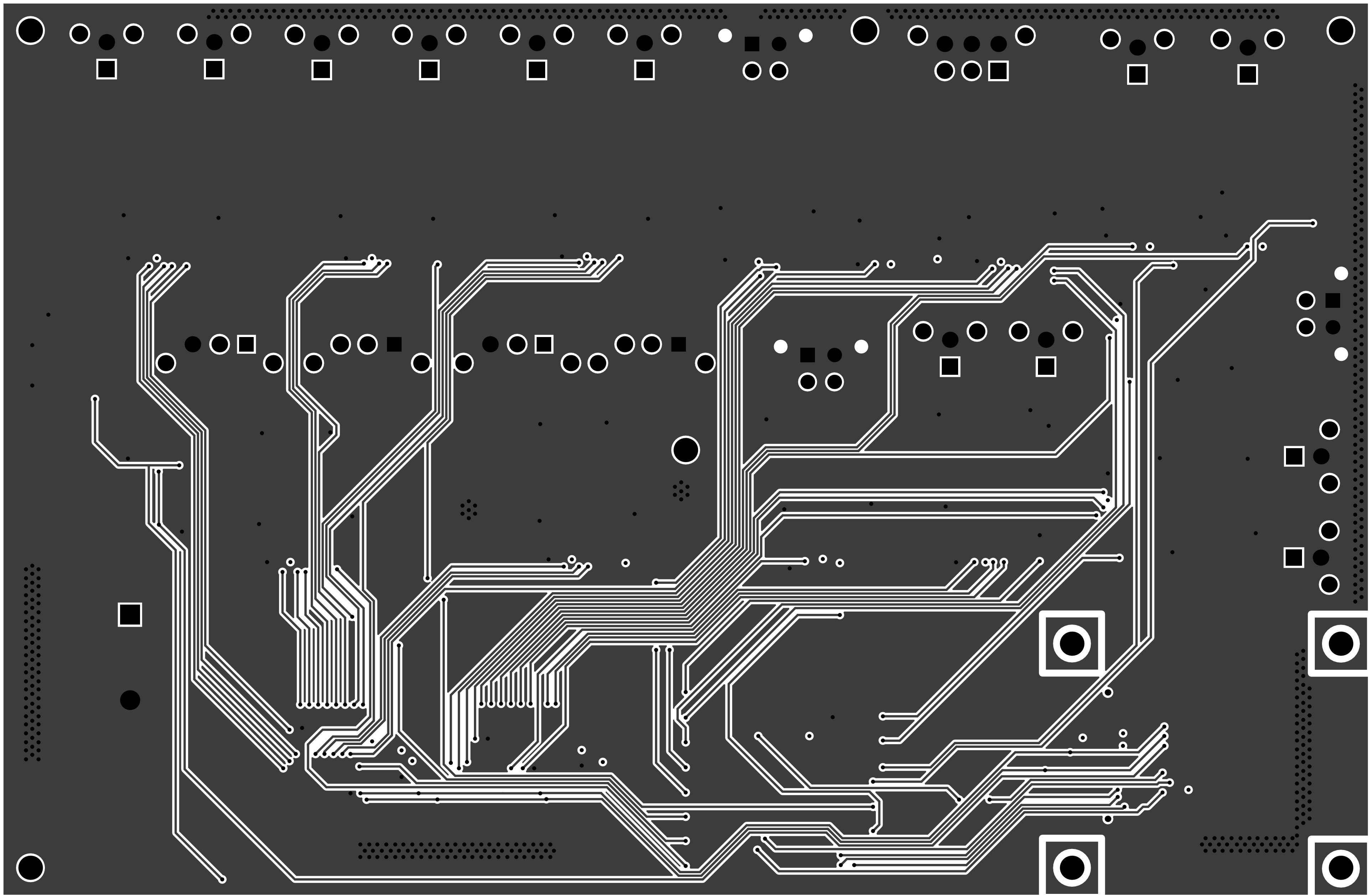


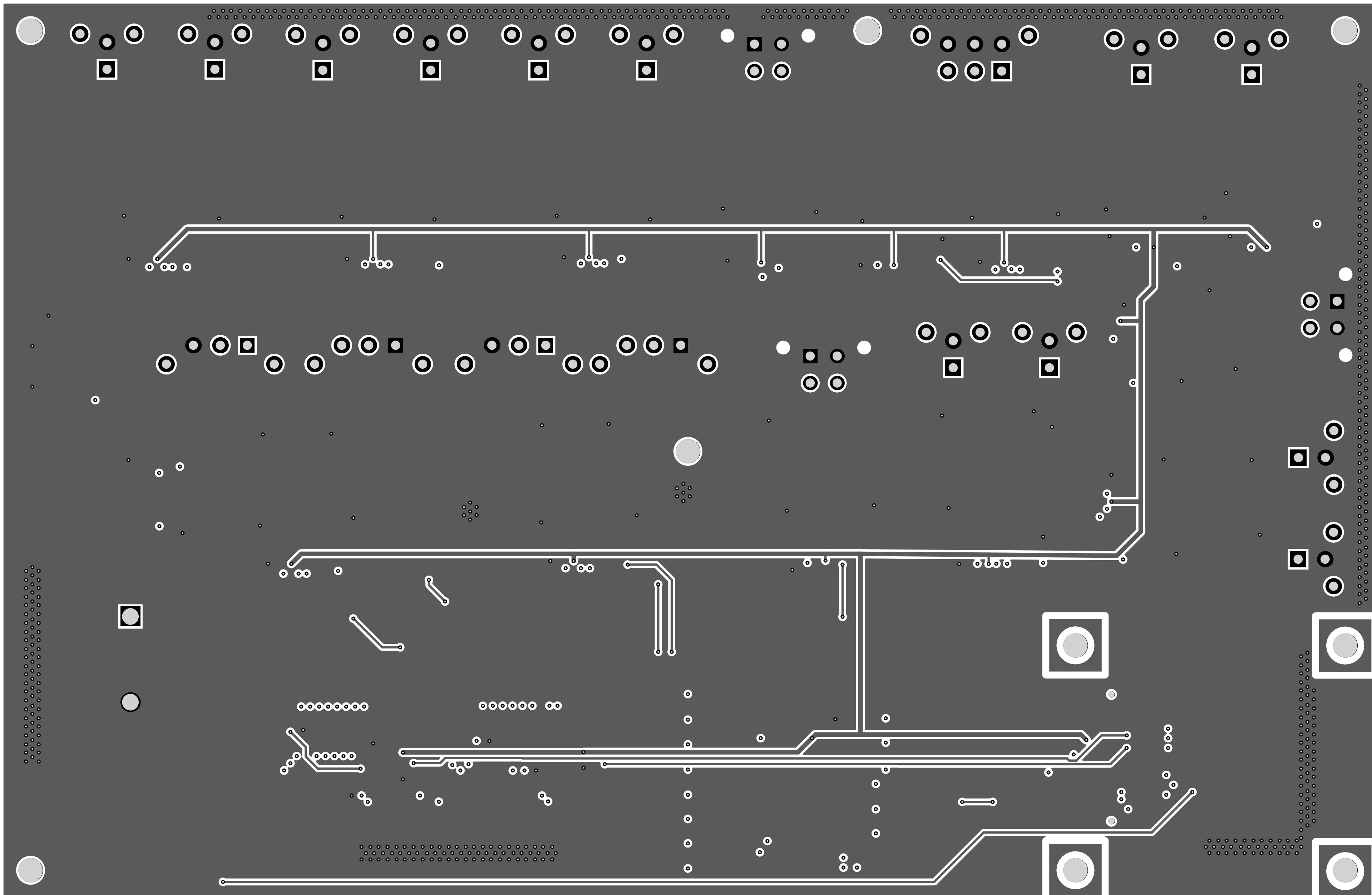


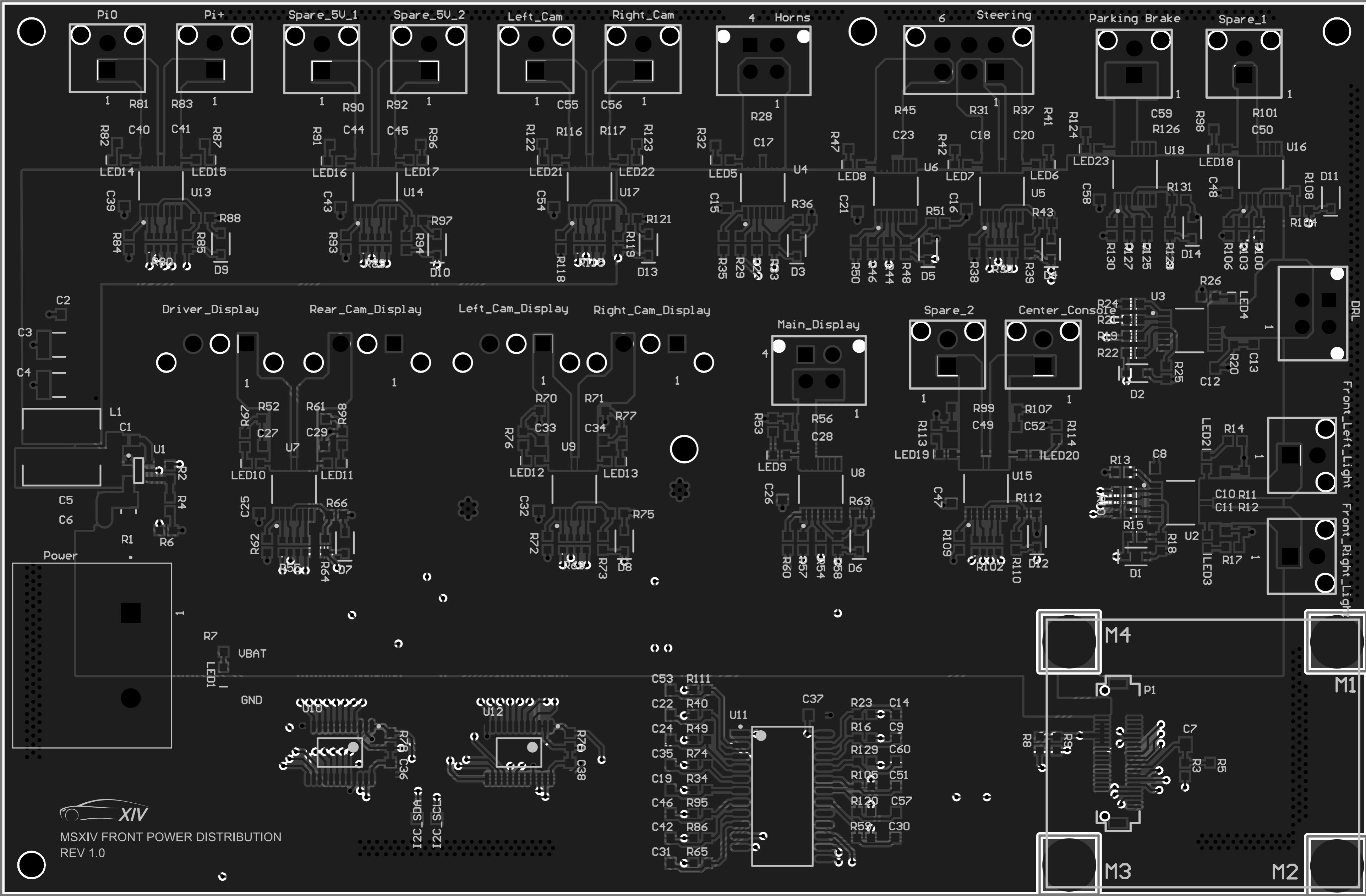












Bill of Materials

Project:	SXIV_Front_Power_Distribution.PrjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2020-02-26 1:58 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	273

MIDNIGHT SUN

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CAP CER 0.1UF 50V 10% X7R 0603	C16,C21,C25,C26,C32,C36,C37,C38,C38	Kyocera AVX	0603C104KAT2A	Digi-Key	478-5052-1-ND	0.09298	20	\$ 1.86
CAP CER 22uF 16V ±20% X5R 1210	C3,C4	Murata	GRM32ER61C22GME20L	Digi-Key	490-1881-1-ND	2.59	2	\$ 5.18
CAP CER 22uF 35V X5R 0805	C5	TDK	C2012X5R1V226M125AC	Digi-Key	445-14428-1-ND	1.51	1	\$ 1.51
CAP CER 0.1UF 100V 10% X7R 0805	C7	Murata	GCM21BR72A104KA37L	Digi-Key	490-4789-1-ND	0.42506	1	\$ 0.43
CAP CER 22PF 50V 10% X7R 0603	C,22,C24,C30,C31,C35,C42,C46,C51,C	KEMET	C0603C22J5GACAUTO	Digi-Key	399-6868-1-ND	0.11689	14	\$ 1.64
CAP CER 10nF 50V 5% X7R 0603	C,27,C28,C29,C33,C34,C41,C44,C	KEMET	C0603C103J5JACTU	Digi-Key	399-1384-1-ND	0.29754	22	\$ 6.55
CONN 2POS MICRO-FIT3mm	Light, Left_Cam, Parking Brake, P10, Pi+, Right	Molex	0430450227	Digi-Key	WM10657-ND	0.98295	12	\$ 11.80
DIODE ZENER 3.3V 200MW SOD323	D3,D4,D5,D6,D7,D8,D10,D11,D12,D	Vishay	BZ384C3V3-E3-08	Digi-Key	ZX384C3V3-E3-08GICT-	0.26433	14	\$ 3.70
CONN 3POS MICROFIT	L, Left_Cam_Display, Rear_Cam_Display, Right	Molex	0436500315	Digi-Key	WM1918-ND	1.37	4	\$ 5.47
CONN 4POS MICRO-FIT3mm	DRL_Horns, Main_Display	Molex	0430450427	Digi-Key	WM10667-ND	1.78	3	\$ 5.34
IND 3.3uH 5.2A 20MOHM SMD	L1	TDK	VLP8040T-3R3N	Digi-Key	445-6581-1-ND	1		
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VST75000	Digi-Key	732-4980-1-ND	0.18596	1	\$ 0.19
LED YELLOW CLEAR 2V 0603	LED11,LED12,LED13,LED14,LED15,LED16	Wurth Electronics	150060VST75000	Digi-Key	732-4981-1-ND	0.18596	22	\$ 4.09
STANDOFF RND M2.5x0.45 STEEL 5MM	M1, M2, M3, M4	Wurth Electronics	9774050151R	Digi-Key	732-7095-1-ND	1.45	4	\$ 5.79
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.91	1	\$ 1.91
CONN BARRIER STRIP 2CIRC 0.375"	Power	BUCHANAN-TECONNECTIVITY	6PCV-02-006	Digi-Key	A98481-ND	2.17	1	\$ 2.17
R ES 0.006 OHM 1% 1/2W 1206	R1	Panasonic	ERJMP2KF6M0U	Digi-Key	P19333CT-ND	1		
RES 54.9KOHM 1% 1/10W 0603	R2	Panasonic	ERJ-3EKF5492V	Digi-Key	P54.9KHTCND	0.13283	1	\$ 0.13
RES 100K OHM 5% 1/8W 0603	R3	Yageo	RC0603JR-0710KL	Digi-Key	311-10.0KGRCT-ND	0.13283	1	\$ 0.13
RES 10K OHM 1% 1/10W 0603	R47,R53,R67,R68,R76,R77,R82,R87,R91	Yageo Phycamp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCTND	0.03055	25	\$ 0.76
RES 4.7K OHM 1% 1/10W 0603	R57,R58,R59,R64,R65,R73,R74,R78,R79	Yageo Phycamp	RC0603FR-0740KL	Digi-Key	311-4.70KHRCTND	0.03055	45	\$ 1.37
RES ARRAY 4 RES 4.7K OHM 1206	R10,R30,R55,R69,R80,R89,R102,R115	Panasonic	EXB-38V472JV	Digi-Key	Y9472CTND	0.13283	8	\$ 1.06
RES 47K OHM 1% 1/10W 0603	R52,R56,R61,R70,R71,R81,R83,R90,R92	Panasonic	ERJ3EKF4702V	Digi-Key	P47.0KHTCND	0.07571	22	\$ 1.67
RES SMA 47 OHM 1% 1/10W 0603	R38,R50,R60,R62,R72,R84,R93,R106,R110	Yageo	AC0603FR-0747RL	Digi-Key	311-47LDCTN	0.03719	14	\$ 0.52
RES 1.6K OHM 1% 1/10W 0603	R18,R43,R66,R75,R88,R97,R112,R121	Yageo	RC0603FR-071K6L	Digi-Key	311-1.60KHRCTND	0.13283	8	\$ 1.06
RES 1.21K OHM 1% 1/10W 0603	R25,R36,R51,R63,R108,R131	Yageo	RC0603FR-071K21L	Digi-Key	311-1.21KHRCTND	0.13283	6	\$ 0.80
CONN 6POS MICRO-FIT3mm	Steering	Molex	43045-0627	Digi-Key	WM10673-ND	2.1	1	\$ 2.10
REG BUCK4.5V TO 17V,5A, SYNCHRONOUS	U1	Texas Instruments	TPS565201DDCT	Digi-Key	296-47501-1-ND	2.05	1	\$ 2.05
LOAD SWITCH BT57200-2EPAVG-TSDSO-14	U2,U5,U7,U9,U13,U14,U15,U17	Infineon	BT572002EPAXUMA1	Digi-Key	S72002EPAXUMA1CT-N	1.73	8	\$ 13.81
LOAD SWITCH BT570401EPAPG-TSDSO-14	U3,U6,U8,U16,U18	Infineon	BT570401EPAXUMA1	Digi-Key	S70401EPAXUMA1CT-N	1.77	5	\$ 8.83
IC LOAD SWITCH BT570081EPPXUMA1	U4	Infineon	BT570081EPPXUMA1	Digi-Key	S70081EPPXUMA1CT-N	2.78	1	\$ 2.78
16-BIT-T2C-BUS AND SMBUS LOW POW	U10,U12	NXP USA	PCA9539PW/Q900J	Digi-Key	568-13622-1-ND	3.17	2	\$ 6.35
IC MUX/DEMUX 1X16 24SSOP	U11	Texas Instruments	CD74HC4067M96	Digi-Key	296-29408-1-ND	0.99623	1	\$ 1.00
					Total:			\$ 102.04

Design Rules Verification Report

Filename : D:\Josh9\Documents\Midnight Sun\hardware\MSXIV_FrontPowerDistribution\Fro

Warnings 0

Rule Violations 115

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=3mm) (All)	4
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	4
Minimum Solder Mask Sliver (Gap=0.15mm) (All), (All)	50
Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)	53
Silk to Silk (Clearance=0.254mm) (All), (All)	4
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	115

Hole Size Constraint (Min=0.025mm) (Max=3mm) (All)	
Hole Size Constraint: (3.7mm > 3mm) Pad M1-(149.6mm,28.4mm) on Multi-Layer Actual Hole Size = 3.7mm	
Hole Size Constraint: (3.7mm > 3mm) Pad M2-(149.6mm,3.3mm) on Multi-Layer Actual Hole Size = 3.7mm	
Hole Size Constraint: (3.7mm > 3mm) Pad M3-(119.6mm,3.4mm) on Multi-Layer Actual Hole Size = 3.7mm	
Hole Size Constraint: (3.7mm > 3mm) Pad M4-(119.6mm,28.417mm) on Multi-Layer Actual Hole Size = 3.7mm	

Hole To Hole Clearance (Gap=0.254mm) (All), (All)	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(119.6mm,28.4mm) on Multi-Layer And Pad M4-(119.6mm,28.417mm) or	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(119.6mm,3.4mm) on Multi-Layer And Pad M3-(119.6mm,3.4mm) or	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(149.6mm,28.4mm) on Multi-Layer And Pad M1-(149.6mm,28.4mm) or	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(149.6mm,3.4mm) on Multi-Layer And Pad M2-(149.6mm,3.3mm) or	

Minimum Solder Mask Sliver (Gap=0.15mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.15mm) Between Pad P1-(123.6mm,22.958mm) on Multi-Layer And Pad P1-(125.1mm,23.708mm)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.15mm) Between Pad P1-(123.6mm,8.858mm) on Multi-Layer And Pad P1-(125.1mm,8.108mm) or
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-1(124.9mm,45.28mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R10-2(124.9mm,44.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-1(109.12mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R102-2(110mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-3(110.8mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-5(111.68mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R102-6(110.8mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-7(110mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-3(124.9mm,43.6mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-5(126.3mm,42.72mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R10-6(126.3mm,43.6mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-7(126.3mm,44.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-1(64.62mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R115-2(65.5mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-3(66.3mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-5(67.18mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R115-6(66.3mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-7(65.5mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-1(110.82mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R30-2(111.7mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-3(112.5mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-5(113.38mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R30-6(112.5mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-7(111.7mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-1(31.52mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R55-2(32.4mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-3(33.2mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-5(34.08mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R55-6(33.2mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-7(32.4mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-1(62.92mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R69-2(63.8mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-3(64.6mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-5(65.48mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R69-6(64.6mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-7(63.8mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-1(16.62mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R80-2(17.5mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-3(18.3mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-5(19.18mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R80-6(18.3mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-7(17.5mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-1(40.62mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R89-2(41.5mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-3(42.3mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-5(43.18mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R89-6(42.3mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-7(41.5mm,73.8mm) on Component Side And Pac

Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (109.062mm,38.038mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (110.762mm,71.438mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (124.438mm,45.338mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (16.562mm,72.038mm) on Top Overlay And Pad R80-1(16.62mm,72.5mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (31.462mm,37.938mm) on Top Overlay And Pad R55-1(31.52mm,38.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (40.562mm,71.938mm) on Top Overlay And Pad R89-1(40.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (62.862mm,38.238mm) on Top Overlay And Pad R69-1(62.92mm,38.7mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (64.562mm,71.938mm) on Top Overlay And Pad R115-1(64.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Center_Console-0(113.7mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Center_Console-0(119.7mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Left_Light-0(148.34mm,46.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Left_Light-0(148.34mm,52.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Right_Light-0(148.3mm,35mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Right_Light-0(148.3mm,41mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad I2C_SCL-TP(48.8mm,8.6mm) on Component Side And Text "I2C_SCL"
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad I2C_SDA-TP(46.6mm,8.6mm) on Component Side And Text "I2C_SDA"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.15mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.15mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Left_Cam-0(56.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Left_Cam-0(62.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad M1-(149.6mm,28.4mm) on Component Side And Text "Front_Right_Light"
Silk To Solder Mask Clearance Constraint: (0.01mm < 0.15mm) Between Pad M1-(149.6mm,28.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad M1-(149.6mm,28.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad M2-(149.6mm,3.3mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad M2-(149.6mm,3.3mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.15mm) Between Pad M3-(119.6mm,3.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.01mm < 0.15mm) Between Pad M3-(119.6mm,3.4mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.15mm) Between Pad M4-(119.6mm,28.417mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.15mm) Between Pad M4-(119.6mm,28.417mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Parking_Brake-0(123.9mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Parking_Brake-0(129.9mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi+-0(20.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi-0(26.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi0-0(14.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi0-0(8.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Right_Cam-0(68.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Right_Cam-0(74.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_1-0(136.2mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_1-0(142.2mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_2-0(103mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_2-0(109mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_1-0(32.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_1-0(38.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_2-0(44.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_2-0(50.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Steering-0(102.4mm,96.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Steering-0(114.4mm,96.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-1(14.275mm,48.55mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-2(14.275mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-3(14.275mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-4(16.525mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-5(16.525mm,47.6mm) on Component Side And Track

Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-6(16.525mm,48.55mm) on Component Side And Track

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "Center_Console" (114.1mm,65.2mm) on Top Overlay And Text "R21"

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "Center_Console" (114.1mm,65.2mm) on Top Overlay And Text "R24"

Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "Front_Right_Light" (150.3mm,43.8mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.24mm < 0.254mm) Between Text "M1" (149.575mm,22.85mm) on Top Overlay And Track