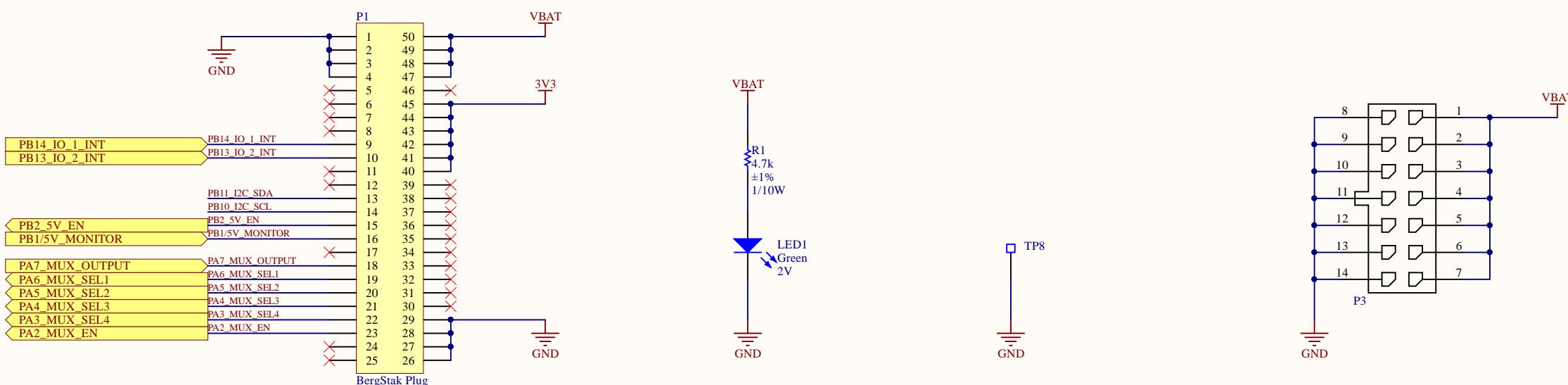
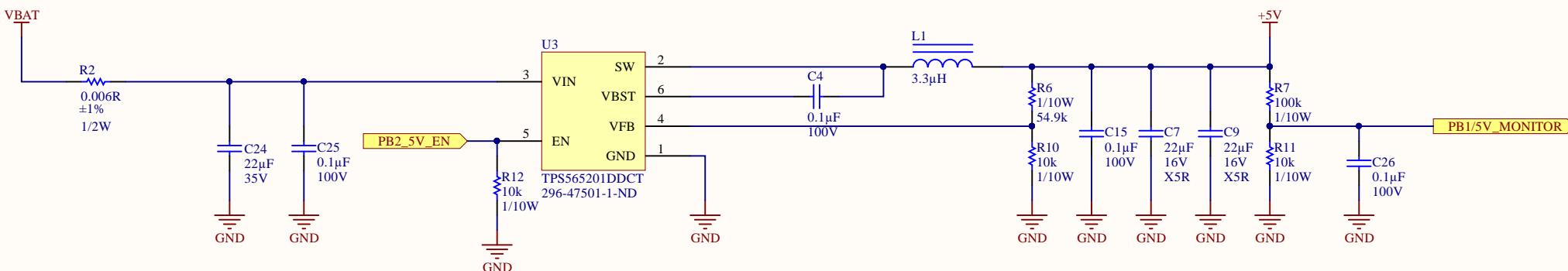
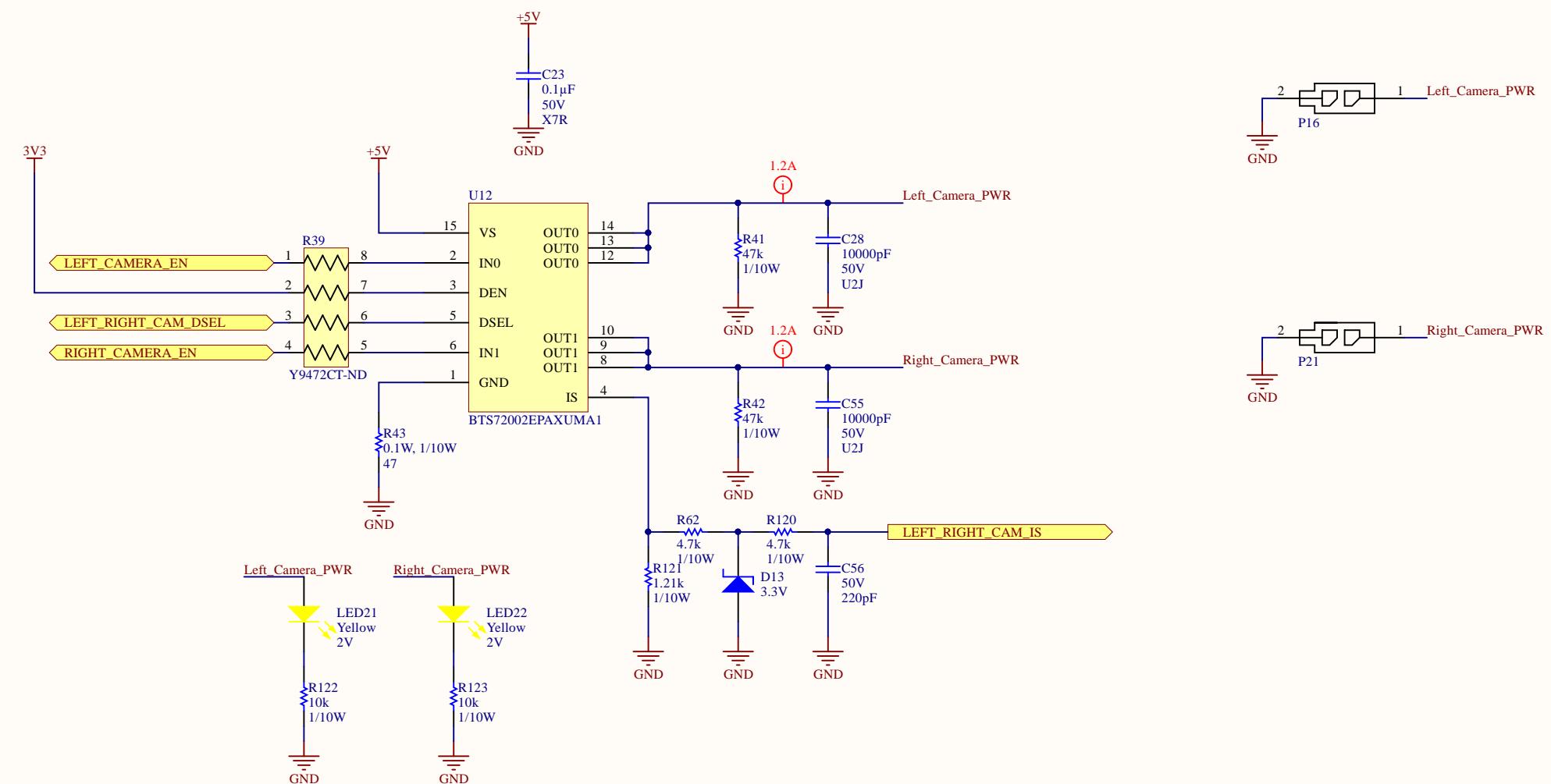


Regulator



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Controller Board Interface
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-19
SHEET *	OF *

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PROJECT MSXIV_Front_Power_Distribution.PrjPcb

DOCUMENT Title

PART NUMBER VARIANT [No Variations]

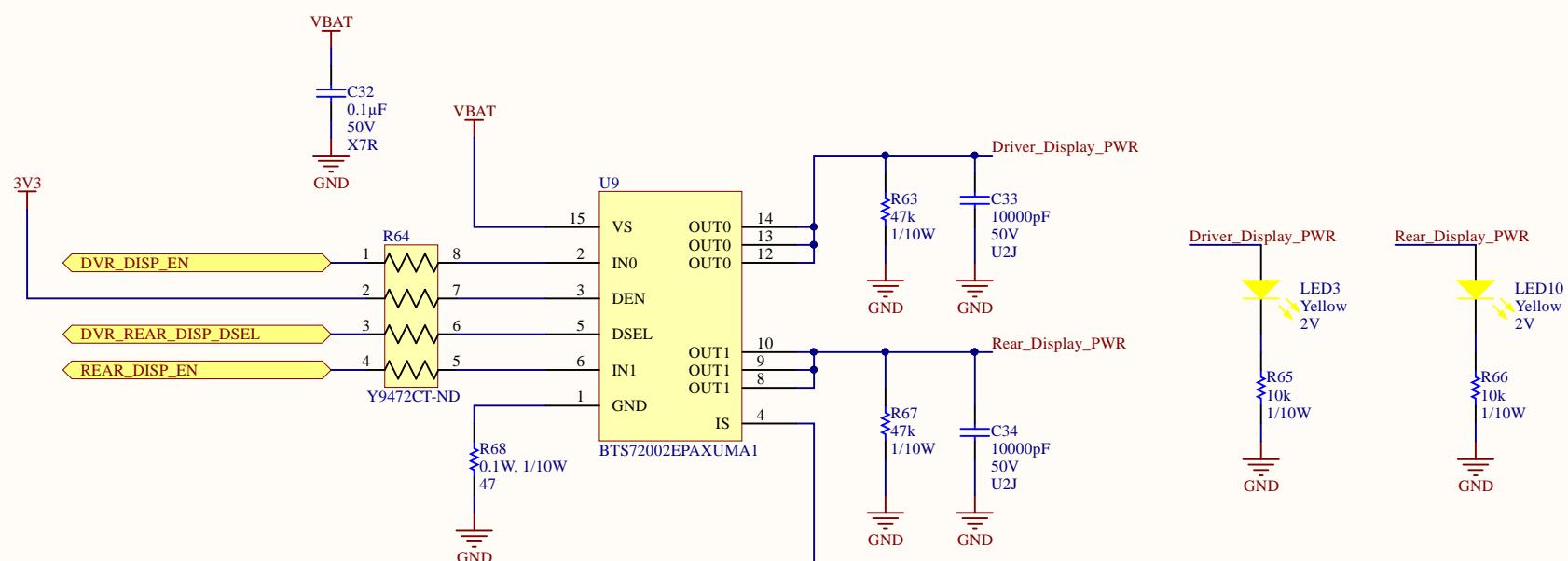
DRAWN BY REVISION

LAST MODIFIED 2020-02-19 SHEET * OF *

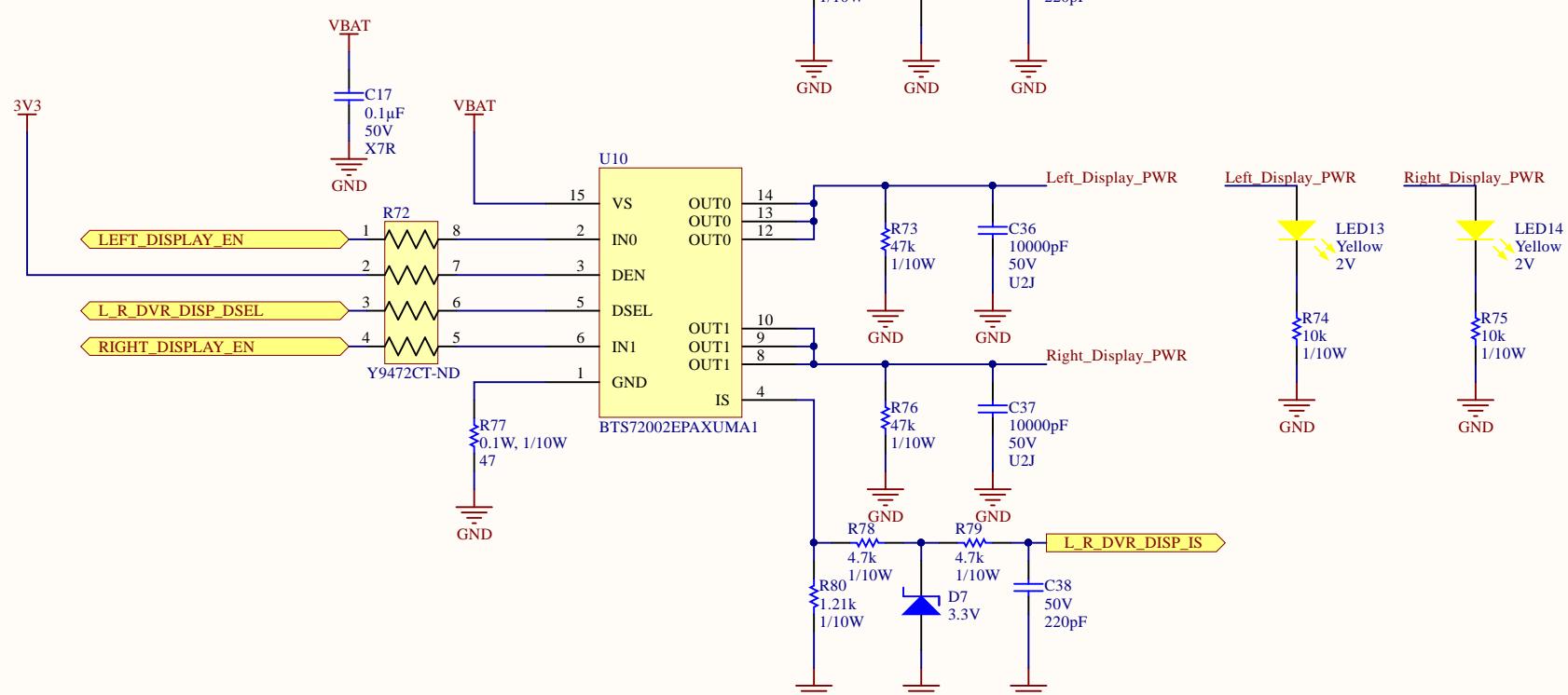


Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

A



B

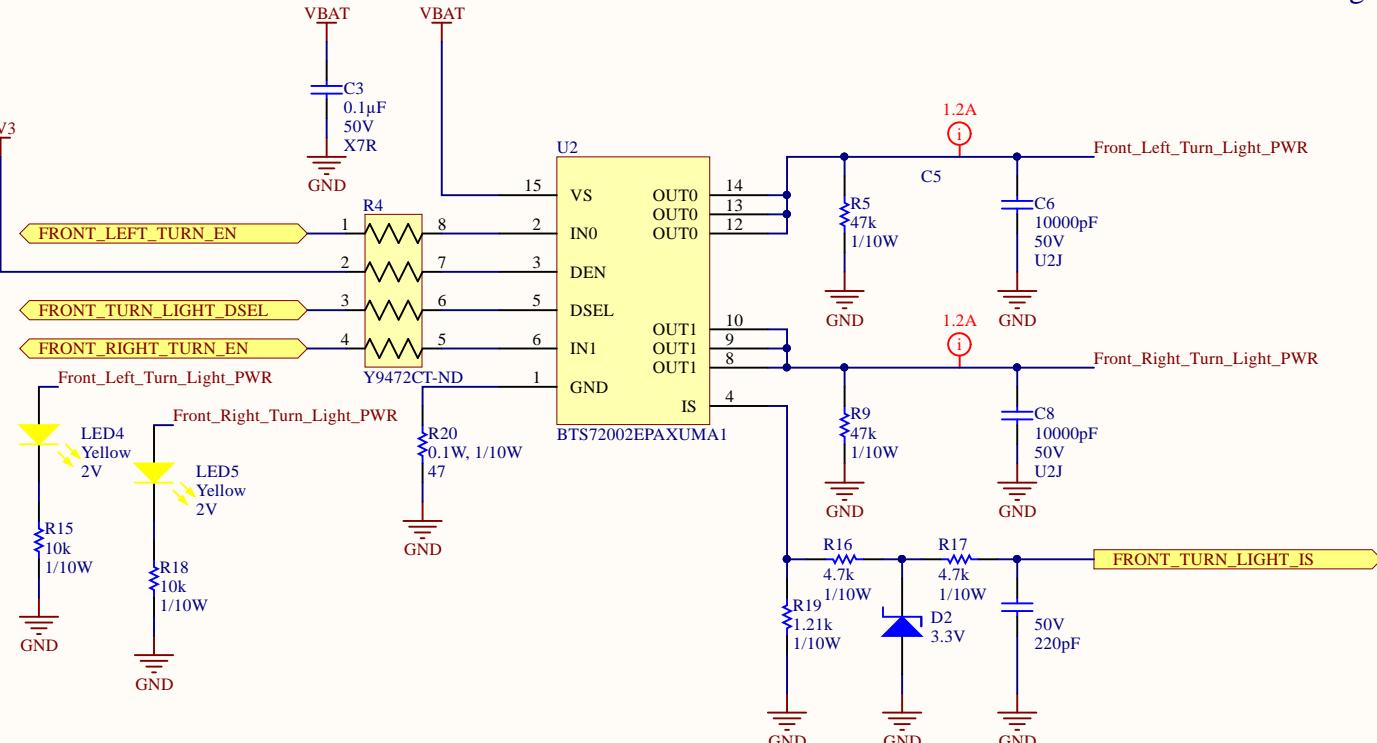


C

D

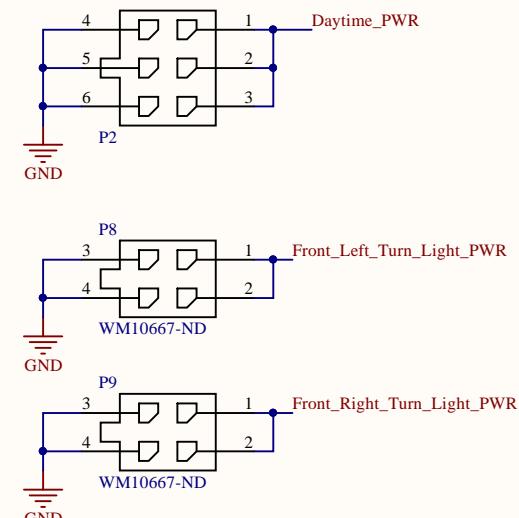
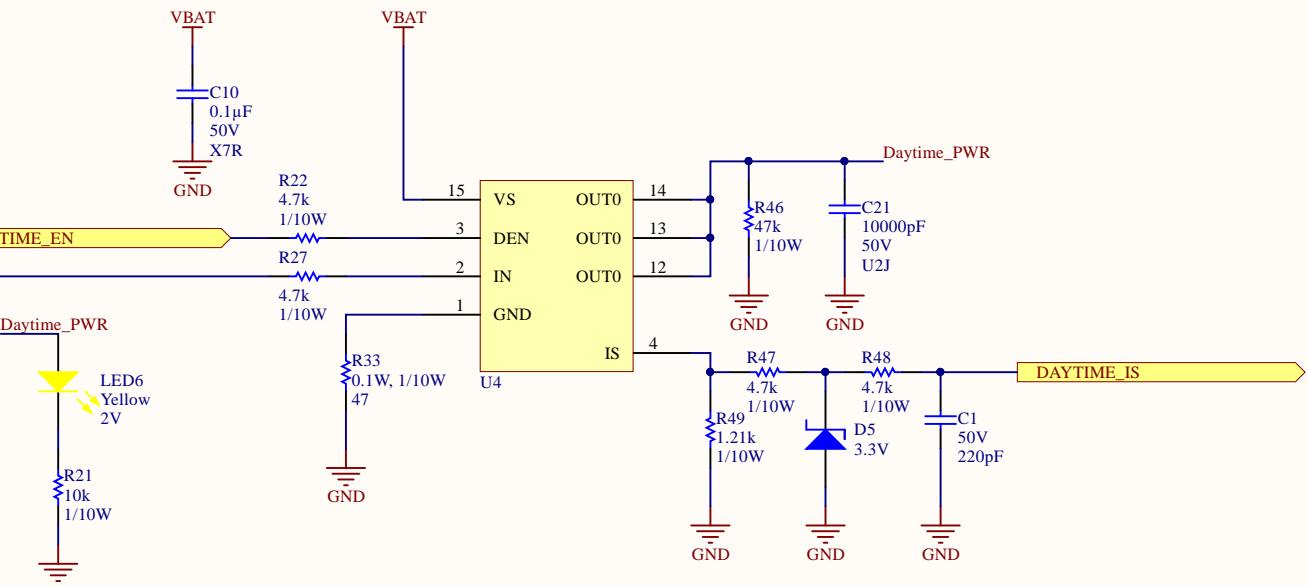
PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-19
SHEET *	OF *

Front light



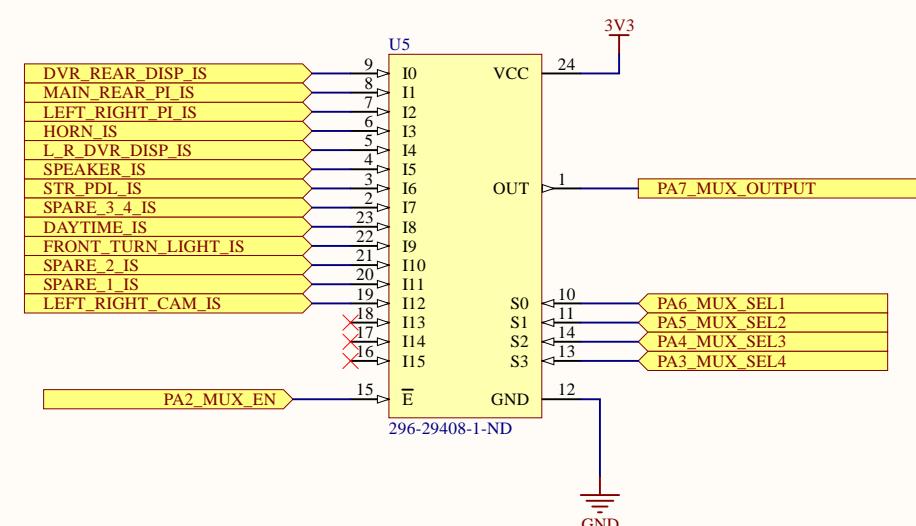
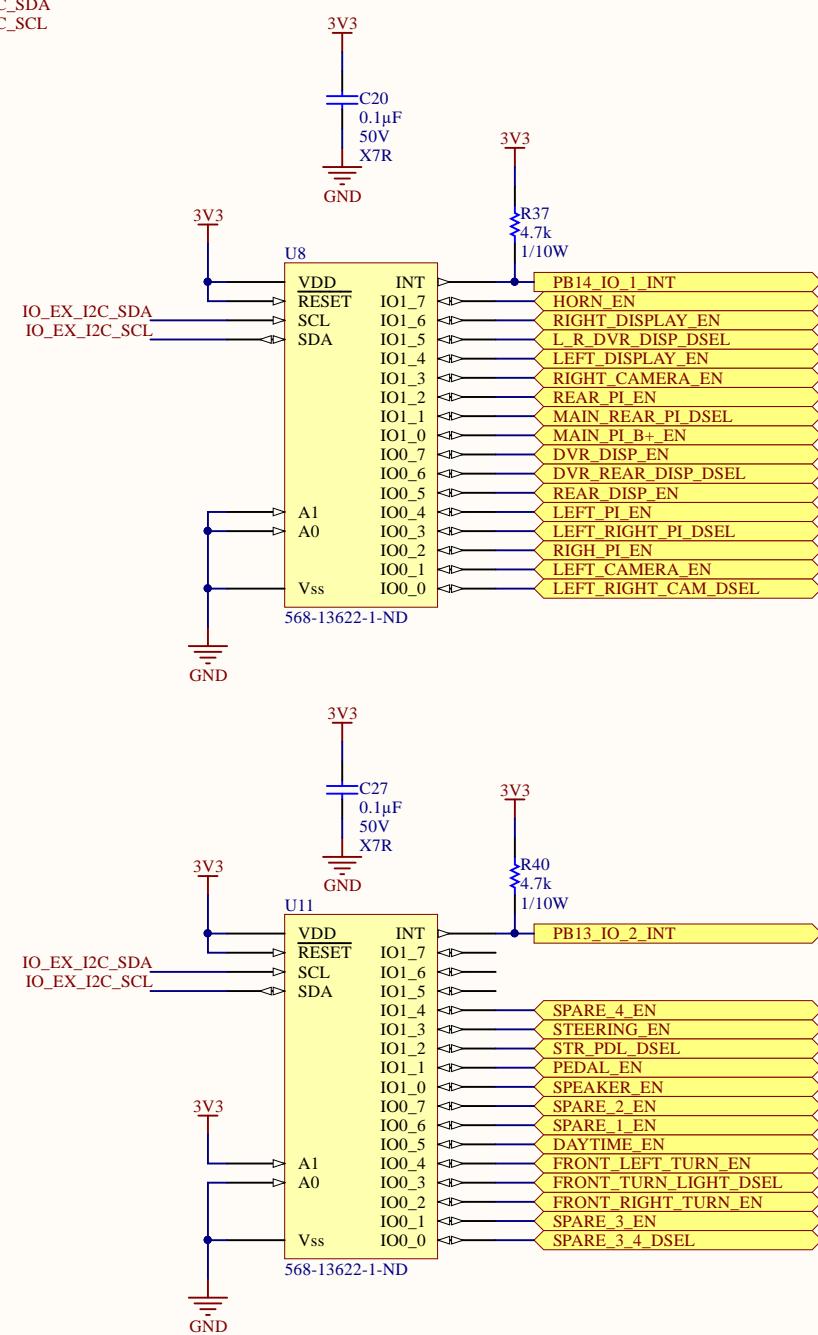
- ▲ Light Load
Nominal Current: 1.2 A
- Overload Current: 8.7 - 11.5 A
- Based on the specs of BTS7200-2EPC

- ▲ Draws 4mA
when active

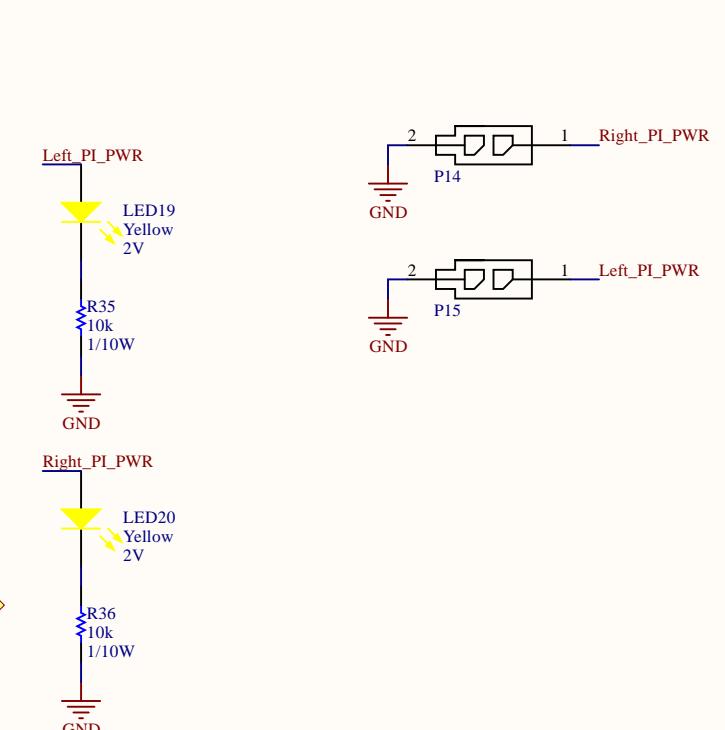
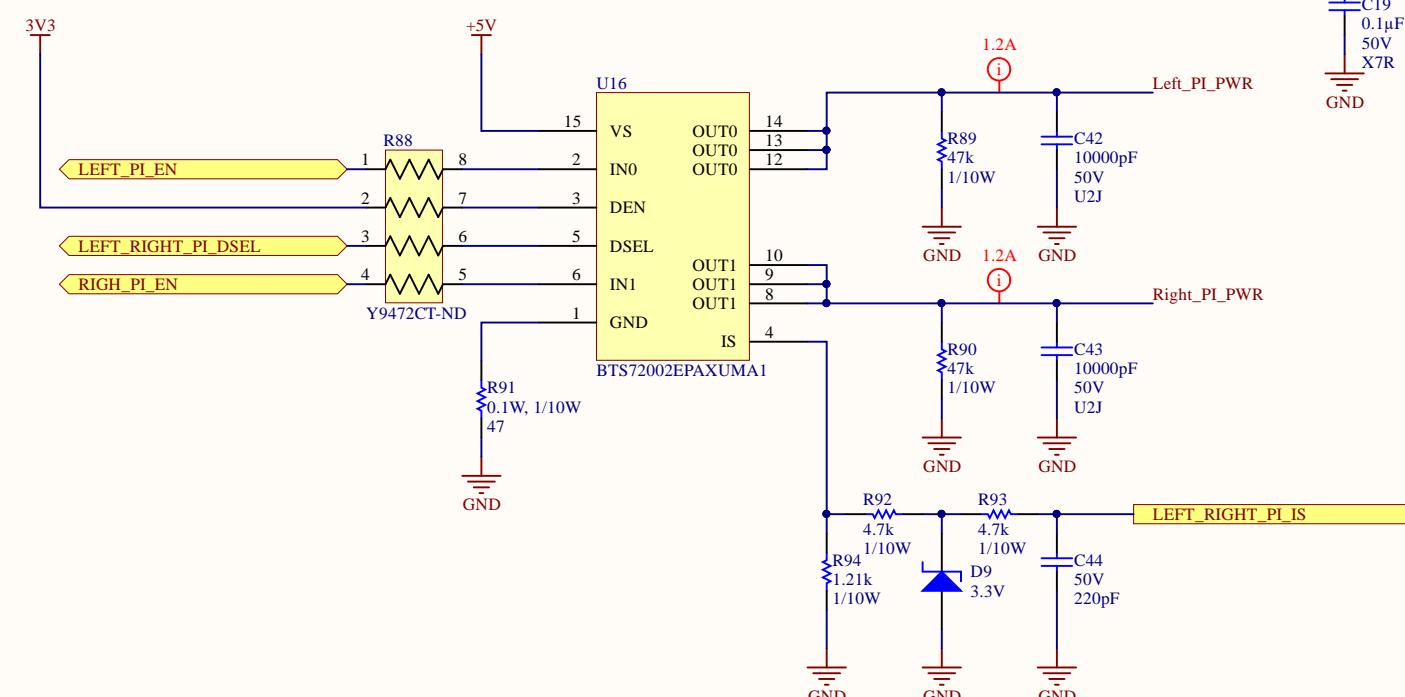
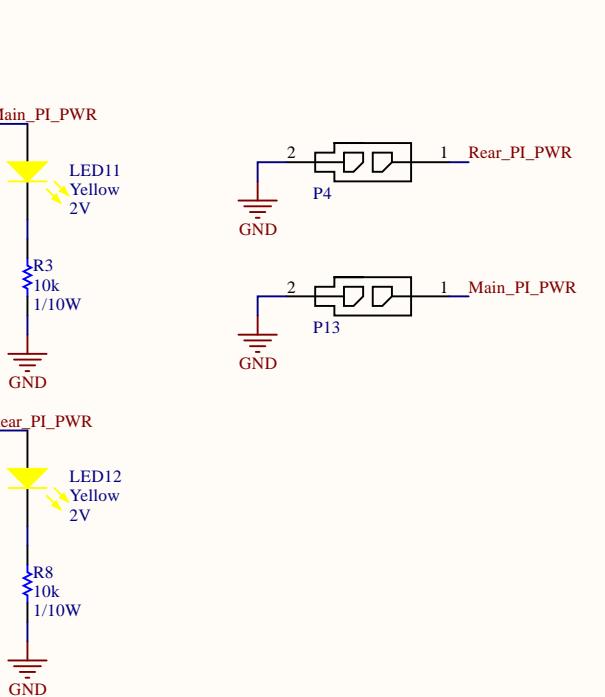
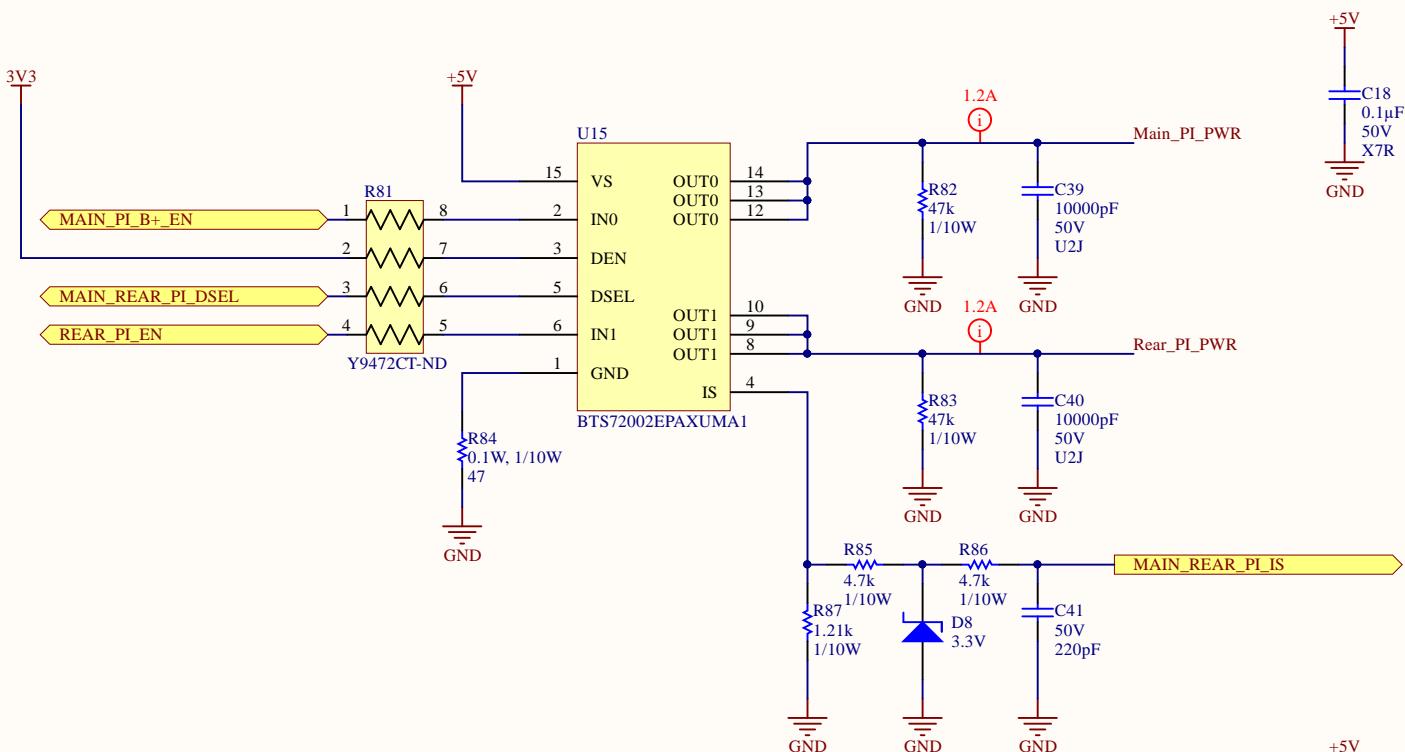


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	
DOCUMENT	Title	
PART NUMBER	VARIANT	[No Variations]
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-19	SHEET * OF *

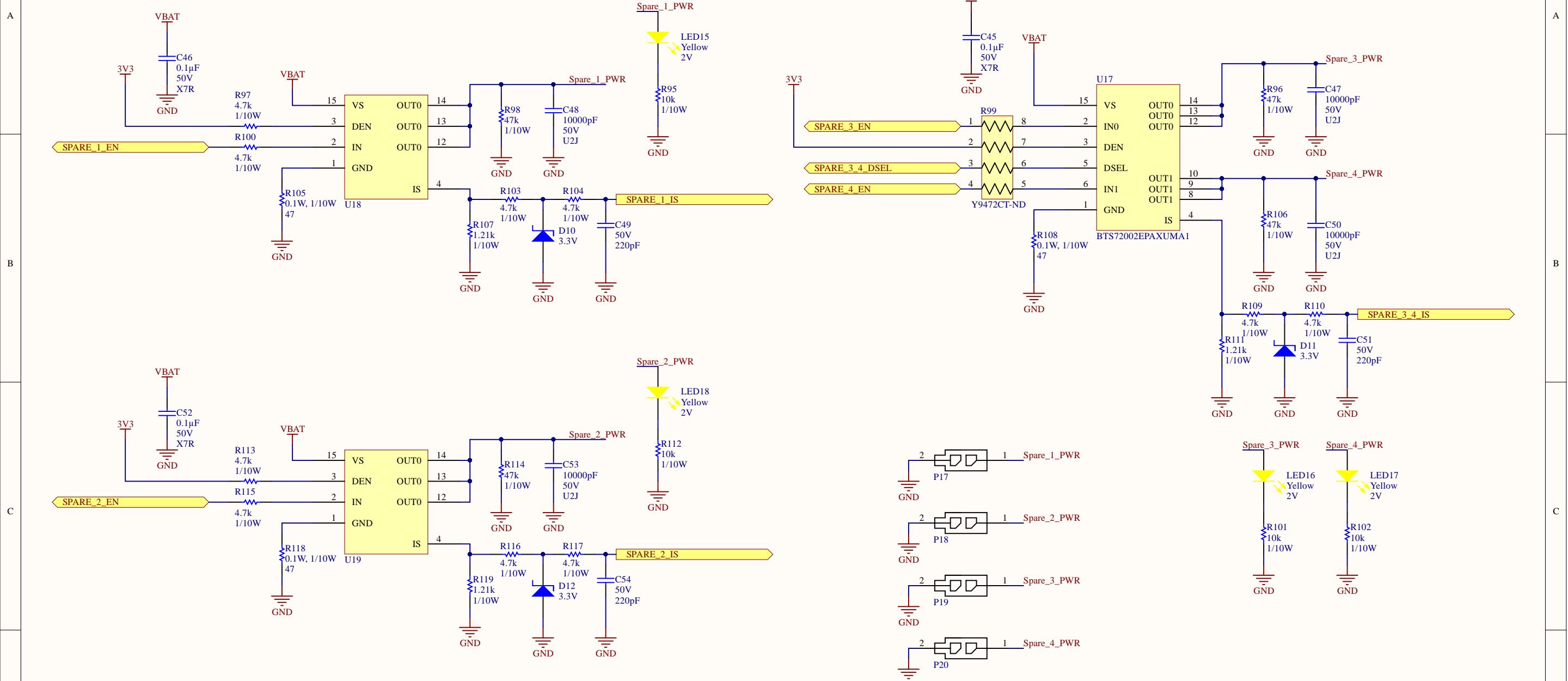
IO_EX_I2C_SDA
IO_EX_I2C_SCL



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-19
	SHEET * OF *

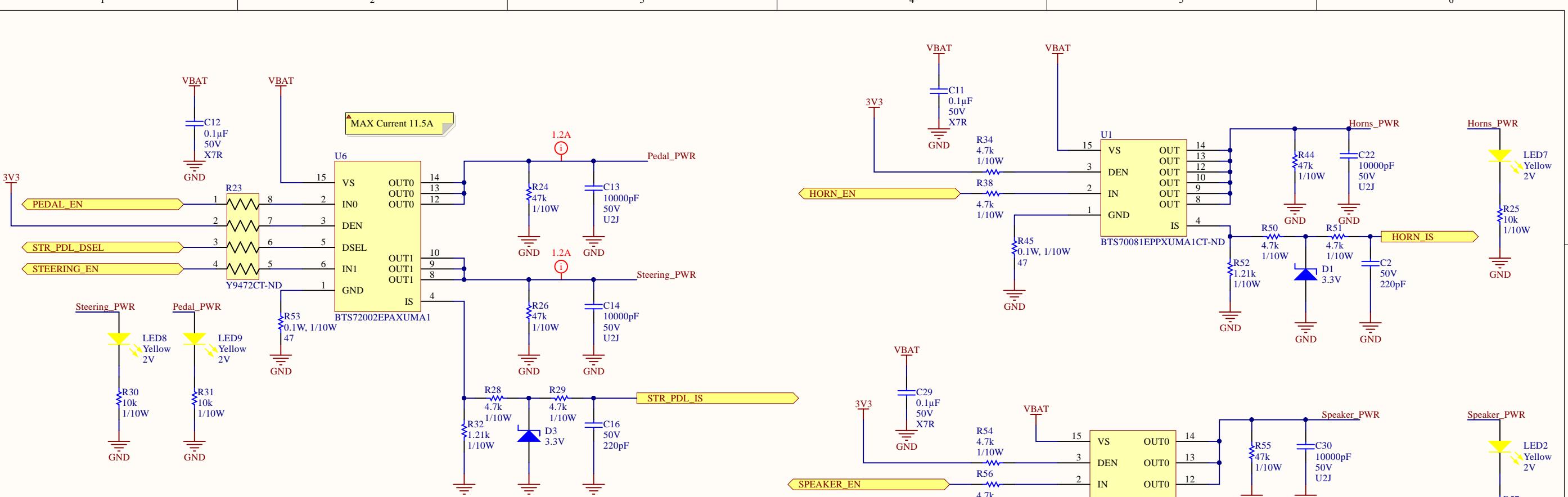


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
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DRAWN BY	REVISION	
LAST MODIFIED	2020-02-19	

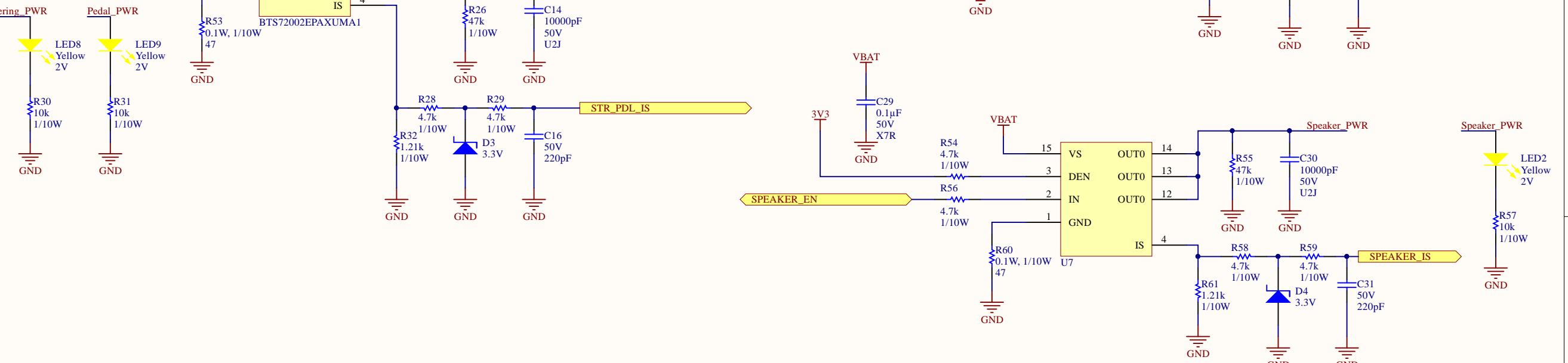


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-19	SHEET * OF *

A



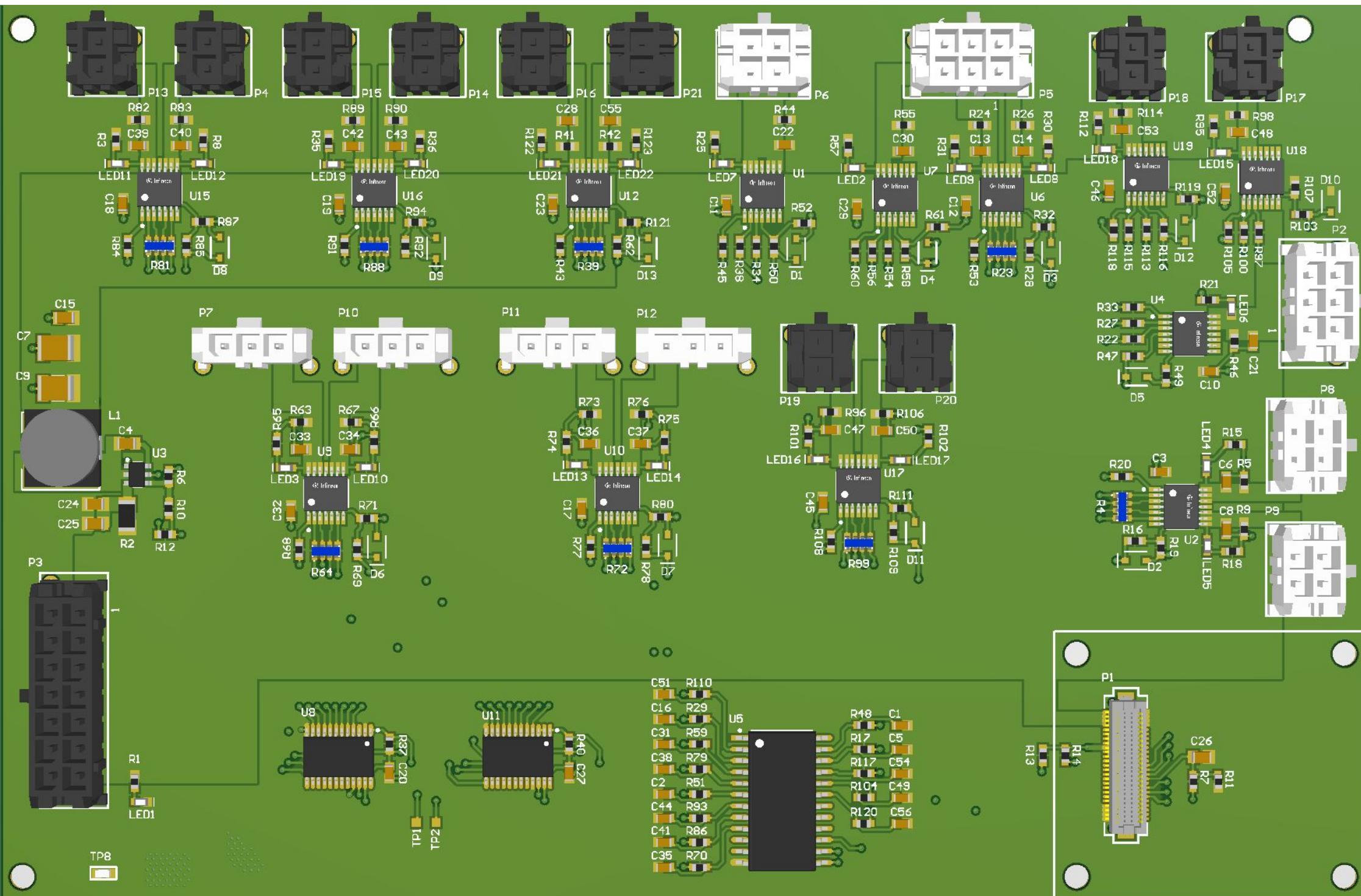
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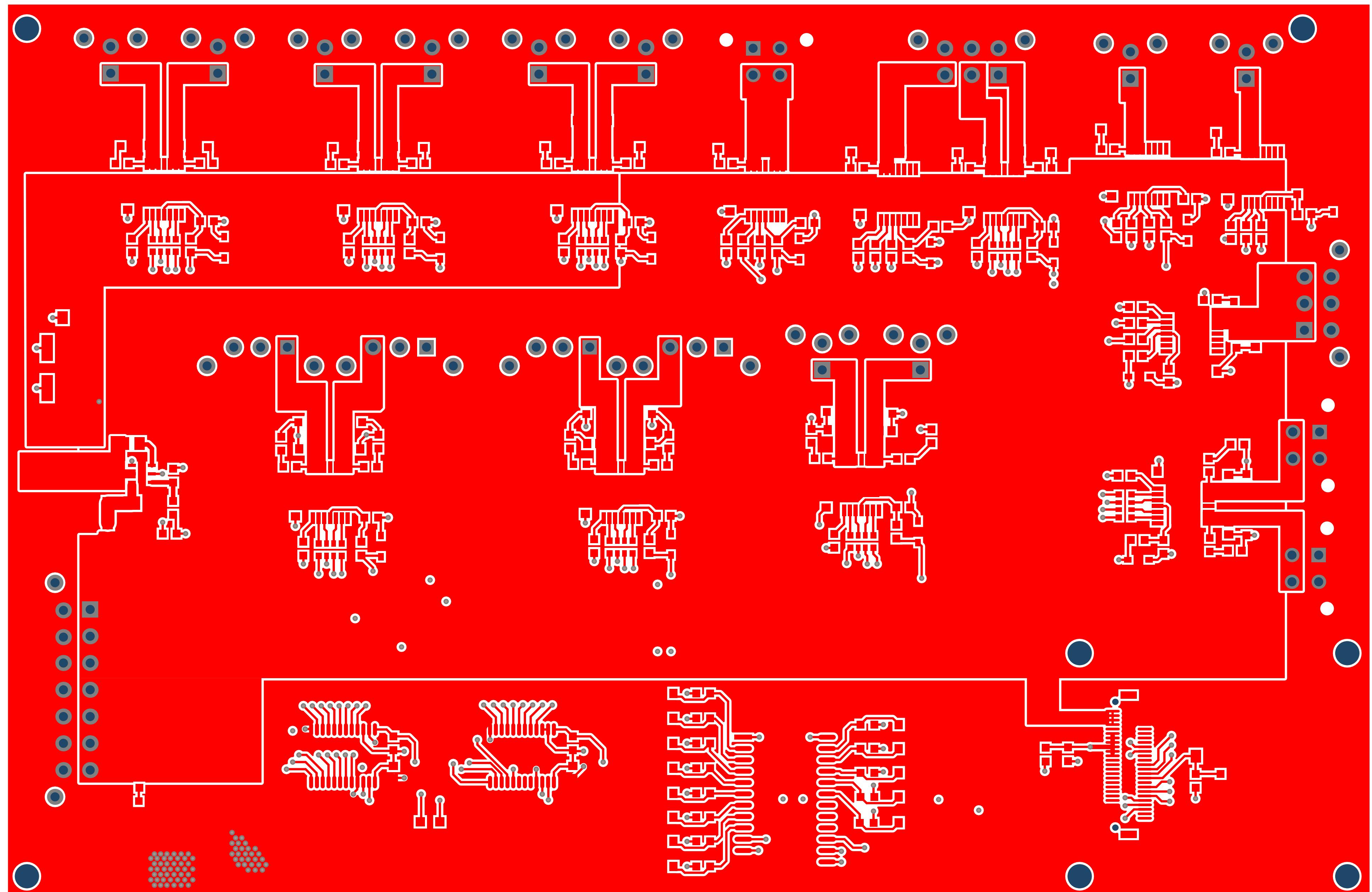


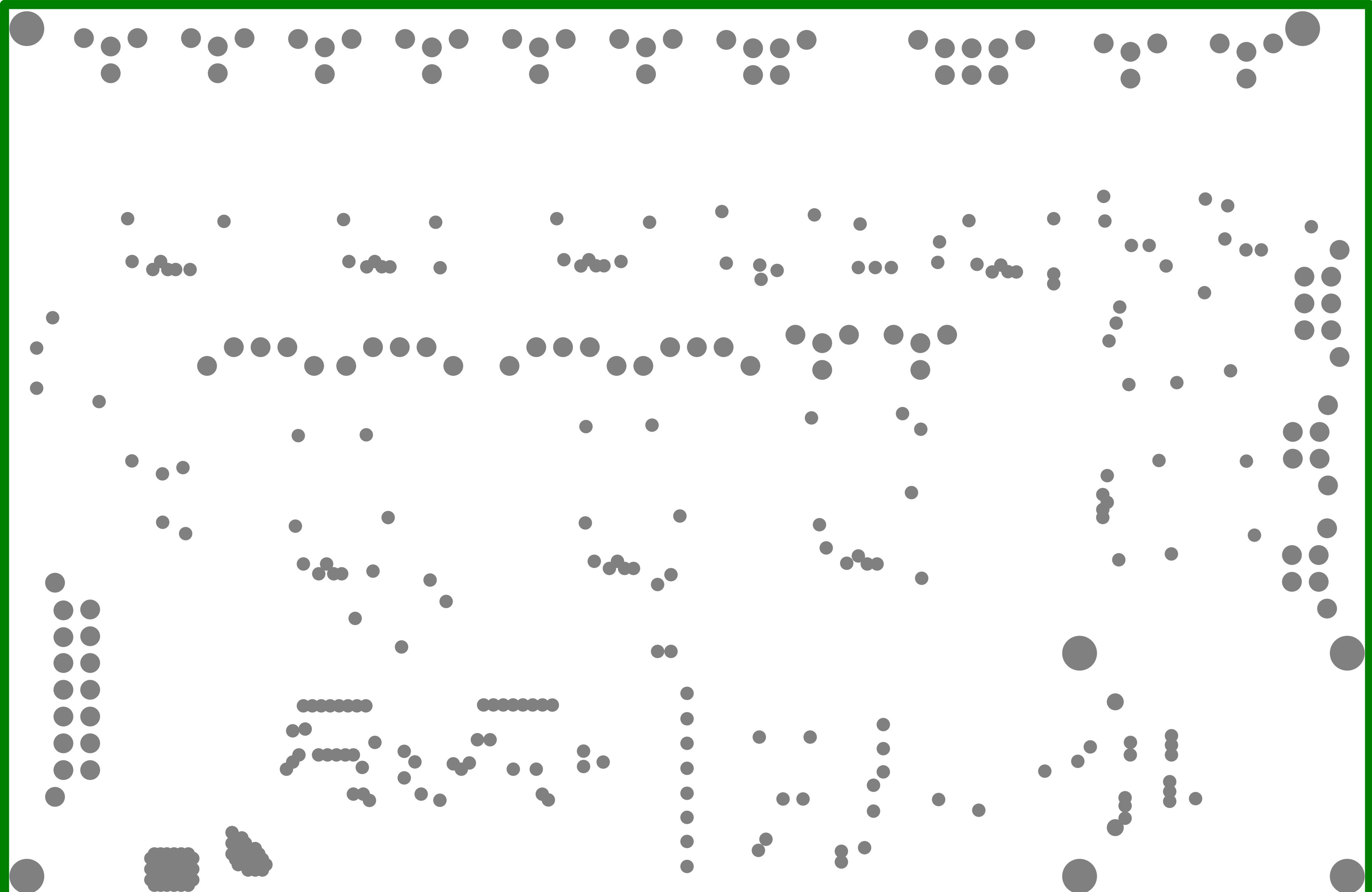
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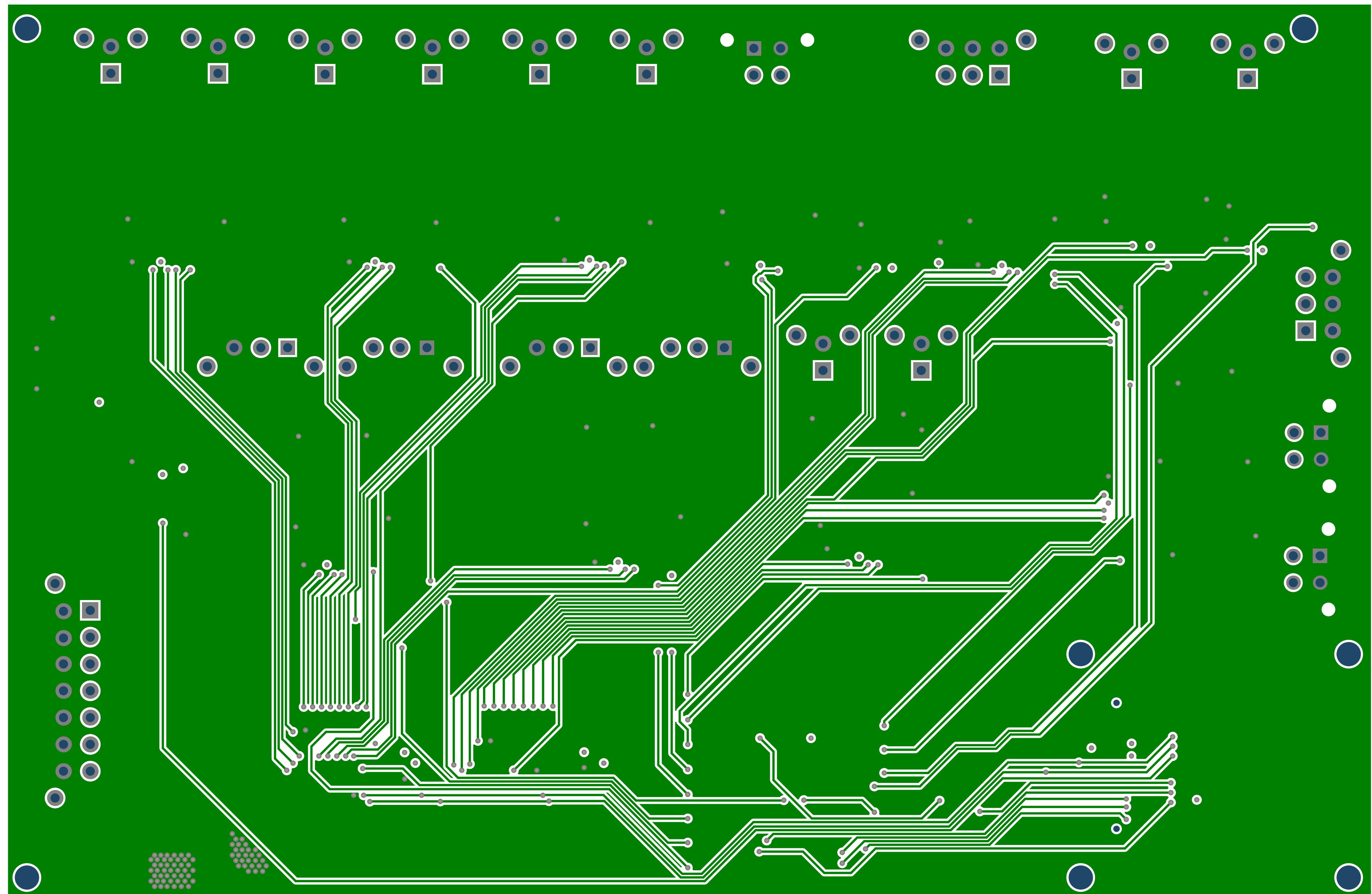
PROJECT	MSXIV_Front_Power_Distribution.PrbPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-19	SHEET * OF *
hardware@uwmidsun.com		Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978

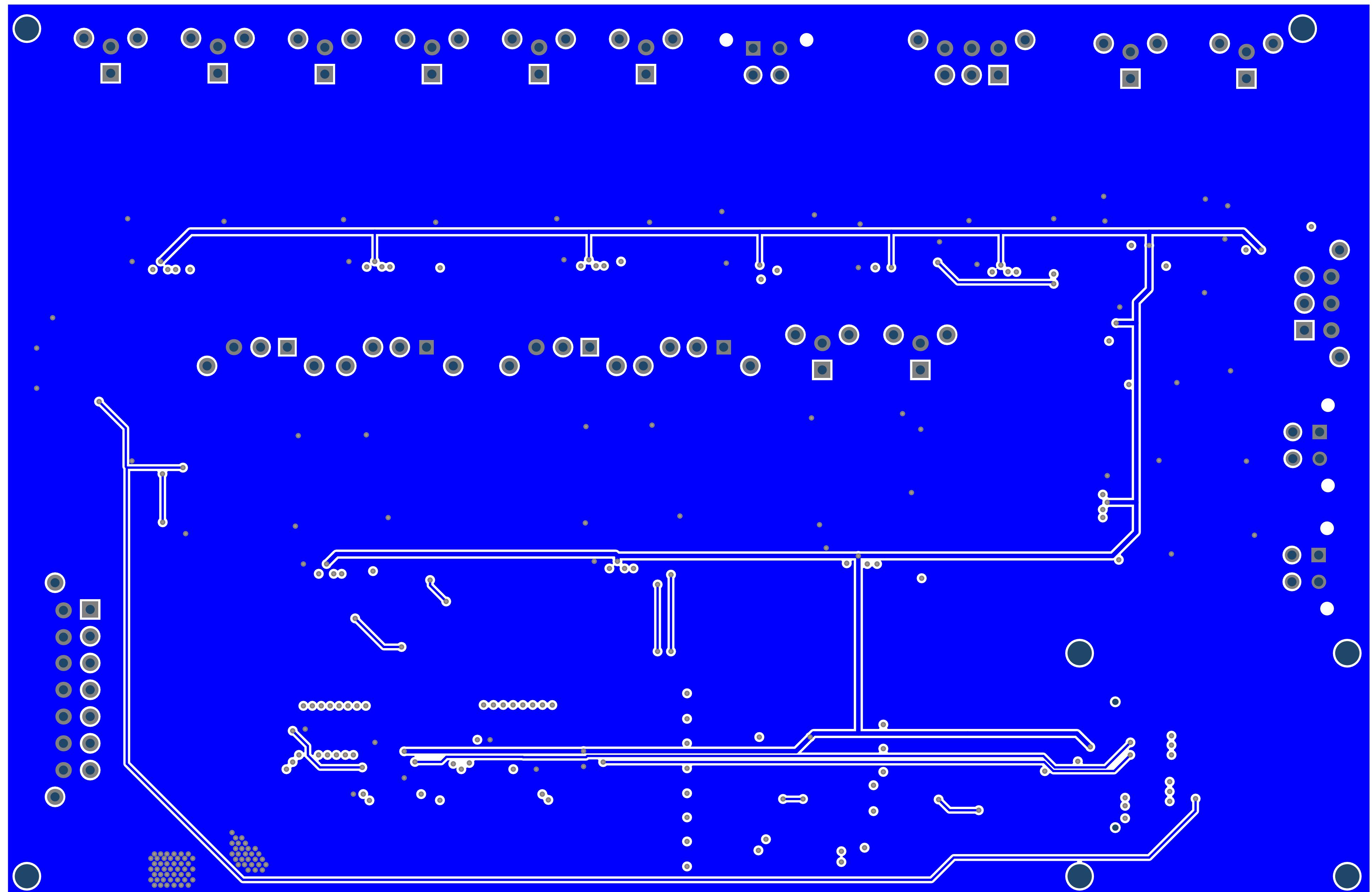
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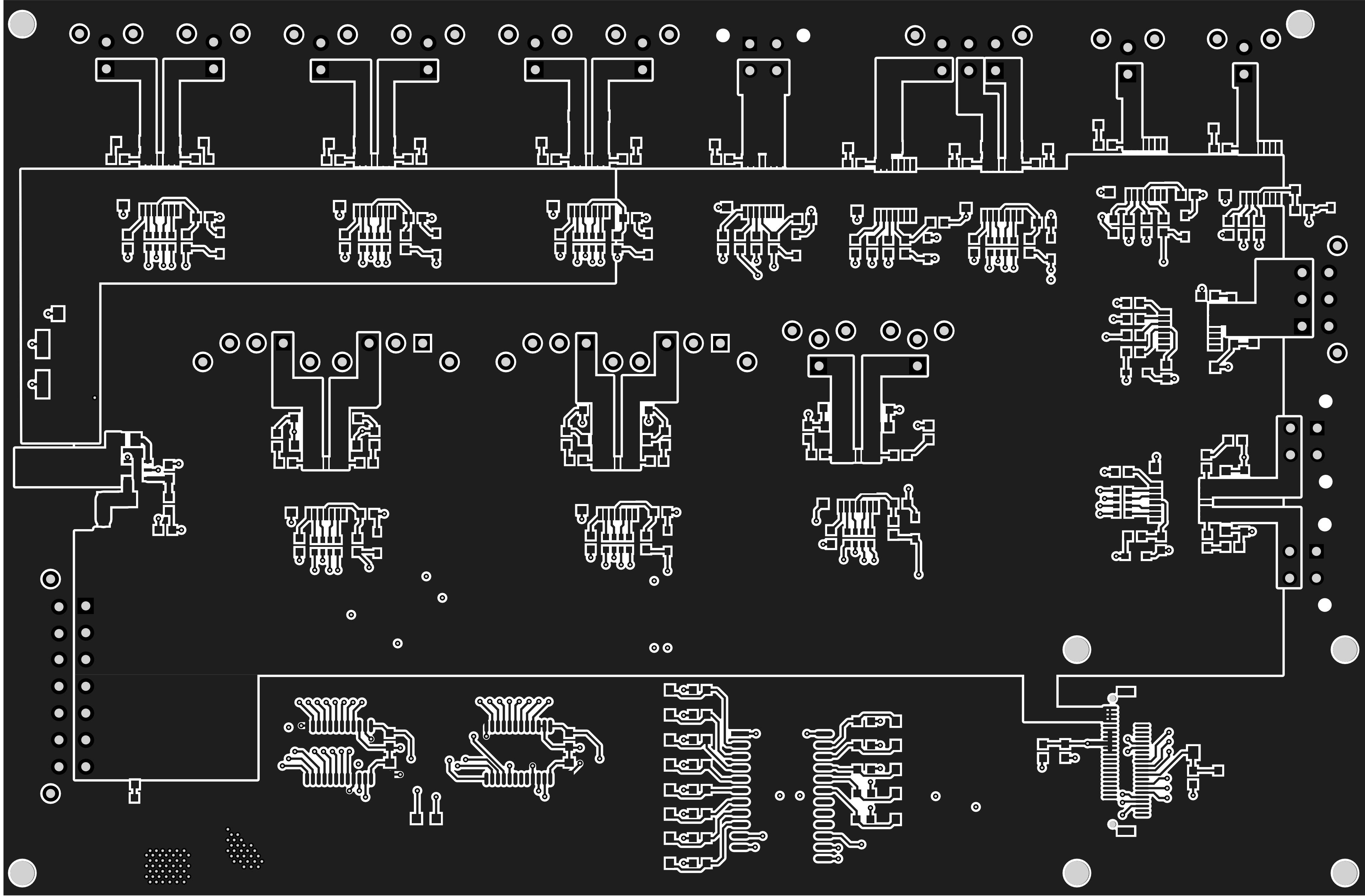


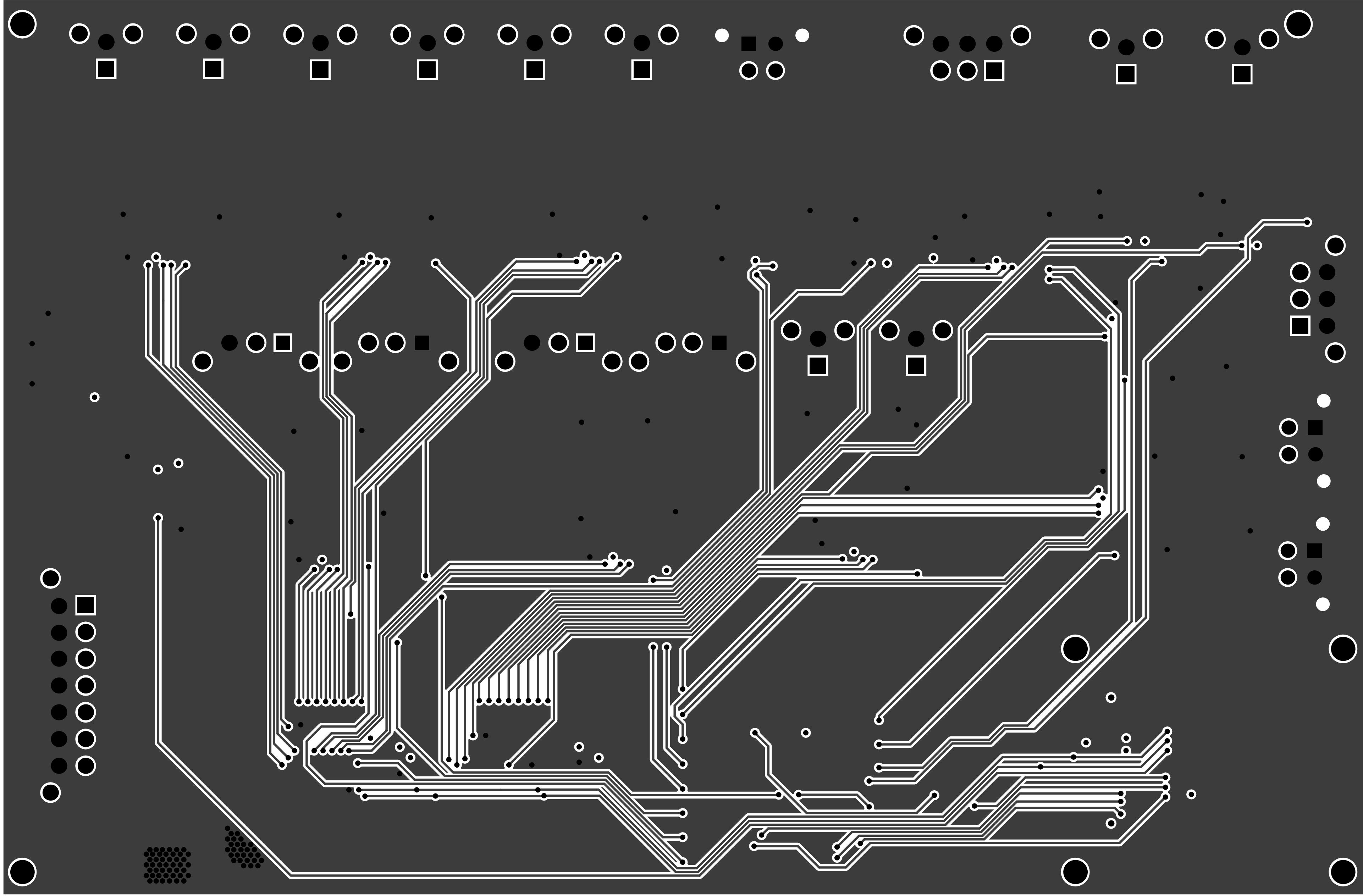


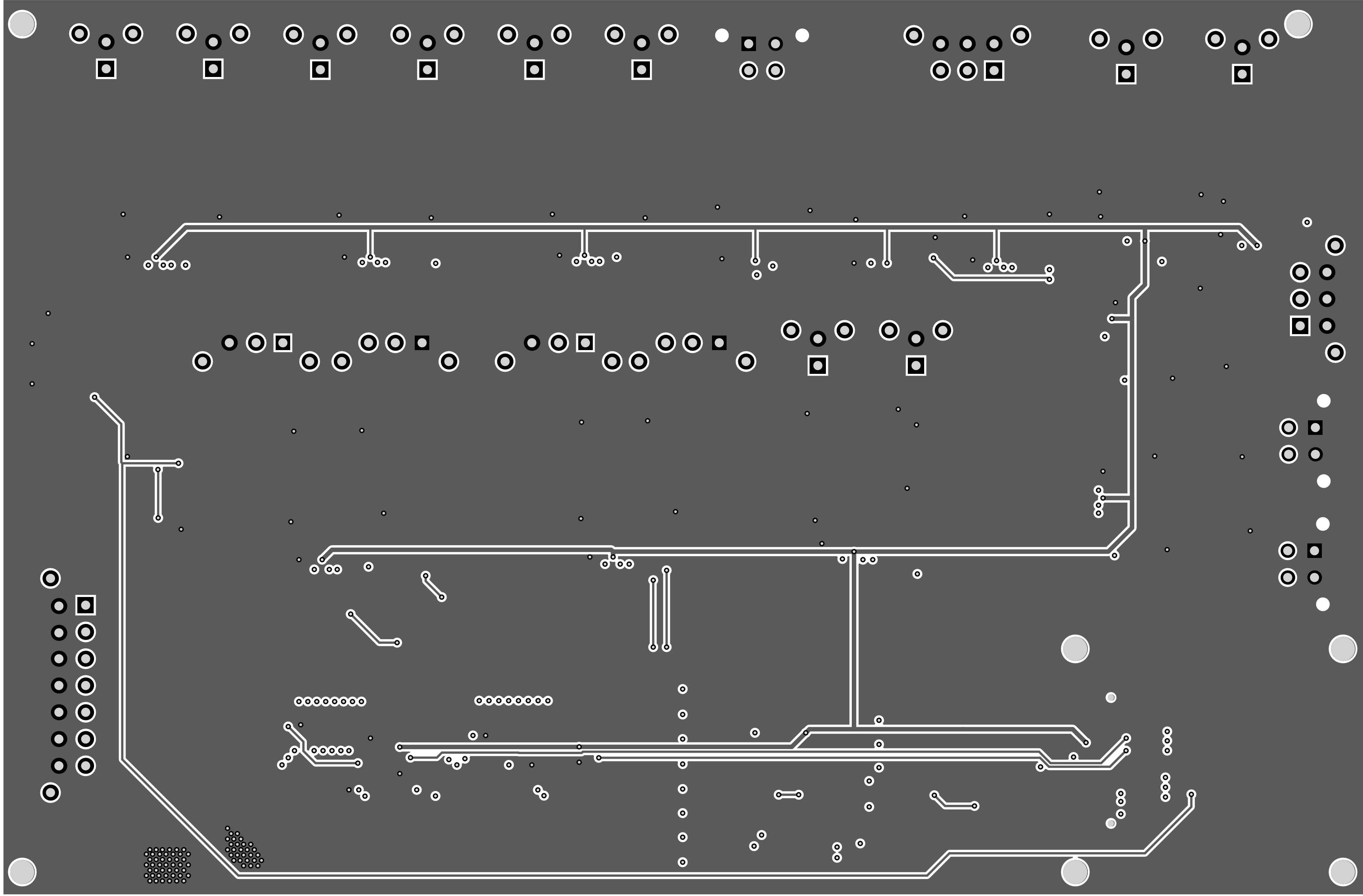


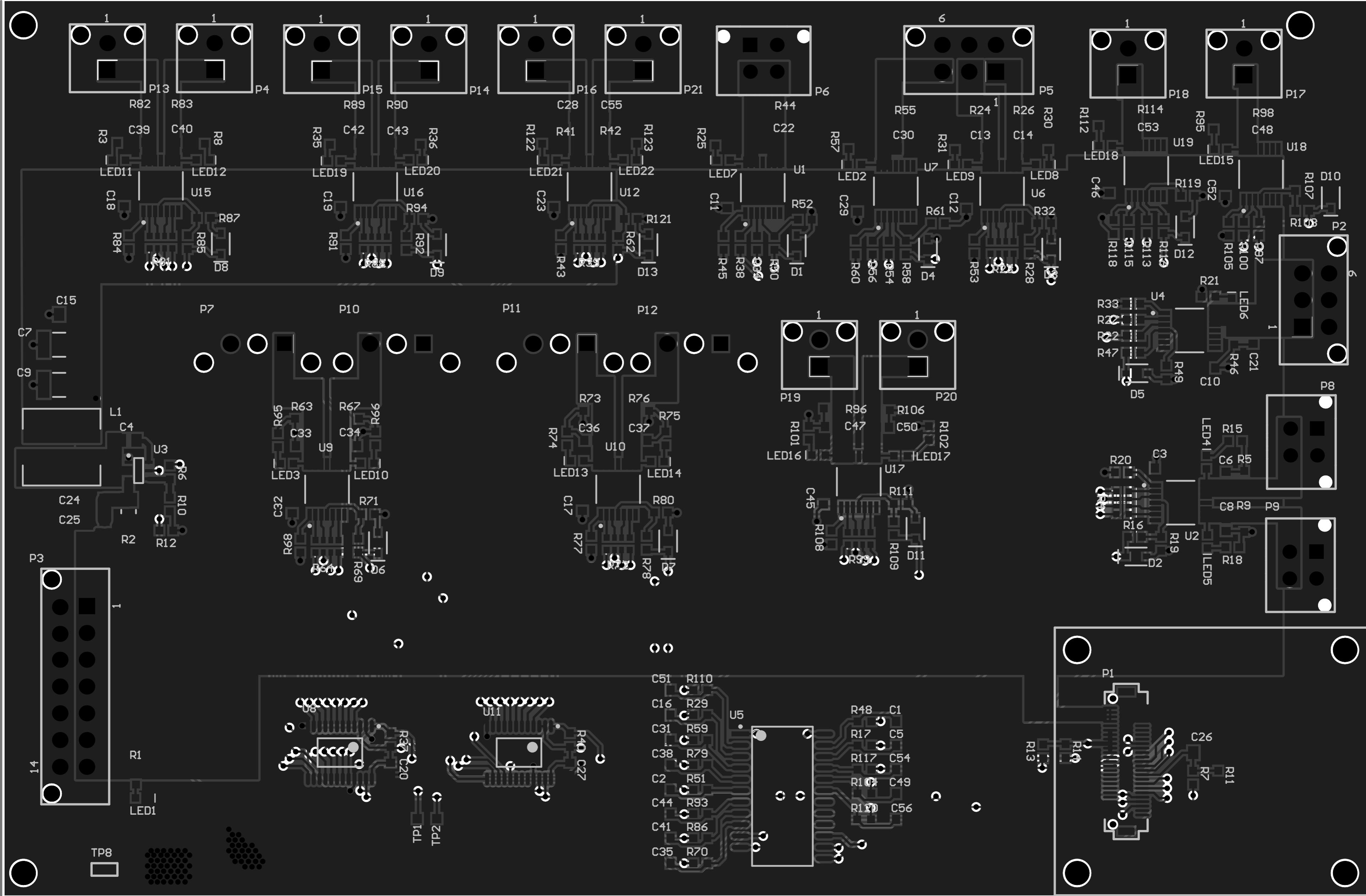












Bill of Materials

Project:	SXIV_Front_Pow er_Distribution.PrjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2020-02-19 10:45 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	254



Design Rules Verification Report

Filename : D:\Josh9\Documents\Midnight Sun\hardware\MSXIV_FrontPowerDistribution\Fr

Warnings 0
Rule Violations 373

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All), (All)	206
Silk To Solder Mask (Clearance=0.254mm) (IsPad), (All)	136
Silk to Silk (Clearance=0.254mm) (All), (All)	24
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	373

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(120.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(120.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(145.5mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(150.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(150.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (110.762mm,71.438mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.254mm) Between Arc (124.438mm,45.338mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (16.562mm,72.038mm) on Top Overlay And Pad R81-1(16.62mm,72.5mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (35.162mm,37.938mm) on Top Overlay And Pad R64-1(35.22mm,38.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (40.562mm,71.938mm) on Top Overlay And Pad R88-1(40.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (44.562mm,71.938mm) on Top Overlay And Pad R39-1(44.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (67.762mm,38.238mm) on Top Overlay And Pad R72-1(67.82mm,38.7mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (94.762mm,38.838mm) on Top Overlay And Pad R99-1(94.82mm,39.3mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad D2-1(128.296mm,37.968mm) on Component Side And Text "D2"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED10-2(41.75mm,48.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED11-2(12.45mm,82.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(16.55mm,10.91mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED12-2(23.35mm,82.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED13-2(63.75mm,48.69mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED14-2(74.25mm,48.61mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED15-2(135.85mm,83.59mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED16-2(90.8mm,49.34mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED17-2(101.5mm,49.26mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.215mm < 0.254mm) Between Pad LED18-1(124.45mm,83.99mm) on Component Side And Text "LED18"
Silk To Solder Mask Clearance Constraint: (0.215mm < 0.254mm) Between Pad LED18-2(122.95mm,83.99mm) on Component Side And Text "LED18"
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED18-2(122.95mm,83.99mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED19-2(36.55mm,82.29mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED20-2(47.15mm,82.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED21-2(60.75mm,82.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED2-2(94.85mm,81.89mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED22-2(71.15mm,82.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED3-2(31.25mm,48.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED4-2(135mm,49.3mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED5-2(135.1mm,38.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED6-2(137.8mm,66.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED7-2(80.15mm,82.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED8-2(117.35mm,81.91mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED9-2(106.75mm,81.89mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(127.8mm,21mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(127.8mm,9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(124.2mm,9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P13-0(14.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P13-0(14.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P13-0(8.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P13-0(8.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P14-0(44.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P14-0(44.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P14-0(50.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P14-0(50.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(124.2mm,21mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P15-0(32.9mm,96.34mm) on Multi-Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U3-2(14.275mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U3-3(14.275mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U3-3(14.275mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U3-4(16.525mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U3-4(16.525mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U3-5(16.525mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U3-6(16.525mm,48.55mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U3-6(16.525mm,48.55mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-1(82.8mm,18.085mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-10(82.8mm,6.655mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-11(82.8mm,5.385mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-12(82.8mm,4.115mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-13(92.2mm,4.115mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-14(92.2mm,5.385mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-15(92.2mm,6.655mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-16(92.2mm,7.925mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-17(92.2mm,9.195mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-18(92.2mm,10.465mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-19(92.2mm,11.735mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-2(82.8mm,16.815mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-20(92.2mm,13.005mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-21(92.2mm,14.275mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-22(92.2mm,15.545mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-23(92.2mm,16.815mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U5-24(92.2mm,18.085mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-3(82.8mm,15.545mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-4(82.8mm,14.275mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-5(82.8mm,13.005mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-6(82.8mm,11.735mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-7(82.8mm,10.465mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-8(82.8mm,9.195mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U5-9(82.8mm,7.925mm) on Component Side And Track

Silk To Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (102.45mm,64.65mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (11.7mm,97.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (126mm,97.3mm) on Top Overlay And Track (122mm,97mm)(130.4mm,97mm)
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (13.3mm,32.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (139mm,97.3mm) on Top Overlay And Track (135mm,97mm)(143.4mm,97mm)
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (142mm,63.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (23.7mm,97.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (35.7mm,97.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (47.7mm,97.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (59.7mm,97.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (71.7mm,97.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (91.45mm,64.65mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "14" (4.1mm,13.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "6" (150.95mm,69.95mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.125mm < 0.254mm) Between Text "D2" (128.596mm,36.868mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "D3" (116.9mm,69.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.025mm < 0.254mm) Between Text "D8" (24mm,70mm) on Top Overlay And Track (23.85mm,71mm)(25.35mm,71mm)
Silk To Silk Clearance Constraint: (0.197mm < 0.254mm) Between Text "LED15" (134.3mm,82mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.097mm < 0.254mm) Between Text "LED18" (121.4mm,82.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "LED20" (45.325mm,80.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.193mm < 0.254mm) Between Text "LED22" (69.3mm,80.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.193mm < 0.254mm) Between Text "LED8" (115.4mm,80.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.251mm < 0.254mm) Between Text "P20" (104.8mm,55.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "P20" (104.8mm,55.5mm) on Top Overlay And Track