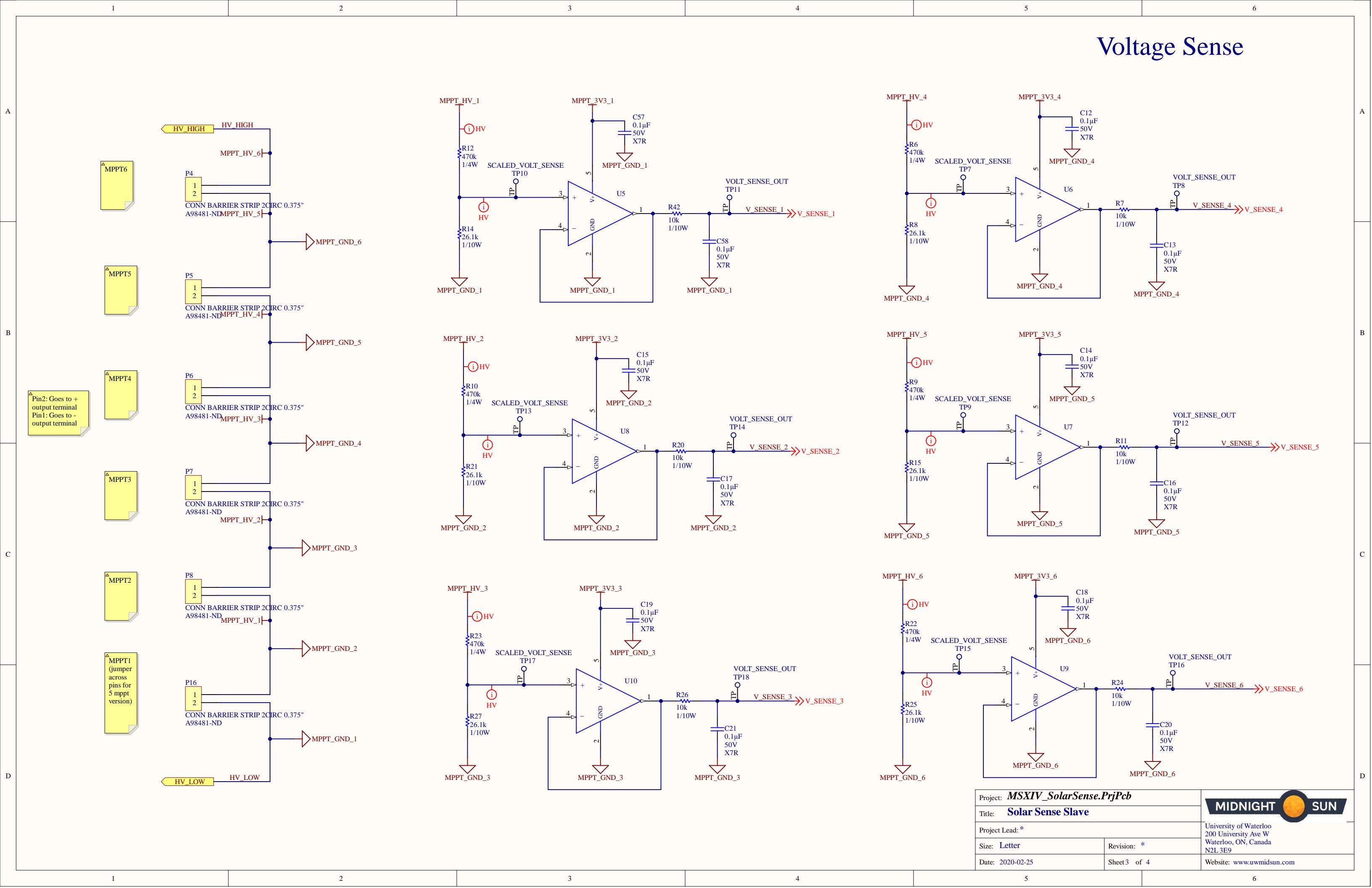
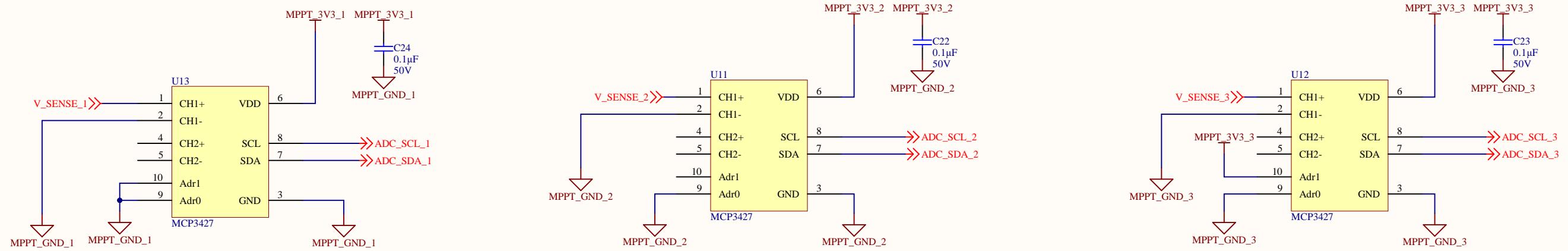


# Voltage Sense

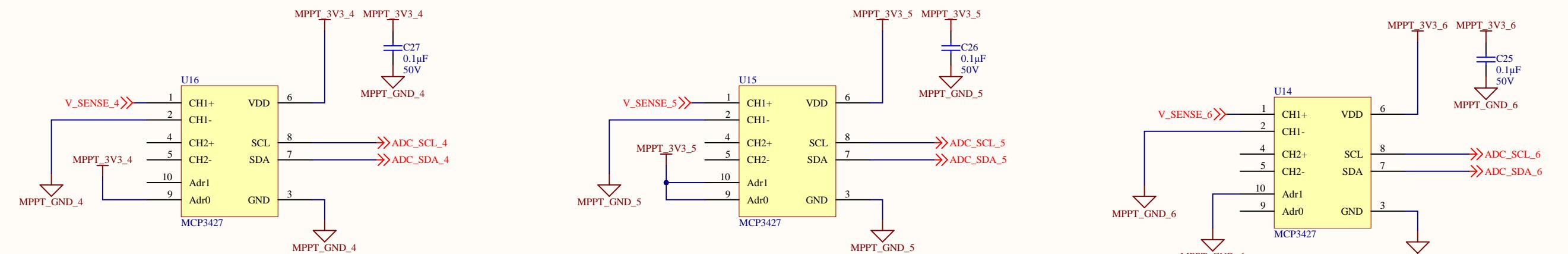


A



I <sup>2</sup> C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float

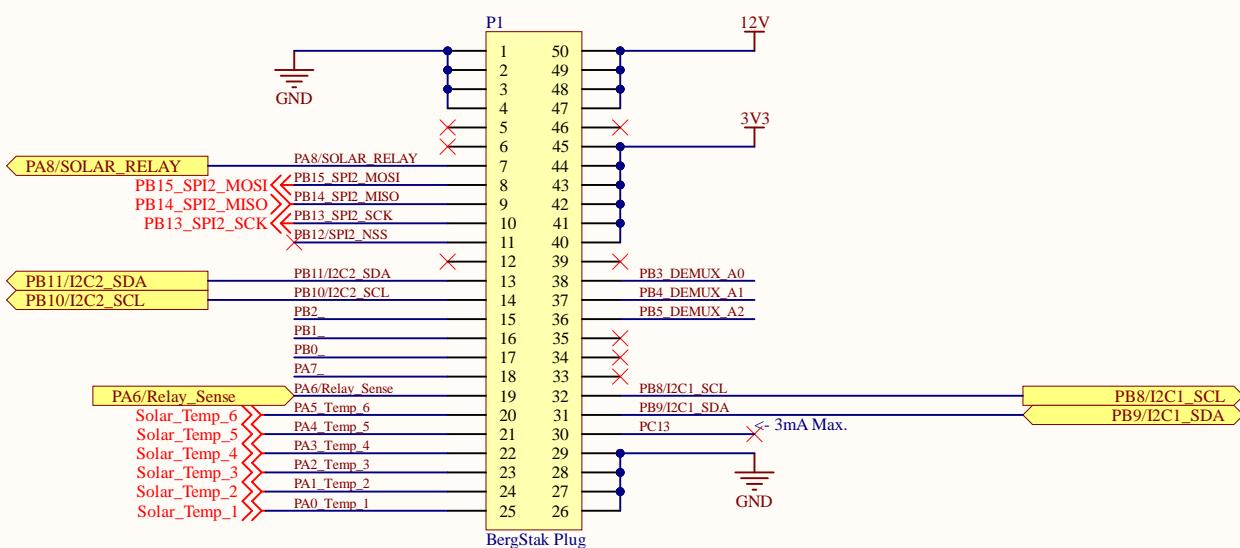
## ADCs



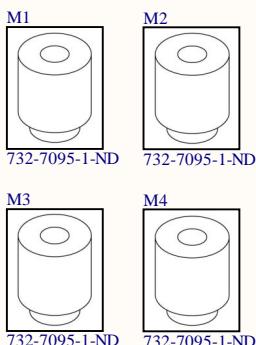
Make combination of pulled high, low and floating (for address pins)

PROJECT	MSXIV_SolarSense.PrjPcb	MIDNIGHT SUN
DOCUMENT	*	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY Aashmika Mali	REVISION 1.0	
LAST MODIFIED 2020-02-25	SHEET * OF *	

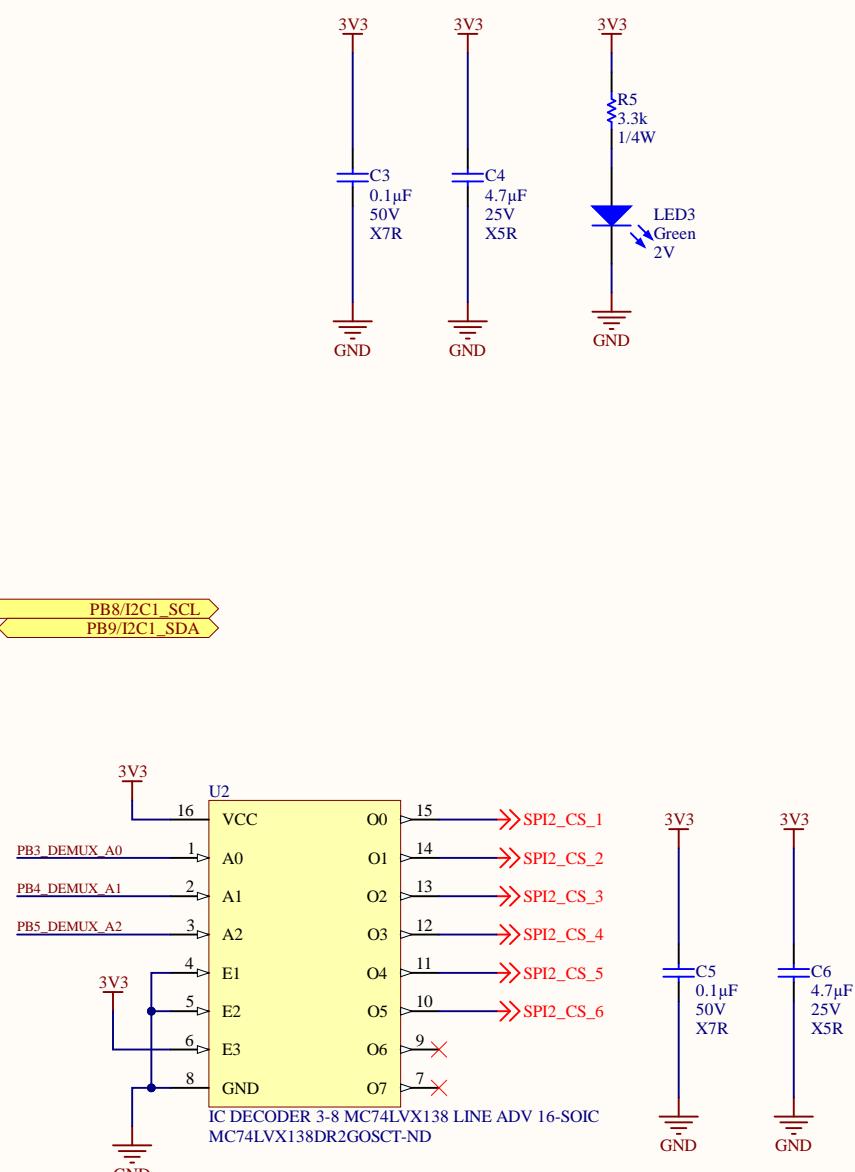
# Controller Board



## Standoffs



Solar Sense Rev 1.0  
MSXIV LOGO  
MSXIV\_LOGO



Project: **MSXIV\_SolarSense.PpjPcb**

Title: \*

Project Author: Aashmika Mali

Size: Letter

Revision: 1.0

Date: 2020-02-25

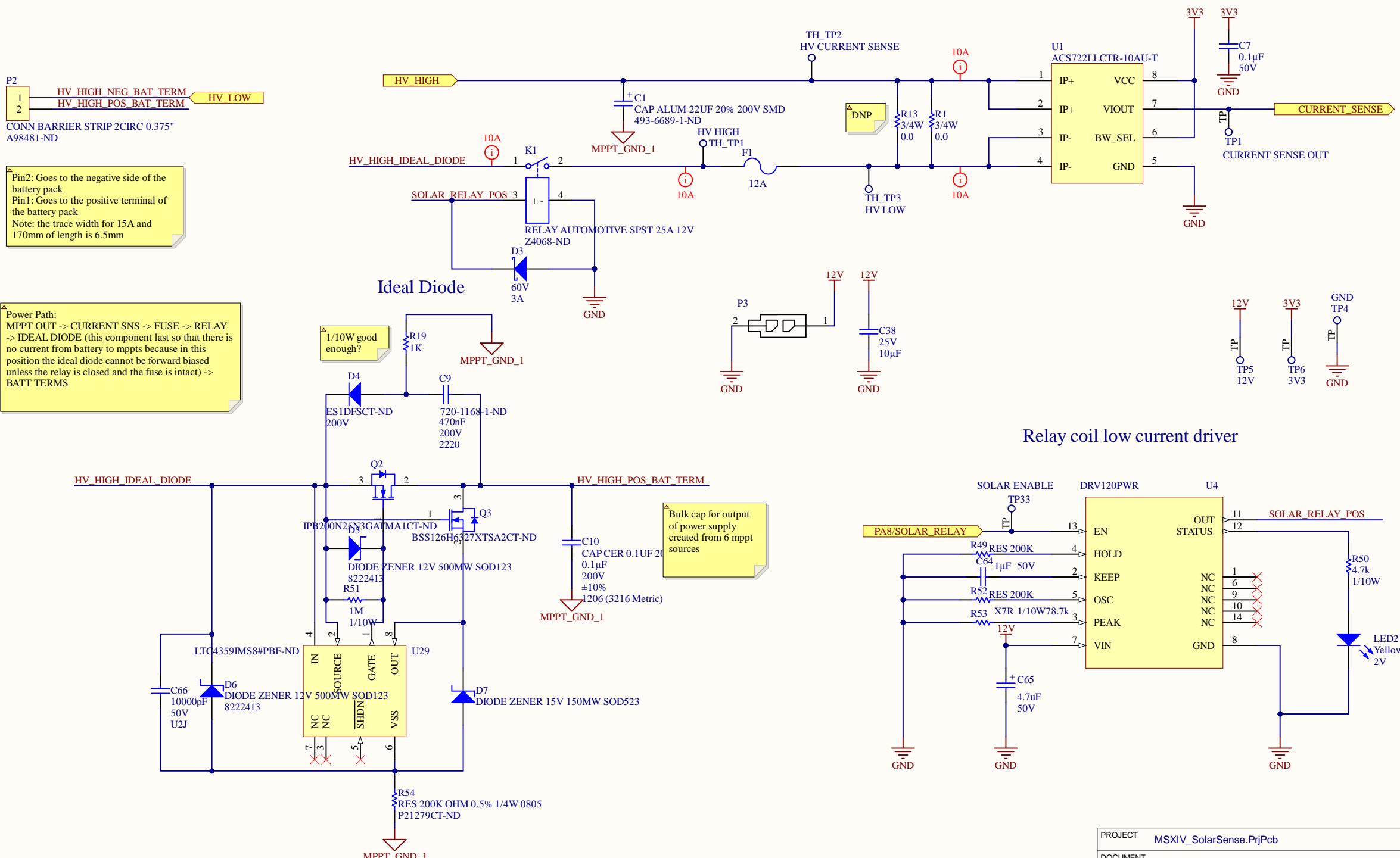
Sheet\* of \*

**MIDNIGHT SUN**

University of Waterloo  
200 University Ave W  
Waterloo, ON, Canada  
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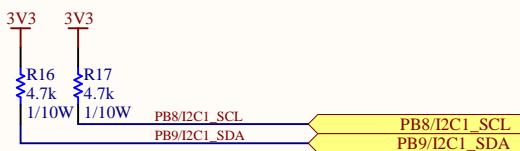
## Passthrough - Current Sense, Fuse, and Relay



PROJECT	MSXIV_SolarSense.PrjPcb		
DOCUMENT	*		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-25	SHEET	*

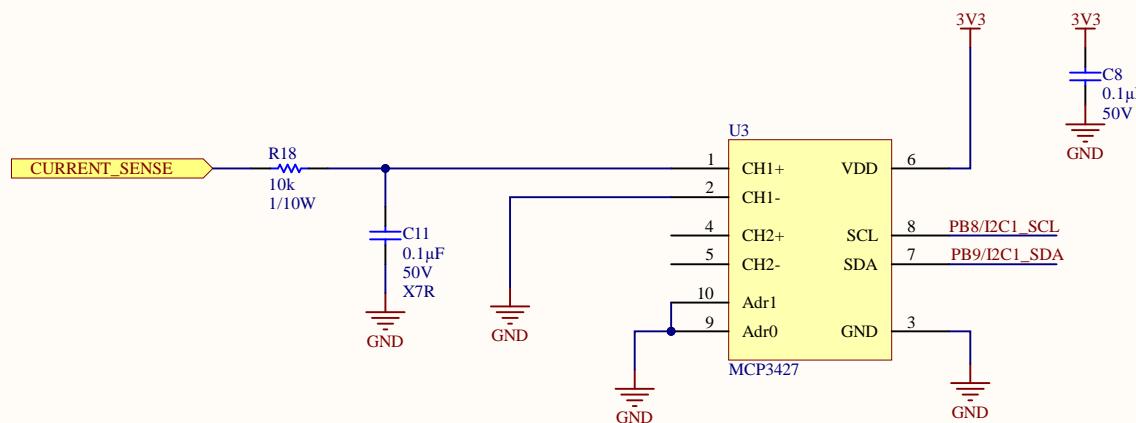
## I2C Interface (for Current Sense)

A



A

B



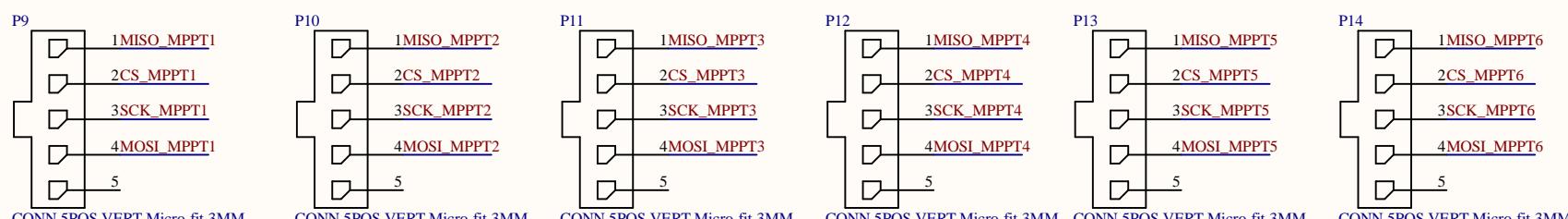
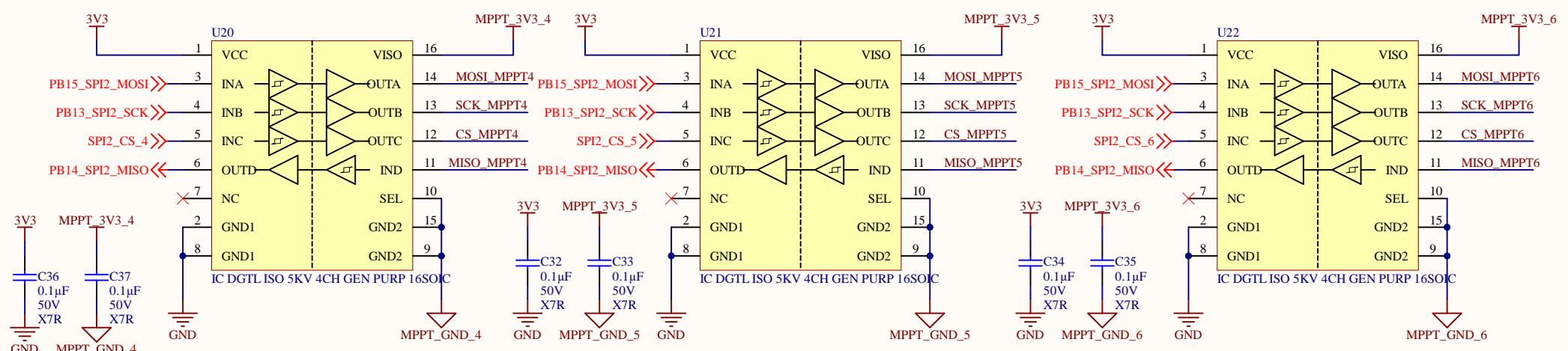
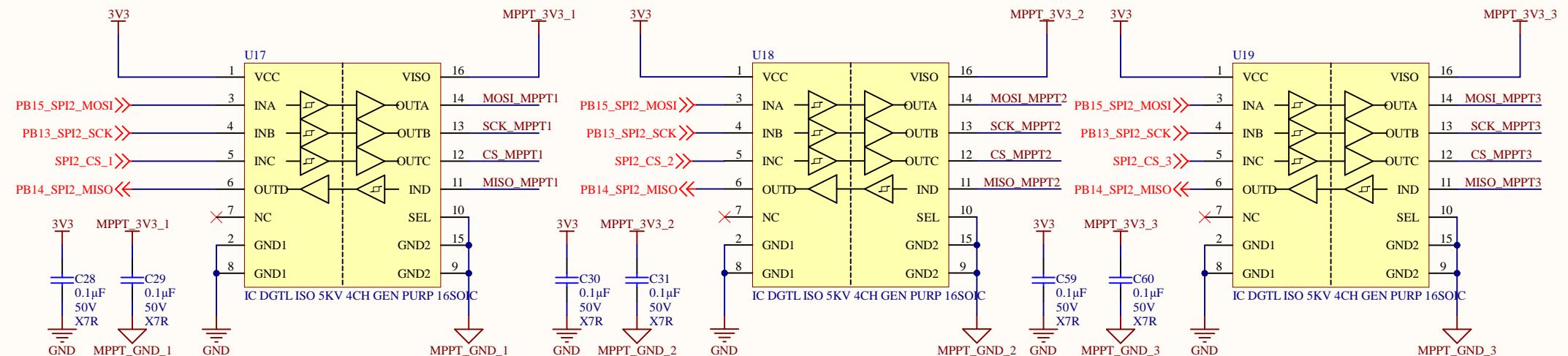
B

C

D

Project: <b><i>MSXIV_SolarSense.PjPcb</i></b>			
Title: *			
Project Author: <a href="#">Aashmika Mali</a>			
Size: Letter	Revision: 1.0		
Date: 2020-02-25	Sheet* of *	Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>	

# SPI Isolators



PROJECT	MSXIV_SolarSense.PrbPcb	MIDNIGHT SUN
DOCUMENT	*	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	Aashmika Mali	
REVISION	1.0	
LAST MODIFIED	2020-02-25	SHEET * OF *

## Temperature Sense for Array Sections

A

A

B

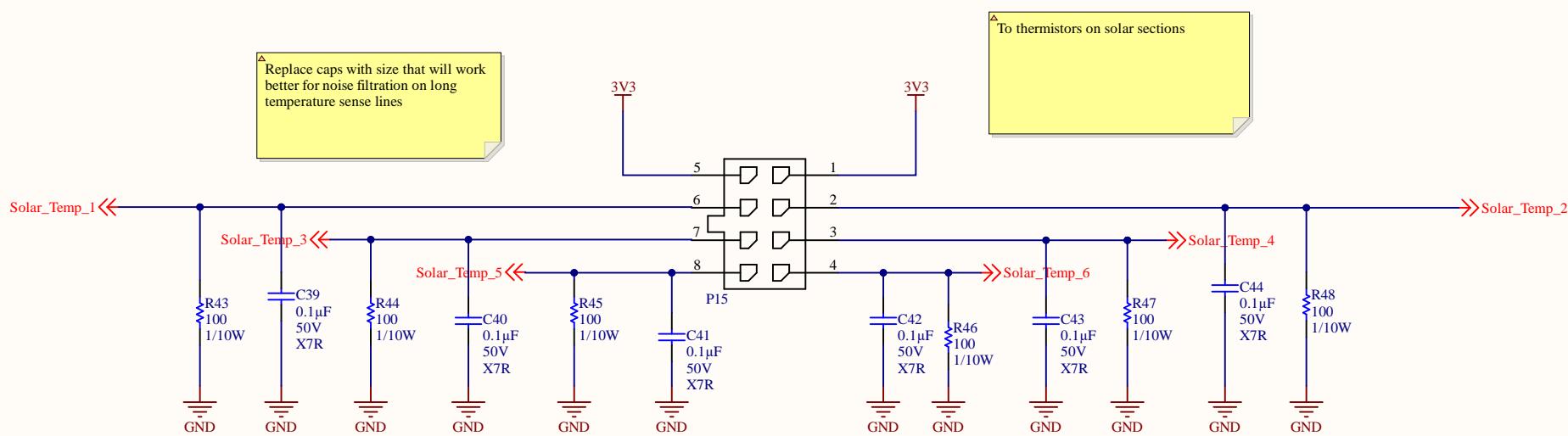
B

C

C

D

D

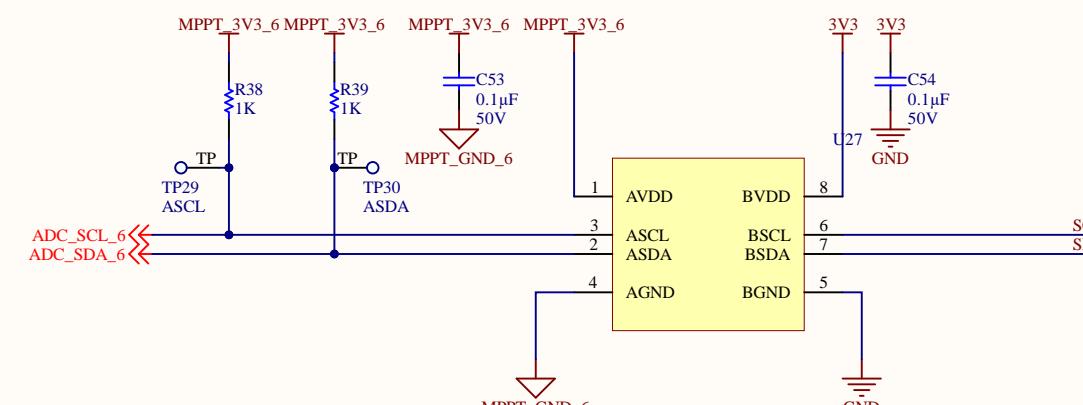
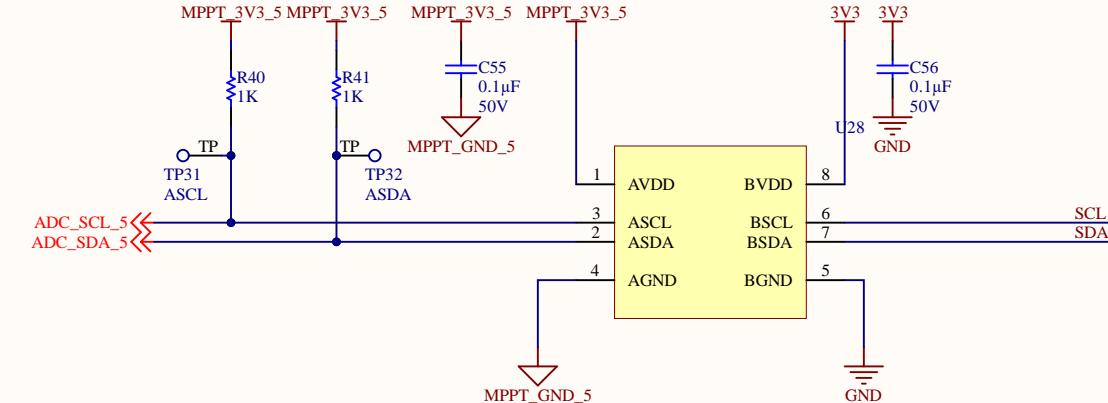
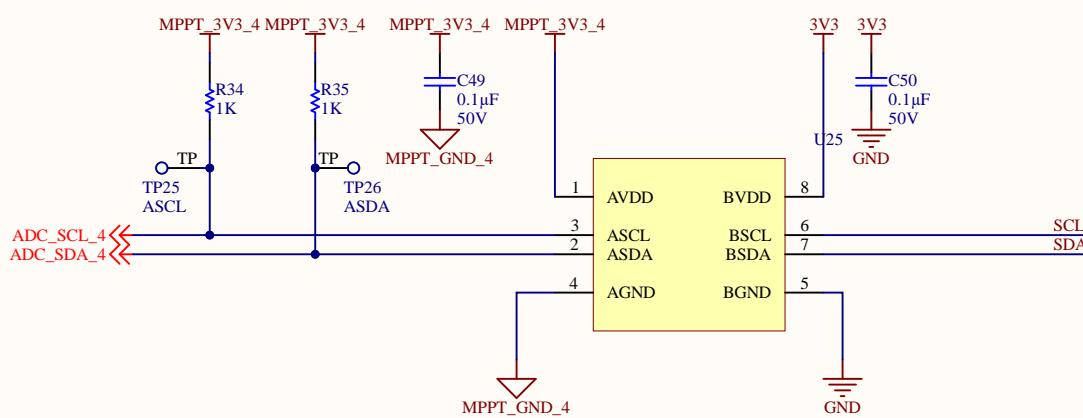
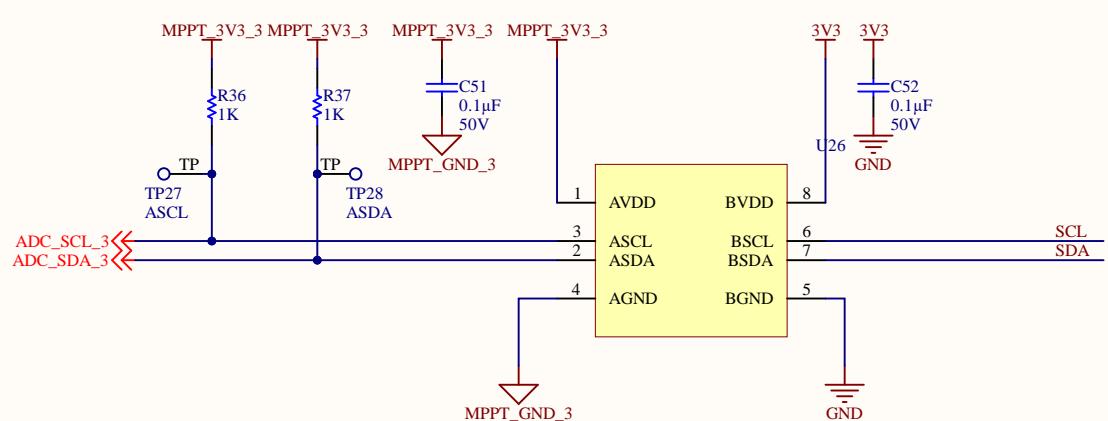
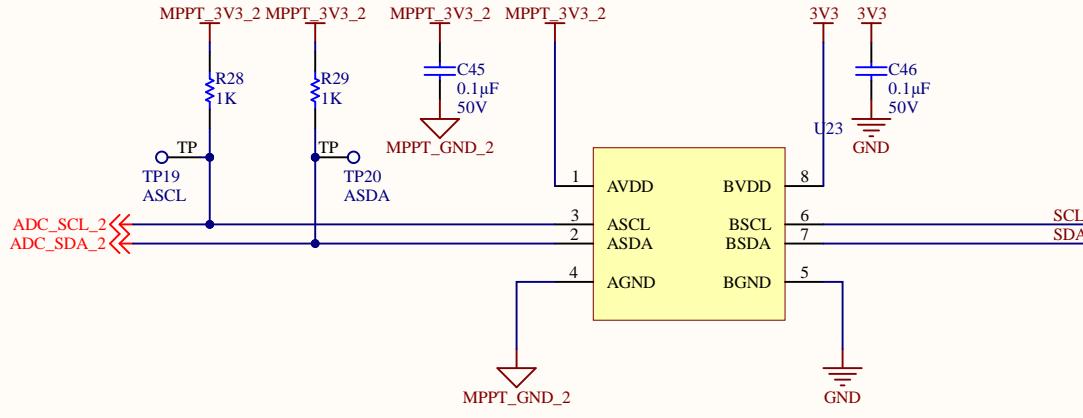
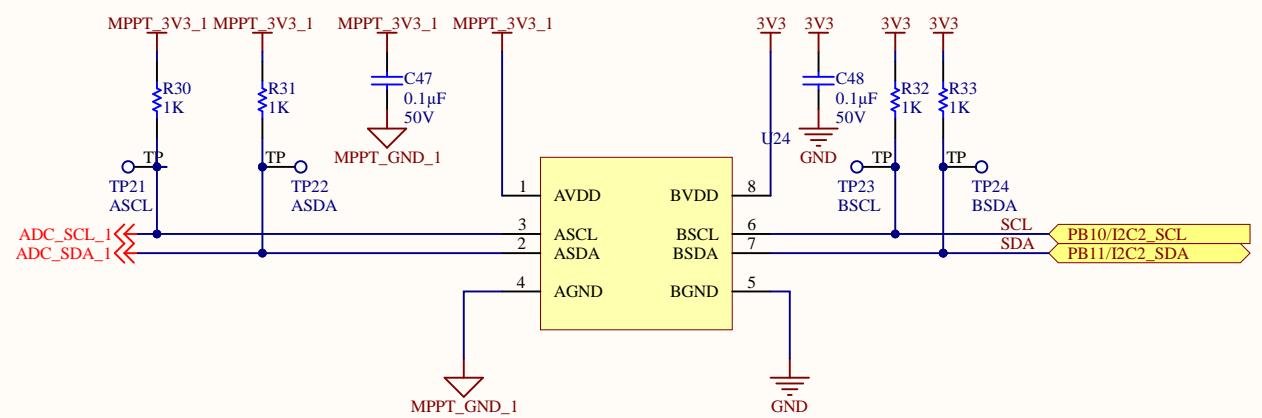


Project: <b><i>MSXIV_SolarSense.PrjPcb</i></b>	
Title: *	
Project Author: <a href="#">Aashmika Mali</a>	
Size: Letter	Revision: 1.0
Date: 2020-02-25	Sheet * of *
Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>	



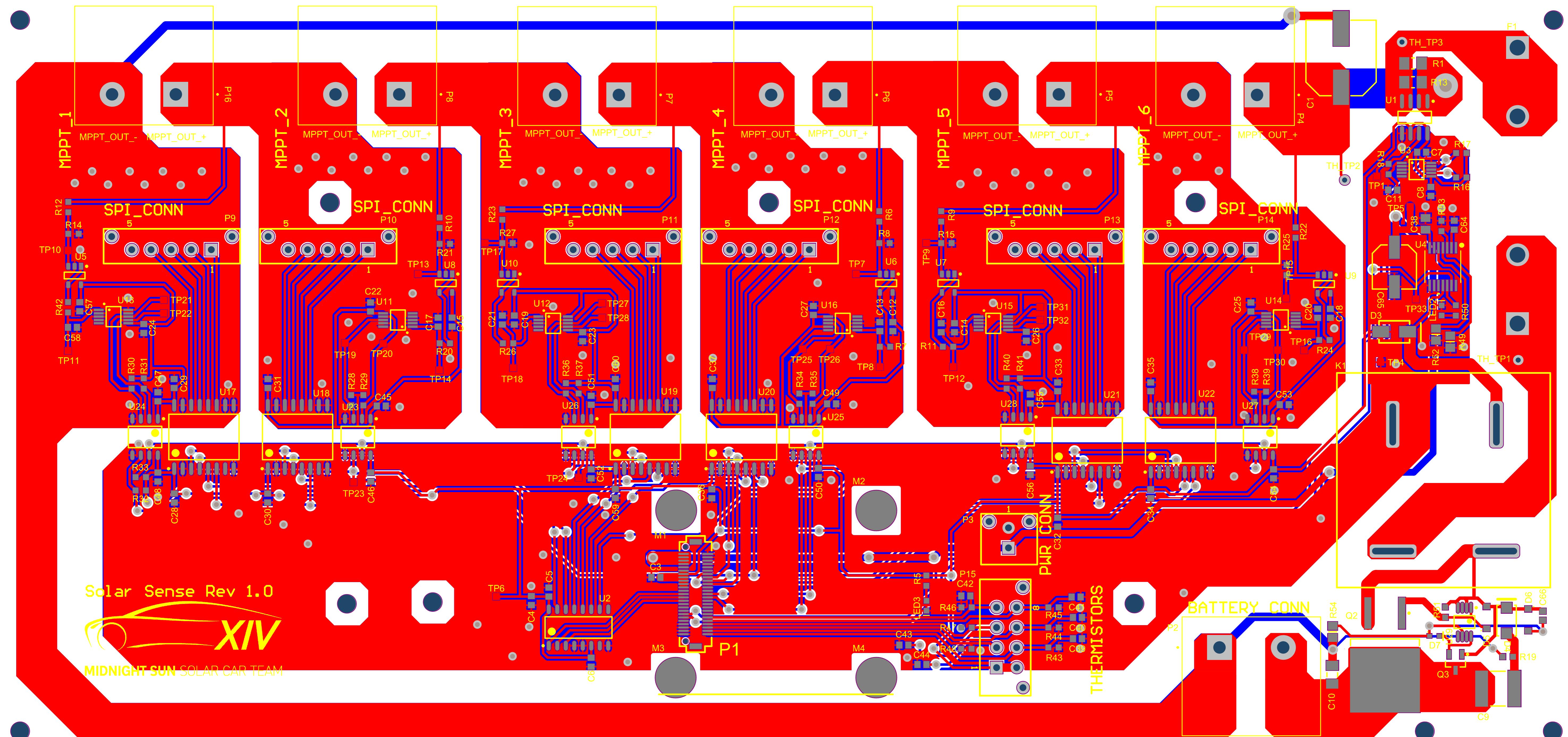
University of Waterloo  
200 University Ave W  
Waterloo, ON, Canada  
N2L 3E9

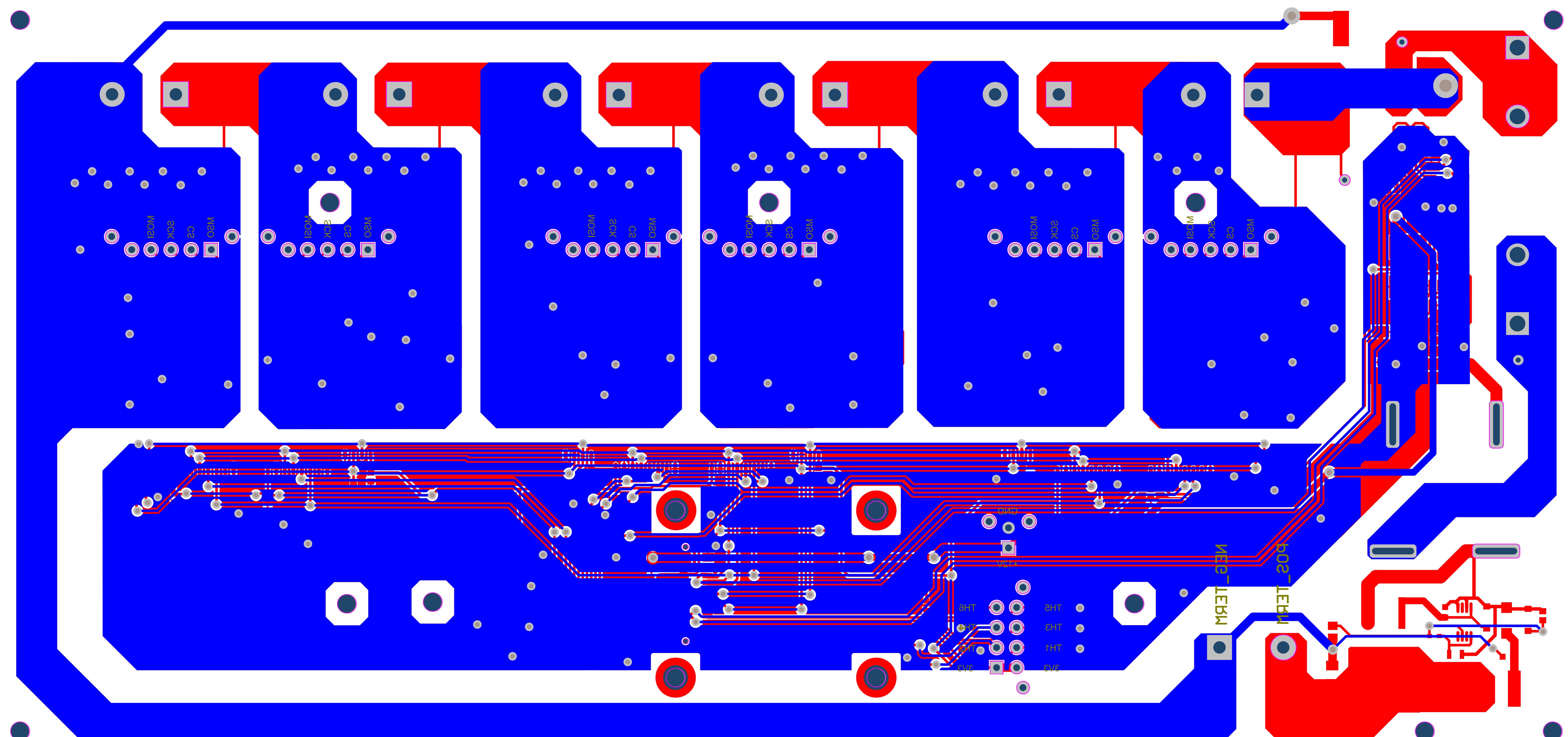
## I<sup>2</sup>C Isolators for V-Sense

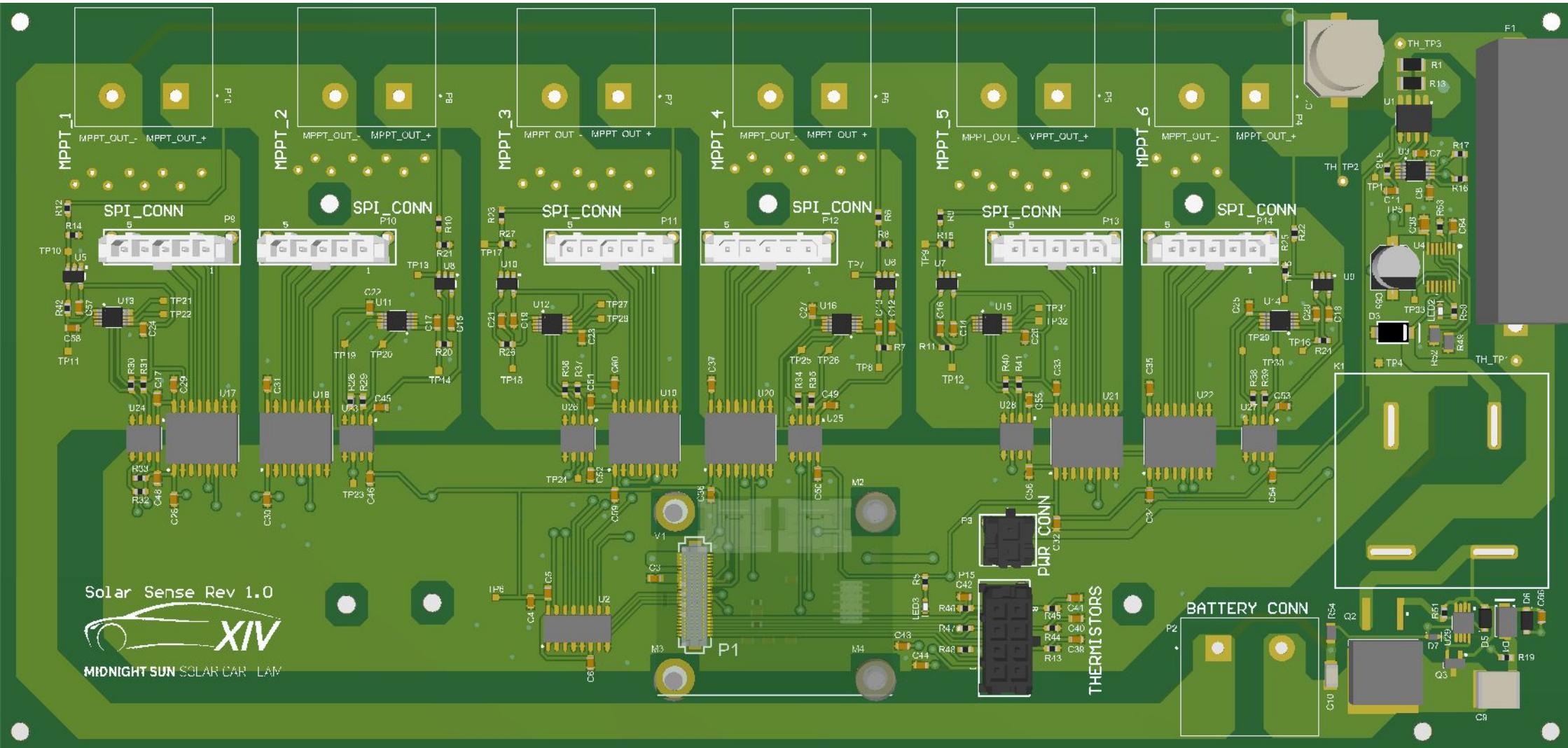


PROJECT	MSXIV_SolarSense.PrjPcb
DOCUMENT	*
PART NUMBER	VARIANT [No Variations]
DRAWN BY	Aashmika Mali
LAST MODIFIED	2020-02-25
SHEET *	OF *

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# Electrical Rules Check Report

Class	Document	Message
Error	Voltage_Sense.SchDoc	HV_LOW contains Power Pin and Output Port objects (Pin U5-2, Port HV_LOW).
Error	Controller_Board_Interface.SchDoc	Net PA6/Relay_Sense has only one pin (Pin P1-19)
Error	Controller_Board_Interface.SchDoc	Net PA7_ has only one pin (Pin P1-18)
Error	Controller_Board_Interface.SchDoc	Net PB0_ has only one pin (Pin P1-17)
Error	Controller_Board_Interface.SchDoc	Net PB1_ has only one pin (Pin P1-16)
Error	Controller_Board_Interface.SchDoc	Net PB2_ has only one pin (Pin P1-15)
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_GND_1 at 3650mil,1830mil has been reduced to local level by presence of port at 2000mil,1300mil
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_HV_6 at 3350mil,9100mil has been reduced to local level by presence of port at 2000mil,9400mil
Warning	Controller_Board_Interface.SchDoc	Net 12V has no driving source (Pin C38-1, Pin C65-1, Pin P1-47, Pin P1-48, Pin P1-49, Pin P1-50, Pin P3-1, Pin TP5-TP, Pin U4-7)
Warning	Current_and_Relay_Sense.SchDoc	Net NetC64_2 has no driving source (Pin C64-2, Pin U4-2)
Warning	Current_and_Relay_Sense.SchDoc	Net NetD7_2 has no driving source (Pin D7-2, Pin Q3-2, Pin U29-8)
Warning	Voltage_Sense.SchDoc	Net NetR6_2 has no driving source (Pin R6-2, Pin R8-1, Pin TP7-TP, Pin U6-3)
Warning	Voltage_Sense.SchDoc	Net NetR9_2 has no driving source (Pin R9-2, Pin R15-1, Pin TP9-TP, Pin U7-3)
Warning	Voltage_Sense.SchDoc	Net NetR10_2 has no driving source (Pin R10-2, Pin R21-1, Pin TP13-TP, Pin U8-3)
Warning	Voltage_Sense.SchDoc	Net NetR12_2 has no driving source (Pin R12-2, Pin R14-1, Pin TP10-TP, Pin U5-3)
Warning	Voltage_Sense.SchDoc	Net NetR22_2 has no driving source (Pin R22-2, Pin R25-1, Pin TP15-TP, Pin U9-3)
Warning	Voltage_Sense.SchDoc	Net NetR23_2 has no driving source (Pin R23-2, Pin R27-1, Pin TP17-TP, Pin U10-3)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR49_2 has no driving source (Pin R49-2, Pin U4-4)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR52_2 has no driving source (Pin R52-2, Pin U4-5)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR53_2 has no driving source (Pin R53-2, Pin U4-3)
Warning	Controller_Board_Interface.SchDoc	Net PB3_DEMUX_A0 has no driving source (Pin P1-38, Pin U2-1)
Warning	Controller_Board_Interface.SchDoc	Net PB4_DEMUX_A1 has no driving source (Pin P1-37, Pin U2-2)
Warning	Controller_Board_Interface.SchDoc	Net PB5_DEMUX_A2 has no driving source (Pin P1-36, Pin U2-3)
Warning	Current_and_Relay_Sense.SchDoc	Nets Wire HV_HIGH has multiple names (Net Label HV_HIGH, Power Object MPPT_HV_6, Power Object MPPT_HV_6)
Warning	ADCs.SchDoc	Nets Wire HV_HIGH_NEG_BAT_TERM has multiple names (Net Label HV_HIGH_NEG_BAT_TERM, Net Label HV_LOW, Power Object MPPT_GND_1, Power Object MPPT_GND_1)
Warning	ADCs.SchDoc	<del>Net Label MPPT_GND_2</del> has multiple names (Power Object MPPT_GND_2, Power Object MPPT_GND_2)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_3 has multiple names (Power Object MPPT_GND_3, Power Object MPPT_GND_3)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_4 has multiple names (Power Object MPPT_GND_4, Power Object MPPT_HV_3)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_5 has multiple names (Power Object MPPT_GND_5, Power Object MPPT_GND_5)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_6 has multiple names (Power Object MPPT_GND_6, Power Object MPPT_GND_6)

Class	Document	Message
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA0_Temp_1 has multiple names (Cross-Sheet Connector Solar_Temp_1, Cross-Sheet Connector Solar_Temp_1, Net Label PA0_Temp_1)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA1_Temp_2 has multiple names (Cross-Sheet Connector Solar_Temp_2, Cross-Sheet Connector Solar_Temp_2, Net Label PA1_Temp_2)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA2_Temp_3 has multiple names (Cross-Sheet Connector Solar_Temp_3, Cross-Sheet Connector Solar_Temp_3, Net Label PA2_Temp_3)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA3_Temp_4 has multiple names (Cross-Sheet Connector Solar_Temp_4, Cross-Sheet Connector Solar_Temp_4, Net Label PA3_Temp_4)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA4_Temp_5 has multiple names (Cross-Sheet Connector Solar_Temp_5, Cross-Sheet Connector Solar_Temp_5, Net Label PA4_Temp_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA5_Temp_6 has multiple names (Cross-Sheet Connector Solar_Temp_6, Cross-Sheet Connector Solar_Temp_6, Net Label PA5_Temp_6)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB10/I2C2_SCL has multiple names (Net Label PB10/I2C2_SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB11/I2C2_SDA has multiple names (Net Label PB11/I2C2_SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA)
Warning	ADCs.SchDoc	Off grid C24 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SCL_1 at 3600mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SDA_1 at 3600mil,7544.41mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB13_SPI2_SCK at 6574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB14_SPI2_MISO at 6574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB15_SPI2_MOSI at 6574.41mil,6851.811mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_2 at 9237.008mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_4 at 7437.008mil,4596.063mil
Warning	Controller_Board_Interface.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 2247.008mil,4300mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 6300mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_1 at 1350mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_2 at 6281.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_3 at 11381.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_4 at 1631.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_5 at 6531.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_6 at 11231.89mil,3400mil
Warning	Controller_Board_Interface.SchDoc	Off grid M1 at 1693.983mil,2899.713mil
Warning	Controller_Board_Interface.SchDoc	Off grid M2 at 2406.601mil,2898.306mil
Warning	Controller_Board_Interface.SchDoc	Off grid M3 at 1693.983mil,1949.714mil
Warning	Controller_Board_Interface.SchDoc	Off grid M4 at 2406.601mil,1948.306mil
Warning	SPI_Interface.SchDoc	Off grid Net Label CS_MPPT2 at 8674.41mil,6451.811mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid Net Label HV_HIGH_NEG_BAT_TERM at 998.148mil,7600mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT2 at 8624.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT3 at 12055.512mil,6250mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT2 at 8674.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT3 at 12055.512mil,6850mil
Warning	SPI_Interface.SchDoc	Off grid Net Label SCK_MPPT2 at 8674.41mil,6651.811mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid Net Label SOLAR_RELAY_POS at 11601.896mil,3900mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid NetParameter at 6495.503mil,7000mil
Warning	SPI_Interface.SchDoc	Off grid No ERC at 6774.41mil,6051.811mil
Warning	TemperatureSense.SchDoc	Off grid P15 at 4521.654mil,5096.063mil
Warning	ADCs.SchDoc	Off grid Pin C24-1 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Pin C24-2 at 3818.11mil,8374.41mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-1 at 5421.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-2 at 5421.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-3 at 5421.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-4 at 5421.654mil,4396.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-5 at 4521.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-6 at 4521.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-7 at 4521.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-8 at 4521.654mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Pin U13-1 at 1658.11mil,8044.41mil

Class	Document	Message
Warning	ADCs.SchDoc	Off grid Pin U13-2 at 1658.11mil,7894.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-3 at 3108.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-4 at 1658.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-5 at 1658.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-6 at 3108.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-7 at 3108.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-8 at 3108.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-9 at 1658.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-10 at 1658.11mil,7344.41mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-1 at 6774.41mil,7051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-2 at 6774.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-3 at 6774.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-4 at 6774.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-5 at 6774.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-6 at 6774.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-7 at 6774.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-8 at 6774.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-9 at 8574.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-10 at 8574.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-11 at 8574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-12 at 8574.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-13 at 8574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-14 at 8574.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-15 at 8574.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-16 at 8574.41mil,7051.811mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 4099.606mil,5389.764mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 5899.606mil,5389.764mil
Warning	SPI_Interface.SchDoc	Off grid Power Object 3V3 at 6174.41mil,7351.811mil
Warning	SPI_Interface.SchDoc	Off grid Power Object GND at 6774.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3218.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3818.11mil,8674.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_3V3_2 at 9074.41mil,7351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 818.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3468.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3818.11mil,8374.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_GND_2 at 8574.41mil,5351.811mil
Warning	Controller_Board_Interface.SchDoc	Off grid Solar Sense Rev 1.0 at 4505.679mil,2561.84mil
Warning	ADCs.SchDoc	Off grid U13 at 1958.11mil,8194.41mil
Warning	SPI_Interface.SchDoc	Off grid U18 at 7474.41mil,6651.811mil

## Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV\_

Warnings 0

Rule Violations 147

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=80mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Direct Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4'	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	23
Hole To Hole Clearance (Gap=10mil) (All),(All)	4
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	26
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	77
Silk to Silk (Clearance=10mil) (All),(All)	17
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	147

Hole Size Constraint (Min=1mil) (Max=100mil) (All)	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.11mil,-118.11mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-123.11mil,-4306.39mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-2225mil,-1193mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-2585.263mil,-3554.855mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4104.519mil,-3006.496mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4104.519mil,-3990.748mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4735.622mil,-1193mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-5285.622mil,-3006.496mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-5285.622mil,-3990.748mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-6715.249mil,-3545.712mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-7220.643mil,-3555.931mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-7320.284mil,-1193mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-876.173mil,-4306.39mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-9143.889mil,-4306.39mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-9143.89mil,-118.11mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-1(-456mil,-3245.5mil) on Multi-Layer Actual Slot Hole Height = 248.031mil	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-2(-1062.299mil,-3245.5mil) on Multi-Layer Actual Slot Hole Height = 248.031mil	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-3(-454.031mil,-2499.437mil) on Multi-Layer Actual Slot Hole Height = 248.031mil	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-4(-1064.267mil,-2499.437mil) on Multi-Layer Actual Slot Hole Height = 248.031mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M1-(-5282.468mil,-3005.091mil) on Multi-Layer Actual Hole Size = 145.669mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M2-(-4104.519mil,-3006.496mil) on Multi-Layer Actual Hole Size = 145.669mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M3-(-5285.622mil,-3990.748mil) on Multi-Layer Actual Hole Size = 145.669mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M4-(-4104.519mil,-3990.748mil) on Multi-Layer Actual Hole Size = 145.669mil	

Hole To Hole Clearance (Gap=10mil) (All),(All)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-4104.519mil,-3006.496mil) on Multi-Layer And Pad Free-(-4104.519mil,-3990.748mil)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-4104.519mil,-3990.748mil) on Multi-Layer And Pad Free-(-5285.622mil,-3990.748mil)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-5285.622mil,-3006.496mil) on Multi-Layer And Pad Free-(-5285.622mil,-3990.748mil)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-5285.622mil,-3990.748mil) on Multi-Layer And Pad Free-(-876.173mil,-4306.39mil)	

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-5167.511mil,-3191.536mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-5167.511mil,-3805.709mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U10-1(-6234.441mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U10-2(-6271.842mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-1(-692.728mil,-1459.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-10(-795.09mil,-1681.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-10(-795.09mil,-1681.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-11(-769.5mil,-1681.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-12(-743.909mil,-1681.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-13(-718.318mil,-1681.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-2(-718.318mil,-1459.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-3(-743.909mil,-1459.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-4(-769.5mil,-1459.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-5(-795.09mil,-1459.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-6(-820.681mil,-1459.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-8(-846.271mil,-1681.245mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U5-1(-8785.031mil,-1568.268mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U5-2(-8822.433mil,-1568.268mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U6-1(-4008.063mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U6-2(-4045.464mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U7-1(-3642.905mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U7-2(-3680.307mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U8-1(-6600.385mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U8-2(-6637.787mil,-1613.78mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U9-1(-1431.291mil,-1618.701mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U9-2(-1468.693mil,-1618.701mil) on Top Layer And Pac

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-235.11mil,-3572.744mil) on Top Overlay And Pad D6-1(-267mil,-3586.13mil)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-543.89mil,-3714.256mil) on Top Overlay And Pad D5-1(-512mil,-3700.87mil)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-858.37mil,-3721.878mil) on Top Overlay And Pac
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-1(-1368.446mil,-514.535mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-1(-1368.446mil,-514.535mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.709mil < 10mil) Between Pad C11-2(-1091.707mil,-1118.5mil) on Top Layer And Text "TP1"
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-2(-1368.446mil,-168.078mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-2(-1368.446mil,-168.078mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.995mil < 10mil) Between Pad C15-1(-6600.385mil,-1871.26mil) on Top Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (7.941mil < 10mil) Between Pad C15-2(-6600.385mil,-1924.409mil) on Top Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (9.475mil < 10mil) Between Pad C6-2(-5781.488mil,-3925.787mil) on Top Layer And Text "C6"
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-1(-1054.5mil,-1456.166mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-1(-1054.5mil,-1456.166mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-2(-1054.5mil,-1688.45mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-2(-1054.5mil,-1688.45mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-1(-1135.007mil,-1954.206mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-1(-1135.007mil,-1954.206mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-2(-977.527mil,-1954.206mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-2(-977.527mil,-1954.206mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (2.839mil < 10mil) Between Pad D7-2(-789.472mil,-3745.5mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED2-2(-777.301mil,-1798.209mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED3-2(-3809.244mil,-3597.047mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.408mil < 10mil) Between Pad M3(-5285.622mil,-3990.748mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.408mil < 10mil) Between Pad M4(-4104.519mil,-3990.748mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P10-0(-6974.598mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-6974.598mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-7683.26mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P10-0(-7683.26mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.78mil < 10mil) Between Pad P1-1(-5096.645mil,-3262.403mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P11-0(-5297.433mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-5297.433mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-6006.094mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P11-0(-6006.094mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P12-0(-4376.173mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-4376.173mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-5084.834mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P12-0(-5084.834mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.767mil < 10mil) Between Pad P1-25(-5096.645mil,-3734.843mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.4mil < 10mil) Between Pad P1-26(-5238.378mil,-3734.843mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P13-0(-2696.055mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-2696.055mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-3404.716mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P13-0(-3404.716mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P14-0(-1777.748mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-1777.748mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-2486.409mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P14-0(-2486.409mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-3240.74mil,-3459.252mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.918mil < 10mil) Between Pad P15-0(-3240.74mil,-3459.252mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-3240.74mil,-4049.803mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.376mil < 10mil) Between Pad P15-0(-3240.74mil,-4049.803mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.401mil < 10mil) Between Pad P1-50(-5238.378mil,-3262.403mil) on Top Layer And Track

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P3-0(-3203.89mil,-3071.382mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-3203.89mil,-3071.382mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-3440.11mil,-3071.382mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P3-0(-3440.11mil,-3071.382mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P9-0(-7895.858mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-7895.858mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-8604.519mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P9-0(-8604.519mil,-1393.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.133mil < 10mil) Between Pad R18-1(-1089.132mil,-965.988mil) on Top Layer And Text "R18"
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R25-1(-1689.549mil,-1620.512mil) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R25-2(-1689.549mil,-1559.488mil) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (2.51mil < 10mil) Between Pad R28-2(-7195.07mil,-2387.402mil) on Top Layer And Text "U23"
Silk To Solder Mask Clearance Constraint: (9.584mil < 10mil) Between Pad R38-2(-1880.11mil,-2367.717mil) on Top Layer And Text "U27"
Silk To Solder Mask Clearance Constraint: (8.106mil < 10mil) Between Pad R45-1(-3091.724mil,-3577.362mil) on Top Layer And Text "R45"
Silk To Solder Mask Clearance Constraint: (8.495mil < 10mil) Between Pad R45-2(-3030.7mil,-3577.362mil) on Top Layer And Text "R45"
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R49-1(-725.701mil,-2048.051mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R49-2(-725.701mil,-1977.185mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R52-1(-810.611mil,-2005.325mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R52-2(-810.611mil,-1934.458mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R54-1(-1418.039mil,-3685.744mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R54-2(-1418.039mil,-3756.611mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.54mil < 10mil) Between Pad TP15-TP(-1692.062mil,-1756.539mil) on Top Layer And Text "U14"
Silk To Solder Mask Clearance Constraint: (9.791mil < 10mil) Between Pad U13-1(-8680.173mil,-1825.394mil) on Top Layer And Text "C57"
Silk To Solder Mask Clearance Constraint: (9.797mil < 10mil) Between Pad U13-2(-8680.173mil,-1845.079mil) on Top Layer And Text "C57"
Silk To Solder Mask Clearance Constraint: (8.009mil < 10mil) Between Pad U4(-659mil,-1443.995mil) on Top Overlay And Polygon Region (26 hole(s))

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (3.858mil < 10mil) Between Text "1" (-3329.874mil,-3013.902mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (-3541.527mil,-3927.756mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-2391.921mil,-1331.693mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-3310.228mil,-1331.693mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-4990.346mil,-1331.693mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-5911.605mil,-1331.693mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-7588.771mil,-1331.693mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-8510.031mil,-1331.693mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (-3179.323mil,-3569.488mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.475mil < 10mil) Between Text "C66" (-161.797mil,-3563.175mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.598mil < 10mil) Between Text "D3" (-1191.989mil,-1876.217mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.598mil < 10mil) Between Text "D3" (-1191.989mil,-1876.217mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.501mil < 10mil) Between Text "MPPT_1" (-8848.997mil,-983.5mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.501mil < 10mil) Between Text "MPPT_1" (-8848.997mil,-983.5mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.775mil < 10mil) Between Text "PWR CONN" (-3078.89mil,-3378.98mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.966mil < 10mil) Between Text "PWR CONN" (-3078.89mil,-3378.98mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.737mil < 10mil) Between Text "PWR CONN" (-3078.89mil,-3378.98mil) on Top Overlay And Track