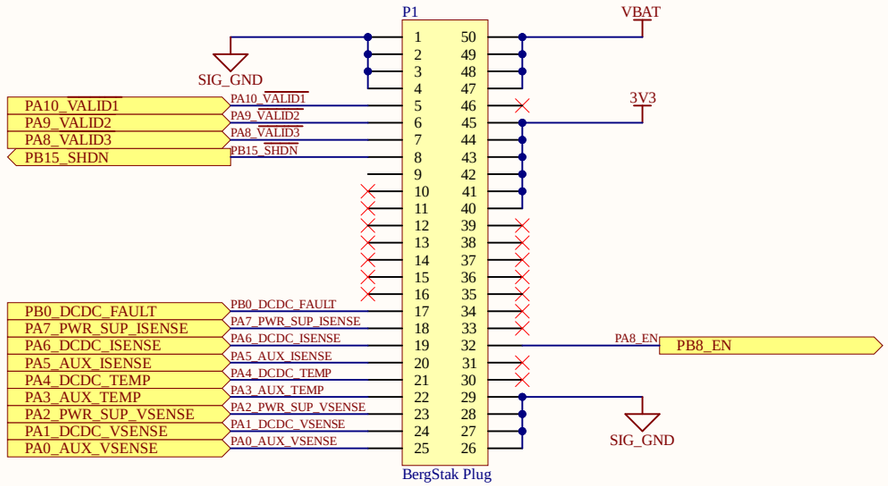
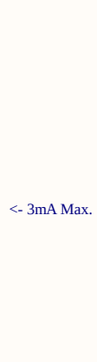
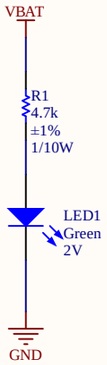
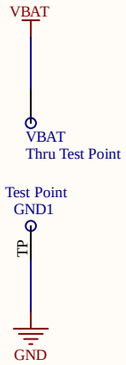
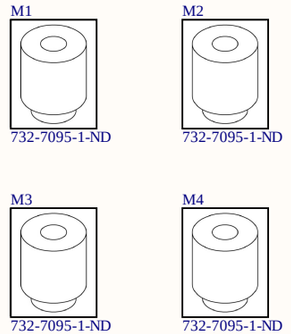
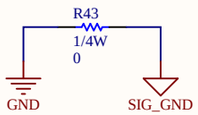


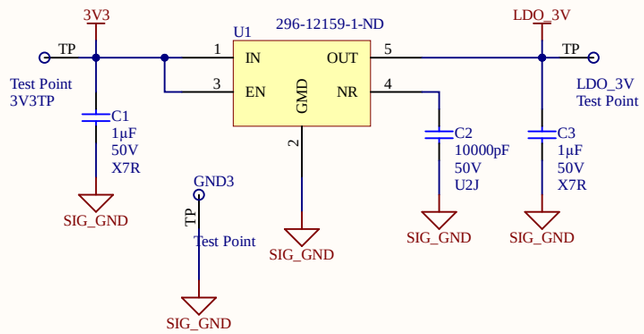


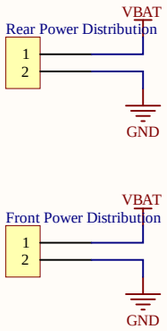




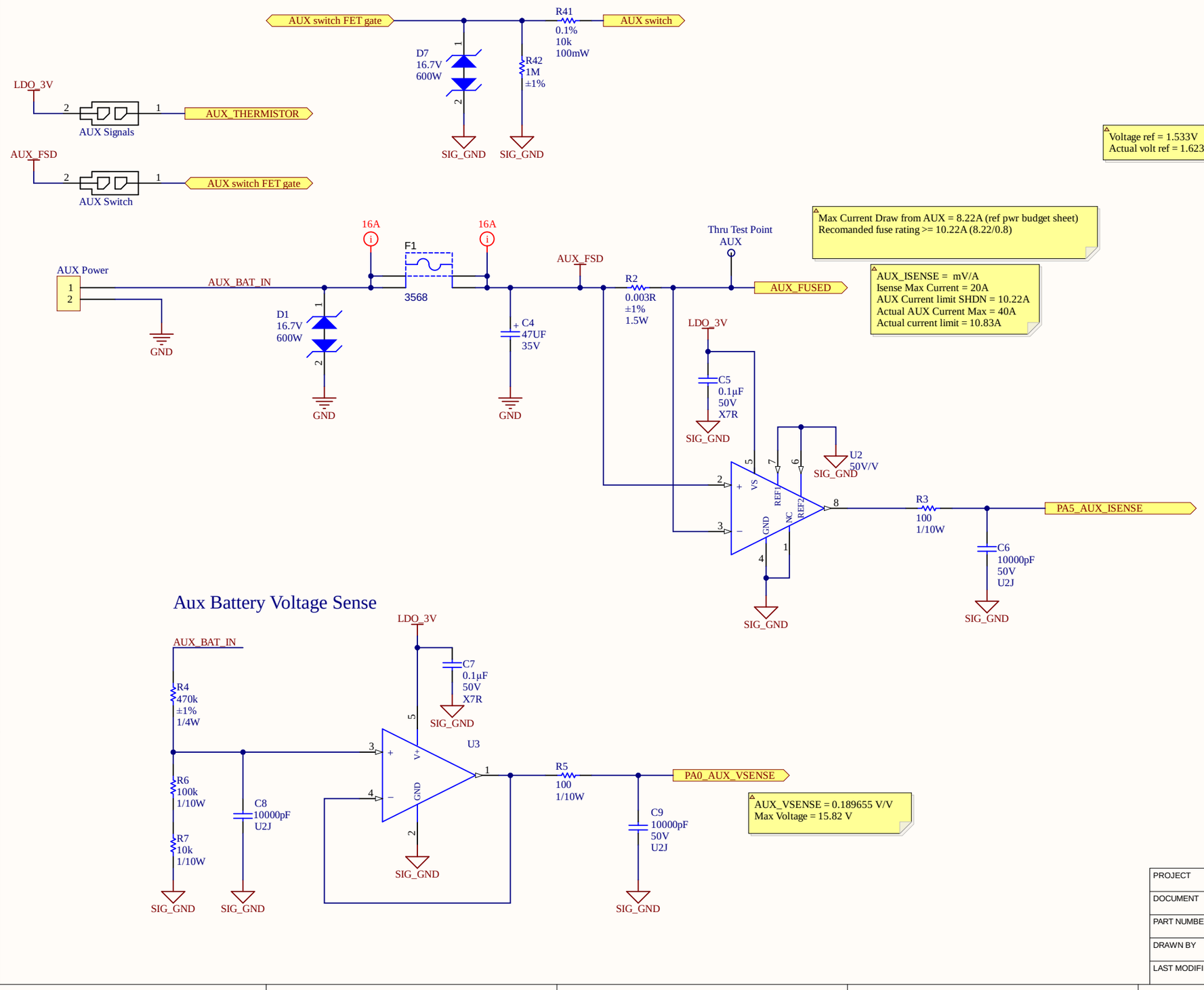








PROJECT	MSXIV_PowerSelection.PrjPcb		MIDNIGHT SUN
DOCUMENT	Title		
PART NUMBER		VARIANT [No Variations]	Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com
DRAWN BY		REVISION	
LAST MODIFIED	2020-05-30	SHEET * OF *	



PROJECT	MSXIV_PowerSelection.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED 2020-05-30	SHEET * OF *

MIDNIGHT SUN

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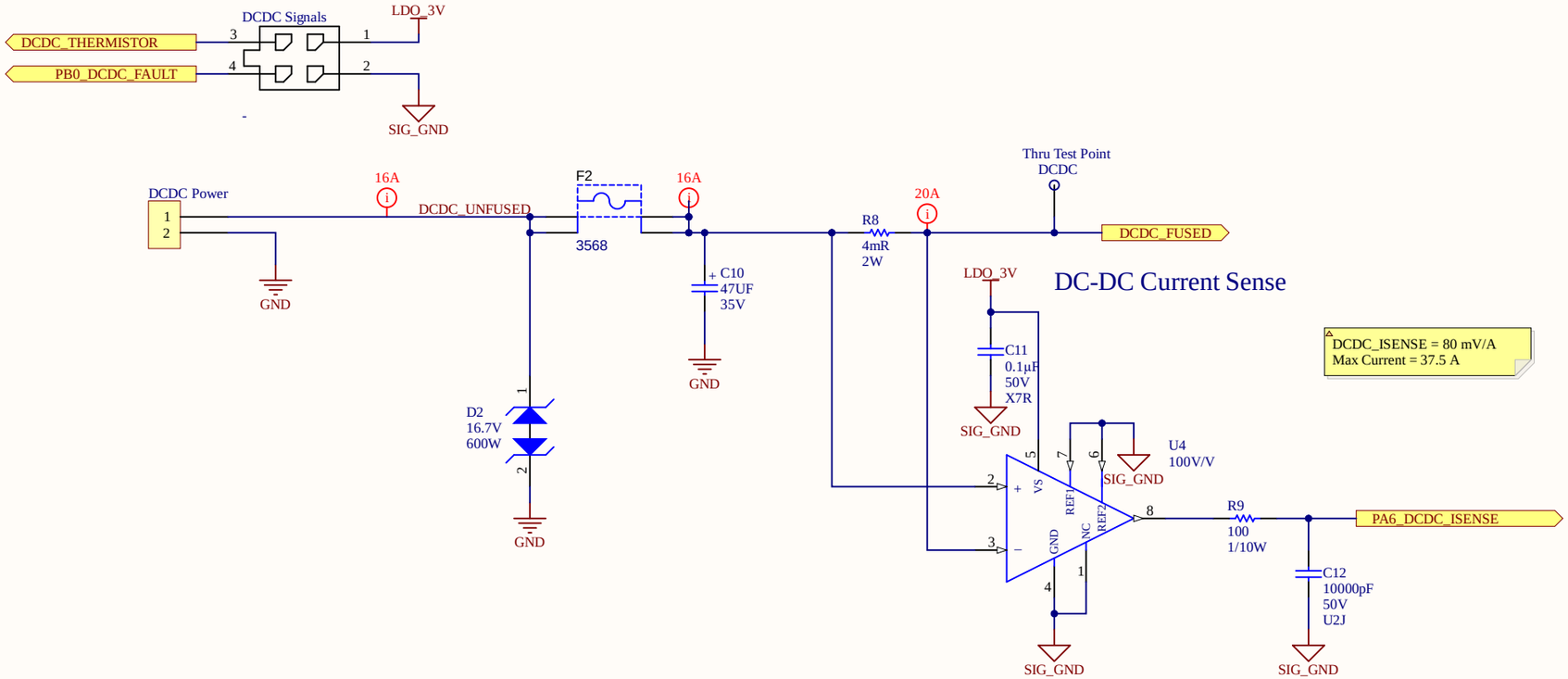

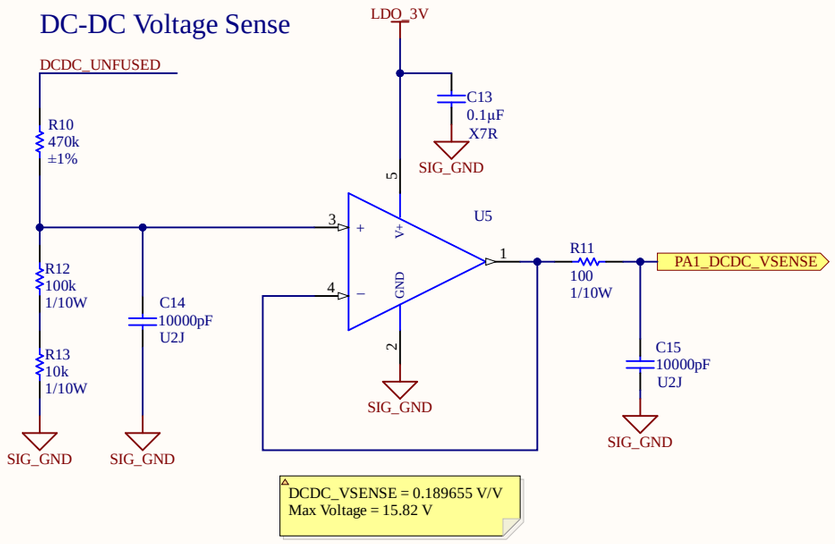

PROJECT	MSXIV_PowerSelection.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
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LAST MODIFIED 2020-05-30	SHEET * OF *

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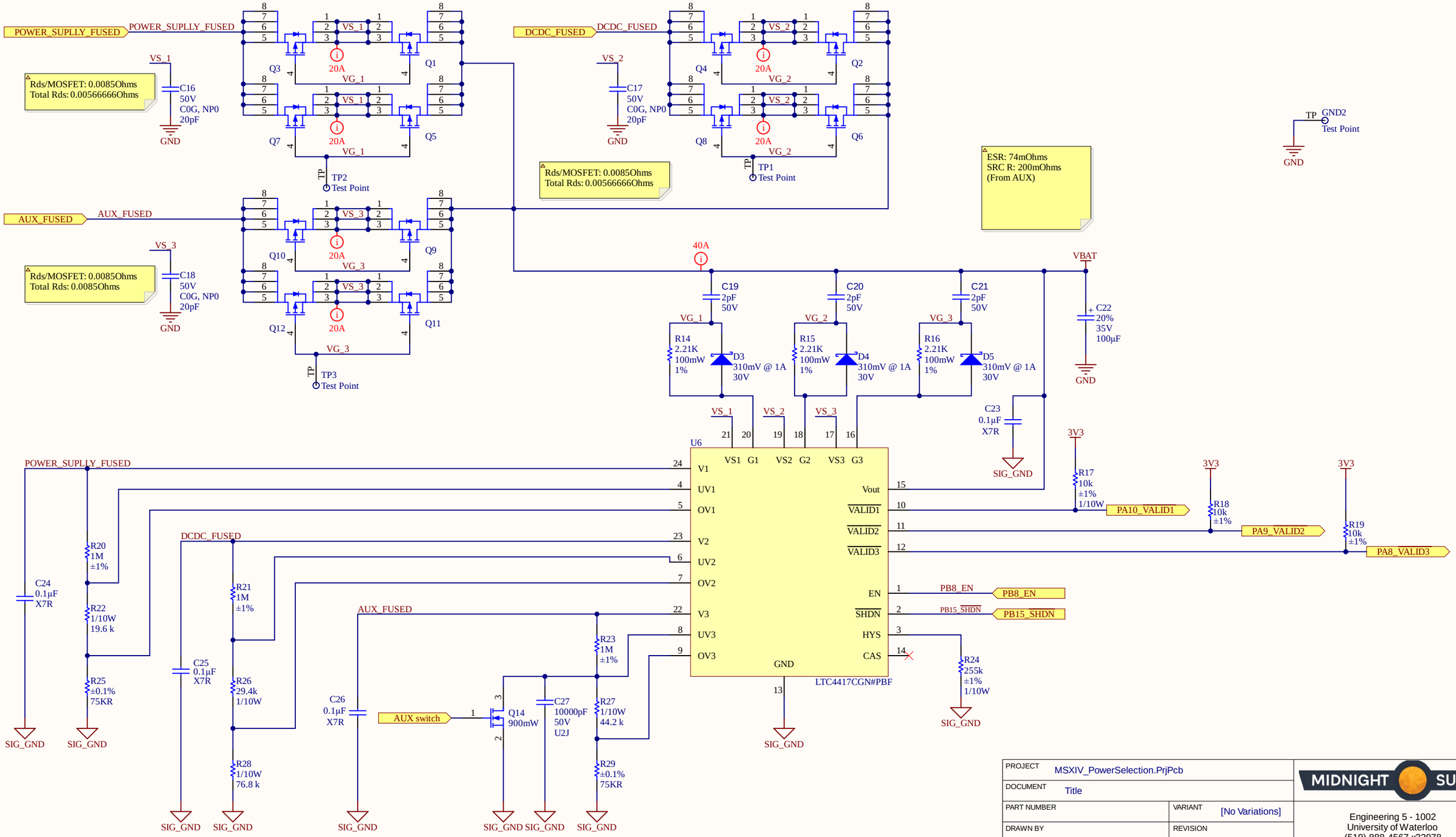

PROJECT	MSXIV_PowerSelection.PrjPcb
DOCUMENT	Title
PART NUMBER	
VARIANT	[No Variations]
DRAWN BY	
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LAST MODIFIED	2020-05-30
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Change connector to avoid wire parraleling
-Megafit
-Sabre

Add current and voltage sense for power supple channel

Power Supply Current Sense

Power Supply
16A
Power Supply_UNFUSED
F3
3568
16A
R34
4mR
2W
POWER_SUPLLY_FUSED
GND
D6
16.7V
600W
Ask for ideal diode placement, after or before fuse
LDO_3V
C33
0.1µF
50V
X7R
SIG_GND
U8
100V/V
VS
REF1
REF2
NC
GND
SIG_GND
Q13
R35
10k
1/10W
GND
R36
100
1/10W
PA7_PWR_SUP_ISENSE
C34
10000pF
50V
U2J
SIG_GND
SIG_GND

PWR_Supply_ISENSE = 80 mV/A
Max Current = 37.5 A

Power Supply Voltage Sense

Power Supply_UNFUSED
LDO_3V
C35
0.1µF
X7R
SIG_GND
R37
470k
±1%
U9
V+
GND
R38
100
1/10W
PA2_PWR_SUP_VSENSE
R39
100k
1/10W
C36
10000pF
U2J
R40
10k
1/10W
C37
10000pF
U2J
SIG_GND
SIG_GND
SIG_GND
SIG_GND

DCDC_VSENSE = 0.189655 V/V
Max Voltage = 15.82 V

PROJECT	MSXIV_PowerSelection.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED 2020-05-30	SHEET * OF *

MIDNIGHT SUN

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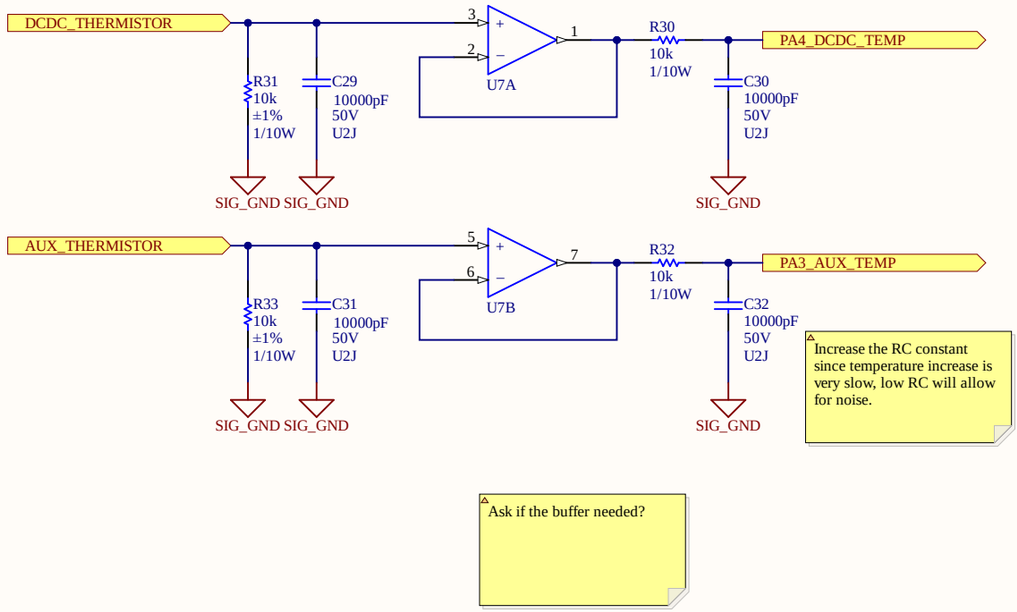
Temperature Sense



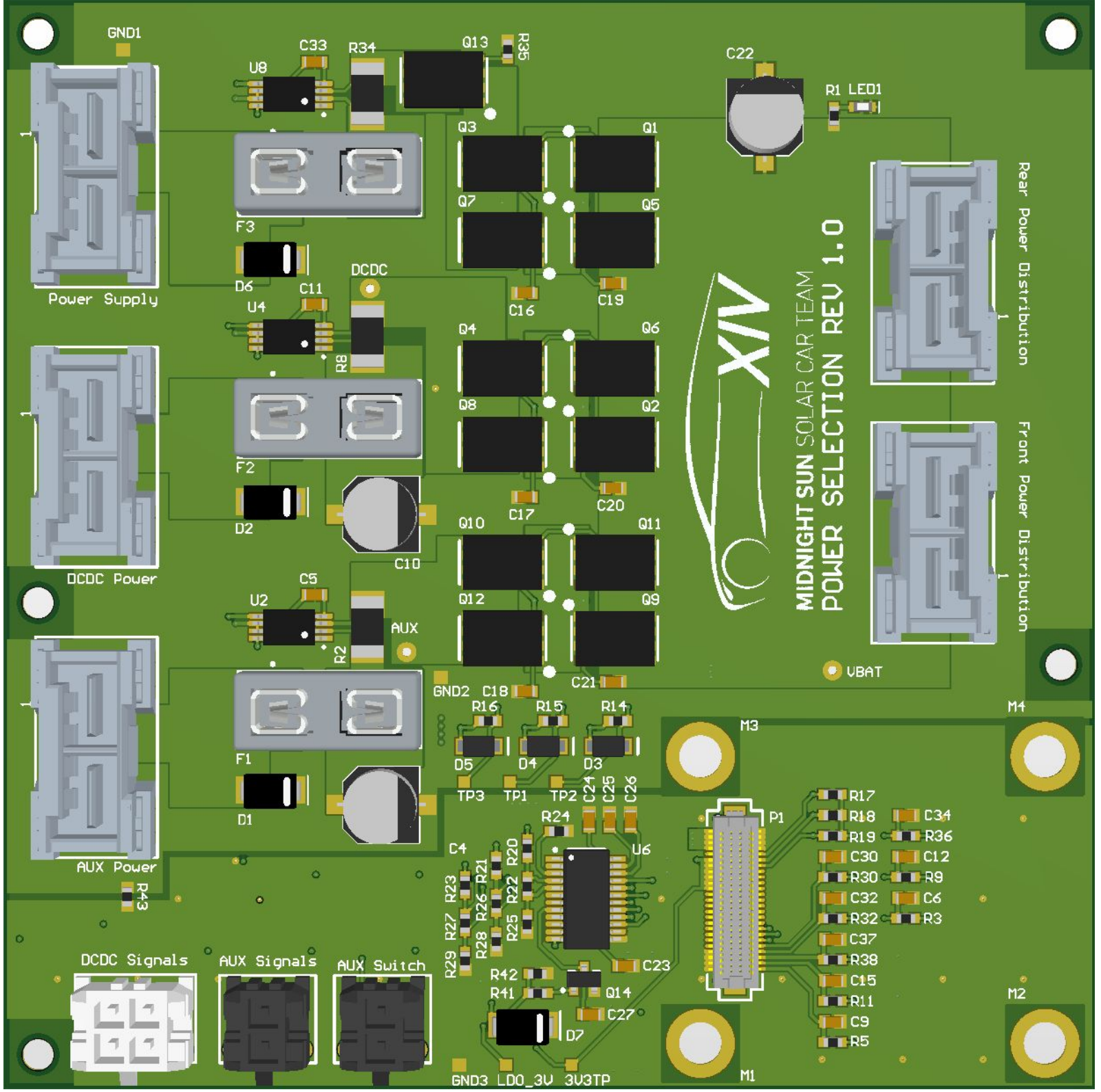
Beaware that there will be two general purpose amp as dcdc and aux both uses this design, please make sure does this part belong in main schematic or stays here.

PROJECT	MSXIV_PowerSelection.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com
DRAWN BY	REVISION	
LAST MODIFIED 2020-05-30	SHEET * OF *	

Bill of Materials

Project:	MSXIV_PowerSelection.PrjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2020-05-30 12:17 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	130

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CMP-002-00071-4	wer, Front Power Distribution, Power Supply, F	TE Connectivity	2042274-1	Farnell	1871344		5	
CONN 2POS MICRO-FIT 3mm	AUX Signals, AUX Switch			Digi-Key	WM10657-ND		2	
Thru Test Point	AUX, DCDC, VBAT						3	
CAP CER 1UF 50V 10% X7R 0603	C1, C3	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND		2	
CAP CER 10nF 50V 5% X7R 0603	9, C12, C14, C15, C27, C29, C30, C31, C32, (	KEMET	C0603C103J5JAC7867	Digi-Key	399-13384-1-ND		15	
CAP ALUM 47UF 20% 35V SMD	C4, C10			Digi-Key	PCE3961CT-ND		2	
CAP CER 0.1UF 50V 10% X7R 0603	C7, C11, C13, C23, C24, C25, C26, C28, C33,	AVX Corporation	06035C104KAT2A	Digi-Key	478-5052-1-ND		11	
CMP-013-0033-1	C16, C17, C18	Murata	GRM1885C1H200JA01D	RSComponents	1694105		3	
CMP-001-00085-4	C19, C20, C21	TDK	CGA3E2C0G1H020C080AA	Digi-Key	445-5616-1-ND	0.26236	3	$ 0.79
CMP-013-0003-1	C22	Panasonic	EEE-1VA101XP	RSComponents	1763750		1	
DIODE TVS 15VWM 24.4VC DO-214AA (SMB)	D1, D2, D6, D7	Fairchild/ON Semiconductor	SMBJ15CA	Digi-Key	SMBJ15CAFSCT-ND		4	
DIODE SCHOTTKY 30V 1A POWERDI123	D3, D4, D5			Digi-Key	DFLS130LDICT-ND		3	
CMP-003-0105-1	DCDC Signals	Molex	430450427	Avnet	430450427		1	
CMP-005-00014-1	F1, F2, F3	Keystone Electronics	3568	Newark	22M2715	1.42	3	$ 4.27
LED GREEN CLEAR 2V 0603	LED1			Digi-Key	732-4980-1-ND		1	
STANDOFF RND M2.5X0.45 STEEL 5MM	M1, M2, M3, M4			Digi-Key	732-7095-1-ND		4	
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND		1	
MOSFET P-CH PWR56 40V 4.9 MOHM	2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13			Digi-Key	DWS9508L-F085OSCT-ND		13	
CMP-003-0074-1	Q14	Diodes	DMN3023L-7	Newark	07AH3765		1	
RES 4.7K OHM 1% 1/10W 0603	R1	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND		1	
RES 0.003 OHM 1% 1.5W 2010	R2	Stackpole Electronics Inc.	CSNL2010FT3L00	Digi-Key	CSNL2010FT3L00CT-ND		1	
RES 100 OHM 1% 1/10W 0603	R3, R5, R9, R11, R36, R38	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND		6	
RES 470K OHM 1% 1/4W 0603	R4, R10, R37	Panasonic Electronic Components	ERJ-PA3F4703V	Digi-Key	P470KBYCT-ND		3	
RES 100K OHM 5% 1/8W 0603	R6, R12, R39	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCT-ND		3	
RES 10K OHM 1% 1/10W 0603	R13, R17, R18, R19, R30, R31, R32, R33, R35	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND		11	
RES 4m OHM 1% 2W 2010	R8, R34			Digi-Key	P-TLR2HWDTE4L00F75CT-ND		2	
RES 2.21K OHM 1% 1/10W 0603	R14, R15, R16			Digi-Key	YAG3586CT-ND		3	
RES 1M OHM 1% 1/10W 0603	R20, R21, R23, R42	Yageo	RC0603FR-071ML	Digi-Key	311-1.00MHRCT-ND		4	
RES 19.6K OHM 1% 1/10W 0603	R22			Digi-Key	RMCF0603FT19K6CT-ND		1	
RES 255K OHM 1% 1/10W 0603	R24	Yageo	RC0603FR-07255KL	Digi-Key	311-255KHRCT-ND		1	
RES SMD 75K OHM 0.1% 1/10W 0603	R25, R29			Digi-Key	P75KDBCT-ND		2	
RES 29.4K OHM 1% 1/10W 0603	R26	Yageo	RC0603FR-0729K4L	Digi-Key	311-29.4KHRCT-ND		1	
RES SMD 44.2K OHM 1% 1/10W 0603	R27			Digi-Key	P44.2KHCT-ND		1	
RES 76.8K OHM 1% 1/10W 0603	R28			Digi-Key	RMCF0603FT76K8CT-ND		1	
CMP-010-0039-1	R41	Panasonic	ERA-3AEB103V	Newark	01X1282		1	
CMP-010-0000-1	R43	Vishay Dale	CRCW06030000Z0EAHP	RSComponents	1701982		1	
IC REG LINEAR 3V 200MA SOT23-5	U1			Digi-Key	296-12159-1-ND		1	
IC CURRENT AMPLIFIER INA240 8-TSSOP	U2	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND		1	
C OP AMP GEN PURPOSE RR 10MHZ SOT-23-	U3, U5, U9	Texas Instruments	TLV316QDBVRQ1	Digi-Key	296-45323-1-ND		3	
IC CURRENT AMPLIFIER INA240 8-TSSOP	U4, U8	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND		2	
C OR CONTROLLER SOURCE SELECT 24SSOF	U6	Linear Technology	LTC4417CGN#PBF	Digi-Key	LTC4417CGN#PBF-ND		1	
IC OP AMP DUAL GP RR 10MHZ 8-VSSOP	U7			Digi-Key	296-47349-1-ND		1	
							Total:	$ 5.06


MIDNIGHT SUN SOLAR CAR TEAM
POWER SELECTION REV 1.0
Power Supply
DCDC Power
AUX Power
Rear Power Distribution
Front Power Distribution
DCDC Signals
AUX Signals
AUX Switch
VBAT
GND1
GND2
GND3
LDO_3V
3V3TP
DCDC
AUX
U8
U4
U2
U6
P1
LED1
F1
F2
F3
D1
D2
D3
D4
D5
D6
D7
Q1
Q2
Q3
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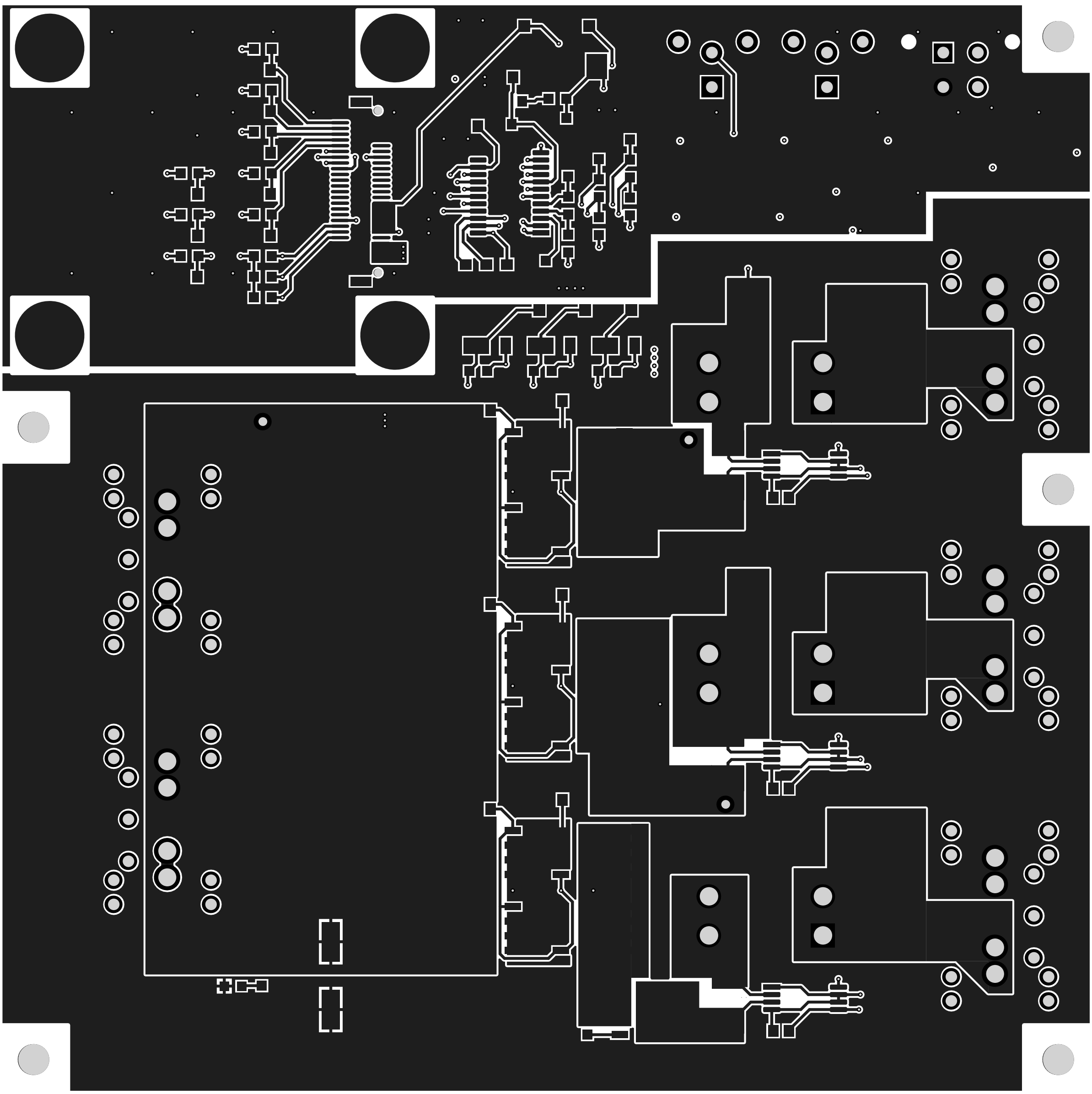
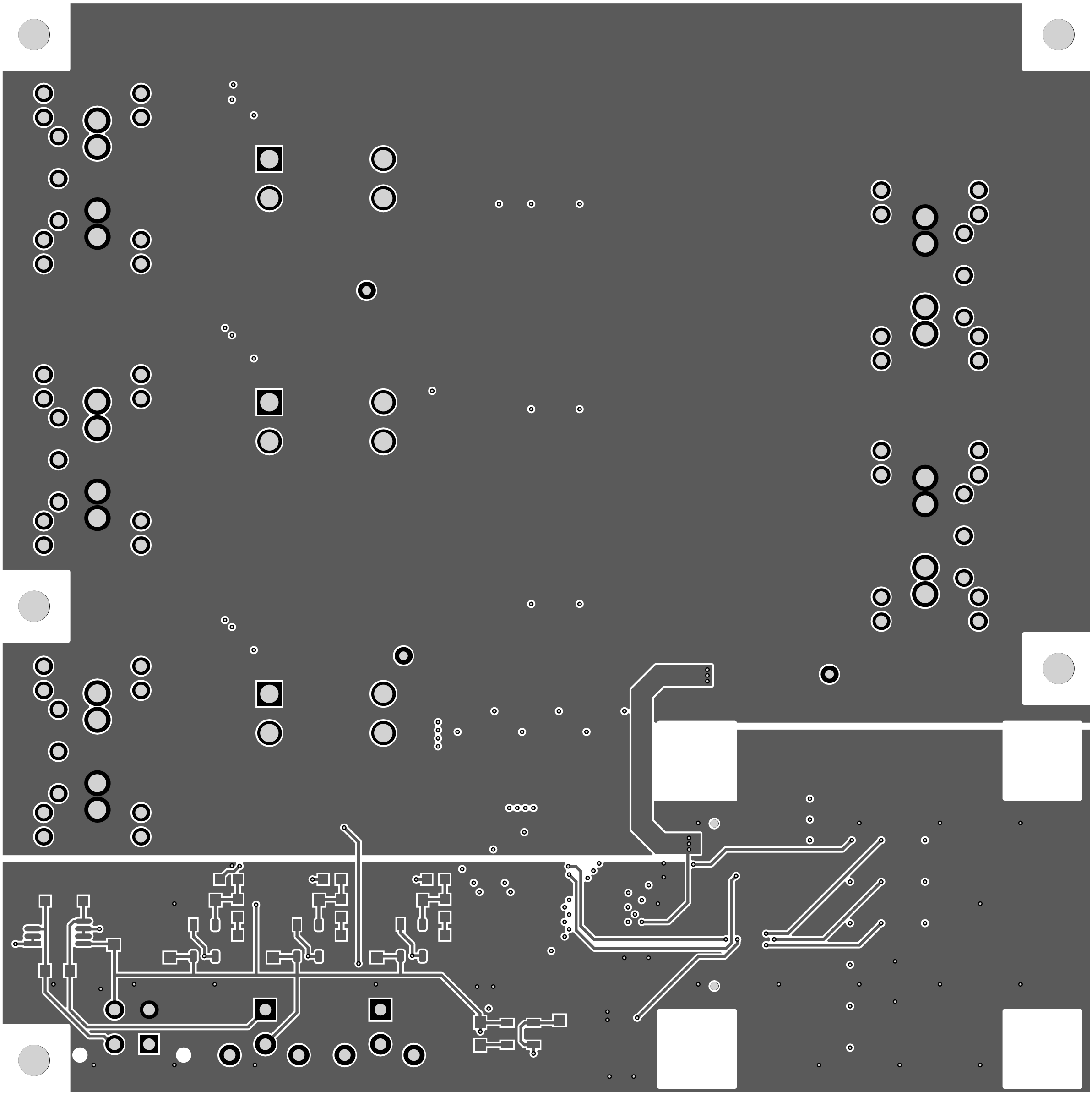
Q10
Q11
Q12
Q13
Q14
M1
M2
M3
M4





Design Rules Verification Report

Filename : D:\Josh9\Documents\Midnight Sun\hardware\MSXIV_PowerSelection\Power Sel

Warnings 0
Rule Violations 222

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	9
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	11
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	196
Silk to Silk (Clearance=0.254mm) (All),(All)	6
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	222

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3mm,3mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3mm,42.4mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3mm,92mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(92mm,37mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(92mm,92mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M1-(60.6mm,4mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M2-(90.6mm,4mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M3-(60.6mm,29mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M4-(90.6mm,29mm) on Multi-Layer Actual Hole Size = 3.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.21mm < 0.254mm) Between Pad DCDC-TH_TP(31.9mm,69.8mm) on Multi-Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(62.1mm,23.55mm) on Multi-Layer And Pad P1-(63.6mm,24.3mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(62.1mm,9.45mm) on Multi-Layer And Pad P1-(63.6mm,8.7mm) on Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-1(46.4mm,6.25mm) on Bottom Layer And Pad U1-2(46.4mm,5.3mm) or
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-2(46.4mm,5.3mm) on Bottom Layer And Pad U1-3(46.4mm,4.35mm) or
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U3-1(34.85mm,14.8mm) on Bottom Layer And Pad U3-2(35.8mm,14.8mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U3-2(35.8mm,14.8mm) on Bottom Layer And Pad U3-3(36.75mm,14.8mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(25.85mm,14.775mm) on Bottom Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(26.8mm,14.775mm) on Bottom Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U9-1(16.85mm,14.775mm) on Bottom Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U9-2(17.8mm,14.775mm) on Bottom Layer And Pac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad AUX Power-0(12.3mm,22.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad AUX Power-0(12.3mm,24.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad AUX Power-0(12.3mm,35.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad AUX Power-0(12.3mm,37.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad AUX Power-0(3.85mm,22.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad AUX Power-0(3.85mm,24.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad AUX Power-0(3.85mm,35.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad AUX Power-0(3.85mm,37.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad AUX Signals-0(20mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.254mm) Between Pad AUX Signals-0(20mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.254mm) Between Pad AUX Signals-0(26mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad AUX Signals-0(26mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad AUX Switch-0(30mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.254mm) Between Pad AUX Switch-0(30mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.254mm) Between Pad AUX Switch-0(36mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad AUX Switch-0(36mm,3.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C10-1(29.95mm,50.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C10-1(29.95mm,50.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C10-2(35.85mm,50.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C10-2(35.85mm,50.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-1(66.2mm,81.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-1(66.2mm,81.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-2(66.2mm,87.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-2(66.2mm,87.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-1(29.95mm,24.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-1(29.95mm,24.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-2(35.85mm,24.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-2(35.85mm,24.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D1-2(25.264mm,26.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D2-2(25.264mm,51.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D6-2(25.264mm,72.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D7-2(47.164mm,5.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad DCDC Power-0(12.3mm,47.7mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad DCDC Power-0(12.3mm,49.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad DCDC Power-0(12.3mm,60.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad DCDC Power-0(12.3mm,62.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad DCDC Power-0(3.85mm,47.7mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad DCDC Power-0(3.85mm,49.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad DCDC Power-0(3.85mm,60.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad DCDC Power-0(3.85mm,62.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Front Power Distribution-0(76.6mm,41.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Front Power Distribution-0(76.6mm,43.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Front Power Distribution-0(76.6mm,53.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Front Power Distribution-0(76.6mm,55.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Front Power Distribution-0(85.05mm,41.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Front Power Distribution-0(85.05mm,43.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Front Power Distribution-0(85.05mm,53.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Front Power Distribution-0(85.05mm,55.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad GND2-TP(38.1mm,35.9mm) on Top Layer And Text "GND2"
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(75.45mm,85.61mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(65.4mm,22.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(65.4mm,10.5mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(61.8mm,10.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(61.8mm,22.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad Power Supply-0(12.3mm,72.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad Power Supply-0(12.3mm,74.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad Power Supply-0(12.3mm,84.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad Power Supply-0(12.3mm,86.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad Power Supply-0(3.85mm,72.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad Power Supply-0(3.85mm,74.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad Power Supply-0(3.85mm,84.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad Power Supply-0(3.85mm,86.9mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-1(46.2mm,44mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-2(46.2mm,45.27mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-3(46.2mm,46.54mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-4(46.2mm,47.81mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-5(40.71mm,47.81mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-6(40.71mm,46.54mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-7(40.71mm,45.27mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-8(40.71mm,44mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-1(50.4mm,82.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-1(50.4mm,47.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-2(50.4mm,46.53mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-3(50.4mm,45.26mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-4(50.4mm,43.99mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-5(55.89mm,43.99mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-6(55.89mm,45.26mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-7(55.89mm,46.53mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-8(55.89mm,47.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-2(50.4mm,81.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-1(46.2mm,37.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-2(46.2mm,38.67mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-3(46.2mm,39.94mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-4(46.2mm,41.21mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-5(40.71mm,41.21mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-6(40.71mm,39.94mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-7(40.71mm,38.67mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-8(40.71mm,37.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-3(50.4mm,79.96mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-1(41.1mm,86.03mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-2(41.1mm,87.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-3(41.1mm,88.57mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-4(41.1mm,89.84mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-5(35.61mm,89.84mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-6(35.61mm,88.57mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-7(35.61mm,87.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-8(35.61mm,86.03mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-4(50.4mm,78.69mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.254mm) Between Pad Q14-1(49.573mm,8.624mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.254mm) Between Pad Q14-2(51.373mm,8.624mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-5(55.89mm,78.69mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-6(55.89mm,79.96mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-7(55.89mm,81.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q1-8(55.89mm,82.5mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-1(50.4mm,58.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-2(50.4mm,56.83mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-3(50.4mm,55.56mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-4(50.4mm,54.29mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-5(55.89mm,54.29mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-6(55.89mm,55.56mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-7(55.89mm,56.83mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q2-8(55.89mm,58.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-1(46.2mm,78.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-2(46.2mm,79.97mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-3(46.2mm,81.24mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-4(46.2mm,82.51mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-5(40.71mm,82.51mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-6(40.71mm,81.24mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-7(40.71mm,79.97mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-8(40.71mm,78.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-1(46.2mm,60.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-2(46.2mm,62.17mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-3(46.2mm,63.44mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-4(46.2mm,64.71mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-5(40.71mm,64.71mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-6(40.71mm,63.44mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-7(40.71mm,62.17mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-8(40.71mm,60.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-1(50.4mm,75.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-2(50.4mm,74.63mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-3(50.4mm,73.36mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-4(50.4mm,72.09mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-5(55.89mm,72.09mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-6(55.89mm,73.36mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-7(55.89mm,74.63mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-8(55.89mm,75.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-1(50.4mm,64.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-2(50.4mm,63.43mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-3(50.4mm,62.16mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-4(50.4mm,60.89mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-5(55.89mm,60.89mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-6(55.89mm,62.16mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-7(55.89mm,63.43mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-8(55.89mm,64.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-1(46.2mm,72.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-2(46.2mm,73.37mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-3(46.2mm,74.64mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-4(46.2mm,75.91mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-5(40.71mm,75.91mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-6(40.71mm,74.64mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-7(40.71mm,73.37mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-8(40.71mm,72.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-1(46.2mm,54.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-2(46.2mm,55.57mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-3(46.2mm,56.84mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-4(46.2mm,58.11mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-5(40.71mm,58.11mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-6(40.71mm,56.84mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-7(40.71mm,55.57mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-8(40.71mm,54.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-1(50.4mm,41.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-2(50.4mm,39.93mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-3(50.4mm,38.66mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-4(50.4mm,37.39mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-5(55.89mm,37.39mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-6(55.89mm,38.66mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-7(55.89mm,39.93mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-8(55.89mm,41.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Rear Power Distribution-0(76.6mm,63.7mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Rear Power Distribution-0(76.6mm,65.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Rear Power Distribution-0(76.6mm,76.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad Rear Power Distribution-0(76.6mm,78.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Rear Power Distribution-0(85.05mm,63.7mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Rear Power Distribution-0(85.05mm,65.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Rear Power Distribution-0(85.05mm,76.4mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad Rear Power Distribution-0(85.05mm,78.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad TP1-TP(44.1mm,26.8mm) on Top Layer And Text "TP1"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad TP2-TP(48.1mm,26.8mm) on Top Layer And Text "TP2"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad TP3-TP(40.1mm,26.8mm) on Top Layer And Text "TP3"
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-1(46.4mm,6.25mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-1(46.4mm,6.25mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-2(46.4mm,5.3mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-3(46.4mm,4.35mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-3(46.4mm,4.35mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-4(44.1mm,4.35mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-4(44.1mm,4.35mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad U1-5(44.1mm,6.25mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad U1-5(44.1mm,6.25mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U7-1(2.9mm,13.125mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U7-2(2.9mm,13.775mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U7-3(2.9mm,14.425mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad U7-4(2.9mm,15.075mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U7-5(7.3mm,15.075mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U7-6(7.3mm,14.425mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U7-7(7.3mm,13.775mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U7-8(7.3mm,13.125mm) on Bottom Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "1" (2.35mm,33.45mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "1" (2.35mm,58.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "1" (2.35mm,83.15mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "1" (86.55mm,44.85mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "1" (86.55mm,67.45mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "AUX Power" (6.5mm,19mm) on Top Overlay And Track