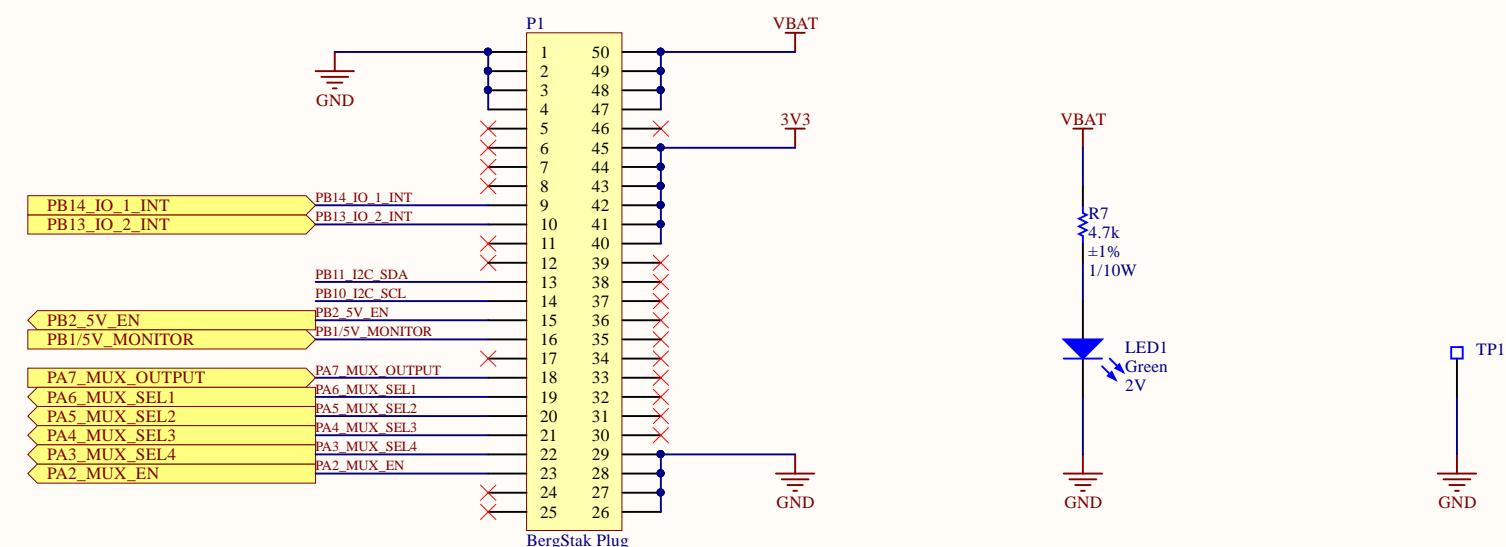
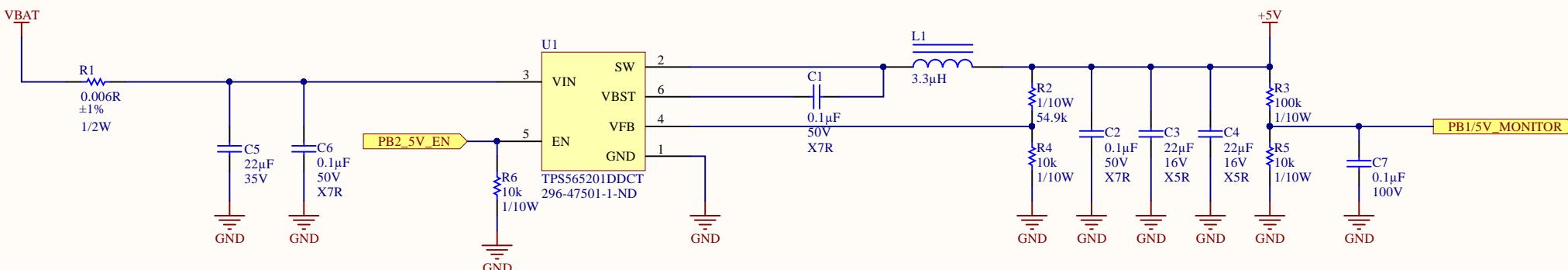


## Regulator

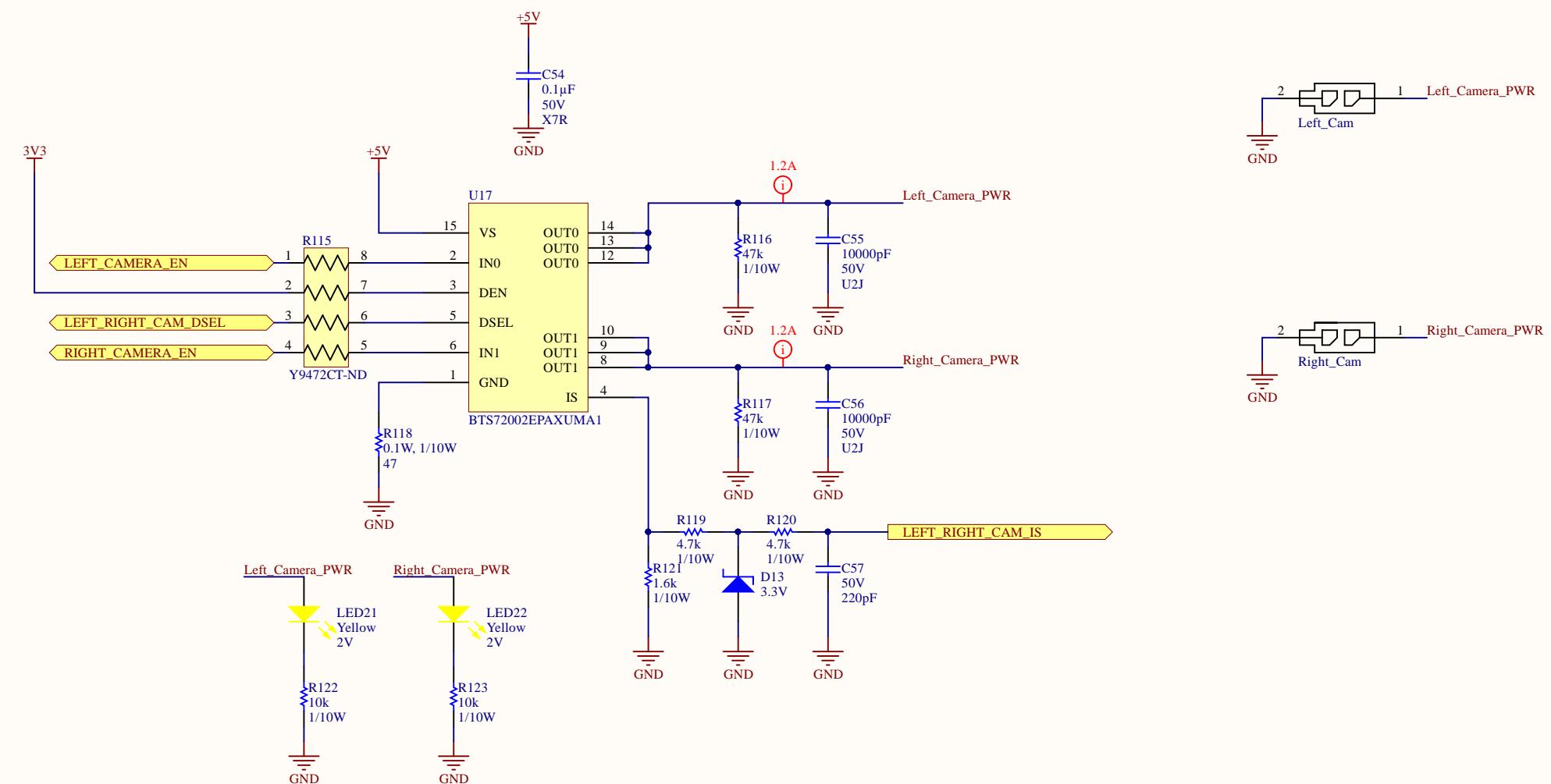


## 12V Power Connector



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Controller Board Interface
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-24
SHEET *	OF *

A



PROJECT MSXIV\_Front\_Power\_Distribution.PrjPcb

DOCUMENT Title

PART NUMBER VARIANT [No Variations]

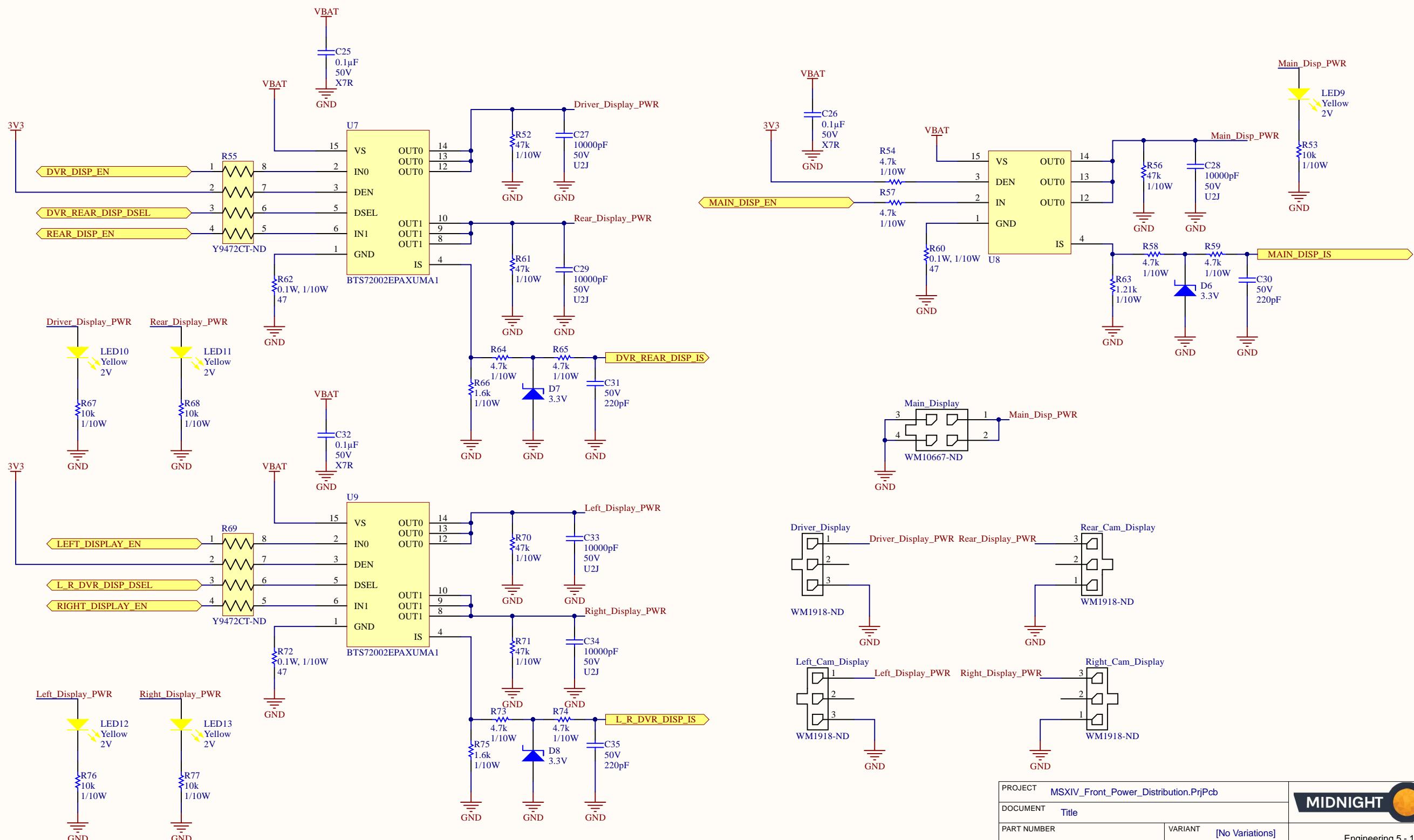
DRAWN BY REVISION

LAST MODIFIED 2020-02-24 SHEET \* OF \*

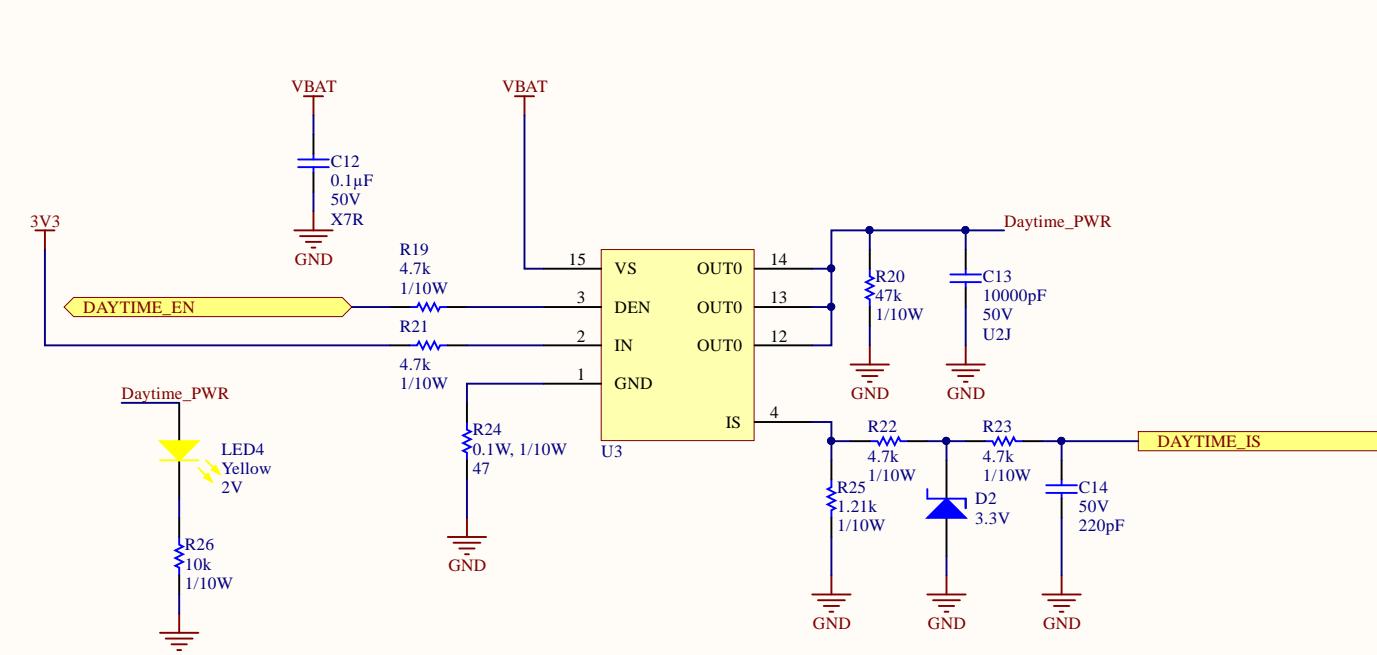
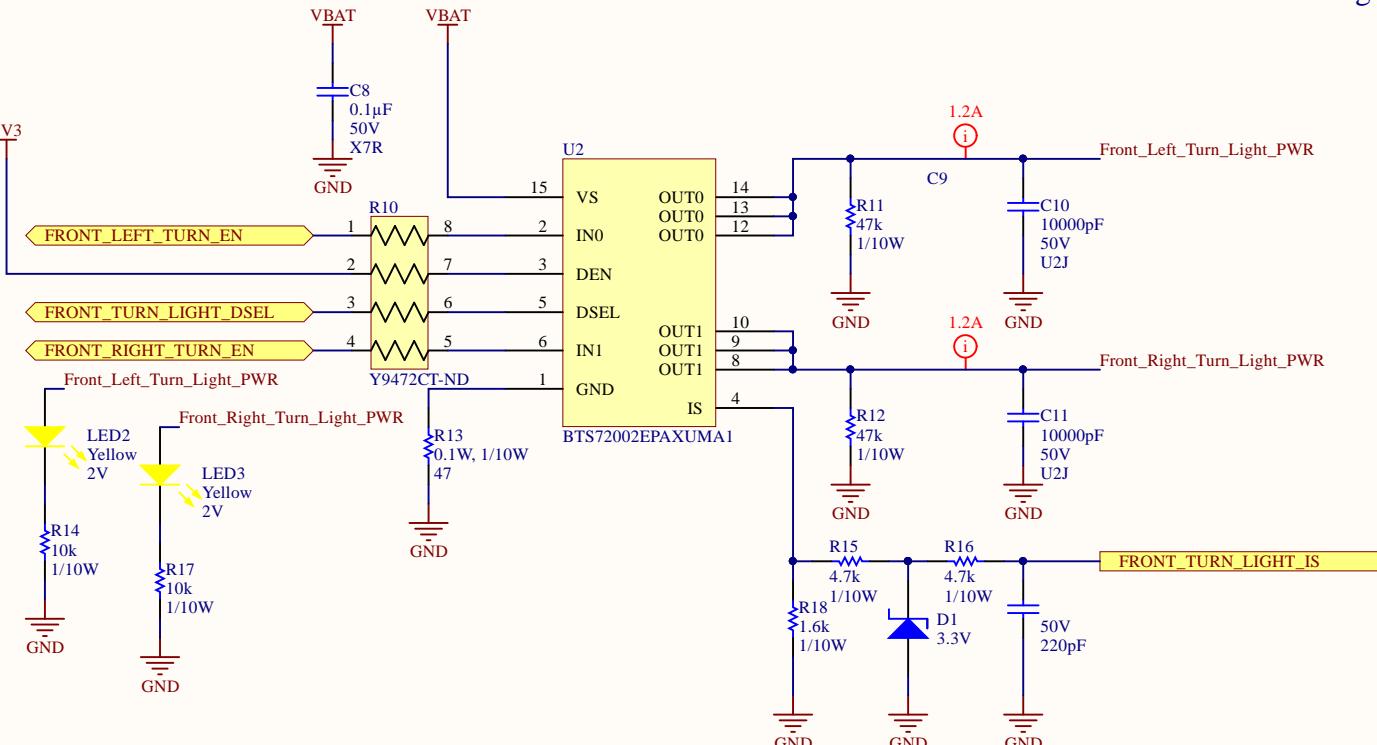


Engineering 5 - 1002  
University of Waterloo  
(519) 888-4567 x32978  
hardware@uwmidsun.com

A

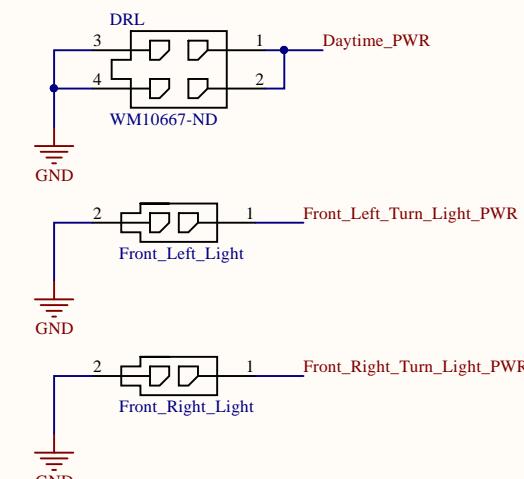


## Front light



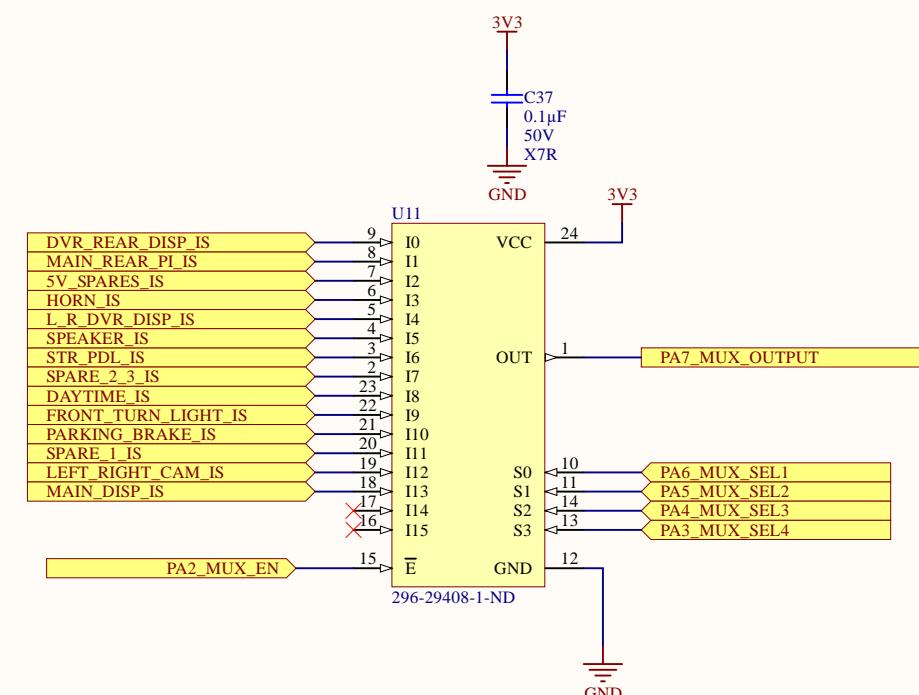
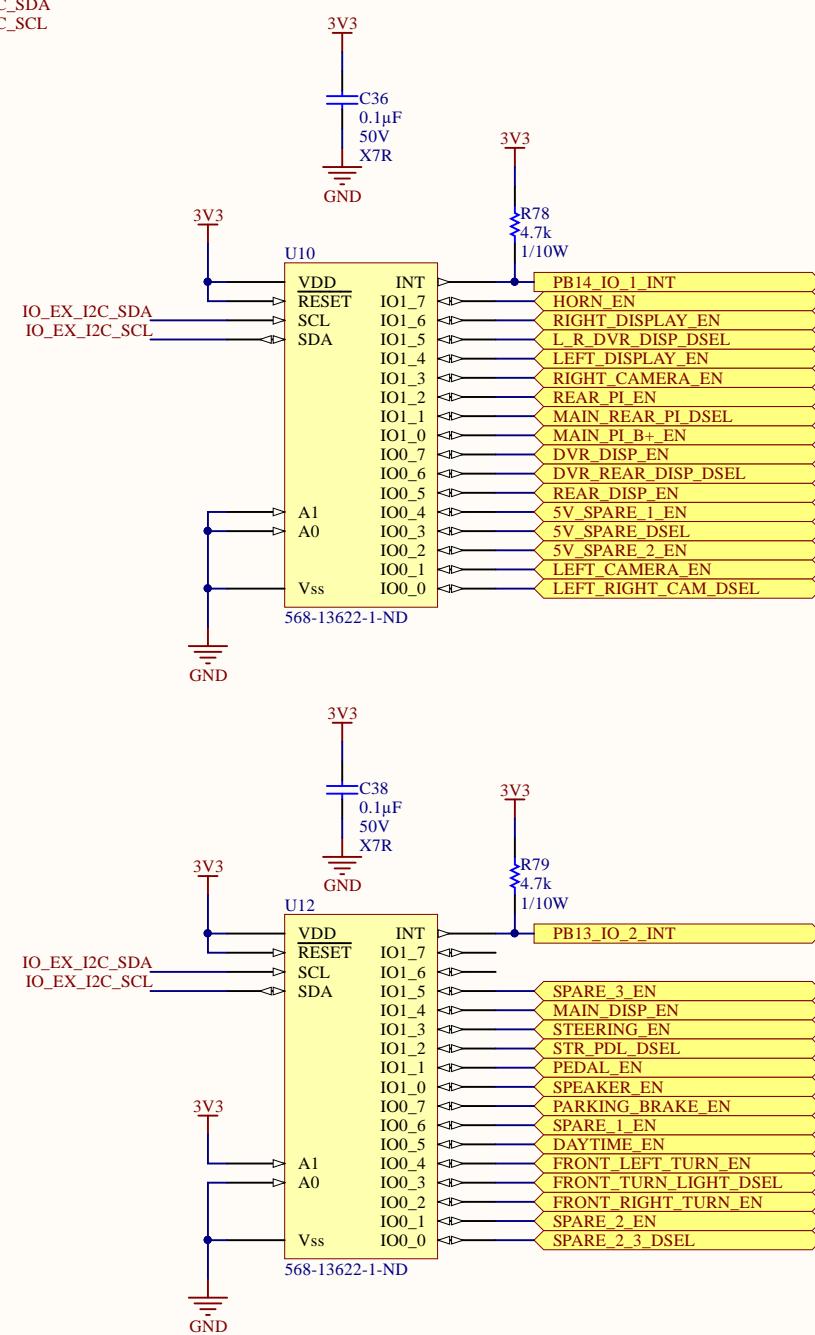
**Light Load**  
Nominal Current: 1.2 A  
Overload Current: 8.7 - 11.5 A  
Based on the specs of BTS7200-2EPC

Draws 4mA when active



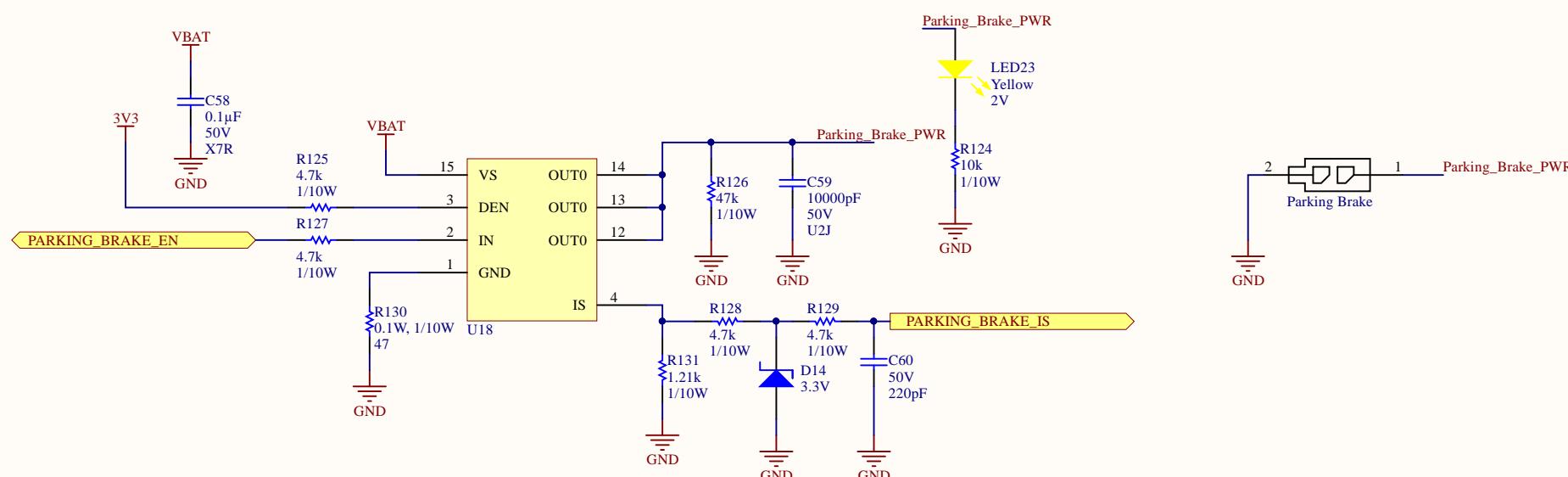
PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	SHEET * OF *
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IO\_EX\_I2C\_SDA  
IO\_EX\_I2C\_SCL

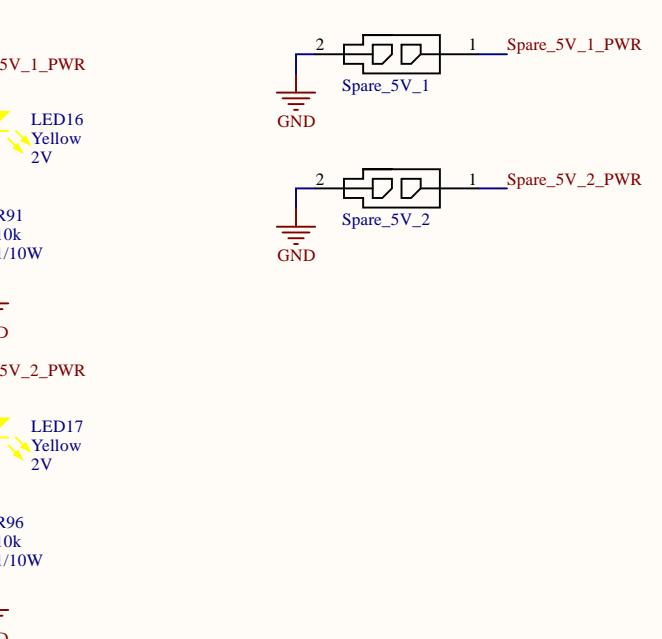
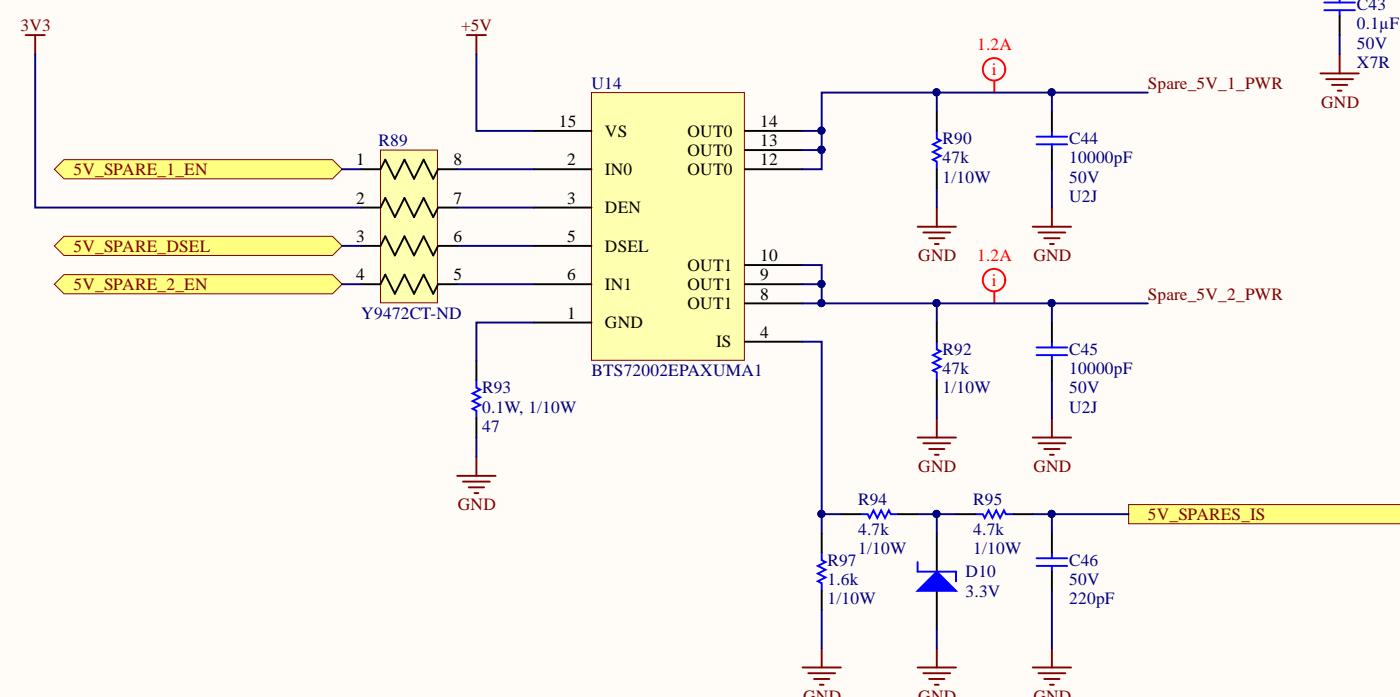
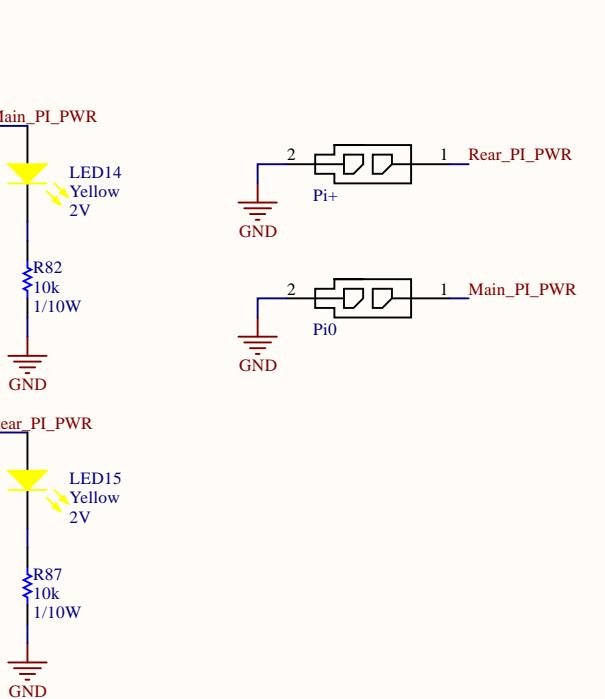
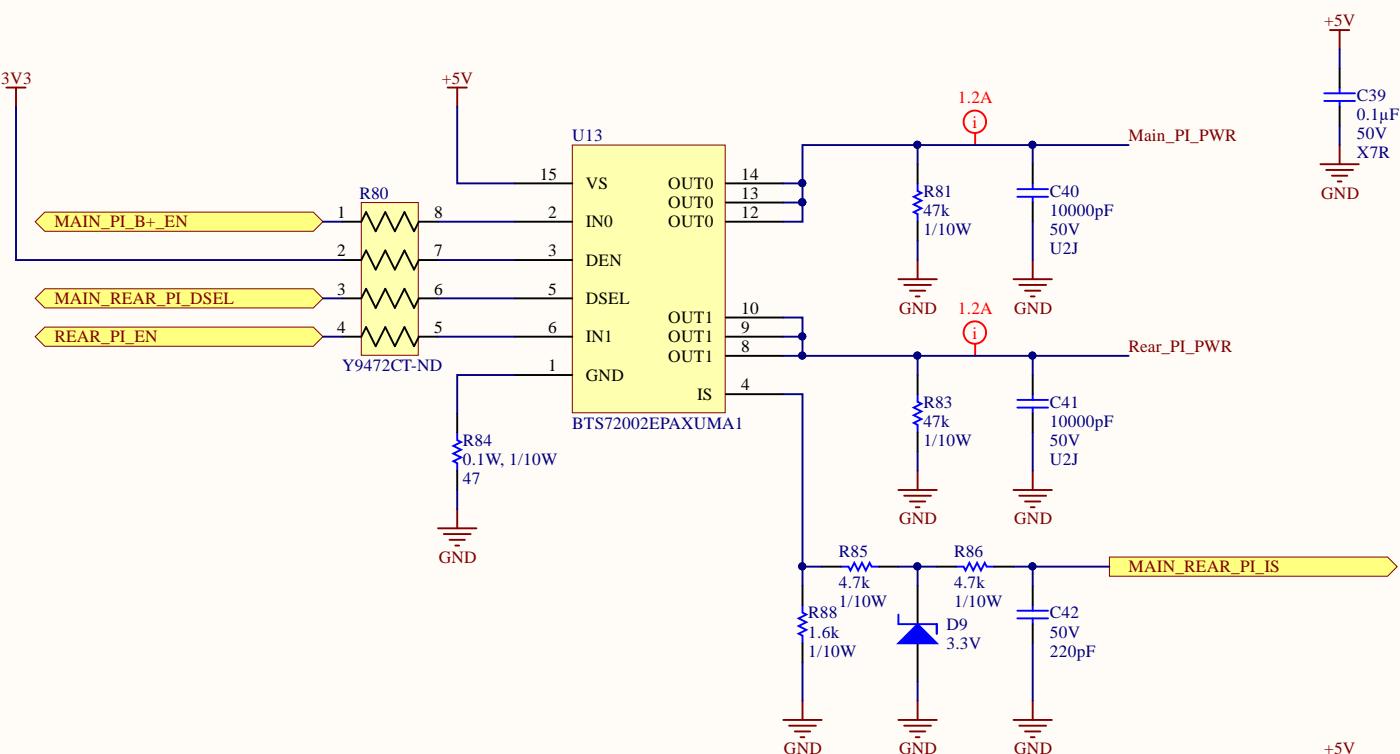


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-24
SHEET *	OF *

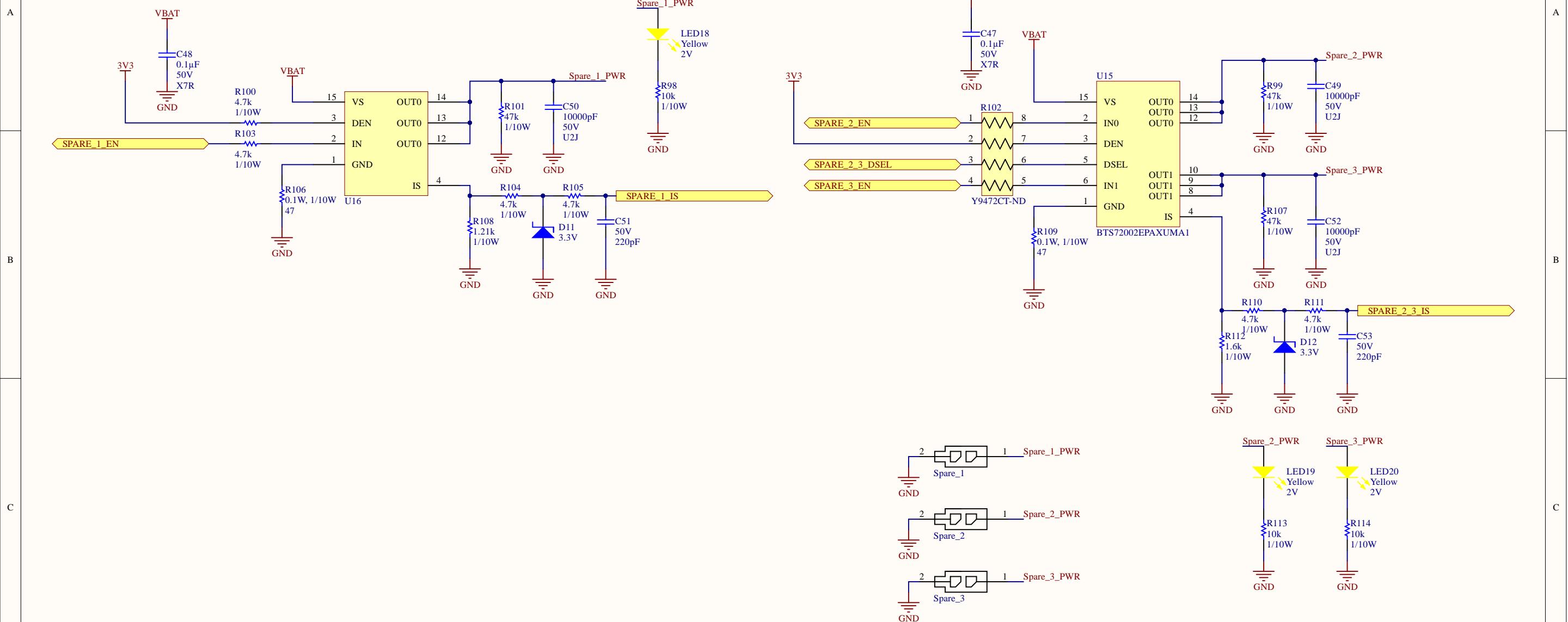
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 University of Waterloo  
 (519) 888-4567 x32978  
 hardware@uwmidsun.com



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	 MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	
SHEET * OF *		Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com

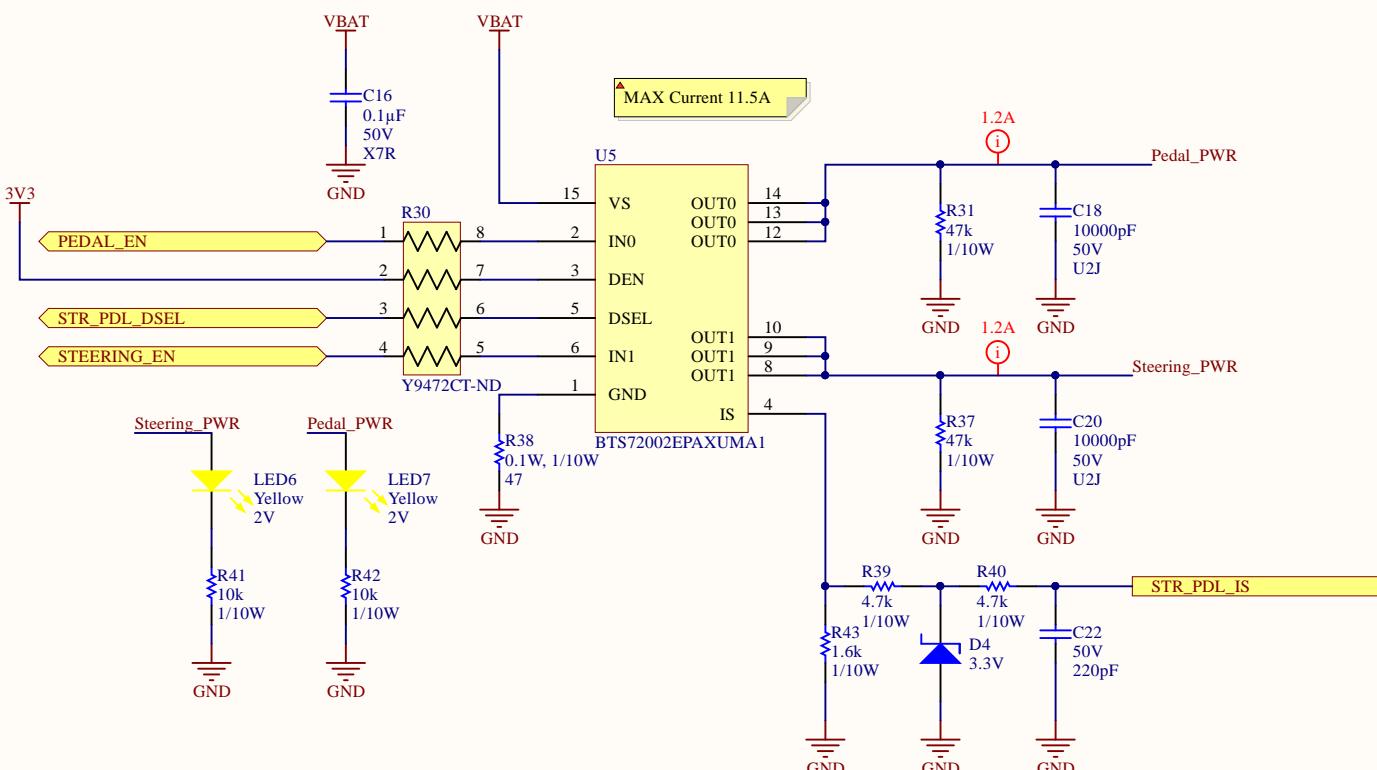


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-24
	SHEET * OF *

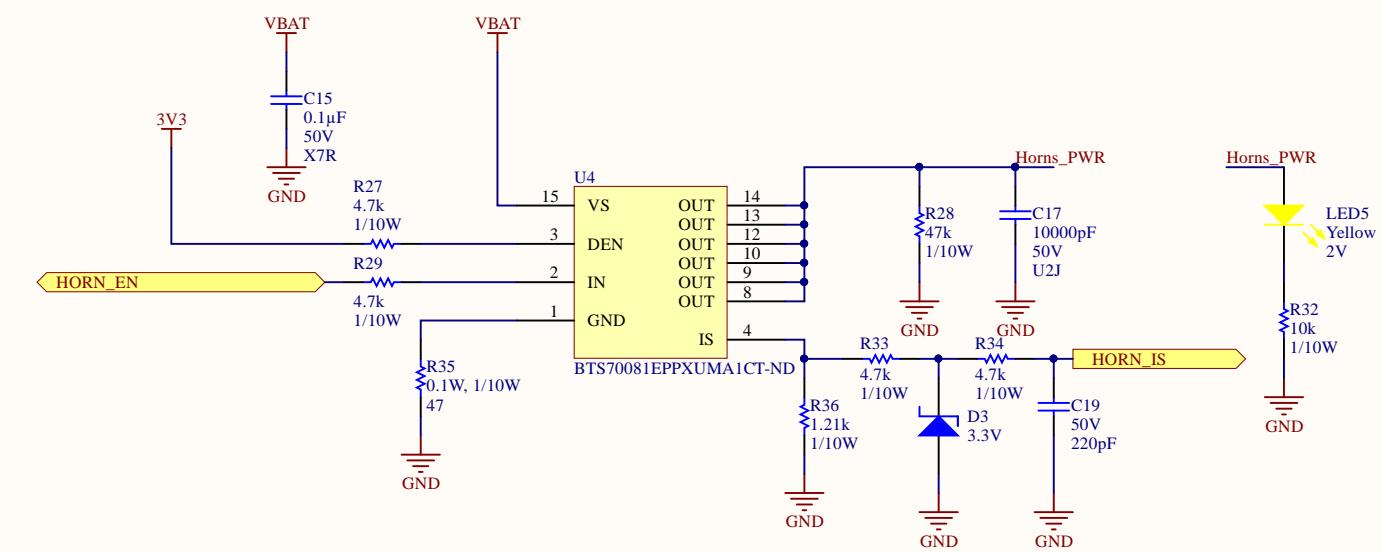


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	
SHEET *	OF *	

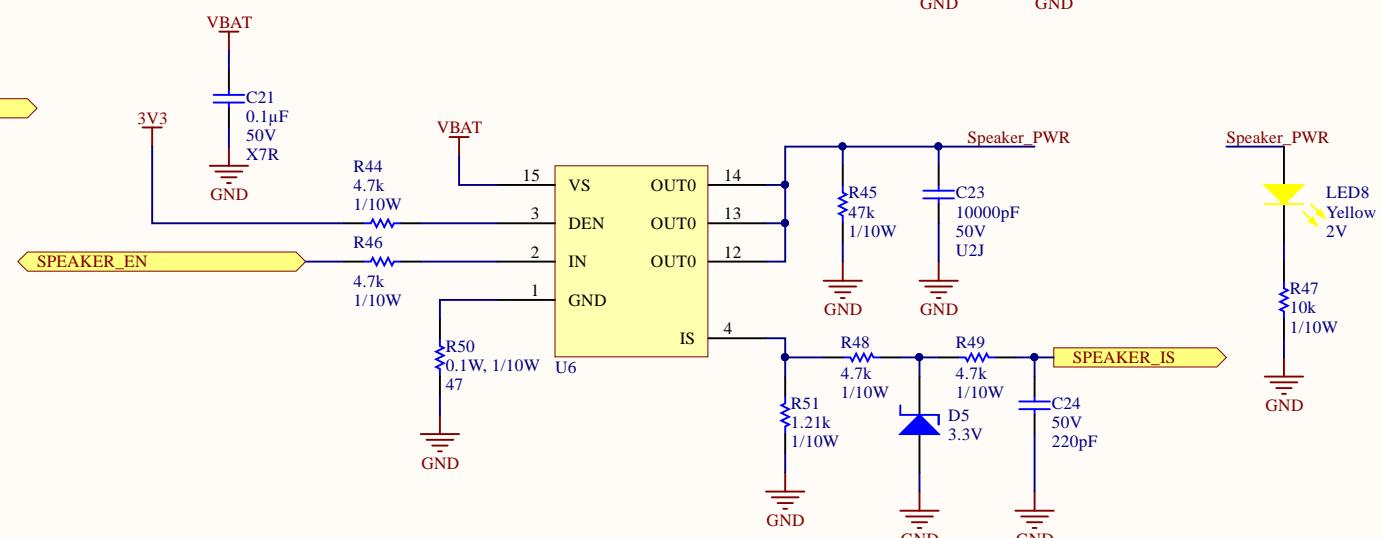
A A



B B

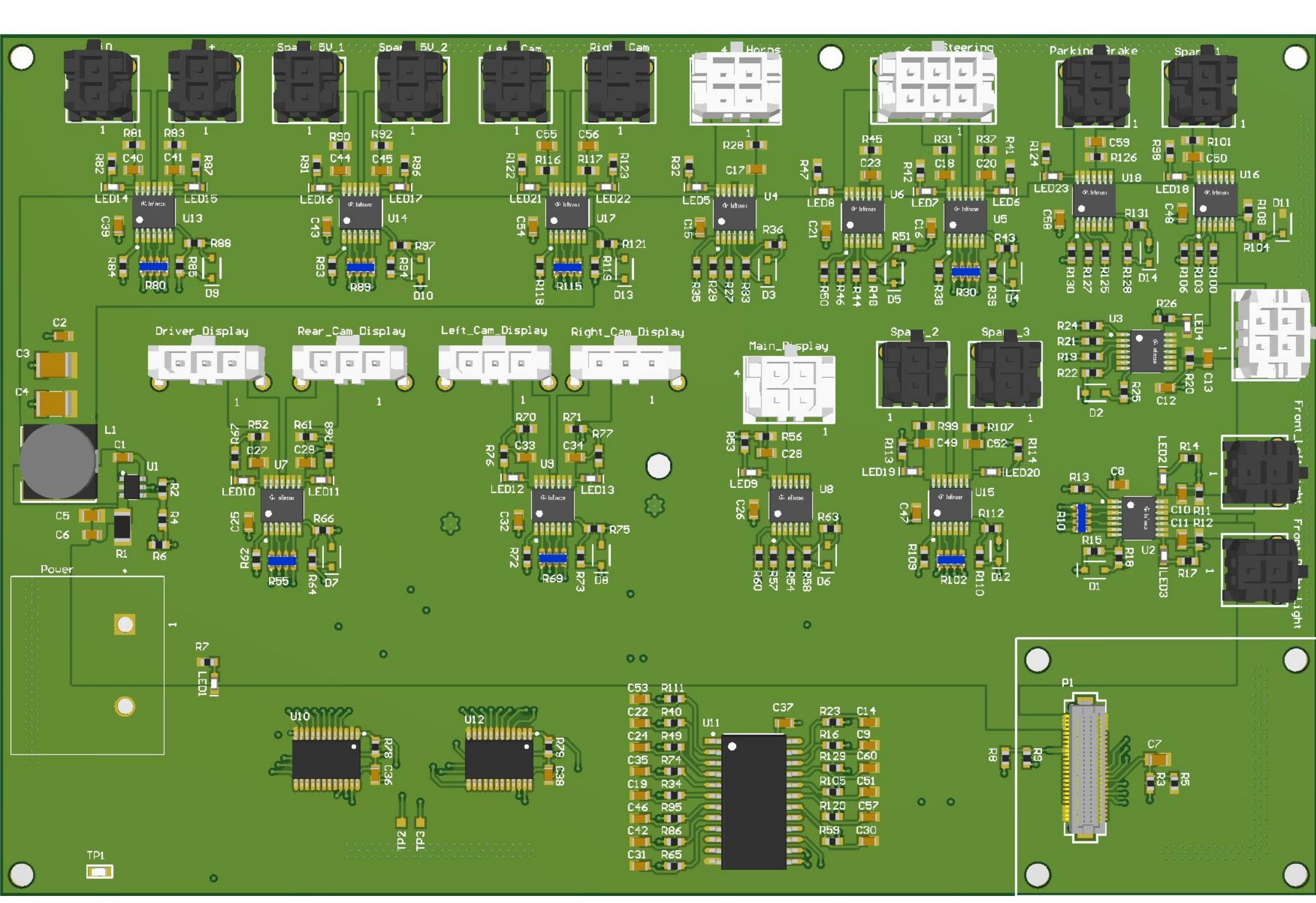


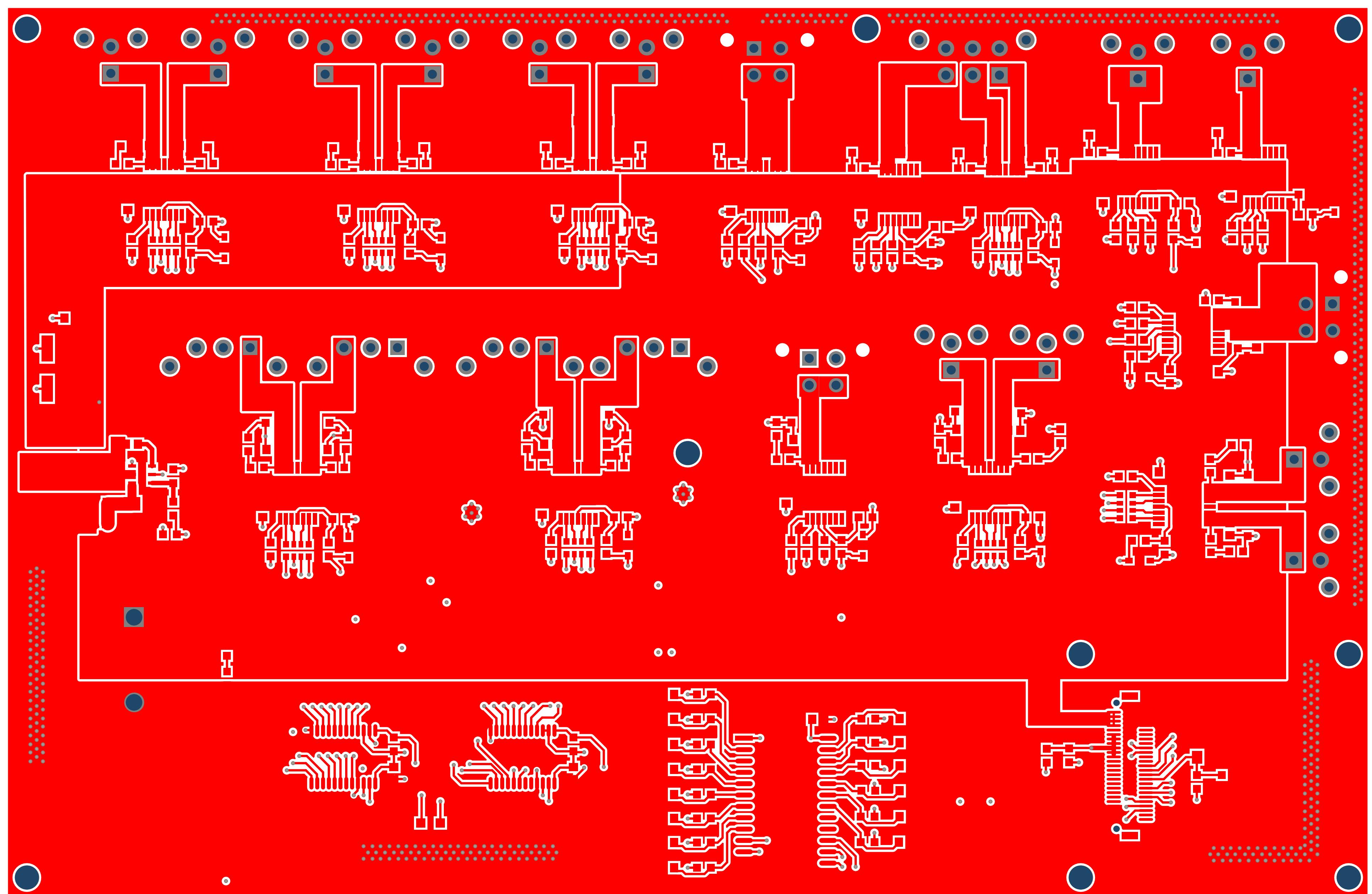
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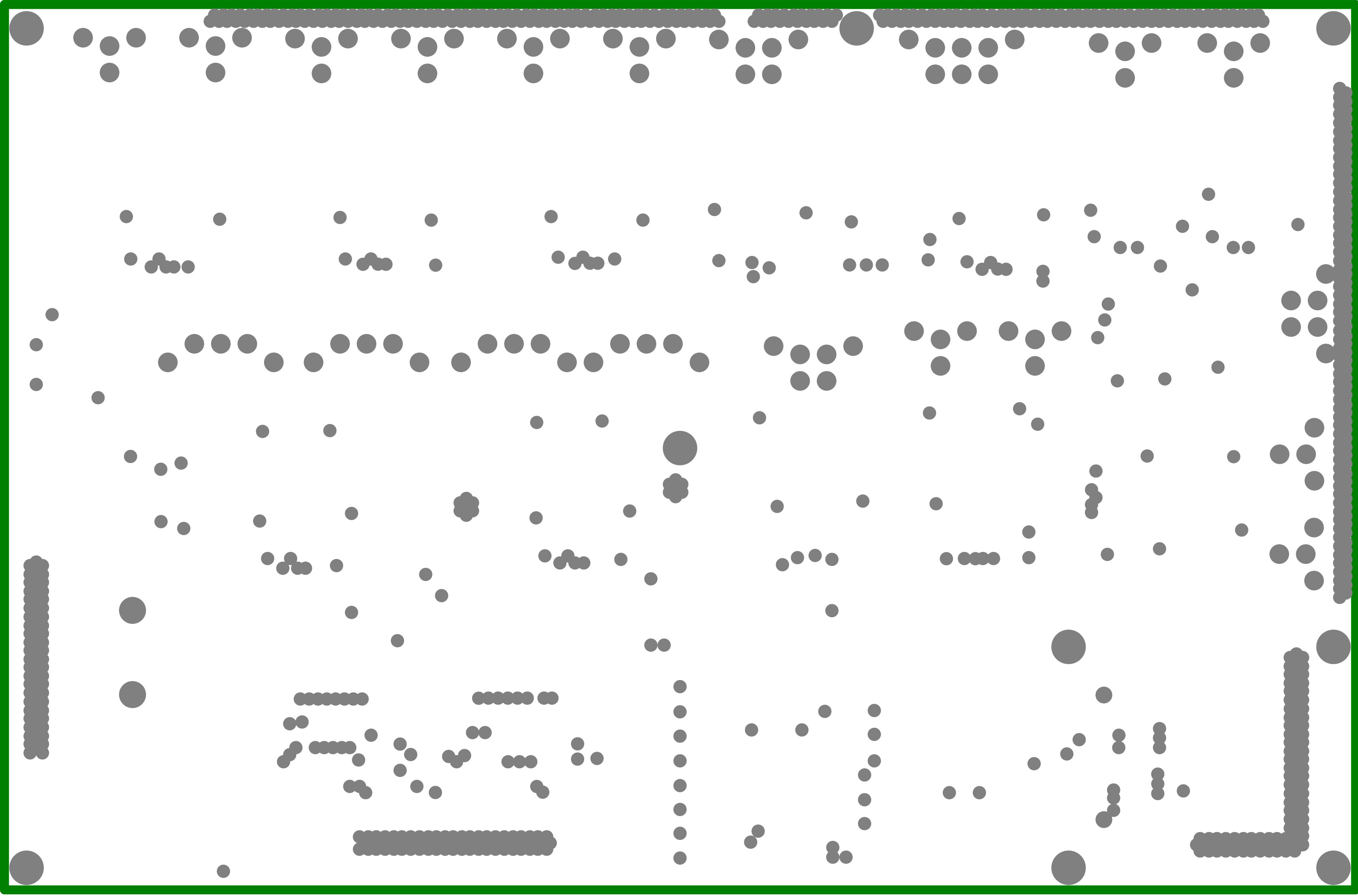


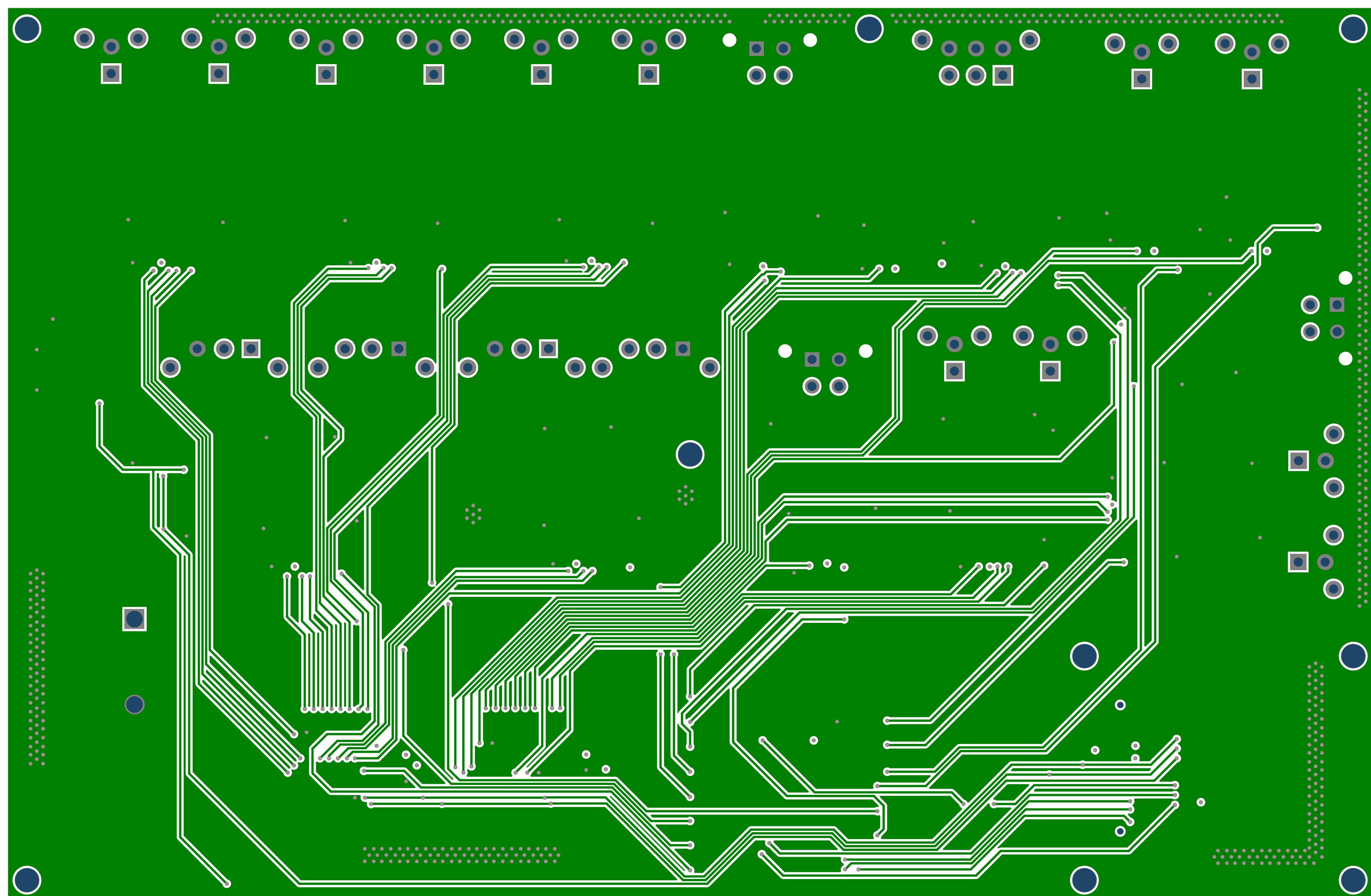
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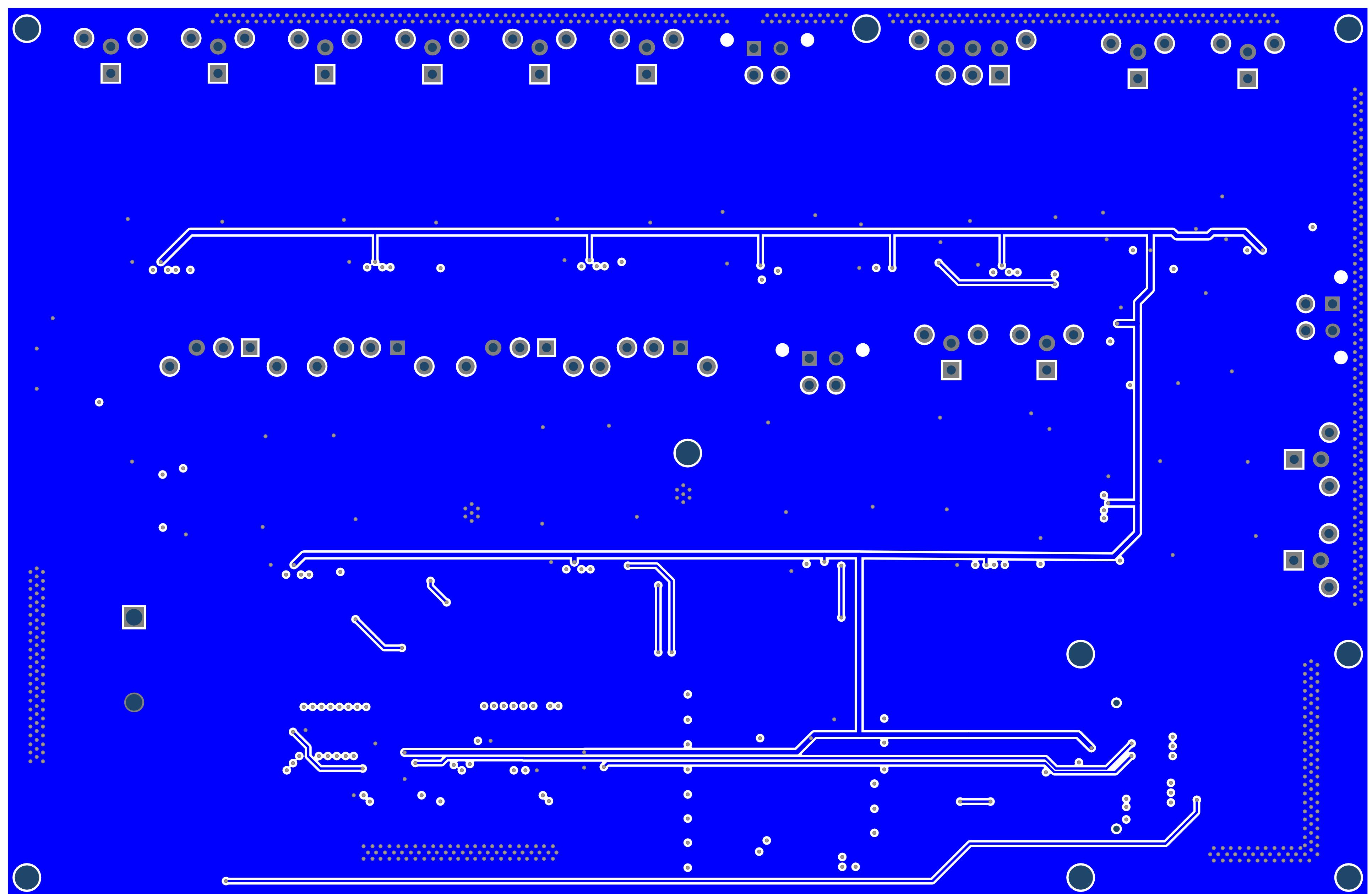
PROJECT	MSXIV_Front_Power_Distribution.PrbPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	SHEET * OF *

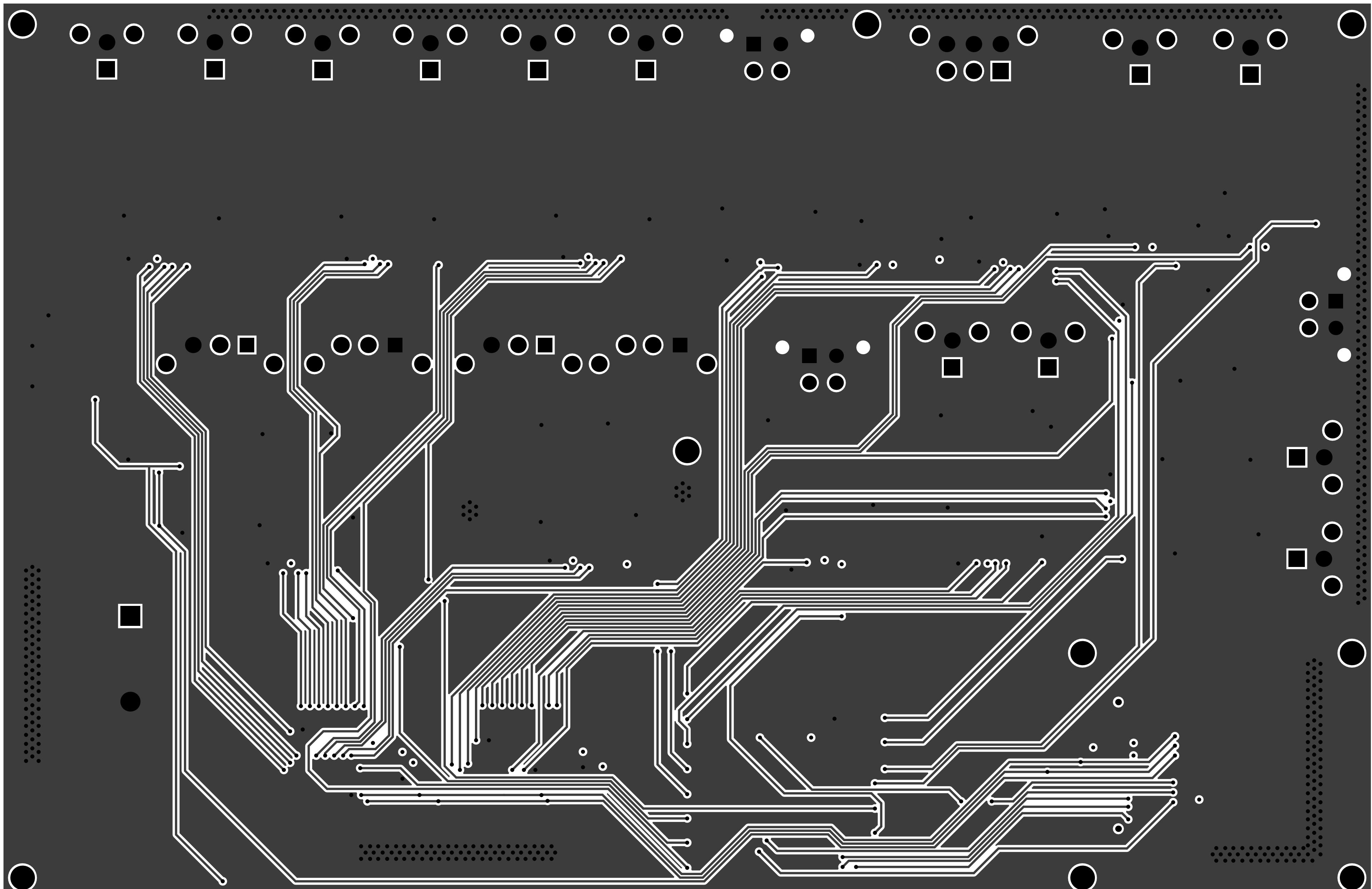


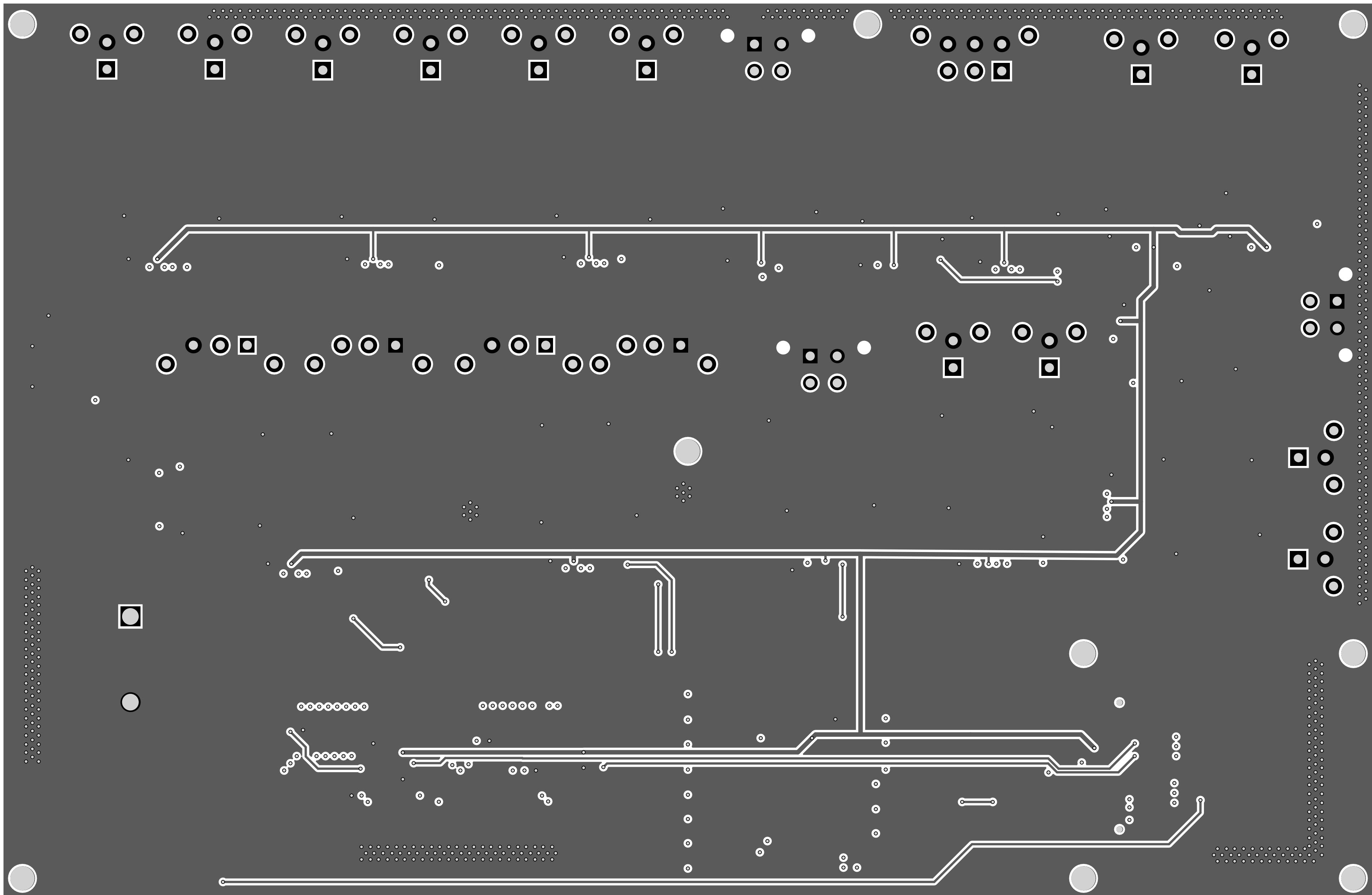


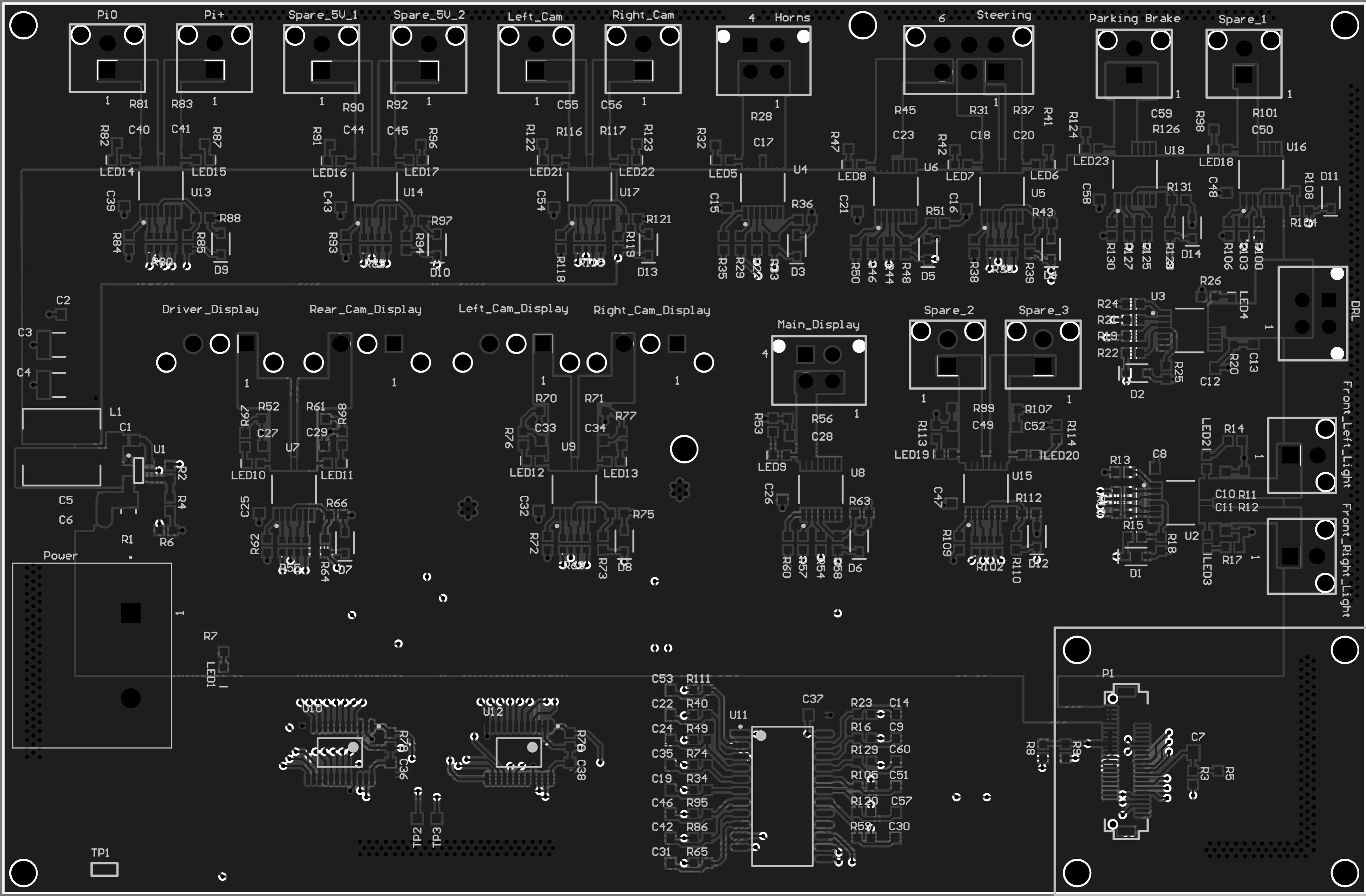












## Bill of Materials

Project:	SXIV_Front_Power_Distribution.PrjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2020-02-24 11:54 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	270

MIDNIGHT SUN

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CAP_CER_0.1UF_50V_10%_X7R_0603	C16,C21,C25,C26,C32,C36,C37,C38,C38	Kyocera AVX	0603C5C104KAT2A	Digi-Key	478-5052-1-ND	0.09291	20	\$ 1.86
CAP_CER_0.22UF_16V_±20%_X5R_1210	C3,C4	Murata	GRM32ER61C22GME20L	Digi-Key	490-1881-1-ND	2.59	2	\$ 5.18
CAP_CER_0.22UF_35V_X5R_0805	C5	TDK	C2012X5R1V226M125AC	Digi-Key	445-14428-1-ND	1.51	1	\$ 1.51
CAP_CER_0.1UF_100V_10%_X7R_0805	C7	Murata	GCM21BR72A104KA37L	Digi-Key	490-4789-1-ND	0.42475	1	\$ 0.42
CAP_CER_0.22UF_50V_10%_NP0_0603	C122,C24,C30,C31,C35,C42,C46,C51,C	KEMET	C0603C22J5GACAUTO	Digi-Key	399-6868-1-ND	0.11681	14	\$ 1.64
CAP_CER_10nF_50V_5%_X7R_0603	C27,C28,C29,C33,C34,C40,C41,C44,C	KEMET	C0603C103J5ACTU	Digi-Key	399-1384-1-ND	0.29732	22	\$ 6.54
DIODE_ZENER_3.3V_200mW_SOD323	D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D	Vishay	BZK384C3V3-E3-08	Digi-Key	ZX384C3V3-E3-08GICTR	0.26414	14	\$ 3.70
CONN_4POS_MICRO-FIT3mm	/, Left_Cam_Display, Rear_Cam_Display, Rg	Molex	0436500315	Digi-Key	WM1918-ND	1.37	4	\$ 5.47
CONN_4POS_MICRO-FIT3mm	DRL_Horns, Main_Display	Molex	0430450427	Digi-Key	WM1067-ND	1.78	3	\$ 5.34
CONN_2POS_MICRO-FIT3mm	m, Parking_Brake, P10,P1+, Right_Cam, Spare	Molex	0430450227	Digi-Key	WM10657-ND	0.98222	12	\$ 11.79
IND_3.5uH_5.2A_20MHzMSMD	L1	TDK	VLP8040T-3R3N	Digi-Key	445-6581-1-ND	1		
LED_GREENCLEAR2V_0603	LED1	Wurth Electronics	1500600VST5000	Digi-Key	732-4980-1-ND	0.18583	1	\$ 0.19
LED_YELLOWCLEAR2V_0603	LED11,LED12,LED13,LED14,LED15,LE	Wurth Electronics	1500600VST5000	Digi-Key	732-4981-1-ND	0.18583	22	\$ 4.09
CONN_50POS_Bergstak_Plug_0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.91	1	\$ 1.91
CONN_BARRIER_STRIP_2CIRCO_3/5"	Power	BUCHANAN-TE CONNECTIVITY	6PCV-02-000	Digi-Key	A98481-ND	2.16	1	\$ 2.16
RES_0.006_OHM_1/2W_1206	R1	Panasonic	ERJMP2KF6M0U	Digi-Key	P19333CTND	1		
RES_54.9K_OHM1%_1/10W_0603	R2	Panasonic	ERJ-3EKF5492V	Digi-Key	P54.9KHCTND	0.13273	1	\$ 0.13
RES_100K_OHM5%_1/8W_0603	R3	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCR-TND	0.13273	1	\$ 0.13
RES_10K_OHM1%_1/10W_0603	R47,R53,R67,R68,R76,R77,R82,R87,R91	Yageo Phycmp	RC0603FR-0710KL	Digi-Key	311-100KHRCR-TND	0.03053	25	\$ 0.76
RES_4.7K_OHM1%_1/10W_0603	R57,R58,R59,R64,R65,R73,R74,R78,R7	Yageo Phycmp	RC0603FR-074K0L	Digi-Key	311-4.70KHRCR-TND	0.03053	45	\$ 1.37
RES_ARRAY_4RES_4.7K_OHM1206	R10,R30,R55,R69,R80,R89,R102,R15	Panasonic	EXB-38V4T2JV	Digi-Key	Y9472CTND	0.13273	8	\$ 1.06
RES_47K_OHM1%_1/10W_0603	R52,R56,R61,R70,R71,R81,R83,R90,R92	Panasonic	ERJ3EKF4702V	Digi-Key	P47.0KHCTND	0.07566	22	\$ 1.66
RES_SMD_47_OHM_1%_1/10W_0603	R38,R50,R60,R62,R72,R84,R93,R106,R1	Yageo	AC0603FR-0747R	Digi-Key	311-47LDC-TND	0.03717	14	\$ 0.52
RES_1.6K_OHM1%_1/10W_0603	R18,R43,R66,T57,R88,R97,R112,R121	Yageo	RC0603FR-0711KL	Digi-Key	311-1.60KHRCR-TND	0.13273	8	\$ 1.06
RES_1.21K_OHM1%_1/10W_0603	R25,R36,R51,R63,R108,R131	Yageo	RC0603FR-071K2L	Digi-Key	311-1.21KHRCR-TND	0.13273	6	\$ 0.80
CONN_6POS_MICRO-FIT3mm	Steering	Molex	43045-0627	Digi-Key	WM10673-ND	2.1	1	\$ 2.10
TestPoint0603SMD	TP1	CGS-TE CONNECTIVITY	RCU-0C	Digi-Key	A106145CTND	0.31856	1	\$ 0.32
REG_BUCK_4.5V_TO_17V_5A_SYNCHRONOUS	U1	Texas Instruments	TPS565201DDCT	Digi-Key	296-47501-1-ND	2.04	1	\$ 2.04
LOAD_SWITCH_BT57200-2EPAVG-TSDSO-14	U2,U5,U7,U9,U13,U14,U15,U17	Infineon	BT572002EPAXUJA1	Digi-Key	S72002EPAXUJA1CT-N	1.73	8	\$ 13.80
LOAD_SWITCH_BT570401EPAPG-TSDSO-14	U3,U6,U8,U16,U18	Infineon	BT570401EPAXUJA1	Digi-Key	S70401EPAXUJA1CT-N	1.77	5	\$ 8.83
IC_LOAD_SWITCH_BT570081EPPXUMA1	U4	Infineon	BT570081EPPXUMA1	Digi-Key	S70081EPPXUMA1CT-N	2.77	1	\$ 2.77
16-BIT12-BUS_and SMBUS_LOWPOWER	U10,U12	NXP USA	PCA9539PW/Q900J	Digi-Key	568-13622-1-ND	3.17	2	\$ 6.34
IC_MUX/DEMUX_1X16_24SSOP	U11	Texas Instruments	CD74HC4067M96	Digi-Key	296-29408-1-ND	0.9955	1	\$ 1.00
					Total:			\$ 96.49

## Design Rules Verification Report

Filename : D:\Josh9\Documents\Midnight Sun\hardware\MSXIV\_FrontPowerDistribution\Fron

Warnings 0

Rule Violations 98

Warnings	
Total	0
Rule Violations	
Clearance Constraint (Gap=0.254mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0.15mm) (All), (All)	50
Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)	48
Silk to Silk (Clearance=0.254mm) (All), (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	98

Minimum Solder Mask Sliver (Gap=0.15mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.15mm) Between Pad P1-(124.5mm,22.05mm) on Multi-Layer And Pad P1-(126mm,22.8mm) or
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.15mm) Between Pad P1-(124.5mm,7.95mm) on Multi-Layer And Pad P1-(126mm,7.2mm) or
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-1(124.9mm,45.28mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R10-2(124.9mm,44.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-1(109.12mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R102-2(110mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-3(110.8mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-5(111.68mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R102-6(110.8mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R102-7(110mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-3(124.9mm,43.6mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-5(126.3mm,42.72mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R10-6(126.3mm,43.6mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R10-7(126.3mm,44.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-1(64.62mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R115-2(65.5mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-3(66.3mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-5(67.18mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R115-6(66.3mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R115-7(65.5mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-1(110.82mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R30-2(111.7mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-3(112.5mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-5(113.38mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R30-6(112.5mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R30-7(111.7mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-1(31.52mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R55-2(32.4mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-3(33.2mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-5(34.08mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R55-6(33.2mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R55-7(32.4mm,39.8mm) on Component Side And Pac
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Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-3(64.6mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-5(65.48mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R69-6(64.6mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R69-7(63.8mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-1(16.62mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R80-2(17.5mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-3(18.3mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-5(19.18mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R80-6(18.3mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R80-7(17.5mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-1(40.62mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R89-2(41.5mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-3(42.3mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-5(43.18mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.15mm) Between Pad R89-6(42.3mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.15mm) Between Pad R89-7(41.5mm,73.8mm) on Component Side And Pac

Silk To Solder Mask (Clearance=0.15mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (109.062mm,38.038mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (110.762mm,71.438mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (124.438mm,45.338mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (16.562mm,72.038mm) on Top Overlay And Pad R80-1(16.62mm,72.5mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (31.462mm,37.938mm) on Top Overlay And Pad R55-1(31.52mm,38.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (40.562mm,71.938mm) on Top Overlay And Pad R89-1(40.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (62.862mm,38.238mm) on Top Overlay And Pad R69-1(62.92mm,38.7mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.15mm) Between Arc (64.562mm,71.938mm) on Top Overlay And Pad R115-1(64.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Left_Light-0(148.34mm,46.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Left_Light-0(148.34mm,52.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Right_Light-0(148.3mm,35mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.15mm) Between Pad Front_Right_Light-0(148.3mm,41mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.15mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.15mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Left_Cam-0(56.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Left_Cam-0(62.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Parking_Brake-0(123.9mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Parking_Brake-0(129.9mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi+-0(20.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi+-0(26.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi0-0(14.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Pi0-0(8.9mm,96.44mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Right_Cam-0(68.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Right_Cam-0(74.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_1-0(136.2mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_1-0(142.2mm,95.84mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_2-0(103mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_2-0(109mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_3-0(113.7mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_3-0(119.7mm,63.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_1-0(32.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_1-0(38.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_2-0(44.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Spare_5V_2-0(50.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Steering-0(102.4mm,96.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.15mm) Between Pad Steering-0(114.4mm,96.24mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.15mm) Between Pad TP1-1(10.8mm,2.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.15mm) Between Pad TP1-1(10.8mm,2.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.15mm) Between Pad TP1-1(12.35mm,2.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.15mm) Between Pad TP1-1(12.35mm,2.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.15mm) Between Pad TP1-1(12.35mm,2.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-1(14.275mm,48.55mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-2(14.275mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-3(14.275mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-4(16.525mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-5(16.525mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.15mm) Between Pad U1-6(16.525mm,48.55mm) on Component Side And Track