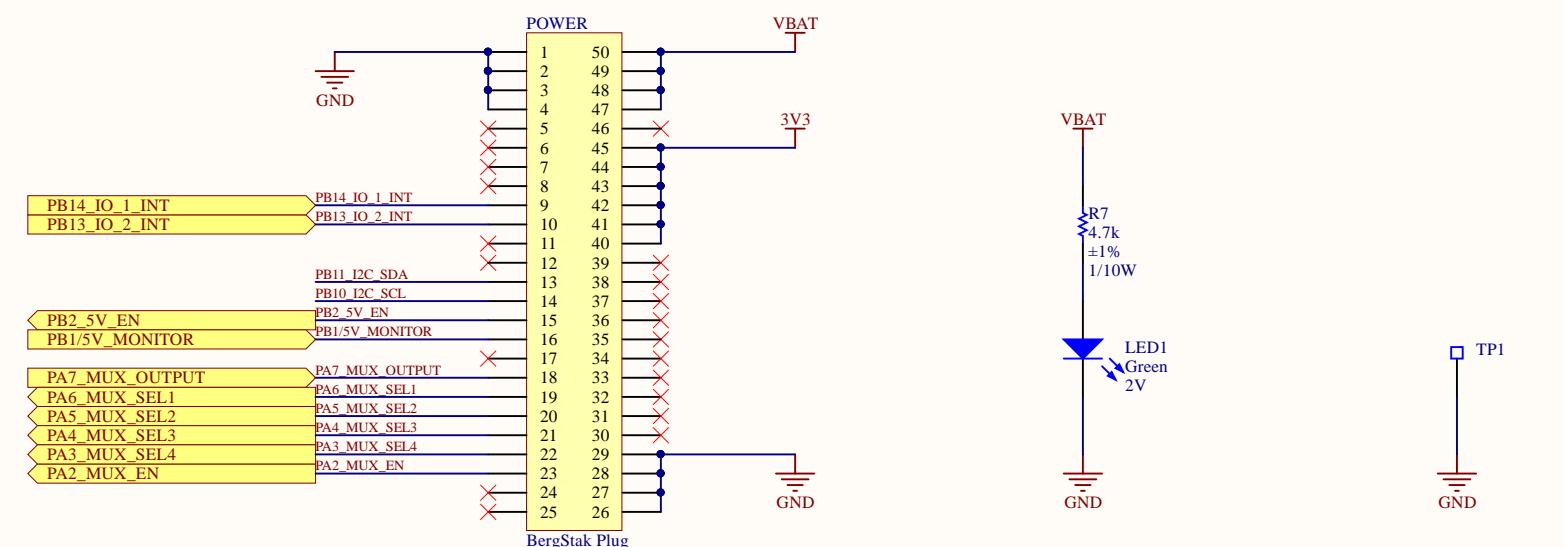
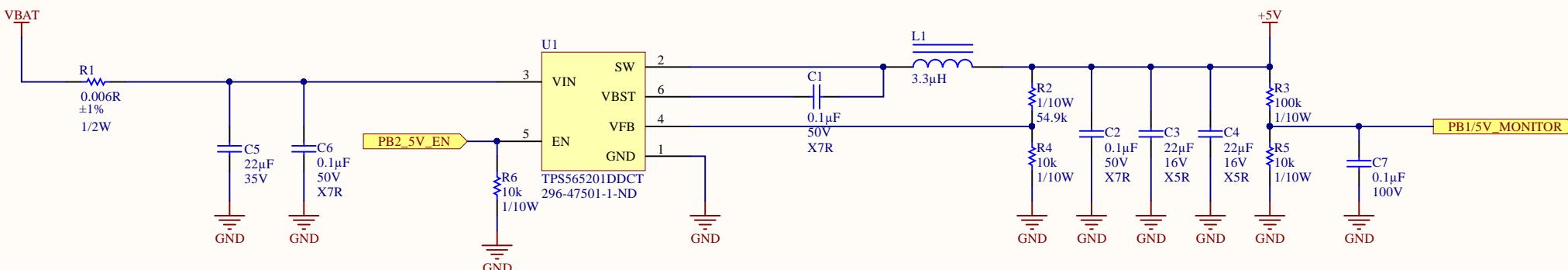
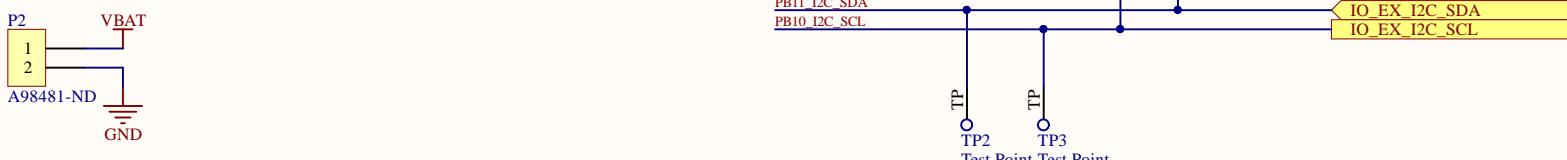


Regulator

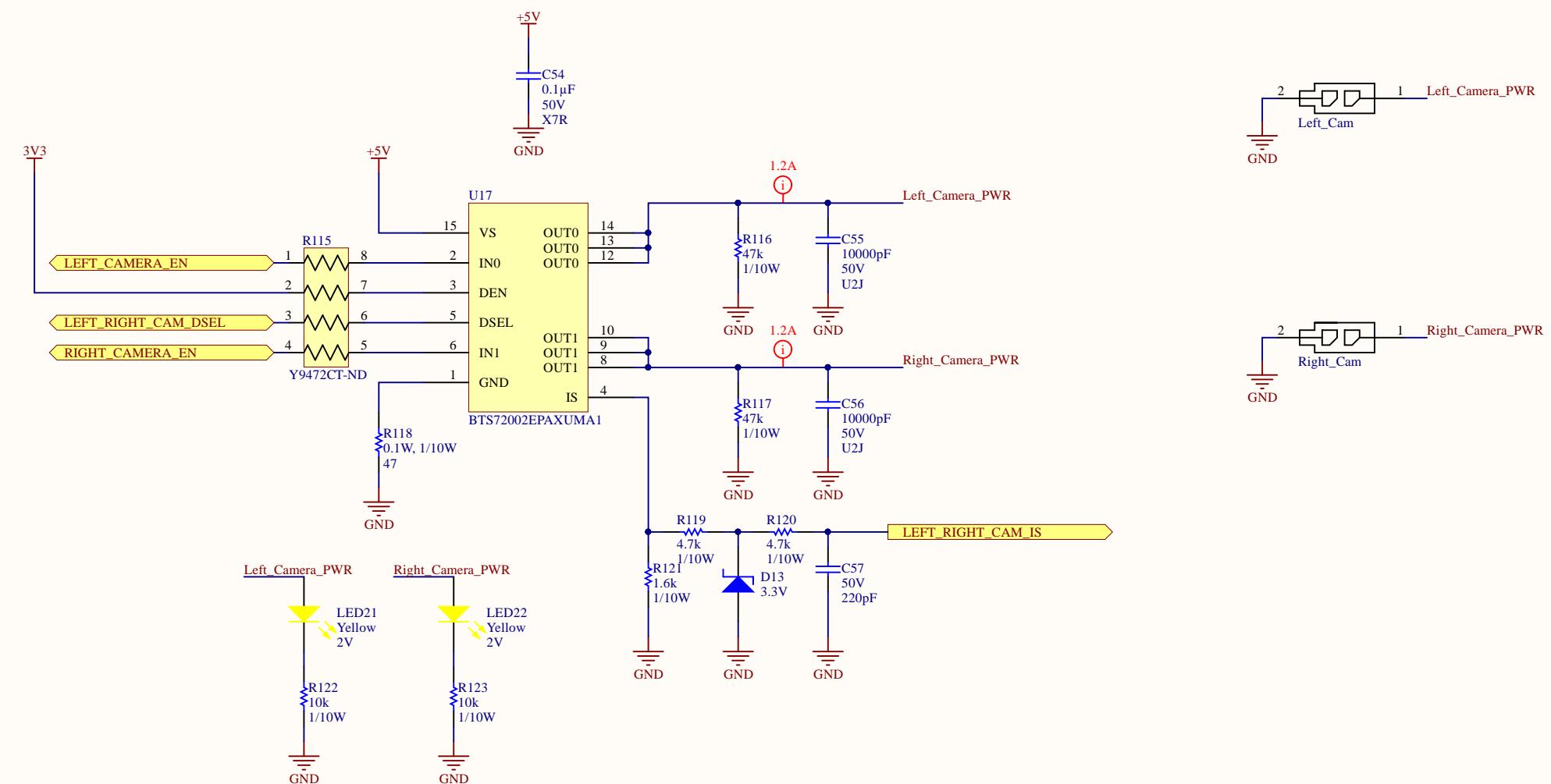


12V Power Connector



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Controller Board Interface
PART NUMBER	VARIANT [No Variations]
DRAWN BY	REVISION
LAST MODIFIED	2020-02-24
SHEET *	OF *

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PROJECT MSXIV_Front_Power_Distribution.PrjPcb

DOCUMENT Title

PART NUMBER VARIANT [No Variations]

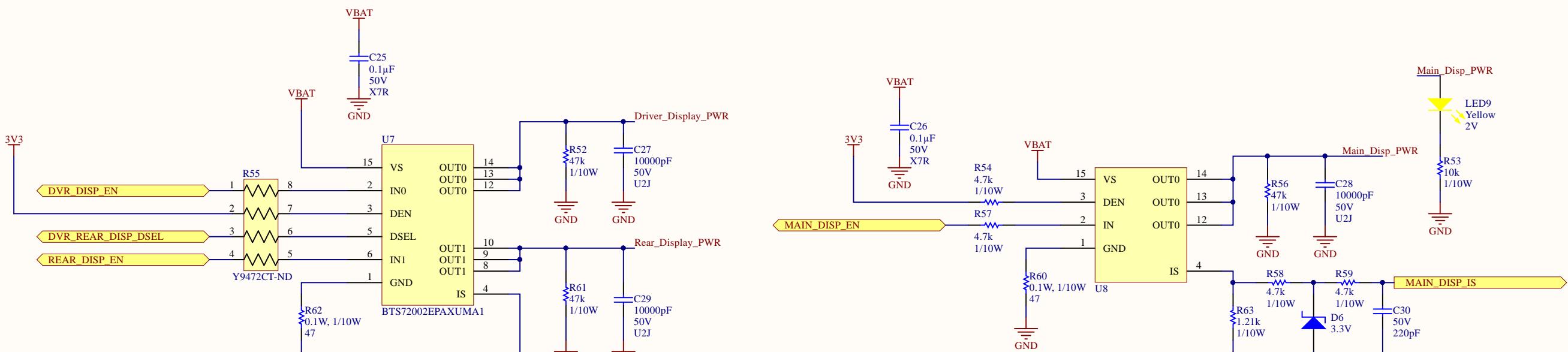
DRAWN BY REVISION

LAST MODIFIED 2020-02-24 SHEET * OF *

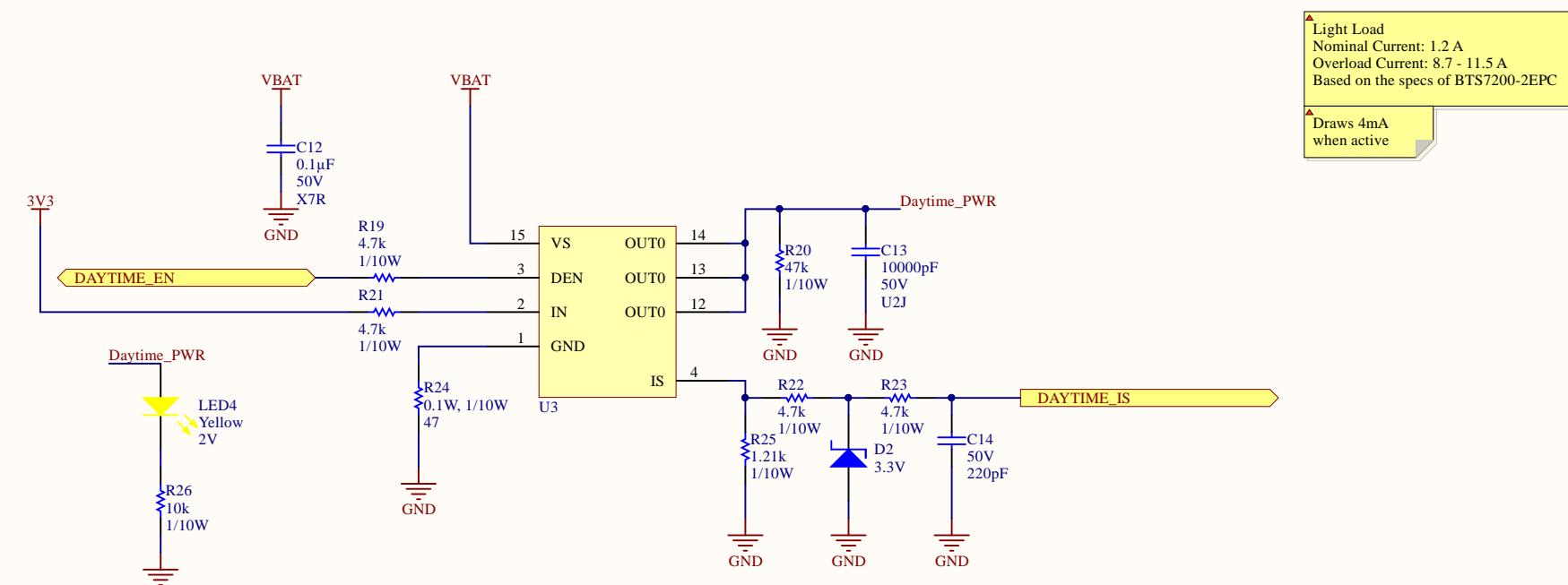
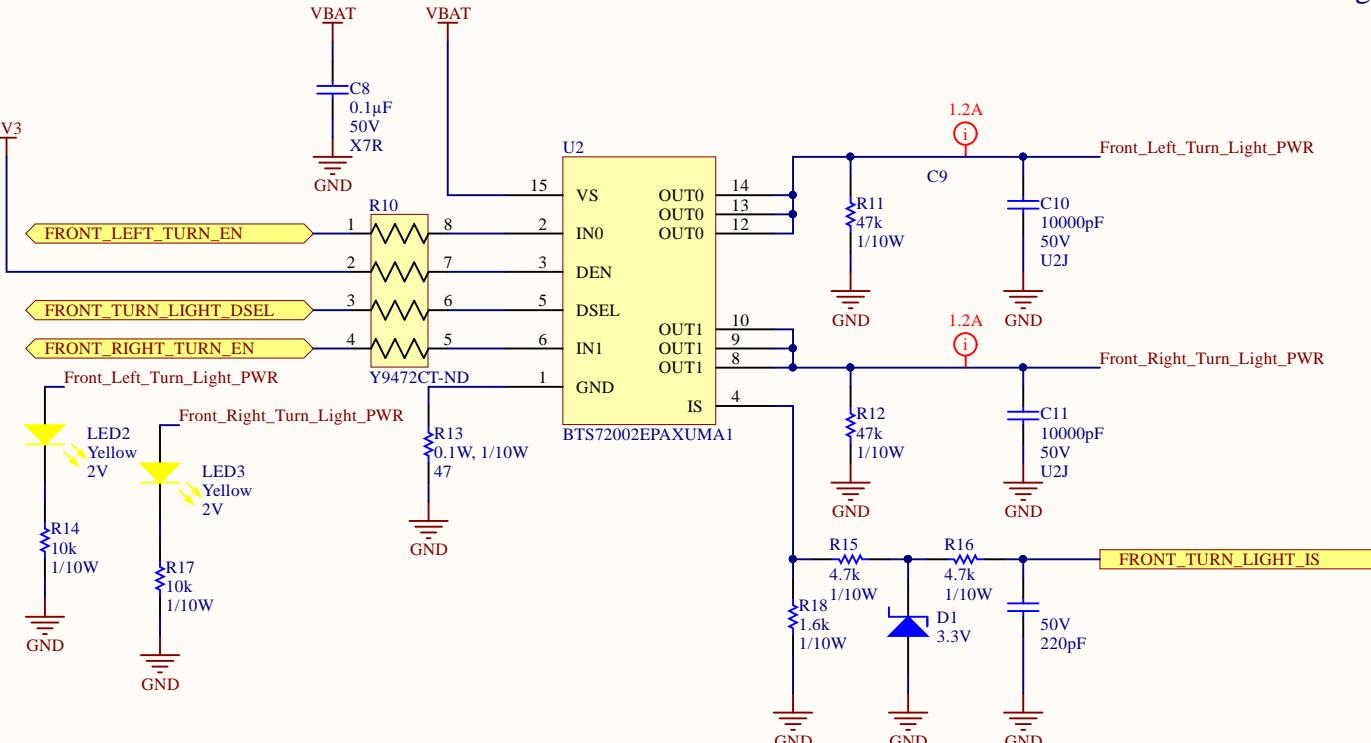


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University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

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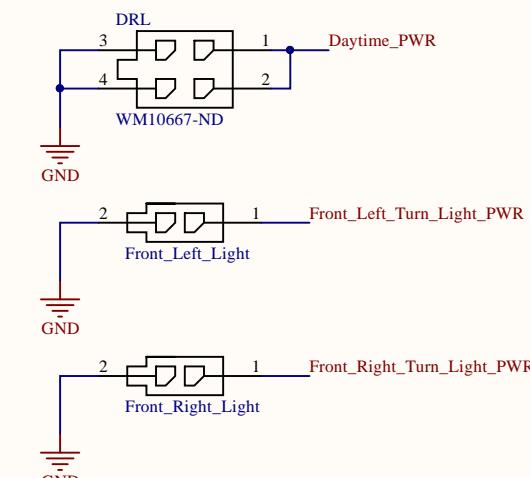


Front light



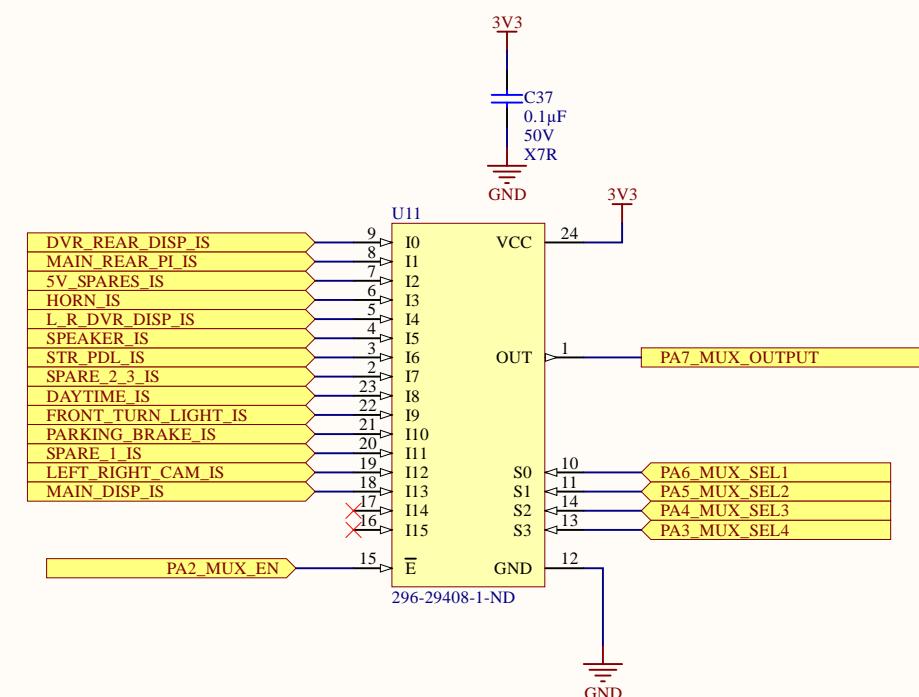
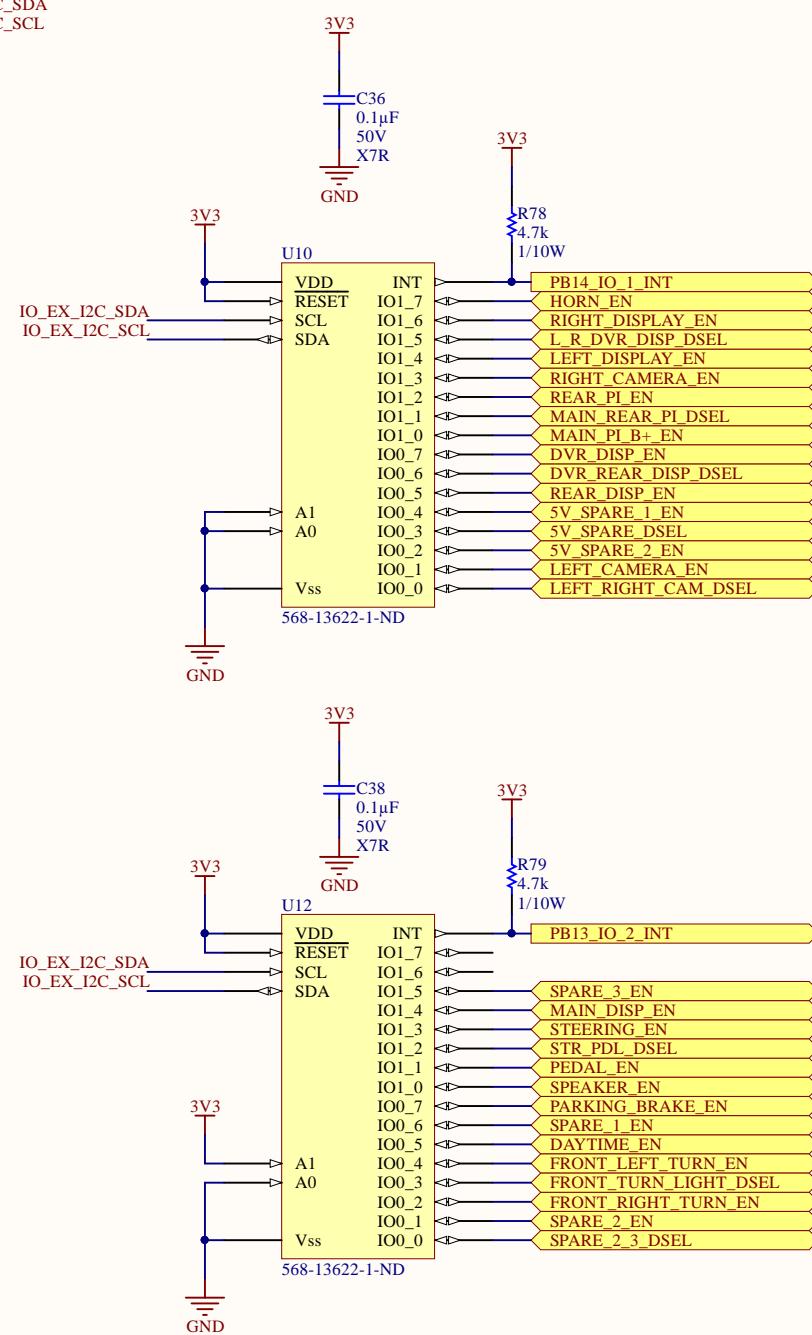
Light Load
Nominal Current: 1.2 A
Overload Current: 8.7 - 11.5 A
Based on the specs of BTS7200-2EPC

Draws 4mA when active



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	SHEET * OF *
hardware@uwmidsun.com		Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978

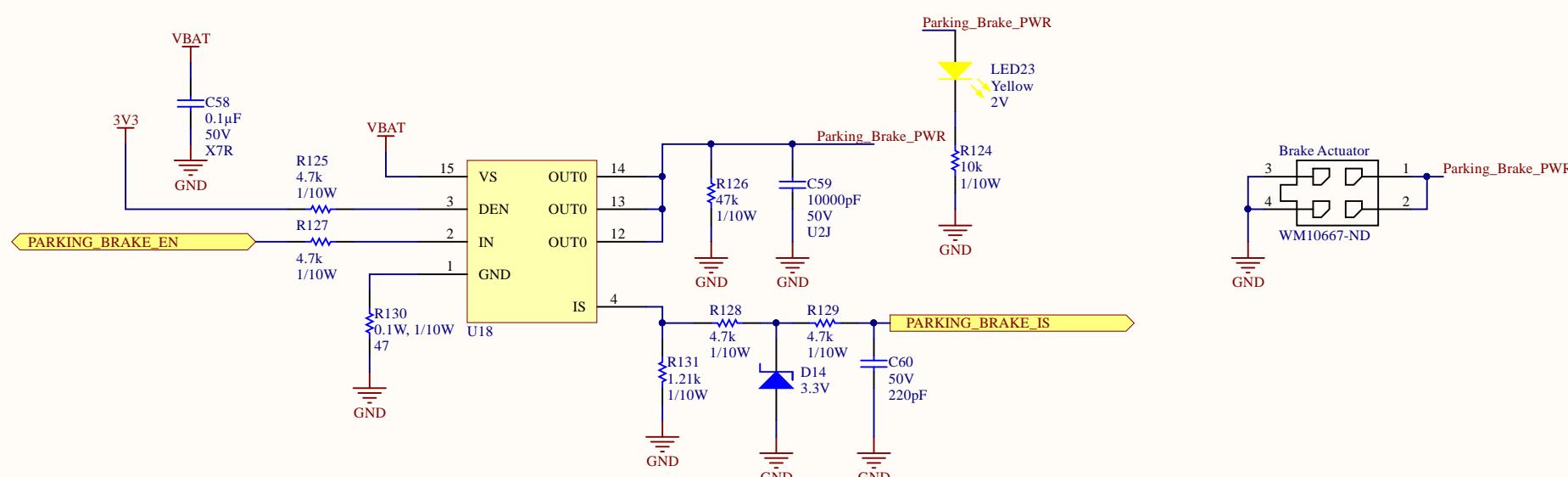
IO_EX_I2C_SDA
IO_EX_I2C_SCL



PROJECT	MSXIV_Front_Power_Distribution.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
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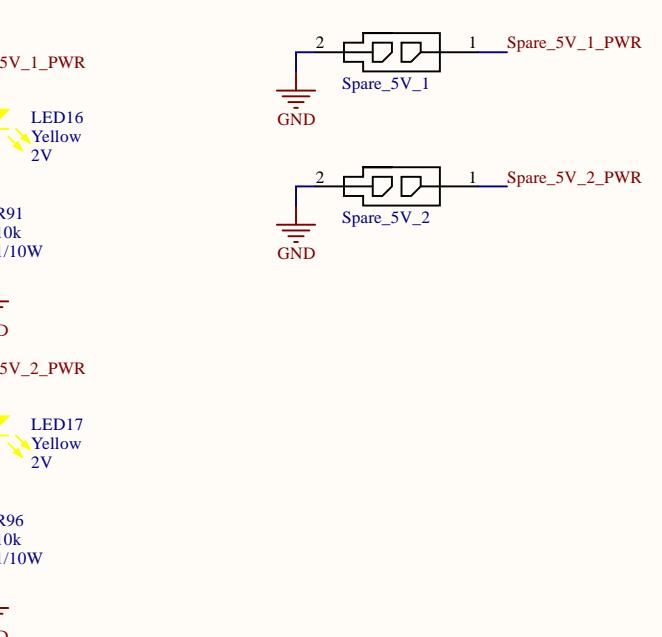
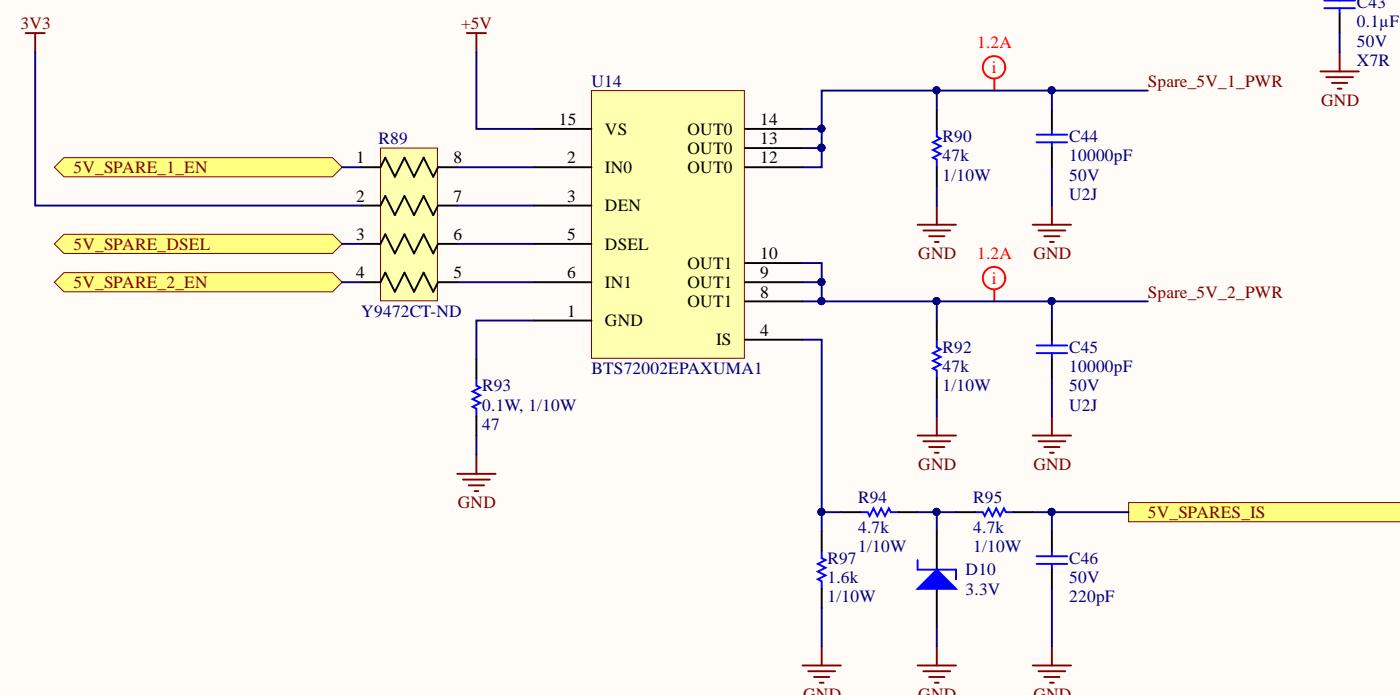
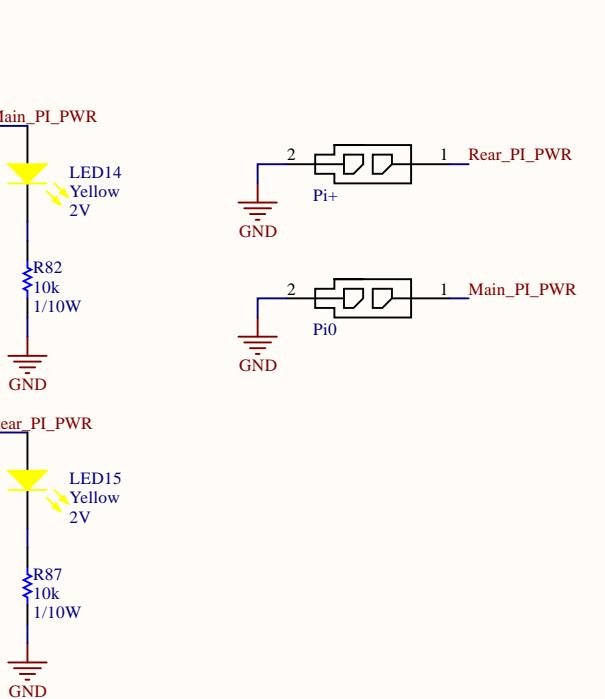
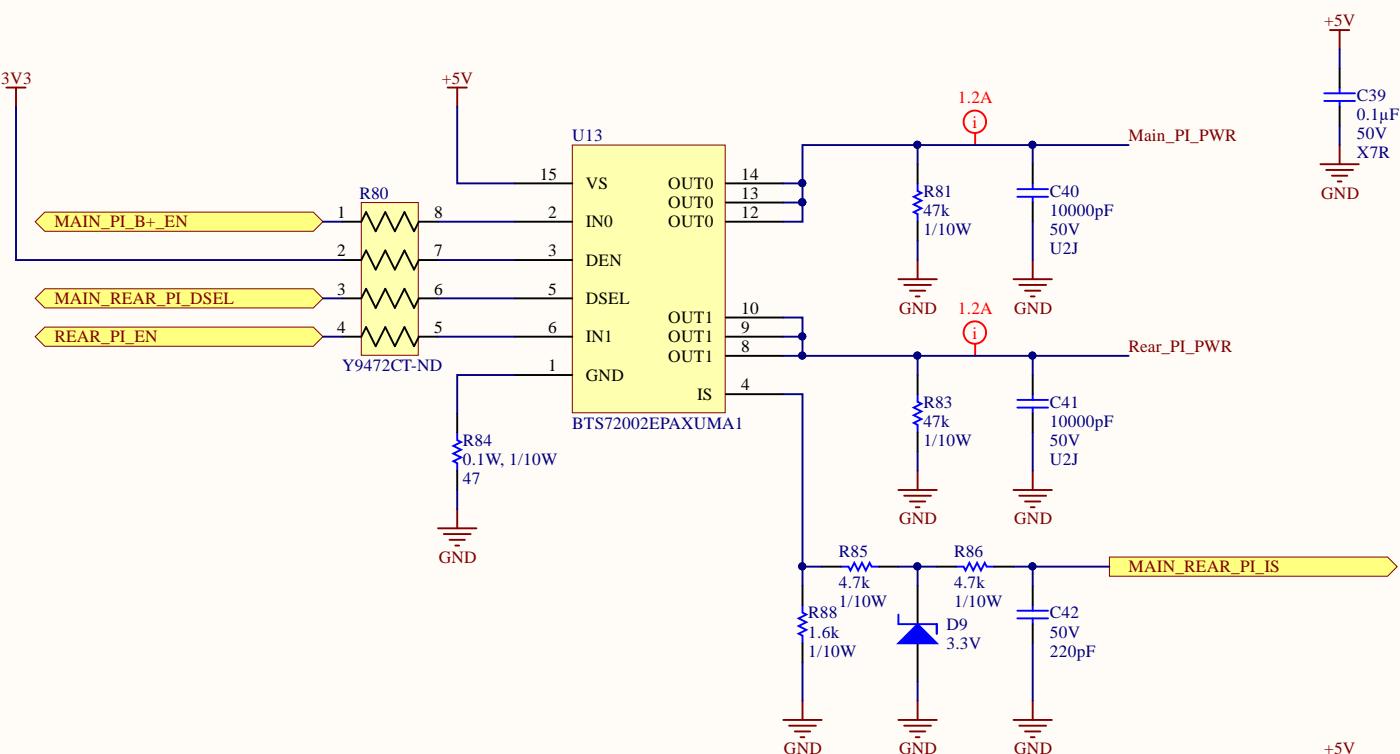
B

C

D

PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	SHEET * OF *

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PROJECT MSXIV_Front_Power_Distribution.PrjPcb

DOCUMENT Title

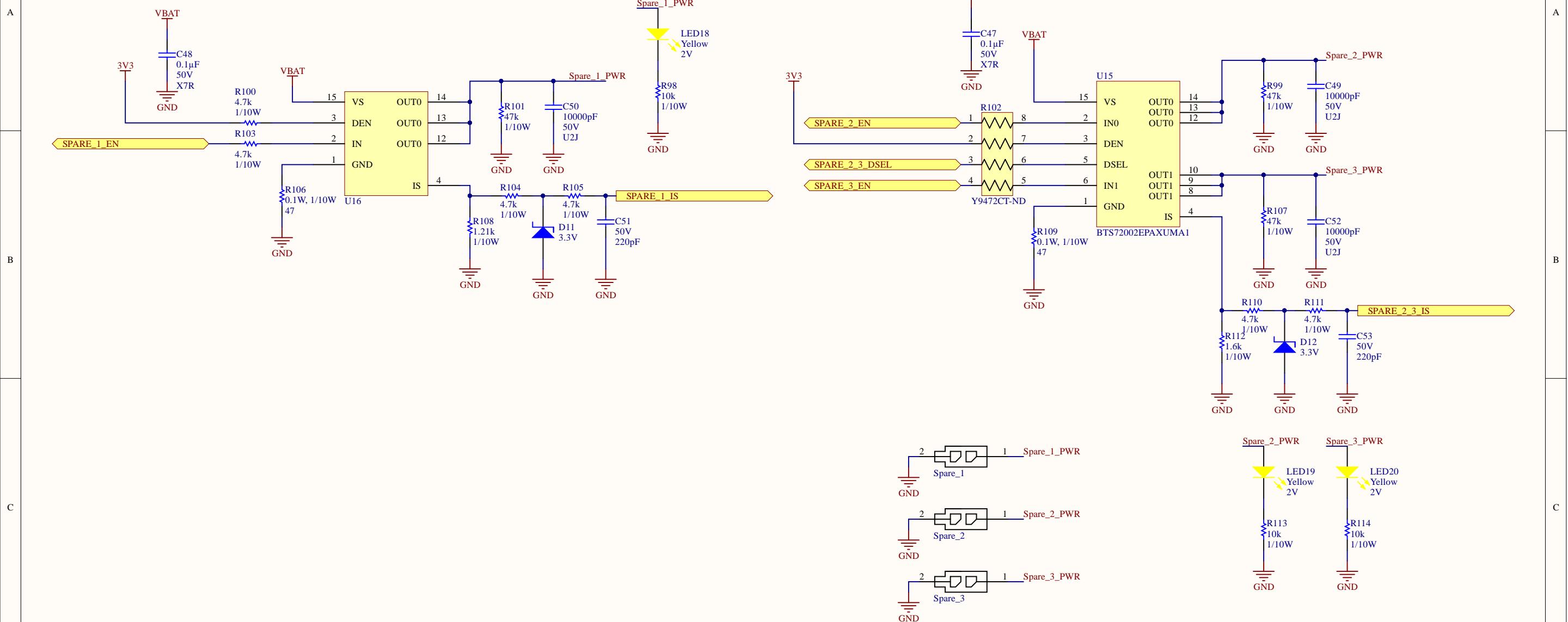
PART NUMBER VARIANT [No Variations]

DRAWN BY REVISION

LAST MODIFIED 2020-02-24 SHEET * OF *

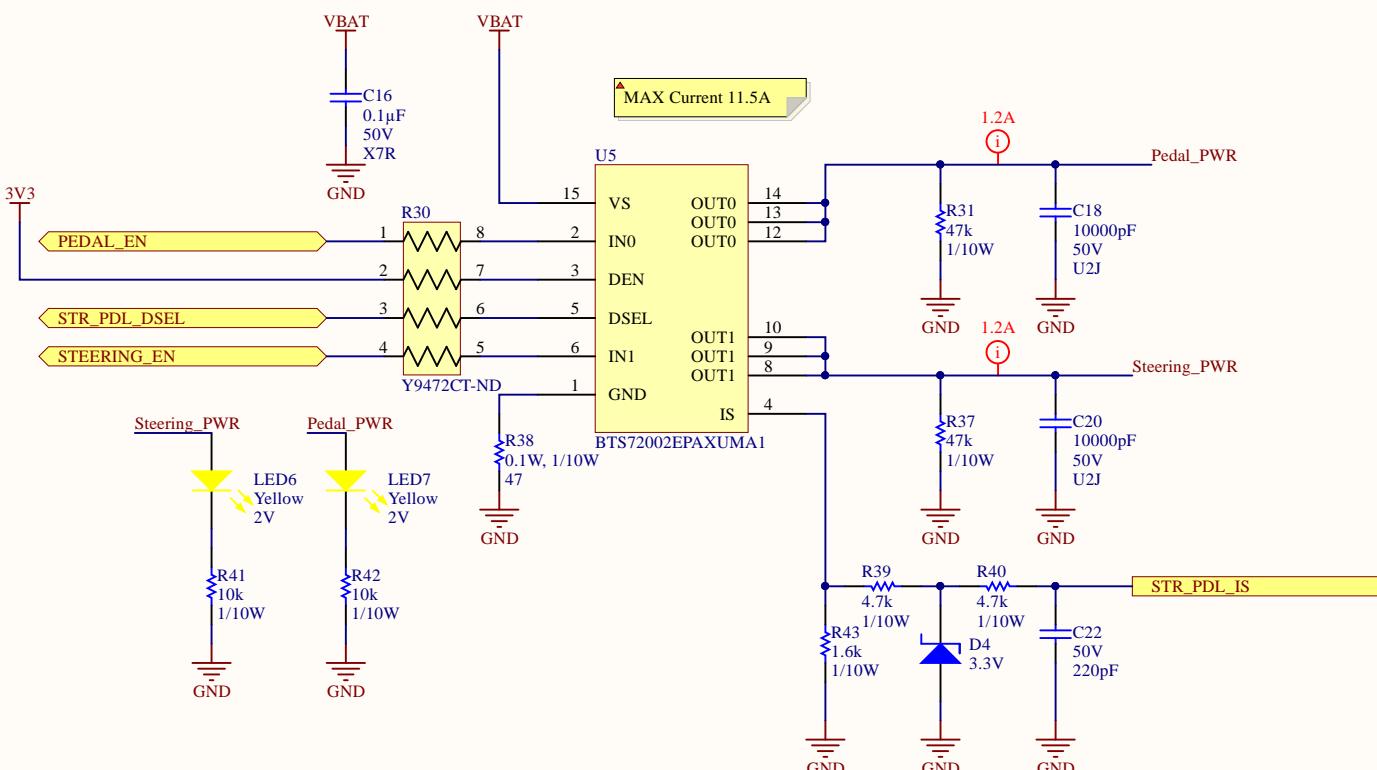


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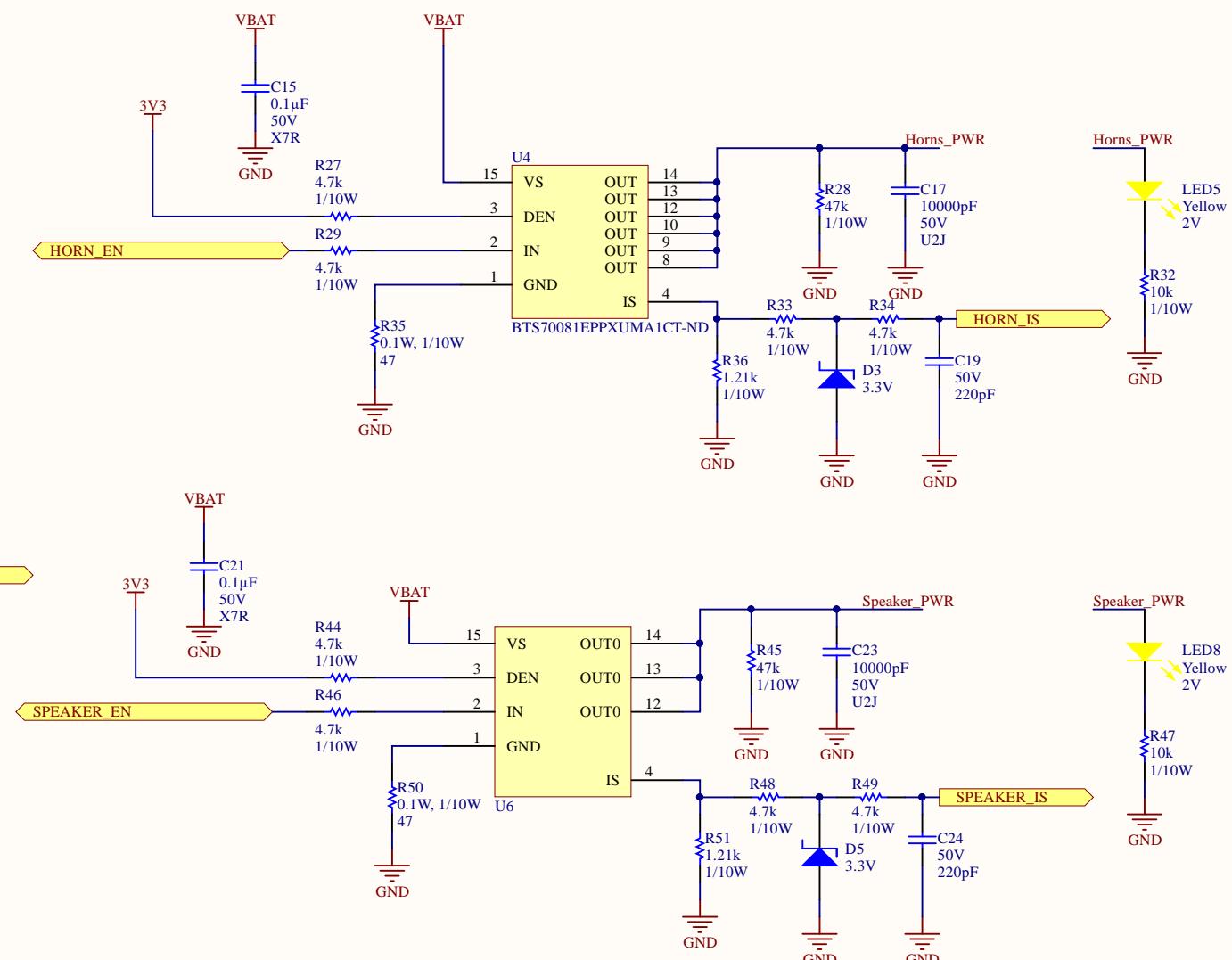


PROJECT	MSXIV_Front_Power_Distribution.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	
SHEET *	OF *	

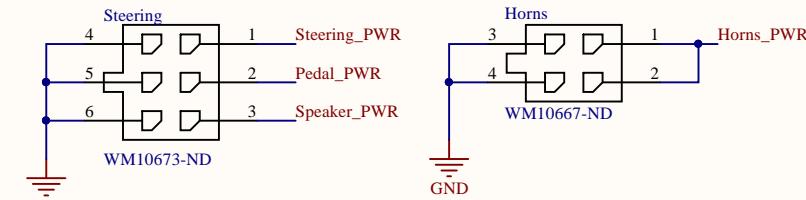
A A



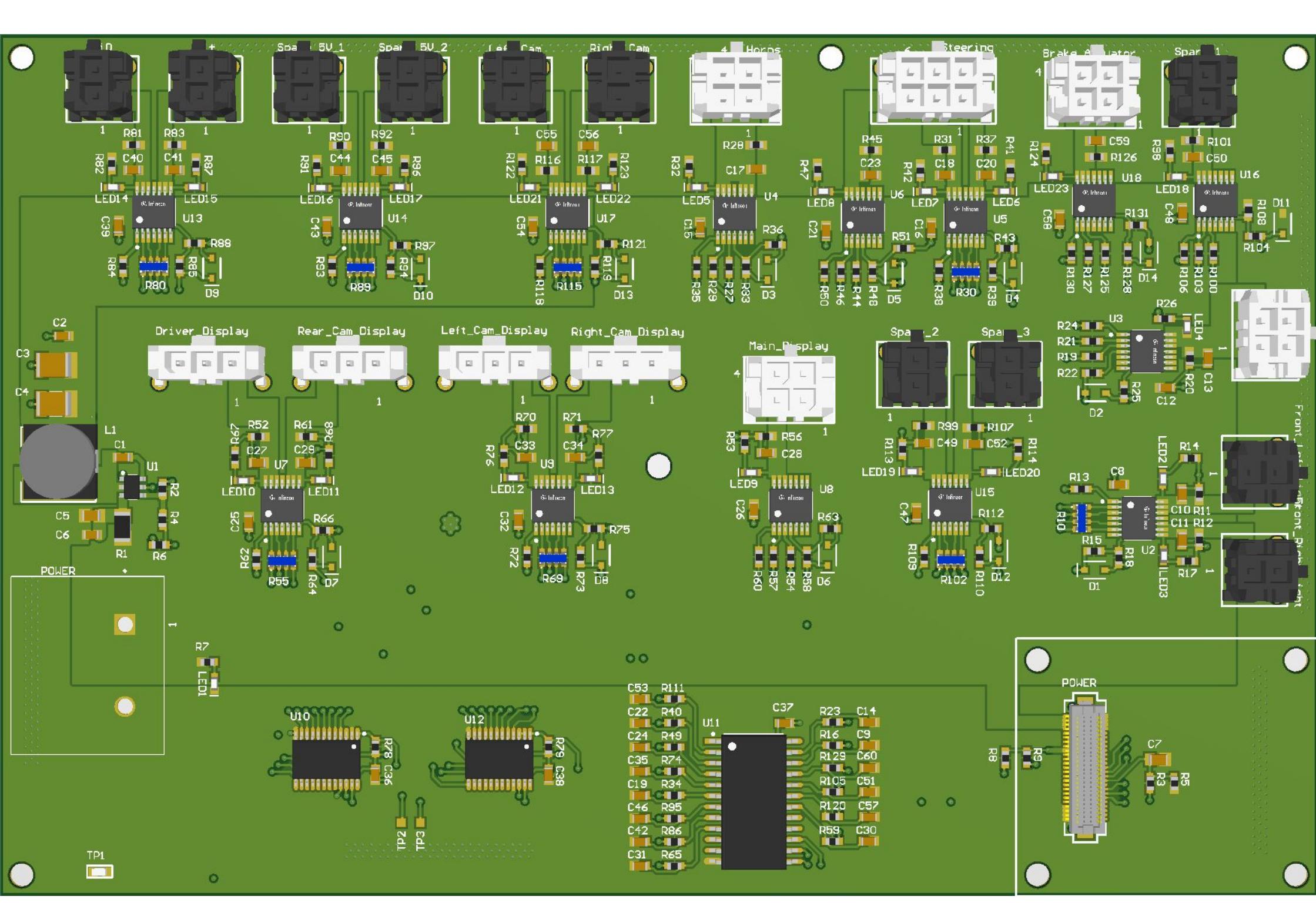
B B

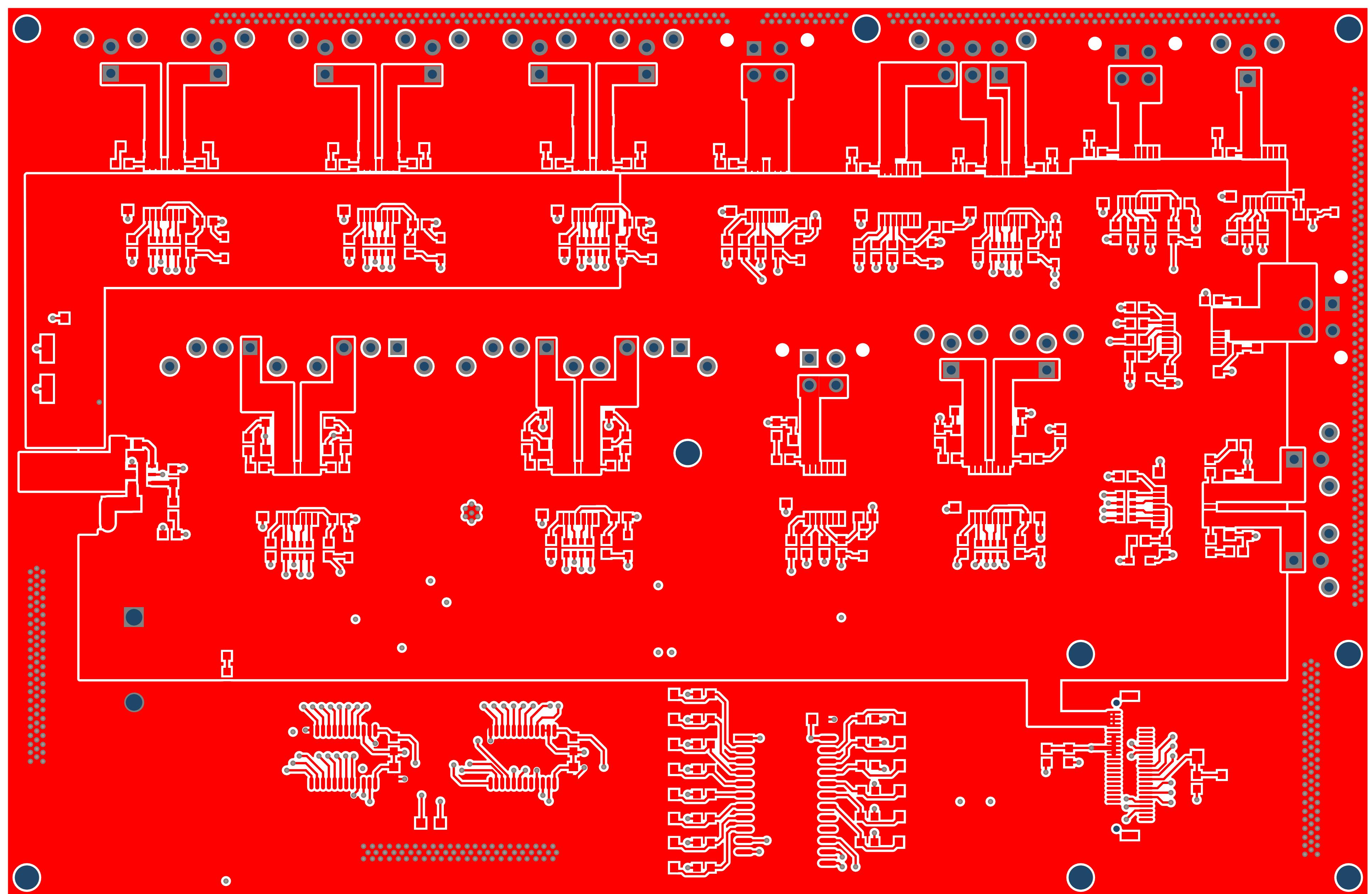


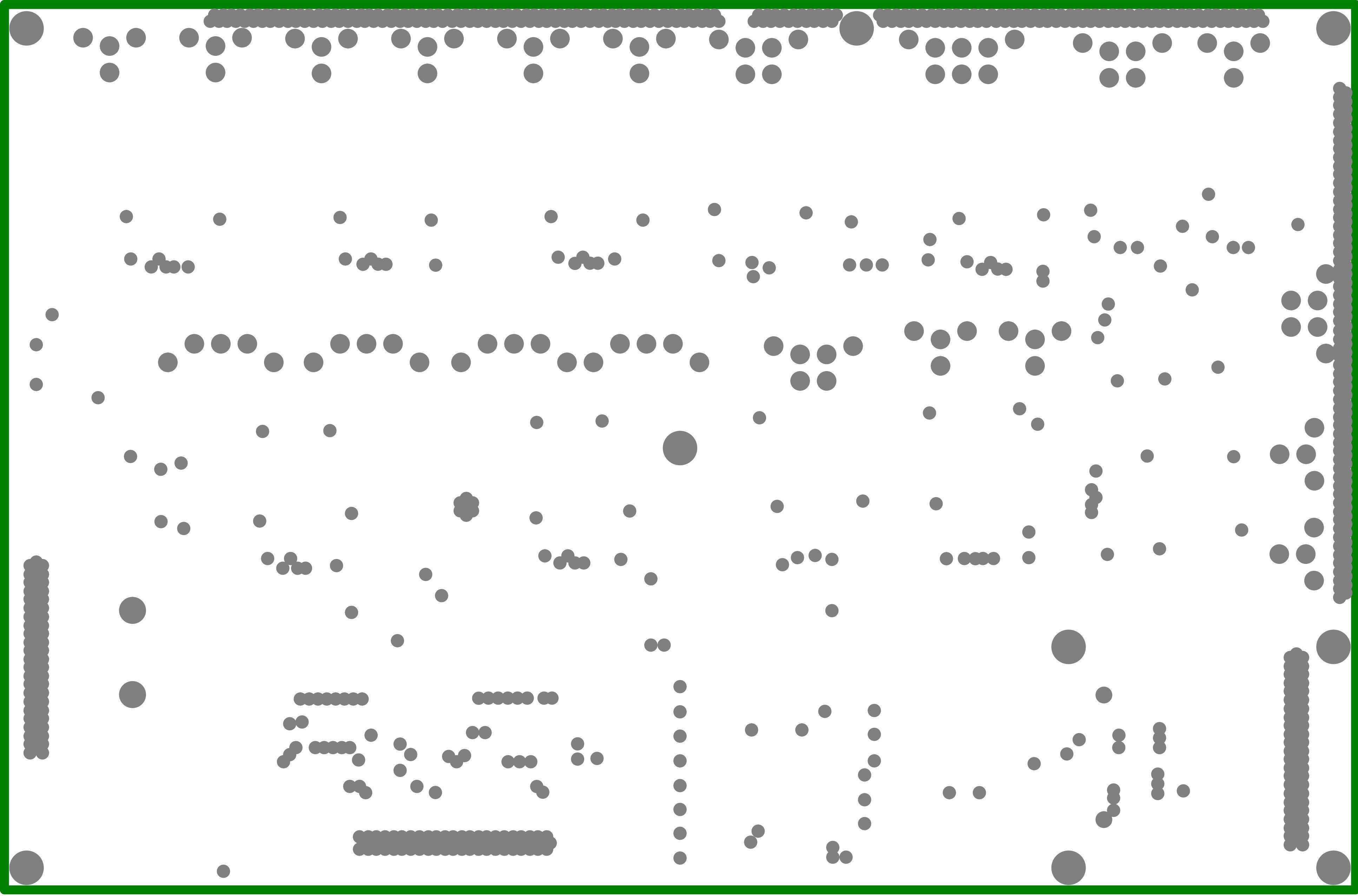
C C

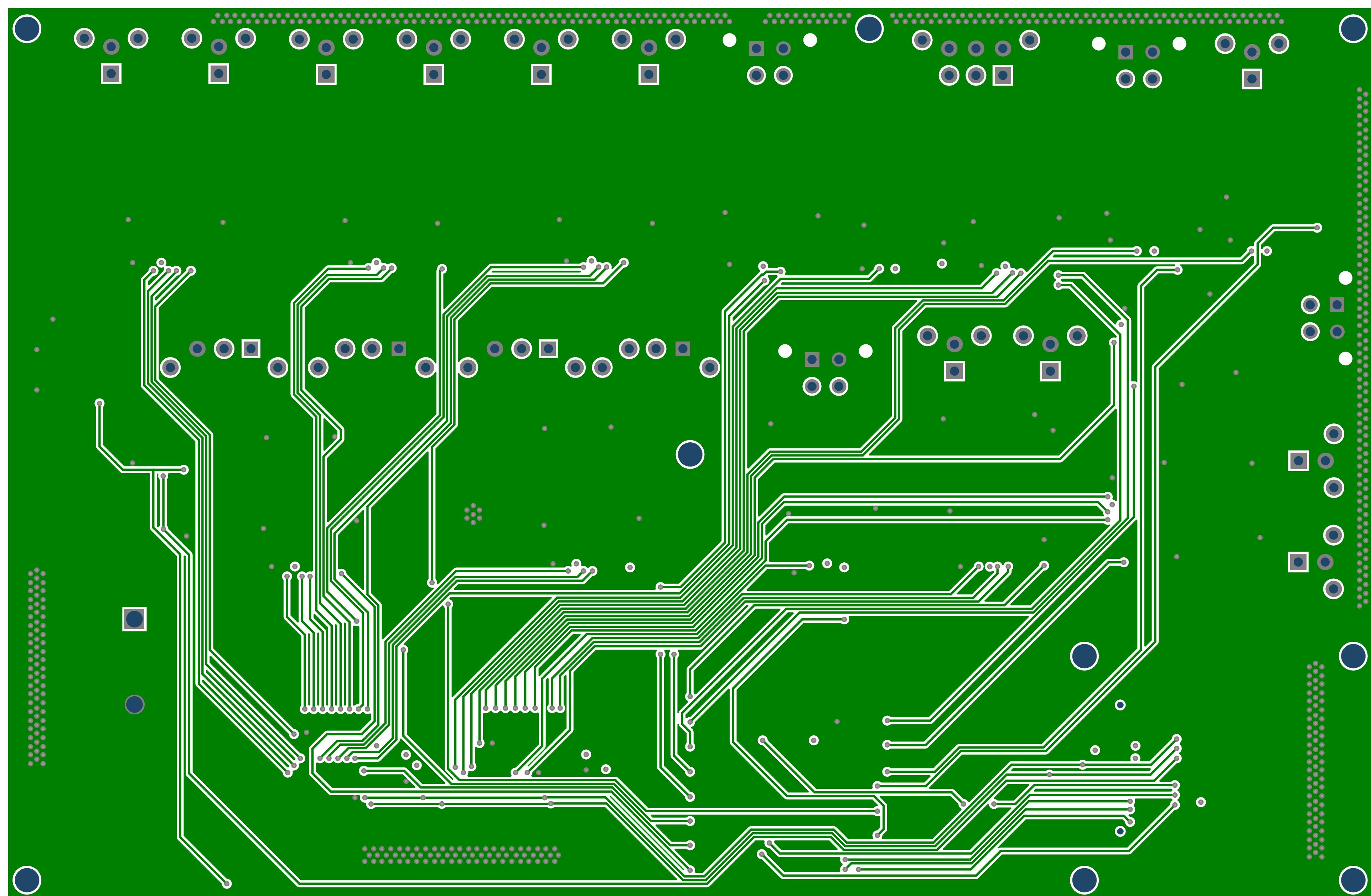


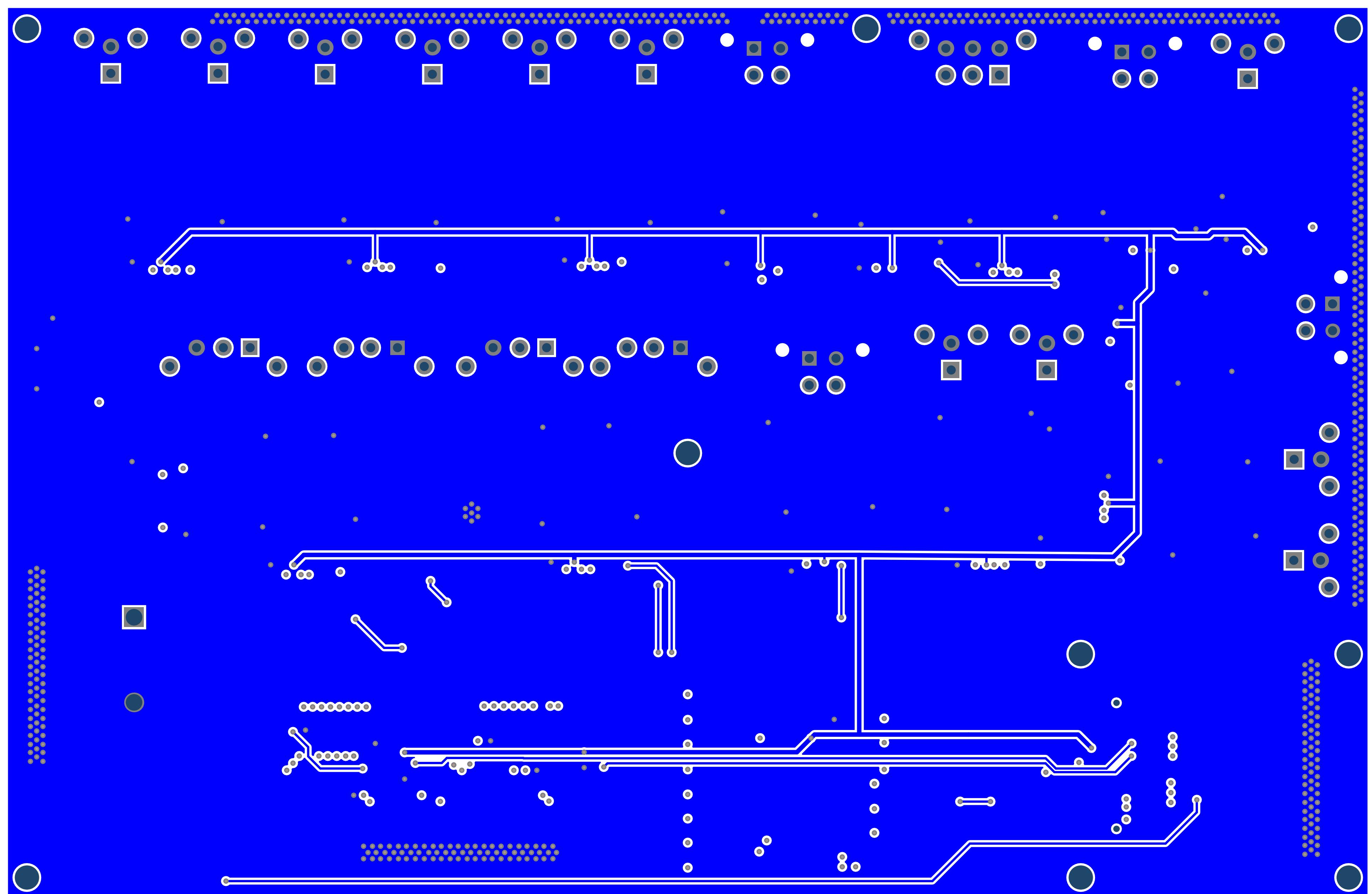
PROJECT	MSXIV_Front_Power_Distribution.PnjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	REVISION	
LAST MODIFIED	2020-02-24	SHEET * OF *

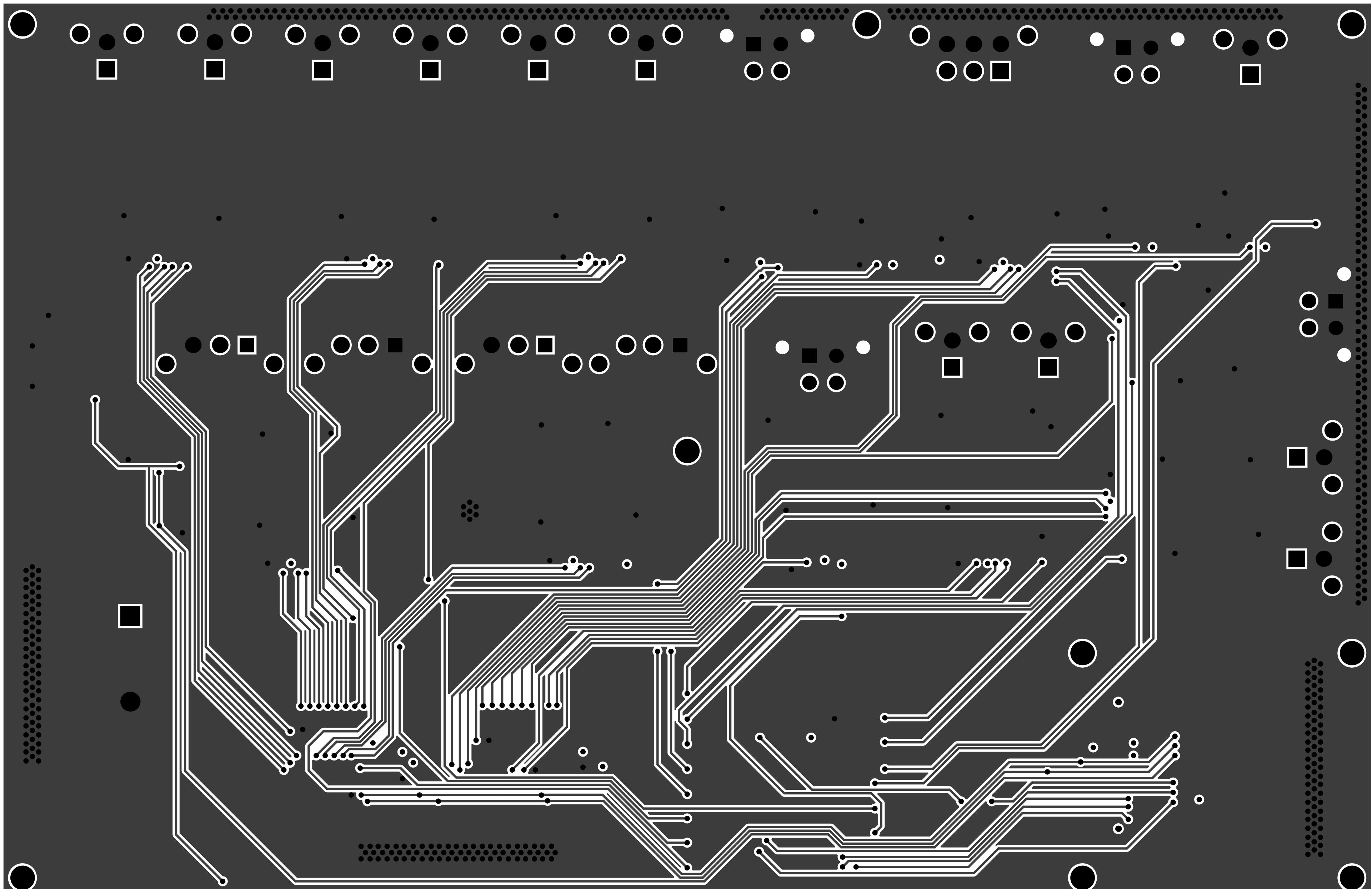


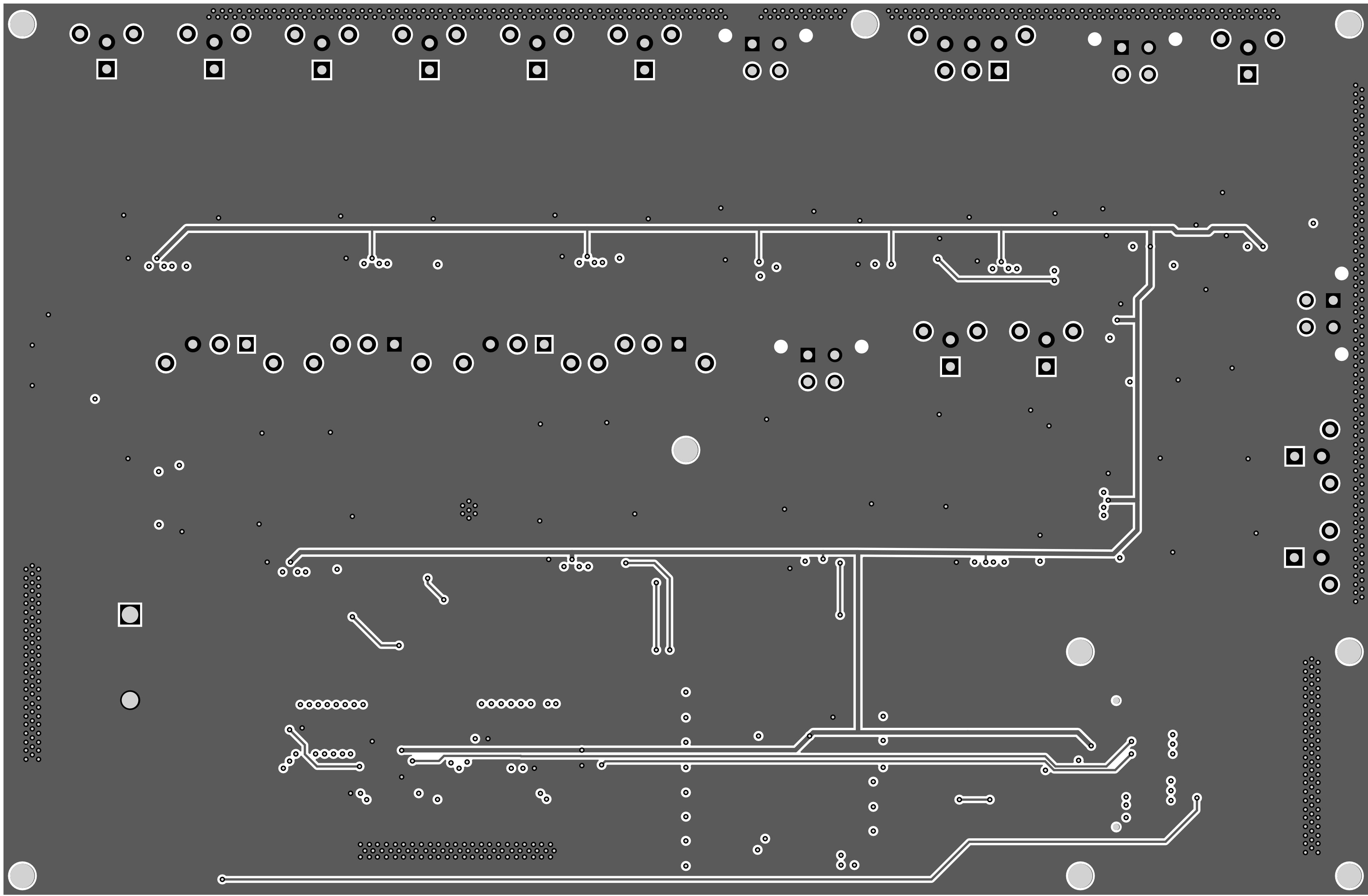


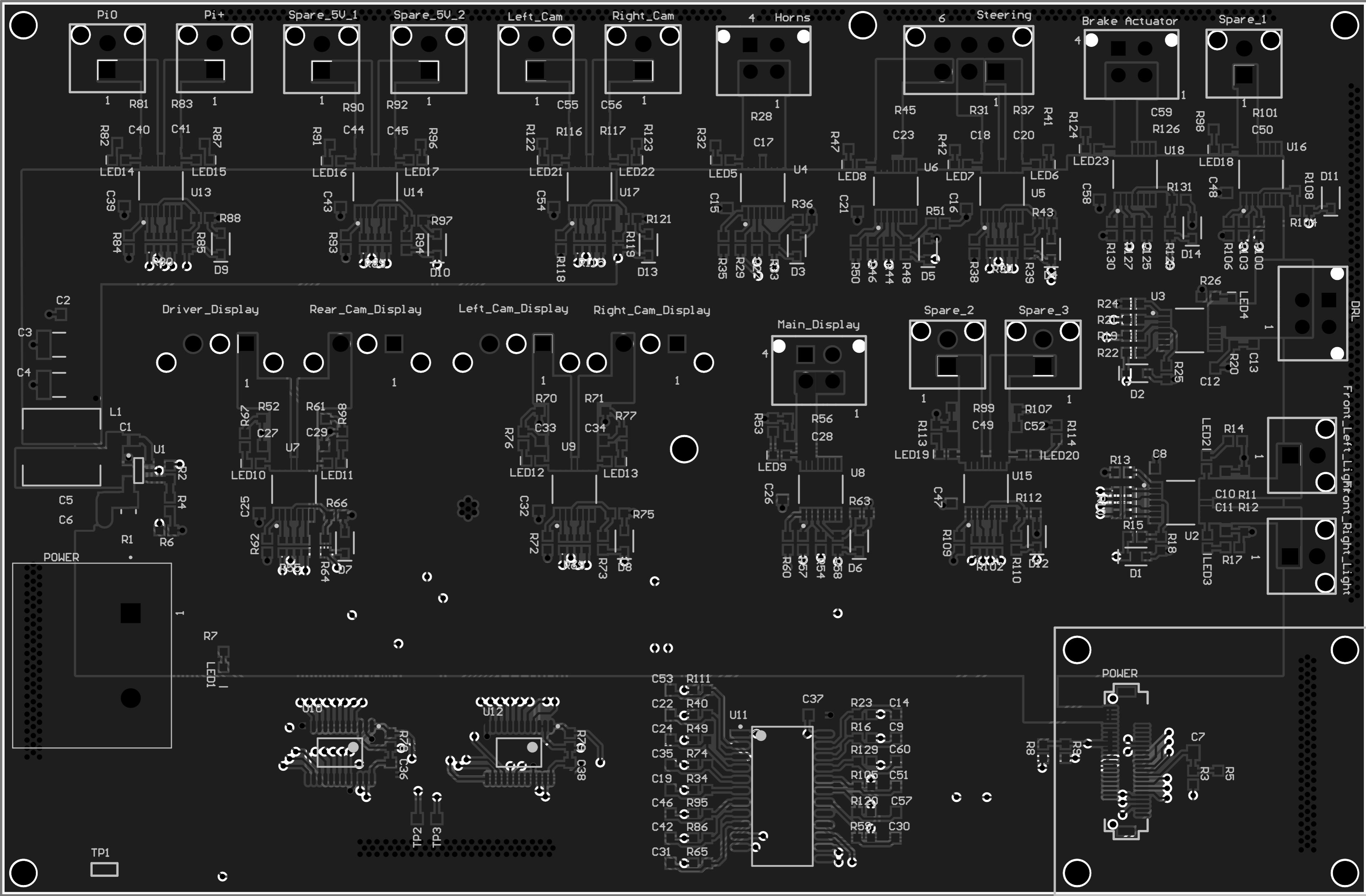












Bill of Materials

Project:	SXIV_Front_Power_Distribution.PjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2020-02-24 2:26 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	270

MIDNIGHT SUN

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CONN 4POS MICRO-FIT3mm	Brake Actuator, DRL, Horns, Main_Display	Molex	43045-0427	Digi-Key	WM10667-ND	1.77	4	\$ 7.09
CAP CER 0.1UF 50V 10% X7R 0603	C16,C21,C25,C26,C32,C36,C37,C38,C39	Kyocera AVX	06035C104KAT2A	Digi-Key	478-5052-1ND	0.09256	20	\$ 1.85
CAP CER 22UF 16V ±20% X5R 1210	C3,C4	Murata	GRM32ER61C226ME20L	Digi-Key	490-1881-1ND	2.58	2	\$ 5.16
CAP CER 22UF 35V X5R 0805	C5	TDK	C2012X5R1V226M125AC	Digi-Key	445-14428-1-ND	1.51	1	\$ 1.51
CAP CER 0.1UF 100V 10% X7R 0805	C7	Murata	GCM21BR72A10KA37L	Digi-Key	490-4789-1-ND	0.42314	1	\$ 0.42
CAP CER 220PF 50V C0G/NP0 0603	C12,C22,C24,C30,C31,C35,C42,C46,C51,C52	KEMET	C0603C221J5GACALTO	Digi-Key	399-6868-1-ND	0.11636	14	\$ 1.63
CAP CER 10nF 50V 5% X7R 0603	C27,C28,C29,C33,C34,C40,C41,C44,C45	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.2962	22	\$ 6.52
DIODE ZENER 3.3V 200MW SOD323	D3,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13	Vishay	BZ3848C3V3-E3-08	Digi-Key	ZX3848C3V3-E3-08GICLT	0.26314	14	\$ 3.68
CONN 3POS MICROFIT	/,Left_Cam_Display, Rear_Cam_Display,Rt_Cam_Display	Molex	43650-0315	Digi-Key	WM1918-ND	1.36	4	\$ 5.45
CONN 2POS MICRO-FIT3mm	/,Left_Cam_Pl0,Pt+,Right_Cam_Spare_1,Spa	Molex	0430450227	Digi-Key	WM10657-ND	0.97851	11	\$ 10.76
IND 3.3uH 5.2A 20MOHM SMD	L1	TDK	VLP8040T-3R3N	Digi-Key	445-6581-1-ND	1		
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	1500600VST5000	Digi-Key	732-4980-1-ND	0.18512	1	\$ 0.19
LED YELLOW CLEAR 2V 0603	LED11,LED12,LED13,LED14,LED15,LED16	Wurth Electronics	1500600VST75000	Digi-Key	732-4981-1-ND	0.18512	22	\$ 4.07
CONN BARRIER STRIP 2CIRCO.3/5"	P2	BUCHANAN-TE CONNECTIVITY	6PCV-02-008	Digi-Key	A98481-ND	2.16	1	\$ 2.16
CONN 50POS Bergstak Plug 0.02"	POWER	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.9	1	\$ 1.90
RES 0.003 OHM 1% 1/2W 1206	R1	Panasonic	ERJMP2KF6M0U	Digi-Key	P19333CTND	1		
RES 54.9KOHM 1% 1/10W 0603	R2	Panasonic	ERJ-3EKF5492V	Digi-Key	P54.9KHCTRND	0.13223	1	\$ 0.13
RES 100K OHM 0.5% 1/8W 0603	R3	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCNTND	0.13223	1	\$ 0.13
RES 10K OHM 1% 1/10W 0603	R47,R53,R67,R68,R76,R77,R82,R87,R91	Yageo Phycmp	RC0603FR-0710KL	Digi-Key	311-100KHRCNTND	0.03041	25	\$ 0.76
RES 4.7K OHM 1% 1/10W 0603	R57,R58,R59,R64,R65,R73,R74,R78,R79	Yageo Phycmp	RC0603FR-074K0L	Digi-Key	311-4.70KHRCNTND	0.03041	45	\$ 1.37
RES ARRAY 4 RES 4.7K OHM1206	R10,R30,R55,R69,R80,R89,R102,R15	Panasonic	EXB-38V4T2JV	Digi-Key	Y9472CTND	0.13223	8	\$ 1.06
RES 47K OHM 1% 1/10W 0603	R52,R56,R61,R70,R71,R81,R83,R90,R92	Panasonic	ERJ3EKF4702V	Digi-Key	P47.0KHCTRND	0.07537	22	\$ 1.66
RES SMD 47 OHM 1% 1/10W 0603	R38,R50,R60,R62,R72,R84,R93,R106,R17	Yageo	AC0603FR-0747R	Digi-Key	311-47LDCNTND	0.03702	14	\$ 0.52
RES 1.6K OHM 1% 1/10W 0603	R18,R43,R66,R75,R88,R97,R112,R121	Yageo	RC0603FR-0711KL	Digi-Key	311-1.60KHRCNTND	0.13223	8	\$ 1.06
RES 1.21K OHM 1% 1/10W 0603	R25,R36,R51,R63,R108,R131	Yageo	RC0603FR-071K2L	Digi-Key	311-1.21KHRCNTND	0.13223	6	\$ 0.79
CONN 6POS MICRO-FIT3mm	Steering	Molex	0430450627	Digi-Key	WM10673-ND	2.09	1	\$ 2.09
TestPoint0603SMD	TP1	CGS-TE CONNECTIVITY	RCU-0-C	Digi-Key	A106145CTND	0.31735	1	\$ 0.32
REG BUCK 4.5V TO 17V,5A,SYNCHRONOUS	U1	Texas Instruments	TPS5656201DDCT	Digi-Key	296-47501-1ND	2.04	1	\$ 2.04
LOAD SWITCH BT57200-2EPAVG-TSDSO-14	U2,U5,U7,U9,U13,U14,U15,U17	Infineon	BT572002PAUXUMA1	Digi-Key	S72002EPAUXUMA1CT-N	1.72	8	\$ 13.75
LOAD SWITCH BT570401EPAPG-TSDSO-14	U3,U6,U8,U16,U18	Infineon	BT570401EPAXUMA1	Digi-Key	S70401EPAXUMA1CT-N	1.76	5	\$ 8.79
IC LOAD SWITCH BT570081EPPXUMA1	U4	Infineon	BT570081EPPXUMA1	Digi-Key	S70081EPPXUMA1CT-N	2.76	1	\$ 2.76
16-BIT-T2C-BUS AND SMBUS LOW POW	U10,U12	NXP USA	PCA9539PW/Q90Q	Digi-Key	568-13622-1-ND	3.16	2	\$ 6.32
IC MUX/DEMUX 1X16 24SSOP	U11	Texas Instruments	CD74HC4067M96	Digi-Key	296-29408-1-ND	0.99173	1	\$ 0.99
					Total:			\$ 96.93

Design Rules Verification Report

Filename : D:\Josh9\Documents\Midnight Sun\hardware\MSXIV_FrontPowerDistribution\Fr

Warnings 0
Rule Violations 372

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	9
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All), (All)	218
Silk To Solder Mask (Clearance=0.254mm) (IsPad), (All)	137
Silk to Silk (Clearance=0.254mm) (All), (All)	8
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	372

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(120.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(120.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(150.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(150.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(150.5mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(76.5mm,50mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(96.5mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All), (All)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad POWER-(124.5mm,22.05mm) on Multi-Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad POWER-(124.5mm,7.95mm) on Multi-Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R10-1(124.9mm,45.28mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R10-2(124.9mm,44.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R102-1(109.12mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R102-2(110mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R102-3(110.8mm,38.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R102-5(111.68mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R102-6(110.8mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R102-7(110mm,39.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R10-3(124.9mm,43.6mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R10-5(126.3mm,42.72mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R10-6(126.3mm,43.6mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R10-7(126.3mm,44.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R115-1(64.62mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R115-2(65.5mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R115-3(66.3mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R115-5(67.18mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R115-6(66.3mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R115-7(65.5mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R30-1(110.82mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R30-2(111.7mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R30-3(112.5mm,71.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R30-5(113.38mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R30-6(112.5mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R30-7(111.7mm,73.3mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R55-1(31.52mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R55-2(32.4mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R55-3(33.2mm,38.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R55-5(34.08mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R55-6(33.2mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R55-7(32.4mm,39.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R69-1(62.92mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R69-2(63.8mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R69-3(64.6mm,38.7mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R69-5(65.48mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R69-6(64.6mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R69-7(63.8mm,40.1mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R80-1(16.62mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R80-2(17.5mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R80-3(18.3mm,72.5mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R80-5(19.18mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R80-6(18.3mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R80-7(17.5mm,73.9mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R89-1(40.62mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R89-2(41.5mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R89-3(42.3mm,72.4mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R89-5(43.18mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad R89-6(42.3mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.107mm < 0.254mm) Between Pad R89-7(41.5mm,73.8mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U13-1(15.95mm,76.65mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U13-10(18.55mm,82.35mm) on Component Side And Pac

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-10(64.85mm,48.35mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-11(64.2mm,48.35mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-12(63.55mm,48.35mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-13(62.9mm,48.35mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-2(62.9mm,42.65mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-3(63.55mm,42.65mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-4(64.2mm,42.65mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-5(64.85mm,42.65mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-6(65.5mm,42.65mm) on Component Side And Pac
Minimum Solder Mask Sliver Constraint: (0.2mm < 0.254mm) Between Pad U9-8(66.15mm,48.35mm) on Component Side And Pac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (109.062mm,38.038mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (110.762mm,71.438mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.254mm) Between Arc (124.438mm,45.338mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (16.562mm,72.038mm) on Top Overlay And Pad R80-1(16.62mm,72.5mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (31.462mm,37.938mm) on Top Overlay And Pad R55-1(31.52mm,38.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (40.562mm,71.938mm) on Top Overlay And Pad R89-1(40.62mm,72.4mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (62.862mm,38.238mm) on Top Overlay And Pad R69-1(62.92mm,38.7mm)
Silk To Solder Mask Clearance Constraint: (0.012mm < 0.254mm) Between Arc (64.562mm,71.938mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C 10-1(137.2mm,46.125mm) on Component Side And Text "C10"
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad C 17-1(87.125mm,84.5mm) on Component Side And Text "C17"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C 9-1(100.225mm,17.6mm) on Component Side And Text "C60"
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C 9-2(101.575mm,17.6mm) on Component Side And Text "C60"
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad Front_Left_Light-0(148.34mm,46.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad Front_Left_Light-0(148.34mm,46.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad Front_Left_Light-0(148.34mm,52.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad Front_Left_Light-0(148.34mm,52.3mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad Front_Right_Light-0(148.3mm,35mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad Front_Right_Light-0(148.3mm,35mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad Front_Right_Light-0(148.3mm,41mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad Front_Right_Light-0(148.3mm,41mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad L1-1(6.8mm,47.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.254mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Pad L1-2(6.8mm,52.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED10-2(27.55mm,48.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED11-2(38.05mm,48.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(24.91mm,24.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED12-2(58.85mm,48.69mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED13-2(69.35mm,48.61mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED14-2(12.45mm,82.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED15-2(23.35mm,82.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED16-2(36.55mm,82.29mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED17-2(47.15mm,82.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED18-2(135.85mm,83.59mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED19-2(105.1mm,49.44mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED20-2(115.8mm,49.36mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED21-2(60.75mm,82.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED2-2(135mm,49.3mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED22-2(71.15mm,82.41mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED23-2(121.45mm,83.64mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED3-2(135.1mm,38.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED4-2(137.8mm,66.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED5-2(80.15mm,82.39mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED6-2(117.35mm,81.91mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED7-2(106.75mm,81.89mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED8-2(94.85mm,81.89mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED9-2(86.45mm,49.317mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Left_Cam-0(56.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad Left_Cam-0(56.9mm,96.34mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad Left_Cam-0(62.9mm,96.34mm) on Multi-Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U1-1(14.275mm,48.55mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-1(82.8mm,18.081mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-10(82.8mm,6.651mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-11(82.8mm,5.381mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-12(82.8mm,4.111mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-13(92.2mm,4.111mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-14(92.2mm,5.381mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-15(92.2mm,6.651mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-16(92.2mm,7.921mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-17(92.2mm,9.191mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-18(92.2mm,10.461mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-19(92.2mm,11.731mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-2(82.8mm,16.811mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-20(92.2mm,13.001mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-21(92.2mm,14.271mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-22(92.2mm,15.541mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-23(92.2mm,16.811mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U11-24(92.2mm,18.081mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-3(82.8mm,15.541mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-4(82.8mm,14.271mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-5(82.8mm,13.001mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-6(82.8mm,11.731mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-7(82.8mm,10.461mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-8(82.8mm,9.191mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U11-9(82.8mm,7.921mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-2(14.275mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-3(14.275mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U1-3(14.275mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U1-4(16.525mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-4(16.525mm,46.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-5(16.525mm,47.6mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad U1-6(16.525mm,48.55mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.254mm) Between Pad U1-6(16.525mm,48.55mm) on Component Side And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.254mm < 0.254mm) Between Text "1" (132.3mm,89.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.253mm < 0.254mm) Between Text "1" (132.3mm,89.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "1" (139.1mm,88.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (35.8mm,88.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (71.9mm,88.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "Front_Left_Light" (150.411mm,57mm) on Top Overlay And Tex
Silk To Silk Clearance Constraint: (0.144mm < 0.254mm) Between Text "POWER" (4.9mm,37.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.231mm < 0.254mm) Between Text "Right_Cam" (68.6mm,98.2mm) on Top Overlay And Track