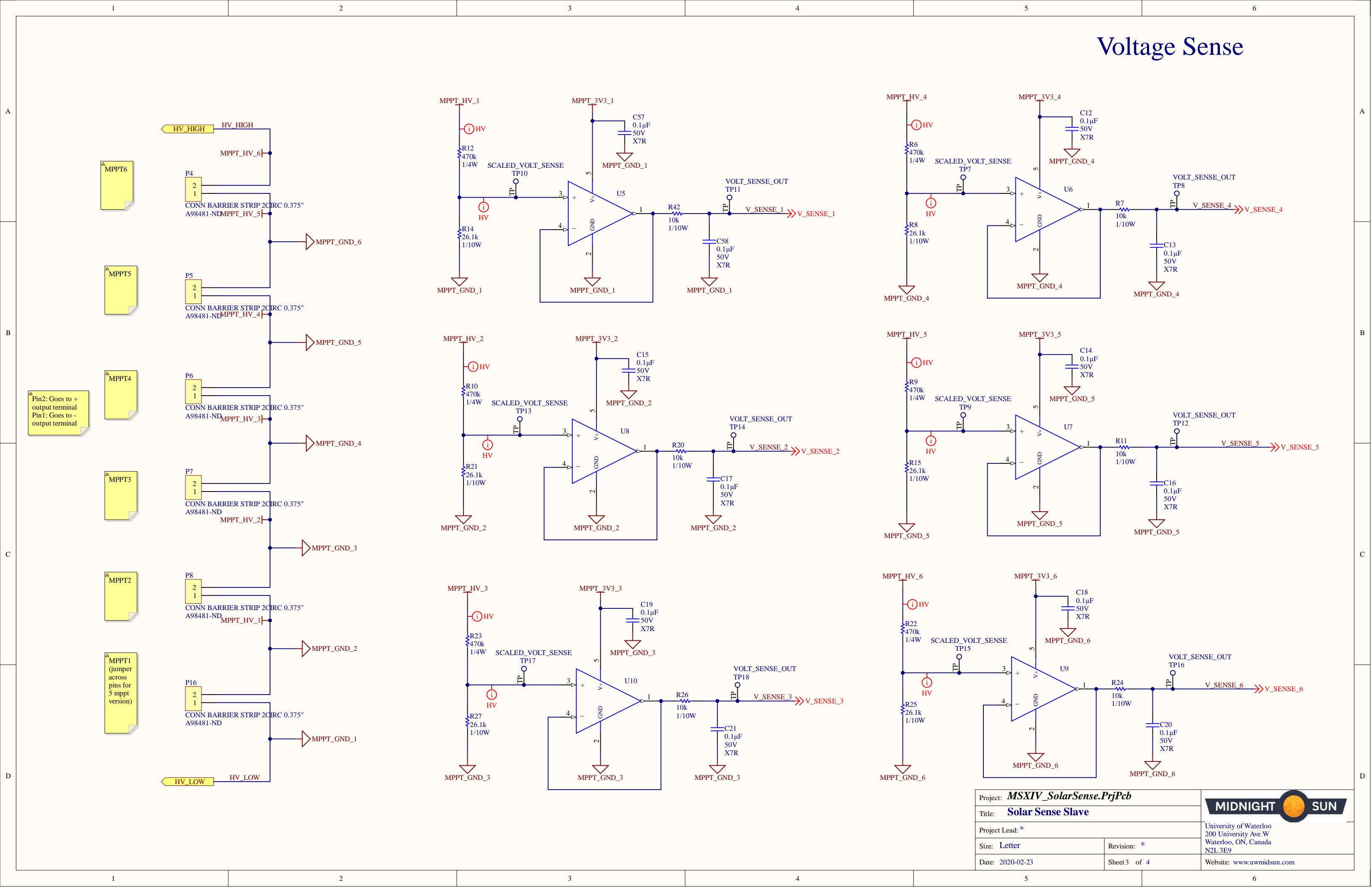
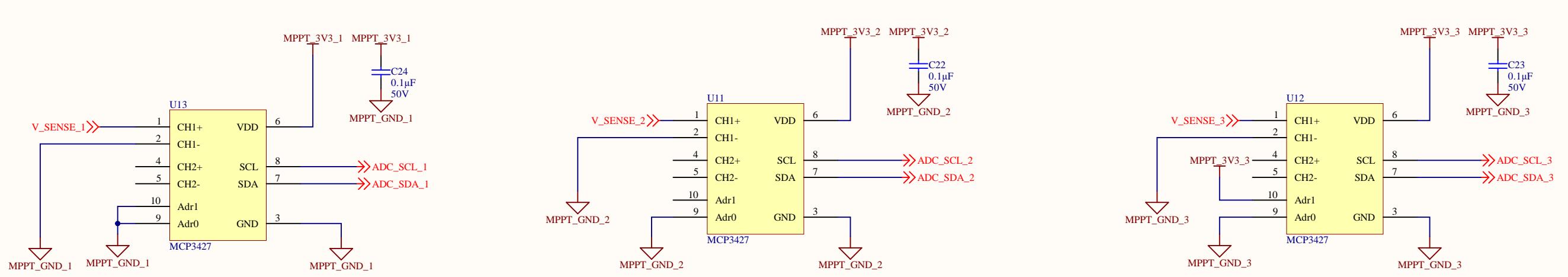


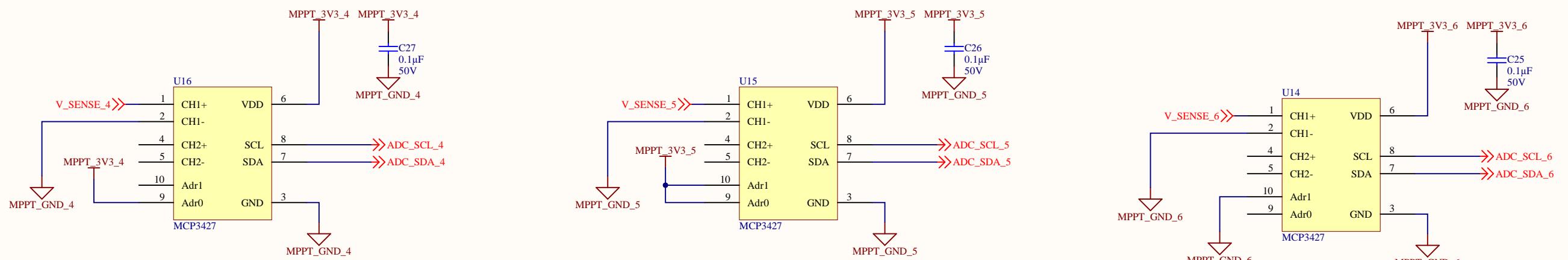
# Voltage Sense





I <sup>2</sup> C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float

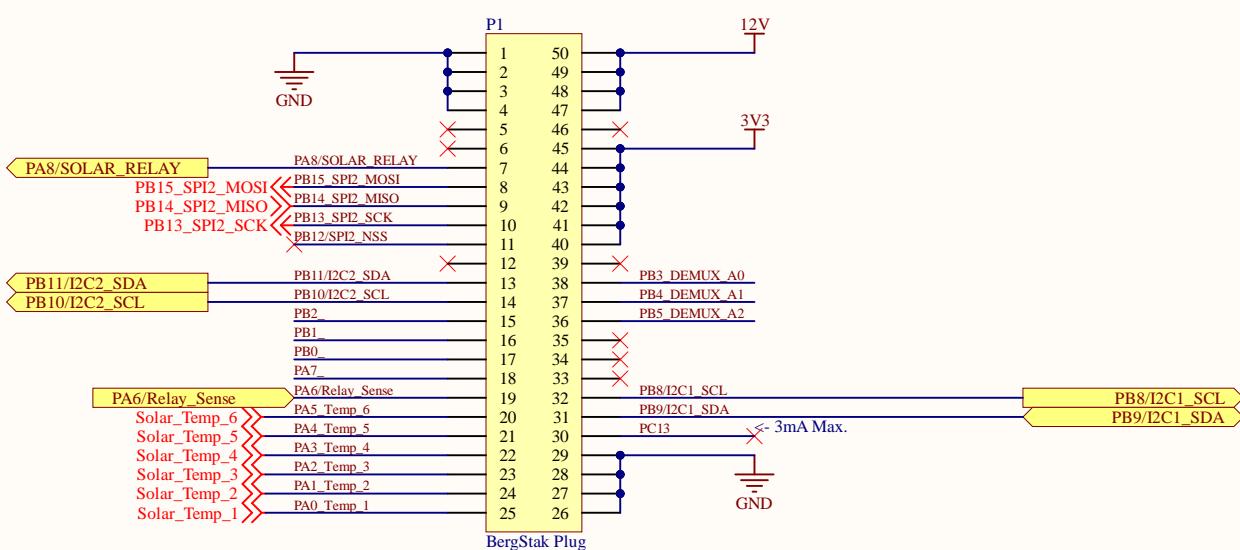
## ADCs



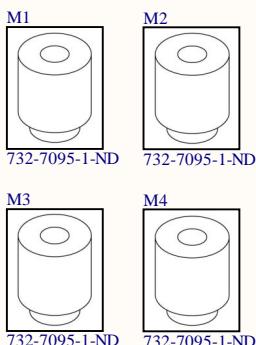
Make combination of pulled high, low and floating (for address pins)

PROJECT	MSXIV_SolarSense.PrjPcb	MIDNIGHT SUN
DOCUMENT	*	
PART NUMBER	VARIANT [No Variations]	
DRAWN BY	Aashmika Mali	
REVISION	1.0	
LAST MODIFIED	2020-02-23	SHEET * OF *

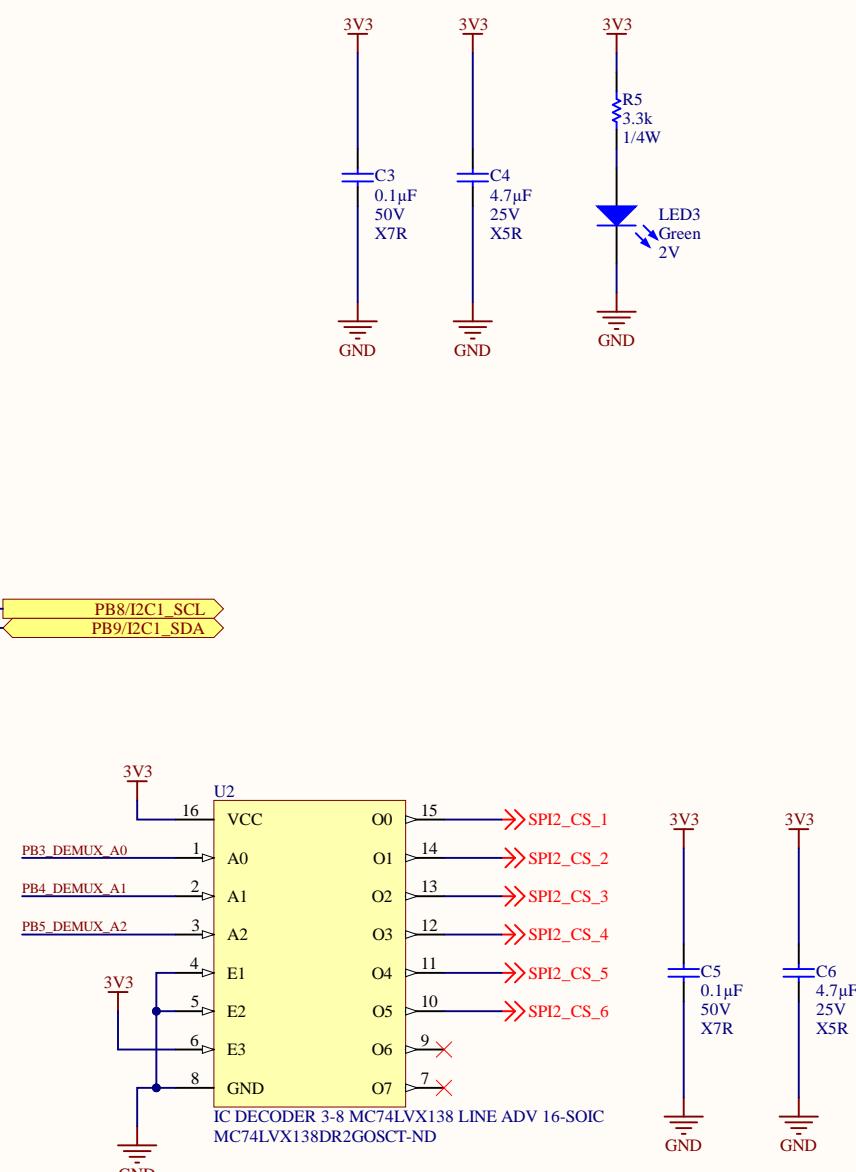
# Controller Board



## Standoffs



Solar Sense Rev 1.0  
MSXIV LOGO  
MSXIV\_LOGO



Project: **MSXIV\_SolarSense.PnjPcb**

Title: \*

Project Author: Aashmika Mali

Size: Letter

Revision: 1.0

Date: 2020-02-23

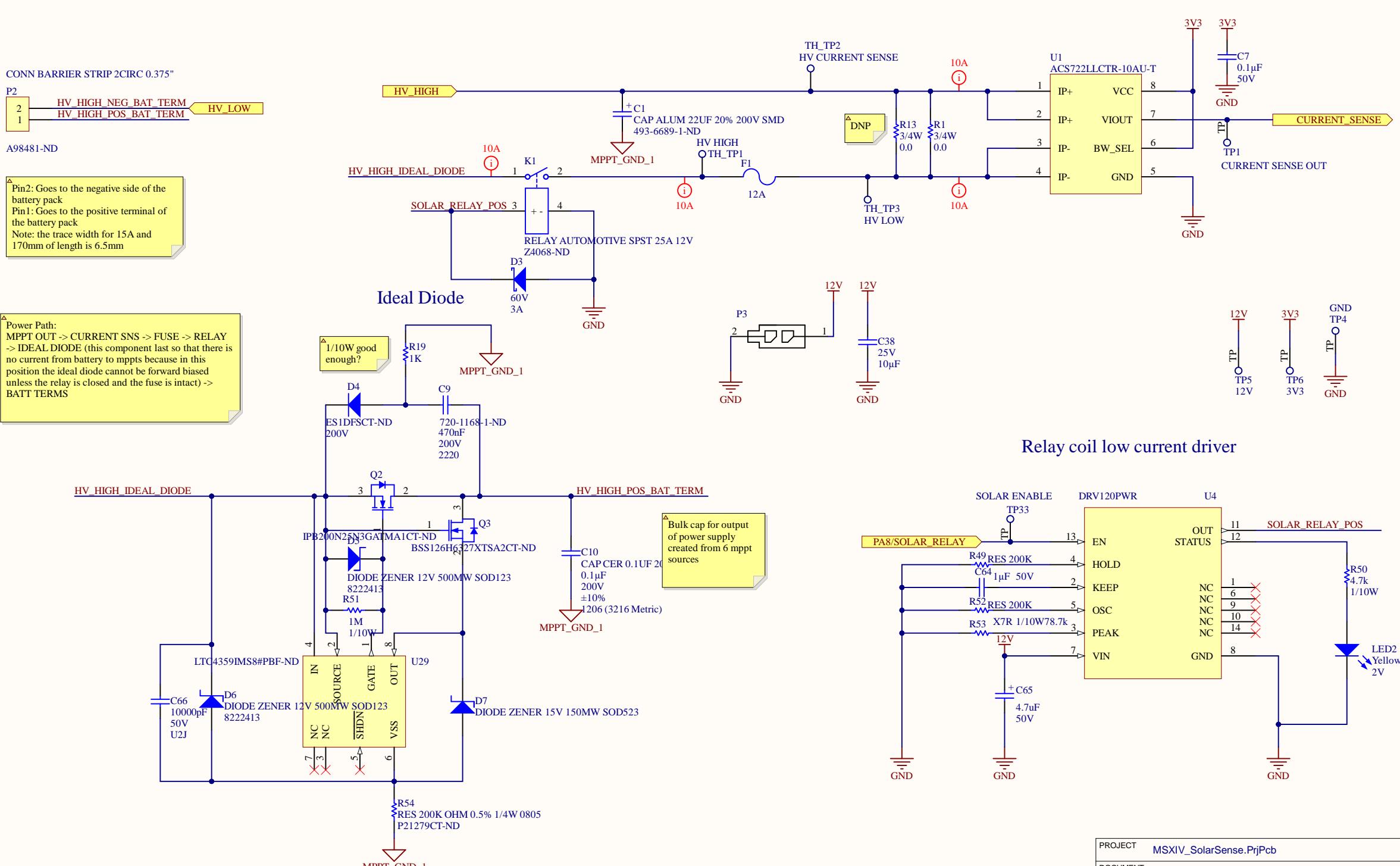
Sheet \* of \*

**MIDNIGHT SUN**

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200 University Ave W  
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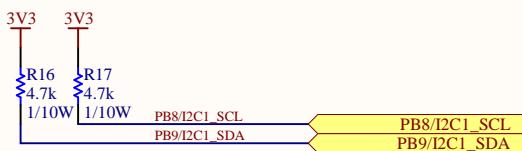
## Passthrough - Current Sense, Fuse, and Relay



PROJECT	MSXIV_SolarSense.Prbcb
DOCUMENT	*
PART NUMBER	VARIANT [No Variations]
DRAWN BY	Aashmika Mali
LAST MODIFIED	2020-02-23
SHEET *	OF *

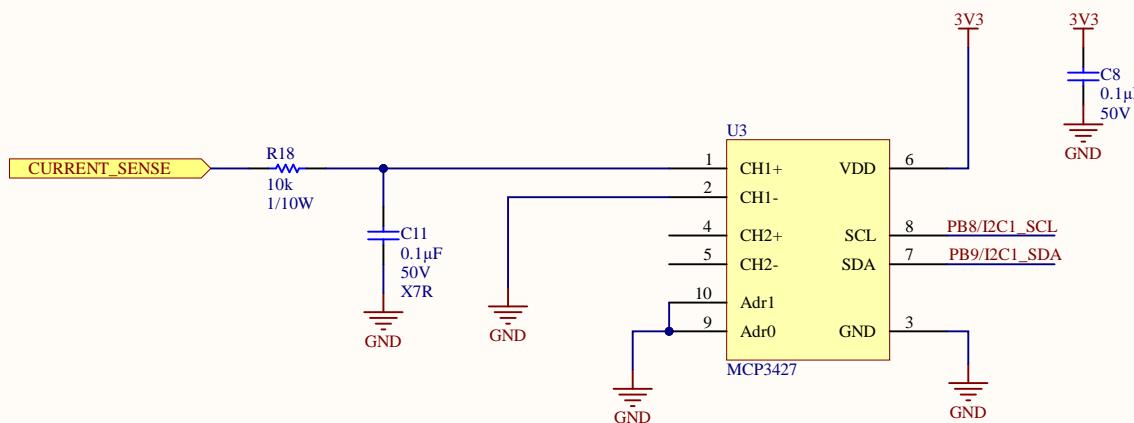
## I2C Interface (for Current Sense)

A



A

B



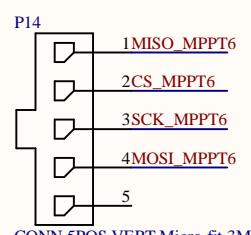
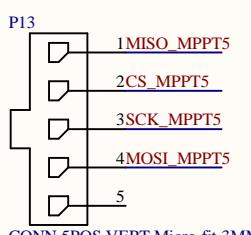
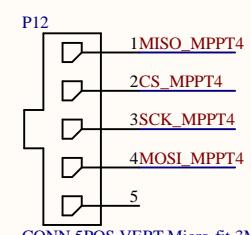
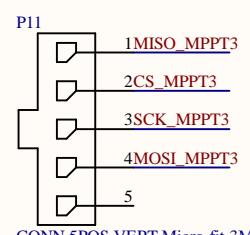
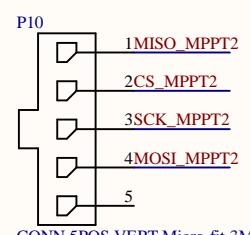
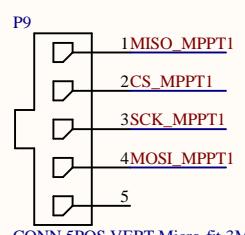
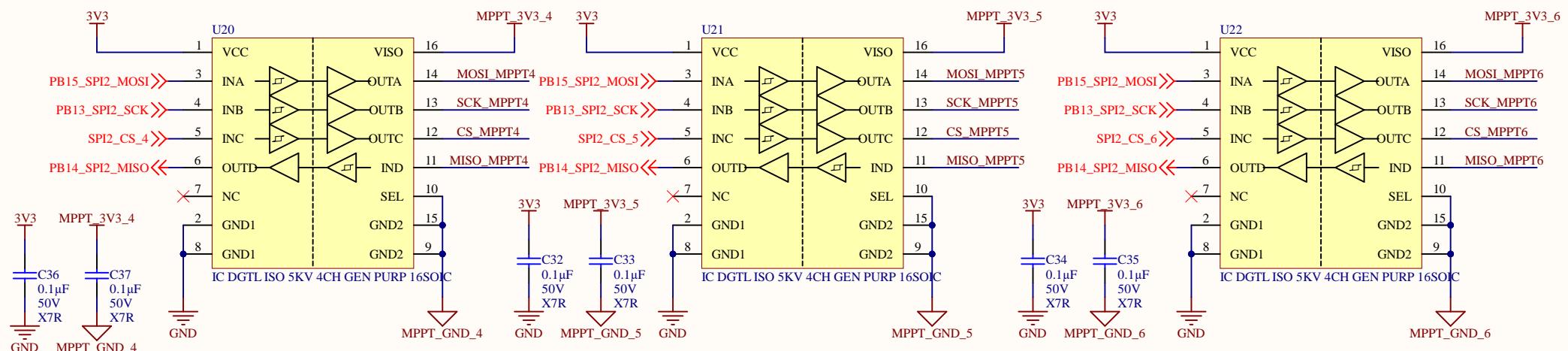
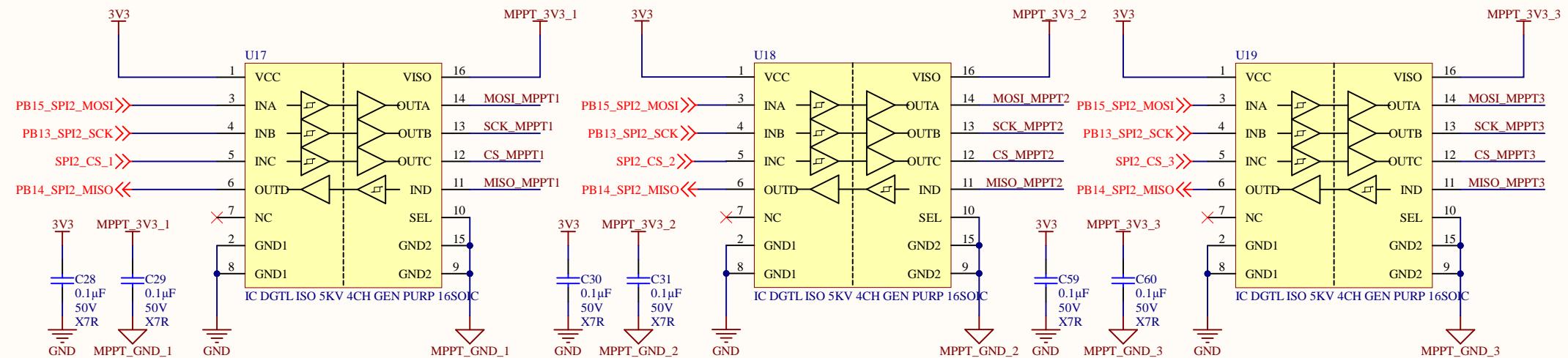
B

C

D

Project: <b><i>MSXIV_SolarSense.PjPcb</i></b>			
Title: *			
Project Author: <a href="#">Aashmika Mali</a>			
Size: Letter	Revision: 1.0		
Date: 2020-02-23	Sheet* of *	Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>	

# SPI Isolators



PROJECT	MSXIV_SolarSense.PrbPcb
DOCUMENT	*
PART NUMBER	VARIANT [No Variations]
DRAWN BY	Aashmika Mali
REVISION	1.0
LAST MODIFIED	2020-02-23
SHEET *	OF *

MIDNIGHT SUN  
Engineering 5 - 1002  
University of Waterloo  
(519) 888-4567 x32978  
hardware@uwmidsun.com

## Temperature Sense for Array Sections

A

A

B

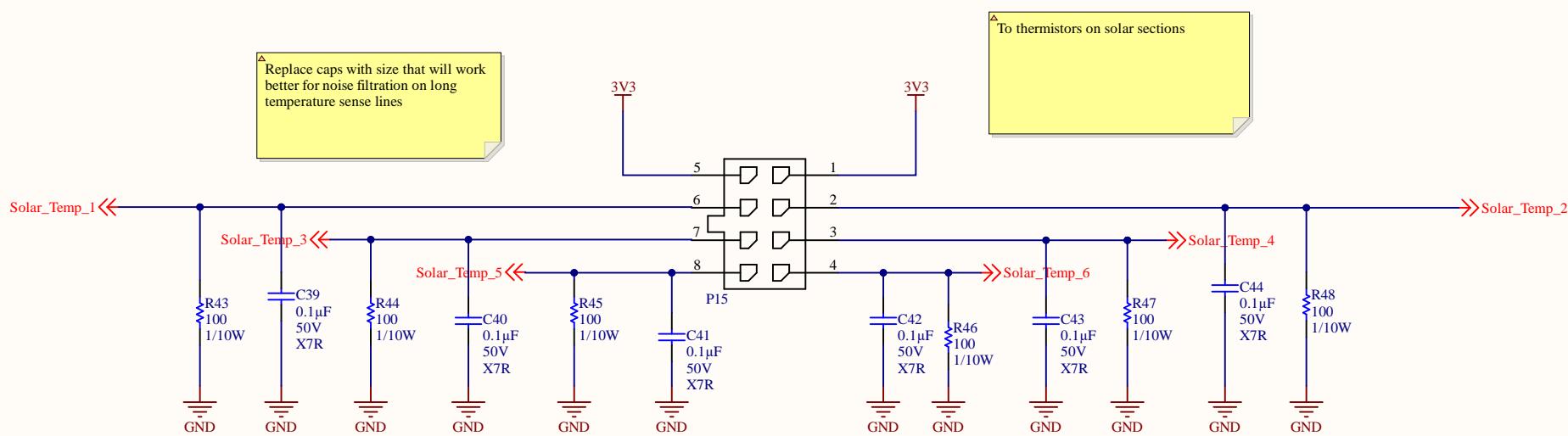
B

C

C

D

D

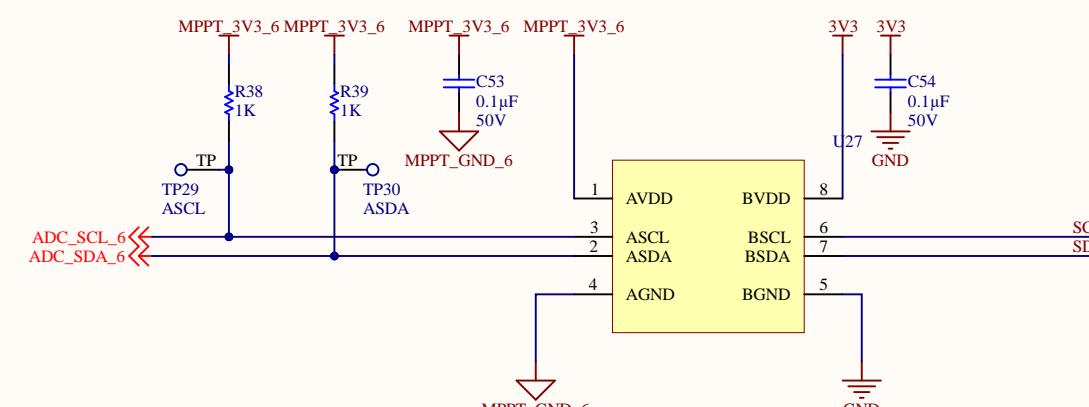
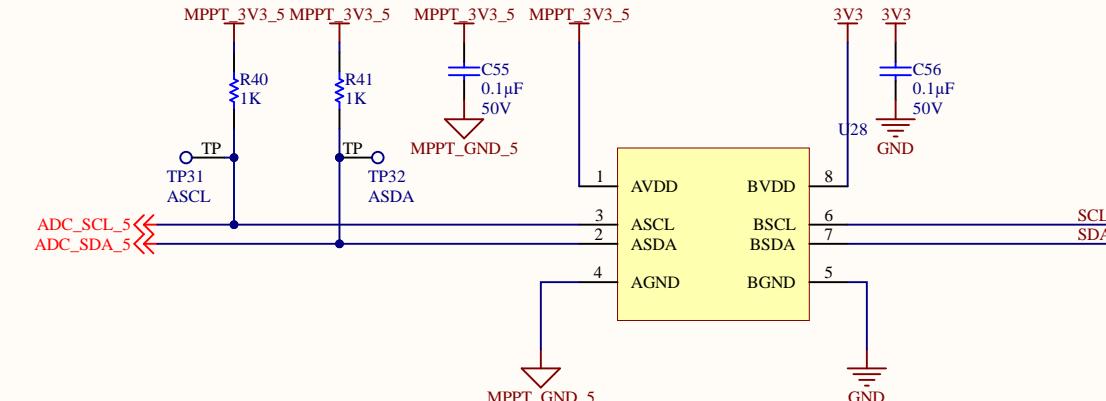
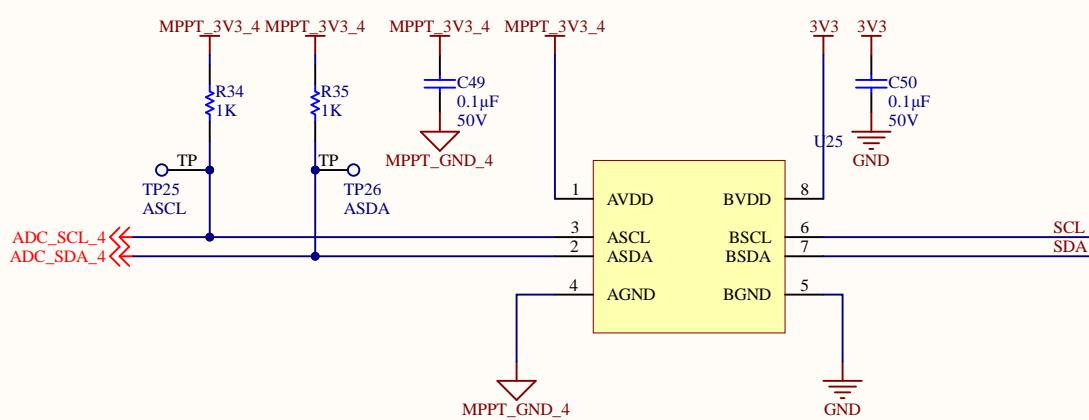
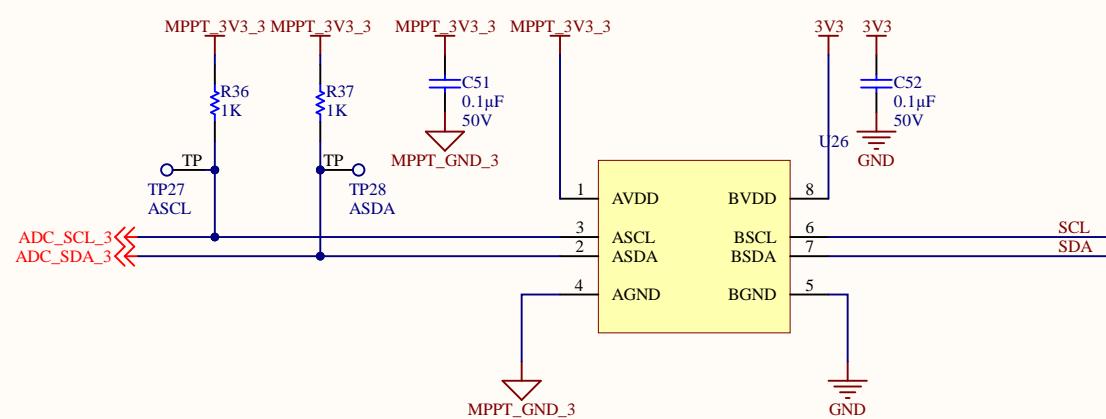
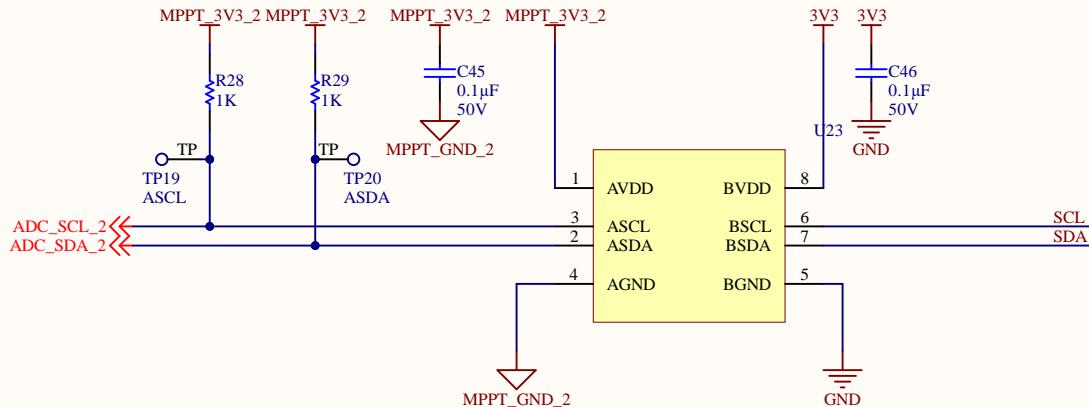
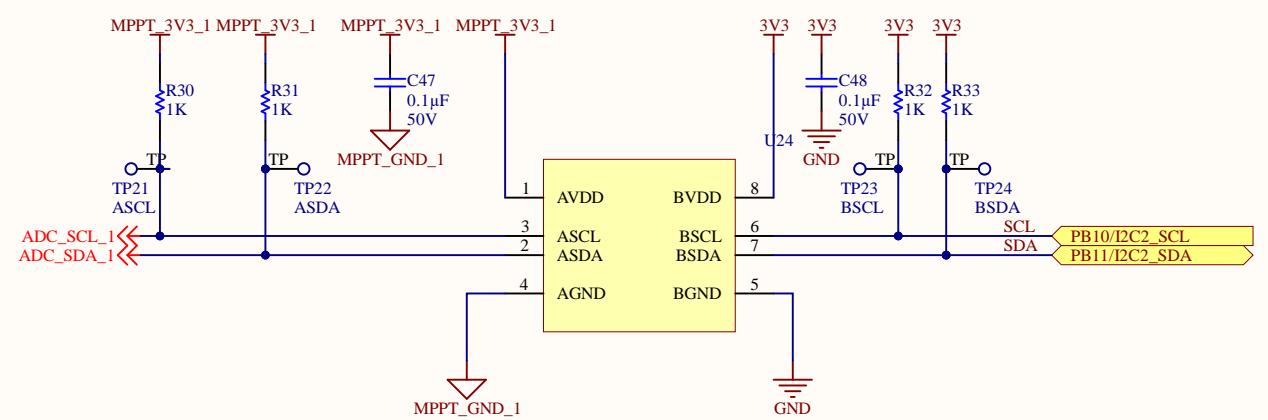


Project: <b><i>MSXIV_SolarSense.PrjPcb</i></b>	
Title: *	
Project Author: <b>Aashmika Mali</b>	
Size: Letter	Revision: 1.0
Date: 2020-02-23	Sheet * of *
Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>	



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200 University Ave W  
Waterloo, ON, Canada  
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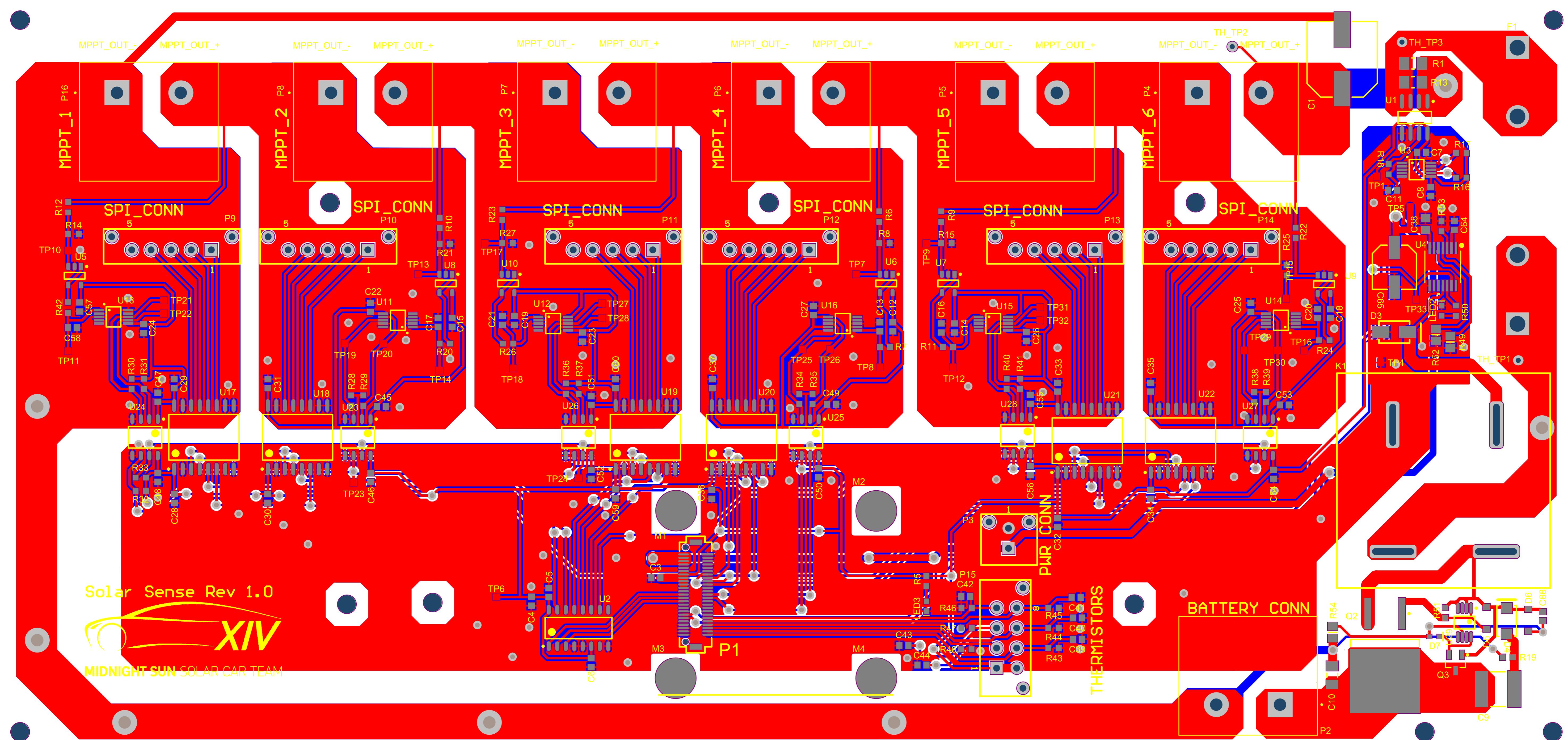
## I<sup>2</sup>C Isolators for V-Sense

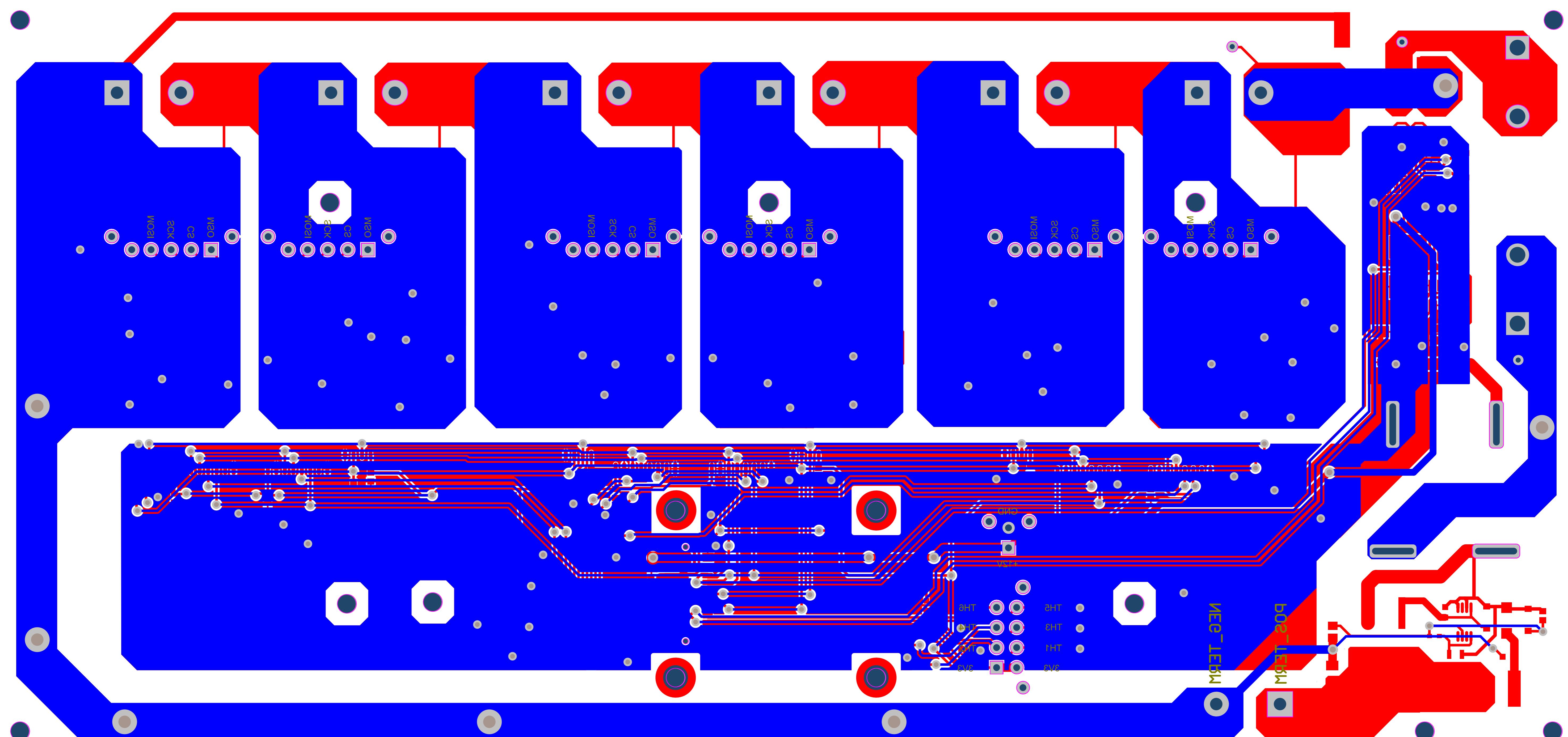


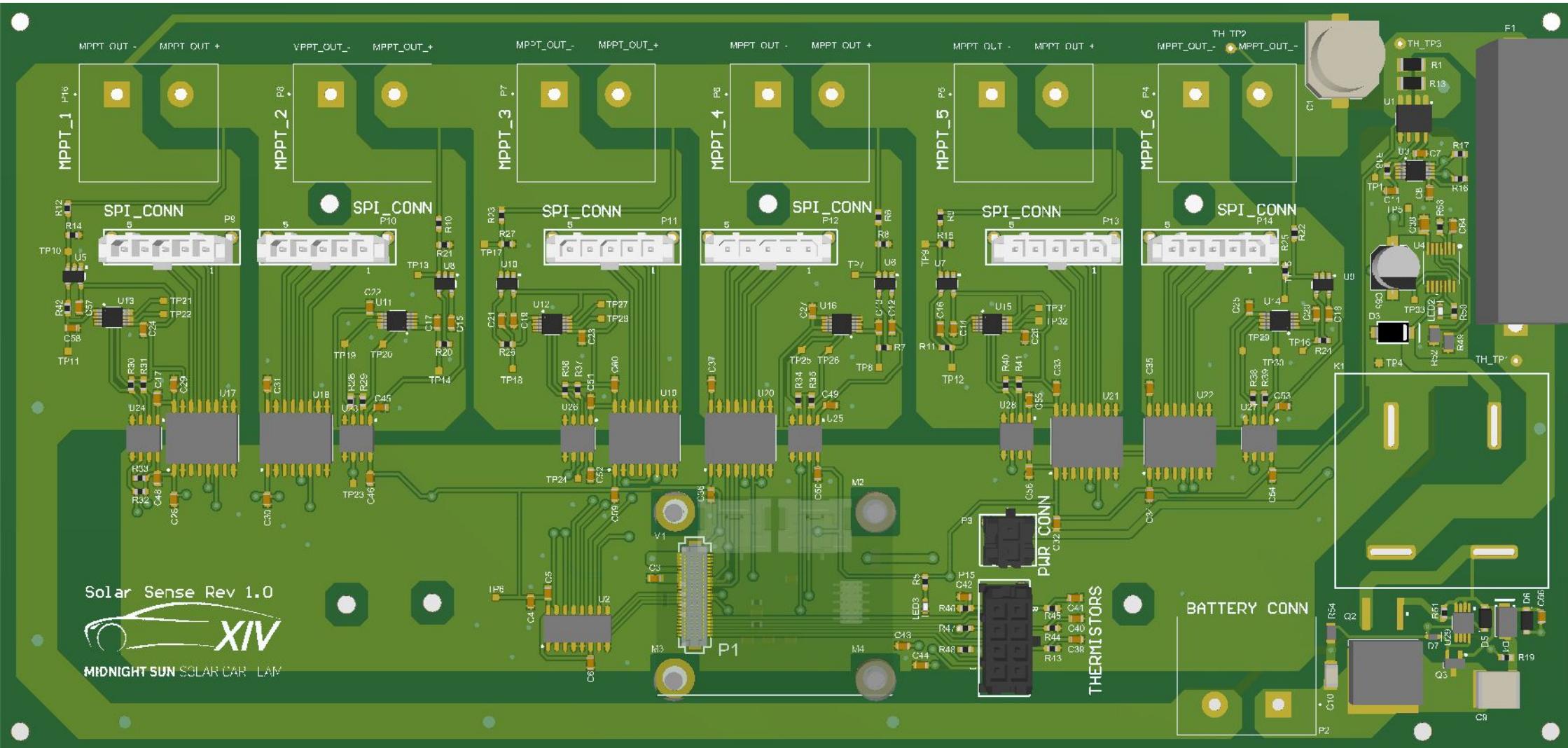
PROJECT	MSXIV_SolarSense.PrjPcb
DOCUMENT	*
PART NUMBER	VARIANT [No Variations]
DRAWN BY	Aashmika Mali
LAST MODIFIED	2020-02-23
SHEET *	OF *

MIDNIGHT SUN  
 Engineering 5 - 1002  
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 hardware@uwmidsun.com









## Electrical Rules Check Report

Class	Document	Message
Error	Voltage_Sense.SchDoc	HV_LOW contains Power Pin and Output Port objects (Pin U5-2, Port HV_LOW).
Error	Controller_Board_Interface.SchDoc	Net PA6/Relay_Sense has only one pin (Pin P1-19)
Error	Controller_Board_Interface.SchDoc	Net PA7_ has only one pin (Pin P1-18)
Error	Controller_Board_Interface.SchDoc	Net PB0_ has only one pin (Pin P1-17)
Error	Controller_Board_Interface.SchDoc	Net PB1_ has only one pin (Pin P1-16)
Error	Controller_Board_Interface.SchDoc	Net PB2_ has only one pin (Pin P1-15)
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_GND_1 at 3650mil,1830mil has been reduced to local level by presence of port at 2000mil,1300mil
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_HV_6 at 3350mil,9100mil has been reduced to local level by presence of port at 2000mil,9400mil
Warning	Controller_Board_Interface.SchDoc	Net 12V has no driving source (Pin C38-1, Pin C65-1, Pin P1-47, Pin P1-48, Pin P1-49, Pin P1-50, Pin P3-1, Pin TP5-TP, Pin U4-7)
Warning	Current_and_Relay_Sense.SchDoc	Net NetC64_2 has no driving source (Pin C64-2, Pin U4-2)
Warning	Current_and_Relay_Sense.SchDoc	Net NetD7_2 has no driving source (Pin D7-2, Pin Q3-2, Pin U29-8)
Warning	Voltage_Sense.SchDoc	Net NetR6_2 has no driving source (Pin R6-2, Pin R8-1, Pin TP7-TP, Pin U6-3)
Warning	Voltage_Sense.SchDoc	Net NetR9_2 has no driving source (Pin R9-2, Pin R15-1, Pin TP9-TP, Pin U7-3)
Warning	Voltage_Sense.SchDoc	Net NetR10_2 has no driving source (Pin R10-2, Pin R21-1, Pin TP13-TP, Pin U8-3)
Warning	Voltage_Sense.SchDoc	Net NetR12_2 has no driving source (Pin R12-2, Pin R14-1, Pin TP10-TP, Pin U5-3)
Warning	Voltage_Sense.SchDoc	Net NetR22_2 has no driving source (Pin R22-2, Pin R25-1, Pin TP15-TP, Pin U9-3)
Warning	Voltage_Sense.SchDoc	Net NetR23_2 has no driving source (Pin R23-2, Pin R27-1, Pin TP17-TP, Pin U10-3)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR49_2 has no driving source (Pin R49-2, Pin U4-4)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR52_2 has no driving source (Pin R52-2, Pin U4-5)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR53_2 has no driving source (Pin R53-2, Pin U4-3)
Warning	Controller_Board_Interface.SchDoc	Net PB3_DEMUX_A0 has no driving source (Pin P1-38, Pin U2-1)
Warning	Controller_Board_Interface.SchDoc	Net PB4_DEMUX_A1 has no driving source (Pin P1-37, Pin U2-2)
Warning	Controller_Board_Interface.SchDoc	Net PB5_DEMUX_A2 has no driving source (Pin P1-36, Pin U2-3)
Warning	Current_and_Relay_Sense.SchDoc	Nets Wire HV_HIGH has multiple names (Net Label HV_HIGH, Power Object MPPT_HV_6, Power Object MPPT_HV_6)
Warning	ADCs.SchDoc	Nets Wire HV_HIGH_NEG_BAT_TERM has multiple names (Net Label HV_HIGH_NEG_BAT_TERM, Net Label HV_LOW, Power Object MPPT_GND_1, Power Object MPPT_GND_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_2 has multiple names (Power Object MPPT_GND_2, Power Object MPPT_GND_2)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_3 has multiple names (Power Object MPPT_GND_3, Power Object MPPT_GND_3)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_4 has multiple names (Power Object MPPT_GND_4, Power Object MPPT_GND_4)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_5 has multiple names (Power Object MPPT_GND_5, Power Object MPPT_GND_5)
Warning	ADCs.SchDoc	Nets Wire MPPT_HV_1 has multiple names (Power Object MPPT_HV_1)

Class	Document	Message
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA0_Temp_1 has multiple names (Cross-Sheet Connector Solar_Temp_1, Cross-Sheet Connector Solar_Temp_1, Net Label PA0_Temp_1)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA1_Temp_2 has multiple names (Cross-Sheet Connector Solar_Temp_2, Cross-Sheet Connector Solar_Temp_2, Net Label PA1_Temp_2)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA2_Temp_3 has multiple names (Cross-Sheet Connector Solar_Temp_3, Cross-Sheet Connector Solar_Temp_3, Net Label PA2_Temp_3)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA3_Temp_4 has multiple names (Cross-Sheet Connector Solar_Temp_4, Cross-Sheet Connector Solar_Temp_4, Net Label PA3_Temp_4)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA4_Temp_5 has multiple names (Cross-Sheet Connector Solar_Temp_5, Cross-Sheet Connector Solar_Temp_5, Net Label PA4_Temp_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA5_Temp_6 has multiple names (Cross-Sheet Connector Solar_Temp_6, Cross-Sheet Connector Solar_Temp_6, Net Label PA5_Temp_6)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB10/I2C2_SCL has multiple names (Net Label PB10/I2C2_SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB11/I2C2_SDA has multiple names (Net Label PB11/I2C2_SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA)
Warning	ADCs.SchDoc	Off grid C24 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SCL_1 at 3600mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SDA_1 at 3600mil,7544.41mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB13_SPI2_SCK at 6574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB14_SPI2_MISO at 6574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB15_SPI2_MOSI at 6574.41mil,6851.811mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_2 at 9237.008mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_4 at 7437.008mil,4596.063mil
Warning	Controller_Board_Interface.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 2247.008mil,4300mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 6300mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_1 at 1350mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_2 at 6281.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_3 at 11381.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_4 at 1631.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_5 at 6531.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_6 at 11231.89mil,3400mil
Warning	Controller_Board_Interface.SchDoc	Off grid M1 at 1693.983mil,2899.713mil
Warning	Controller_Board_Interface.SchDoc	Off grid M2 at 2406.601mil,2898.306mil
Warning	Controller_Board_Interface.SchDoc	Off grid M3 at 1693.983mil,1949.714mil
Warning	Controller_Board_Interface.SchDoc	Off grid M4 at 2406.601mil,1948.306mil
Warning	SPI_Interface.SchDoc	Off grid Net Label CS_MPPT2 at 8674.41mil,6451.811mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid Net Label HV_HIGH_NEG_BAT_TERM at 998.148mil,7600mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT2 at 8624.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT3 at 12055.512mil,6250mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT2 at 8674.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT3 at 12055.512mil,6850mil
Warning	SPI_Interface.SchDoc	Off grid Net Label SCK_MPPT2 at 8674.41mil,6651.811mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid Net Label SOLAR_RELAY_POS at 11601.896mil,3900mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid NetParameter at 6495.503mil,7000mil
Warning	SPI_Interface.SchDoc	Off grid No ERC at 6774.41mil,6051.811mil
Warning	TemperatureSense.SchDoc	Off grid P15 at 4521.654mil,5096.063mil
Warning	ADCs.SchDoc	Off grid Pin C24-1 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Pin C24-2 at 3818.11mil,8374.41mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-1 at 5421.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-2 at 5421.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-3 at 5421.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-4 at 5421.654mil,4396.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-5 at 4521.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-6 at 4521.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-7 at 4521.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-8 at 4521.654mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Pin U13-1 at 1658.11mil,8044.41mil

Class	Document	Message
Warning	ADCs.SchDoc	Off grid Pin U13-2 at 1658.11mil,7894.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-3 at 3108.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-4 at 1658.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-5 at 1658.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-6 at 3108.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-7 at 3108.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-8 at 3108.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-9 at 1658.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-10 at 1658.11mil,7344.41mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-1 at 6774.41mil,7051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-2 at 6774.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-3 at 6774.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-4 at 6774.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-5 at 6774.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-6 at 6774.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-7 at 6774.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-8 at 6774.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-9 at 8574.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-10 at 8574.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-11 at 8574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-12 at 8574.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-13 at 8574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-14 at 8574.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-15 at 8574.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-16 at 8574.41mil,7051.811mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 4099.606mil,5389.764mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 5899.606mil,5389.764mil
Warning	SPI_Interface.SchDoc	Off grid Power Object 3V3 at 6174.41mil,7351.811mil
Warning	SPI_Interface.SchDoc	Off grid Power Object GND at 6774.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3218.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3818.11mil,8674.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_3V3_2 at 9074.41mil,7351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 818.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3468.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3818.11mil,8374.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_GND_2 at 8574.41mil,5351.811mil
Warning	Controller_Board_Interface.SchDoc	Off grid Solar Sense Rev 1.0 at 4505.679mil,2561.84mil
Warning	ADCs.SchDoc	Off grid U13 at 1958.11mil,8194.41mil
Warning	SPI_Interface.SchDoc	Off grid U18 at 7474.41mil,6651.811mil

## Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV\_

Warnings 0

Rule Violations 145

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=2.032mm) (Preferred=0.381mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	23
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	4
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	26
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	77
Silk to Silk (Clearance=0.254mm) (All),(All)	15
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	145

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-104.255mm,-101.365mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-104.255mm,-76.365mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-120.285mm,-30.302mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-134.255mm,-101.365mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-134.255mm,-76.365mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-170.567mm,-90.061mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-183.404mm,-90.321mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-185.935mm,-30.302mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-22.255mm,-109.382mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-232.255mm,-109.382mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-232.255mm,-3mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-3.127mm,-109.382mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-3mm,-3mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-56.515mm,-30.302mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-65.666mm,-90.293mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (6.3mm > 2.54mm) Pad K1-1(-11.582mm,-82.436mm) on Multi-Layer Actual Slot Hole Height = 6.3mm	
Hole Size Constraint: (6.3mm > 2.54mm) Pad K1-2(-26.982mm,-82.436mm) on Multi-Layer Actual Slot Hole Height = 6.3mm	
Hole Size Constraint: (6.3mm > 2.54mm) Pad K1-3(-11.532mm,-63.486mm) on Multi-Layer Actual Slot Hole Height = 6.3mm	
Hole Size Constraint: (6.3mm > 2.54mm) Pad K1-4(-27.032mm,-63.486mm) on Multi-Layer Actual Slot Hole Height = 6.3mm	
Hole Size Constraint: (3.7mm > 2.54mm) Pad M1-(-134.175mm,-76.329mm) on Multi-Layer Actual Hole Size = 3.7mm	
Hole Size Constraint: (3.7mm > 2.54mm) Pad M2-(-104.255mm,-76.365mm) on Multi-Layer Actual Hole Size = 3.7mm	
Hole Size Constraint: (3.7mm > 2.54mm) Pad M3-(-134.255mm,-101.365mm) on Multi-Layer Actual Hole Size = 3.7mm	
Hole Size Constraint: (3.7mm > 2.54mm) Pad M4-(-104.255mm,-101.365mm) on Multi-Layer Actual Hole Size = 3.7mm	

Hole To Hole Clearance (Gap=0.254mm) (All),(All)	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(-104.255mm,-101.365mm) on Multi-Layer And Pad Free-(-104.255mm,-76.365mm)	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(-104.255mm,-76.365mm) on Multi-Layer And Pad Free-(-134.255mm,-101.365mm)	
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(-134.255mm,-76.365mm) on Multi-Layer And Pad Free-(-104.255mm,-101.365mm)	

<b>Minimum Solder Mask Sliver (Gap=0.254mm) (All)(All)</b>
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(-131.255mm,-81.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(-131.255mm,-96.665mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U10-1(-158.355mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U10-2(-159.305mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-1(-17.595mm,-37.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-10(-20.195mm,-42.704mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-10(-20.195mm,-42.704mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-11(-19.545mm,-42.704mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-12(-18.895mm,-42.704mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-13(-18.245mm,-42.704mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-2(-18.245mm,-37.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-3(-18.895mm,-37.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-4(-19.545mm,-37.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-5(-20.195mm,-37.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-6(-20.845mm,-37.065mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad U4-8(-21.495mm,-42.704mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(-223.14mm,-39.834mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(-224.09mm,-39.834mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-1(-101.805mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-2(-102.755mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U7-1(-92.53mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U7-2(-93.48mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U8-1(-167.65mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U8-2(-168.6mm,-40.99mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U9-1(-36.355mm,-41.115mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U9-2(-37.305mm,-41.115mm) on Top Layer And Pac

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (-13.815mm,-94.342mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (-21.803mm,-94.536mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Arc (-5.972mm,-90.748mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-1(-34.595mm,-13.258mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-1(-34.595mm,-13.258mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.221mm < 0.254mm) Between Pad C11-2(-27.729mm,-28.41mm) on Top Layer And Text "TP1"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-2(-34.595mm,-4.458mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-2(-34.595mm,-4.458mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad C15-1(-167.65mm,-47.53mm) on Top Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (0.202mm < 0.254mm) Between Pad C15-2(-167.65mm,-48.88mm) on Top Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad C6-2(-146.85mm,-99.715mm) on Top Layer And Text "C6"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C65-1(-26.784mm,-36.987mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C65-1(-26.784mm,-36.987mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C65-2(-26.784mm,-42.887mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C65-2(-26.784mm,-42.887mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D3-1(-28.829mm,-49.637mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D3-1(-28.829mm,-49.637mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D3-2(-24.829mm,-49.637mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D3-2(-24.829mm,-49.637mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.072mm < 0.254mm) Between Pad D7-2(-20.053mm,-95.136mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED2-2(-19.743mm,-45.675mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED3-2(-96.755mm,-91.365mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.01mm < 0.254mm) Between Pad M3-(-134.255mm,-101.365mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.01mm < 0.254mm) Between Pad M4-(-104.255mm,-101.365mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P10-0(-177.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P10-0(-177.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P10-0(-195.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P10-0(-195.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(-129.455mm,-82.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P11-0(-134.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P11-0(-134.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P11-0(-152.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P11-0(-152.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P12-0(-111.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P12-0(-111.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P12-0(-129.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P12-0(-129.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(-129.455mm,-94.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(-133.055mm,-94.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P13-0(-68.48mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P13-0(-68.48mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P13-0(-86.48mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P13-0(-86.48mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P14-0(-45.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P14-0(-45.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P14-0(-63.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P14-0(-63.155mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(-133.055mm,-82.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P15-0(-82.315mm,-102.865mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad P15-0(-82.315mm,-102.865mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P15-0(-82.315mm,-87.865mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P15-0(-82.315mm,-87.865mm) on Multi-Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P3-0(-81.379mm,-78.013mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-0(-81.379mm,-78.013mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-0(-87.379mm,-78.013mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P3-0(-87.379mm,-78.013mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P9-0(-200.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P9-0(-200.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P9-0(-218.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P9-0(-218.555mm,-35.385mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.232mm < 0.254mm) Between Pad R18-1(-27.664mm,-24.536mm) on Top Layer And Text "R18"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R25-1(-42.915mm,-41.161mm) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R25-2(-42.915mm,-39.611mm) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (0.064mm < 0.254mm) Between Pad R28-2(-182.755mm,-60.64mm) on Top Layer And Text "U23"
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad R38-2(-47.755mm,-60.14mm) on Top Layer And Text "U27"
Silk To Solder Mask Clearance Constraint: (0.206mm < 0.254mm) Between Pad R45-1(-78.53mm,-90.865mm) on Top Layer And Text "R45"
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R45-2(-76.98mm,-90.865mm) on Top Layer And Text "R45"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R49-1(-18.433mm,-52.02mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R49-2(-18.433mm,-50.22mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R52-1(-20.59mm,-50.935mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R52-2(-20.59mm,-49.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.216mm < 0.254mm) Between Pad R54-1(-36.018mm,-93.618mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad R54-2(-36.018mm,-95.418mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad TP15-TP(-42.978mm,-44.616mm) on Top Layer And Text "U14"
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U13-1(-220.476mm,-46.365mm) on Top Layer And Text "C57"
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U13-2(-220.476mm,-46.865mm) on Top Layer And Text "C57"
Silk To Solder Mask Clearance Constraint: (0.203mm < 0.254mm) Between Pad U4(-16.739mm,-36.677mm) on Top Overlay And Polygon Region (26)

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (-84.579mm,-76.553mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (-89.955mm,-99.765mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-126.755mm,-33.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-150.155mm,-33.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-192.755mm,-33.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-216.155mm,-33.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-60.755mm,-33.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-84.08mm,-33.825mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "8" (-80.755mm,-90.665mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.241mm < 0.254mm) Between Text "C66" (-4.11mm,-90.505mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.244mm < 0.254mm) Between Text "D3" (-30.277mm,-47.656mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.244mm < 0.254mm) Between Text "D3" (-30.277mm,-47.656mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.197mm < 0.254mm) Between Text "PWR CONN" (-78.204mm,-85.826mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.228mm < 0.254mm) Between Text "PWR CONN" (-78.204mm,-85.826mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "PWR CONN" (-78.204mm,-85.826mm) on Top Overlay And Track