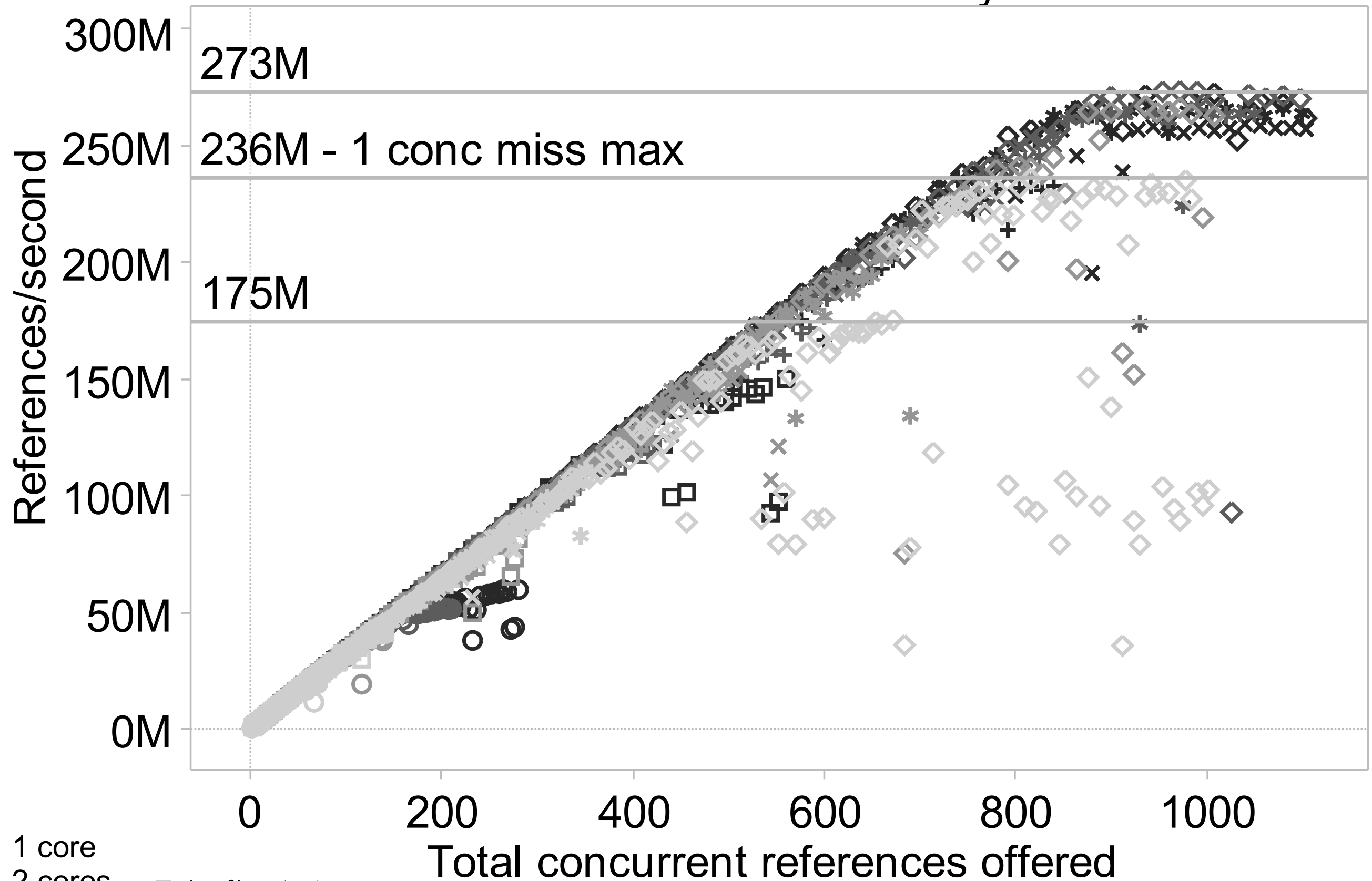


Coroutines and simulated latency



- 1 core
- 2 cores
- +
- × 4 cores
- * 5 cores
- ◇ 6 cores
- 1 ref/context
- 2 ref/context
- 3 ref/context
- 4 ref/context