Computer Architecture

Fall, 2019

Week 11

2019.11.18

組別：_____ 簽名：_____

[group3] (對抗賽)

1. Assume that individual stages of the datapath have the following latencies:

IF:300ps ID:400ps EX:350ps MEM:500ps WB:100ps

(1) What is the clock cycle time in a **pipelined** processor? What is the clock cycle time in a **single-cycle** processor?

(2) What is the total latency of a lw instruction in a **pipelined** processor? What is the total latency of a lw instruction in a **single-cycle** processor?

(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

Ans :

(1) Pipelined:500ps single-cycle:1650ps

(2) Pipelined:2500ps single-cycle:1650ps

(3) Spilt MEM stage, new clock cycle time is 400ps

[group9] (對抗賽)

2. When we use a pipelined processor，it may cause some problems，and we call them hazards。Please write down all kinds of hazards and the reason why it occurs?(if it doesn’ t happen in MIPS 5 state pipeline，explain why)

Ans.

Structural hazards : attempt to use same resource in two different ways at the same time.

Data hazards:RAW WAR WAW.Insruction depends on result of prior instruction still in the pipeline.

WAR doesn’t happen in MIPS 5 state pipeline because in 5 states reads are always in state 2 and writes are always in state 5.

WAW doesn’t happen in MIPS 5 state pipeline because in 5 states writes are always in state 5.

Control hazards:attend to make decision before the condition is evaluated.

[group5] (對抗賽)

3. 下列選項有關 Pipeline Datapath 的 stages 哪些正確？

(A) 在 Instruction fetch 階段，branch 的 PC = PC + sign-ext(IR[15-0])<<2 + 4

(B) 在 Instruction fetch 階段，jump 的 PC = PC + 4

(C) 由於 Pipeline Datapath 將 Single-cycle Datapath 切成 5 個 stages，要加上 5 個 Pipeline registers 來儲存每個 stage 完成的東西

(D) Branch instruction 只需要三個 stages，Memory access 和 Write back 為 NOP stages

(E) Pipeline R-type 和 Load instruction 的時候由於所需 stage 的數目不同，有時候會在同一個 stage 撞車，這是屬於 Data Hazard

Ans : (B) (D)

(A) PC = PC + 4

(C) 4 個 Pipeline registers

(E) Structural Hazard

[group2] (對抗賽)

4. 下列為連續的指令，在 five-stage pipeline 的情況下，那些指令會出現 RAW hazard

(1)add $s1, $s2, $s3
(2)sub $s4, $s1, $s2
(3)or $t1, $s1, $s5
(4)add $s6, $t2, $s1
(5)add $t3, $s1, $s1

Ans: (2)、(3)
以上三者會用到舊的$s1 的值

[group8] (對抗賽)

5. 下列選項之描述何者正確 ?(複選)

(a)將機器 pipelining, 對單一工作的 latency time 有幫助

(b)藉由 pipelining, 可能可以提升其 throughput

(c)各個 stage 分割不平衡, 並不會影響 pipelining 的加速效果

(d)理想上, 使用 pipelining 的加速幅度約等於 stage 之數目

Ans : (b),(d)

[group12] (對抗賽)

6. 是非題

- Structure Hazard 意思為不同的 instruction 同時想要去用同一個資源
- Pipeline 能夠改善 instruction latency
- Data Hazard 中 MIPS 不會發生 RAW(read after write) 這種 type
- Pipeline 中 Control signal 需要不斷的傳到下一個 stage 的 reg 直到最後，不管有沒有需要。
- Pipeline 中 需要把 write register 傳到最後一個 stage。

Ans:

1. (o)

2.(x) 為改善 throughput

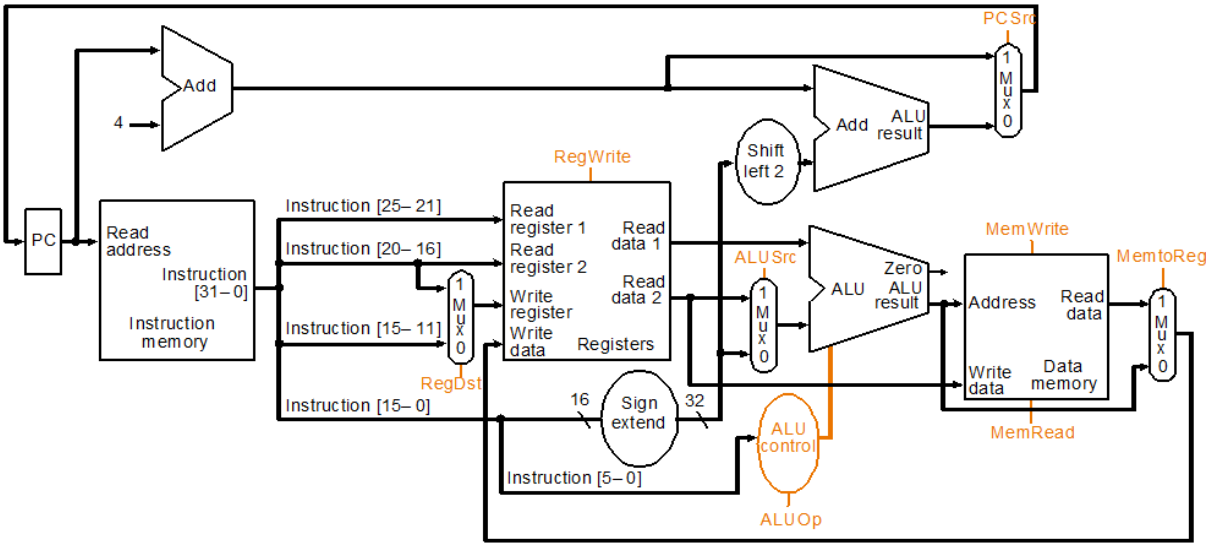
3. (x) 是 WAR(write after read) 和 WAW(write after write)

4.(x) 用到的就可以不要了，沒用到的要繼續傳下去

5. (o)

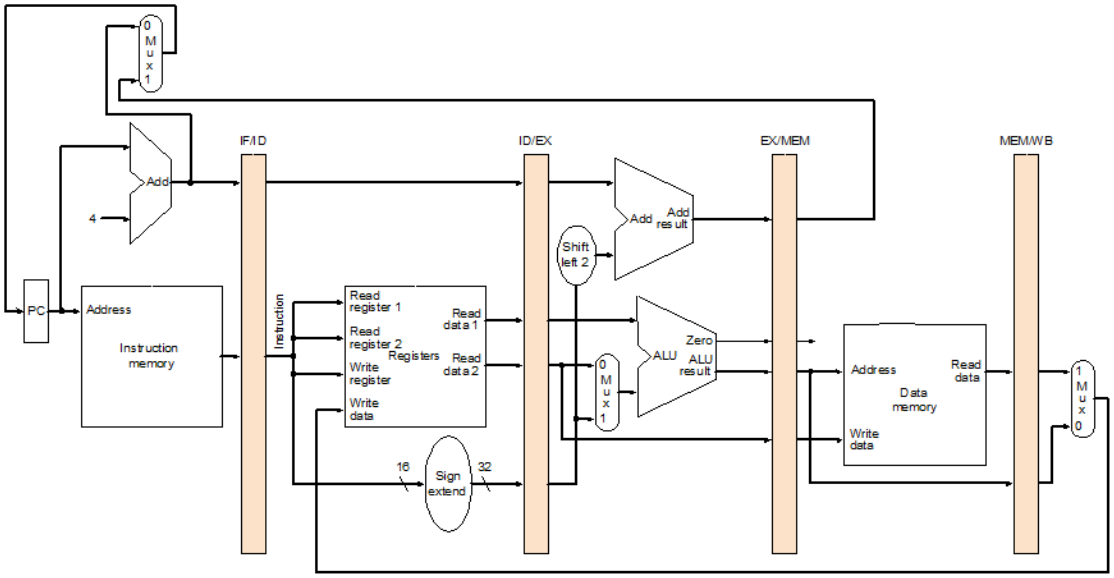
[group11]

7. In pipeline processor, we split single-cycle datapath into 5 pieces (IF, ID, EX, MEM, WB), and add four pipeline registers. Please draw the four registers and write down where the 5 pieces should be.



Ans:

IF | ID | EX | MEM | WB



[group7]

8. 請問以下那些 MIPS 指令會發生 data hazard？請畫圖表示。(我們假設每個指令的長度都一樣)

add $3 $1 $5

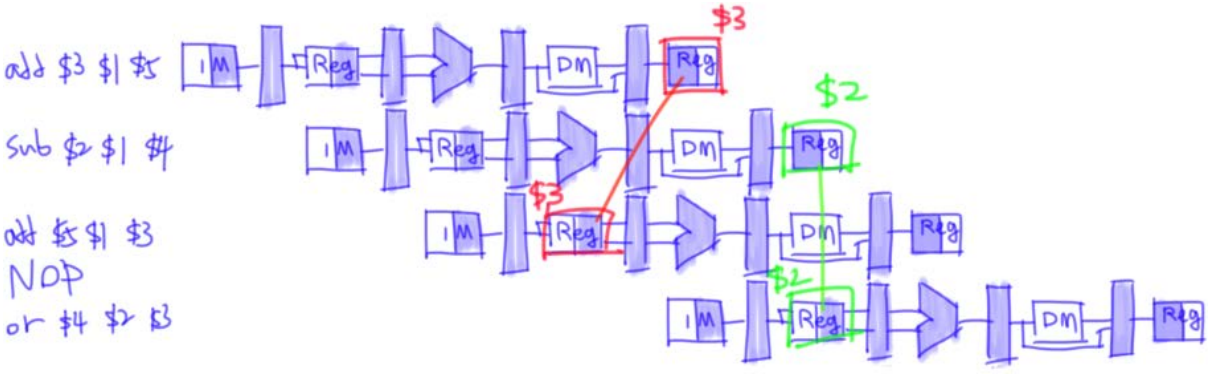
sub $2 $1 $4

add $5 $1 $3

NOP

or $4 $2 $3

A：



指令一及指令三($3 會衝突)。