CS4100: 計算機結構

Course Outline

國立清華大學資訊工程學系

一零零學年度第二學期

為什麼電腦不用十進位而用二進位？

Signal: Two States (二進制)

對、錯

本土化、非本土化

陰、陽

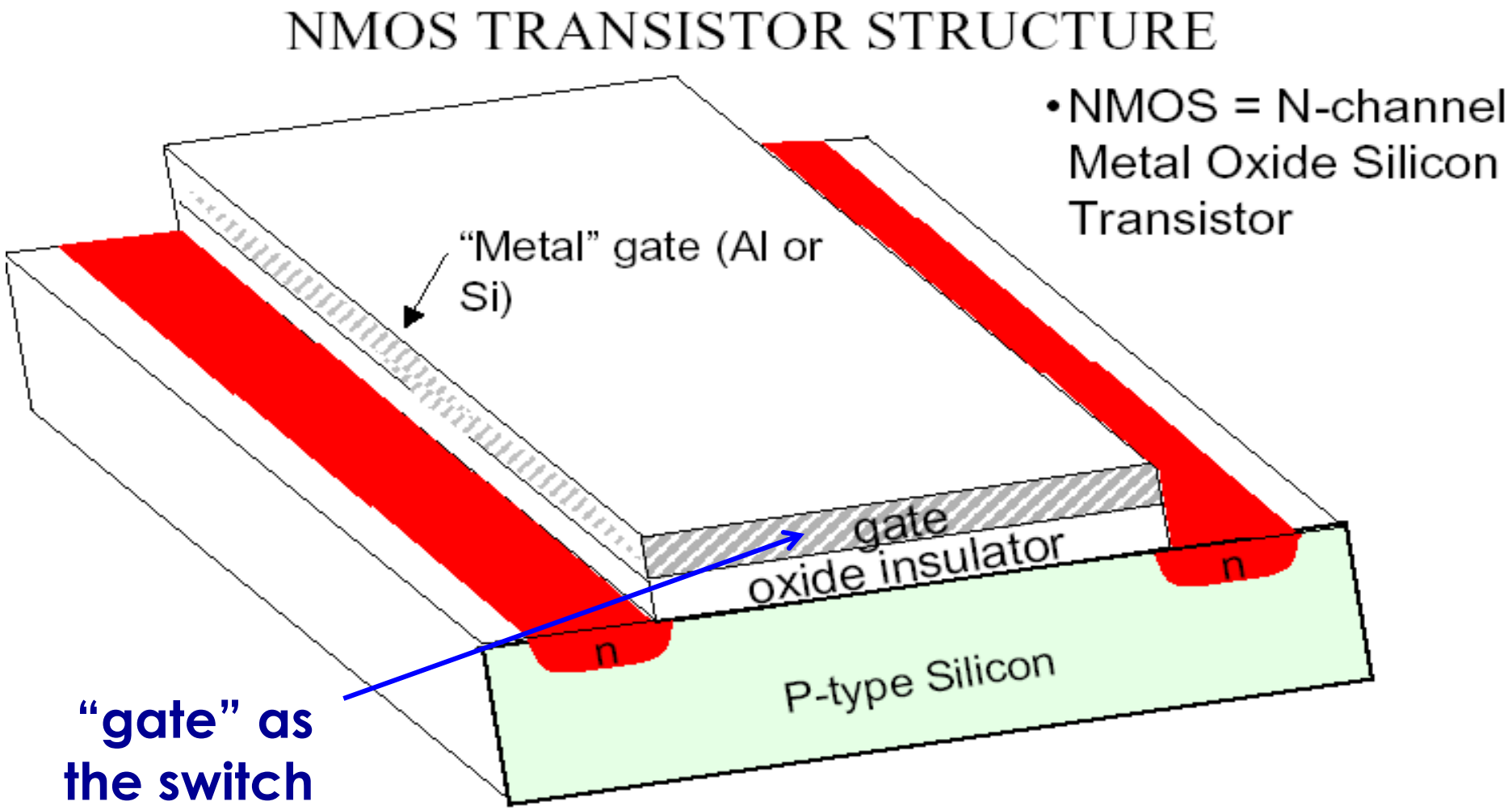
high、low

正、反

真、偽

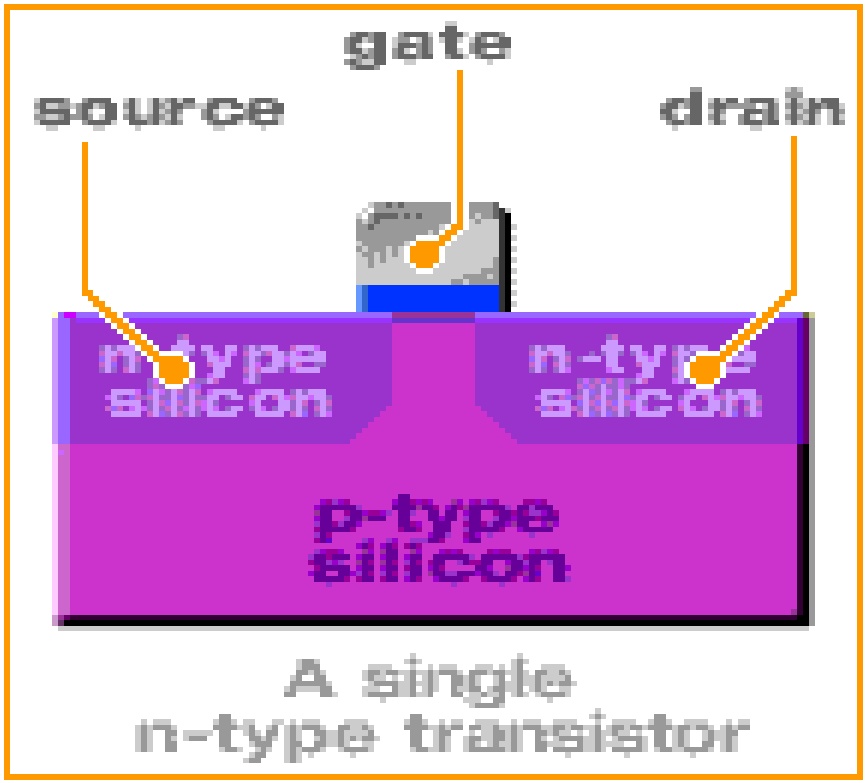
勝、負

Switch (電子開關)


NMOS TRANSISTOR STRUCTURE
•NMOS = N-channel Metal Oxide Silicon Transistor
"Metal" gate (Al or Si)
gate
oxide insulator
n
n
P-type Silicon
"gate" as the switch

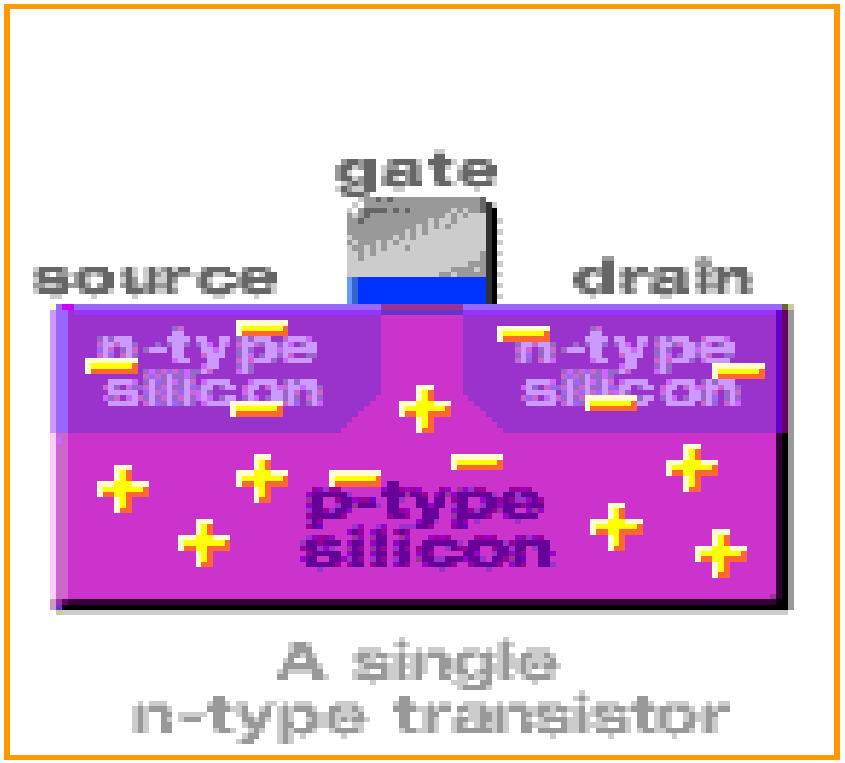
A Working Transistor (1/5)

- Transistors consist of three terminals; the source, the gate, and the drain:



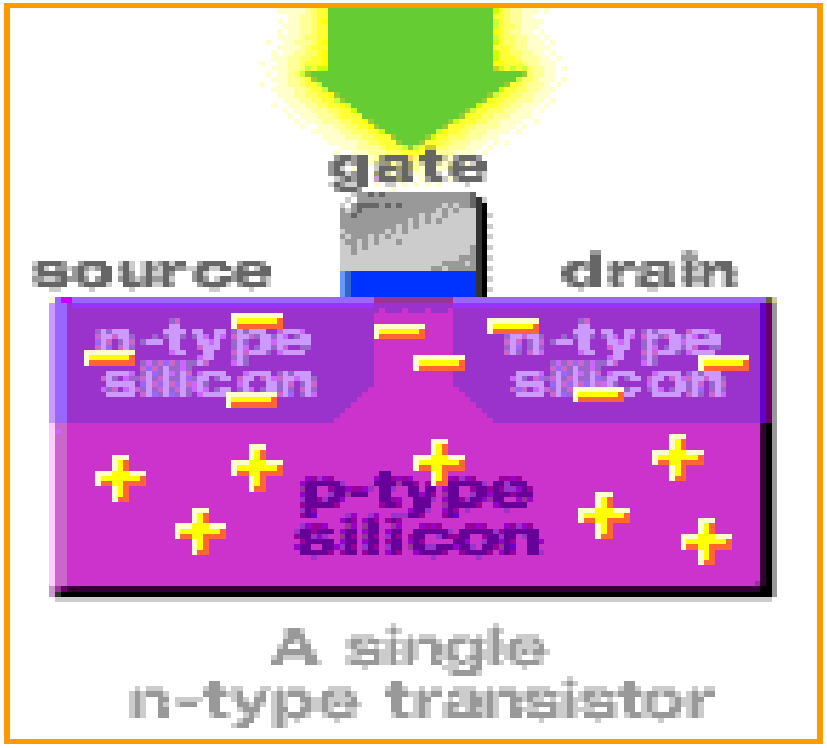
A Working Transistor (2/5)

- In the n-type transistor, both the source and the drain are negatively-charged and sit on a positively-charged well of p-silicon.



A Working Transistor (3/5)

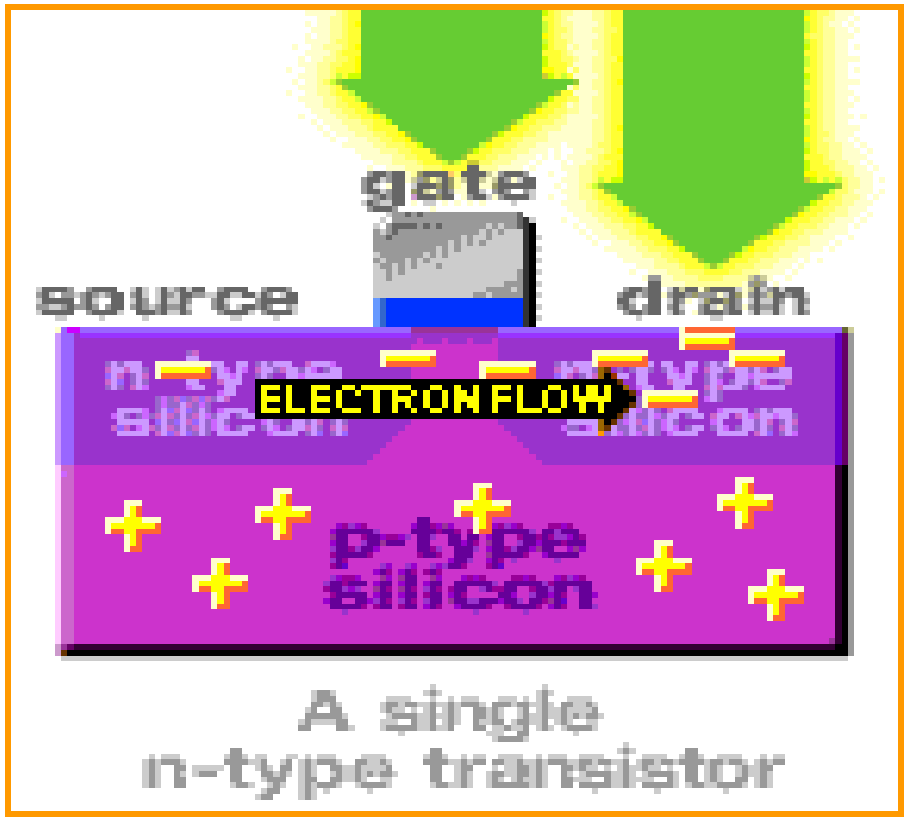
- When positive voltage is applied to the gate, electrons in the p-silicon are attracted to the area under the gate forming an electron channel between the source and the drain.



A Working Transistor (4/5)

- When positive voltage is applied to the drain, the electrons are pulled from the source to the drain. In this state the transistor is on.

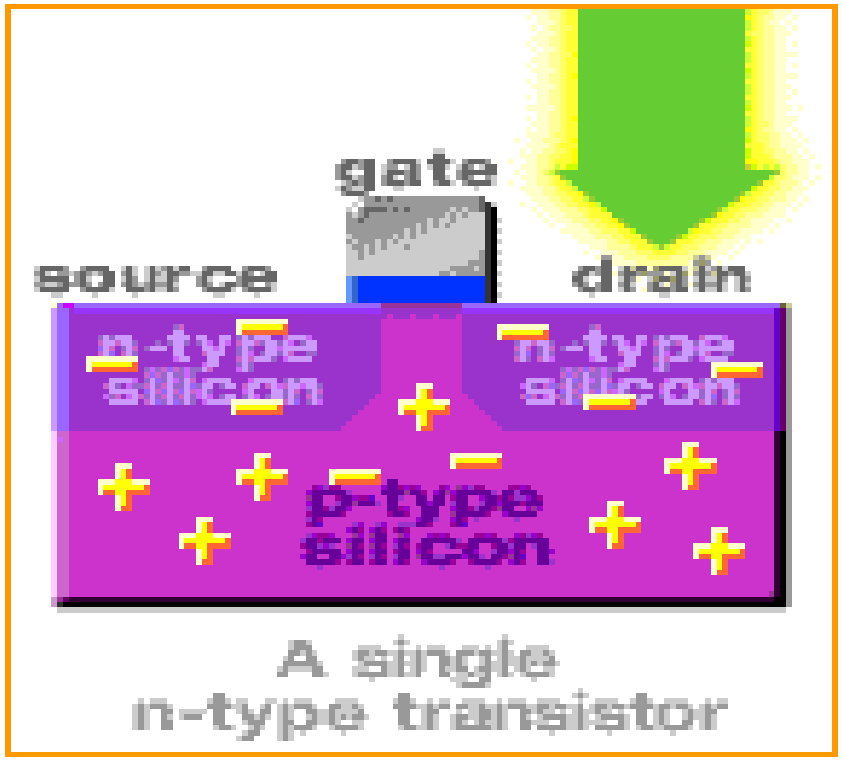
開



A Working Transistor (5/5)

- If the voltage at the gate is removed, electrons are not attracted to the area between the source and drain. The pathway is broken and the transistor is turned off.

關



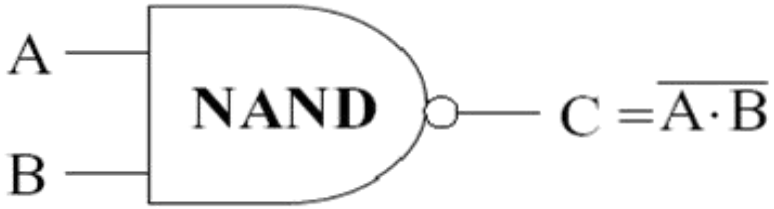
相關電壓電流特性
及電路分析等知識
我們是在_____課中介紹的

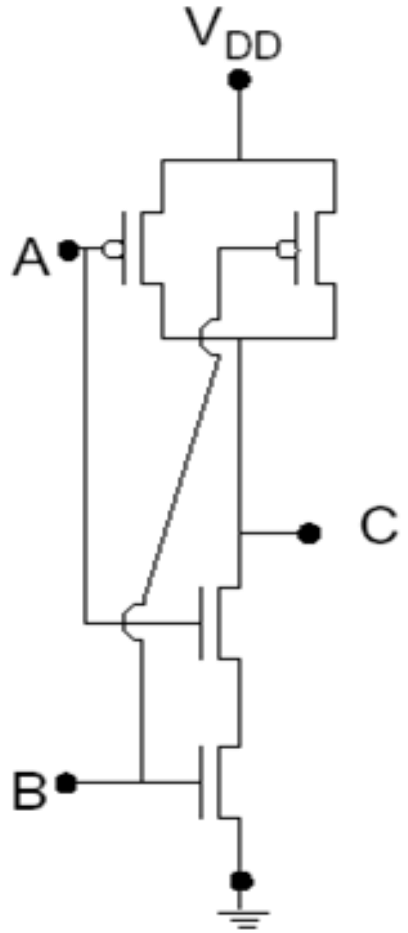
答：「電子電路學」「超大型積體電路設計」

有了開關就可以做邏輯閘

- **CMOS NAND:**

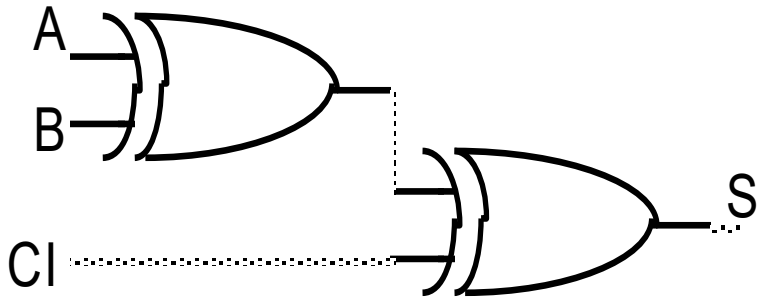
A	B	A B	C= $\overline{A\ B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

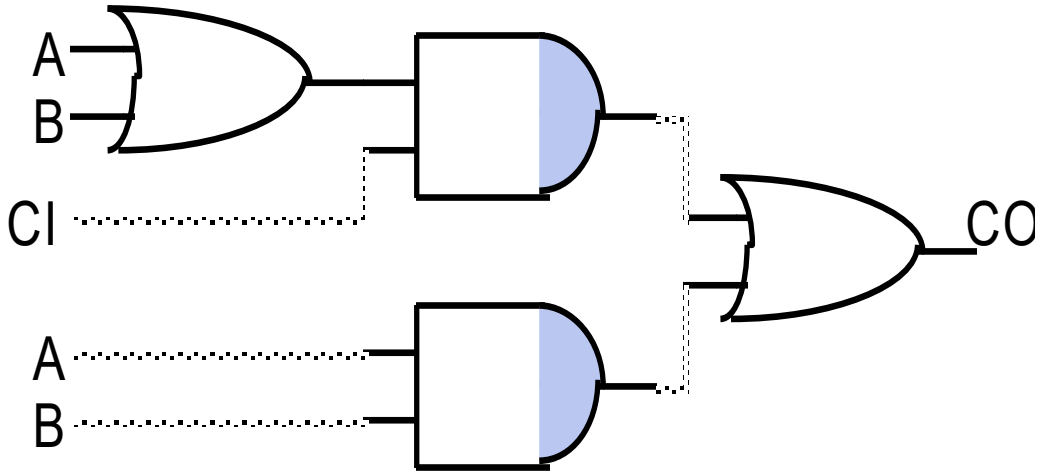




有了邏輯閘就可做邏輯電路

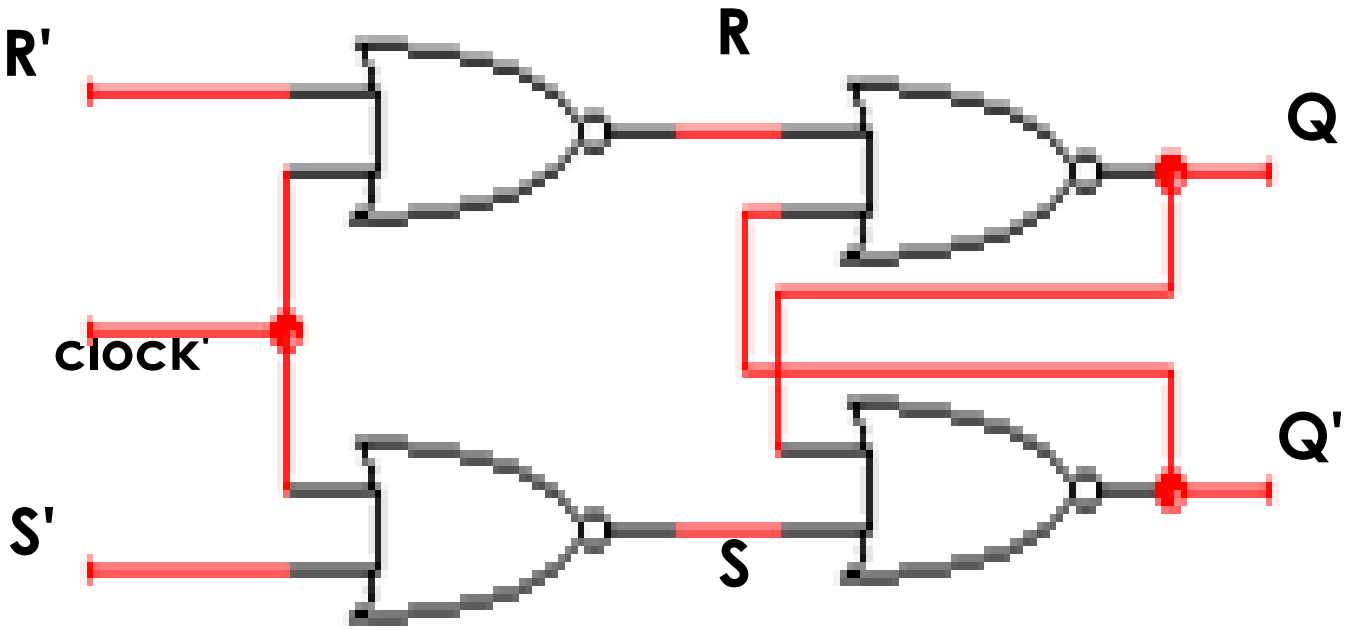
- 加法器：





也可以做記憶元件

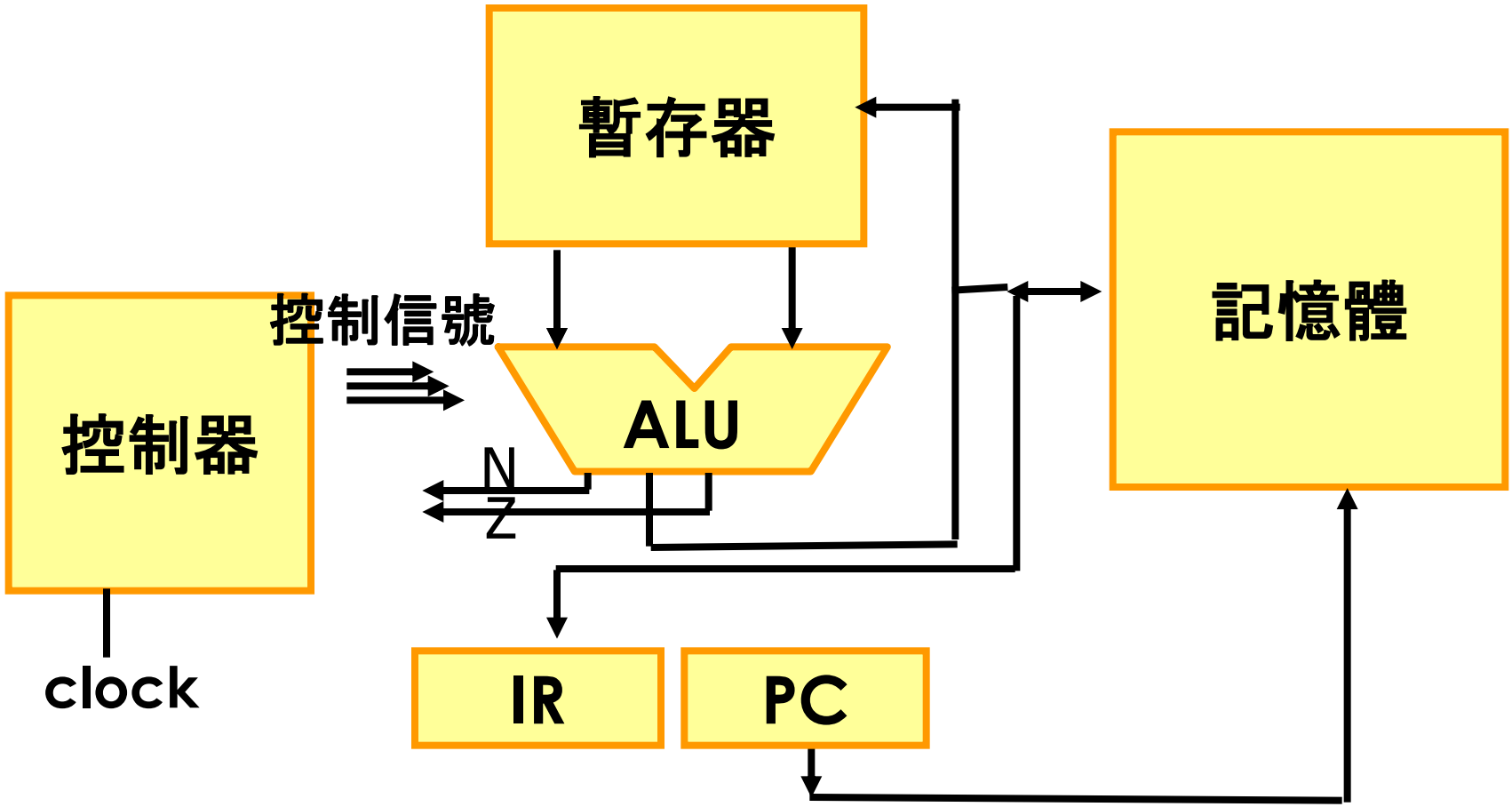
- 可存一個bit的東西：



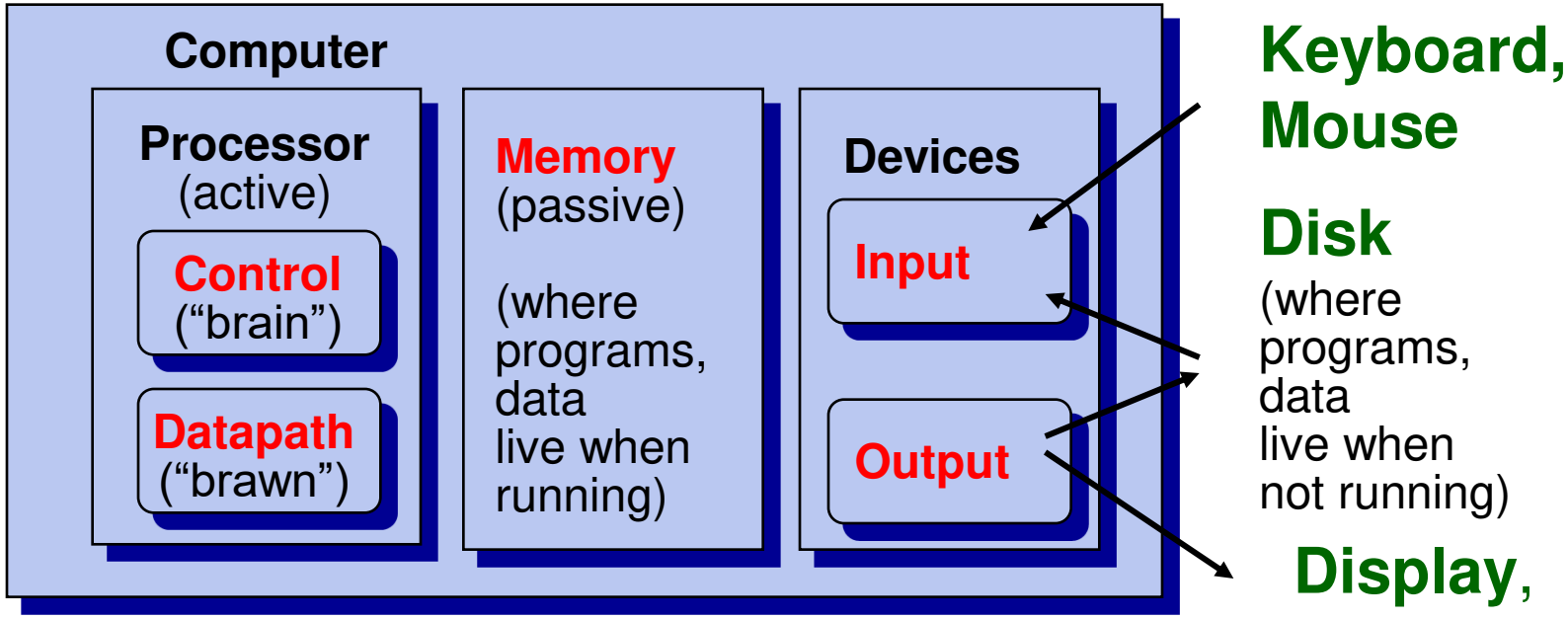
這部份的學問叫_____

答：「數位邏輯設計」

最後,
電腦的主要部份就都可以做了



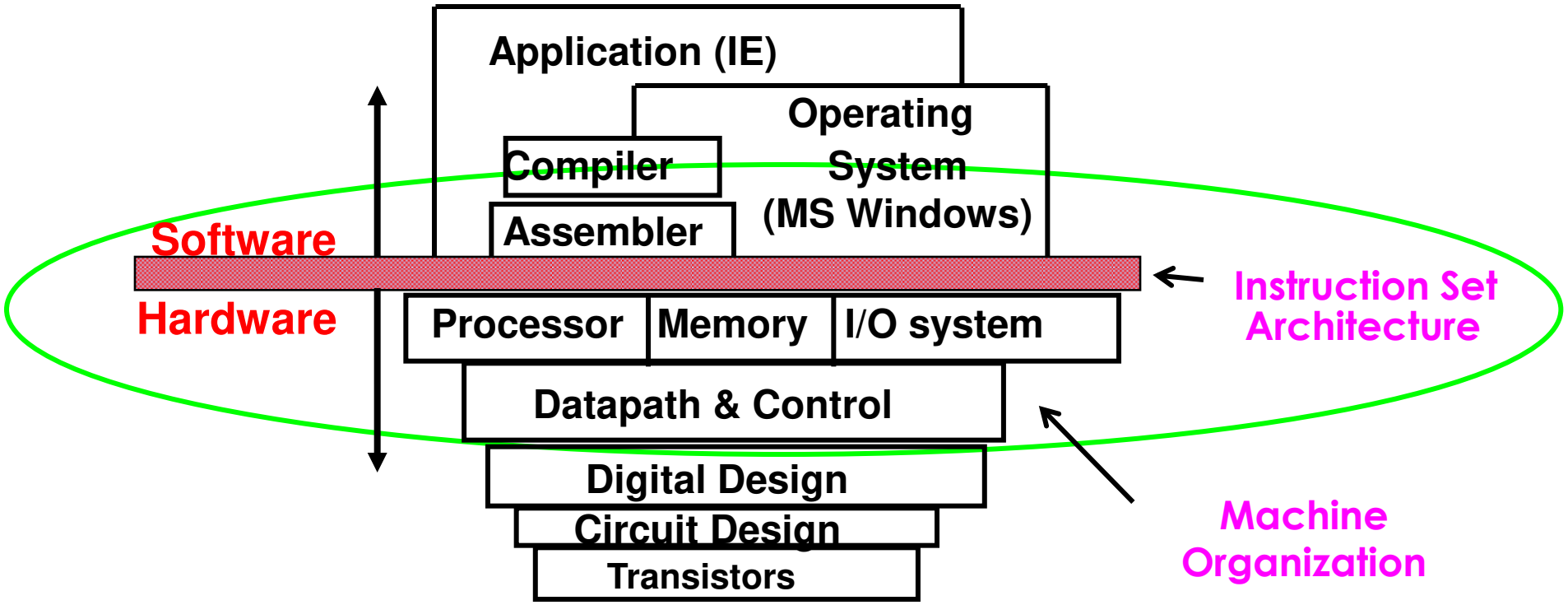
Basic Organization of Any Computer



Computer Organization

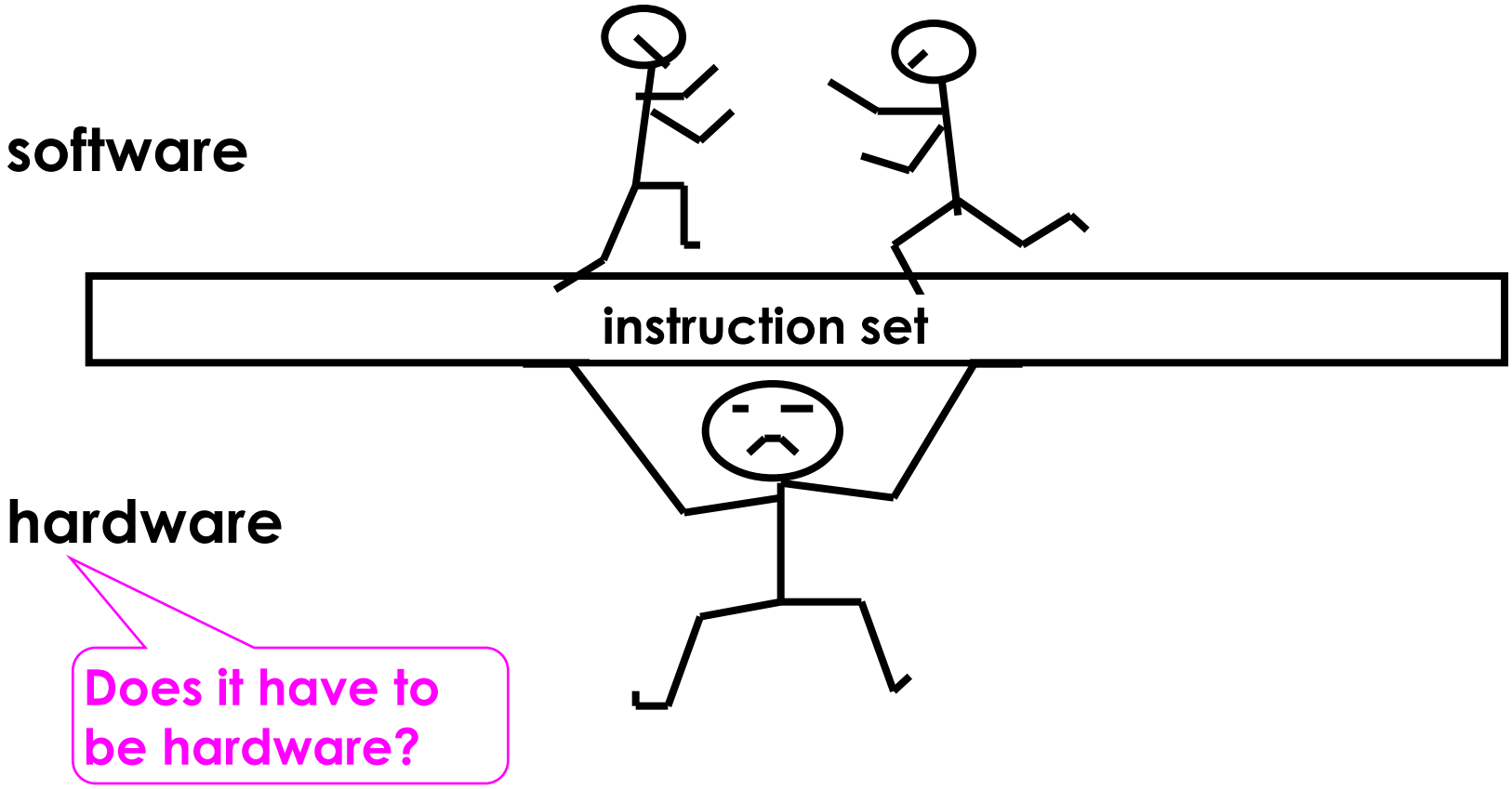
- Capabilities and performance characteristics of principal functional units, e.g., registers, ALU, shifters, ...
- Ways in which these components are interconnected (*structure*)
- Information flows between components *(data, datapath*)
- Logic and means by which such information flow is controlled (control logic)
- *Register Transfer Level* (RTL) description

What is Computer Architecture?



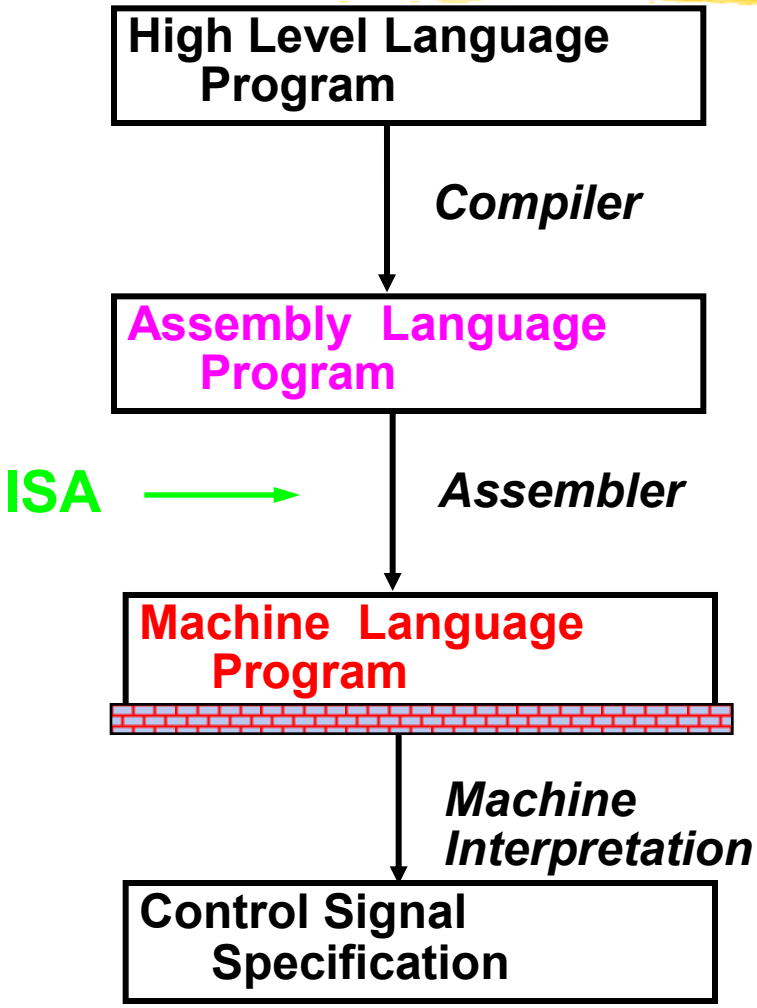
Computer Architecture =
Instruction Set Architecture
+ Machine Organization

Instruction Set as a Critical Interface



- Coordination of many levels of abstraction

Another Perspective




```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

```
lw      $15,  0($2)
lw      $16,  4($2)
sw      $16,  0($2)
sw      $15,  4($2)
```

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

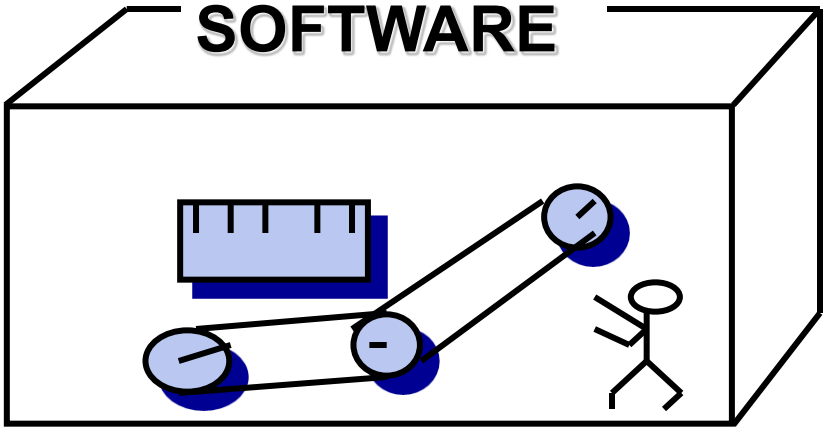
ALUOP[0:3] <= InstReg[9:11] & MASK

Instruction Set Architecture (ISA)

"... the attributes of a [computing] system as seen by the programmer, *i.e.* the conceptual structure and functional behavior, as distinct from the organization of the data flows and controls, the logic design, and the physical implementation."

— Amdahl, Blaaw, and Brooks, 1964

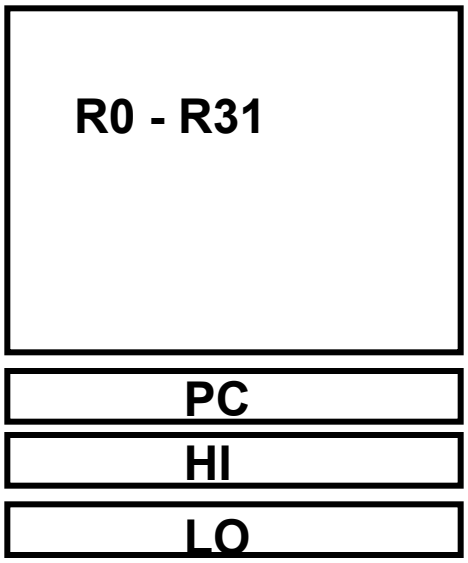
- Organization of Programmable Storage
- Data Types and Data Structures: Encodings and Representations
- Instruction Set
- Instruction Formats
- Modes of Addressing and Accessing Data Items and Instructions
- Exceptional Conditions



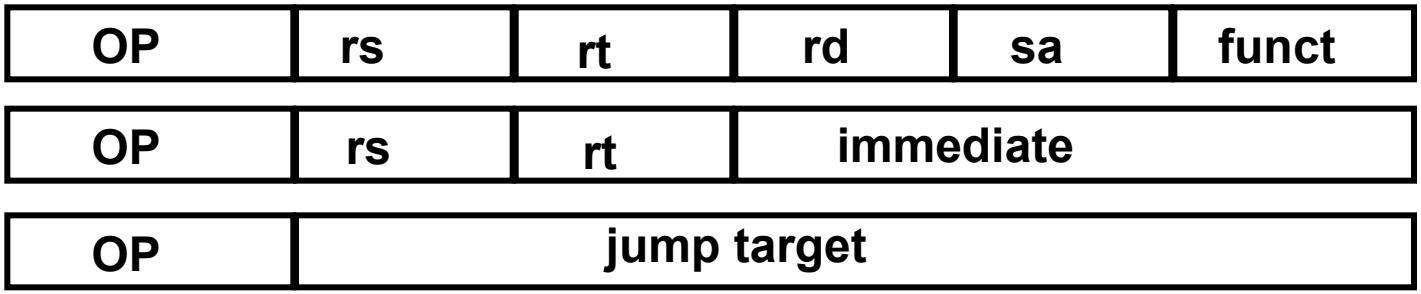
MIPS R3000 ISA

- Instruction categories:
  - Load/Store
  - Computational
  - Jump and Branch
  - Floating Point
    - coprocessor
  - Memory Management
  - Special

Registers



3 Instruction Formats: all 32 bits wide



Example ISA

Digital Alpha	(v1, v3)	1992-97
HP PA-RISC	(v1.1, v2.0)	1986-96
Sun Sparc	(v8, v9)	1987-95
SGI MIPS	(MIPS I, II, III, IV, V)	1986-96
Intel	(8086,80286,80386, 80486,Pentium, MMX, SIMD, IA-64, ...)	1978-
ARM	(v1,v2…v8)	1985-

Why Do Computer Architecture?

- RAPID CHANGES
- It is exciting!
- It has never been more exciting!
- It impacts every other aspect of electrical engineering and computer science

Course Administration

- 授課老師: 黃婷婷
  - 辦公室: 資電442　　電話: □31310
    email: tingting@cs.nthu.edu.tw
- 助教:

許博揚 pyhsu@cs.nthu.edu.tw Office Hour: wed 16:00-17:00 (資電227)
張洸鋐 s100062540@m100.nthu.edu.tw O.H.: thu 17:00-18:00 (資電 228)
丁慧玲 s100062541@m100.nthu.edu.tw O.H.: wed 17:00-18:00 (資電 228)
楊惠敏 s100062585@m100.nthu.edu.tw O.H.: tue 17:00-18:00 (資電228)

- 上課時間:
  - CS4100-02:　星期二10:10-12:00
    星期四10:10-12:00
- 上課地點: 台達館 132室
- 課程網頁:
  http://www.cs.nthu.edu.tw/~tingting/courses/cs4100.html

Text Book

***Computer Organization and Design: The Hardware/Software Interface*, 4th ed.,**
David Patterson and John Hennessy, 2010

RISC, RAID

史丹福大學
校長

Topics Covered

Computer Organization and Design: The Hardware/Software Interface,4th ed., D. Patterson and J. Hennessy, 2010

Topic	Chapter
Introduction	1
The Role of Performance	1
Instructions: Language of the Machine	2
Arithmetic for Computers	3
The Processor: Datapath and Control	4
Enhancing Performance with Pipelining	4
Exploiting Memory Hierarchy	5
Storage and Other I/O Topics *	6
Multicores, Multiprocessors and Clusters*	7

Prerequisite

- **Prerequisite courses:**
  - **Logic design**

Expected Course Workload

- Learn MIPS instruction set
- Learn processor emulators and benchmarking
- 6+ homework assignments (1 per 2 weeks) & 1 final project
  - Each assignment is a mixture of design, calculation, programming, measurement, and discussion problems
  - Assignments will be posted on the course homepage
  - Independent of, but complement, examinations
- One mid-term and one final examination
- Grade breakdown
  - Homework Assignments & Final project 30%
  - Midterm Exam (April 24): 35%
  - Final Exam (June 12): 35%

Course Problems

- Cannot make examinations
  - No makeup examinations
- Cannot turn in homework on time
  - No late homework is accepted
- What is cheating?
  - Study together in groups is encouraged
  - Work must be your own