AN1050: Using the Si3402-C PoE PD Controller in Isolated and Non-Isolated Designs

The Si3402-C integrates all power management and control functions required in a Power-over-Ethernet (PoE) powered device (PD) application. The Si3402-C converts the high voltage supplied over the 10/100/1000BASE-T Ethernet connection into a regulated, low-voltage output supply. The optimized architecture of the Si3402-C minimizes the solution footprint, reduces external BOM cost, and enables the use of low-cost external components while maintaining high performance.

The Si3402-C integrates the required diode bridges and transient surge suppressor, thus enabling direct connection of the IC to the Ethernet RJ-45 connector.

In combination with a Schottky type diode bridge, the Si3402-C provides a valid detection signature even if the CT/SP pins are not connected. This allows the designer to add external TVS protection devices to enhance common mode and differential mode surge protection.

The switching power FET and all associated functions are also integrated. The integrated switching regulator supports isolated (flyback) and non-isolated (buck) converter topologies. The Si3402-C supports IEEE 802.3 Type 1 (Class 3 and below) Powered Device applications. Standard external resistors connected to the Si3402-C provide the proper IEEE 802.3 signatures for the detection function and programming of the requested power class. Startup circuits ensure well-controlled initial operation of both the hotswap switch and the voltage regulator.

The Si3402-C is available in a low-profile, 20-pin, 5 x 5 mm QFN package. The Si3402-C is a pin-compatible replacement of the obsolete Si3402-A. PCB layouts designed for Si3402-A can be reused with Si3402-C, but some component value changes are required.

The Si3402-C's functionality is similar to that of the Si3402-A and Si3402-B but without the requirement to make a connection between the Ethernet jack and CT1, CT2, SP1, or SP2 pins when bypassing the integrated diode bridge with external Schottky diodes. Further, PLOSS functionality is removed from the Si3402-C.

KEY POINTS

- IEEE 802.3 standard-compliant solution, including pre-standard (legacy) PoE support
- Pin-compatible replacement for the obsolete Si3402-A (nploss function not available)
- Allows external Schottky diode bypass of integrated diode bridges without requiring CT/SP pin connection
- Low-profile 5 x 5 mm 20-pin QFN

1. Introduction

Power over Ethernet (PoE) is an IEEE standard (IEEE 802.3-2012) for delivering power through Ethernet cables. The first PoE standard (IEEE802.3af) was ratified in 2003. This standard defined power classes 0–3 with a maximum cable current of 350 mA and 15.4 W power delivery capability. This was extended to 30 W (Class 4) by the IEEE802.3at standard in 2009. According to the revised standard, the maximum cable current is 600 mA. The PoE devices were divided into two types:

- Type 1 devices, which are compatible with the 802.3af standard.
- Type 2 devices, which are compatible with the newly-defined Class 4 power class. These devices are also called PoE+.

The 802.3at standard is backward-compatible with the 802.3af version, and the latest published IEEE802.3-2012 standard contains the 802.3at specification.

Two configurations of connection of PSEs to PDs are shown in the figures below. The option shown in the first figure must be used for “midspan equipment”, which injects power on the Ethernet connection of an existing Ethernet link. Endpoint equipment, such as an Ethernet switch, can use either option.

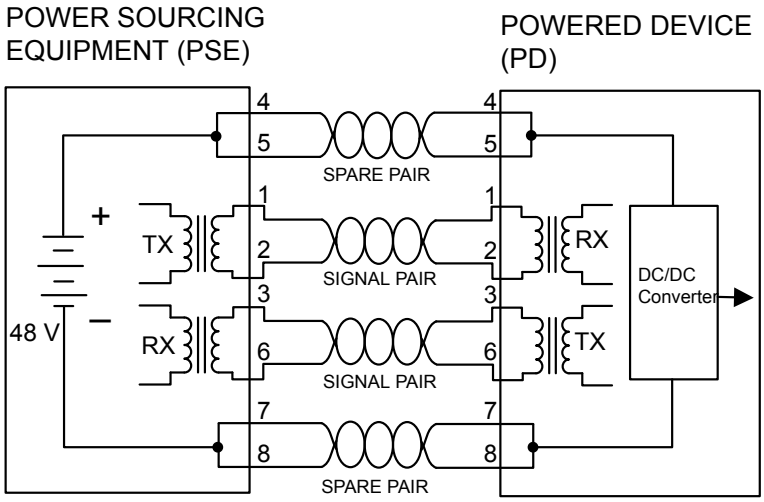


Figure 1.1. Power Delivered over Spare Pair (Midspan)

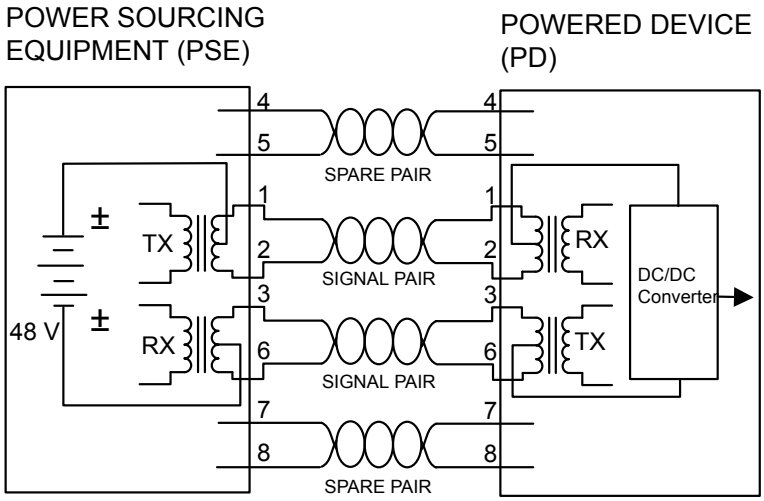


Figure 1.2. Power Delivered over Signal Pair

Introduction

The IEEE802.3-2012 Type 1 compatible Power Sourcing Equipment (PSE) supplies 44 to 57 VDC and must be isolated from earth ground. The powered device (PD) must not consume more than 12.95 W (PD input power for Class 3), which translates to no more than 350 mA (Type 1) of steady state input current, allowing for 20 Ω of cabling resistance between the PSE and PD. This means that with practical conversion efficiencies, approximately 10 W of regulated power is available to PD applications, making PoE a preferred alternative for powering devices, such as VoIP phones, wireless routers, and security devices, because it eliminates the need for a local power source, greatly simplifies installation, and allows easy power backup through an uninterruptible power source (UPS) on the PSE end. The advantages of IEEE 802.3-2012-compliant equipment include:

- This standard provides a way for the PSE to recognize that the PD side is PoE-enabled and not supply power unless a valid signature is detected, thus eliminating the possibility of damaging equipment that is not PoE-enabled.
- This standard provides a method of allowing the 802.3af PD device to supply classification information to the PSE so that the PSE can determine the load requirements of the multiple pieces of PD equipment it is powering.
- This standard ensures interoperability of PSE and PD devices from different manufacturers.

The Si3402-C device is a highly-integrated, efficient IC with both a Power over Ethernet PD interface and PWM dc-dc converter. It is fully-compatible with IEEE 802.3-2012 Type 1 specification, and has a two-step inrush current-limiting feature to allow PD designs that are compatible with pre-standard PSE equipment. It supports PD designs that require isolation between the Ethernet cables and powered equipment as well as the lower-cost option without isolation for fully-enclosed devices.

This application note covers the basic operation of the Si3402-C as well as design equations and selection criteria for signature resistors and capacitors, dc-dc converter power train, input filter, output filter, feedback and compensation, soft-start, duty cycle limits, and switcher current limit. The Si3402-C also features integrated surge protection.

2. Typical Application Schematics

The following figures show the basic application circuits for the Si3402-C evaluation board.

Note:

1. The external diode bridge (D8–D15), built from Schottky type diodes, is recommended for high power levels (Class 3 operation). For lower power levels, such as Class 1 and Class 2, the diodes can be removed.
2. The Si3402-C is detectable by the PSE even if the CT/SP pins are not connected. If CT/SP are not connected, then external Schottky type bridge must be used.

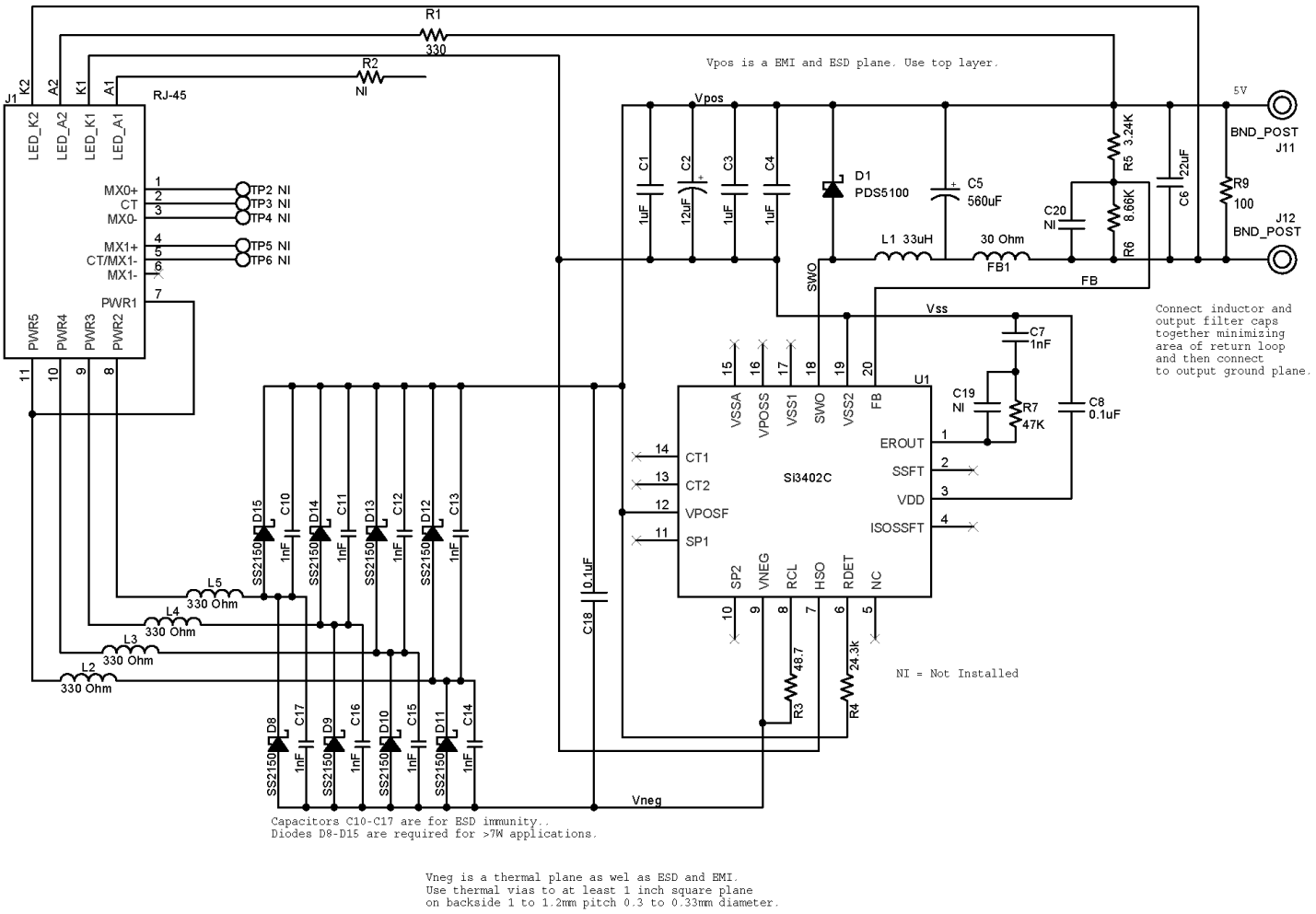


Figure 2.1. Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output)

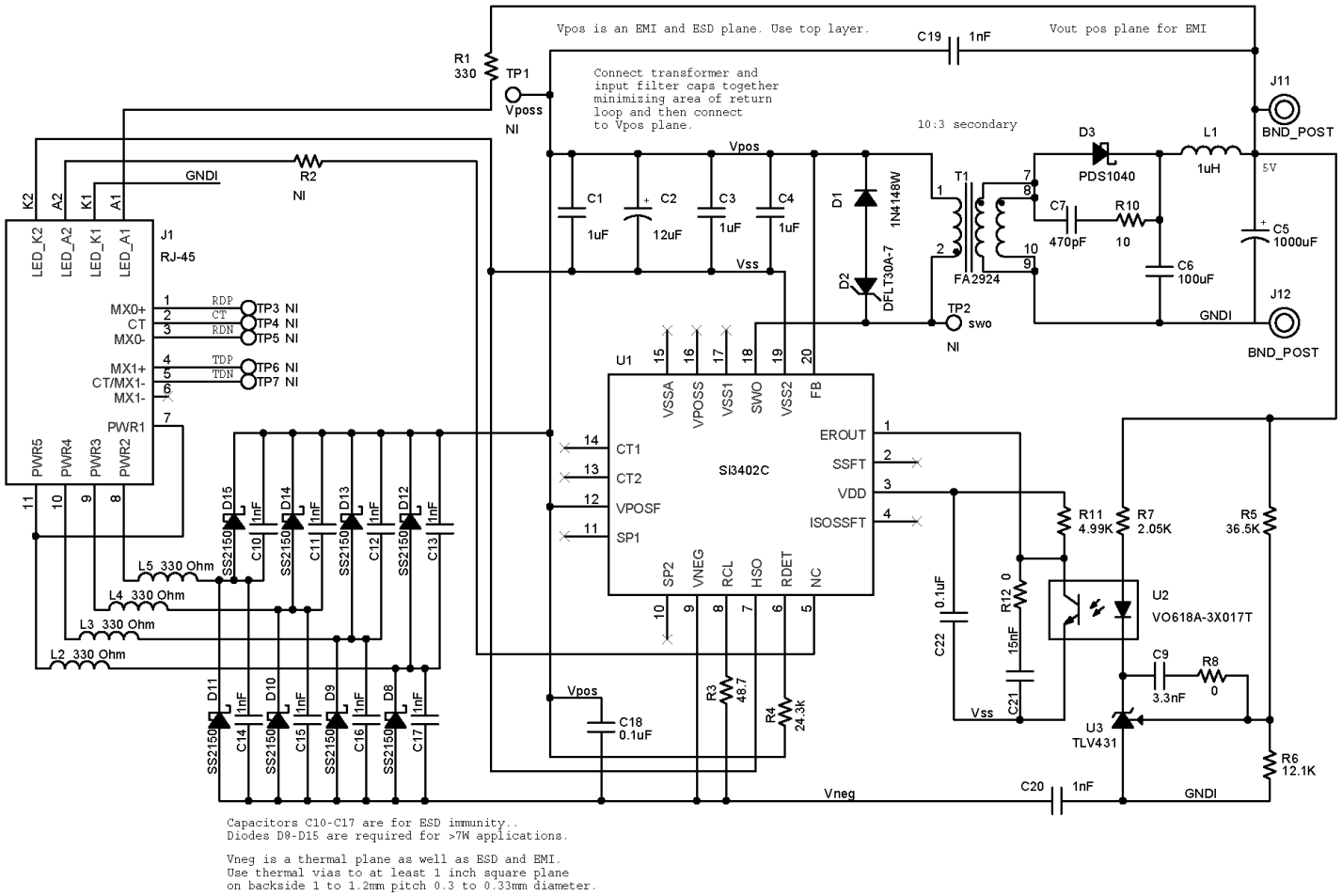


Figure 2.2. Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output)

3. Detection, Classification, and Power Sequencing

The circuit configurations shown in Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4 and Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5 have the same operation during detection, classification, and power sequencing. A full power cycle is shown in the following figure.

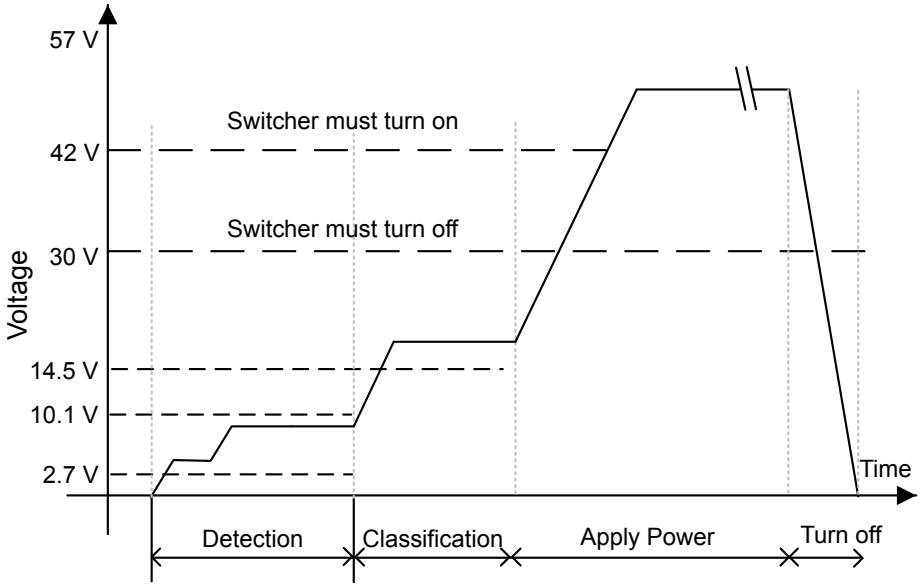


Figure 3.1. Full Power Cycle

As described in more detail below, a low voltage is used to detect a valid PD; a higher voltage is used to classify the power level of the PD, and full-power operation starts at voltages of 42 to 57 V.

3.1 Diode Bridge

The internal diode bridge of Si3402-C can be used for up to 10 W input power.

Above 10 W input power, an external diode bridge is required. If the CT/SP pins are connected, then either a standard or Schottky external diode bridge can be used.

The Si3402-C is capable of operating with CT/SP pins open. In that case, the external diode bridge must be the Schottky type.

3.2 Detection

During the detection phase, the PSE applies two voltages between 2.8 and 10 V dc and measures the current (with a current limit of 5 mA). The slope of the I-V characteristic of the PD must be between 23.75 and 26.25 kΩ. This slope is set by the resistor, RDET (R4 in Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4 and Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5). 24.3 kΩ 1% resistor ensures valid detection in all conditions. Additionally, the input capacitance must be between 50 and 120 nF, which is set by the capacitor, CDET (C18 in Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4 and Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5).

If Schottky type external bridge is used, it can happen that the PSE will not detect the PD with 24.3 kΩ 1% detection resistor due to the nature of the Schottky type diode leakage current, which rises with temperature rise. The solution for this is to use 24.9 kΩ 1% RDET if Schottky type external bridge is used. The low voltage and current applied in the detect phase as well as the requirement for specific values of resistance and capacitance makes it unlikely that non-PoE-enabled equipment will be recognized if plugged into PSE equipment that supports PoE.

3.3 Classification

During the classification phase, the PSE applies a voltage between 15.5 and 20.5 V, current-limited to 100 mA, and determines the maximum output power requirement: PD requested Class, based on the current consumed by the PD.

Table 3.1. Supported Power Levels

Class	Power Level that PSE Must Support
0	15.4 W
1	4.0 W
2	7 W
3	15.4 W

Over the range of 14.5 to 20.5 V, the PD current during the classification stage must be as shown in the following table.

Table 3.2. Classification Stage PD Current

Class	Minimum Current	Maximum Current	Units
0	0	4	mA
1	9	12	mA
2	17	20	mA
3	26	30	mA

The classification current for the Si3402-C is set by the resistor, Rclass (R3 in Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4 and Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5.

3.4 PoE Power Clarification

Per the IEEE standard for Type 1 configuration, the maximum allowed cable resistance is Rmax = 20 Ω between the PSE and PD. Additionally, the standard defines the following magnitudes: PSE maximum output current (Iout_max PSE), PSE minimum output voltage (VPSE_out_min), and PSE output power (PPSE_out).

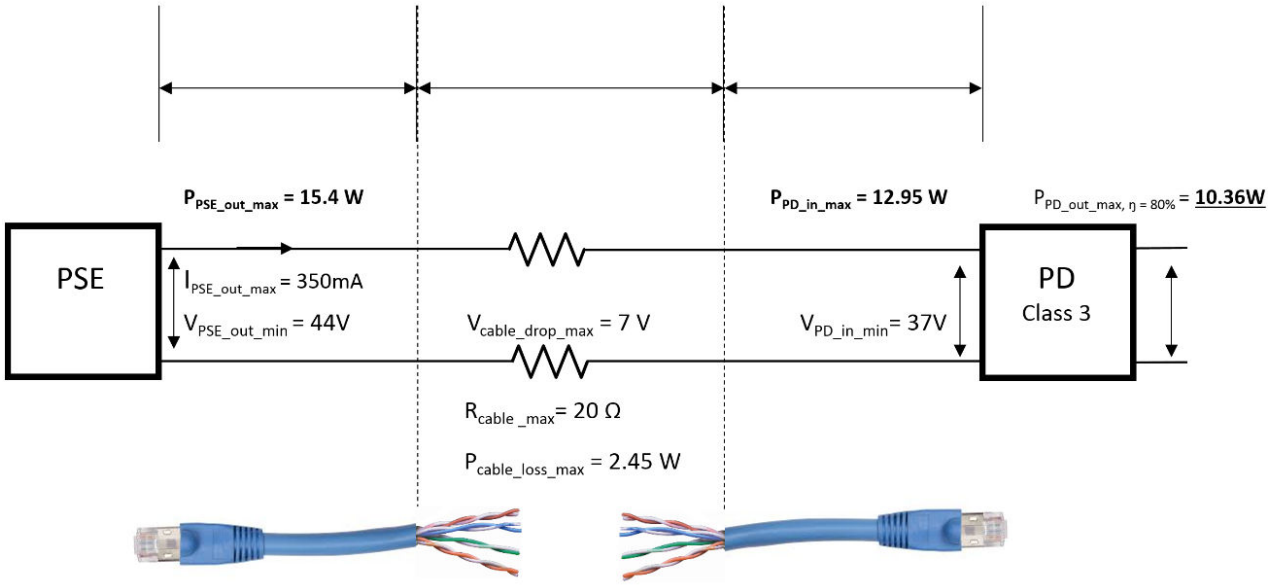


Figure 3.2. Power Clarification in Class 3 Example

The above figure represents an example for Type 1, Class 3 option. Due to the resistance of the Ethernet cable, by increasing the PSE output current, a significant power loss can occur in the cable. In worst-case (20 Ω cable resistance + maximum PSE output current I = 350 mA for Class 3), it means almost 2.5 W of cable losses. By reducing the cable length, this loss can be decreased, but it is strongly recommended to include the reduction in the calculations. The following table includes a brief summary of power magnitudes required and allowed by the IEEE standard.

Table 3.3. Type 1 Power Magnitudes by PoE Classes with Maximum Allowed Cable Resistance

Class	PSE Pout Max [W]	Rcable Max [Ω]	PSE Vout Min [V]	PSE Iout Max [mA]	Max Cable Loss [W]	PD Pinmax [W]	PD Pout max η = 80% [W]	Type
0	15.40	20	44	350.00	2.45	12.95	10.36	1
1	3.84	20	44	87.27	0.15	3.69	2.95	1
2	6.49	20	44	147.50	0.44	6.05	4.84	1
3	15.40	20	44	350.00	2.45	12.95	10.36	1

3.5 Powerup

During detection and classification, the PD must isolate the switcher input filter and not apply power to the load. After completion of this phase, the PSE ramps up to between 44 and 57 V, and PD turns on by closing the internal hot swap switch.

The PD must turn on at an input voltage of 42 V. After turning on, this voltage can drop to 37 V due to cabling resistance.

The Si3402-C hot swap switch has a two-step current limit. The input filter capacitor is first charged to about 1% less than VPOS of its final value at a typical current of 150 mA. When the filter input capacitor is nearly charged, the current limit is increased to over 400 mA, and the switcher is allowed to turn on. The hot swap switch operates at the higher current limit as long as the input voltage is higher than UVLO (falling edge).

The Si3402-C is designed so that the hot swap switch current limit is generally not the limiting factor in terms of the amount of power the PD can draw. This limit is intended to be set by the application or by the PSE.

However, to limit inrush current as the switcher turns on, the switcher design supports integrated dynamic soft-start operation, which is further described in the detailed switcher descriptions of this application note.

The following figure shows the input current and output voltage vs. time when 48 VDC is suddenly applied to the PD circuit. The initial current spike is due to the charging of the 0.1 µF input capacitor. For this particular device, the filter capacitor charges up with a current limit of 141 mA in 5 msec.

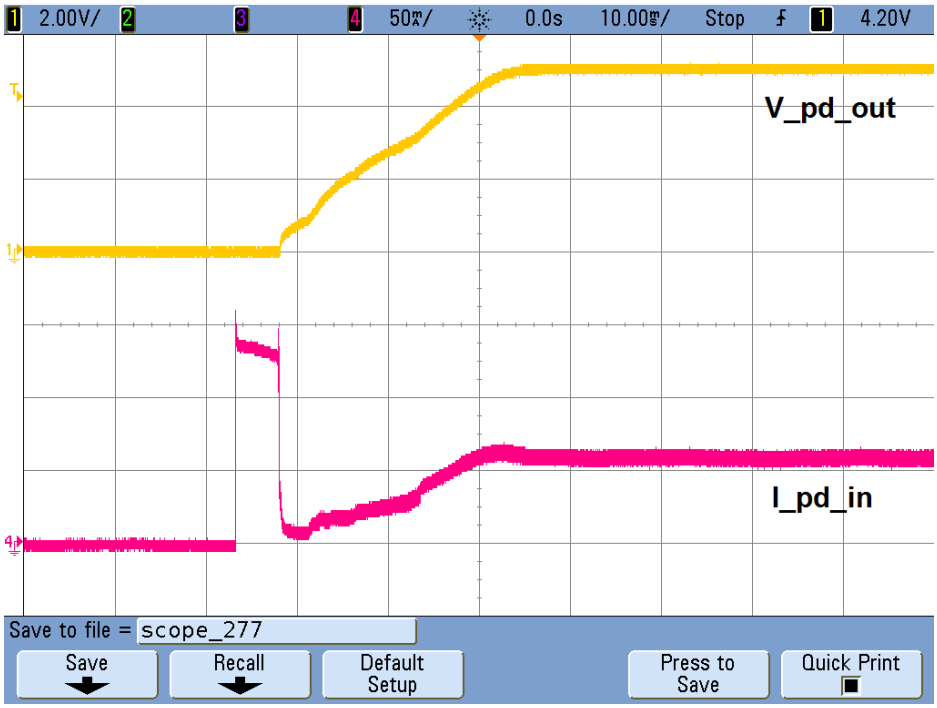


Figure 3.3. Typical Startup Waveform with 2.5 Ω Load

3.6 Maintain Power Signature (MPS)

The PSE detects the dc current to the PD by either looking for the low ac impedance of the input filter or by verifying that it is drawing current.

For this reason, the input filter capacitor must be >5 µF, and the load must be such that the input current is >10 mA. Since the Si3402-C is designed to be very efficient and dissipate very little power, there is a minimal load current requirement of 250 mW (50 mA at 5 V output) so as to draw >10 mA from the input supply. If the Si3402-C converter circuit consumes less than 10 mA from the PSE, the PSE will disconnect that particular port. This port will be in the loop of detection, classification, turn ON, and turn OFF until the PD consumption rises above 10 mA. To ensure stable connection with the PSE, it is recommended that a 250 mW load always be present.

3.7 Turn Off

The minimum input voltage level at which the PD is required to turn off is 30 V.

The Si3402-C has approximately 4 V of hysteresis between turn-on and turn-off with respect to the voltage across the switcher input filter capacitor so that inrush current at startup will not cause the part to turn off.

3.8 Signature Resistors and Capacitors and Component Selection Criteria

The Si3402-C is designed to meet IEEE 802.3 signature requirements with RDET (connected to pin RDET) = 24.3 kΩ, ±1%.

Recommended resistor values for RCLASS (connected to pin RCL) are listed in the following table.

Table 3.4. RCLASS Recommended Resistor Values

Class	Requested PSE Power Level	RCLASS ±1%
0	15.4 W	Open Circuit
1	4.0 W	140 Ω
2	7 W	75 Ω
3	15.4 W	48.7 Ω

The voltage across these resistors is limited so that 0603 or larger surface mount resistors may be used.

C18 should be a 100 V, X7R type surface mount with tolerance of ±10%. While this type of capacitor exhibits strong voltage and temperature dependency, the 50–120 nF requirement of IEEE 802.3 will be met.

3.9 Input Filter

IEEE 802.3 requires that the input filter capacitor be greater than 5 µF. Additionally, the ripple at the RJ–45 input at the switching frequency of approximately 350 kHz must be less than 150 mV. To reduce the chance of conducted or radiated emissions due to induced common-mode voltage on the Ethernet cable pairs, it may be desirable to further reduce the input ripple.

To maintain the >5 µF input capacitance, an aluminum electrolytic capacitor (e.g., Sanyo 100ME12AX or Panasonic EEUFC120) is used. This capacitor has an ESR of up to 0.4 Ω and results in excessive input ripple caused by the ripple current from the switcher, which can be as much as 3 A. To keep input ripple down, it is recommended that additional X7R surface mount capacitors be used in parallel (for example, a 1 µF, 100 V, X7R 1210 capacitor with an ESR of less than 0.6 mΩ is available from several vendors).

The input filter capacitor also helps to absorb surge current. The IEEE 802.3 standard requires a minimum input filter capacitor value of 5 µF. An input filter capacitor of 15 µF total has been found to be a good compromise between price, size, and performance.

4. DC-DC Converter Operation

There are two basic configurations for the dc-dc converter: buck and flyback. Additionally, the converter may be designed so that its power output is electrically isolated from the power input. Per IEEE 802.3, PDs shall provide isolation between all accessible external conductors, including frame ground.

In the non-isolated case, buck topology is generally used, and, in the isolated case, flyback topology is generally used. It is possible to use flyback topology in the non-isolated case, although this is not described in detail in this application note.

The equations used for determining all of the components surrounding the switching converter are briefly described below.

4.1 Non-Isolated Buck Design

Under most conditions, the current through the inductor (L1 in Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4) is continuous, and the voltage across the inductor switches from positive to negative as shown in the figure below.

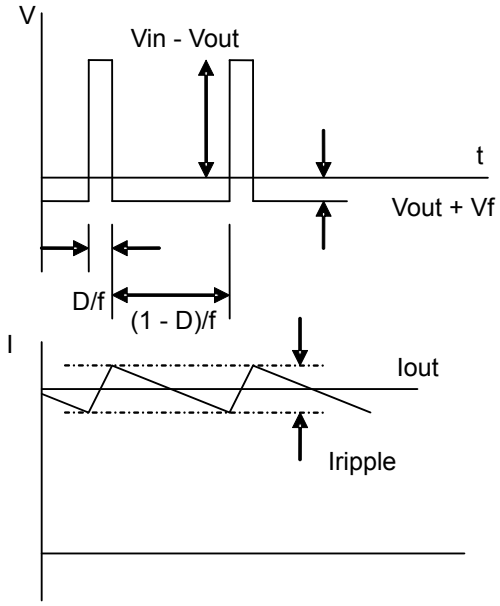


Figure 4.1. Voltage Polarity

The average voltage across the inductor must be zero; so, the duty cycle is:

$$D \times (V_{in} - V_{out}) = (1 - D) \times (V_{out} + V_f)$$

Where V_{out} is the desired output voltage; V_f is the forward drop of the diode (D1 in Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4), and V_{in} varies with the PD input voltage, which is generally 42–55 V. Solving:

$$D = \frac{(V_{out} + V_f)}{(V_{in} + V_f)}$$

The ripple current that must be supported in the output filter is:

$$I_{ripple} = \frac{(V_{in} - V_{out}) \times (V_{out} + V_f)}{((V_{in} + V_f) \times L \times f)}$$

Where:

L is the inductance.

L = 33 µH, Vout = 5 V, V_{in} = 53 V, V_f = 0.5 V

R_{ESR} = Internal resistance (Equivalent Series Resistance)

f is the internally-set switch frequency of approximately 350 kHz
I_{ripple} = 441 mA

This is the ripple current into the output filter. The peak-to-peak ripple current that must be handled by the input filter is equal to the average current delivered to the output plus half of the ripple current in the inductor.

The rectifier diode in the non-isolated design must be rated for at least the input voltage. Generally, a 100 V diode is chosen for margin. A Schottky diode is preferred to avoid the large voltage drop and excess power associated with stored charge. Typical part numbers are PDS5100 from Diodes Incorporated or the equivalent UPS5100 from Microsemi. Note that these 100 V diodes have a larger forward drop than the lower voltage diodes used for the non-isolated design below.

Overall efficiency is determined by dividing the output power by the input power including conduction losses in the inductor, rectifier, switching FET, input bridge, and hot swap switch, as well as bias and switching losses.

4.1.1 Output Voltage (Non-Isolated Design)

The output voltage in the isolated case is determined by R5 and R6 according to the following equation:

$$V_{out} = 1.35 \times \left(1 + \frac{R6}{R5}\right)$$

For example, for a 5 V output, values of 8.66 kΩ for R6 and 3.24 kΩ for R5 are recommended.

The supported minimum output voltage in a non-isolated buck topology is 3.3 V. A lower output voltage would result in an excessively low duty cycle, which is not supported by the Si3402C.

4.1.2 Output Filter and Loop Stability—Non-Isolated Design

Generally, the current in the output inductor is continuous (does not return to zero). The current becomes discontinuous for very light loads, but the continuous mode of operation is most difficult to stabilize due to the LC filter resonance that occurs in this case.

The output filter section has a resonant frequency described by the following equation:

$$\frac{1}{2 \times \pi \times \sqrt{LC}}$$

The circuit will be critically damped with a resistance of:

$$2 \times \sqrt{\frac{L}{C}}$$

For a typical 33 µH inductor and 560 µF filter cap, the resonant frequency is 1170 Hz, and the resistance for critical damping is 0.48 Ω.

The damping resistance is a combination of capacitor ESR, inductor series resistance, and switch and diode resistance. It has been found that the combination of switcher FET resistance and Schottky diode effective series resistance results in an effective 0.5–1 Ω in series with the inductance for the recommended applications circuit. This damps the output resonance and allows for the use of low ESR filter capacitors without stability concerns.

The network of Rc and Cc stabilizes the feedback loop by introducing a zero in the feedback loop. It has been found that values for C7 and R7 of 1 nF and 47 kΩ, respectively (see Figure 2.1 Non-Isolated Buck Configuration for Si3402-C-EVB (5 V Output) on page 4), work well. This translates to a zero at 3.3 kHz.

For designs that must operate below 0 °C, it has been found that a low ESR 560 µF capacitor, such as the Panasonic EEU-FM0J561 gives better results with the same stability network.

4.1.3 Soft Start Non-Isolated Case

The Si3402-C has an internal dynamic soft-start circuitry, which further reduces BOM costs. The dynamic soft-start function adapts the rise time to the load attached to the output at start-up. Under light load conditions, the rise time is very short, typically 5–10 ms. Under heavy load conditions at start-up, the rise-up time is much longer to ensure safe power-up and no overshoot voltage on the output.

A typical startup waveform on the buck-based EVB board with a 2.5 Ω load is shown in the following figures.

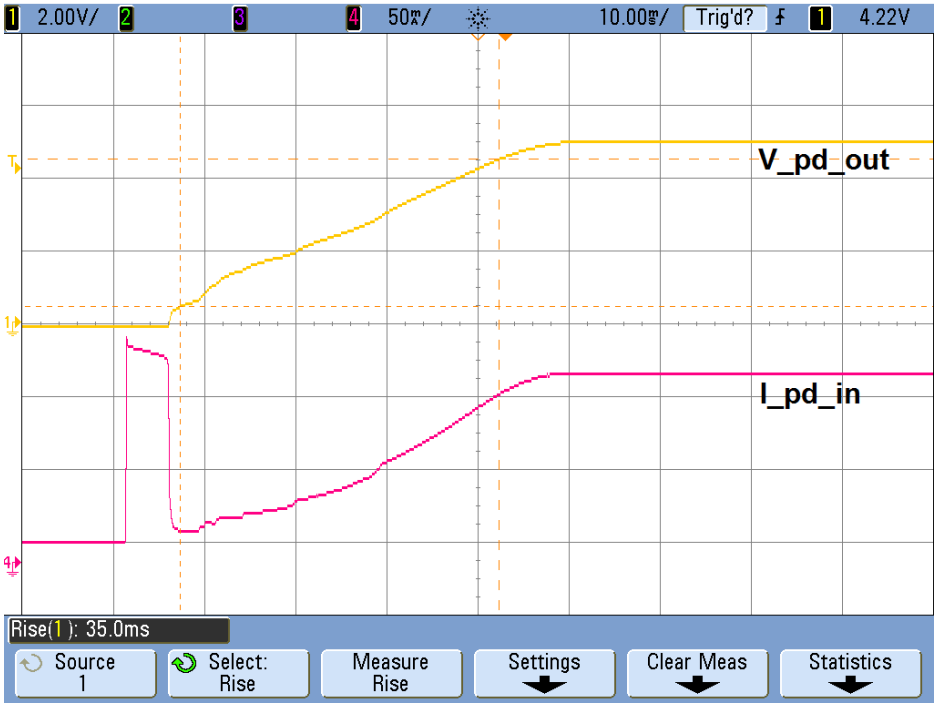


Figure 4.2. Typical Startup Waveform on the Buck-based EVB Board with a 10 Ω Load, Rise Time = 35 ms

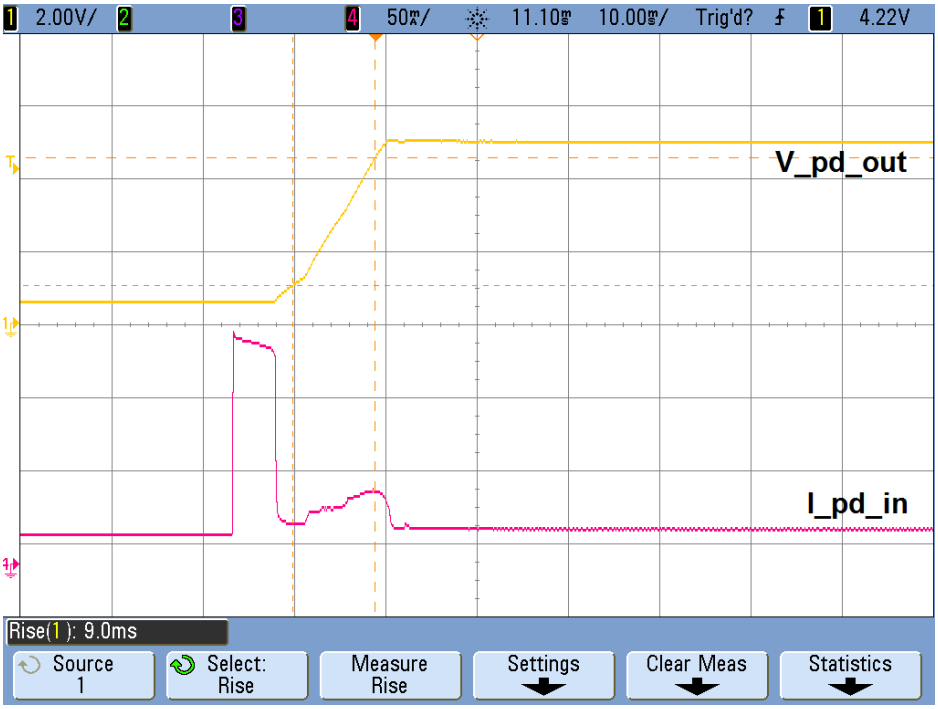


Figure 4.3. Typical Startup Waveform on the Buck-based EVB Board without Load-Rise Time = 9 ms

4.2 Isolated Flyback Design

For the isolated design, a flyback transformer approach is used. In a flyback transformer, the primary inductance is "charged" when the main switcher FET turns on, and the energy stored in this inductance is delivered to the secondary when the switcher FET turns off. This type of circuit may be designed to operate in either the continuous or discontinuous mode. In the continuous mode, current always flows in either the transformer primary or secondary. In the discontinuous mode, the secondary current drops to zero before the next cycle of primary current. Typical waveforms are shown below.

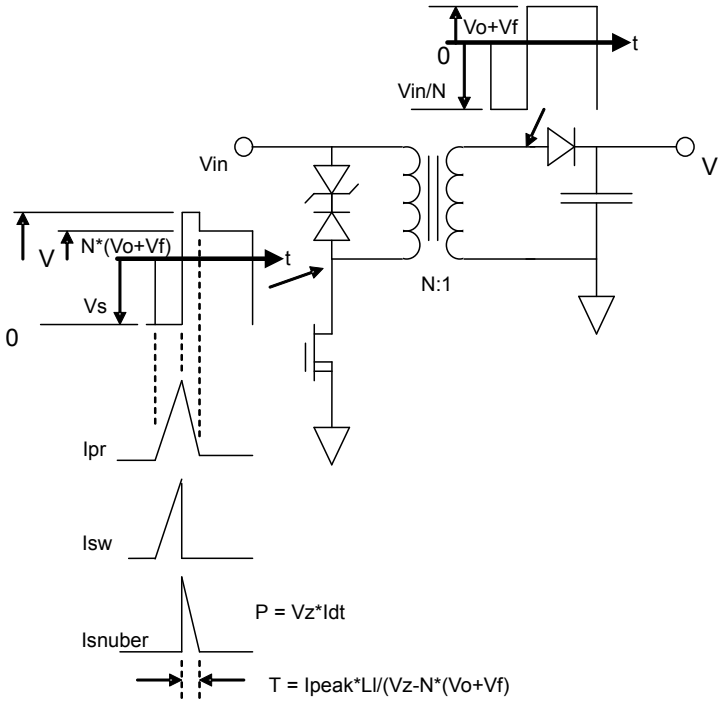


Figure 4.4. Typical Waveforms

A transformer with a turns ratio of N:1 is used to help reduce peak currents of the switcher.

In the discontinuous mode, the output power, I_0 x V_0, must be supplied by the ½ x LI^2 energy stored in the transformer with some margin for switching losses. If ϵ is the margin for switching losses (typically 90%), then:

$$P_0 = I_0 \times V_0 = \frac{1}{2} \times I_p^2 \times L_m \times f \times \varepsilon$$

Where P_0, I_0, and V_0 are output power, current and voltage, and I_p, L_m, and f are transformer primary peak current, magnetizing inductance, and operating frequency.

The portion of the switching waveform where the FET is on d_1 is:

$$d_1 = I_p \times L_m \times \frac{f}{V_p}$$

Where V_p is the input voltage.

The time, d_2, where current flows in the secondary is:

$$d_2 = V_p \times \frac{d1}{\left(N \times \left(V_0 + V_f\right)\right)}$$

Where V_o is the output voltage (plus diode drop), and N is the transformer turns ratio.

Solving with the constraint gives the following:

$$I_0 = \left[\varepsilon \times \frac{V_0 + V_f}{\left(2 \times f \times L_m\right)}\right] \times \left[\frac{N}{1 + N \times \frac{\left(V_0 + V_f\right)}{V_p}}\right]^2$$

For a given power transformer magnetizing inductance, turns ratio, output voltage, frequency, and input voltage, this gives the output current at which the current becomes continuous and always flows in either the transformer primary or secondary.

Lm = 40 µH gives a good compromise between transformer size (larger Lm gives a larger transformer) and peak current (larger Lm gives smaller peak current at the input and output).

Plugging in $V_0 + V_f = 5.7$ V, $V_p = 48$ V, N = 3, $L_m = 40$ µH, $\epsilon = 0.9$, and f = 350 kHz gives $I_0 = 0.85$ A.

Above this current, the transformer current becomes continuous in that there is always current flow in either the transformer primary or secondary.

For larger output current, the duty cycle stays fairly constant at:

$$D = N \times \frac{(V_0 + V_f)}{(V_p + N(V_0 + V_f))}$$

In the continuous mode, the average current while the switcher FET is on is determined by setting the average input power after an efficiency, ϵ, to equal the average output power:

$$I_{avg} \times V_p \times \varepsilon \times D = I_O \times (V_0 + V_f)$$

In this mode of operation, there is a change in primary current while the FET is on.

$$\Delta I = \frac{V_p \times D}{(L_m \times f)}$$

The peak current that the transformer must handle is:

$$I_{peak} = I_{avg} + \frac{\Delta I}{2}$$

For the same transformer above with $I_O = 3$ A, the peak transformer current is 1.85 A.

Increasing the turns ratio decreases peak current, particularly on the primary side. However, the secondary voltage is reflected back to the primary, and the increased turns ratio also increases the voltage on the switcher FET. Additionally, transformer leakage inductance causes an additional spike of voltage on the switcher FET, which must be clamped by a snubber.

The FET maximum drain voltage is 120 V, and the maximum voltage at Vpos is about 57 V; so, the snubber must clamp to 63 V.

A Zener diode and fast recovery diode are recommended to clamp the output at less than 40 V above VPOS to have around 20 V margin.

Increasing the turns ratio will increase dissipated power in the snubber. Therefore, there is an optimal turns ratio that compromises between high peak current at a low turns ratio and high snubber power dissipation at a high turns ratio.

Silicon Labs has partnered with Coilcraft to develop flyback transformers that are optimized for the Si3402-C at 3.3, 5, and 12 V output. The recommended part numbers are:

- FA2924-AL for 3.3 V and 5 V output voltages (40 µH and 1:0.3 turns ratio)
- FA2805-CL for 12 V output voltages (40 µH and 1:0.4 turns ratio)

Note: For the Si3402-C, follow the recommendation from this document, not from the Coilcraft data sheet. FA2805-CL can be used for 5 V output as it was recommended for the obsolete Si3402-A. For new designs with the Si3402-C, Silicon Labs recommends FA2924-AL for 5 V output for better efficiency and FA2805-CL for 12 V output voltages. Contact Silicon Labs for other output supply configurations and recommendations.

The rectifier for 3.3 or 5 V output does not need as high a voltage rating because the transformer turns ratio limits the reverse voltage to ((1/N) x Vin) + Vout. The PDS1040 from diodes incorporated or the equivalent UPS1040 from Microsemi can be used, and these parts have much lower forward drop and overall loss due to their lower voltage rating of 40 V. For 9 V and 12 V output voltages, the PS5100 is recommended.

4.2.1 Output Voltage—Isolated Design

In the isolated design, a TLV431 (U3 in Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5) is used as an isolated reference voltage. The TLV431 is available from many suppliers and regulates at a reference voltage of 1.24 V; so, the output voltage is:

VOUT = 1.24 x (1 + R5/R6)

An opto-isolator, such as VO618A (U2 in Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5), which is also available from many suppliers, is used to couple the error signal back to the Si3402-C.

4.2.2 Output Filter and Loop Stability—Isolated Design

In the flyback design, even if the transformer current always flows in the transformer primary or secondary (i.e. is continuous), the secondary current does not flow during the time that primary current flows; thus, there is always a large ripple current in the output that must be filtered. For the isolated design, it is recommended that a pi-section filter be used with a 1.0 µH inductor, such as Coilcraft D01608-102ML.

The feedback compensation for the isolated case was chosen to be Type 2 for improved load transient response.

A typical Bode plot is shown in the figure below, in the 5 V output, under worst-case (minimum Vin and max Iload) conditions for CCM operation.

By setting C21 = 15 nF, R12 = 0 Ω, and C9 = 3.3 nF, R8 = 0 Ω a high dc gain has been achieved with unity gain frequency at around 3.3 kHz. 60° of phase margin and ~17 dB of gain margin results stable output voltage with good transient response. Figure 4.6 Step Load Transient from 2.5 W to 10 W on page 18 and Figure 4.7 Step Load Transient from 10 W to 2.5 W on page 18 show the transient response of the converter, where the output starts with light load (discontinuous case) and ends with a heavy load (continuous case). Further optimization of this result is possible with larger or lower ESR output filter capacitors.

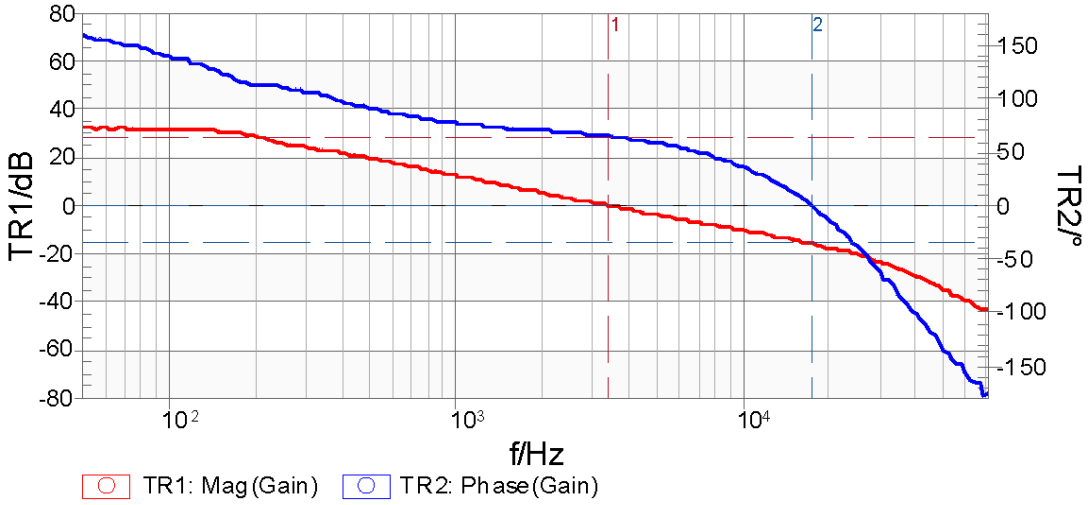


Figure 4.5. Bode Plots for Minimum Input Voltage, and Maximum Output Current (Blue = Phase; Red = Gain)

Notice that measurement by breaking the loop with the injection signal will give the phase margin directly, without having to measure it from –180 °. That is because the measurement test setup includes an extra inversion that was not part of Bode's original theory for loop gains.

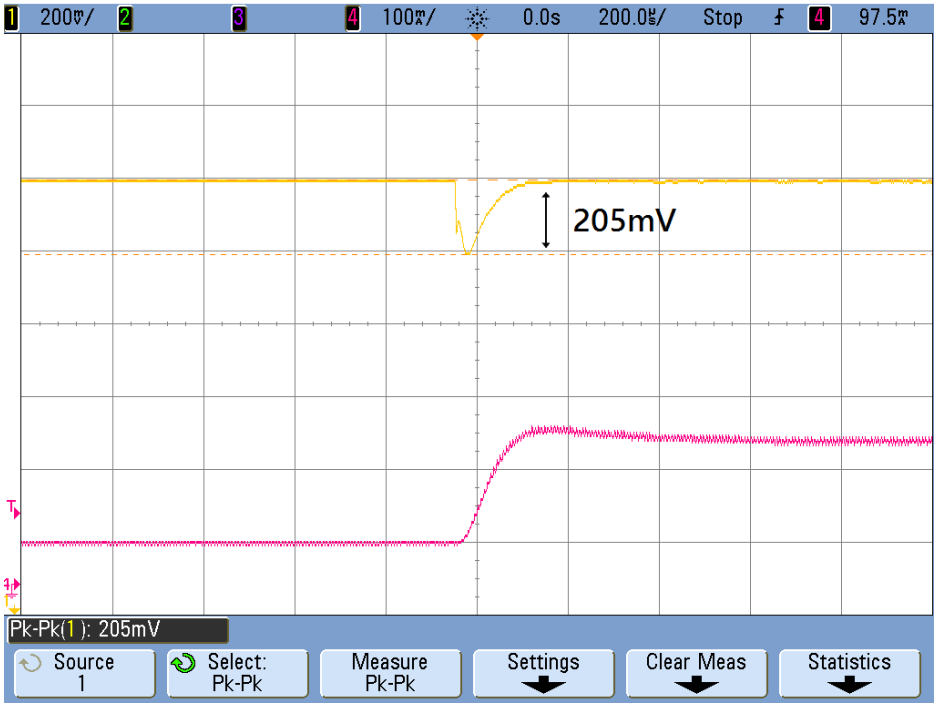


Figure 4.6. Step Load Transient from 2.5 W to 10 W

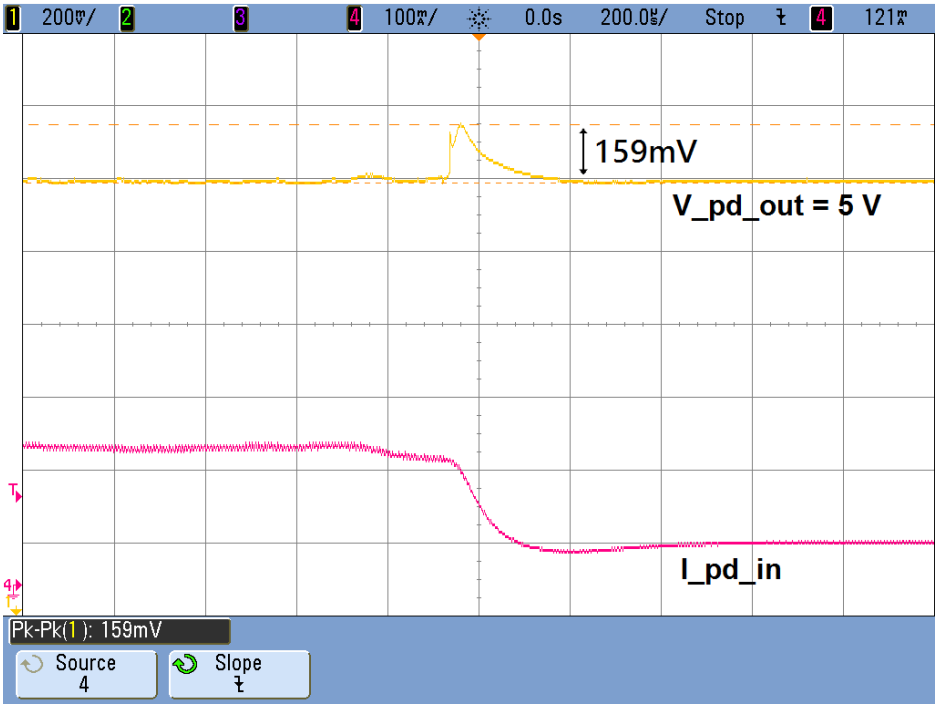


Figure 4.7. Step Load Transient from 10 W to 2.5 W

4.2.3 Soft Start Isolated Case

The Si3402-C employs a dynamic soft-start described in 4.1.3 Soft Start Non-Isolated Case.

5. General Guidelines for Selecting Output Filter Capacitor

5.1 Non-Isolated Buck Case Output Capacitor Selection

In the non-isolated Buck case, the peak-to-peak ripple current is generally low enough that a single electrolytic capacitor can be used for the output filter with reasonable output ripple voltage.

Generally, the main selection factor for the output filter is load transient response.

The change in output voltage for a load step of I_step is:

$$\Delta V = \Delta I \times \left(ESR + \frac{K}{C_{out} \times B} \right)$$

Where ESR is the output capacitor ESR; Cout is the output capacitor value, and B is the loop bandwidth and experimentally, K ~ 0.3.

Higher values of Cout and lower values of ESR generally result in lower loop bandwidth. As discussed in 4.1.2 Output Filter and Loop Stability—Non-Isolated Design, it has been found that, due to the stabilizing effects of the switch and rectifier resistance, even ultra-low ESR capacitors do not exhibit large peaking in the feedback loop. For this reason, lower ESR capacitors and higher values of capacitance always give better load transient response despite the reduced bandwidth.

Standard designs from Silicon Laboratories, Inc. have been optimized for a load transient response of about 10% to full load or full load to 10% load. For optimal load transient response, the low ESR designs are recommended.

In general, it can be expected that, for low ESR designs, the load transient response is dominated by:

$$\Delta V = I\_step \times \left(\frac{K}{C_{out} \times B} \right)$$

and the bandwidth is decreased as the square root of capacitance; so:

$$\Delta V \quad \Delta I \times \frac{1}{\sqrt{Cout}}$$

When varying the output capacitor, it is important to optimize and verify the loop stability.

5.2 Isolated Flyback Case Output Capacitor Selection

For the isolated case, the output ripple current is much larger, and a pi section filter is used.

The first capacitor is used to reduce most of the ripple. Generally, very low ESR ceramic capacitors are used in the first section of the filter because of their small size and excellent ripple handling capability. One 1210 capacitor in parallel is generally adequate.

A small inductor of about 1 µH is used in the pi filter to avoid saturation and to avoid inductive resonance with the output filter capacitor.

The final capacitor for the pi filter is chosen based on load transient response.

As with the non-isolated case, the change in output voltage for a load step of ΔI is:

$$\Delta V = \Delta I \times \left(ESR + \frac{K}{Cout \times B} \right)$$

Where:

ESR is the output capacitor ESR

Cout is the final output capacitor value

B is the loop bandwidth

Experimentally, K ~ 0.3

Higher values of Cout and lower values of ESR generally result in lower loop bandwidth.

Standard designs from Silicon Laboratories, Inc. have been optimized for a load transient response of about 10% to full load or full load to 10% load. For optimal load transient response, the low ESR designs are recommended.

In general, it can be expected that, for low ESR designs, the load transient response is dominated by:

$$\Delta V = \Delta I \times \left(\frac{K}{Cout \times B} \right)$$

and the bandwidth is decreased as the square root of capacitance; so:

$$\Delta V = \Delta I \times \left(\frac{1}{\sqrt{Cout}} \right)$$

When varying the output capacitor, it is important to optimize and verify the loop stability.

5.3 Steady State Failure Rate

The MTBF (Mean Time Between Failure) value is a quantitative measure of component reliability. The output capacitor determines overall loop stability, output voltage ripple, and, more importantly, load transient response.

The life of aluminum electrolytic capacitors is very dependent on environmental and electrical factors. Environmental factors include temperature, humidity, atmospheric pressure, and vibration. Electrical factors include operating voltage, ripple current, and charge-discharge duty cycle. Among these factors, temperature (ambient temperature and internal heating due to ripple current) is most critical to the life of aluminum electrolytic capacitors, whereas conditions, such as vibration, shock, and humidity, have little affect on the actual life of the capacitor. The electrolytic capacitors are evaluated by accelerated life tests. The acceleration tests contain three factors: temperature, voltage, and ripple current, which are shown in the following equation:

$$L_B = L_A \times L_T \times A_V \times A_R$$

Where:

L_B = Lifetime under a certain condition, "B"

L_A = Lifetime under a certain condition, "A"

A_T = Temperature acceleration factor

A_V = Voltage acceleration factor

A_R = Ripple current acceleration factor

In case of Si3402-C-based flyback designs, the output filter stage typically consists of a two-stage LC filter or a simple Pi filter. In both these cases, the capacitor close to the output rectifier diode should have the lowest ESR and be able to absorb most of the ac current ripple. The second-stage capacitor is meant to have high capacitance in order to give good transient response; therefore, ESR does not become a critical factor. The location of the second-stage capacitor is also not critical and can be moved away from heat dissipating components. In most of the designs, the first-stage capacitor is a ceramic capacitor with very low ESR, and the second-stage capacitor is aluminum electrolytic with high capacitance. Generally, the temperature acceleration factor (AT) is between 1.7 and 2.3.

Voltage within the allowed operating range has little effect on the actual life expectancy of a capacitor. However, in certain applications (or misapplications), the applied voltage can be detrimental to the life of an aluminum electrolytic capacitor. When capacitors are used at or below their rated voltage, the acceleration factor (AV) is equal to 1.

Finally, compared with other types of capacitors, aluminum electrolytic capacitors have a higher dissipation factor Tan Delta and, therefore, are subject to greater internal heat generation when ripple currents are present. To assure the capacitor's life, the maximum permissible ripple current of the product is specified.

When ripple current flows through the capacitor, heat is generated by the power dissipated in the capacitor, and temperature increases. Internal heating produced by ripple currents can be represented by the following equation:

$$W = I_R^2 \times R_{ESR} + V \times I_L \quad \ldots(1)$$

Where:

W = Internal power loss

I_R = Ripple current

R_{ESR} = Internal resistance (Equivalent Series Resistance)

V = Applied voltage

I_L = Leakage current

The ripple current multiplier (A_R) dependency on the frequency is attached here.

Table 5.1. Typical Values for Working Voltage ≤ 100

Nominal Capacitance (µF)	Frequency (Hz)					
	50/60	100/120	300	1K	10K	50K
4.7 or below	0.65	1.00	1.35	1.75	2.30	2.50
10 to 47	0.75	1.00	1.25	1.50	1.75	1.80
100 to 1,000	0.80	1.00	1.15	1.30	1.40	1.50

For Si3402-C based designs, the aluminum electrolytic capacitor is normally operated at a voltage much lower than its rating, and it does not absorb much of the ripple current.

The output filter capacitor value for a given output voltage and the converter configuration must be close to the value specified in the Si3402-C-EVB and Si3402-C-ISO-EVB users guide available on the Silicon Laboratories, Inc. web site:

http://www.silabs.com/products/power/poe/Pages/PoweredDevices.aspx

For users who would like to use the Si3402-C dc-dc converter as an add-in module to a system that has its own input capacitance, the total output capacitance of the Si3402-C dc-dc converter, including the input capacitance of the system, should not exceed the specified value.

6. Internal High-Voltage Protection

The Si3402-C has an input clamp that will protect it against surges as described in IEEE 802.3.

IEEE 802.3 specifies a 1000 V surge with 0.3 µsec rise time and 50 µsec fall time applied to each conductor through a series resistance of 402 Ω. Because this pulse is generally applied to all conductors, the differential current at the input is generally very limited.

The Si3402-C is designed to handle a 50 µsec, 5 A pulse that would result from applying the surge to either both Tx or Rx pairs and grounding the other pair. This is accomplished by turning on the hot swap switch while disabling the switcher if current flows in the input clamp. During the 50 µs transient, a large portion of the input energy is redirected to the switcher input capacitor. For this reason, a 15 µF minimum input capacitor is recommended.

The Si3402-C is also required to survive the application of telephony ringing voltage. IEEE 802.3 specifies 56 V dc + 175 V peak ringing applied through 400 Ω source impedance at a frequency of 20 to 60 Hz. In this case, when the voltage reaches 100 V, the telephony switch turns ON, protecting the controller.

Continuous application of such a large ringing signal will damage the Si3402-C (although it will not cause a safety hazard). However, such a large ringing signal should also cause a "ring trip" or apparent off-hook indication at the central office within 200 msec. It has been found that the Si3402-C can withstand application of telephony ringing for over one second before damage occurs; so, in general, telephony ringing will not cause damage.

In some applications, up to 16 kV of system-level ESD immunity is required. The standard Si3402-C EVB designs meet this requirement when the input is not powered. However, when the input is powered and the Si3402-C is producing an output through the dc-dc converter, damage may occur to the input diode bridges for ESD events above 4 kV when applied to the output terminals if C10 to C17 are not used. Capacitors C10 to C17 allow passing system-level ESD events in excess of 16 kV.

For isolated applications that require a high level of system-level ESD immunity, the capacitors are recommended. For non-isolated applications, it is generally not possible for an ESD event (at the output supply) to occur because the output terminals of the dc-dc converter are generally not accessible while input power is applied. However, even for non-isolated designs, there is a possibility that large ESD events may reach the power supply terminals, in which case these capacitors (C10 to C17) are also recommended.

7. Use with an Auxiliary Power Supply

In some applications, it is desirable to be able to use either the power from the RJ45 Power over Ethernet or from a low-cost auxiliary power supply. This is very easy to do with the Si3402-C, and a 48 V auxiliary supply is shown below.

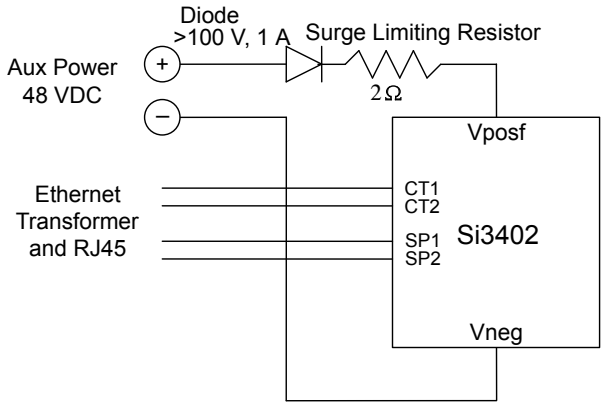


Figure 7.1. 48 V Auxiliary Supply

The auxiliary power source must supply between 41 and 56 V and at least 15 W for Class 0 or 3 equipment (less if the equipment is Class 1 or 2). It must also have output that is isolated from earth ground. To prevent damage from hot insertion suddenly charging the 0.1 µF input capacitor, a 2 Ω surge limiting resistor in series with the auxiliary power supply is recommended.

This provides a very simple and inexpensive means of providing auxiliary power. The diode bridges in the Si3402-C ensure that no power is fed back to the PSE.

The auxiliary power source always provides the power if it is plugged in first because the PSE will not successfully complete the detection and classification cycle. If the PSE is plugged in first, the auxiliary power or the auxiliary power source could provide the power, whichever has the greater output voltage. If the auxiliary power source provides the power, the PSE will generally sense a disconnect.

It is also possible to use a lower-voltage auxiliary power source, such as 12 V by diode OR at the output of the switching converter, as shown in the following figure.

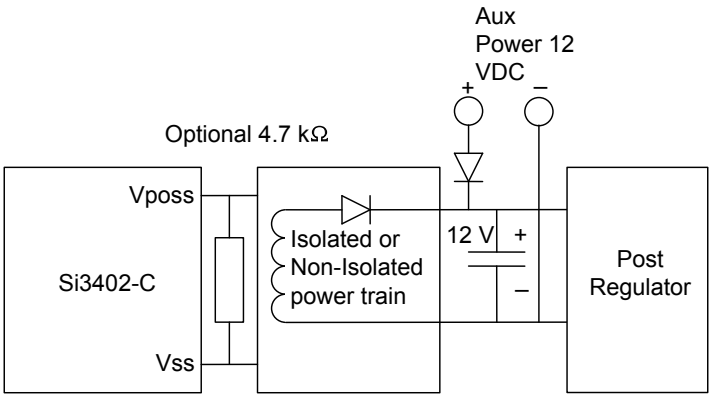


Figure 7.2. 12 V Auxiliary Supply

This option may be preferable when a post regulator is required for generation of very low voltages, such as 1.8 V, or when a post regulator is required for low noise.

With the post regulator option, the larger output voltage will again supply the power. In this case, the Si3402-C attempts to go through the detection and classification cycle, but, if the AUX supply is providing the power, the Si3402-C will not draw enough dc current, and the PSE may disconnect and cycle continuously. To prevent this, it is possible to add a 4.7 kΩ, 1 W resistor from VPOSF to VSS of the Si3402-C to ensure >10 mA power drain from the PSE. If this resistor is added, the PSE will always have >10 mA power drain and will stay connected even if the auxiliary power source is providing the load current.

8. Use with a Legacy PoE Injector

PoE injectors turn ON the connected PD without detection and classification phases. The PoE voltage is being forced to the PD input. In most cases, dV/dt is not controlled and could violate IEEE requirements.

At the moment of turning ON the PD, PoE injectors can generate high-voltage spikes that could damage the Si3402-C. The best way to protect the IC from such spikes is to add some series resistance to the input.

In the internal diode bridge case, install 2 Ω series resistors on all four input lines (CT/SP), in series with the ferrite beads.

In the external diode bridge case, install one 3 Ω resistor between the external bridge and the C18 capacitor.

The added series resistor and C18 form a low-pass filter.

9. Layout, EMI, and EMC Considerations

Refer to the files located at www.silabs.com/PoE under the documentation page for examples of recommended PCB layouts in the evaluation board user's guides. To avoid potential performance issues, Silicon Labs strongly recommends adherence to the layouts shown in these designs. In general, four-layer PCB designs yield the most robust design, as shown in the evaluation board user's guides. Two-layer PCB designs must be carefully considered. Silicon Labs strongly recommends that all two-layer PCB designs be reviewed before fabrication.

Submit PCB schematics and layout files to PoEinfo@silabs.com for feedback and recommendations on these designs.

9.1 Thermal Considerations

The thermal pad of the Si3402-C must be connected to a heat spreader. Generally, a 2-inch^2 bottom plane connected to the thermal pad of the Si3402-C and electrically connected to Vneg is recommended. While the heat spreader generally is not a circuit ground, it is a good reference plane for the Si3402-C and is also useful as a shield layer for EMI reduction.

With the 2 in^2 thermal plane on an outer layer, the thermal impedance of the Si3402-C was measured at 44 °C/W. As an added data point, 54 °C/W was measured with a 1-inch^2 plane on an inner layer.

Due to heating of the ambient air from the Schottky diode etc., the effective thermal impedance can be considerably higher than this. It is not unusual for the Si3402-C junction temperature to rise 70 °C. The Si3402-C is rated up to a junction temperature of 140 °C, with thermal shutdown to 160 °C typical. If such a high junction temperature is a concern, it can be reduced by bypassing the on-chip diode bridges.

9.2 Voltage Considerations

Since the Si3402-C is not exposed to dc voltages over 60 V dc, it is generally considered to be a safety-extra-low-voltage (SELV) circuit, and there are no particular spacing requirements other than those of high-yield board manufacture.

9.3 Current Considerations

Pins CT1, CT2, SP1, SP2, HSO, and V_{POSF} carry up to 325 mA dc. 12 mil traces have been found to be adequate. Pins SWO and VSS carry current spikes of up to several amps, although the dc current is no more than 325 mA, and 25 mil traces are used for these pins. Output current can be up to 3 A depending on output voltage, and 50 mil traces are recommended in the output section.

9.4 Minimum Load Considerations

To ensure that the PD is not disconnected by the PSE in a "no load" situation, Silicon Labs recommends that a load $\geq$250 mW be present. See 3.6 Maintain Power Signature (MPS) for more information.

9.5 EMI and EMC Considerations

As with any switching converter, care taken in overall circuit design and layout is necessary to meet the stringent requirements for EMI (i.e., CISPR 22 Class B in the 30 MHz to 1 GHz band) and EMC (i.e., EN55022 in the 150 kHz to 30 MHz band). While the comments in this section apply to both the isolated Flyback approach and non-isolated topologies, the Flyback topology is the most challenging and, therefore, the focus of the discussion.

To prevent radiated emissions, care must be taken to keep the circuit nodes with high ac voltages very short and to keep the current loops carrying high ac current of a very small diameter. Referring to Figure 2.2 Isolated Flyback Configuration for Si3402-C-ISO-EVB (5 V Output) on page 5, the circuit nodes with high voltage swing are as follows:

- The node connecting SWO (Si3402 pin 18) and the transformer primary.
- The node connecting the transformer secondary to the anode of D2.

These circuit nodes should be kept extremely short to minimize EMI. While the current flowing is fairly high (about 1 A on the primary side and 3 A on the secondary side), trace width should be limited to about 25 mils to cut down on radiation. While it is possible to reduce radiation by routing these nodes on an inner layer, in practice, it should be possible to arrange the layout so that these two nodes are sufficiently short that there is little advantage to be gained by this. An R-C snubber across the transformer primary or across the output rectifier can reduce dV/dt and thus radiation. In practice, it has been found that the secondary side snubber is quite effective, but the primary side snubber is not helpful in this regard due to the high current peak associated with switcher FET turn-on in the case of the primary side snubber.

The loops carrying high ac current are as follows:

- The loop from the input filter, C1–C4, to the transformer returning from the transformer to SWO, then to VSS and back to the input filter capacitors
- The loop from the transformer secondary to D3, the filter capacitor C6, and returning to the transformer secondary
- The loop associated with the primary side snubber and transformer

These loops should be kept small in diameter to avoid EMI. An effective way of doing this is to route the return for the loop underneath the source for the loop as much as possible, effectively shrinking the loop diameter to almost zero. Ferrite beads L2–L5 are primarily for conducted emissions reduction, although they have been found to improve radiated emissions as well. Using these methods, the test results shown below have been obtained for EMI.

The figure below shows the isolated EVB test result for EN55022 Class B radiated EMI measurement.

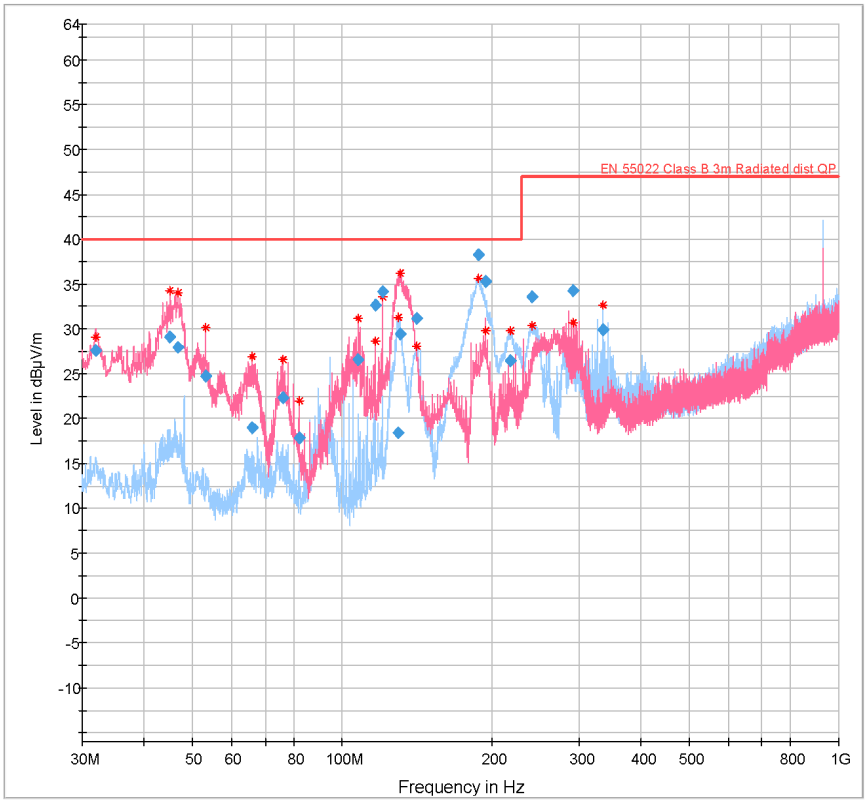


Figure 9.1. Si3402-C Graph of Radiated EMI Measurements at 5 V Output Voltage and 12.5 W Output Power

Lab testing of conducted emissions has shown that if the power output is not referenced to earth ground (as is the case in many applications), conducted emissions are not a problem because there are no path-induced common-mode disturbances on the loop. However, it has been found that if the output has an earth ground reference, common-mode current can be quite high at lower frequencies.

The following figure is the measured conducted emissions result. For the grounded-output case, a common-mode choke or non-interleaved transformer technique is required to reduce the conducted emissions.

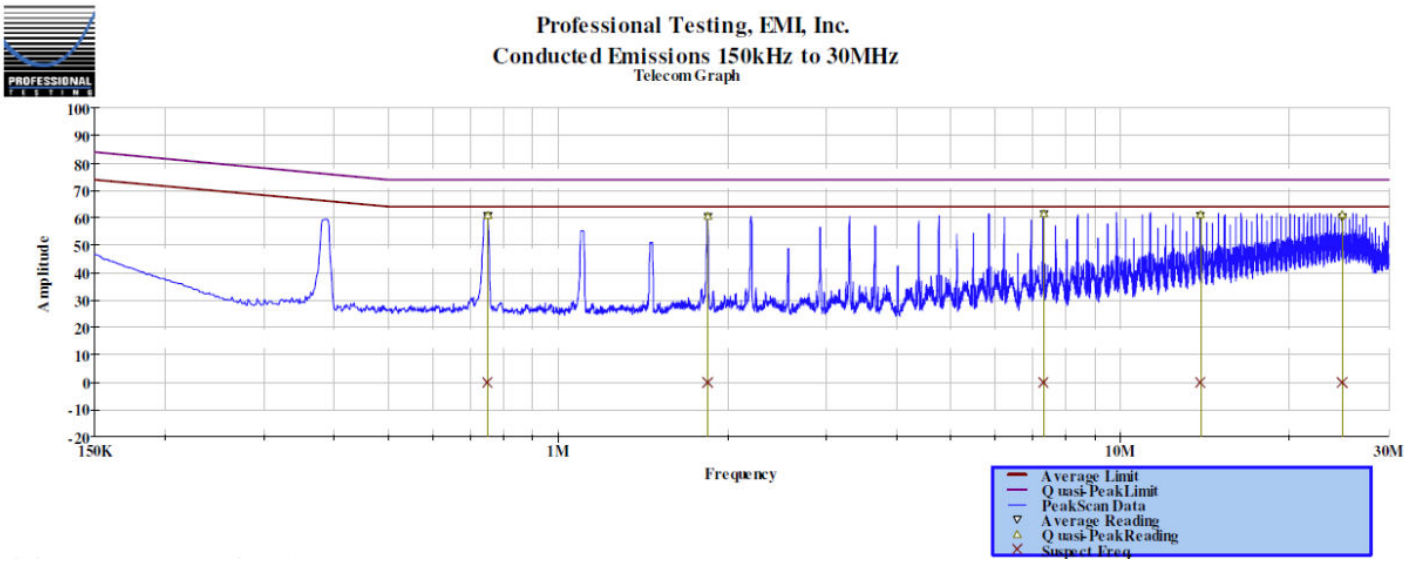
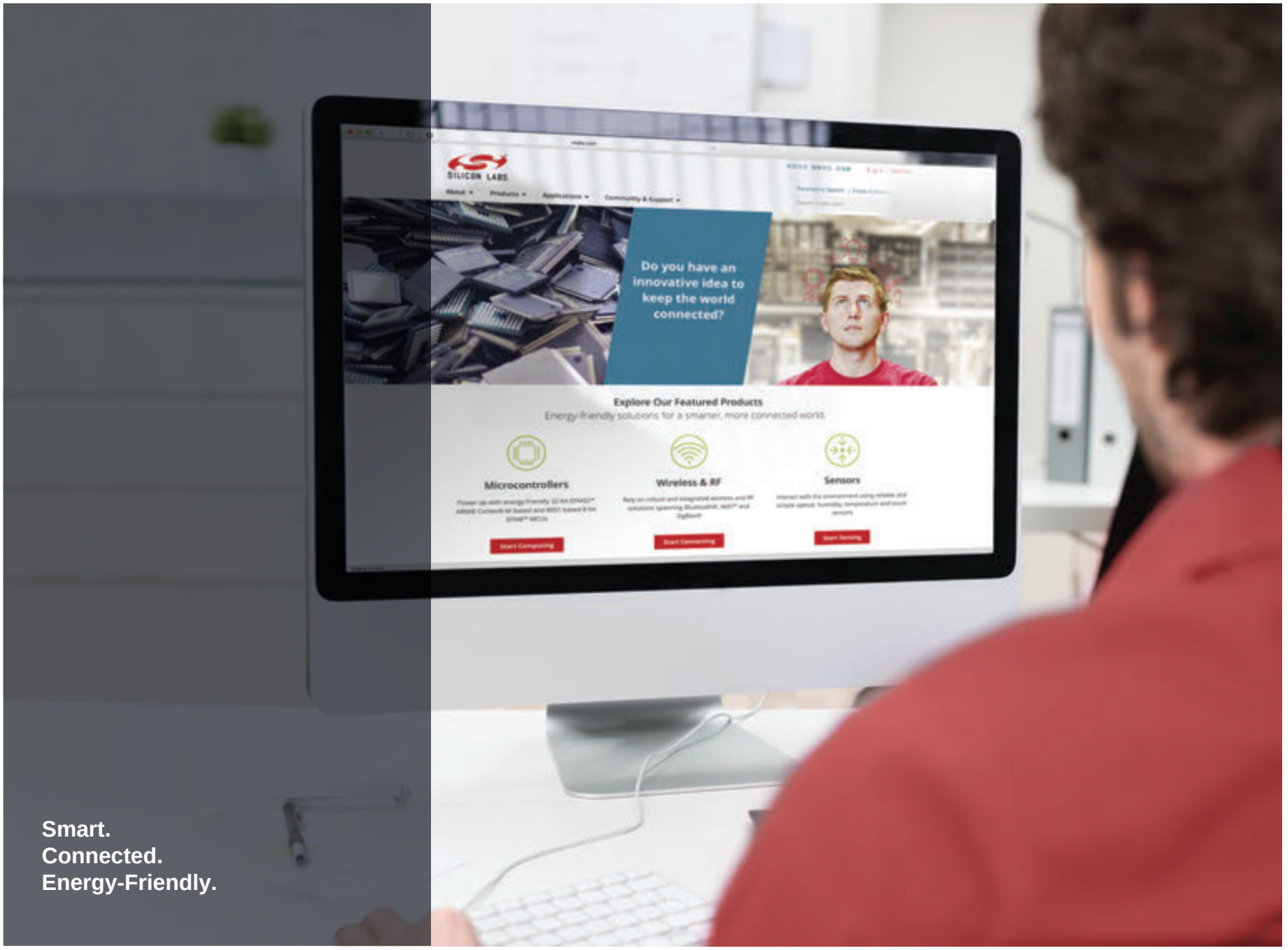


Figure 9.2. Si3402-C Measured Conducted Emissions Results

10. Conclusion

This application note has covered the basic operation and design equations for the Si3402-C, allowing the design of highly-integrated and efficient PDs for PoE applications.

As mentioned earlier, reference designs are available at www.silabs.com/PoE to assist in the easy design-in process for the Si3402-C. The evaluation boards and reference designs are documented separately and include example layouts and bill-of-materials lists.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com