J1 — USB3_A

Pin	Signal
VBUS	1
D−	2
D+	3
SSRX−	5 LV1−ATN
SSRX+	6 LV2−DAT
SSTX−	8 LV4−CLK
SSTX+	9 LV5−SRQ

SHIELD
DRAIN
GND
10
7
4

VBUS

J4 — SRQ−LV

GND
LV3−RST

U2 — LDO

Pin	Signal
1	VIN
2	VOUT
3	GND

+3V3 VBUS

GND

C1 4.7uF / J3 — Barrel_Jack

VBUS

| 1 | |
| 2 | |

GND

U1 — 4-Channel_LevelShifter

LV	HV
LV1−ATN 7 LV1	HV1 6 HV1−ATN
LV2−DAT 8 LV2	HV2 5 HV2−DAT
9 LV	HV 4
10 GND	GND 3
LV3−RST 11 LV3	HV3 2 HV3−RST
LV4−CLK 12 LV4	HV4 1 HV4−CLK

+3V3   VBUS

GND   GND

J2 — DIN−6

HV3−RST 6
HV2−DAT 5
HV4−CLK 4
HV1−ATN
14 3 15 2 1 HV5−SRQ

J5 — SRQ−HV

GND

Pins
1: SRQ , C64 unused, C128 Fast Serial Clock IN/OUT
2: GND
3: ATN OUT
4: CLK IN/OUT
5: DATA IN/OUT
6: RESET OUT(IN)
See https://www.c64-wiki.com/wiki/Serial_Port

H1 M3   H2 M3
H3 M3   H4 M3

Notes:
a) Add U1&U2 but not R1,R2,R3,R4 if you connect the Adapter directly to the MiSTer FPGA SNAC Port.
b) Add R1,R2,R3,R4 (0R,SMD 0805) but not U1&U2 if you connect the Adapter using a SNAC Port Level
   Shifter Adapter to the MiSTer FPGA SNAC Port.
c) Add C1 (4.7uF,SMD 0805) if you draw more than 500ma on J3 or the power cable is longer than 20cm.
d) For SRQ usage (C128), solder LV,HV,GND and one Channel for LV5/HV5 onto a "stacked" Level−Shifter.

Converts the MiSTer FPGA SNAC Port into a Commodore IEC/CBM (Serial) Bus Port.

Sheet: /
File: SNAC2IEC_Breakout.kicad_sch
Title: SNAC2IEC
Size: A4 | Date: 2023−02−27 | **Rev: v1.2**
KiCad E.D.A. kicad (6.0.11) | Id: 1/1