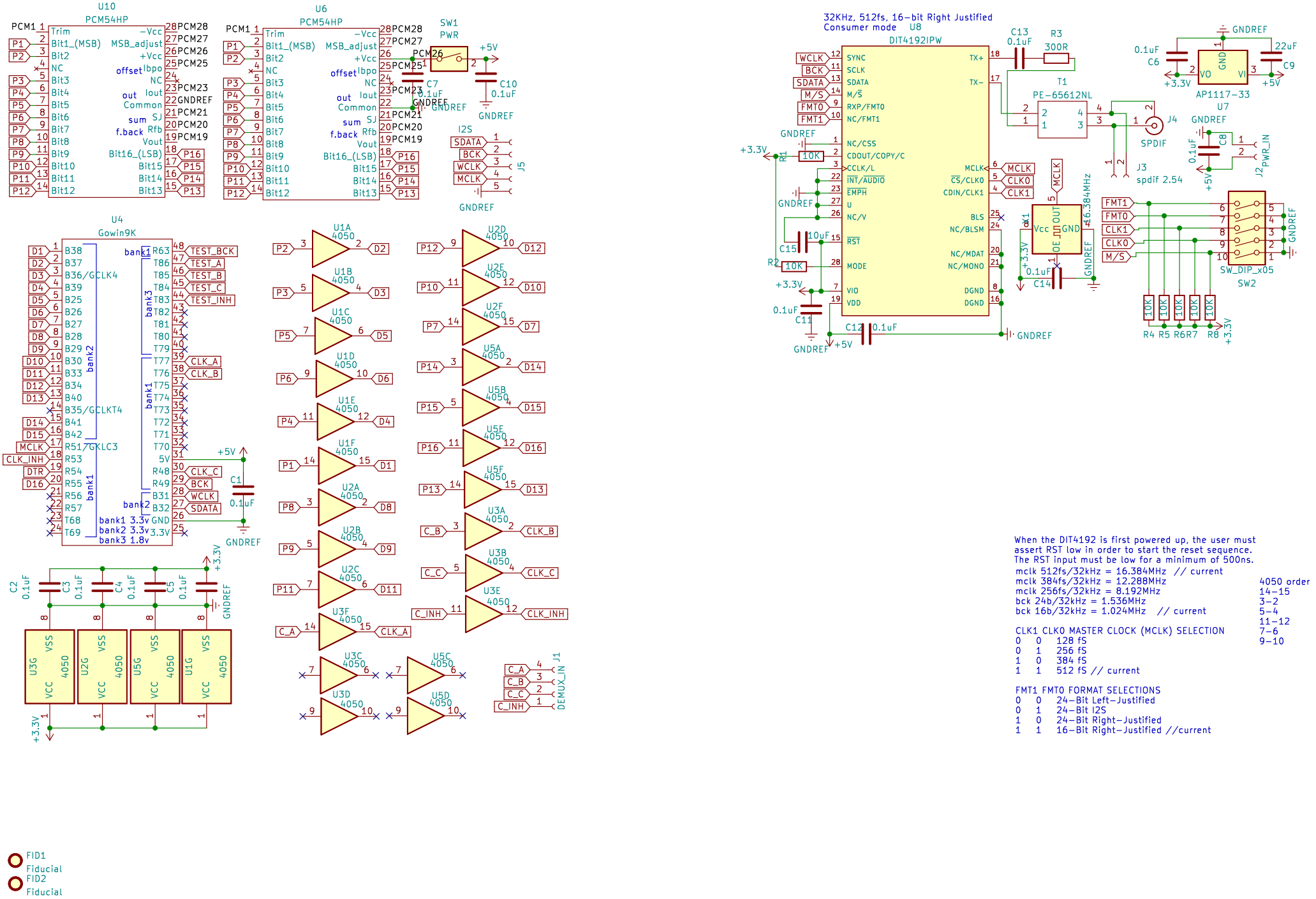


When the DIT4192 is first powered up, the user must assert RST low in order to start the reset sequence. The RST input must be low for a minimum of 500ns.

mclk 512fs/32kHz = 16.384MHz // current
mclk 384fs/32kHz = 12.288MHz
mclk 256fs/32kHz = 8.192MHz
bck 24b/32kHz = 1.536MHz
bck 16b/32kHz = 1.024MHz // current

| CLK1 | CLK0 | MASTER CLOCK (MCLK) SELECTION |
|---|---|---|
| 0 | 0 | 128 fS |
| 0 | 1 | 256 fS |
| 1 | 0 | 384 fS |
| 1 | 1 | 512 fS // current |

| FMT1 | FMT0 | FORMAT SELECTIONS |
|---|---|---|
| 0 | 0 | 24-Bit Left-Justified |
| 0 | 1 | 24-Bit I2S |
| 1 | 0 | 24-Bit Right-Justified |
| 1 | 1 | 16-Bit Right-Justified //current |

| 4050 order |
|---|
| 14-15 |
| 3-2 |
| 5-4 |
| 11-12 |
| 7-6 |
| 9-10 |