

DIGITAL DESIGN AND COMPUTER ORGANIZATION

Latches, Flip-flops - 1

Reetinder Sidhu

Department of Computer Science and Engineering



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Course Outline



- Digital Design
 - Combinational logic design
 - Sequential logic design
 - ★ Latches, Flip-flops 1
- Computer Organization
 - Architecture (microprocessor instruction set)
 - Microarchitecure (microprocessor operation)

Concepts covered

- Memory Elements
- SR Latch

How does Sequential Logic differ from Combinational Logic?



- Sequential logic circuits contain logic elements that can "remember"
 - Such a logic circuit, called a memory or storage element, remembers one or more bits of data which forms the state of the logic circuit
- Recall that combinational logic circuits implement Boolean functions
 - Functions cannot "remember" (output is a function of inputs)
- Also recall that in combinational logic circuits, an output of a logic circuit cannot be connected back to one of its inputs
 - Can breaking above restriction yield storage elements?

LATCHES, FLIP-FLOPS - 1 How to Implement Memory?



- The inverter is essentially the simplest logic gate
- What happens when we connect its output to input, forming a loop?



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• Inverter loop is thus not in a stable state

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Inverter loop is thus not in a stable state

• How about a loop of two inverters?



 Two inverter loop can be in one of two stable states

How to Implement Memory?



- The inverter is essentially the simplest logic gate
- What happens when we connect its output to input, forming a loop?



Inverter loop is thus not in a stable state



- Two inverter loop can be in one of two stable states
- A bit can have one of two different values

How to Implement Memory?



- The inverter is essentially the simplest logic gate
- What happens when we connect its output to input, forming a loop?



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- Two inverter loop can be in one of two stable states
- A bit can have one of two different values
- Thus a two inverter loop can store ("remember") a single bit

How to Implement Memory?



- The inverter is essentially the simplest logic gate
- What happens when we connect its output to input, forming a loop?



Inverter loop is thus not in a stable state



- Two inverter loop can be in one of two stable states
- A bit can have one of two different values
- Thus a two inverter loop can store ("remember") a single bit
- But how to change the bit stored / stable state?





SR Latch



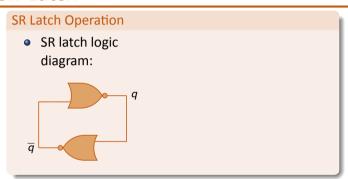
SR Latch Operation

SR latch logic diagram:

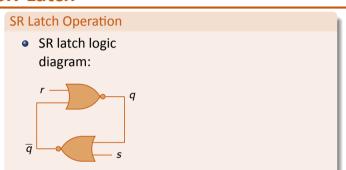




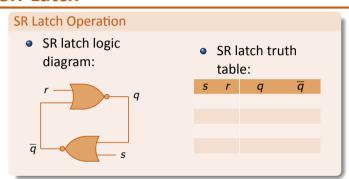




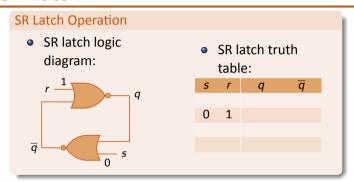




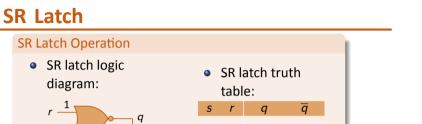








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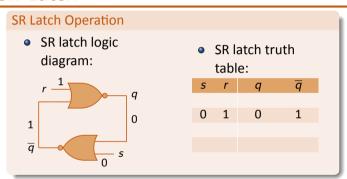


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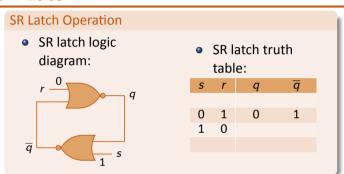




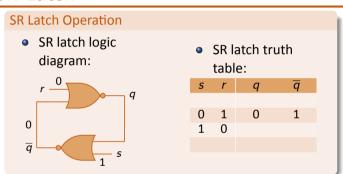




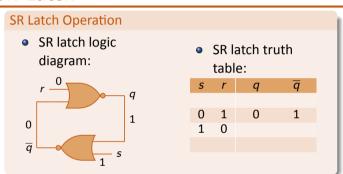




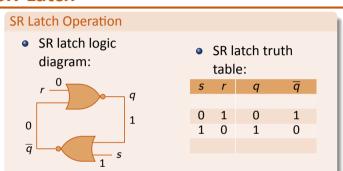










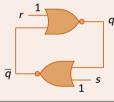


SR Latch



SR Latch Operation

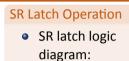
SR latch logic diagram:

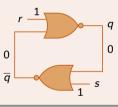


5	r	q	\overline{q}
0	1	0	1
1	0	1	0
1	1		

SR Latch



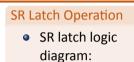


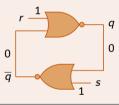


5	r	q	\overline{q}
0	1	0	1
1	0	1	0
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SR Latch





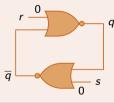


S	r	q	\overline{q}
0	1	0	1
1	0	1	0
1	1	0	0

SR Latch



SR latch logic diagram:



0 0 0 1 0 1 1 0 1 0	S	r	q	\overline{q}
1 0 1 0	0	0		
	0	1	0	1
1 1 0 0	1	0	1	0
1 1 0 0	1	1	0	0

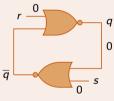


SR Latch



SR Latch Operation

SR latch logic diagram:



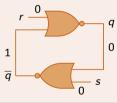
S	r	q	\overline{q}
0	0		
0	1	0	1
1	0	1	0
1	1	0	0

SR Latch



SR Latch Operation

SR latch logic diagram:



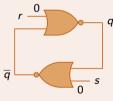
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0	0		
0	1	0	1
1	0	1	0
1	1	0	0

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SR Latch Operation

SR latch logic diagram:



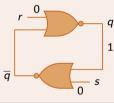
S	r	q	\overline{q}
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0	1	0	1
1	0	1	0
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SR Latch



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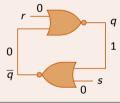
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0	1	0	1
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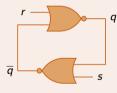


S	r	q	\overline{q}
0	0		
0	1	0	1
1	0	1	0
1	1	0	0

SR Latch

SR Latch Operation

• SR latch logic diagram:



5	r	q	\overline{q}
0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	1
1	0	1	0
1	1	0	0

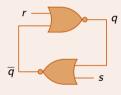


SR Latch

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SR Latch Operation

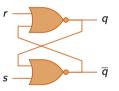
SR latch logic diagram:



SR latch truth table:

$egin{array}{cccccccccccccccccccccccccccccccccccc$	
0 1 0 1	_ v
1 0 1 0	
1 1 0 0	

SR latch conventional logic diagram:

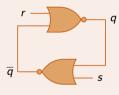


SR Latch



SR Latch Operation

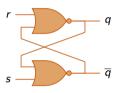
SR latch logic diagram:



SR latch truth table:

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1	1	0	0

SR latch conventional logic diagram:



SR latch symbol:

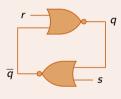


SR Latch



SR Latch Operation

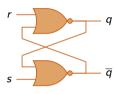
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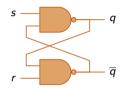


- In this manner a single bit (0 or 1) can be stored in an SR latch
 - ▶ Bit stored when r = 0, s = 1 or r = 1, s = 0
 - ▶ Bit remembered when r = 0, s = 0

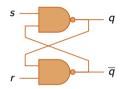


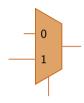




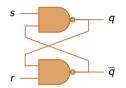


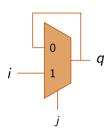






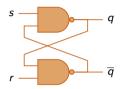


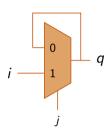




Think About It







Write the truth tables for the above logic circuits