Digital Design and Computer Organization

Memory Arrays - 1

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
    - ★ **Memory Arrays - 1**
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Demultiplexers (demuxes)

Memory Arrays - 1
2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

2:1 Mux

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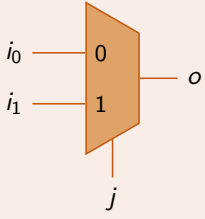

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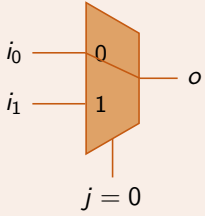

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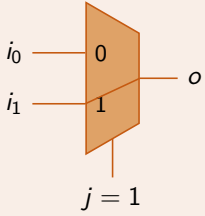

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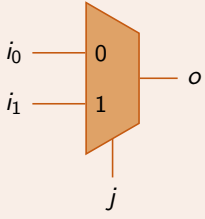

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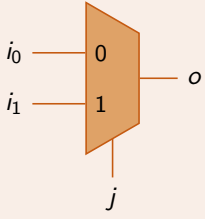

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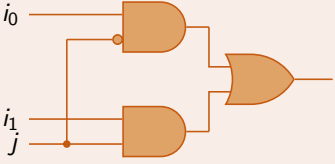
- 2:1 mux logic circuit:



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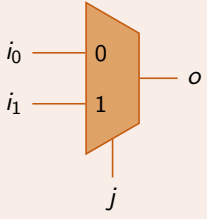

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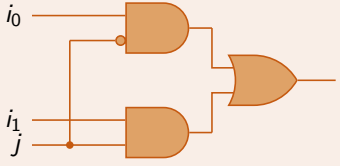

- 2:1 mux truth table:

i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
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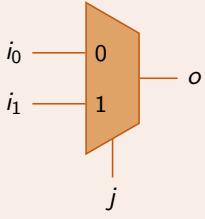

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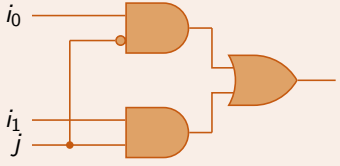

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1	1	0	1
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- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

Memory Arrays - 1
1:2 Demultiplexer

- A demultiplexer (also called a demux) *demultiplexes* single input onto a many outputs

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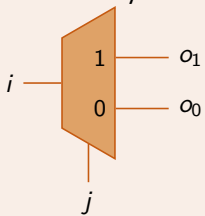

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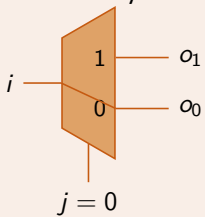

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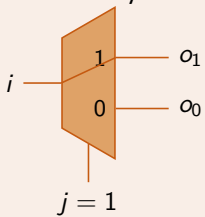

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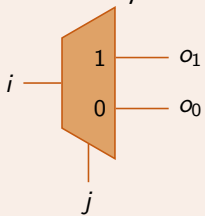

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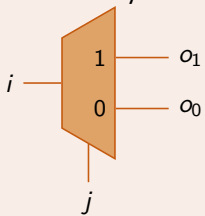

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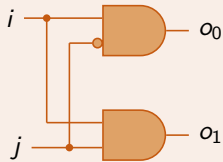
- 1:2 mux logic circuit:



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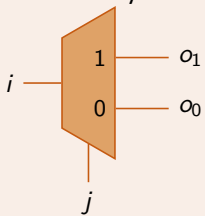

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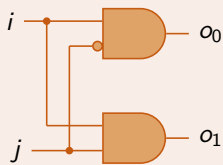

- 2:1 mux truth table:

i	j	o_0	o_1
0	0	0	0
0	1	0	0
1	0	1	0
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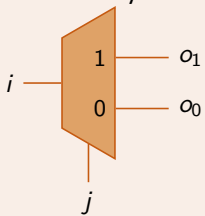

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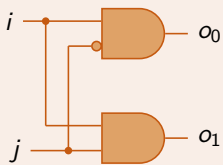

- 2:1 mux truth table:

i	j	o_0	o_1
0	0	0	0
0	1	0	0
1	0	1	0
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- 2:1 mux Boolean formula:

$o_0 = \bar{j}\, i$

$o_1 = j\, i$

Memory Arrays - 1
1:4 Demultiplexer

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1:4 demux

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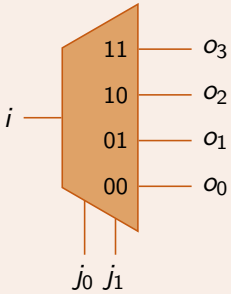
1:4 Demultiplexer

1:4 demux

- 1:4 demux symbol:

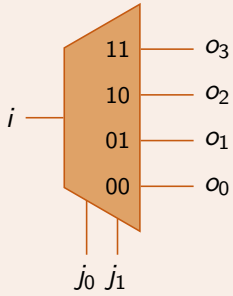


- Data outputs: o_0, o_1, o_2, o_3
- Control inputs: j_0, j_1

Memory Arrays - 1
1:4 Demultiplexer

1:4 demux

- 1:4 demux symbol:

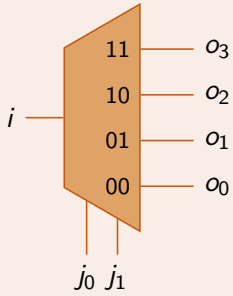


- Data outputs: o_0, o_1, o_2, o_3
- Control inputs: j_0, j_1
- 1:4 demux Boolean formulas:
  $o_0 = \overline{j_1}\,\overline{j_0}\,i$
  $o_1 = \overline{j_1}\,j_0\,i$
  $o_2 = j_1\,\overline{j_0}\,i$
  $o_3 = j_1\,j_0\,i$

Memory Arrays - 1
1:4 Demultiplexer

1:4 demux

- 1:4 demux symbol:



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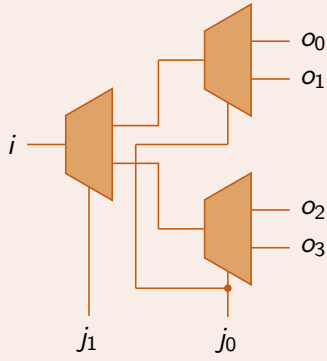
- 1:4 demux logic circuit using 2:1 muxes:



Memory Arrays - 1

1:n Demultiplexer

Memory Arrays - 1
1:n Demultiplexer

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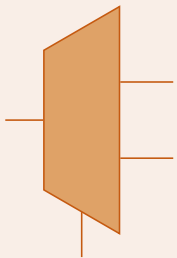
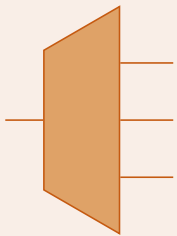
1:2 Demux



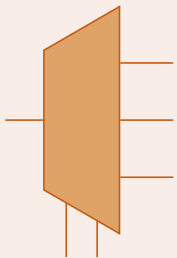
Memory Arrays - 1
1:n Demultiplexer

1:3 Demux



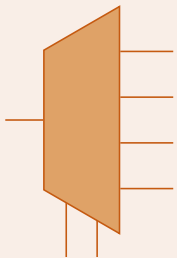
Memory Arrays - 1
1:n Demultiplexer

1:3 Demux



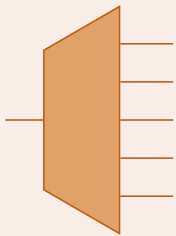
Memory Arrays - 1
1:n Demultiplexer

1:4 Demux



Memory Arrays - 1
1:n Demultiplexer

1:5 Demux



Memory Arrays - 1
1:n Demultiplexer

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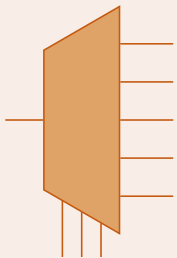
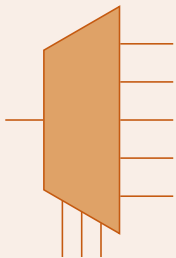
1:5 Demux



Memory Arrays - 1
1:n Demultiplexer

1:5 Demux



$1 : n$ Demux

A combinational logic circuit having one data input, $\lceil \log_2 n \rceil$ control inputs and n outputs, that connects the data input to the output indicated by the control inputs

Memory Arrays - 1

Think About It

- What is the Boolean formula for a 1:5 demux?
- Construct a 1:5 demux using
  - 1:2 demuxes
  - AND, OR and NOT gates