QUESTIONS UNIT 3

1. Why is a refresh cycle necessary for a dynamic RAM?

2. List and explain which technique extends the storage capacities of main memory beyond the actual size of the main memory.

3. Explain how the L2 cache memory structure gives an advantage of reduction in delay to access RAM on the motherboard?

4. Give the reason why for a memory system, the cycle time is longer than the access time.

5. Consider the situation for a k-way set associative cache which is divided into v sets. Each set consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. Describe the procedure how the main memory block numbered j is mapped to cache lines.

6. Explain why the difference between processor and memory speeds is a major obstacle towards achieving good performance.

7. Explain the need for a mapping function which can determine which blocks in the main memory are in the cache.

8. Explain the process to identify whether a given block is present in the cache or not?

9. Elaborate on how block replacement algorithms are essential to determine which block should be replaced on a cache miss?

10. Explain why for a direct mapped cache, the miss rate may go up due to possible increase of mapping conflicts?