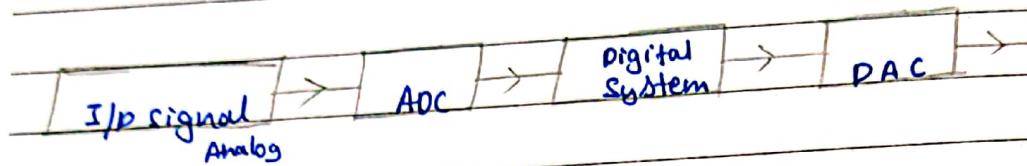
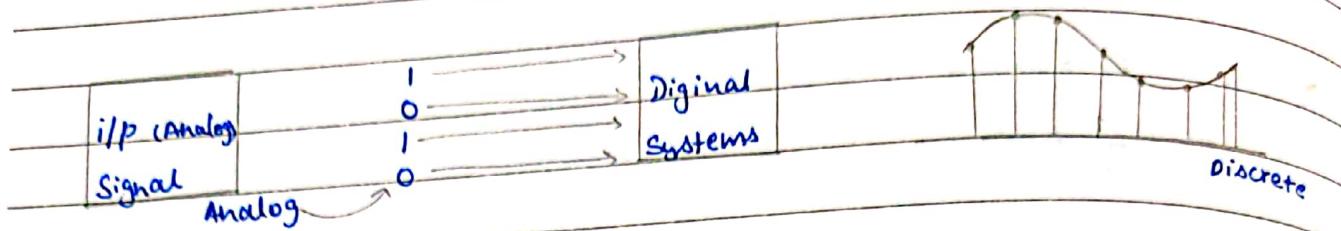


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## Unit-5

### Digital Electronics



1 → High voltage / on 15V

0 → Low voltage / off 0V

### Boolean Algebra

$$1) A + 1 = 1$$

AND  $A \cdot B$

$$2) A + 0 = A$$

OR  $A + B$

$$3) A \cdot 1 = A$$

NOT  $\bar{A}$

$$4) A \cdot 0 = 0$$

$$5) A + A = A$$

$$6) A \cdot A = A$$

$$7) A + \bar{A} = 1$$

$$8) A \cdot \bar{A} = 0$$

$$9) A + \bar{A}B = A + B$$

### DeMorgan's Law

$$1) \overline{A + B} = \bar{A} \cdot \bar{B}$$

$$2) \overline{A \cdot B} = \bar{A} + \bar{B}$$

$$f(A, B) = \overline{A + B} = \bar{A} \cdot \bar{B}$$

$$= \bar{A} \cdot \bar{B} = \bar{A} + \bar{B}$$

### Verification of DeMorgan's Law

$$1) \overline{A + B} = \bar{A} \cdot \bar{B}$$

Verification through Truth Table

## Truth Table

A	B	$\bar{A}$	$\bar{B}$	$A+B$	$\bar{A}+\bar{B}$	$\bar{A}\cdot\bar{B}$	
0	0	1	1	0	1	1	
0	1	1	0	1	0	0	
1	0	0	1	1	0	0	
1	1	0	0	1	0	0	

2)  $\overline{A \cdot B} = \bar{A} + \bar{B}$

## Truth Table

A	B	$\bar{A}$	$\bar{B}$	$A \cdot B$	$\bar{A} \cdot \bar{B}$	$\bar{A} + \bar{B}$	
0	0	1	1	0	1	1	
0	1	1	0	0	1	1	
1	0	0	1	0	1	1	
1	1	0	0	1	0	0	

9)  $A + \bar{A} \cdot B = A + B$

## Truth Table

A	B	$\bar{A}$	$\bar{A} \cdot B$	$A + \bar{A} \cdot B$	$A + B$	
0	0	1	0	0	0	
0	1	1	1	1	1	
1	0	0	0	1	1	
1	1	0	0	1	1	

10)  $\bar{\bar{A}} = A \rightarrow$  Involutory law

11)  $A + AB = A \rightarrow$  Absorption law

12)  $(A+B)(A+C) = A + BC \rightarrow$  Distributive law

## Canonical / Standard form of Representation

$$f = A\bar{B} + \bar{C}$$

A	$A\bar{B} + \bar{C}$	$\rightarrow$
B		
C	D.S.	

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$$\begin{aligned}
 f &= A \cdot \bar{B} \cdot 1 + \bar{C} \cdot 1 \cdot 1 \\
 &= A \cdot \bar{B} \cdot (C + \bar{C}) + \bar{C} \cdot (A + \bar{A}) \cdot (B + \bar{B}) \\
 &= A\bar{B}C + A\bar{B}\bar{C} + (A\bar{C} + \bar{C}\bar{A})(B + \bar{B}) \\
 &= A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} \\
 &= A\bar{B}C + 2A\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} \\
 f &= A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} = \text{SOP (Sum of Product)}
 \end{aligned}$$

Truth Table

A	B	C	$\bar{B}$	$\bar{C}$	$A\bar{B}$	$A\bar{B} + \bar{C}$	
0	0	0	1	1	0	1	$= A\bar{B}\bar{C}$
0	0	1	1	0	0	0	
0	1	0	0	1	0	1	$= \bar{A}B\bar{C}$
0	1	1	0	0	0	0	
1	0	0	1	1	1	1	$= A\bar{B}\bar{C}$
1	0	1	1	0	1	1	$= A\bar{B}C$
1	1	0	0	1	0	1	$= AB\bar{C}$
1	1	1	0	0	0	0	

$$f(0, 2, 4, 5, 6) = \text{sop}$$

Q3D  $f = AR + AC$  . get SOP of  $f$  using Boolean Algebra & Truth Table

Solution

$$\begin{aligned}
 f &= A \cdot B \cdot 1 + A \cdot 1 \cdot C \\
 &= A \cdot B \cdot (C + \bar{C}) + A \cdot C \cdot (B + \bar{B}) \\
 &= ABC + A\bar{B}C + ABC + A\bar{B}C \\
 &= ABC + A\bar{B}C + A\bar{B}C
 \end{aligned}$$

A	B	C	AB	AC	$AB + AC$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

$$\begin{aligned}
 &= A\bar{B}C + A\bar{B}\bar{C} + ABC \\
 &= A\bar{B}C + A\bar{B}\bar{C} + ABC \\
 &= ABC
 \end{aligned}$$

## Logic Gates

AND



OR



NOT



Truth Table

x	y	xy
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table

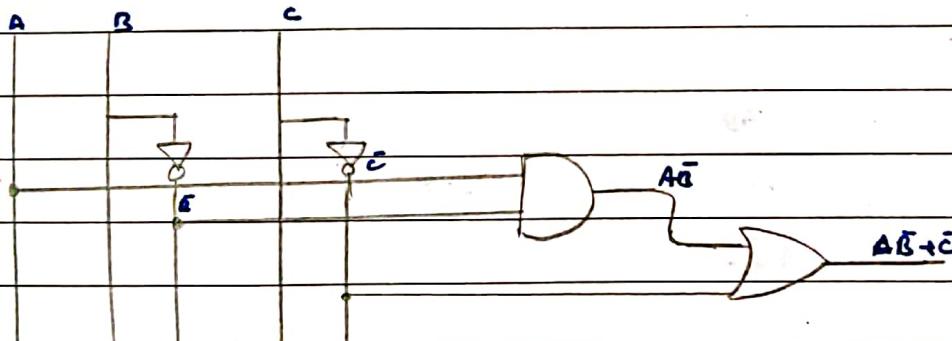
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table

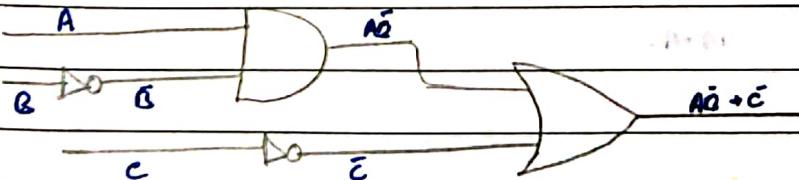
A	Ā
0	1
1	0

Realisation of expression using logic gates

$$f = A\bar{B} + \bar{C}$$



(OR)

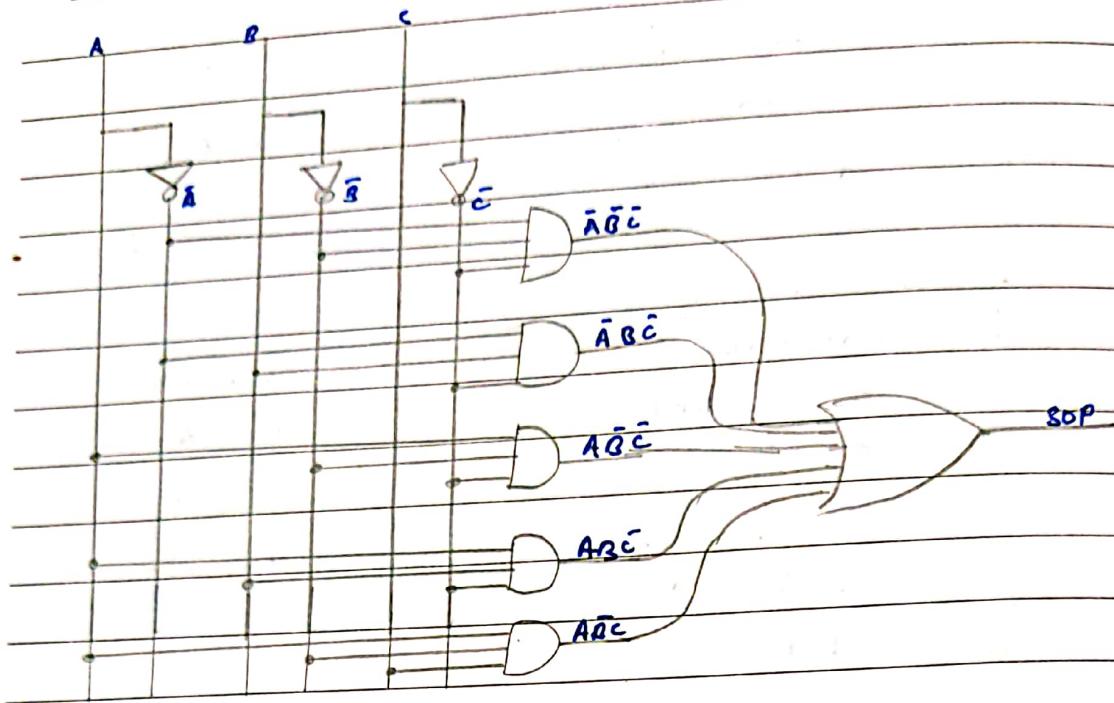


$$\text{SOP form } f = A\bar{B} + \bar{C} \text{ is}$$

$$\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + A\bar{B}C$$

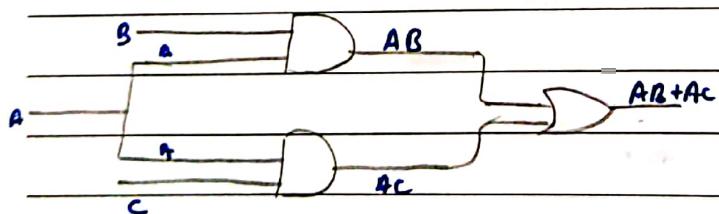
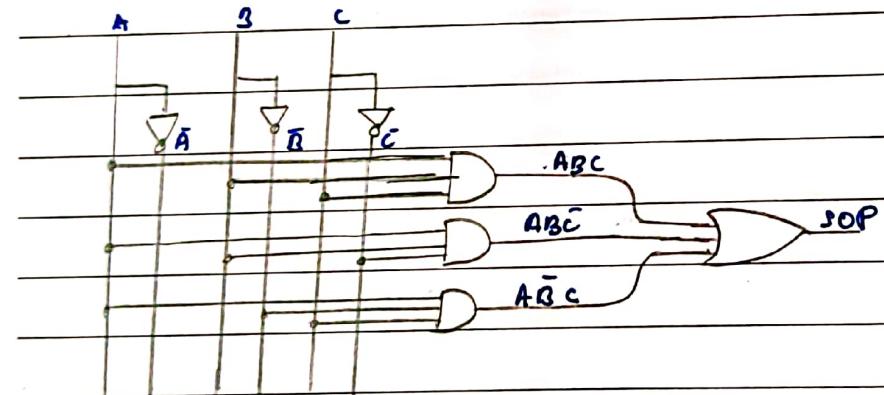
logic gate

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$$2) f = AB + AC$$

$$SOP: ABC + AB\bar{C} + A\bar{B}\bar{C}$$



- ③ Verify the function using truth table  $AB + \bar{A}C + AC = AB + \bar{A}C$ . Find the SOP for the given function. Realise the SOP and the simplified form using logic gate.

Solution

$$AB + \bar{A}C + AC = AB + \bar{A}C \text{ (Commutative Theorem)}$$

Truth Table

A	B	C	$\bar{A}$	AB	$\bar{A}C$	BC	$AB + \bar{A}C$	$AB + \bar{A}C + BC$
0	0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	1	1
0	1	0	1	0	0	0	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	1	0	0	1	1
1	1	1	0	1	0	1	1	1

From truth Table,

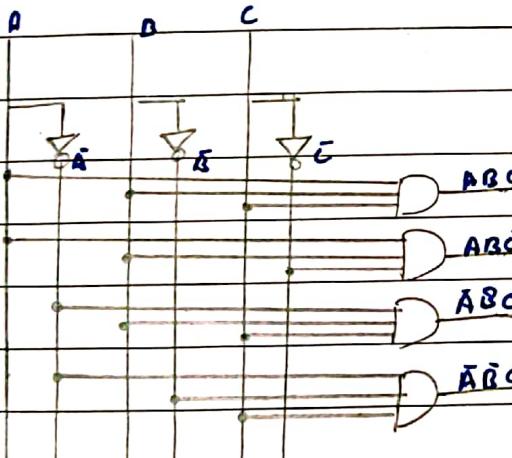
verified that  $AB + \bar{A}C + BC = AB + \bar{A}B$

$$f(1, 3, 6, 7)$$

$$SOP: f(\Sigma 1, 3, 6, 7)$$

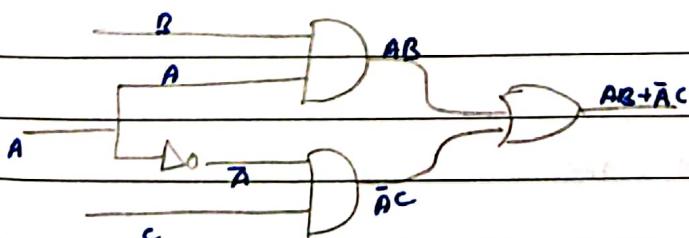
$$AB + \bar{A}C = AB(C + \bar{C}) + \bar{A}(B + \bar{B})C$$

$$= ABC + AB\bar{C} + \bar{A}BC + \bar{A}\bar{B}C$$



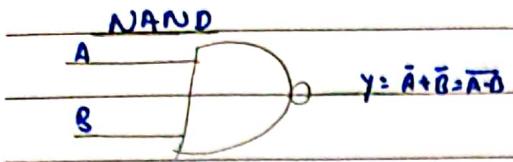
$$AB + AB\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C}$$

∴ SOP represents min terms. Each term in a SOP is known as a min term.



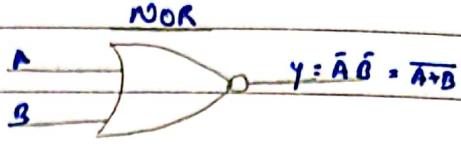
Universal Gates

The 2 universal gates are: NAND & NOR



Truth Table

X	Y	$\bar{A} \cdot \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0

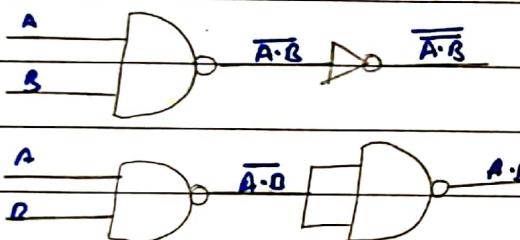


Truth Table

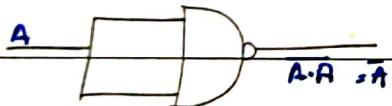
X	Y	$\bar{A} + \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0

- Realisation of basic gates using Universal gates.

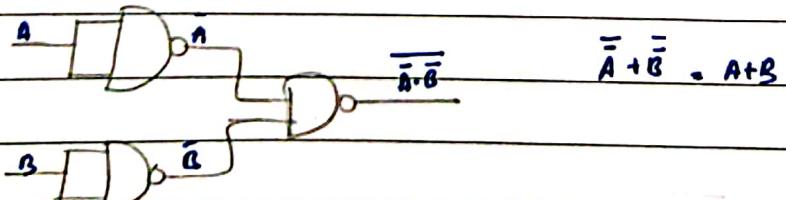
→ AND using NAND



→ NOT using NAND



→ OR using NAND



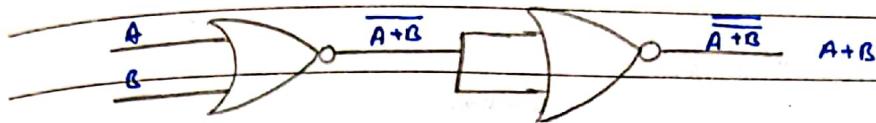
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• Realisation of basic gates using NOR gates.

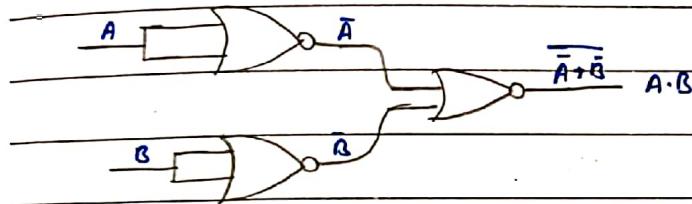
→ NOT using NOR



→ OR using NOR



→ AND using NOR



• Simplify the logical expression using boolean algebra realisize the same using NAND gate.

$$1. \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$\bar{A}BC + A\bar{B}C + AB(C + C)$$

$$\bar{A} + \bar{A} = 1$$

$$\bar{A}BC + A\bar{B}C + AB$$

$$A \cdot 1 = A$$

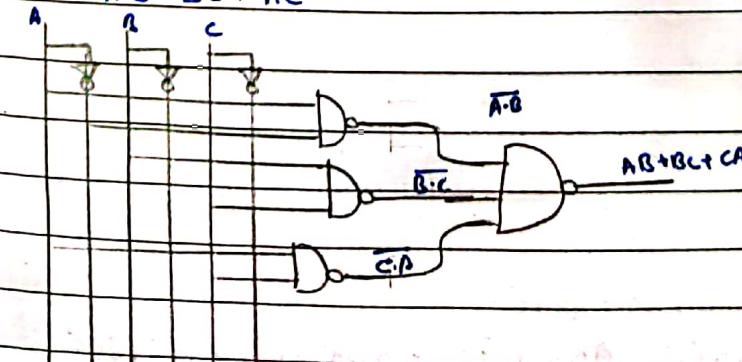
$$\bar{A}BC + A(\bar{B}C + B)$$

$$\bar{A}B + A = A + B$$

$$\bar{A}BC + AB + AC$$

$$A(\bar{A}C + A) + AC$$

$$AB + BC + AC$$



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NOTE: OR GATE  is equal to 

NAND GATE

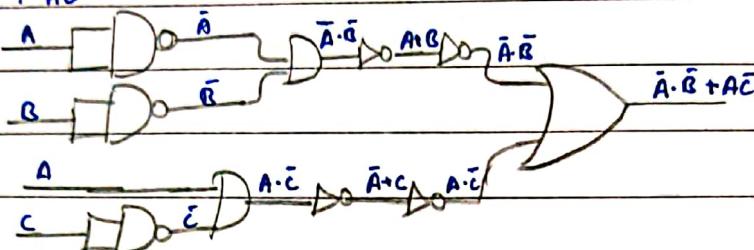
$$2. A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B} + A\bar{C}$$

$$(A\bar{C} + \bar{A})\bar{B} + \bar{C}(\bar{A}\bar{B} + A)$$

$$\bar{A}\bar{B} + \bar{B}\bar{C} + A\bar{C} + \bar{B}\bar{C}$$

$$\bar{A}\bar{B} + \bar{B}\bar{C} + A\bar{C}$$

$$\bar{A}\bar{B} + A\bar{C}$$



$$3. AB + \bar{A}C + A\bar{B}C(A\bar{B} + C)$$

$$AB + \bar{A}C + A\bar{B}C$$

$$AB + C(\bar{A} + A\bar{B})$$

$$AB + \bar{A}C + \bar{B}C$$

$$AB + AC + \bar{A}C$$

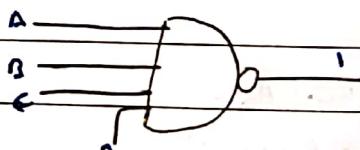
$$AB + C$$

$$4. AB + \bar{A}C + A\bar{B}C (AB + C)$$

$$AB + \bar{A} + \bar{C} + A\bar{B}C$$

$$A(B + \bar{B}C) + \bar{A} + \bar{C}$$

$$AB + AC + \bar{A} + \bar{C} = AB + \bar{B} + \bar{A} + \bar{C} = AB + \bar{A} + 1 = 1$$



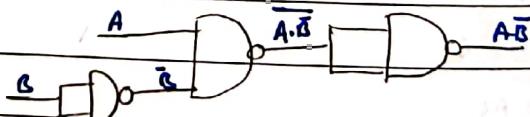
$$5. \bar{A}B + \bar{A} + AB$$

$$\bar{A}\bar{B} \cdot \bar{A} \cdot \bar{A}\bar{B} = (\bar{A} + \bar{B}) \cdot A \cdot (\bar{A} + \bar{B})$$

$$(\bar{A} + AB) \cdot (\bar{A} + \bar{B})$$

$$A \cdot 0 + 0 + A\bar{B} + A\bar{B}$$

$$A\bar{B}$$



$$6. (A + \bar{B} + C)(\bar{A} + B + \bar{C})(A + \bar{B})$$

$$(A\bar{A} + \bar{A}\bar{B} + \bar{A}C + AB + B\bar{B} + BC + A\bar{C} + \bar{B}\bar{C} + C\bar{C})(A + \bar{B})$$

$$A\bar{A} + \bar{A}\bar{A} + A\bar{C} + AB + B\bar{B} + BC + A\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{B} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{B} + B\bar{B} + A\bar{A}\bar{C} + \bar{B}\bar{B}\bar{C}$$

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$$AB + ABC + AC\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B} + A\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{B}\bar{C}$$

~~$$AB + ABC + AC\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{B}C + \bar{B}\bar{C}$$~~

~~$$AB + AC(1+\bar{B}) + A\bar{B}(1+C) + \bar{B}C$$~~

~~$$AB + AC\bar{C} + A\bar{B} + \bar{B}C$$~~

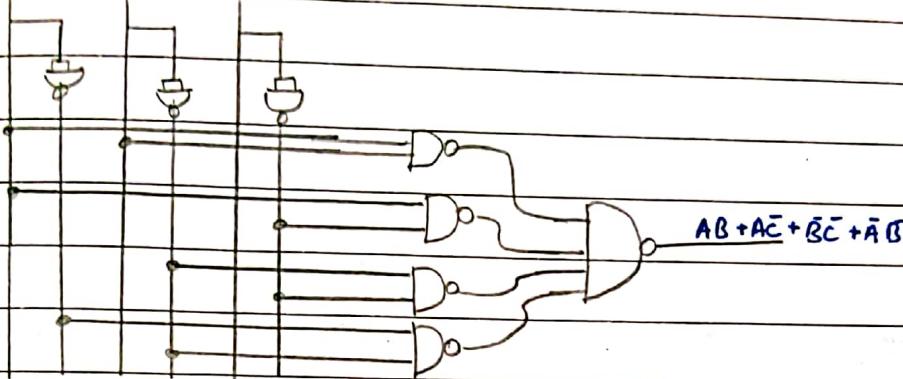
~~$$A + AC\bar{C} + \bar{B}C$$~~

~~$$AB + \bar{A}\bar{B} + AC\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}C$$~~

~~$$AB + \bar{A}\bar{B} + \bar{B}\bar{C} + AC$$~~

$$\Rightarrow AB + AC\bar{C} + \bar{B}\bar{C} + \bar{A}\bar{B}$$

A B C



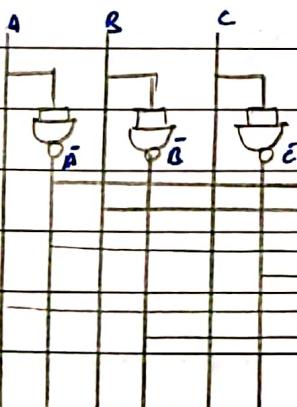
7.  $(A + \bar{B} + \bar{C})(A + \bar{B}C)(\bar{A} + B)$

$$(A + \bar{B}C) + (A + \bar{B} + \bar{C}) + (\bar{A} + B)$$

$$\bar{A}(B + \bar{C}) + (\bar{A}BC) + A\bar{B}$$

$$\bar{A}B + \bar{A}\bar{C} + \bar{A}BC + A\bar{B}$$

$$\bar{A}B + \bar{A}\bar{C} + A\bar{B}$$



8.  $(\bar{A} + \bar{B}C)(\bar{A} + \bar{B} + \bar{C})(\bar{A} + B)$

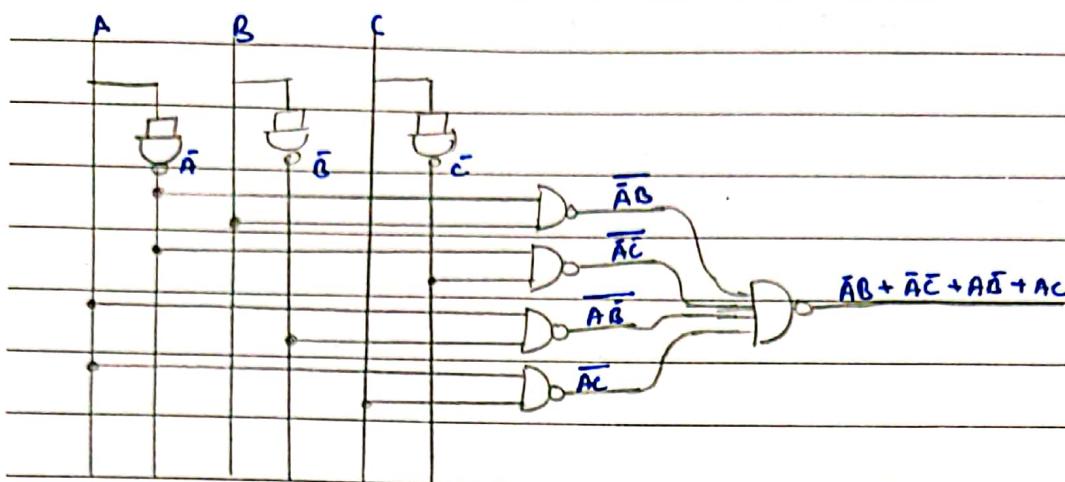
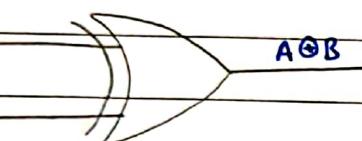
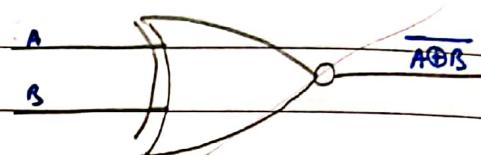
$$(\bar{A} + \bar{B}C) + (\bar{A} + \bar{B} + \bar{C}) + (\bar{A} + B)$$

$$\bar{A}(B + \bar{C}) + ABC + A\bar{B}$$

$$\bar{A}B + \bar{A}\bar{C} + ABC + A\bar{B}$$

$$\bar{A}B + \bar{A}\bar{C} + A(\bar{B} + BC)$$

$$\bar{A}B + \bar{A}\bar{C} + A\bar{B} + AC$$

XORXNORTruth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

$$A \oplus B = \bar{A}B + A\bar{B}$$

$$\overline{A \oplus B} = \bar{A}\bar{B} + A\bar{B}$$

Combinational Circuits

- Combinational circuits do not store any information/ do not have any memory.

Half Adder

$$\text{sum: } 0+0=0$$

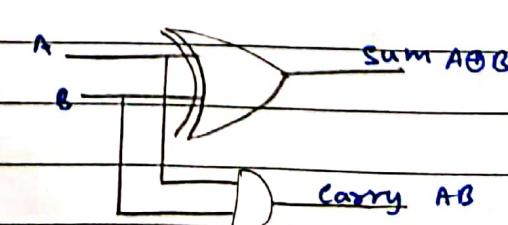
$$0+1=1$$

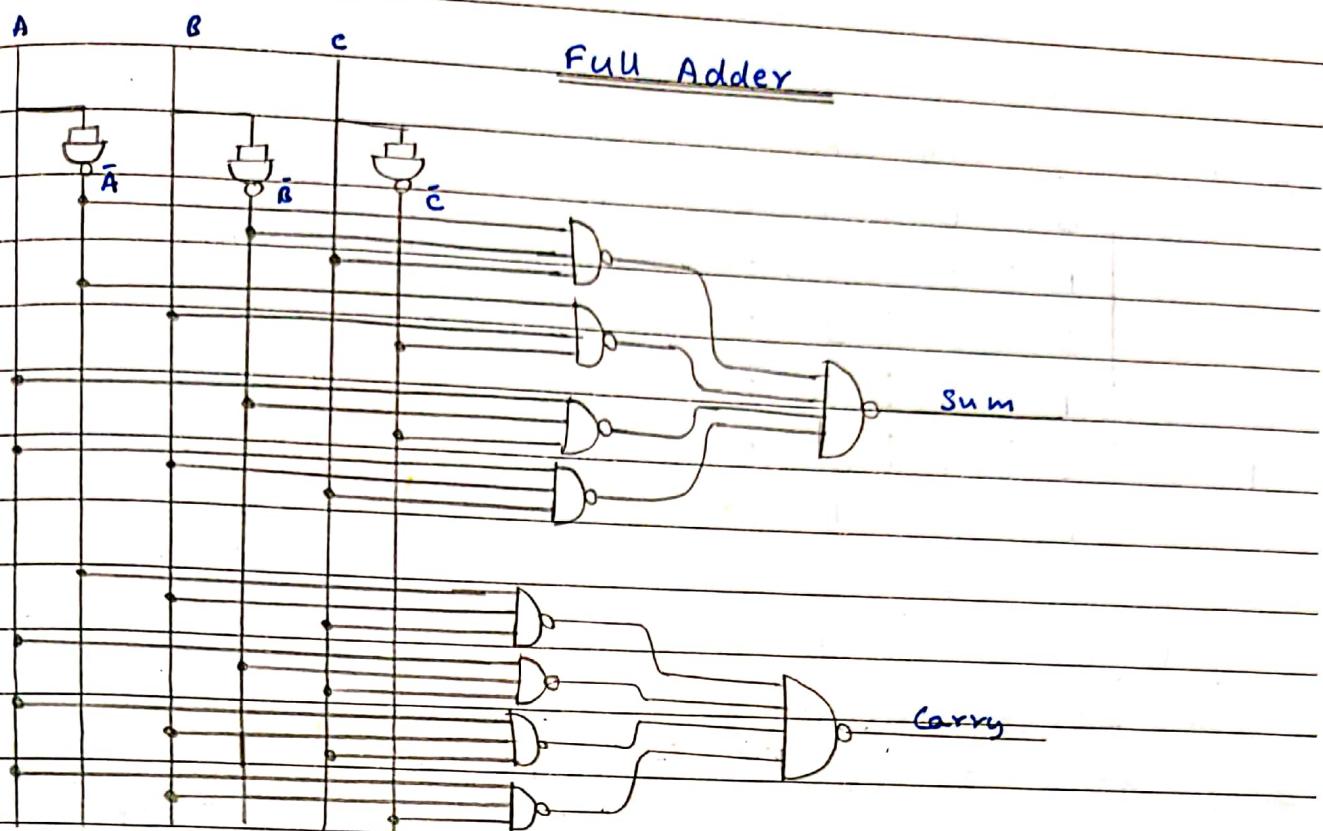
$$1+0=1$$

$$1+1=10$$

↓  
Carry

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1





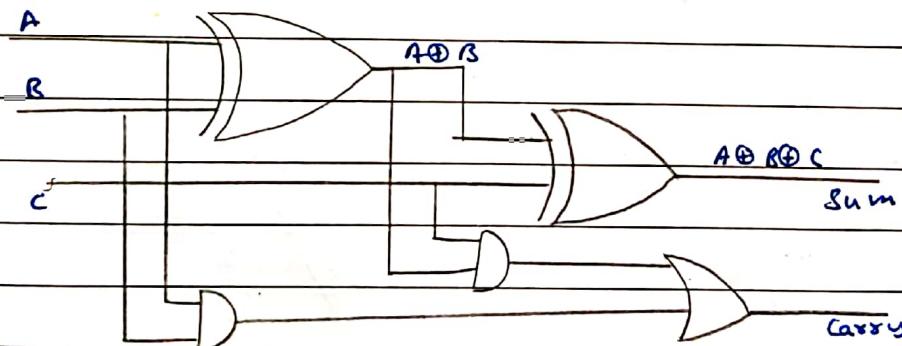
Simplification (sum)

$$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$\bar{A}(\bar{B}\bar{C} + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$A(B \oplus C) + A(\overline{B \oplus C})$$

$$A \oplus B \oplus C$$



Carry

$$\bar{A}B\bar{C} + A\bar{B}C + AB\bar{C} + ABC$$

$$(\bar{A}B + A\bar{B})C + AB(C + \bar{C}) - \Theta$$

$$(A \oplus B)C + AB$$

Carry 0	Carry 1	Carry 0	Carry 1
0	0	0	0
+ 0	0	1	1
0 0 → sum	0 1 → sum	0 1 → sum	1 0 → sum
Carry	Carry	Carry	Carry

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\text{Sum} = \bar{A}\bar{B}\text{Cin} + \bar{A}B\bar{\text{Cin}} + A\bar{B}\bar{\text{Cin}} + AB\text{Cin}$$

$$\text{Carry} = \bar{A}B\text{Cin} + A\bar{B}\text{Cin} + AB\bar{\text{Cin}} + A\bar{B}\text{Cin}$$

From ②

$$(\bar{A}B + A\bar{B})\text{Cin} + AB$$

$$\bar{A}B\text{Cin} + A\bar{B}\text{Cin} + AB$$

$$\bar{A}B\text{Cin} + A(B\text{Cin} + B)$$

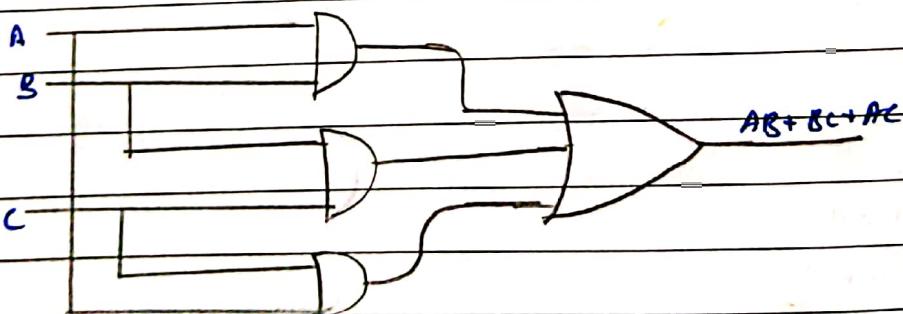
$$\bar{A}B\text{Cin} + A(B + \text{Cin})$$

$$\bar{A}B\text{Cin} + AB + AC\text{in}$$

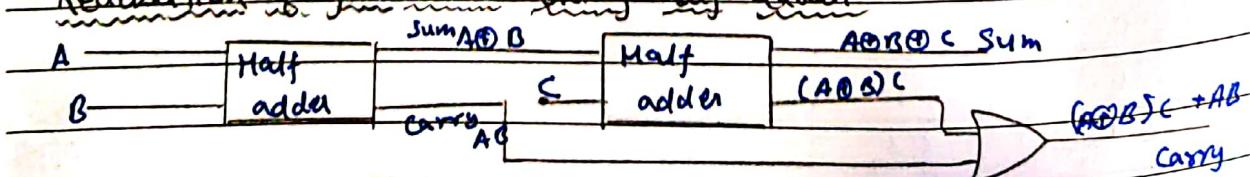
$$B(A + \bar{A}\text{Cin}) + AC\text{in}$$

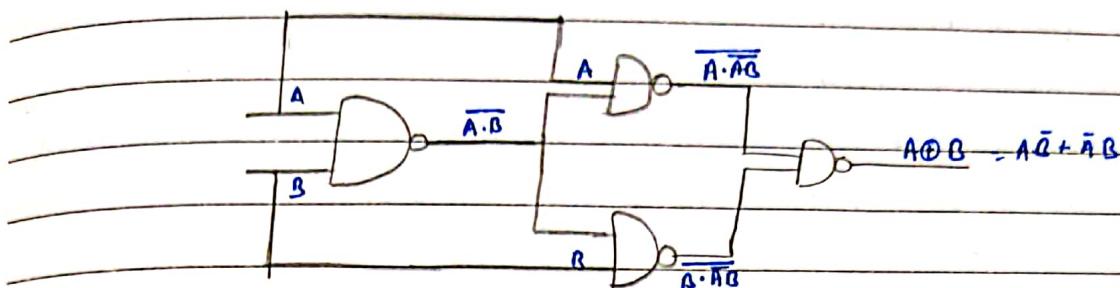
$$B(A + \text{Cin}) + AC\text{in}$$

$$AB + BC + AC$$



Realisation of full adder using half adder



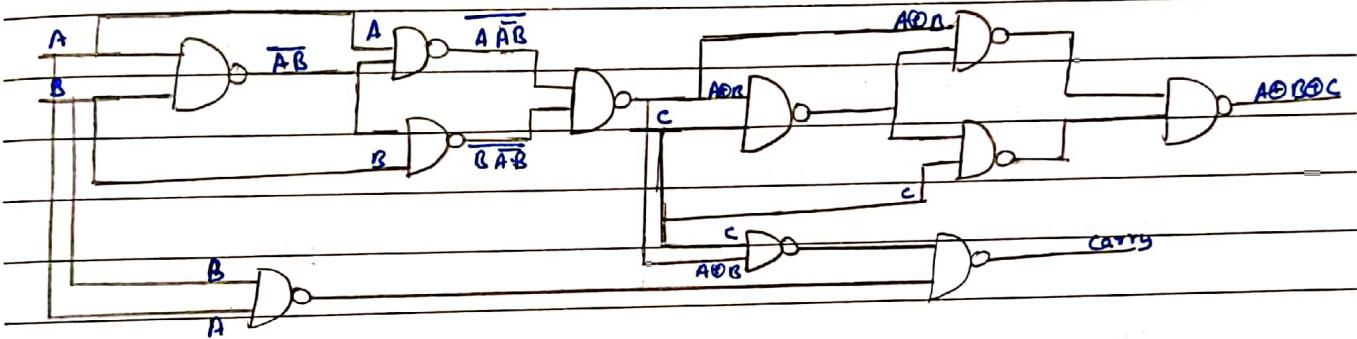
XOR using NAND GatesHalf Adder

$$A \cdot (\bar{A} + \bar{B}) = \bar{A}\bar{B} + \bar{A}B$$

$$\bar{B} \cdot (\bar{A} + \bar{B}) = \bar{A}\bar{B}$$

$$(\bar{A} + B) \cdot (A + \bar{B}) = (\bar{A}\bar{B} + \bar{B}B) = (\bar{A}\bar{B} + B) = (\bar{A} + \bar{B})(A + B) = \bar{A}B + A\bar{B}$$

$$\bar{A}\bar{B} \cdot \bar{A}\bar{B} = \bar{A}\bar{B} + A\bar{B} = \bar{A}B + A\bar{B} \rightarrow \text{DeMorgan's Law}$$

Full Adder

For Sum: 8 NAND GATES

Total: 11 NAND GATES

For Carry: 3 NAND GATES

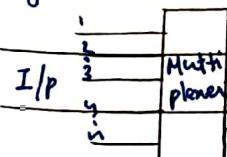
NOTE: XNOR can be realised using NAND gates with an additional NAND gate to the XOR circuit at the O/P with both the input shorted.

Q) Prove that NAND GATE is a universal gate

(Hint: Realize all gates using NAND gates)

Multiplexer and Demultiplexer

- A multiplexer is a circuit which takes the input from 'n' devices but gives out a single output. Demultiplexer is the reverse of multiplexer.



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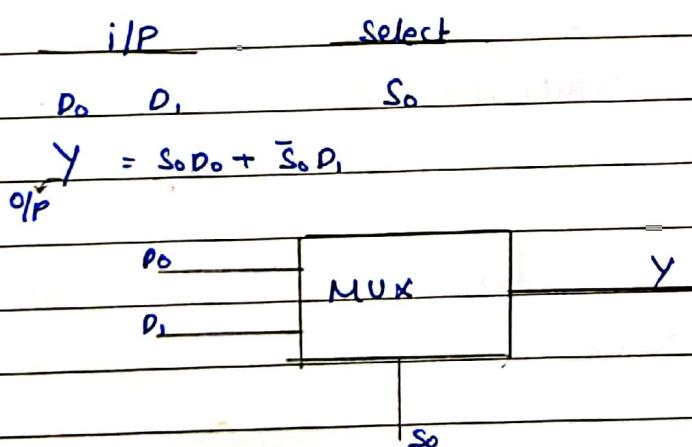
- The number of inputs for a multiplexer is  $2^n$  where  $n$  is the no. of selectors.
- The number of outputs for a demultiplexer is  $2^n$  where  $n$  is the no. of selectors.
- Multiplexer & Demultiplexer are combinational circuits which are designed to handle more number of inputs and outputs.
- In case of multiplexer the no. of inputs is  $2^n$  for  $n$  no. of selectlines whereas demultiplexer has  $2^n$  no. of outputs for  $n$  no. of selectors.

$2^n : 1 \Rightarrow$  Multiplexer

$1 : 2^n \Rightarrow$  Demultiplexer

	M	DM
$n=1$	$2:1$	$1:2$
$n=2$	$4:1$	$1:4$
$n=3$	$8:1$	$1:8$
$n=4$	$16:1$	$1:16$

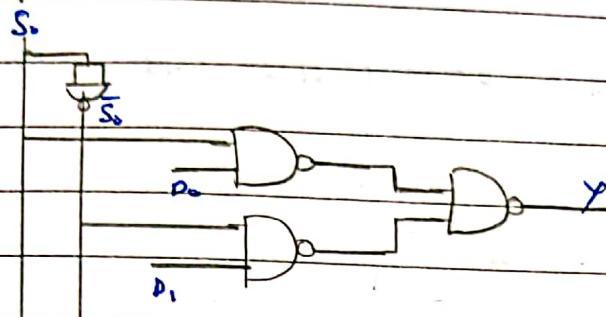
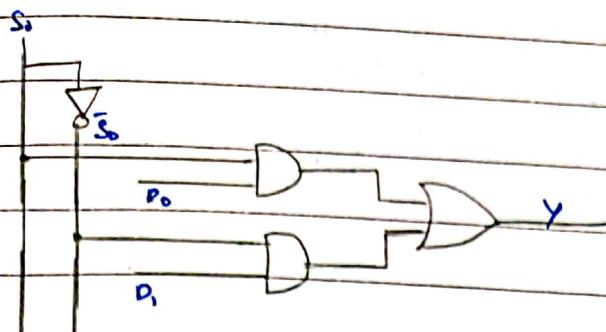
Design of  $2:1$  Multiplexer(Mux) using basic gates and NAND gates



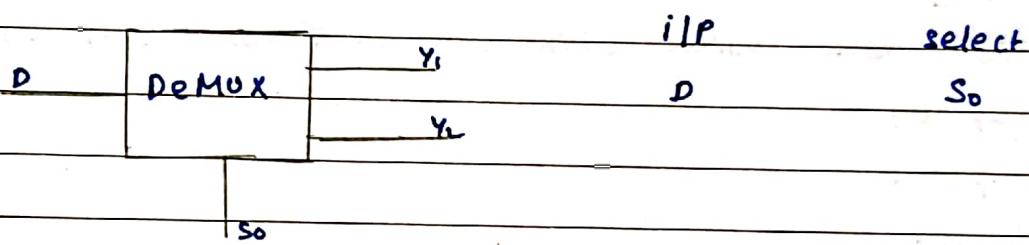
If  $S_0 =$

1	0	1	0	1	0
$D_0$	$D_1$	$D_0$	$P_1$	$B$	$P_1$

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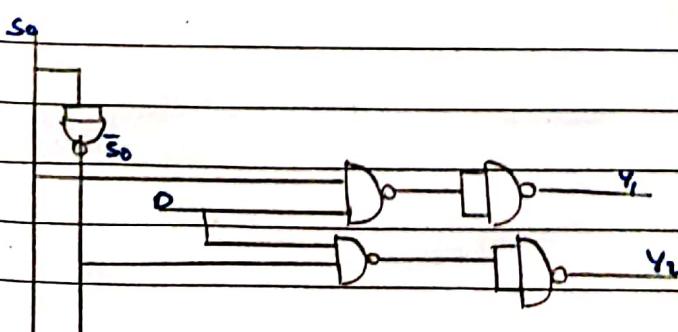
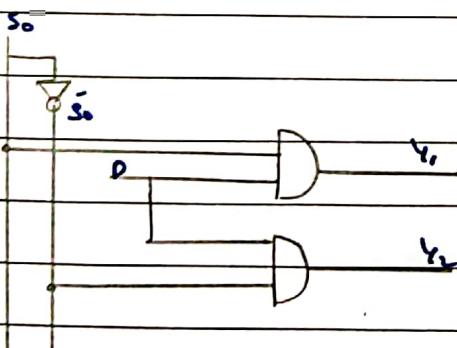


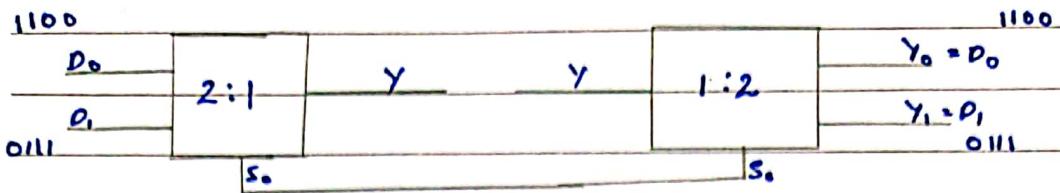
### DeMux - De-Multiplexer



$$y_1 = S_0 D$$

$$y_2 = \bar{S}_0 D$$





## Sequential Circuits

In these circuits, output depends on present state and previous state.

Eg:- Flip - Flop

Registers

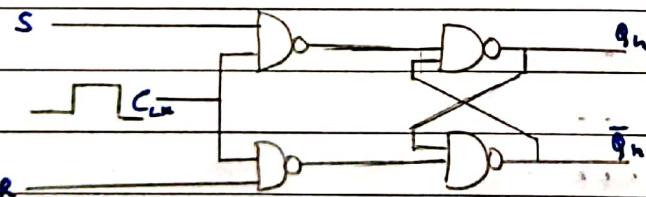
Counters

## Flip - Flop

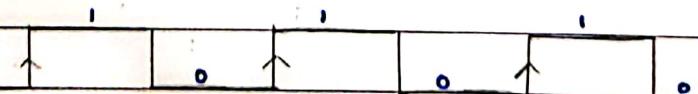
It is a device with 1 bit memory. Types of flip-flop are:-

- SR flip flop
- J-K flip flop
- T flip flop
- D flip flop

## SR flip flop



Flip-Flops are called edge trigger

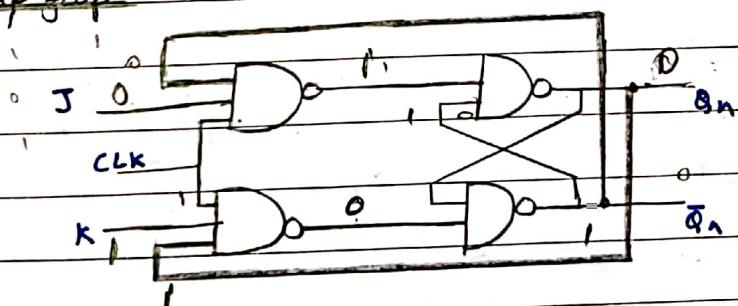


Present Next

CLK	S	R	$Q_n(t)$	$Q_n(t+1)$
$\uparrow L$	0	0	0	0
$\uparrow L$	0	0	1	1
$\uparrow L$	0	1	0	0
$\uparrow L$	0	1	1	0
$\uparrow L$	1	0	0	1
$\uparrow L$	1	0	1	1
$\uparrow L$	1	1	0	-
$\uparrow L$	1	1	1	-

CLK	S	R	O/P $Q_n$
$\uparrow L$	0	0	No change
$\uparrow L$	0	1	0
$\uparrow L$	1	0	1
$\uparrow L$	1	1	forbidden

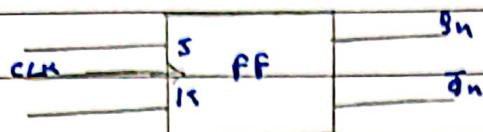
- When both the inputs are 1 the output of the NAND gate is driven to 0. Therefore,  $Q_n$  and its complement is driven to same state which has to be avoided hence, we call it as forbidden state.

JK flip flop

CLK	J	K	$Q_n(t)$	$Q_n(t+1)$
$\uparrow L$	0	0	0	0
$\uparrow L$	0	0	1	1
$\uparrow L$	0	1	1	0
$\uparrow L$	1	0	0	1
$\uparrow L$	1	1	1	1

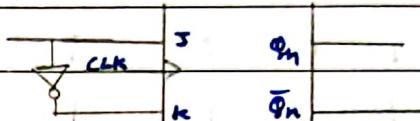
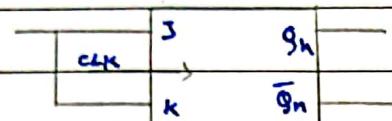
CLK	J	K	O/P $Q_n$
$\uparrow L$	0	0	No change
$\uparrow L$	0	1	0
$\uparrow L$	1	0	1
$\uparrow L$	1	1	Toggle

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T- flip flop

D- flip flop

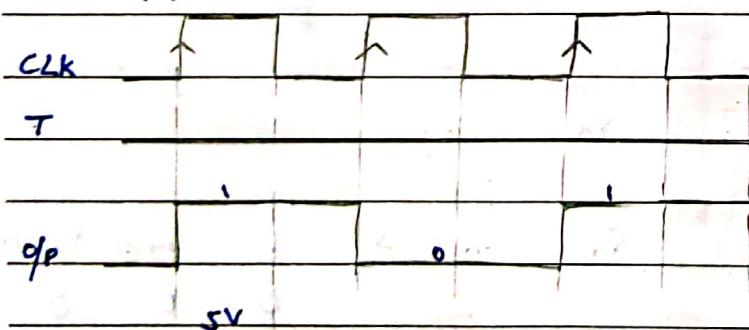


clk	T	Qn	Qn+1
↑	0	0	0
↑	0	1	1
↑	1	0	1
↑	1	1	0

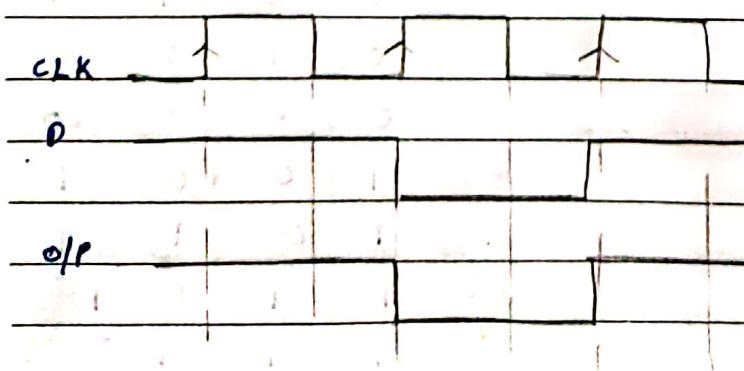
clk	D	Qn	Qn+1
↑	0	0	0
↑	0	1	0
↑	1	0	1
↑	1	1	1

- D-flip flop is also known as data flip flop i.e. whatever the input is given to the flip flop will be stored by the device (either 0 or 1)
- T-flip flop is called Toggle flip flop i.e. when both the inputs are 1 the value changes to next state.

10V



5V



Counters

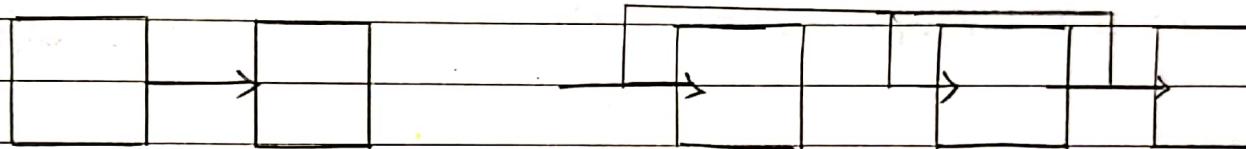
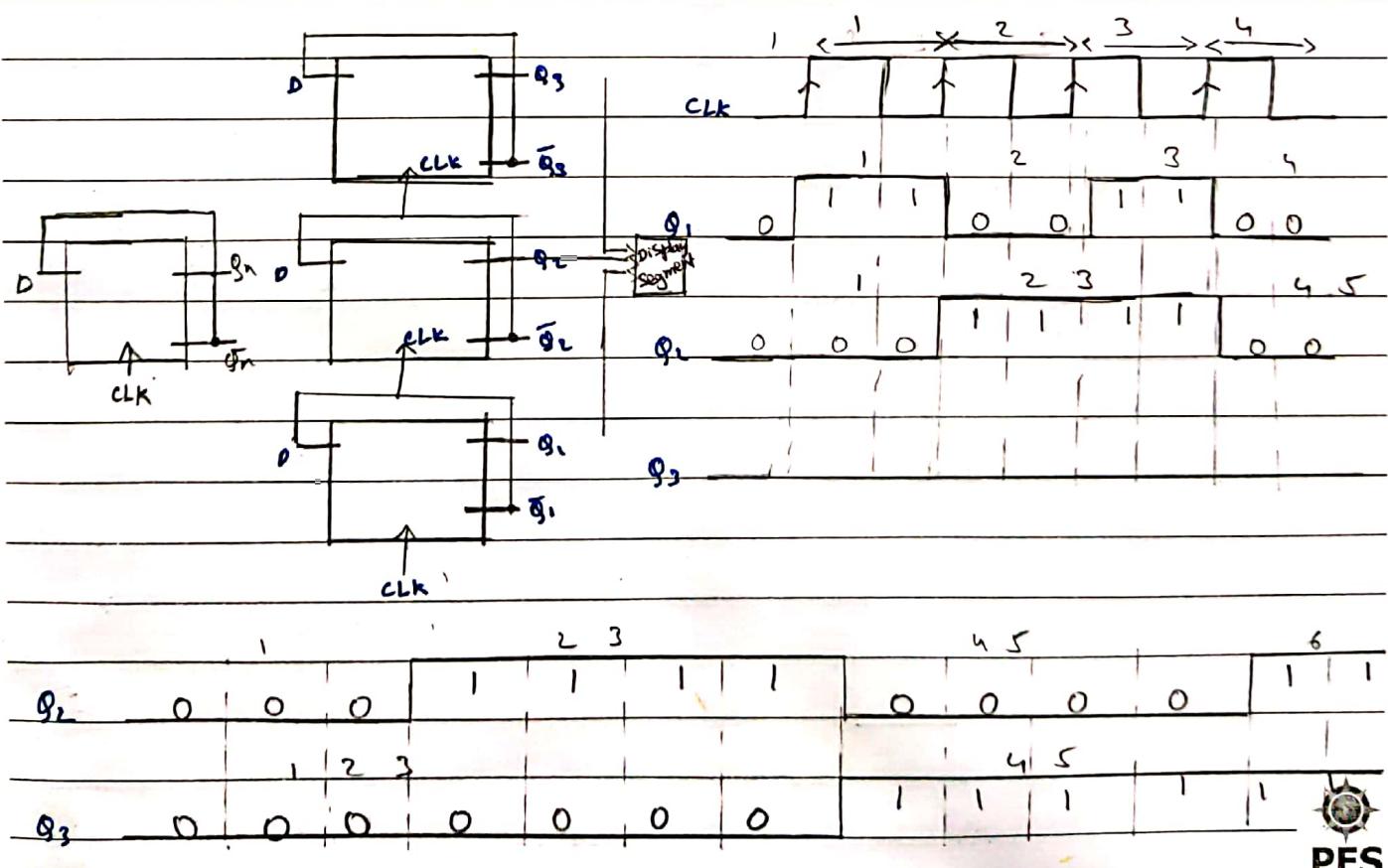
- Counters are the sequential digital circuits used to count the no. of pulses or events occurring in specified interval of time.
  - Counters are designed using flip-flops connected in a cascade.
  - Asynchronous counters ?
  - Synchronous counters
- Types of counters

Asynchronous Counters

- Does not have common clock
- Known as ripple counters

Synchronous Counters

Have a common clock

AsynchronousSynchronousDesign of counters using D-flip flop (Asynchronous)

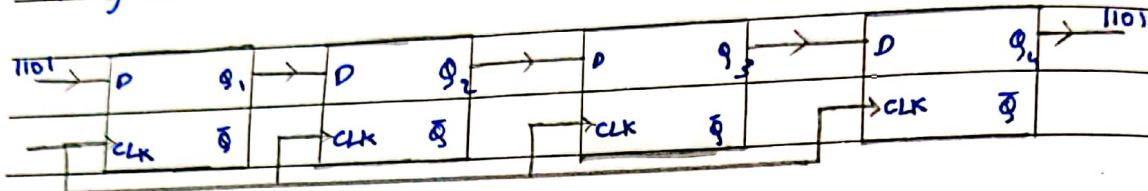
$CLK$	$Q_1$	$Q_2$	$Q_3$
0	0	0	0
1	0	0	1
0	0	1	0
0	0	1	1
1	0	0	0
1	0	0	1
1	1	0	0
1	1	1	0
1	1	1	1

$2^n$  = count we can do

$n$  = no. of flip flops required to  $2^n$  count ( . . . )

Shift Register (4 bit)

- It requires 4 flip flop, common clock.
- The output of flip flop acts as an input for next flip flop.
- They are used to store more than 1 bit of memory.



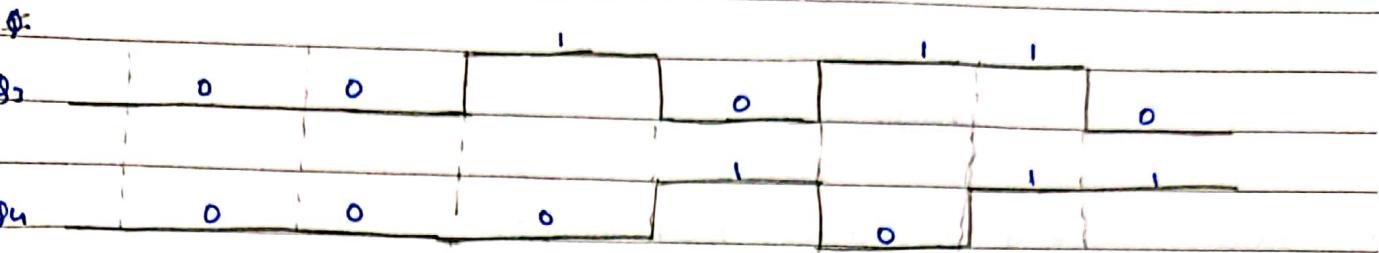
SISO - serial in serial out (output is derived from last flip flop)

SIPO - serial in parallel out (output is derived from all flip flops)

CLK	i/p	$Q_{10}$	$Q_{20}$	$Q_{30}$	$Q_{40}$	$Q_1, Q_2, Q_3, Q_4 \rightarrow$ initially
↑	1	1	0	0	0	
↑	0	0	1	0	0	
↑	1	1	0	1	0	
↑	1	1	1	0	1	$\rightarrow 4^{th}$
↑	0	0	1	1	0	$\rightarrow 5^{th}$
↑	0	0	0	1	1	$\rightarrow 6^{th}$
↑	0	0	0	0	1	$\rightarrow 7^{th}$

- 7 clock are required for 4 bit register to get all the output
- For SIPO we require 4 clock pulse to register in a 4 bit register
- For SISO we require a minimum of clock pulse to register in a 4 bit register.

CLK	1	2	3	4	5	6	7
$Q_1$	1		0		1		1
$Q_2$	0		1	0	1	1	0



Q) Assuming initial condition of a 4 bit register is 0011, if a serial input of 1100 is applied to a 4 bit register write the truth table and timing diagram

### Solution

CLK	i/p	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>
↑	0	0	0	0	0
↑	0	0	0	0	0
↑	1	1	0	0	0
↑	1	1	1	0	0 → SOSP
↑	0	0	1	1	0 → SISO
↑	0	0	0	1	1
↑	0	0	0	0	1

CLK	i/p	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>
↑	0	0	0	0	1
↑	0	0	0	0	0
↑	1	1	0	0	0 → SOSP
↑	1	1	1	0	0
↑	0	0	1	1	0 → SISO
↑	0	0	0	1	1
↑	0	0	0	0	1

