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PES University, Bangalore

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UE15CS253

DEC 2019: END SEMESTER ASSESSMENT (ESA) B.TECH. IV SEMESTER

UE15CS253- Microprocessors & Computer Architecture

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Differentiate the following i. Microprocessors and Microcontroller. ii. Computer Organization and Computer Architecture. iii. RISC and CISC.	06
	b)	What are the most notable features of ARM instruction set?	05
	c)	The address for the memory system starts from 1000. It is byte addressable and follows and follows little endian. Show memory the memory allocated for the following data declaration in ARM memory organization. a:.halfword 200 b:.byte 20,10,60 c:.halfword 30 d:.halfword 100 e:.word 600	05
	d)	Write a program using ARM to add 5 numbers where values are present in registers.	04
2	a)	What are 3 ways of specifying operand values in data processing instructions? Give an example for each.	06

	b)	Write the conditional code for the following code snippets.
		1)
		if (r0 > r1)
		{
		r2= 5
		r3 = r4 + r5
		}
		else
		r6 = r4 –r5
		2)
		if ((r0==r1) && (r2==r3)) then
		R4 := r4 + 1
			06

	c)	In ARM Processor barrel shift is implemented as 32x32 matrix (cross-bar switch). Identify the diagonals that are activated on the execution of the following instructions. I) MOV R0, R1, LSR #2; II)ADD R1, R0, R1, LSL #0; III) ADD R1, R0, R1, LSR #32	03
	d)	Explain the handshaking signals used by ARM and its coprocessor for execution of coprocessor instructions?	05
3.	a)	Explain pipelining with an example.	06
	b)	Consider two instructions *i* and *j*, with *i* occurring before *j*. Explain the possible data hazards.	06

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	c)	What is a hazard? Explain different types of hazards.	06
	d)	What is data forwarding?	02
4.	a)	A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. a) How many bits are there in a main memory address? b) How Many bits are there in each of the TAG, SET and WORD fields?	06
	b)	Write a note on DMA.	05
	c)	Write the corresponding miss category in each of the following scenario. i. Initially, the cache is empty. The very first access to the block will generate a miss. ii. During the execution of the program, cache generated a miss. This is because the cache could not contain all the blocks needed during the execution of the program. iii. Multiple blocks map to its set(set=1 for direct cache) higher in the hierarchy.	03
	d)	Briefly explain the different write strategies.	06
5.	a)	What is an interrupt? Explain hardware and software interrupts.	05
	b)	Explain the interrupt handling scheme for a non-nested interrupt .	05
	c)	What is instruction level parallelism?Consider the following program: e = a + b f = c + d m = e * f If we assume that each operation can be completed in one unit of time what is the total amount of time required to execute the above program?	05
	d)	Explain the following techniques i. Polling ii. Daisy Chain Technique.	05