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# UNIT V

# CORE OF THE EMBEDDED SYSTEM

# UNIT OUTCOME

**At the end of this unit, student will be able to**

Understand about the following concepts:

Microprocessors

Microcontrollers

GPP Vs ASIC

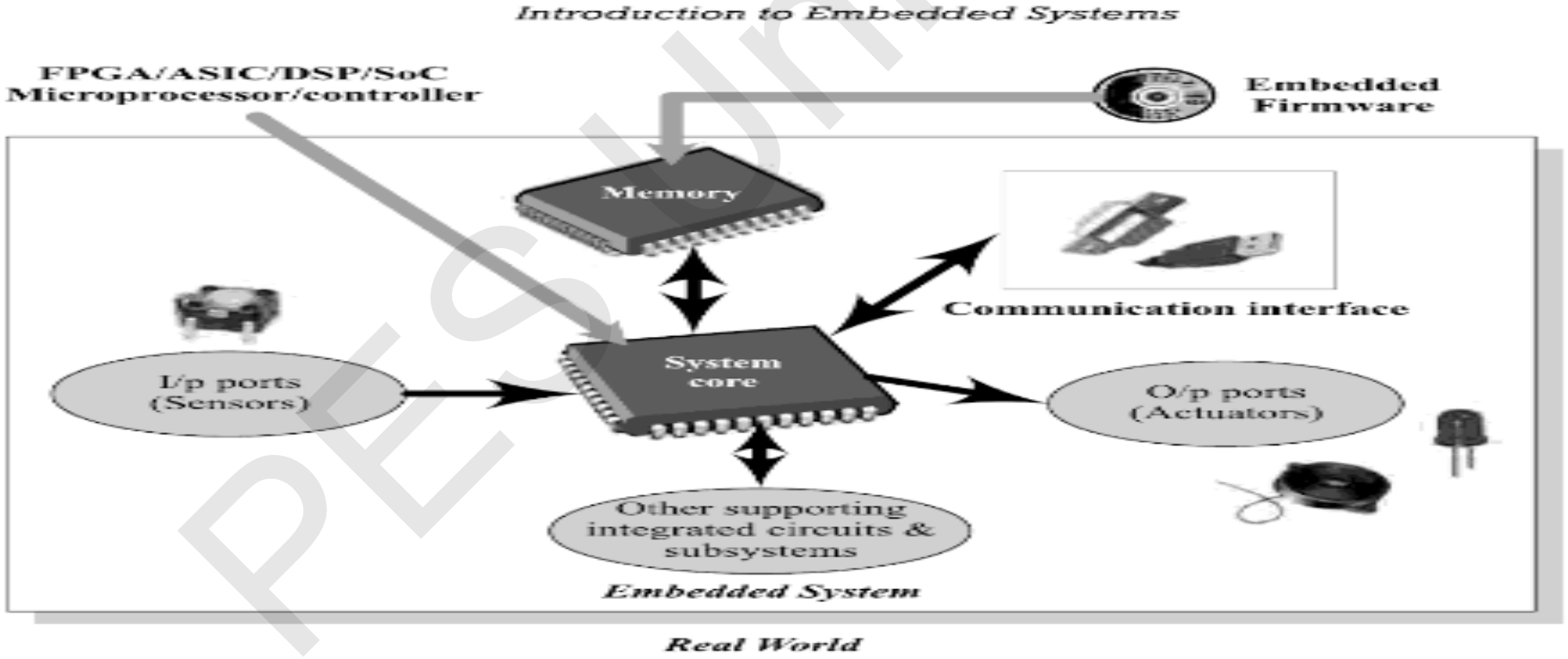
Basics of ARM PROCESSOR

# INTRODUCTION TO EMBEDDED SYSTEMS

- An Embedded system is an electronic /elctromechanical system designed to perform a specific function and is a combination of both Hardware and Software.

- It is unique and the hardware and firmware are highly specialized to the application domain.

- It may or maynot contain an operating system for functioning.



# INTRODUCTION TO EMBEDDED SYSTEMS

## Purpose of Embedded Systems

- Data Collection/ Storage/Representation
- Data Communication
- Data processing, Monitoring
- Control Application specific user interface.

## Applications of Embedded Systems

- Consumer electronics
- Household appliances
- Home automation
- Banking and retail
- Measurement and Instrumentation
- Health care
- Automotive industry.

# Characteristics of an Embedded Systems

- A system which is a combination of special purpose hardware and embedded OS for executing a specific set of applications.
- May or maynot contain an operating system for functioning.
- The firmware of an ES is pre-programmed and it is non alterable by the end user.
- Application specific requirements are the key deciding factors.
- Highly tailored to take advantage of the power saving modes supported by the hardware and the OS.
- Execution behavior is deterministic for certain types of ES like “Hard Real Time Systems”.
- The response time requirement is crtical for some critical systems.

# Classification of Embedded System

**Multiple Classifications based on different criteria:**

- **Based on Generation**
  - First Generation
  - Second Generation
  - Third Generation
  - Fourth Generation
- **Based on complexity and Performance**
  - Small Scale Embedded systems
  - Medium Scale Embedded systems
  - Large Scale Embedded systems
- **Based on Deterministic Behaviour**
  - Deterministic/Non Deterministic
  - Real time ES: Hard/ Soft

# Core of the Embedded Systems

- Embedded Systems are built around a central Core
- General Purpose and Domain Specific Processors
  - Microprocessors
  - Microcontrollers
  - Digital Signal processors
- Application Specific Integrated Circuits (ASIC's)
- Programmable Logic Devices (PLD's
- Commercial Off the Shelf Components (COTS)

# General Purpose and Domain Specific Processors contd....

- Endianess Operation
- Endianness specifies the order in which the data is stored in the memory by processor operations in a multi byte system.
    - Little Endian Operation
    - Big Endian Operation
- Load and Store Operation
- The memory access related operations are performed by the special instructions load and store.

# essors: General Purpose and Domain Specific Processors

- Silicon chip representing a CPU, performing aritmetic and logical operations according to a pre-defined set of instructions.
- CPU contains Arithmetic and Logic Unit(ALU) ,control units and working registers.
- It is independent unit requires different combination of hardwares for proper functiong.
- First microprocessor unit intel 4004 a 4 bit processor was introduced by intel in November 1971.
- Technical advances in the field of semiconductor industry leads to the improved performance of microprocessors in terms of clock speed,size,cost performance etc.
- **Architecture:**

  **Harvard Architecture**-Separate buses for program memory and data memory.

  **Von Neumann Architecture**-Share a single system bus or program memory and data memory.
- **Instruction Sets:**

  **RISC** (Reduced Instruction Set Computing) &

  **CISC** (Complex Instruction Set Computing)

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# Microcontrollers

- Super set of Microprocessors
- Highly integrated chip consist of CPU, Scratch pad RAM, special and general purpose register arrays, on chip ROM/FLASH memory for program storage, timer and interrupt controller units and dedicated I/O ports.
- Independent of working, cheap, cost effective and readily available in market.
- Texas Instruments TMS 1000 is the world's first microcontroller.
- The most fruitful design of microcontroller is the 8 bit microcontroller 8051 family and its derivatives.
- Instruction set architecture of a microcontroller can be either RISC or CISC.

# General Purpose and Domain Specific Processors contd...

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# Microprocessor Vs Microcontroller

| Microprocessor | Microcontroller |
| --- | --- |
| A silicon chip representing CPU, performing ALU operations according to pre defined set of instructions. | A highly integrated chip that contains Scratch pad RAM, special and general purpose register arrays, on chip ROM/FLASH memory for program storage, timer and interrupt controller units and dedicated I/O ports. |
| It is a dependent unit. | It is independent unit. |
| General purpose design and operation. | Application oriented or domain specific. |
| Doesn't contain a built in I/O port. | Contains multiple built in I/O ports. |
| Targeted for high end market where performance is important. | Targeted for Embedded market. |
| Limited power saving options. | Includes lot of power saving features. |

# Digital Signal Processor

- Powerful special purpose 8/16/32 bit microprocessor designed specifically to meet the computational demands and power constraints of different application's.
- 2 to 3 times faster than GPP in signal processing application's.
- It implements algorithms in hardware which speeds up the execution.
- A typical DSP incorporates the following units:
  - Program Memory: storing program required by DSP.
  - Data Memory: Storing temporary variables and data /signal to be processed.
  - Computational Engine: Performs the signal processing accordance with the stored program memory.
  - I/O unit: Acts as an interface between the outside world and DSP( capturing signals and delivering processed signals).
- Ex: Audio video signal processing, telecommunication and Multimedia Application, real time calculations like FFT, DFT, SOP etc.,

# General Purpose Processor Vs Application Specific Instruction Set Processor

## GPP

- Designed for general Computational Tasks.

  Ex: laptop, Desktop
- It contains ALU and Control Unit.
- High volume of production / low cost per unit.

## ASIP

- The processors contains architecture and instruction set optimised to specific domain/ application requirements.

  Ex: SoC, DSP's used in automotive, Telecom, media applications etc.,
- It incorporates a processor and on chip peripherals demanded by the application requirement, program and data memory.
- It fills the architectural spectrum between GPP and ASIC's.

# Application Specific Integrated Circuits (ASIC's)

- It is a microchip deigned to perform a specific or unique application.
- Used as a replacement for conventional general purpose logic chips.
- It integrates several functions into a single chip and consumes very small area in the total system.
- It can be pre-fabricated for a special application or it can be custom fabricated by using the components from a re-usable building block library of components .
- Non Recurring Engineering Charge (NRE) : It is a non refundable initial investment for the fabrication of ASIC's and it is a one time investment.
- Application Specific Standard Product (ASSP): If the Non Recurring Engineering Charges is borne by a third party and the Application Specific Integrated Circuit (ASIC) is made openly available in the market, the ASIC is reffered as ASSP.

Ex: ADE7760 Energy Metre ASIC developed by Analog Devices for Energy Metreing applications.

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# Programmable Logic Devices (PLD's)

- PLD's can be re- configured to perform any number of functions at any time.

**Features of PLD's**

- It has a wide range of logic capacity, features, speed and voltage characteristics
- The designers uses inexpensive software tools to quickly develop, simulate and test their designs.
- There are no NRE cost and the final design is completed fastly.
- PLD's are based on re-writable memory technology.

**Two major types of PLD's are**

- **CPLD's** : offer smaller amount of logic up to about 10,000 gates, offer very predictable timing characteristics suitable for critical control applications. Ex: Xilinx Coolrunner.
- **FPGA's**: offer highest amount of logic density, the most features and the highest performance. Ex: Xilinx VirtexTM.

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# Commercial Off -the -Shelf Components (COTS)

- COTS provides easy integartion and interoperability with existing system components.
- It can be developed around GPP, Domain specific Processor , ASIC or PLDs

**Advantage:**

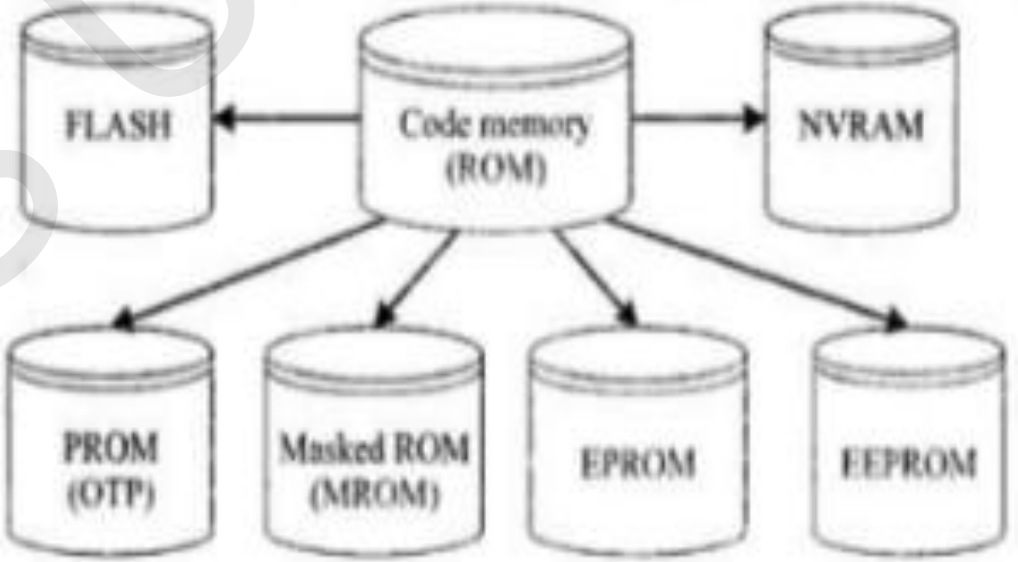
- Readily available in market, cheap and a developer can cut down his/her development time to a great extent.

**Disadvantage:**

- Due to rapid change in technology, if the COTS component is withdrawn by the manufacturer/ or discontinue the production , will adversely affect a commercial manufacturer of ES which make use of the specific COTS product.

# Memory

- Memory is required for holding data temporarily during certain operations.
- On chip memory: built in memory
- Off chip memory: external memory connected with the controller/ processor for storing controller algorithm.
- Program Storage Memory
- Also called as code storage memory of an ES stores the program instructions.
- It retains its contents e storage memory)



# Program Storage Memory (ROM)- Classification

- Depends on fabrication, erasing and programming technique, ROM is divided as follows:

**A) Masked ROM (MROM)**

- One time Programmable device
- Uses hardwired technology to store the data
- This is low cost for high volume of production.
- It is a good candidate for storing the embedded firmware for low cost embedded device.
- Limitation is that its inability to modify the device firmware against firmware upgrades.

**B) Programmable Read Only memory (PROM/OTP)**

- The end user is responsible for programming this memory
- This memory consists of polysilicon or nichrome wires functionally viewed as fuses
- Fuses which are not blowned /burned represents logic “1” whereas fuses which are blowned/ burned represents logic “0”
- OTP isused in commercial production of ES

# Program Storage Memory (ROM)-Classification (contd...)

**C) Erasable Programmable Read Only Memory ( EPROM)**

- EPROM gives flexibility to re-program the same chip.
- It stores the bit information by charging the floating gate of an FET to a high voltage.
- It contains a quartz crystal window , which is exposed to UV rays rays for 20 to 30 minutes, the entire memory will be erased.
- Limitation is Erasing the memory using UV rays is tedious and time consuming process.

**D) Electrically Erasable Programmable Read Only Memory ( EEPROM)**

- The information contained in this memory can be erased and re-programmed in-circuit using electrical signals at register/Byte level.
- It provides greater flexibility for system design.
- Limitation is its capacity (only a few kilobytes).

# Program Storage Memory (ROM)- Classification (contd...)

**E) FLASH**

- Latest ROM technology which combines the re-progarmmability of EEPROM and high capacity of standard ROMs.
- It is organized as sectors /pages.
- It stores the information in array of floating gate of an MOSFET.
- Each sector is erased before re-programming and it is done at sector level /page level without affecting sector/page.
- The typical erasable capacity is 1000cycles.

Ex: W27C512 from WINDBOND (64 KB FLASH memory)

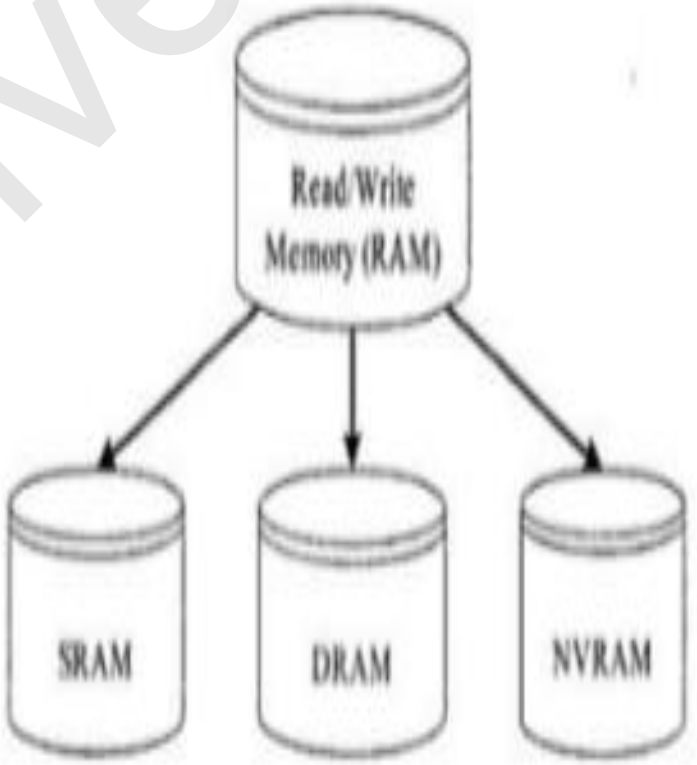
**F) NVRAM ( Non volatile RAM)**

- It is a RAM with battery backup.
- The lifespan of NVRAM is around 10 years

Ex: DS1644 from Maxim/Dallas (32 KB NVRAM)

# Read- Write Memory/ Random Access Memory (RAM)

- **RAM** is the data or working memory of controller/ processor wher it can read from it and write to it.
- It is volatile in nature
- It is a direct access memory
- **Categories:**
  - Static RAM (SRAM)
  - Dynamic RAM (DRAM)
  - Non-volatile RAM (NVRAM)



# Read- Write Memory/ Random Access Memory (RAM) - Classification

- **A) Static RAM (SRAM)**
  - It is the fastest form of RAM available (Resistive networking and Switching capabilities).
  - It is made up of flip-flops and stores data in the form of voltage.
  - It is realised using six transitors (MOSFET) out of which four is for building the latch part of memory cell and two for controlling the access.
  - The major limitation of SRAM are low capacity and high cost.
- **B) Dynamic RAM**
- It stores the data in the form of charge

Advantage: high density and low cost

Disadvantage: Since it is stored as charge , it will get leaked off with

time, so refreshing is needed.

- Special circuits called DRAM controllers are used for refreshing the operation.

# Difference between SRAM and DRAM

**SRAM**

- Made up of 6 CMOS Transistors (MOSFET)
- Doesn't require refreshing
- Low capacity
- Fast in operation. Typical access time is 10ns

**DRAM**

- Made up of a MOSFET and a capacitor
- Require refreshing
- High Capacity
- Less expensive
- Slow in operation. Typical access time is 60ns
- Write Operation is faster tahn read operation

# Read- Write Memory/ Random Access Memory (RAM)- Classification contd...

**C) NVRAM ( Non volatile RAM)**

- It is a RAM with battery backup.
- It contains static RAM based memory
- The lifespan of NVRAM is around 10 years
- Ex: DS1744 from Maxim/Dallas (32 KB NVRAM)

**D) Memory according to the Type of Interface**

- Parallel Interface: Parallel data lines for an 8 bit processor/controller will be connected to the memory (memory size is in terms of kilobytes).
- Serial Interface: I2C :2 line serial interface (used for data storage memory like EEPROM, memory size is in terms of kilobits) .
- Ex: Atmel Corporations AT24C512 (512 K bits/ 2 wire interface).
- Serial Peripheral Interface (SPI) : 2+n line interface where n stands for the total number of SPI bus devices in the system.
- Single wire interconnection.

# Sensors and Actuators

## Sensors

- A sensor is a transducer device that converts energy from one form to another for any measurement or control purpose.

## Actuators

- An actuator is a form of transducer device (mechanical or electrical) which converts signals to corresponding physical motion. It is an output device.

# I/O Subsystem

- The I/O subsystem of the embedded system facilitates the interaction of the embedded system with the external world.
  - Light Emitting Diode (LED)
  - 7 Segment LED display
  - Optocoupler
  - Stepper Motor
  - Relay
  - Piezo Buzzer
  - Push Button Switch
  - Keyboard
  - Programmable Peripheral Interface (PPI)

# Communication Interface

- Device/ Board level communication Interface ( Onboard Communication Interface)
  - The communication channel which interconnects the various components within an embedded product

  Ex: Serial Interface like I2C, Spi, UART, 1-Wire & parallel bus interface
- Product level Communication Interface (External Communication Interface)
  - Responsible for data transfer between the embedded system and other devices or modules.
  - It can be wired media , wireless media , serial or parallel interface

  Ex: IR, Bluetooth, Wi- Fi, RS232c, USB, Ethernet etc

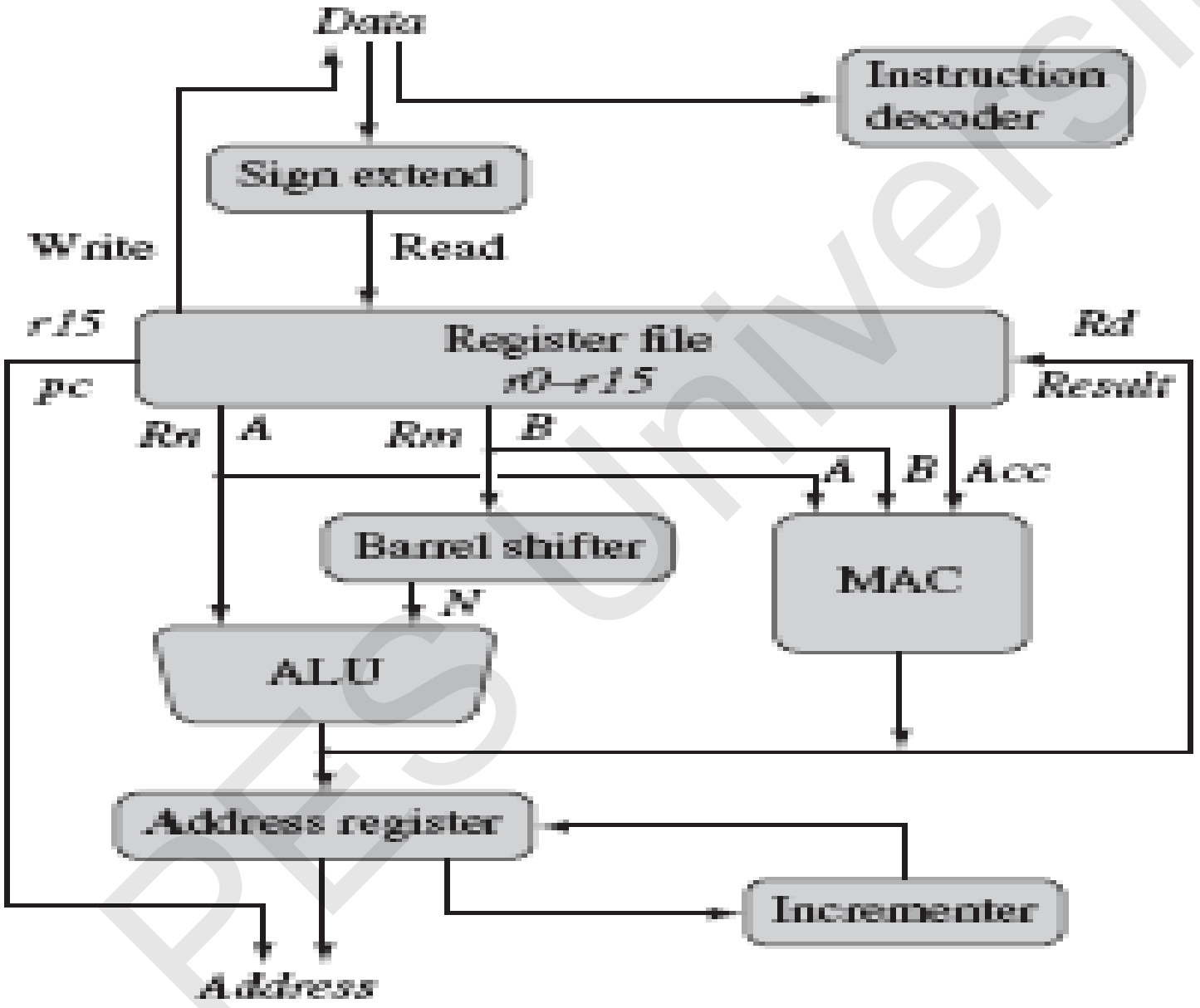
# Onboard communication Interfaces

- **Inter Integrated Circuit (I2C)**
  - It is a synchronous bi-directional half duplex two wire serial interface bus.
  - It provides an easy way of connection between a microprocessor/ microcontroller system and the peripheral chips in television sets.
  - It comprise of two bus lines:
    - » **Serial Clock- SCL:** Responsible for generating synchronisation clock pulses
    - » **Serial Data – SDA :** Responsible for transmitting the serial data across devices.
  - It supports multimasters on the same bus
  - It supports three different data rates
    - » Standard Mode: ( Data rate upto 100Kbps)
    - » Fast Mode: ( Data rate upto 400Kbps)
    - » High Speed Mode: ( Data rate upto 3.4Mbps)

# Onboard communication Interfaces contd...

- It is a shared bus system. The devices connected to it can act as Master or Slave.
- Master: Responsible for controlling the communication by initiating/terminating data transfer, sending data and generating synchronisation clock pulses.
- Slave : waits for the commands from the master and respond upon the receiving commands.
- Master and slave device can act as either transmitter or receiver.
- The synchronisation clock signal is generated by the Master device , regardless the master is acting as transmitter or receiver.

# ARM PROCESSOR FUNDAMENTALS



# Data flow model

- Data enters the processor core through data bus
- Instruction decoder translates instructions before they are executed.
- Data items are placed in register file-storage bank made of **32- bit registers**
- Sign extend converts signed **8-bit and 16-bit numbers to 32 bit** values
- **Two source registers-Rn and Rm Single destination register Rd**
- Source operands are read from register file using internal buses A and B
- ALU takes the register values Rn and Rm and computes the result
- Barrel shifter computes the result for any number of shifts within a clock cycle .
- This is achieved as it is combinational logic (not sequential)

ex:ADD R3,R2,LSL#4

- Multiply-Accumulate Circuit is used to perform both multiply and add

Ex : Matrix addition and multiplication

- Load and store instructions use the ALU to generate an address to be held in the address register and broadcast on the Address bus

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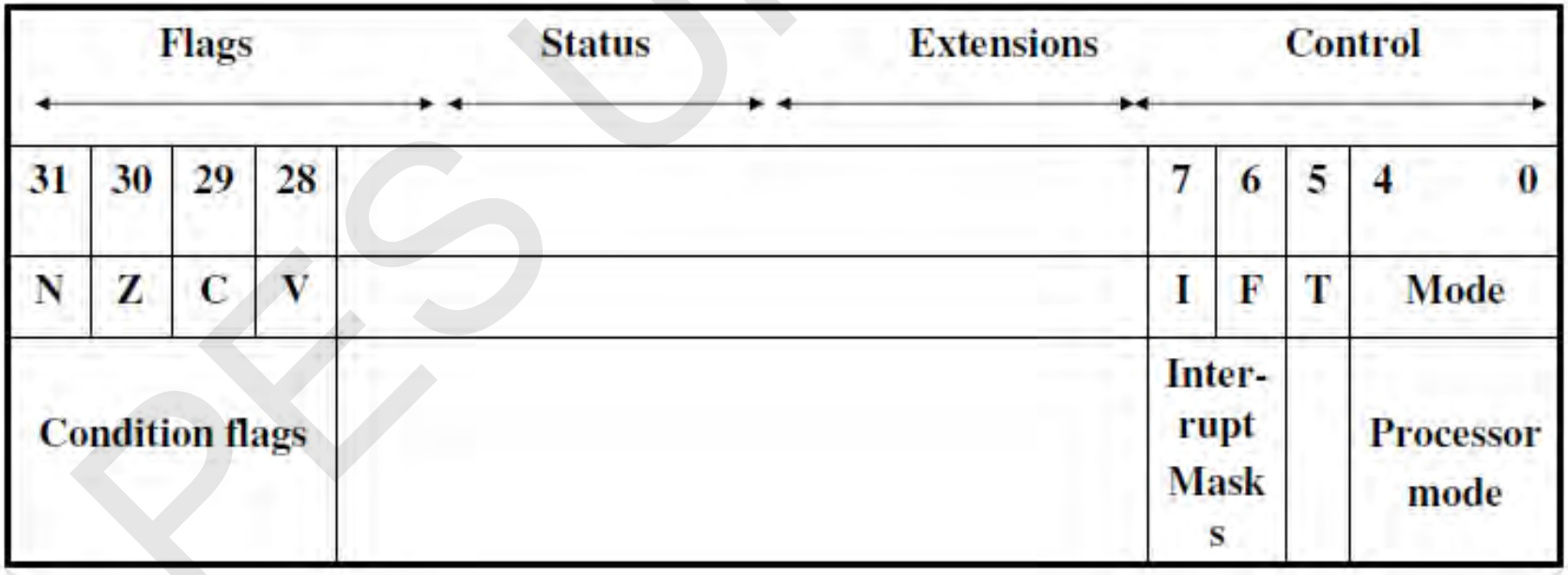
# REGISTERS

- **Stack Pointer**- stores the head of the stack in the current processor mode
- **Link register**- core puts the return address when it calls a subroutine
- **Program counter**- contains the address o the next instruction to be fetched by the processor
- In ARM state the registers R0 – R15 are orthogonal.
- Any instruction that you can apply to R0 can equally well apply to other registers

# Current Program Status Register (CPSR)

- 32-bit register
- contains the present status of an internal operation
- ARM uses CPSR to monitor and control internal operations.
- CPSR is a dedicated 32-bit register and resides in the register file.
- A generic program status register



# Current Program Status Register (CPSR) contd...

**PROCESSOR MODES**

- The processor mode determines which registers are active and the access rights to the CPSR bregister itself.

**Privileged mode-**allows full read write access to CPSR

- Abort
- fast interrupt request
- Interrupt request
- Supervisor
- System
- Undefined

**Non –Privileged mode**

- read access to control field to CRSP
- read-write access to conditional flags
- User

# Current Program Status Register (CPSR) contd...

**PROCESSOR MODES**

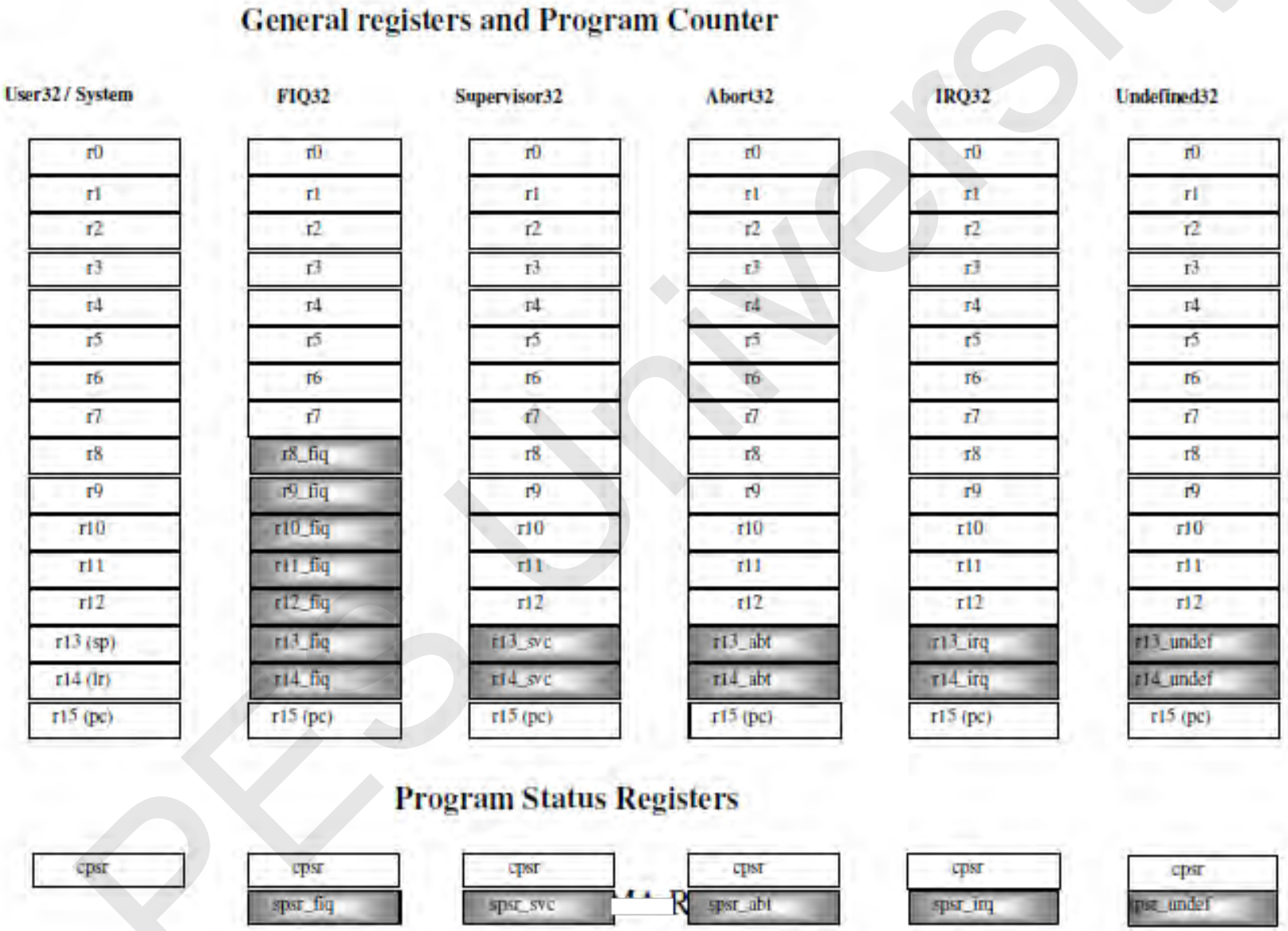
The ARM has seven operating modes:

- User (unprivileged mode under which most tasks run).
- FIQ (entered when a high priority (fast) interrupt is raised).
- IRQ (entered when a low priority (normal) interrupt is raised).
- Supervisor (entered on reset and when a Software Interrupt instruction is executed).
- Abort (used to handle memory access violation.
- Undefined (used to handle undefined instructions).
- System (privileged mode using the same registers as user mode).

# Banked Registers

- ARM has 37 registers in total, all of which are 32-bits long.
- 1 dedicated program counter
- 1 dedicated current program status register
- 5 dedicated saved program status registers
- 30 general purpose registers
- 20 registers are hidden from a program at different times. These registers are called banked registers
- They are available only when the processor is in a particular mode.

# Register Organization



# Current Program Status Register (CPSR) contd..

**State and instruction sets**

- The state of the core determines which instruction set is being executed.Three instruction sets

  ARM-Arm state

  Thumb-Thumb state

  Jazelle- Jazelle state

**Interrupt Masks**

- Interrupt masks are used to stop specific interrupt requests from interrupting the processor.
- Two interrupt request levels- IRQ, FIQ

  CPSR has two interrupt mask bits

  7(I bit )-IRQ

  8 (F bit )-FIQ

  These interrupt requests are masked when set.

# Conditional Flags/Conditional Execution

**Conditional Flags**

- Updated by comparisons
- Results of ALU operations that specify S instruction suffix.

Eg: SUBS

- **Conditional execution**
- Conditional execution controls whether or not the core will execute an instruction.
- Condition attribute is post fixed to the instruction mnemonic, which is encoded into the instruction.
- Prior to execution, the processor compares the condition attribute with the conditional flags in the CPSR.
- If they match then the condition is executed.
- When a condition mnemonic is not present, it always AL