

DIGITAL DESIGN AND COMPUTER ORGANIZATION

Logic Minimization, K-Maps - 4

Reetinder Sidhu

Department of Computer Science and Engineering



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Course Outline



- Digital Design
 - Combinational logic design
 - ★ Logic Minimization, K-Maps 4
 - Sequential logic design
- Computer Organization
 - Architecture (microprocessor instruction set)
 - Microarchitecure (microprocessor operation)

Concepts covered

- K-Map for Four Inputs
- K-Map for Two inputs
- Truth Tables with Don't Care Symbols
- K-Maps with Don't Care Symbols



K-Map Structure (four input Boolean function)

а	Ь	С	d	У	minterm
0	0	0	0	1	$\overline{a}\overline{b}\overline{c}d$
0	0	0	0	0	ābcd
0	0	1	0	1	$\overline{a}\overline{b}c\overline{d}$
0	0	1	0	0	ābcd
0	1	0	0	0	$\overline{a}b\overline{c}\overline{d}$
0	1	0	0	1	ābcd
0	1	1	1	0	$\overline{a}bc\overline{d}$
0	1	1	1	1	ābcd
1	0	0	1	1	ab c d
1	0	0	1	0	a b cd
1	0	1	0	1	$a\overline{b}c\overline{d}$
1	0	1	0	0	abcd
1	1	0	1	0	$ab\overline{c}\overline{d}$
1	1	0	1	1	abcd
1	1	1	1	0	abcd
1	1	1	1	1	abcd

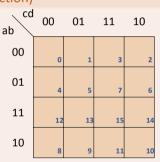
Four Input Truth Table



K-Map Structure (four input Boolean function)

а	Ь	С	d	y	minterm
0	0	0	0	1	ābcd
0	0	0	0	0	<u>ā</u> b̄cd
0	0	1	0	1	$\overline{a}\overline{b}c\overline{d}$
0	0	1	0	0	$\overline{a}\overline{b}cd$
0	1	0	0	0	$\overline{a}b\overline{c}\overline{d}$
0	1	0	0	1	ābcd
0	1	1	1	0	$\overline{a}bc\overline{d}$
0	1	1	1	1	ābcd
1	0	0	1	1	a b cd
1	0	0	1	0	a b cd
1	0	1	0	1	abcd
1	0	1	0	0	abcd
1	1	0	1	0	ab c d
1	1	0	1	1	ab c d
1	1	1	1	0	abcd
1	1	1	1	1	abcd
	E		A. T.	4.1	T- I- I -

Four Inp	ut	Tru	th	Table	e
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- Each square corresponds to a row of the truth table
- Any two adjacent squares differ only in one literal

Columns as well as rows arranged in binary order 00,01,11,10



K-Map Structure (four input Boolean function)

а	Ь	С	d	У	minterm
0	0	0	0	1	$\overline{a}\overline{b}\overline{c}\overline{d}$
0	0	0	0	0	<u>a</u> b̄cd
0	0	1	0	1	$\overline{a}\overline{b}c\overline{d}$
0	0	1	0	0	<u>a</u> bcd
0	1	0	0	0	$\overline{a}b\overline{c}\overline{d}$
0	1	0	0	1	ābcd
0	1	1	1	0	$\overline{a}bc\overline{d}$
0	1	1	1	1	ābcd
1	0	0	1	1	$a\overline{b}\overline{c}\overline{d}$
1	0	0	1	0	$a\overline{b}\overline{c}d$
1	0	1	0	1	$a\overline{b}c\overline{d}$
1	0	1	0	0	abcd
1	1	0	1	0	$ab\overline{c}\overline{d}$
1	1	0	1	1	ab c d
1	1	1	1	0	abc d
1	1	1	1	1	abcd
	F		T.		Talala

Four Input Truth Table

iction)				
ab cd	00	01	11	10
00	$\overline{a}\overline{b}\overline{c}\overline{d}$	ā b cq	ābcd₃	ābc
01	āb⊽ <mark>d</mark>	āb⊽d s	ābcd	ābc d
11	$ab\overline{c}\overline{q}_{12}$	ab c d	abcd	abc d
10	abcd	a b cd	abcd 11	$a\overline{b}c\overline{d}_{10}$

- Each square corresponds to a row of the truth table
- Any two adjacent squares differ only in one literal

Columns as well as rows arranged in binary order 00,01,11,10



K-Map Structure (four input Boolean function)

а	Ь	С	d	У	minterm
0	0	0	0	1	ābcd
0	0	0	0	0	$\overline{a}\overline{b}\overline{c}d$
0	0	1	0	1	$\overline{a}\overline{b}c\overline{d}$
0	0	1	0	0	$\overline{a}\overline{b}cd$
0	1	0	0	0	$\overline{a}b\overline{c}\overline{d}$
0	1	0	0	1	ābcd
0	1	1	1	0	$\overline{a}bc\overline{d}$
0	1	1	1	1	ābcd
1	0	0	1	1	$a\overline{b}\overline{c}\overline{d}$
1	0	0	1	0	$a\overline{b}\overline{c}d$
1	0	1	0	1	$a\overline{b}c\overline{d}$
1	0	1	0	0	$a\overline{b}cd$
1	1	0	1	0	$ab\overline{c}\overline{d}$
1	1	0	1	1	ab c d
1	1	1	1	0	abcd
1	1	1	1	1	abcd

Four Input Truth Table

ction)				
ab cd	00	01	11	10
00	$\overline{a}\overline{b}\overline{c}\overline{d}$	ā b cq	a bcd₃	ābcd
01	ābcd	ābcd	ābcd	ābc₫
11	abcd	ab c d	abcd	abc d
10	abcd	a b cd	abcd	$a\overline{b}c\overline{d}_{10}$

- Each square corresponds to a row of the truth table
- Any two adjacent squares differ only in one literal

- Columns as well as rows arranged in binary order 00,01,11,10
- Notion of "wrap-around"
 - Far left and right squares are adjacent
 - Top and bottom squares are also adjacent



K-Map Structure (four input Boolean function)

а	Ь	С	d	У	minterm
0	0	0	0	1	$\overline{a}\overline{b}\overline{c}\overline{d}$
0	0	0	0	0	$\overline{a}\overline{b}\overline{c}d$
0	0	1	0	1	$\overline{a}\overline{b}c\overline{d}$
0	0	1	0	0	$\overline{a}\overline{b}cd$
0	1	0	0	0	$\overline{a}b\overline{c}\overline{d}$
0	1	0	0	1	ābcd
0	1	1	1	0	$\overline{a}bc\overline{d}$
0	1	1	1	1	ābcd
1	0	0	1	1	$a\overline{b}\overline{c}\overline{d}$
1	0	0	1	0	abcd
1	0	1	0	1	$a\overline{b}c\overline{d}$
1	0	1	0	0	abcd
1	1	0	1	0	$ab\overline{c}\overline{d}$
1	1	0	1	1	ab c d
1	1	1	1	0	abc d
1	1	1	1	1	abcd

Four Input Truth Table

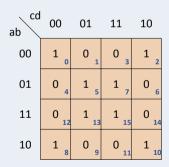
ction)				
ab cd	00	01	11	10
00	1 0	0 1	0 3	1 2
01	0 4	1 5	1 ,	0 6
11	0 12	1 13	1 15	0 14
10	1 8	0 9	0 11	1 10

- Each square corresponds to a row of the truth table
- Any two adjacent squares differ only in one literal

- Columns as well as rows arranged in binary order 00,01,11,10
- Notion of "wrap-around"
 - Far left and right squares are adjacent
 - Top and bottom squares are also adjacent

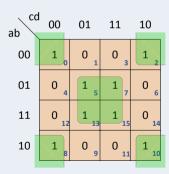


а	Ь	С	d	у
0	0	0	0	1
0	0	0	0	0
0	0	1	0	1
0	0	1	0	0
0	1	0	0	0
0	1	0	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	1	1
1	0	0	1	0
1	0	1	0	1
1	0	1	0	0
1	1	0	1	0
1	1	0	1	1
1	1	1	1	0
1	1	1	1	1
our	Inpu	ıt Trı	uth T	able



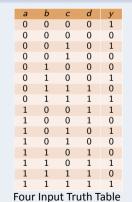


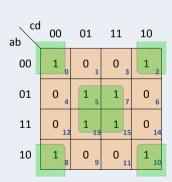
а	Ь	С	d	y
0	0	0	0	1
0	0	0	0	0
0	0	1	0	1
0	0	1	0	0
0	1	0	0	0
0	1	0	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	1	1
1	0	0	1	0
1	0	1	0	1
1	0	1	0	0
1	1	0	1	0
1	1	0	1	1
1	1	1	1	0
1	1	1	1	1
our	Inpu	ıt Trı	uth T	able





K-Map Example (four inputs)

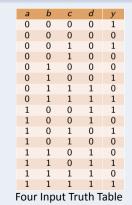


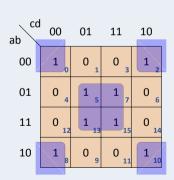


 Two prime implicants



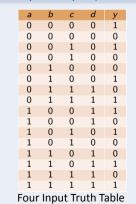
K-Map Example (four inputs)

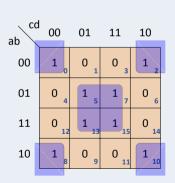




Two prime implicants



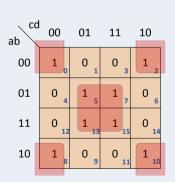




- Two prime implicants
- Two essential prime implicants



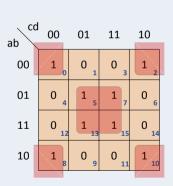
а	Ь	С	d	У
0	0	0	0	1
0	0	0	0	0
0	0	1	0	1
0	0	1	0	0
0	1	0	0	0
0	1	0	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	1	1
1	0	0	1	0
1	0	1	0	1
1	0	1	0	0
1	1	0	1	0
1	1	0	1	1
1	1	1	1	0
1	1	1	1	1



- Two prime implicants
- Two essential prime implicants



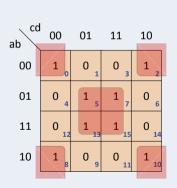
а	Ь	С	d	У
0	0	0	0	1
0	0	0	0	0
0	0	1	0	1
0	0	1	0	0
0	1	0	0	0
0	1	0	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	1	1
1	0	0	1	0
1	0	1	0	1
1	0	1	0	0
1	1	0	1	0
1	1	0	1	1
1	1	1	1	0
1	1	1	1	1



- Two prime implicants
- Two essential prime implicants
- Two required prime implicants: bd, bd



а	Ь	С	d	y
0	0	0	0	1
0	0	0	0	0
0	0	1	0	1
0	0	1	0	0
0	1	0	0	0
0	1	0	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	1	1
1	0	0	1	0
1	0	1	0	1
1	0	1	0	0
1	1	0	1	0
1	1	0	1	1
1	1	1	1	0
1	1	1	1	1



- Two prime implicants
- Two essential prime implicants
- Two required prime implicants: bd, bd
- Minimized Boolean formula: $f(a, b, c, d) = bd + \overline{b} \overline{d}$





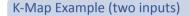
a	b	У
0	0	1
0	1	0
1	0	1
1	1	1





a	b	y
0	0	1
0	1	0
1	0	1
1	1	1

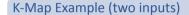




a	b	y
0	0	1
0	1	0
1	0	1
1	1	1

b 0 1 0 1 1 1 1





а	b	y	
0	0	1	
0	1	0	
1	0	1	
1	1	1	

b 0 1 0 1 1 1 1

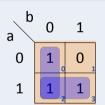
Two prime implicants





a	b	y
0	0	1
0	1	0
1	0	1
1	1	1

Two Input Truth Table

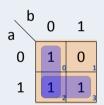


• Two prime implicants



K-Map Example (two inputs)

a	b	У	
0	0	1	
0	1	0	
1	0	1	
1	1	1	

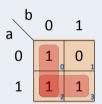


- Two prime implicants
- Two essential prime implicants



K-Map Example (two inputs)

a	b	У	
0	0	1	
0	1	0	
1	0	1	
1	1	1	

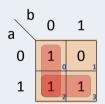


- Two prime implicants
- Two essential prime implicants



K-Map Example (two inputs)

а	b	У
0	0	1
0	1	0
1	0	1
1	1	1

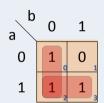


- Two prime implicants
- Two essential prime implicants
- Two required prime implicants



K-Map Example (two inputs)

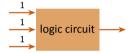
a	Ь	y
0	0	1
0	1	0
1	0	1
1	1	1



- Two prime implicants
- Two essential prime implicants
- Two required prime implicants
- Minimized Boolean formula: $f(a, b, c, d) = \overline{b} + a$

Don't Cares

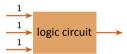
 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



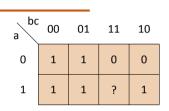


Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



а	Ь	С	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	?



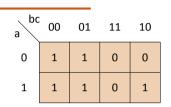


Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



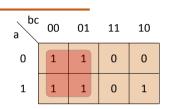


Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



а	Ь	С	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



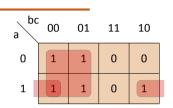


Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



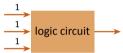
а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0





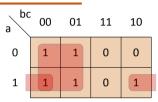
Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



guaranteed can't happen

а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0





PES

Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



guaranteed can't happen

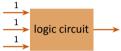
а	Ь	С	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

a bo	00	01	11	10
0	1	1	0	0
1	1	1	1	1

Don't Cares

PES UNIVERSITY

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



guaranteed can't happen

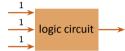
а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

a bo	00	01	11	10
0	1	1	0	0
1	1	1	1	1

PES UNIVERSITY

Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



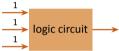
guaranteed can't happen

а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

a bo	00	01	11	10
0	1	1	0	0
1	1	1	1	1

Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



guaranteed can't happen

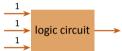
а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

a bc 00 01 11 10 0 1 1 0 0 1 1 1 1

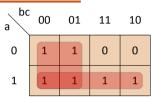
- Case 0: $y = \overline{b} + \overline{c}a$
- Case 1: $y = \overline{b} + a$

Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



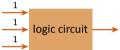
а	Ь	С	У
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



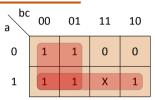
- Case 0: $y = \overline{b} + \overline{c}a$
- Case 1: $y = \overline{b} + a$
- Either 0 or 1 can result in smaller formula

Don't Cares

 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



а	Ь	С	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	X



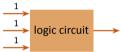
- Case 0: $y = \overline{b} + \overline{c}a$
- Case 1: $y = \overline{b} + a$
- Either 0 or 1 can result in smaller formula
- So initially write X in truth table and K-Map



Don't Cares



 Suppose we are asked to design a three input logic circuit all whose inputs can never be 1 simultaneously



guaranteed can't happen

а	Ь	С	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	X

a bc 00 01 11 10 0 1 1 1 1 X 1

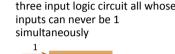
- Case 0: $y = \overline{b} + \overline{c}a$
- Case 1: $y = \overline{b} + a$
- Either 0 or 1 can result in smaller formula
- So initially write X in truth table and K-Map

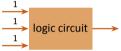
Don't Care

Output(s) we **don't care** about are denoted by X, can be treated as either 0 or 1

Don't Cares

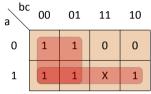






guaranteed can't happen

а	Ь	С	y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	X



- Case 0: $v = \overline{b} + \overline{c}a$
- Case 1: $y = \overline{b} + a$
- Either 0 or 1 can result in smaller formula
- So initially write X in truth table and K-Map

Don't Care

Output(s) we **don't care** about are denoted by X, can be treated as either 0 or 1

Don't Care / X has other use cases, discussed later



Think About It



Minimize using K-Maps

- $f(a,b) = \Sigma(0,1,2,3)$
- $f(a, b, c, d) = \Sigma(0, 1, 5, 7, 15, 14, 10)$

_					
â	3	Ь	С	d	У
C)	0	0	0	0
0)	0	0	0	0
C)	0	1	0	0
C)	0	1	0	0
C)	1	0	0	0
C)	1	0	0	0
C)	1	1	1	0
C)	1	1	1	0
1		0	0	1	1
1		0	0	1	1
1		0	1	0	1
1		0	1	0	Χ

Minimize using K-Maps