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PES UNIVERSITY

PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

UE 17 / 18
CS253

DECEMBER 2020: END SEMESTER ASSESSMENT (ESA) B TECH IV SEMESTER

UE17/ UE18CS253- Microprocessors & Computer Architecture

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Differentiate the following i. Microprocessors and Microcontroller. ii. Computer Organization and Computer Architecture. iii. RISC and CISC.	06
	b)	Write assembly language program to search for an element using linear search, where the elements are stored in memory locations.	06
	c)	Given a C code convert it in to its equivalent Arm Code. Note: x,a,b,c,z are memory locations. i) x = (a + b) – c; ii) z = (a << 2) |(b & 15);	05
	d)	Mention the 3 - addressing modes used in ARM instruction set architecture	03
2	a)	What is a hazard. How will you classify it ? Explain any one of the hazard with an example.	05
	b)	Consider the unpipelined processor . Assume that it has a 1ns clock cycle and that it uses 4 cycles for ALU operations and branches, and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20%, and 40%, respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline?	05
	c)	How data hazards are minimized using data forwarding in a 5 stage pipeline architecture? Explain with an Example.	05
	d)	Consider the following RISC assembly code. load r1,45(r2) (1) add r7 <- r1, r5 (2) sub r8 <- r1, r6 (3) or r9 <- r5, r1 (4) brneq r7, target (5) add r10 <- r8, r5 (6) xor r2 <- r3, r4 (7) Identify each dependence; list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved (register or memory).	05
3.	a)	Consider a 8-way set associative cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find the Size of main memory.	05
	b)	Find the average memory access time for a processor given the following: - The clock rate is 1 ns	5

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		- The miss penalty is 30 clock cycles - 2% of instructions are not found in the cache. - 5% of data references are not found in the cache - 15% of memory accesses are for data. - The memory system has a cache access time (including hit detection) of 1 clock cycle. - Assume that the read and write miss penalties are the same and ignore other write stalls.	
	c)	Explain the following: i. Write-through. ii. Copy-back (also known as write-back).	05
	d)	What are the different types of cache misses? Explain any one of them.	05
4.	a)	"Multi level cache reduces miss penalty". Justify the statement with an example.	05
	b)	Write a note on DMA.	05
	c)	Write a note on Flynn's Classification of parallel computing. And Explain any one classification with an example.	06
	d)	Explain the following techniques i. Polling ii. Daisy Chain Technique	04
5.	a)	Write the limitations of serial computing and the applications of parallel computing.	05
	b)	What is instruction level parallelism ? Explain with an example.	05
	c)	What is Cache Coherency? Explain with an example.	05
	d)	Mention the limitations of ILP.	05