QUESTIONS UNIT 3

1. Explain the challenges, requirements and solutions for memory design. What are the recent advancement in this area?

2. Explain with example and justify your answer why Fully Associative mapping cache is faster than Direct mapping. Explain with example and justify your answer why Set Associative mapping is faster than Direct mapping.

3. Explain the challenges, requirements and solutions for Cache memory design. What are the recent advancement in this area?

   Reference:
   (http://www.academia.edu/Documents/in/Cache_Memory_Design_Issues)
   Note: Do not copy as is given from the reference.

4. Cache Coherence is challenging in Multicore era. Explain the Challenges, requirements and elaborate one solution for the same.

5. Explain the issues in designing Multilevel Cache on Uniprocessor environment.
   a. **Reference 1: https://ieeexplore.ieee.org/document/331852**
   b. **Reference 2: https://www.researchgate.net/publication/329446520_A_Multilevel_Cache_Management_Policy_for_Performance_Improvement_in_Distributed_System**
   c. **Note: Do not copy as is given from the reference.**

6. Explain the issues in designing Multilevel Cache in Multiprocessor environment
   a. **Reference: https://www.sciencedirect.com/science/article/abs/pii/0743731589900014**
   b. **Note: Do not copy as is given from the reference.**

7. Explain the replacement policies used in cache design. Perform detail survey and explain their contribution w.r.t performance and power consumption.

   a. **Reference: https://ieeexplore.ieee.org/document/7806218**
   b. **Note: Do not copy as is given from the reference.**

8. Discuss Capacity Miss in detail w.r.t Cause, effect on performance, solutions and advancement in the area of multicore with an example.

9. Discuss Compulsory Miss in detail w.r.t Cause, effect on performance, solutions and advancement in the area of multicore with an example.

10. Discuss Conflict Miss in detail w.r.t Cause, effect on performance, solutions and advancement in the area of multicore with an example.

11. Discuss the Write through policy in multilevel cache environment (L1 Private & L2 Public) w.r.t Design principles, Challenges and Performance with an example. You can take any configuration example: L1 Private & L2 Public. Or L1 & L2 Private and L3 is public.

12. Discuss the Write Back policy in multilevel cache environment w.r.t Design principles, Challenges and Performance with an example. You can take any configuration example: L1 Private & L2 Public. or L1 & L2 Private and L3 is public.

13. Discuss the Cache Architecture of ARM processor i: Philosophy ii: Design iii: Read and Write Policy iv: Optimizations. You can select ARM processor of your choice example: ARM940T.

14. Discuss the Philosophy and working of Von Neumann cache and Harvard Cache w.r.t Need of shift from Von Neumann design, Performance, Pros and Cons. Give the Diagram, Equations and an example.

15. Discuss the Prefetching process w.r.t Performance, Correctness, Predictions, Compiler Contribution, and dynamic prefetching with examples where ever necessary.

   a. **Reference 1: Jouppi, "Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers, " ISCA 1990.**

b. **Reference 2: Joseph and Grunwald, "Prefetching using Markov Predictors, " ISCA 1997.**
c. **Reference 3: Mowry et al., "Design and Evaluation of a Compiler Algorithm for Prefetching , " ASPLOS 1992.**
d. **Note: Do not copy as is given from the reference.**

16. Discuss Locality of reference with examples. Extend your discussion to parallel processing.
    a. **Reference**
    b. **1: https://link.springer.com/referenceworkentry/10.1007%2F978-0-387-09766-4_206**
    c. **Note: Do not copy as is given from the reference.**

17. Explain how the principle of locality has led to hierarchies based on memory of different speeds and sizes.

18. Explain how memory hierarchy design becomes crucial for the recent multicore processors.

19. Explain the reason why it takes longer time to retrieve a block of data from main memory compared to the time taken to retrieve data when the cache acts as a bridge between main memory and the CPU

20. Explain why the WRITE THROUGH cache write mechanism creates more bus traffic?

21. Why is a refresh cycle necessary for a dynamic RAM?

22. List and explain which technique extends the storage capacities of main memory beyond the actual size of the main memory.

23. Explain how the L2 cache memory structure gives an advantage of reduction in delay to access RAM on the motherboard?

24. Give the reason why for a memory system, the cycle time is longer than the access time.

25. Consider the situation for a k-way set associative cache which is divided into v sets. Each set consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. Describe the procedure how the main memory block numbered j is mapped to cache lines.

26. Explain why the difference between processor and memory speeds is a major obstacle towards achieving good performance.

27. Explain the need for a mapping function which can determine which blocks in the main memory are in the cache.

28. Explain the process to identify whether a given block is present in the cache or not?

29. Elaborate on how block replacement algorithms are essential to determine which block should be replaced on a cache miss?

30. Explain why for a direct mapped cache, the miss rate may go up due to possible increase of mapping conflicts?

31. Explain why local cache miss rate is not a good measure of secondary caches.

32. Differentiate between the need for the use of an inclusive cache versus the need for an exclusive cache.

33. Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

34. Consider a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find the Size of main memory.

35. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory.

36. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory.

37. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.
    (a)Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.
    (b) When a program is executed, the processor reads data sequentially from the following word addresses: **128, 144, 2176, 2180, 128, 2176**
    All the above addresses are shown in decimal values. Assume that the cache is initially empty.
    For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

38. Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

39. Consider a 8-way set associative cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find the Size of main memory.

40. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory

41. Consider a 4 way set associative cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory

42. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a 2-way set associative manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

43. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

    (b) When a program is executed, the processor reads data sequentially

from the following word addresses: **128, 144, 2176, 2180, 128, 2176**

All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.