PES UNIVERSITY

QUESTION BANK

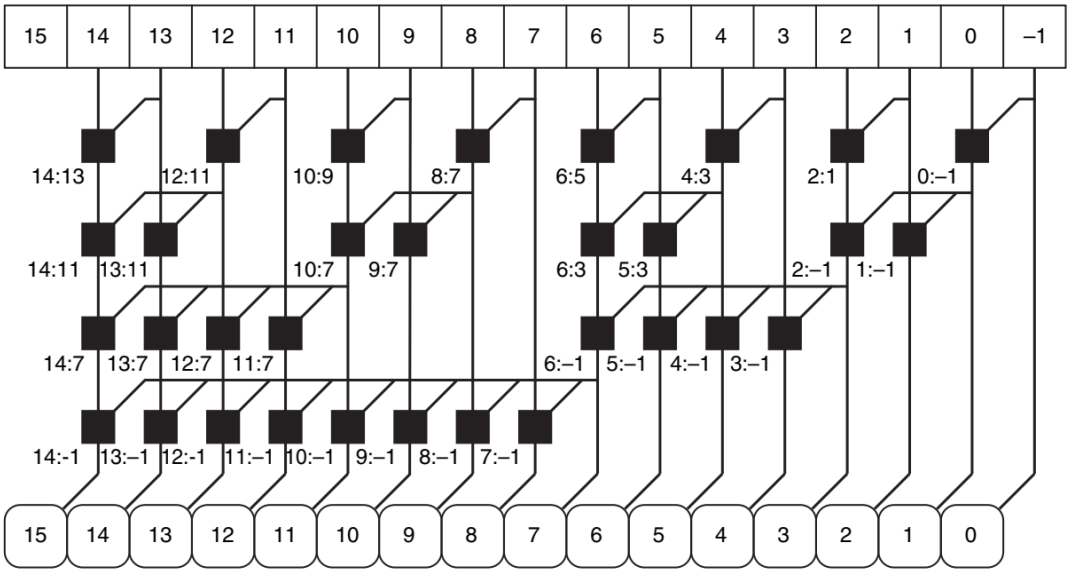
UNIT 3: Carry lookahead Adders

1. What is the delay for the following types of 64-bit adders? Assume that each two-input gate delay is 150 ps and that a full adder delay is 450 ps.
   (a) a ripple-carry adder
   (b) a carry-lookahead adder with 4-bit blocks
   (c) a prefix adder

2. Design two adders: a 64-bit ripple-carry adder and a 64-bit carrylookahead adder with 4-bit blocks. Use only two-input gates. Each two-input gate is 15 µm2, has a 50 ps delay, and has 20 fF of total gate capacitance. You may assume that the static power is negligible.
   (a) Compare the area, delay, and power of the adders (operating at 100 MHz and 1.2 V).
   (b) Discuss the trade-offs between power, area, and delay.

3. Explain why a designer might choose to use a ripple-carry adder instead of a carry-lookahead adder.

4. The prefix network shown in Figure uses black cells to compute all of the prefixes. Some of the block propagate signals are not actually necessary.
   Design a "gray cell" that receives G and P signals for bits i:k and k-1:j but produces only Gi:j, not Pi:j. Redraw the prefix network, replacing black cells with gray cells wherever possible



UNIT 3: COUNTERS

1. Build a 32-bit synchronous Up/Down counter. The inputs are Reset and Up. When Reset is 1, the outputs are all 0. Otherwise, when Up = 1, the circuit counts up, and when Up = 0, the circuit counts down.

2. Design a 32-bit counter that adds 4 at each clock edge. The counter has reset and clock inputs. Upon reset, the counter output is all 0.

3. Modify the counter from Exercise 2 such that the counter will either increment by 4 or load a new 32-bit value, D, on each clock edge, depending on a control signal Load. When Load = 1, the counter loads the new value D.

4. A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if
   (a) the normal outputs of the flip-flops are connected to the clock and
   (b) the complement outputs of the flip-flops are connected to the clock?

5. Draw the logic diagram of a four-bit binary ripple countdown counter using
   (a) flip-flops that trigger on the positive-edge of the clock and
   (b) flip-flops that trigger on the negative-edge of the clock.

6. Design a four-bit binary synchronous counter with *D* flip-flops.

7. A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if

(a) the normal outputs of the flip-flops are connected to the clock and
(b) the complement outputs of the flip-flops are connected to the clock?

8. Draw the logic diagram of a four-bit binary ripple countdown counter using
   (a) flip-flops that trigger on the positive-edge of the clock and
   (b) flip-flops that trigger on the negative-edge of the clock

UNIT 3: FINITE STATE MACHINES

1. You are designing an FSM to keep track of the mood of four students working in the digital design lab. Each student's mood is either HAPPY (the circuit works), SAD (the circuit blew up), BUSY (working on the circuit), CLUELESS (confused about the circuit), or ASLEEP (face down on the circuit board). How many states does the FSM have? What is the minimum number of bits necessary to represent these states?

2. How would you factor the FSM from question 1 into multiple simpler machines? How many states does each simpler machine have? What is the minimum total number of bits necessary in this factored design?

3. Describe in words what the state machine in the following figure does. Using
   binary state encodings, complete a state transition table and output table for the
   FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

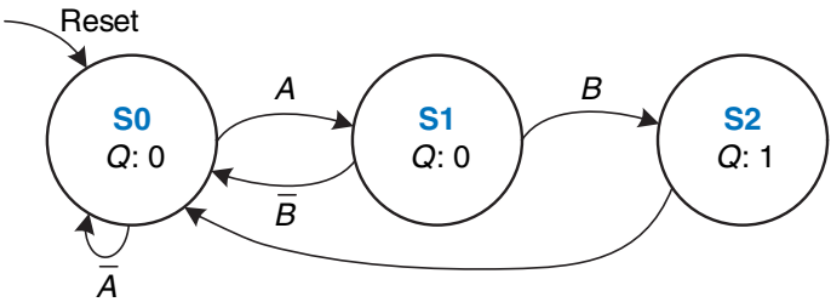


Figure: State transition diagram

4. Describe in words what the state machine in the following figure does. Using
binary state encodings, complete a state transition table and output table for the
FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

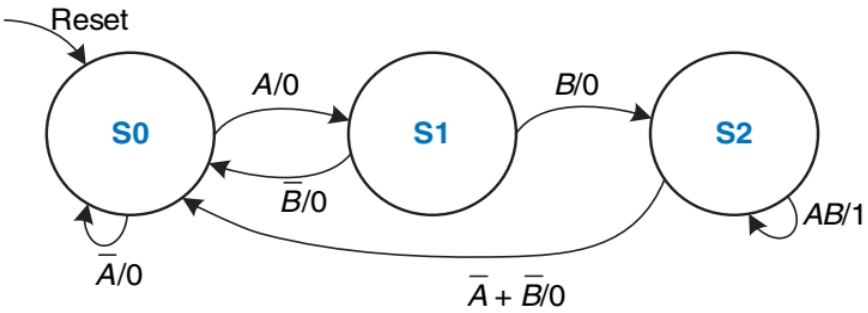


Figure: State transition diagram

5. Accidents are still occurring at the intersection of Academic Avenue and Bravado Boulevard. The football team is rushing into the intersection the moment light B turns green. They are colliding with sleep-deprived CS majors who stagger into the intersection just before light A turns red. Extend the traffic light controller so that both lights are red for 5 seconds before either light turns green again. Sketch your improved Moore machine state transition diagram, state encodings, state transition table, output table, next state and output equations, and your FSM schematic.

6. Alyssa P. Hacker's snail has a daughter with a Mealy machine FSM brain. The daughter snail smiles whenever she slides over the pattern 1101 or the pattern 1110. Sketch the state transition diagram for this happy snail using as few states as possible. Choose state encodings and write a combined state transition and output table using your encodings. Write the next state and output equations and sketch your FSM schematic.

7. Gray codes have a useful property in that consecutive numbers differ in only a single bit position. Table 1 lists a 3-bit Gray code representing the

numbers 0 to 7. Design a 3-bit modulo 8 Gray code counter FSM with no inputs and three outputs. (A modulo N counter counts from 0 to N - 1, then repeats. For example, a watch uses a modulo 60 counter for the minutes and seconds that counts from 0 to 59.) When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000.

Table 1 3-bit Gray code

Number	Gray code		
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

8. Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Zn, is either the Boolean AND or OR of the corresponding input An and the previous input An-1, depending on the other input, Bn:

   Zn = An An-1 if Bn = 0

   Zn = An + An-1 if Bn = 1

   (a) Sketch the waveform for Z given the inputs shown in figure.
   (b) Is this FSM a Moore or a Mealy machine?

(c) Design the FSM. Show your state transition diagram, encoded state transition

table, next state and output equations, and schematic.

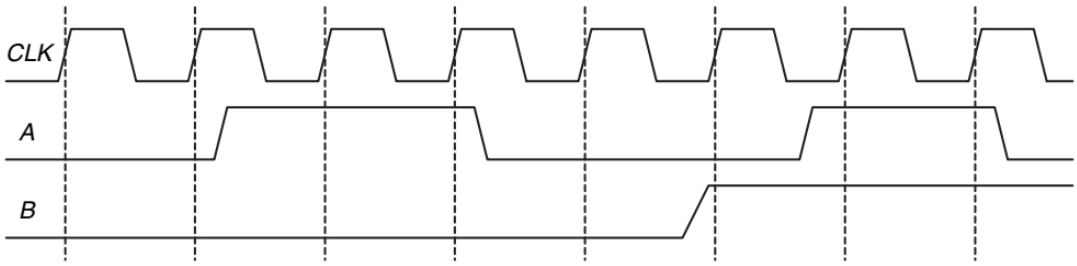


Figure. FSM input waveforms

9. Design an FSM with one input, A, and two outputs, X and Y. X should be 1 if A has been 1 for at least three cycles altogether (not necessarily consecutively). Y should be 1 if A has been 1 for at least two consecutive cycles. Show your state transition diagram, encoded state transition table, next state and output equations, and schematic

10. Analyze the FSM shown in Figure. Write the state transition and output tables and sketch the state transition diagram. Describe in words what the FSM does.

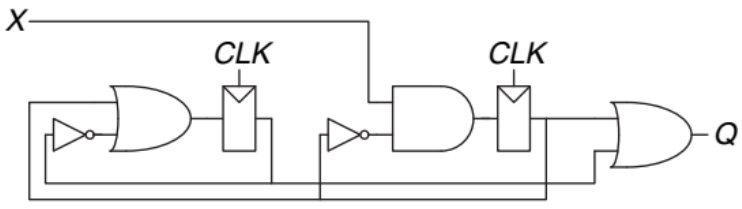


Figure : FSM schematic

UNIT 3 MEMORY ARRAYS

1. Flash EEPROM, simply called Flash memory, is a fairly recent invention that has revolutionized consumer electronics. Research and explain how Flash memory works. Use a diagram illustrating the floating gate. Describe how a bit in the memory is programmed. Properly cite your sources.

2. Implement the following functions using a single 16 × 3 ROM. Use dot notation to indicate the ROM contents.

   (a) $X = AB + B\overline{C}D + \overline{A}\,\overline{B}$

   (b) $Y = AB + BD$

   (c) $Z = A + B + C + D$

3. Implement the functions from Exercise 2 using a 4 × 8 × 3 PLA. You may use dot notation.

4. The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and input–output data lines are needed in each case?

(a) 8K x 16	(b) 2G x 8
(c) 16M x 32	(d) 256K x 64