PES UNIVERSITY

Unit 2 assignment 3

1	Explain Structural hazard with an example?
2	What is control hazard ? Explain with an example?
3	When a branch instruction occurs in a pipeline in the form of an exception (interrupt), what additional hardware is required to overcome the hazard. Which architecture supports the same. What is done to the 5 stage pipeline to reduce two stall cycles?
4	What is delayed branch in pipeline?
5	What is delay slot in pipelining?
6	What is ment by branch prediction?
7	What are the different techniques for branch prediction?
8	What is static branch prediction?
9	What is dynamic branch prediction?
10	Consider the following RISC assembly code. load r1,45(r2) (1) add r7 <- r1, r5 (2) sub r8 <- r1, r6 (3) or r9 <- r5, r1 (4) brneq r7, target (5) add r10 <- r8, r5 (6) xor r2 <- r3, r4 (7) Identify each dependence; list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved (register or memory).
11	What is branch branch penalty?

12	How the branch delay slot will occur?