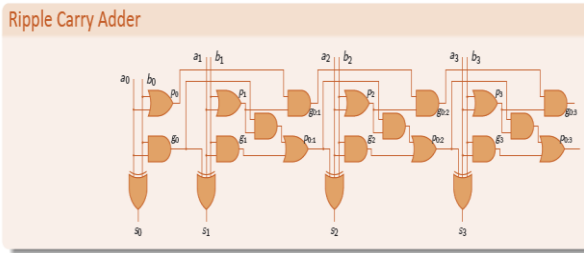



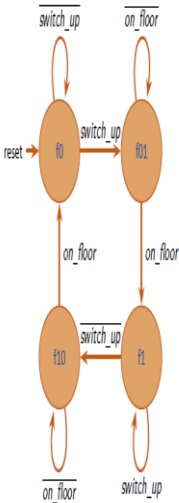
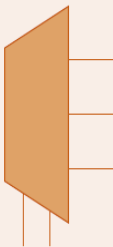
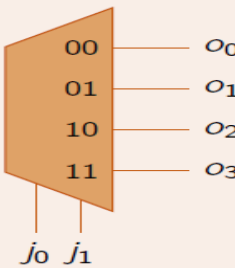
PES UNIVERSITY
3rd SEMESTER

Errata for
DIGITAL DESIGN AND COMPUTER ORGANISATION
Slides Uploaded to PESU ACADEMY Portal

Errata Last updated 27th October 2020

This list is a work in progress. Some of the following corrections may be revised, and additional corrections will probably be added.

Sl. No	Lecture Number	Content in the slide	To be Corrected as
1.	UNIT3 Lecture 34 Slide 16	<p>CARRY-LOOKAHEAD AND PREFIX ADDERS - 4 Associative Ripple Carry?</p>  <ul style="list-style-type: none"> • $c_{i+1} = ab + bc_i + c_i a$ • Generate and Propagate: <ul style="list-style-type: none"> ▶ g_i carry generated in position i ▶ p_i carry propagated in position i ▶ $g_{0:i}$ carry generated in positions 0 to i ▶ $p_{0:i}$ carry propagated in positions 0 to i • $g_i = a_i b_i$ • $p_i = a_i + b_i$ • $g_{0:i+1} = g_i + p_i g_{0:i}$ • $p_{0:i+1} = p_i p_{0:i}$ 	In the figure the labels $p_{0:i}$ and $g_{0:i}$ need to be interchanged.
2.	UNIT3 Lecture 31 Slide 5	<ul style="list-style-type: none"> • Time requirements: For an n-bit ripple carry adder, critical path delay is composed of: <ul style="list-style-type: none"> ▶ Propagation delay from c_0 to c_{n-1} <ul style="list-style-type: none"> ★ Signal passes through two gates in each of the $n - 1$ stages ★ $2(n - 1)t_g$ time required ▶ Sum computation <ul style="list-style-type: none"> ★ $2t_g$ time required for three input XOR gate • An n-bit ripple carry adder thus occupies $2nt_g$ time 	Propagation delay from c_0 to $c_{(n-1)}$ should be $3(n-1)t_g$ instead of $2(n-1)t_g$ because although the carry signal passes through two gates in each stage, one of the gates has three inputs which counts as two 2 input gates..

3.	UNIT3 Lecture 31 Slide 34,35	<div>CARRY-LOOKAHEAD AND PREFIX ADDERS - 1</div> <div>Performance Comparison</div> <div><ul style="list-style-type: none">Area and time estimates for n-bit adders:<table><thead><tr><th></th><th>Area</th><th>Time</th></tr></thead><tbody><tr><td>Ripple carry</td><td>$7na_g$</td><td>$2nt_g$</td></tr><tr><td>Carry-lookahead</td><td>$(n^2 + 5n)a_g$</td><td>$2\lceil \log_2(n - 1) \rceil t_g + 3t_g$</td></tr></tbody></table><ul style="list-style-type: none">Compared to the ripple carry adder's linear delay increase with size, the carry-lookahead adder delay increase only logarithmically, resulting in dramatically faster addersHowever, the area of the carry-lookahead adder increase quadratically with sizeIs there an adder design that retains the carry-lookahead adder's speed but has significantly lesser area?</div> <div></div> <div>$\log_2(n-1)$ should be replaced by $\log_2(n)$.</div>		Area	Time	Ripple carry	$7na_g$	$2nt_g$	Carry-lookahead	$(n^2 + 5n)a_g$	$2\lceil \log_2(n - 1) \rceil t_g + 3t_g$																																																																																																																																																																											
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4.	UNIT3 Lecture 24 Slide 42 till Slide 83	<div></div> <div>Elevator Example State Transition Table</div> <table><thead><tr><th colspan="4">Current State</th><th colspan="2">Inputs</th><th colspan="4">Next State</th></tr><tr><th>s_3</th><th>s_2</th><th>s_1</th><th>s_0</th><th>switch_up</th><th>on_floor</th><th>s'_3</th><th>s'_2</th><th>s'_1</th><th>s'_0</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></tbody></table> <div><p>on_first should be equal to 1 in state 3(0100) instead of the incorrectly mentioned on_first should be equal to 1 in state 4(1000)</p><p>'lift_down' be 1 in state 4 (1000) according to the state diagram</p></div>	Current State				Inputs		Next State				s_3	s_2	s_1	s_0	switch_up	on_floor	s'_3	s'_2	s'_1	s'_0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	1	1	0	0	0	1
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5.	UNIT 2, Lecture 14 Slide 20	<div>1:3 Decoder</div> <div></div>	To be corrected as 2:3 decoder																																																																																																																																																																																			
6.	UNIT 2 Lecture 14 Slide 12-16	<div>1:4 Decoder</div> <div>1:4 Decoder</div> <div><ul style="list-style-type: none">1:4 decoder symbol:</div> <div></div>	To be corrected as 2:4 decoder																																																																																																																																																																																			

7.	UNIT1, Lecture 3, Slide 12	<table><tr><th><i>a</i></th><th><i>b</i></th><th><i>c</i></th><th><i>y</i></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> <p>Truth table</p>	<i>a</i>	<i>b</i>	<i>c</i>	<i>y</i>	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1	1	0	0	0	1	0	1	1	1	1	0	1	1	1	1	1	<table><tr><th><i>a</i></th><th><i>b</i></th><th><i>c</i></th><th><i>Y</i></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	<i>a</i>	<i>b</i>	<i>c</i>	<i>Y</i>	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	1	0	1	1	1	1	1																																																																																																		
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8.	UNIT1, Lecture 4, Slide 13	<p>Boolean Algebra</p> <ul style="list-style-type: none">1 Set {0, 1}2 Operations AND, OR, NOT3 Identity elements 0 (for AND), 1 (for OR)4 Laws/Identities Commutative, associative, distributive, ...	<p>Set f0; 1g</p> <p>Operations AND, OR, NOT</p> <p>Identity elements 1 (for AND), 0 (for OR)</p> <p>Laws/Identities Commutative, associative, distributive:</p>																																																																																																																																																																										
9.	UNIT1, Lecture 8 Slide 4 till Slide 16,Also same error in Slide 40	<table><tr><th><i>a</i></th><th><i>b</i></th><th><i>c</i></th><th><i>d</i></th><th><i>y</i></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> <p>Four Input Truth Table</p>	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>y</i>	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	0	1	1	1	0	0	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	1	1	0	1	0	0	1	1	0	1	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	<table><tr><th><i>a</i></th><th><i>b</i></th><th><i>c</i></th><th><i>d</i></th><th><i>y</i></th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>y</i>	0	0	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	0	0	1	0	1	0	1	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0	1	1	1	1	1	0	0	1	1	1	1	1
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			The min terms for table are $F(a, b, c, d) = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$
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