Digital Design and Computer Organization

Gate/Wire Delays, Timing

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

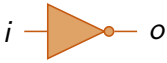
- Digital Design
  - Combinational logic design
    - ★ **Gate/Wire Delays, Timing**
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Propagation Delay
- Timing Diagram
- Critical Path

Gate/Wire Delays, Timing

Delay



Gate/Wire Delays, Timing

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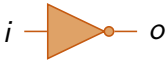

Propagation Delay of a Gate

Propagation delay (t_{pd}) of gate is the time required for the output to change after an input has changed

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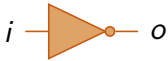

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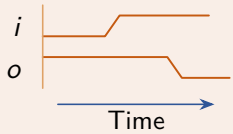

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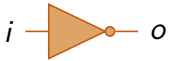

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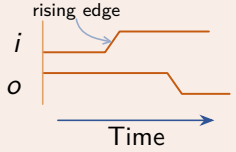

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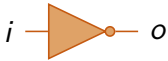

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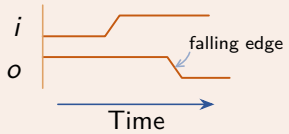

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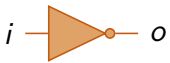

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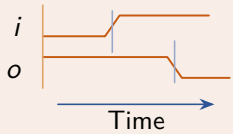

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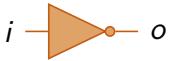

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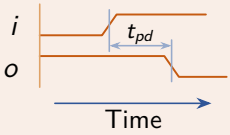

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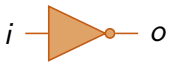

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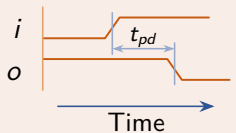
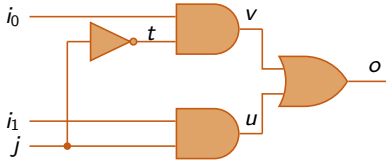


Critical Path Delay or Propagation Delay of a Logic Circuit

In a combinational logic circuit, there are typically multiple **paths** from input to output. A path along which the delay is maximum is called the **critical path** and the delay is called the **critical path delay** or the propagation delay for the logic circuit

Gate/Wire Delays, Timing

Delay Example



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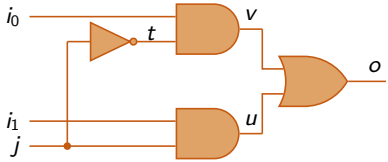

- Assume $t_{pd} = 100$ps for each gate

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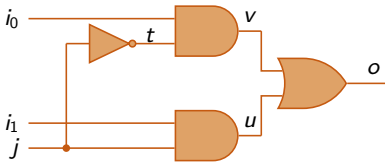

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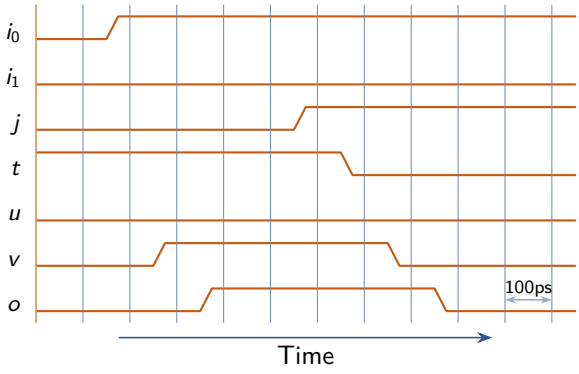

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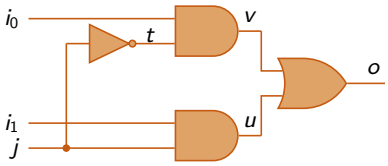

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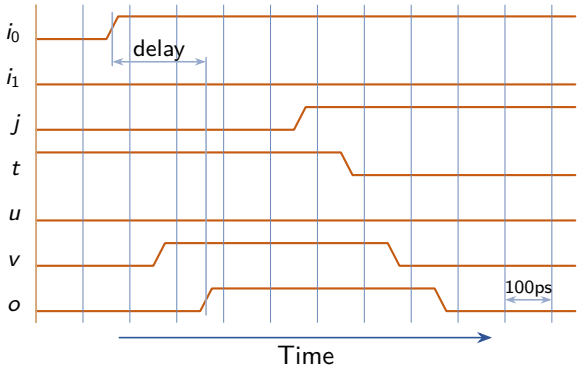

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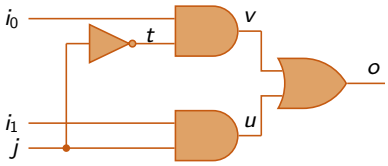

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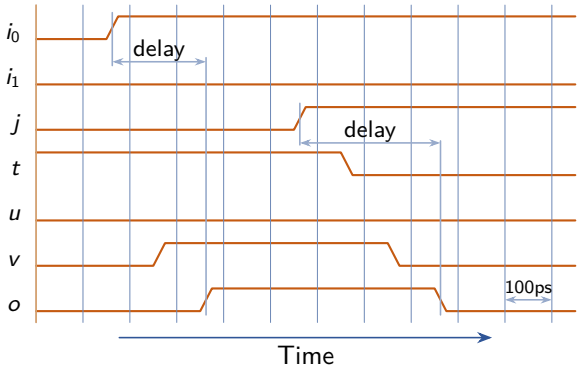

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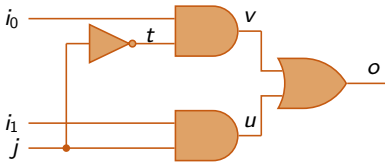
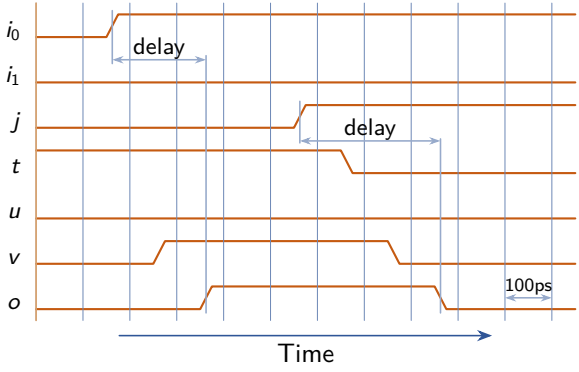


- Assume $t_{pd} = 100$ps for each gate
- Critical path: j, t, v, o
  - Through NOT, AND and OR gates



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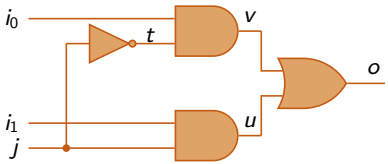
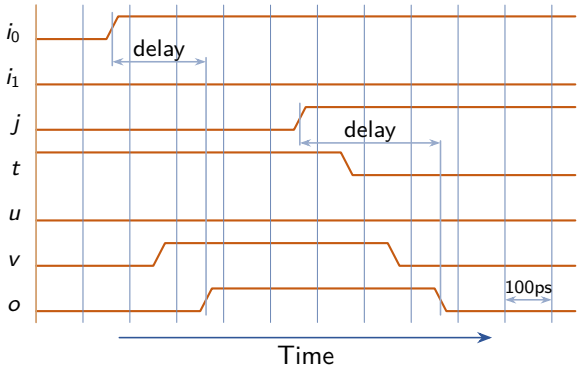


- Assume $t_{pd} = 100$ps for each gate
- Critical path: j, t, v, o
  - Through NOT, AND and OR gates
- Critical path delay (three gates): 300ps



Wire Delay

- Wires connecting gates also have a finite delay, but wire delay outside the scope of this course

Think About It

- Critical path delay of example 2:1 mux circuit: 300ps
- How many input changes can the logic circuit perform in one second?