OPERATING SYSTEMS

Memory Management

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- Structure of the Page Table

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Slides Credits for all PPTs of this course

- The slides/diagrams in this course are an **adaptation**, **combination**, and **enhancement** of material from the following resources and persons:

1. Slides of Operating System Concepts, Abraham Silberschatz, Peter Baer Galvin, Greg Gagne - 9th edition 2013 and some slides from 10th edition 2018
2. Some conceptual text and diagram from Operating Systems - Internals and Design Principles, William Stallings, 9th edition 2018
3. Some presentation transcripts from A. Frank – P. Weisberg
4. Some conceptual text from Operating Systems: Three Easy Pieces, Remzi Arpaci-Dusseau, Andrea Arpaci Dusseau

Structure of the Page Table

- Memory structures for paging can get huge using straight-forward methods
  - Consider a 32-bit logical address space as on modern computers
  - Page size of 4 KB (2^{12})
  - Page table would have 1 million entries (2^{32} / 2^{12})
  - If each entry is 4 bytes -> 4 MB of physical address space / memory for page table alone
    - That amount of memory used to cost a lot
    - Don't want to allocate that contiguously in main memory
- Hierarchical Paging
- Hashed Page Tables
- Inverted Page Tables

Hierarchical Page Tables

- Break up the logical address space into multiple page tables
- A simple technique is a two-level page table
- We then page the page table

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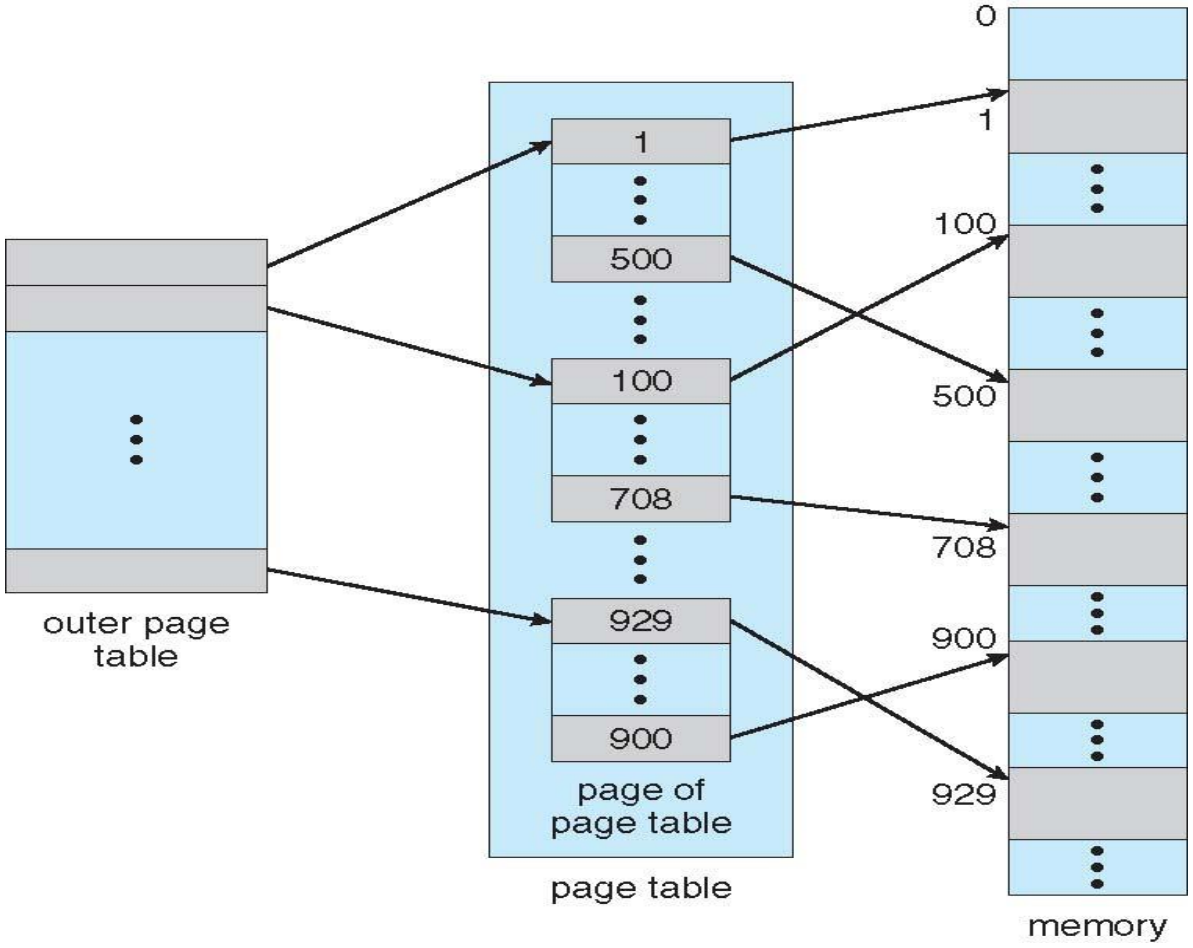
Two-Level Page-Table Scheme



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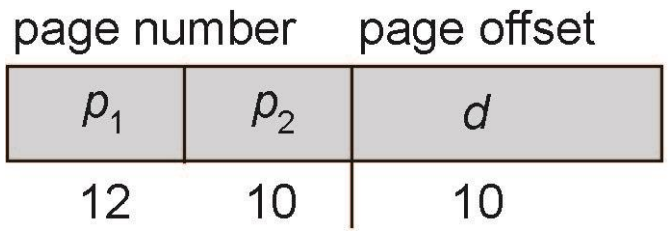
Two-Level Paging Example

- A logical address (on 32-bit machine with 1K page size) is divided into:
  - a page number consisting of 22 bits
  - a page offset consisting of 10 bits
- Since the page table is paged, the page number is further divided into:
  - a 12-bit page number
  - a 10-bit page offset
- Thus, a logical address is as follows:



where p_1 is an index into the outer page table, and p_2 is the displacement within the page of the inner page table

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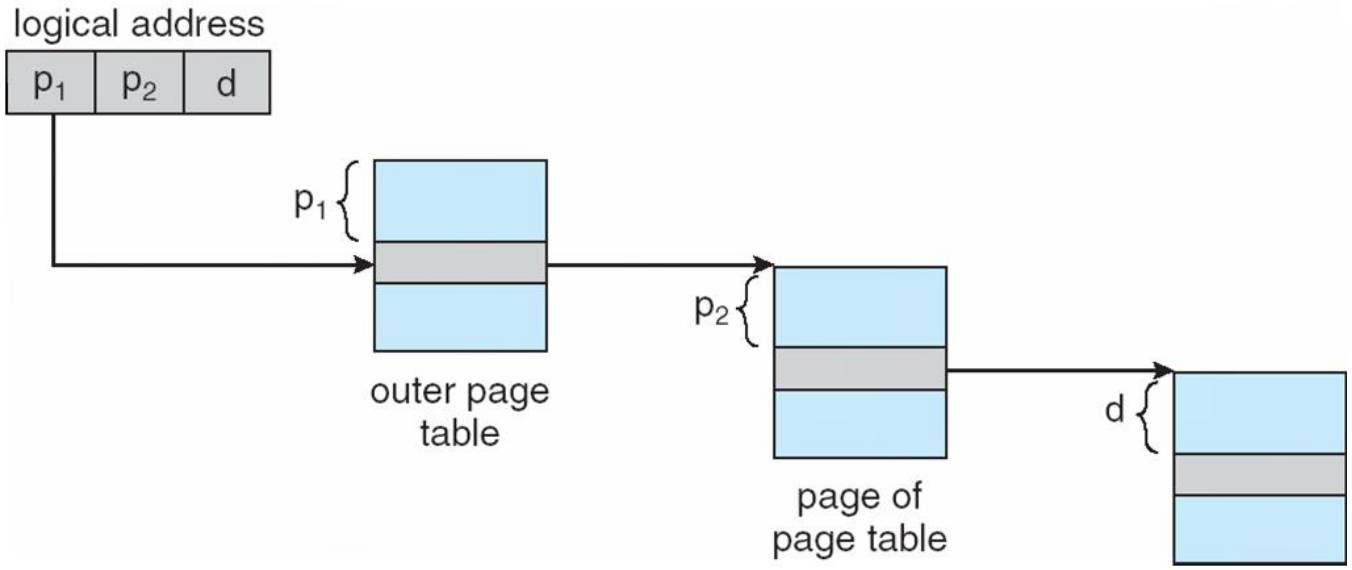
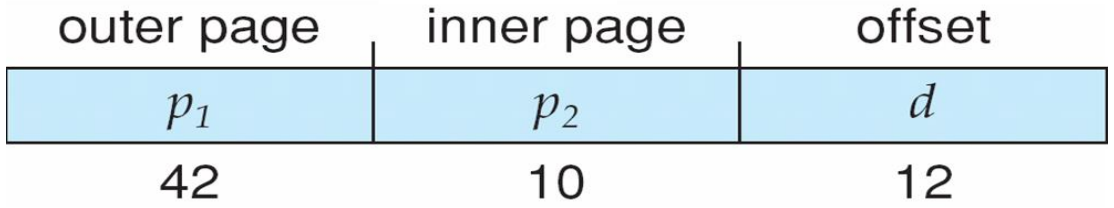
Address-Translation Scheme

- This scheme is known as **forward-mapped page table as** address translation works from the outer page table inward.



64-bit Logical Address Space

- Even two-level paging scheme not sufficient
- If page size is 4 KB (2^{12})
  - Then page table has 2^{52} entries
  - If two level scheme, inner page tables could be 2^{10} 4-byte entries
  - Address would look like



  - Outer page table has 2^{42} entries or 2^{44} bytes
  - One solution is to add a 2^{nd} outer page table

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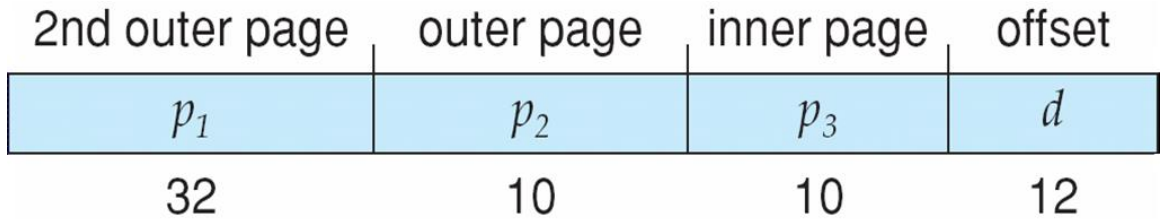
Three-level Paging Scheme

- We can divide the outer page table in various ways.
- For example, we can page the outer page table, giving us a three-level paging scheme. Suppose that the outer page table is made up of standard-size pages (2^{10} entries, or 2^{12} bytes).
- In this case, a 64-bit address space is still daunting:



The outer page table is still 2^{34} bytes (16 GB) in size. And possibly 4 memory access to get to one physical memory location

- The next step would be a four-level paging scheme, where the second-level outer page table itself is also paged, and so forth.
- The 64-bit UltraSPARC would require seven levels of paging—a prohibitive number of memory accesses— to translate each logical address. So, for 64-bit architectures, hierarchical page tables are generally considered inappropriate.

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Hashed Page Tables

- Common in address spaces > 32 bits
- The virtual page number (VPN) is hashed into a page table
  - Each entry in the page table contains a linked list of elements that hash to the same location (to handle collisions)
- Each element contains three fields: (1) the virtual page number (2) the value of the mapped page frame (3) a pointer to the next element
- Virtual page numbers are compared (with field 1) in this chain searching for a match
  - If a match is found, the corresponding physical frame (field 2) is extracted
  - If there is no match, subsequent entries in the linked list are searched for a matching VPN

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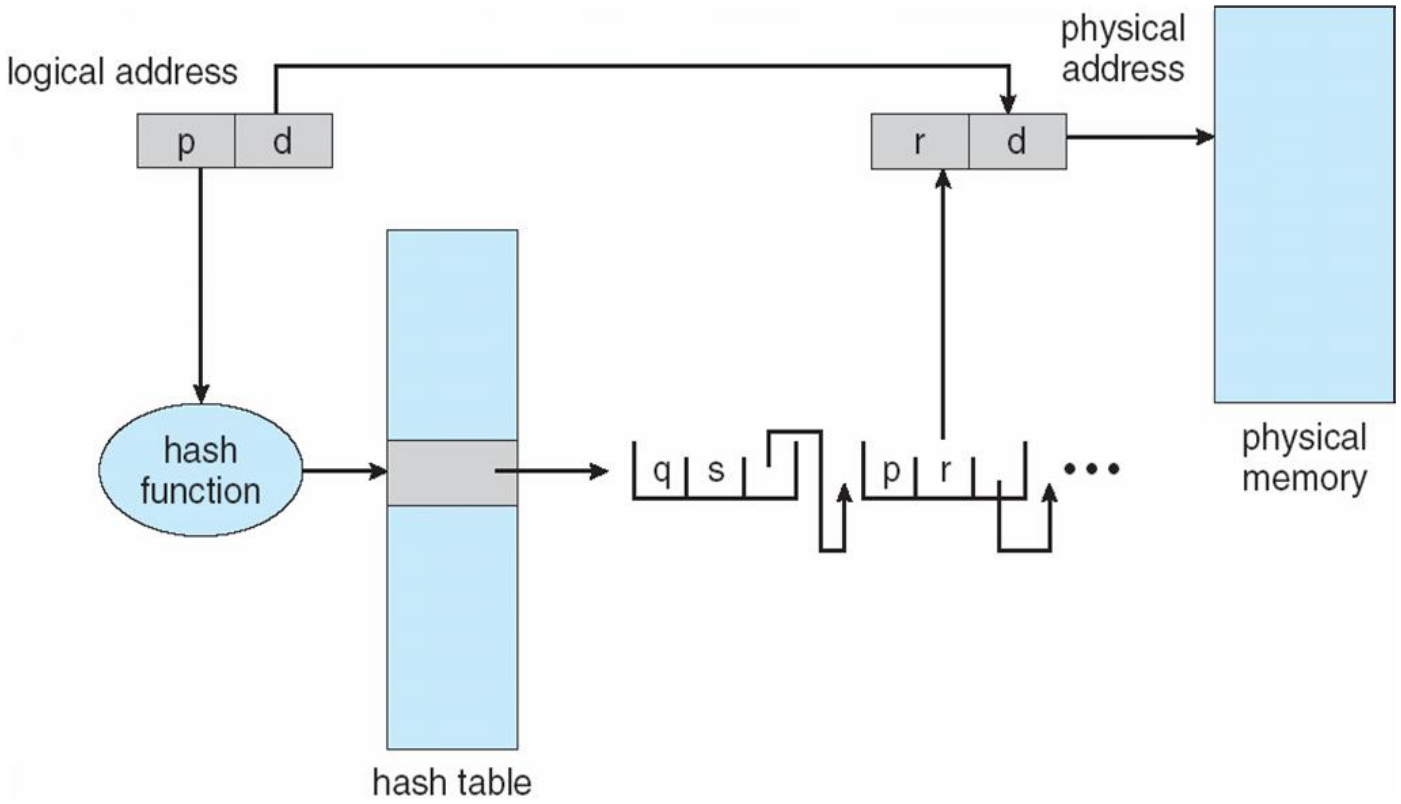
Hashed Page Table



THANK YOU

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