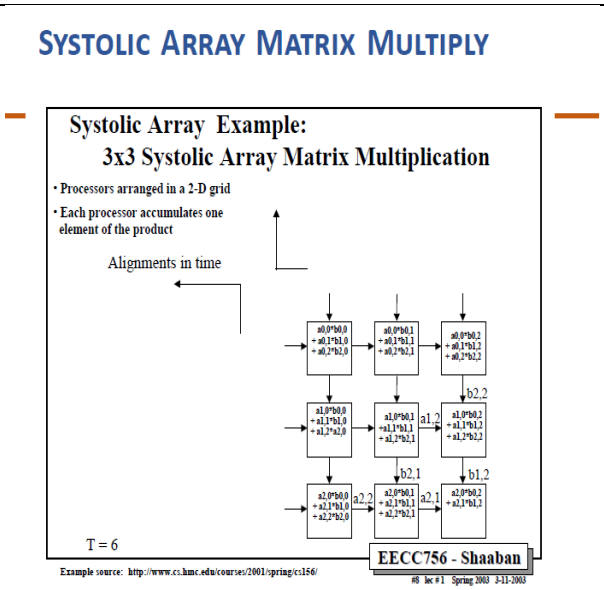
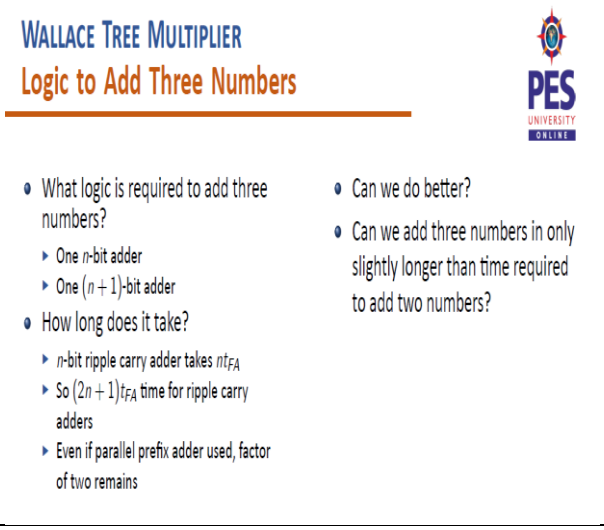
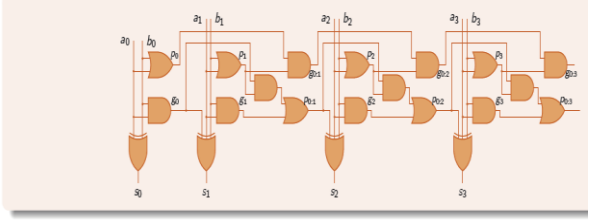
PES UNIVERSITY
3rd SEMESTER

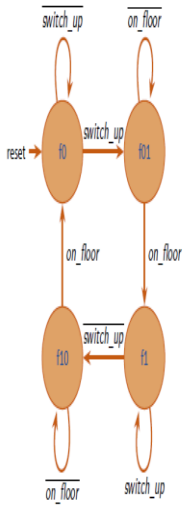
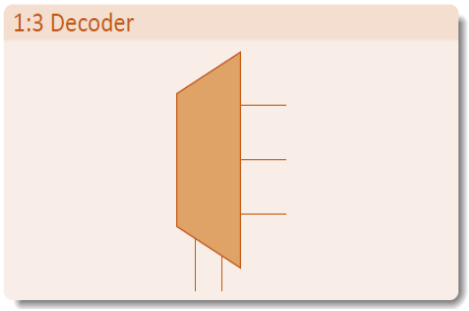
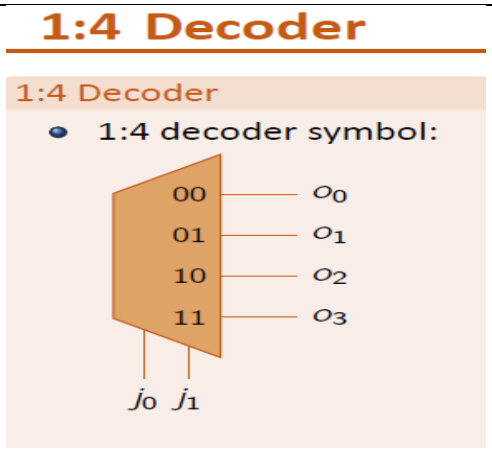
Errata for
DIGITAL DESIGN AND COMPUTER ORGANISATION
Slides Uploaded to PESU ACADEMY Portal

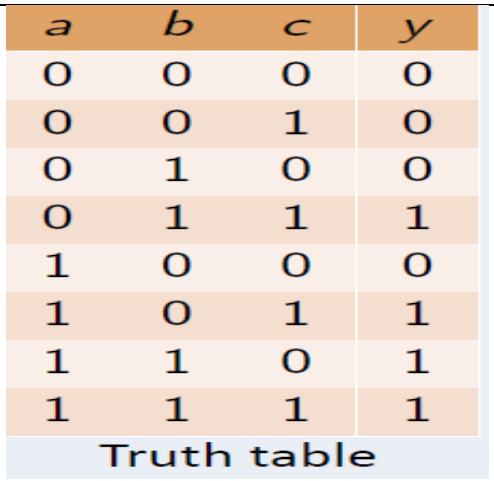
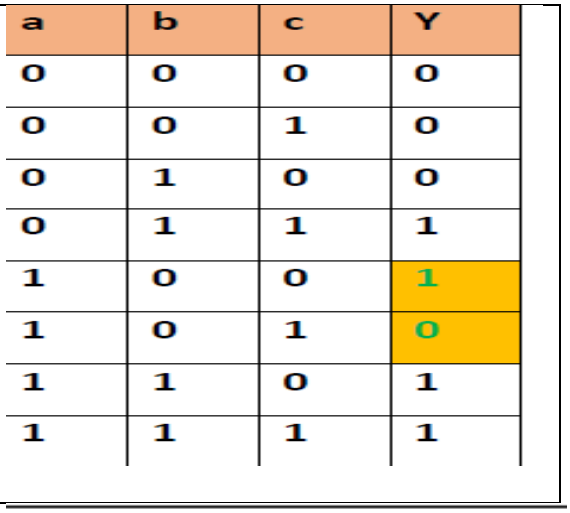
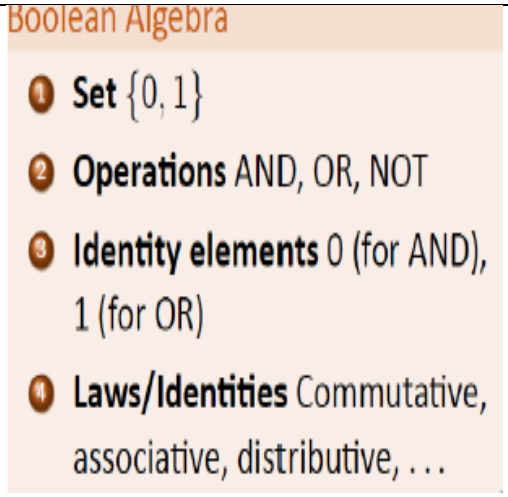
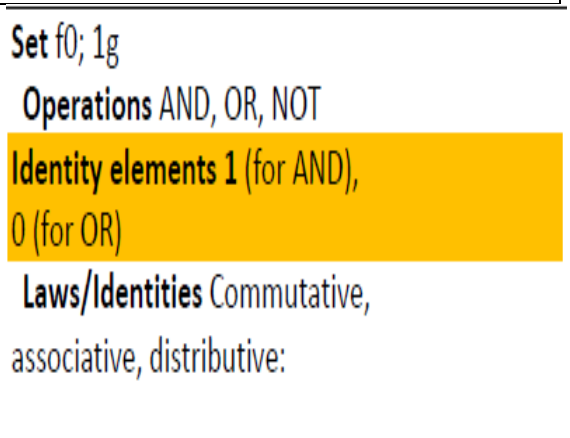
Errata Last updated 20th November 2020

This list is a work in progress. Some of the following corrections may be revised, and additional corrections will probably be added.

Sl. No	Lecture Number	Content in the slide	To be Corrected as
1.	UNIT5 Lecture 53 Slide 10		The total time needed for computation (of the matrix C) with the systolic array will be equal to 3n-2 clock cycles to perform nxn matrix multiplication.
2.	UNIT4 Lecture 38 Slide 18		The time required to add three Numbers using ripple carry Adders is incorrectly mentioned as **(2n + 1)tFA** **The correct time using ripple carry Adders is (n + 2) tFA**

3.	UNIT3 Lecture 34 Slide 16	**CARRY-LOOKAHEAD AND PREFIX ADDERS - 4** **Associative Ripple Carry?** Ripple Carry Adder  • $c_{i+1} = ab + bc_i + c_i a$ • Generate and Propagate: ▸ g_i carry generated in position i ▸ p_i carry propagated in position i ▸ $g_{0:i}$ carry generated in positions 0 to i ▸ $p_{0:i}$ carry propagated in positions 0 to i • $g_i = a_i b_i$ • $p_i = a_i + b_i$ • $g_{0:i+1} = g_i + p_i g_{0:i}$ • $p_{0:i+1} = p_i p_{0:i}$	In the figure the labels p0: i and g0:1 need to be interchanged.
4.	UNIT3 Lecture 31 Slide 5	• Time requirements: For an n-bit ripple carry adder, critical path delay is composed of: ▸ Propagation delay from c_0 to c_{n-1} ★ Signal passes through two gates in each of the $n-1$ stages ★ $2(n-1)t_g$ time required ▸ Sum computation ★ $2t_g$ time required for three input XOR gate • An n-bit ripple carry adder thus occupies $2nt_g$ time	Propagation delay from c0 to c(n-1) should be 3(n-1)tg instead of 2(n-1) tg because although the carry signal passes through two gates in each stage, one of the gates has three inputs which counts as two 2 input gates..
5.	UNIT3 Lecture 31 Slide 34,35	**CARRY-LOOKAHEAD AND PREFIX ADDERS - 1** **Performance Comparison** PES UNIVERSITY ONLINE • Area and time estimates for n-bit adders: Ripple carry: Area $7na_g$, Time $2nt_g$ Carry-lookahead: Area $(n^2+5n)a_g$, Time $2\lceil \log_2(n-1) \rceil t_g + 3t_g$ • Compared to the ripple carry adder's linear delay increase with size, the carry-lookahead adder delay increase only logarithmically, resulting in dramatically faster adders • However, the area of the carry-lookahead adder increase qudratically with size • Is there an adder design that retains the carry-lookahead adder's speed but has significantly lesser area?	log2(n-1) should be replaced by log2(n).

6.	UNIT3 Lecture 24 Slide 42 till Slide 83	 Elevator Example State Tansition Table Current State | Inputs | Next State s_3 s_2 s_1 s_0 | switch_up | on_floor | s_3' s_2' s_1' s_0' 0 0 0 1 | 0 | 0 | 0 0 0 1 0 0 0 1 | 0 | 1 | 0 0 0 1 0 0 0 1 | 1 | 0 | 0 0 1 0 0 0 0 1 | 1 | 1 | 0 0 1 0 0 0 1 0 | 0 | 0 | 0 0 1 0 0 0 1 0 | 0 | 1 | 0 1 0 0 0 0 1 0 | 1 | 0 | 0 0 1 0 0 0 1 0 | 1 | 1 | 0 1 0 0 0 1 0 0 | 0 | 0 | 1 0 0 0 0 1 0 0 | 0 | 1 | 1 0 0 0 0 1 0 0 | 1 | 0 | 0 1 0 0 0 1 0 0 | 1 | 1 | 0 1 0 0 1 0 0 0 | 0 | 0 | 1 0 0 0 1 0 0 0 | 0 | 1 | 0 0 0 1 1 0 0 0 | 1 | 0 | 1 0 0 0 1 0 0 0 | 1 | 1 | 0 0 0 1	on_first should be equal to 1 in state 3(0100) instead of the incorrectly mentioned on_first should be equal to 1 in state 4(1000) 'lift_down' be 1 in state 4 (1000) according to the state diagram
7.	UNIT 2, Lecture 14 Slide 20		To be corrected as 2:3 decoder
8.	UNIT 2 Lecture 14 Slide 12-16		To be corrected as 2:4 decoder

9.	UNIT1, Lecture 3, Slide 12		
10.	UNIT1, Lecture 4, Slide 13		
11.	UNIT1, Lecture 8 Slide 4 till Slide 16,Also same error in Slide 40