DIGITAL DESIGN AND COMPUTER ORGANIZATION

Dr. Reetinder Sidhu
Department of Computer Science and Engineering

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Multi-Cycle Processor - 1

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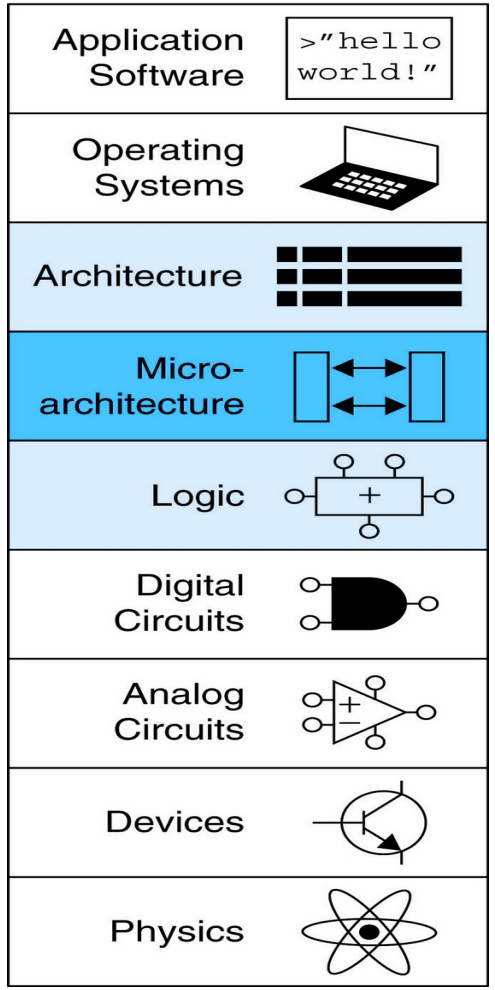
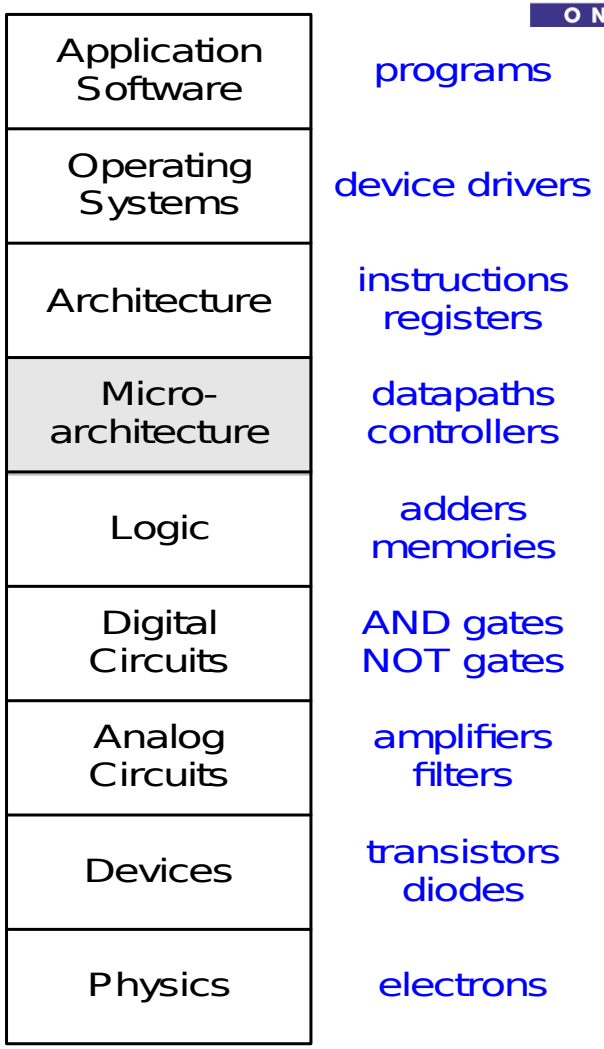
Outline

- **Introduction**
- **Performance Analysis**
- **Multicycle Processor Datapath**
- **Multicycle Processor Control Logic**

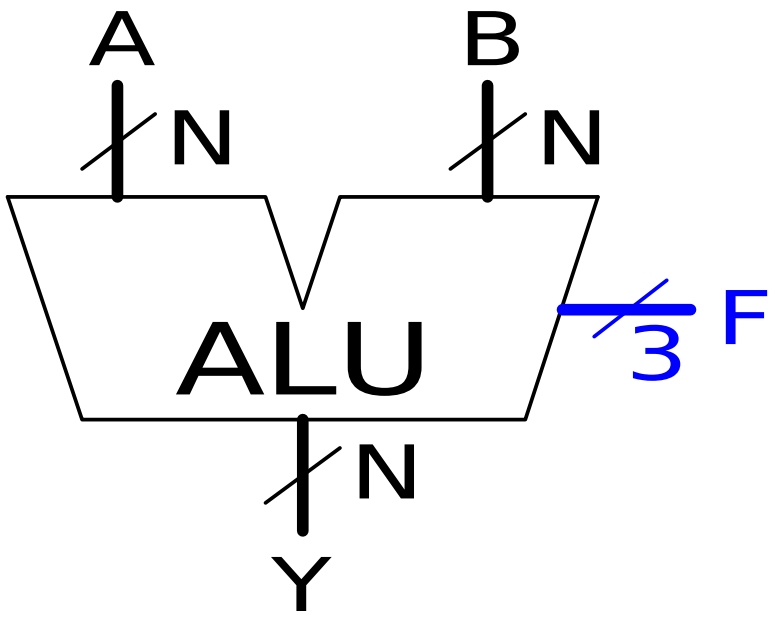


Multi-Cycle Processor - 1
Introduction

- **Microarchitecture:** how to implement an architecture in hardware
- Processor:
  - **Datapath:** functional blocks
  - **Control:** control signals



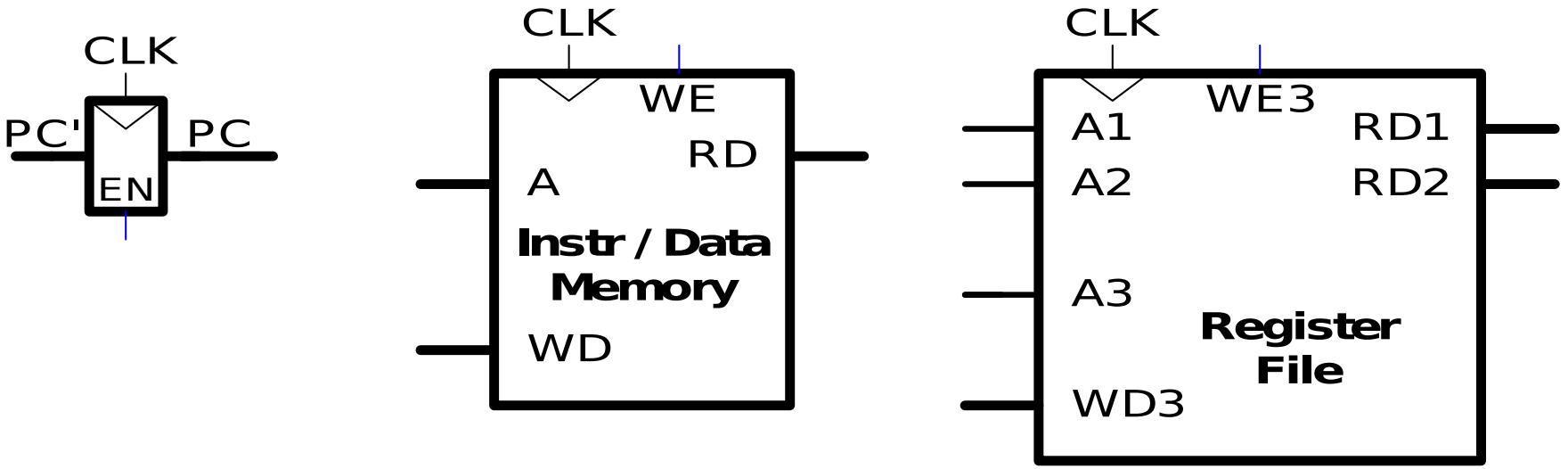
Multi-Cycle Processor - 1
Review: ALU



$F_{2:0}$	Function
000	A & B
001	A | B
010	A + B
011	not used
100	A & ~B
101	A | ~B
110	A - B
111	SLT

Multi-Cycle Processor - 1
Architecture State Elements

- Program Counter, Register File and Main memory
  - Latter outside microprocessor



Multi-Cycle Processor - 1

Reading Word-Addressable Memory

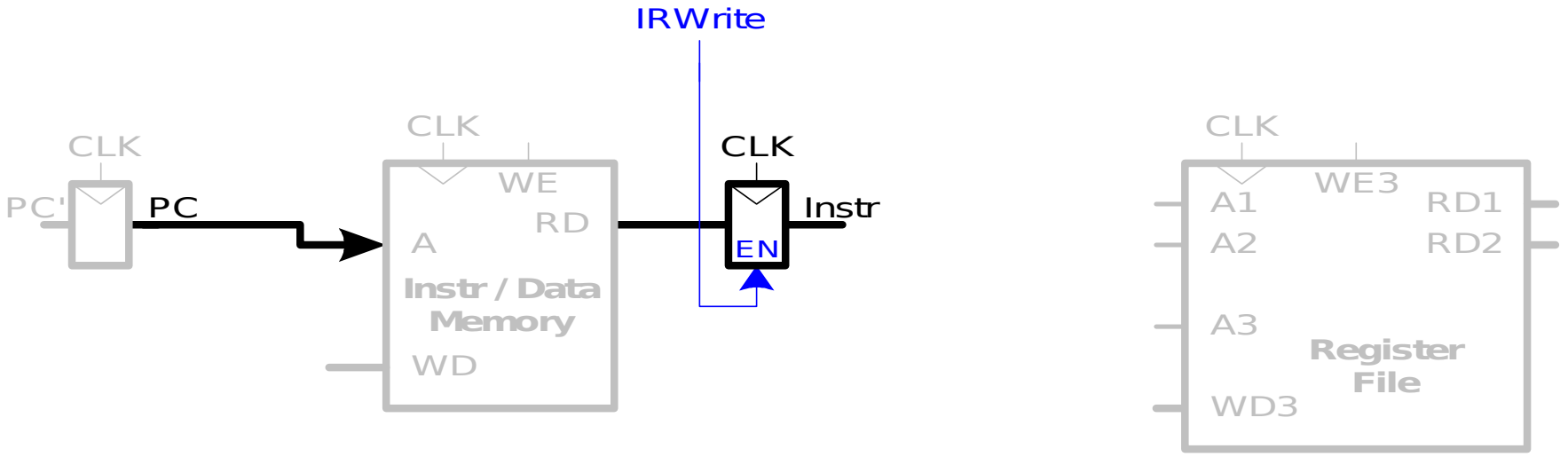
- Memory read called ***load***
- **Mnemonic:** *load word* (lw)
- **Format:**

  lw $s0, 5($t1)
- **Address calculation:**
  - add *base address* ($t1) to the *offset* (5)
  - address = ($t1 + 5)
- **Result:**
  - $s0 holds the value at address ($t1 + 5)

Any register may be used as base address

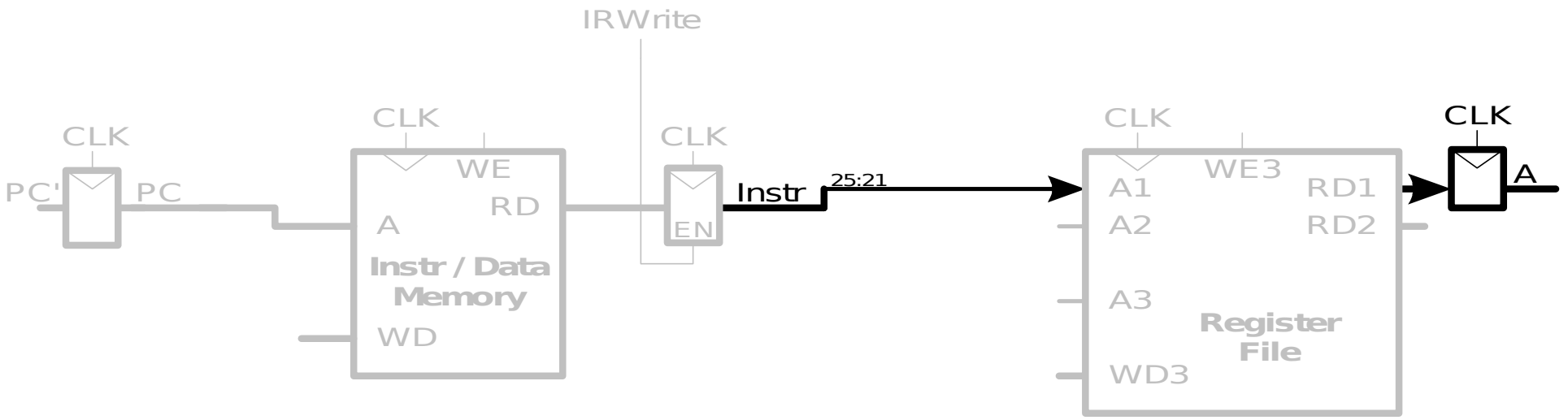
Multi-Cycle Processor - 1
Multicycle Datapath: Instruction Fetch

STEP 0: Fetch instruction



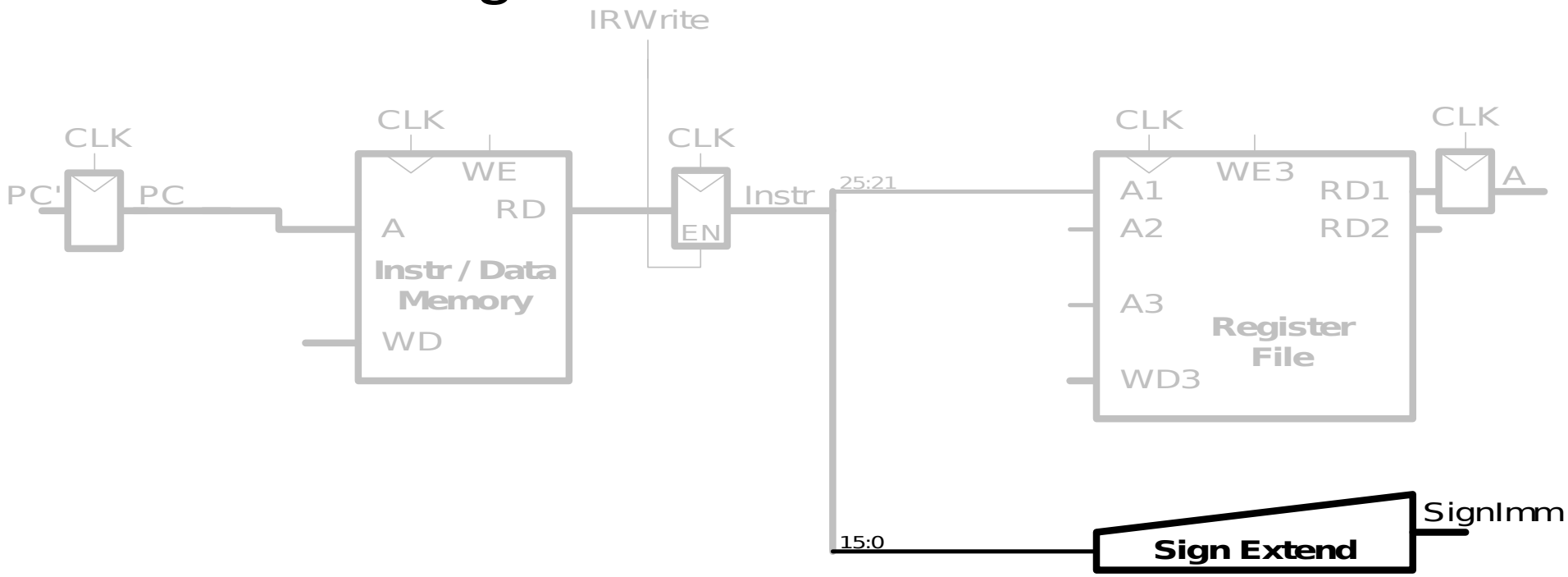
Multi-Cycle Processor - 1
Multicycle Datapath: lw Register Read

STEP 1: Read source operands from RF



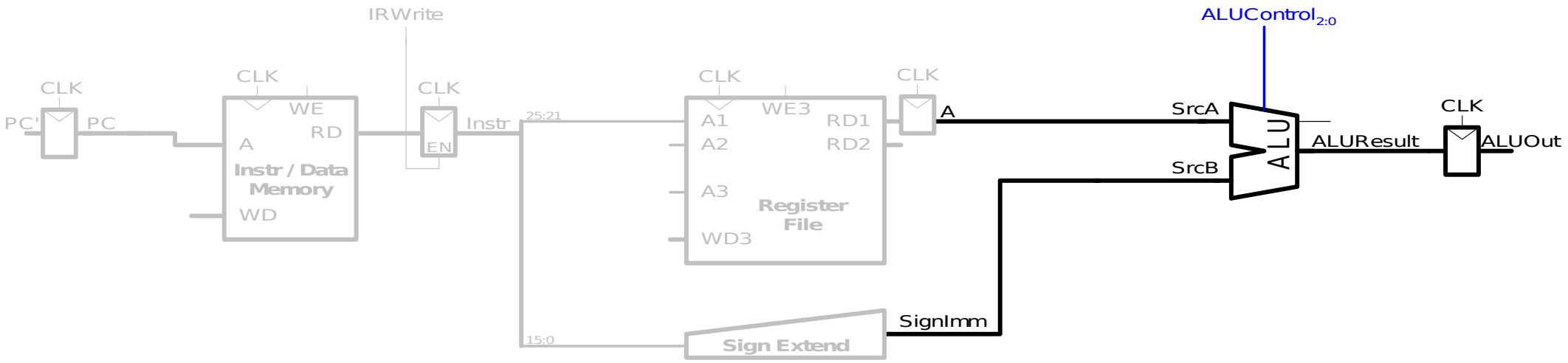
Multi-Cycle Processor - 1
Multicycle Datapath: lw Immediate

STEP 2: Read and Sign-extend the immediate



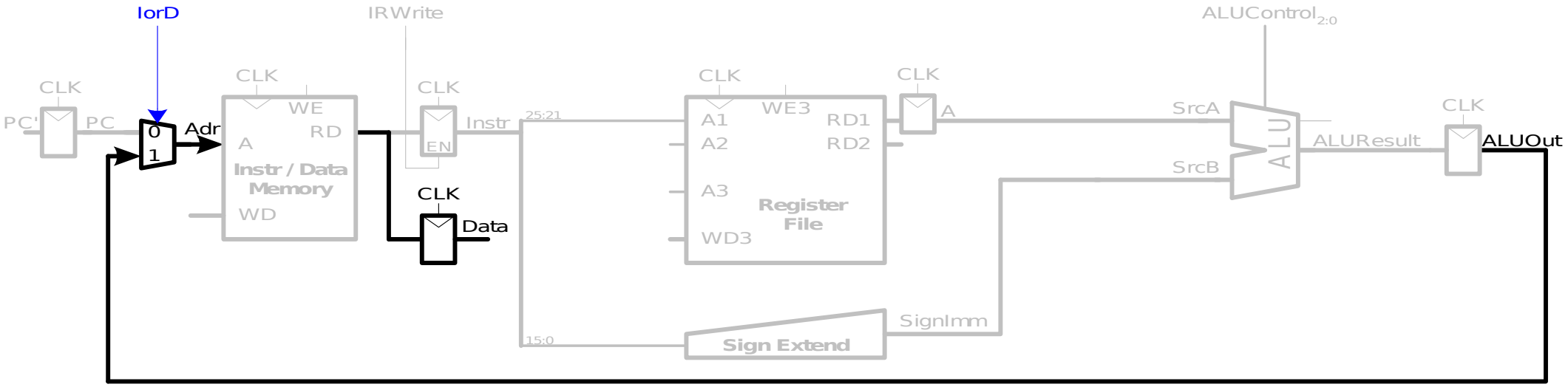
Multi-Cycle Processor - 1
Multicycle Datapath: lw Address

STEP 3: Compute the memory address



Multi-Cycle Processor - 1
Multicycle Datapath: lw Memory Read

STEP 4: Read data from memory



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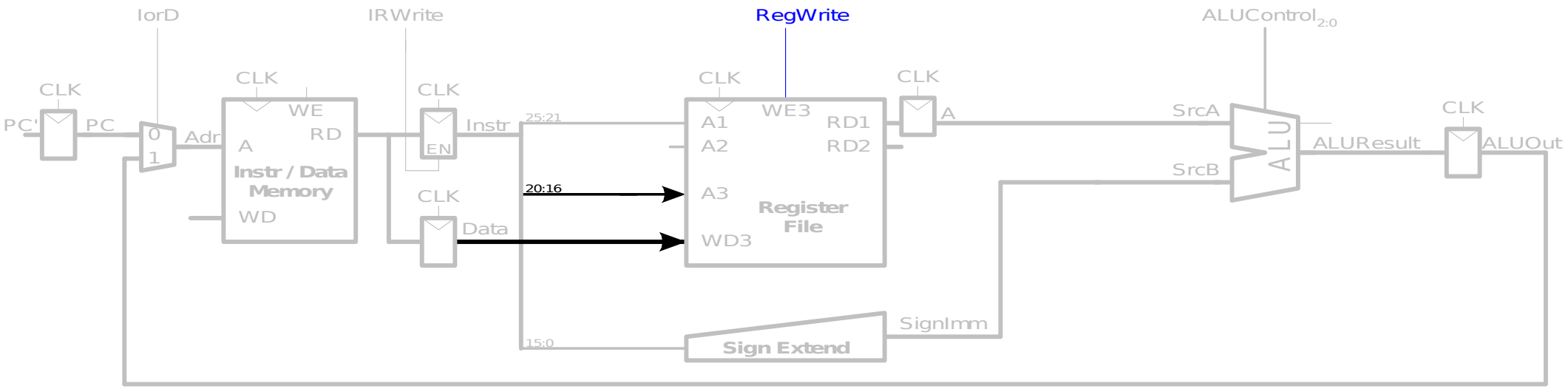
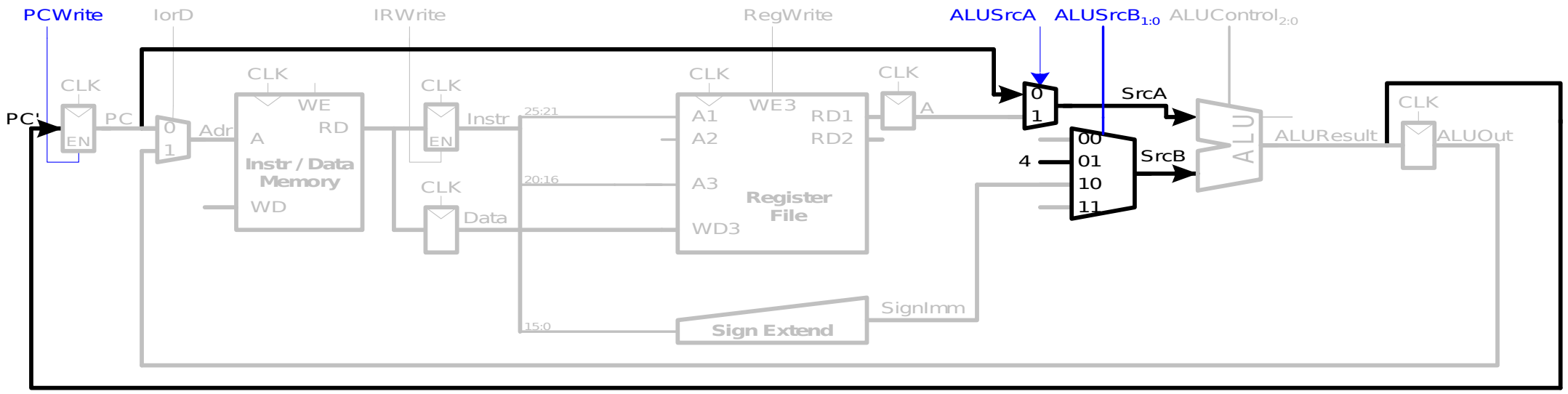
Multicycle Datapath: lw Write Register

STEP 5: Write data back to register file



Multicycle Datapath: Increment PC

STEP 6: Increment PC



Multi-Cycle Processor
Think About It

- Only one adder (inside ALU)
- In lab datapath design, two adders used (separate adder for PC)
- Would using two adders in current design help? How?
- Note that in both cases, architecture remains the same