Digital Design and Computer Organization

Synchronous Sequential Logic Circuits

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Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
    - ★ **Synchronous Sequential Logic Circuits**
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

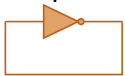
Concepts covered

- Synchronous Sequential Logic Circuits

Synchronous Sequential Logic Circuits

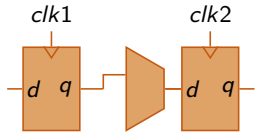
Potential Problems with Sequential Logic Circuits

- Combinational logic circuits do not contain **loops** or **cyclic paths** but sequential logic circuits do
- Loops can cause problems



  - Unstable state

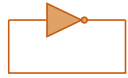
- Memory elements can suffer from **race** conditions (also called **race hazards**)



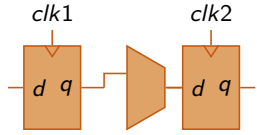
  - Output depends upon input sequence

Synchronous Sequential Logic Circuits

- Cyclic paths are broken by inserting flip-flops in them



- Flip-flops are synchronized by connecting them to a common clock
  - Race conditions are eliminated if the clock time period is long enough



Synchronous Sequential Logic Circuits

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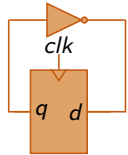

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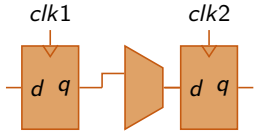

Synchronous Sequential Logic Circuits

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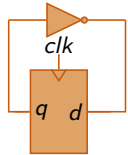

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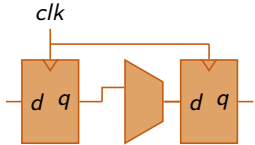

Synchronous Sequential Logic Circuits

- A **synchronous sequential logic circuit** is one in which:[1]
  - Every circuit element is either a register (flip-flop) or a combinational logic circuit
  - At least one circuit element is a register
  - All registers receive the same clock signal
  - Every cyclic path contains at least one register

[1] From "Digital Design and Computer Architecture 2nd Ed.", *Harris and Harris*, ©Elsevier, 2013.

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  - Every cyclic path contains at least one register
- Only above type of sequential logic circuits studied henceforth in this course

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Think About It

- Classify the following logic circuits as combinational or synchrnous sequential or neither
  - AND gate (output not connected to own input)
  - AND gate (output connected to own input)
  - D flip-flop
  - SR latch
  - Series of D flip-flops (with common clock) with output of one connected to the input of the next via an inverter