Assignment questions on 4th unit

1. Explain the cache optimization: Giving Read priority over write priority.
2. Consider the following code sequence.

```
STR   R3,  512 (R0)

LDR   R1,  1024 ( R0)

LDR  R2,  512 (R0)
```

   Assume Direct mapped: Write –through cache that maps 512 and 1024 to the same block. Four word write buffer that is not checked on a read miss. Will the value in R2 always be equal to the value in R3? Explain with steps.

3. Explain write through cache and write back cache with respect to giving read priority over write priority.
4. Explain virtual address. How it differs with physical address.
5. How virtual address is translated to physical address. Explain with suitable diagram.
6. What are the two tasks in address translation? Explain.
7. What is virtual cache? Explain the difficulties.
8. Explain the solution to Aliasing with respect to virtual cache.
9. Explain TLB with necessary diagrams.
10. Explain simplifications of TLB.
11. Define speedup in parallel architecture. Give example.
12. Explain Amdahl's law with example.

13. Explain Gustafson’s law with example.
14. Write a note on “limitations of speedup”.
15. Compare Amdahl’s law and Gustafson’s law with example.
16. Write a note on:
    - Scalability
    - Efficiency
    - Flat memory Approximation

17.Mention two categories of parallel computers and explain them with their architectures

18.Discuss and compare the 5 stage pipelined superscalar processing

19.Explain with diagrams : Flynn's Classification of SIMD,SIMD,MISD and MIMD

20.Discuss in detail about symmetric and distributed shared memory architecture

21.Draw and explain the structure of a superscalar processor

22. Differentiate between UMA and NUMA architectures, with suitable diagrams(if any)

23.explain with a neat diagram , symmetric shared memory architecture

24.Explain the various approaches to Parallel Programming.

25.Differentiate symmetric memory architecture and distributed memory architecture.

26.Explainin detail the distributed shared memory architecture highlighting the directory based cache coherence protocol.

27. Explain with examples different ILP techniques.

28. What is Parallelism? Explain its different types with appropriate examples.

29.Mention different approches to parallel programming

30. Explain different memory architecture with an example each

31. Address translation time needs to be reduced , Explain the meaning of the statement, also describe how this is achieved

32. what are the entries of TLB? Explain TLBs role in reducing the address translation time