Digital Design and Computer Organization

Muxes, Decoders, Shifters - 1

Reetinder Sidhu

Department of Computer Science and Engineering

Digital Design and Computer Organization

Muxes, Decoders, Shifters - 1

Reetinder Sidhu

Department of Computer Science and Engineering

Muxes, Decoders, Shifters - 1

Course Outline

- Digital Design
  - Combinational logic design
    - **Muxes, Decoders, Shifters - 1**
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Multiplexers

Muxes, Decoders, Shifters - 1

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

2:1 Mux

Muxes, Decoders, Shifters - 1

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

2:1 Mux

- 2:1 mux truth table:

i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Muxes, Decoders, Shifters - 1

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

2:1 Mux

- 2:1 mux truth table:

i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

Muxes, Decoders, Shifters - 1

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

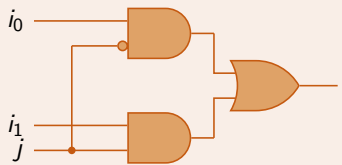
2:1 Mux

- 2:1 mux truth table:

i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

- 2:1 mux logic circuit:



2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

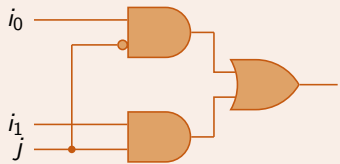
2:1 Mux

- 2:1 mux truth table:

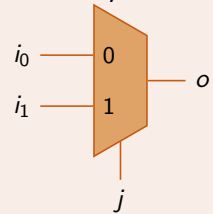
i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

- 2:1 mux logic circuit:



- 2:1 mux symbol:



  - Data inputs: i_0, i_1
  - Control input: j

Muxes, Decoders, Shifters - 1

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

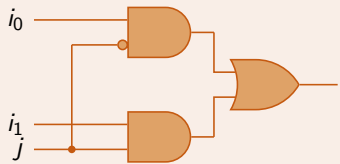
2:1 Mux

- 2:1 mux truth table:

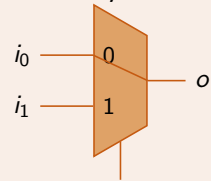
i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

- 2:1 mux logic circuit:



- 2:1 mux symbol:



  - Data inputs: i_0, i_1
  - Control input: j

Muxes, Decoders, Shifters - 1

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

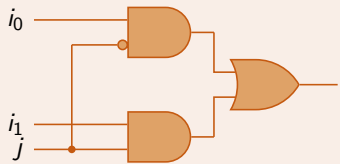
2:1 Mux

- 2:1 mux truth table:

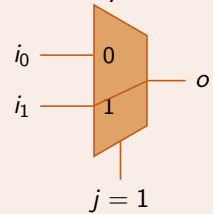
i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

- 2:1 mux logic circuit:



- 2:1 mux symbol:



  - Data inputs: i_0, i_1
  - Control input: j

2:1 Multiplexer

- A multiplexer (also called a mux) *multiplexes* many inputs onto a single output

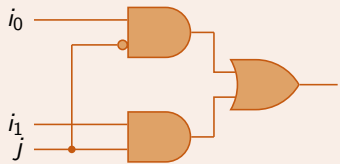
2:1 Mux

- 2:1 mux truth table:

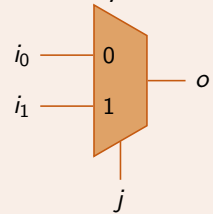
i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- 2:1 mux Boolean formula:
  $o = \bar{j}\, i_0 + j\, i_1$

- 2:1 mux logic circuit:



- 2:1 mux symbol:



  - Data inputs: i_0, i_1
  - Control input: j

Muxes, Decoders, Shifters - 1

4:1 Multiplexer

PES UNIVERSITY ONLINE

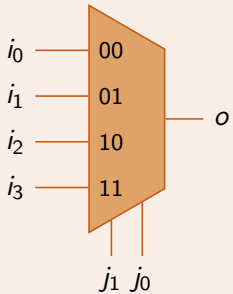
4:1 Mux

Muxes, Decoders, Shifters - 1

4:1 Multiplexer

4:1 Mux

- 4:1 mux symbol:



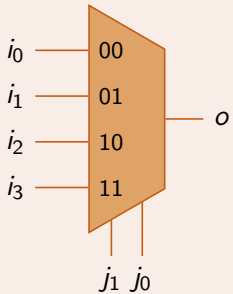
- Data inputs: i_0, i_1, i_2, i_3
- Control inputs: j_0, j_1

Muxes, Decoders, Shifters - 1

4:1 Multiplexer

4:1 Mux

- 4:1 mux symbol:



- Data inputs: i_0, i_1, i_2, i_3
- Control inputs: j_0, j_1

- 4:1 mux Boolean formula:

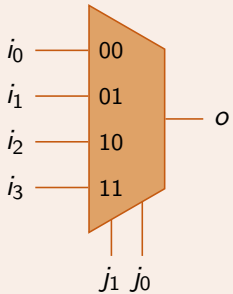
$$o = \overline{j_1}\,\overline{j_0}\,i_0 + \overline{j_1}\,j_0\,i_1 + j_1\,\overline{j_0}\,i_2 + j_1\,j_0\,i_3$$

Muxes, Decoders, Shifters - 1

4:1 Multiplexer

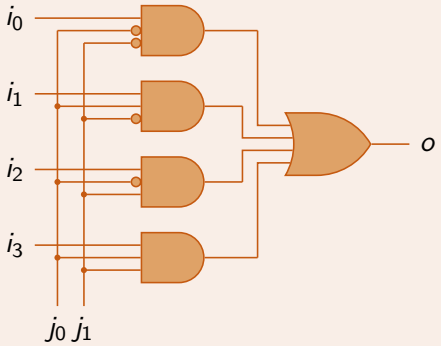
4:1 Mux

- 4:1 mux symbol:



- Data inputs: i_0, i_1, i_2, i_3
- Control inputs: j_0, j_1

- 4:1 mux logic circuit:



- 4:1 mux Boolean formula:

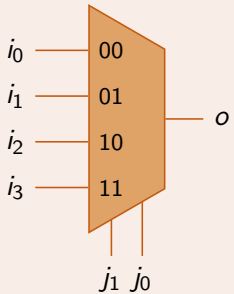
$$o = \overline{j_1}\,\overline{j_0}\,i_0 + \overline{j_1}\,j_0\,i_1 + j_1\,\overline{j_0}\,i_2 + j_1\,j_0\,i_3$$

Muxes, Decoders, Shifters - 1

4:1 Multiplexer

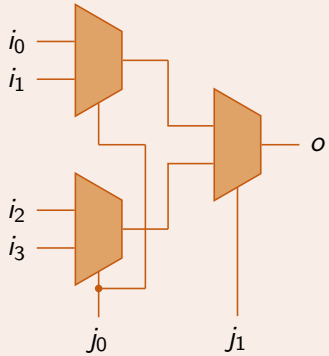
4:1 Mux

- 4:1 mux symbol:



- Data inputs: i_0, i_1, i_2, i_3
- Control inputs: j_0, j_1

- 4:1 mux logic circuit using 2:1 muxes:



- 4:1 mux Boolean formula:

$$o = \overline{j_1}\,\overline{j_0}\,i_0 + \overline{j_1}\,j_0\,i_1 + j_1\,\overline{j_0}\,i_2 + j_1\,j_0\,i_3$$

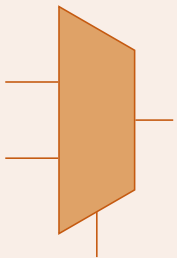
Muxes, Decoders, Shifters - 1

n:1 Multiplexer

Muxes, Decoders, Shifters - 1

n:1 Multiplexer

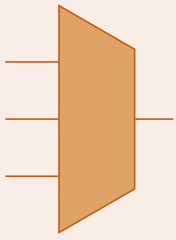
2:1 Mux



Muxes, Decoders, Shifters - 1

n:1 Multiplexer

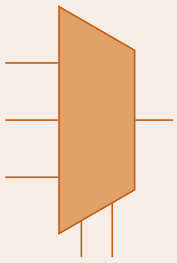
3:1 Mux



Muxes, Decoders, Shifters - 1

n:1 Multiplexer

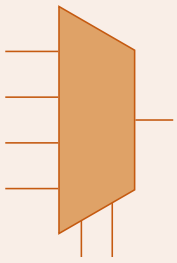
3:1 Mux



Muxes, Decoders, Shifters - 1

n:1 Multiplexer

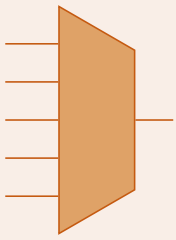
4:1 Mux



Muxes, Decoders, Shifters - 1

n:1 Multiplexer

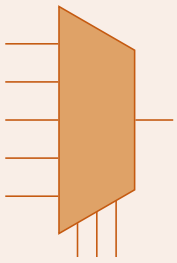
5:1 Mux



Muxes, Decoders, Shifters - 1

n:1 Multiplexer

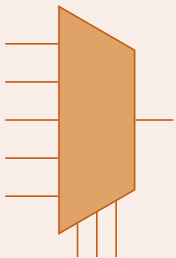
5:1 Mux



Muxes, Decoders, Shifters - 1

n:1 Multiplexer

5:1 Mux



n : 1 Mux

A combinational logic circuit having n data inputs, $\lceil \log_2 n \rceil$ control inputs and one output, that connects the data input indicated by the control inputs to the output

Muxes, Decoders, Shifters - 1

Think About It

- What is the Boolean formula for a 3:1 mux?
- Construct a 3:1 mux using
  - 2:1 muxes
  - AND, OR and NOT gates