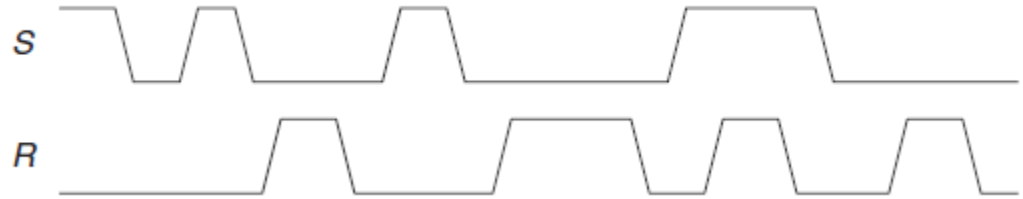
2 Marks Questions

1: Implement NAND gate using 2:1 MUX

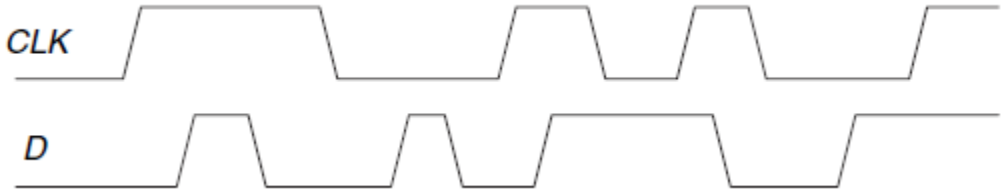
2: Implement NOR gate using 2:1 MUX

3: Implement 16:1 MUX using 4:1 MUX

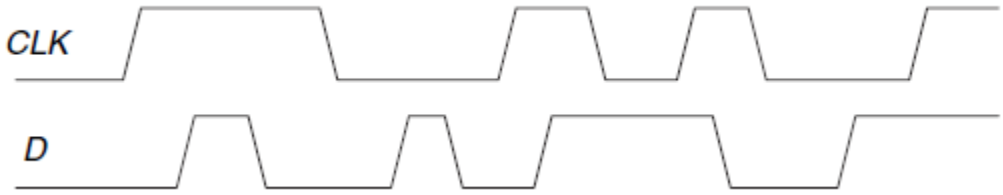
4: Given the input waveforms shown in Figure , sketch the output, Q, of an SR latch.



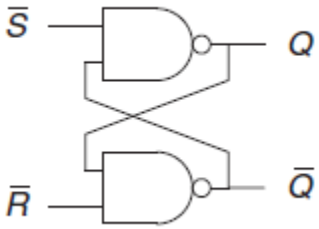
5: Given the input waveforms shown in Figure, sketch the output, Q, of a D latch.



6: Given the input waveforms shown in Figure, sketch the output, Q, of a D flip-flop.



7: Is the circuit combinational logic or sequential logic? Explain in a simple fashion what the relationship is between the inputs and outputs. What would you call this circuit?



8: Draw a state machine that can detect when it has received the serial input sequence 01010.

9: What is the difference between a latch and a flip-flop? Under what circumstances is each one preferable?

10: Design an asynchronously resettable D latch using logic gates.

11: Design an asynchronously resettable D flip-flop using logic gates.

12: Design a synchronously settable D flip-flop using logic gates.

13: Design an asynchronously settable D flip-flop using logic gates.

6 Marks Questions

1: Implement 1 bit full adder using 8:1 Multiplexer

2: Implement full adder using decoders (4 bit)

Hint: $Sum(x, y, z) = \sum(1, 2, 4, 7)$ $Carry(x, y, z) = \sum(3, 5, 6, 7)$

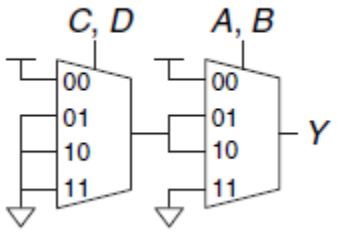
3: Complete the design of the seven-segment decoder segments Sc through Sg (see Example 2.10):

(a) Derive Boolean equations for the outputs Sc through Sg assuming that inputs greater than 9 must produce blank (0) outputs.

(b) Derive Boolean equations for the outputs Sc through Sg assuming that inputs greater than 9 are don't cares.

(c) Sketch a reasonably simple gate-level implementation of part (b). Multiple outputs can share gates where appropriate.

4: Write a minimized Boolean equation for the function performed by the circuit in

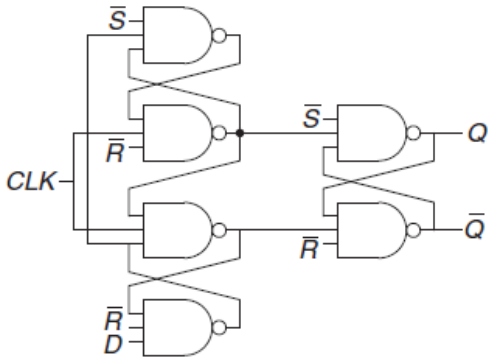


5: Design an 8:1 multiplexer with the shortest possible delay from the data inputs to the output. You may use any of the gates. Sketch a schematic. Using the gate delays from the table, determine this delay.

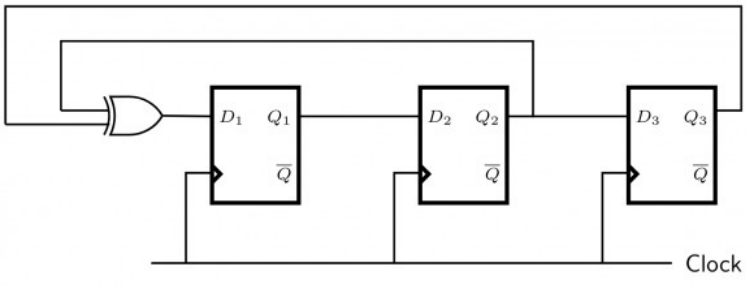
6: Sketch a schematic for a fast 3:8 decoder. Suppose gate delays are given in Table (and only the gates in that table are available). Design your decoder to have the shortest possible critical path, and indicate what that path is. What are its propagation delay and contamination delay?

Gate	t_{pd} (ps)	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40

7. Is the circuit in combinational logic or sequential logic? Explain in a simple fashion what the relationship is between the inputs and outputs. What would you call this circuit?



8: Consider the sequential circuit given below



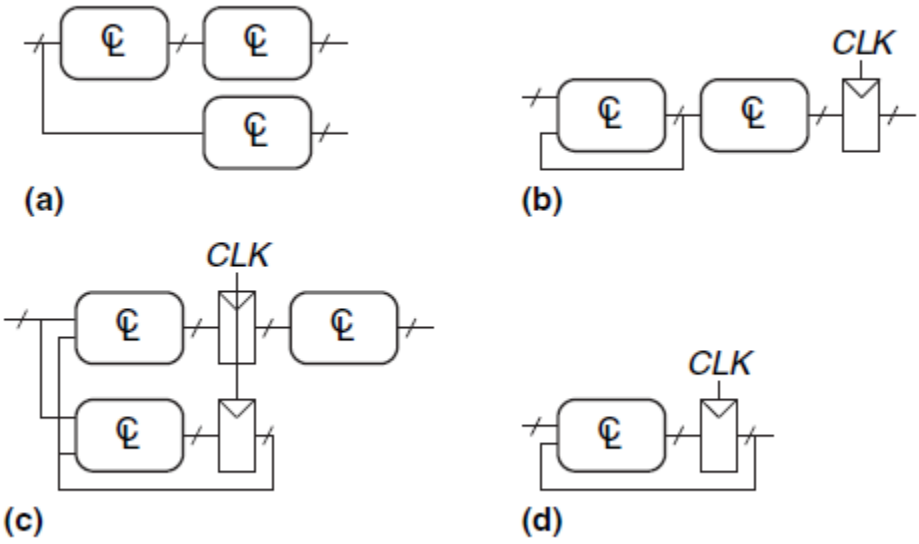
State(Q1,Q2,A3) S0: (000) S1(001) S2(010) S3(011) S4(100) S5(101) S6(110) S7(111)

Given the initial state is S4, identify the state which are not reachable:

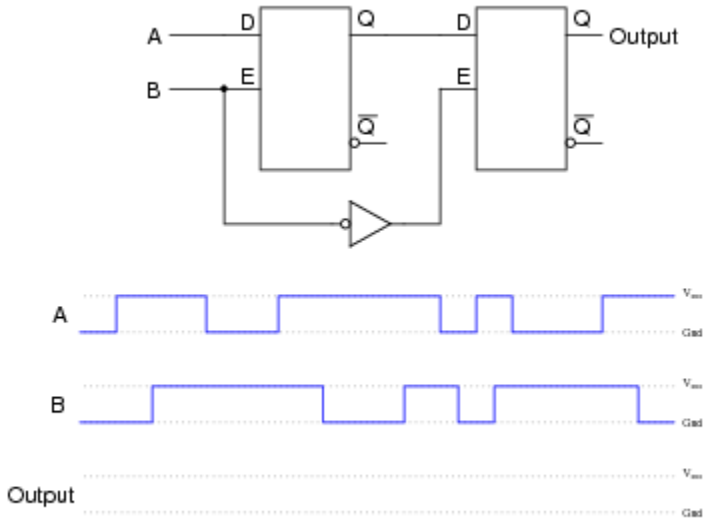
9: Design a serial (one bit at a time) two's complementer FSM with two inputs, Start and A, and one output, Q. A binary number of arbitrary length is provided to input A, starting with the least significant bit. The corresponding bit of the output appears at Q on the same cycle. Start is asserted for one cycle to initialize the FSM before the least significant bit is provided.

10: Design a 5-bit counter finite state machine.

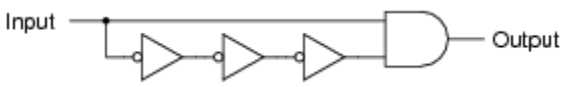
11: Which of the circuits in Figure are synchronous sequential circuits? Explain.



12: Determine the final output states over time for the following circuit, built from D-type gated latches:

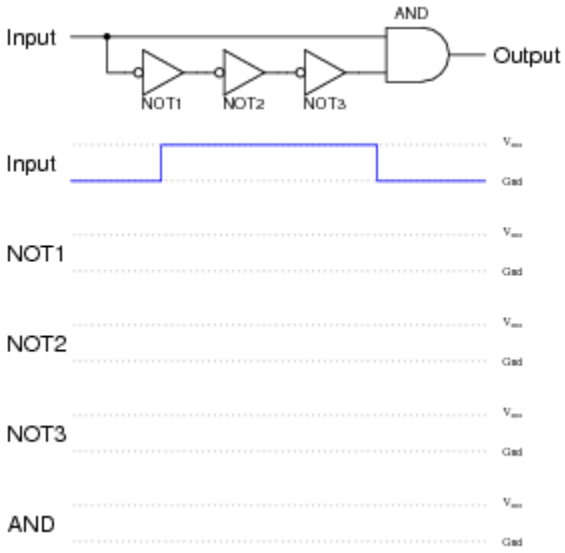


13: Usually, propagation delay is considered an undesirable characteristic of logic gates, which we simply have to live with. Other times, it is a useful, even necessary, trait. Take for example this circuit:

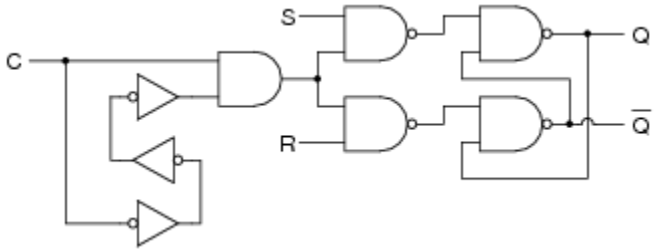


If the gates constituting this circuit had zero propagation delay, it would perform no useful function at all. To verify this sad fact, analyze its steady-state response to a "low" input signal, then to a "high" input signal. What state is the AND gate's output always in?

Now, consider propagation delay in your analysis by completing a timing diagram for each gate's output, as the input signal transitions from low to high, then from high to low:



14: Explain how the addition of a propagation-delay-based one-shot circuit to the enable input of an S-R latch changes its behavior:



Specifically, reference your answer to a truth table for this circuit.

15: Give the next-state equations and the state table corresponding to the sequential circuit shown below.