Digital Design and Computer Organization

Latches, Flip-flops - 3

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
    - ★ **Latches, Flip-flops - 3**
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

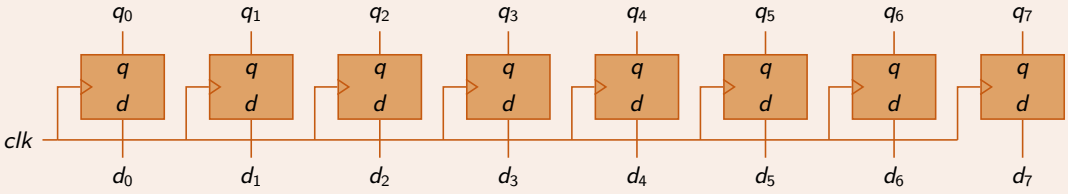
- Register
- Flip-Flop with Enable
- Flip-Flop with Reset

Register

Register

- An n-bit register consists of n flip-flops with their clock inputs connected together
- It can store n-bits of data
  - Also called an n-bit word

- 8-bit D flip-flop based register:



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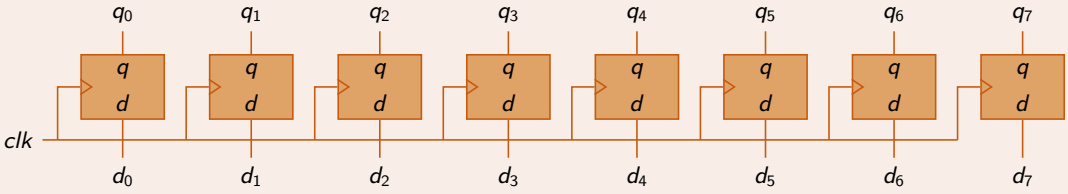

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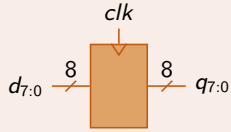

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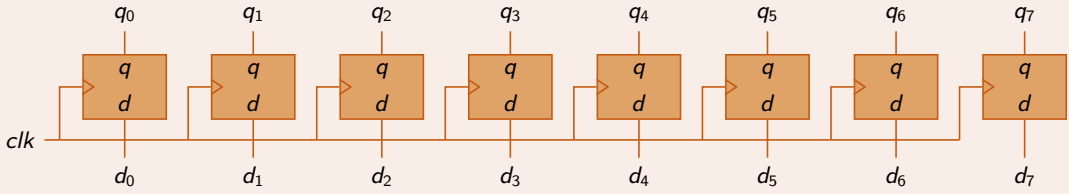

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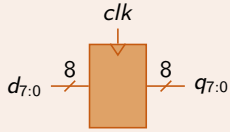
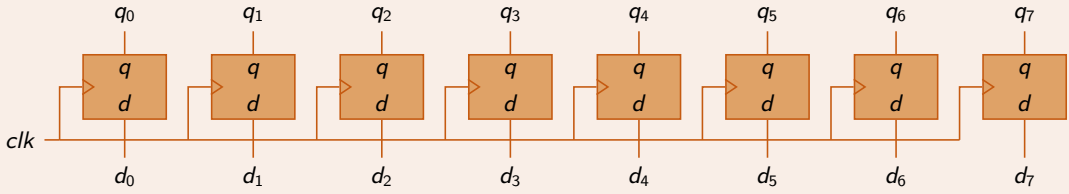


- Symbol (8-bit):
- A single D flip-flop can also be called a register

- 8-bit D flip-flop based register:



Flip-Flop with Enable

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Flip-flop with additional **enable** (or load) signal that determines when new input stored

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- Clock gating approach:

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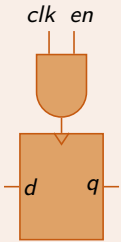

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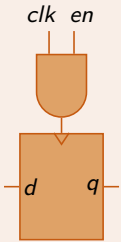

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  - Clock gating can cause timing problems
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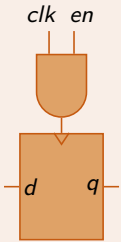

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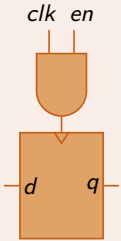

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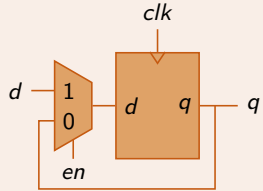

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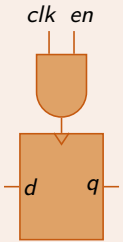

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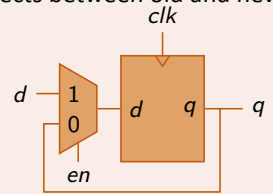

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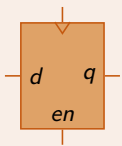

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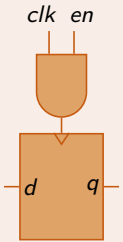

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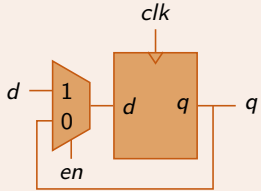

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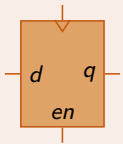

- At the rising edge of *clk*:

en	*d*	*q*
0	0	q_{prev}
0	1	q_{prev}
1	0	0
1	1	1

Latches, Flip-flops - 3
Resettable Flip-Flop

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Resettable Flip-Flop

Flip-flop with additional **reset** signal used to store 0 irrespective of the input

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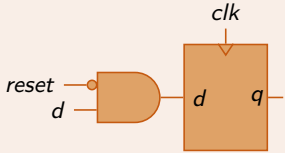
- Logic Diagram:



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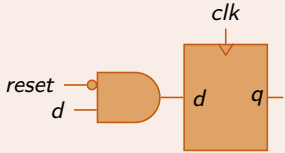

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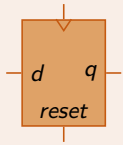

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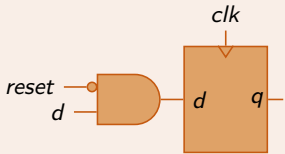

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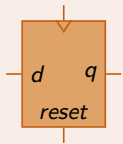

- At the rising edge of *clk*:

reset	*d*	*q*
0	0	0
0	1	1
1	0	0
1	1	0

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Think About It

- Construct a JK flip-flop with enable and reset signals