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## <u>PES University, Bangalore</u> (Established under Karnataka Act 16 of 2013)

**UE18EC101** 

## END SEMESTER ASSESSMENT (ESA) B. Tech II SEMESTER- May '19 UE18EC101 - BASIC ELECTRONICS (Common to all branches)

Time: 3 Hrs

Answer All The Questions

Max Marks: 100

1	0	Count the number of bronches and nodes in the in it IC' 24 14 10 X	
1.	a.	Count the number of branches and nodes in the circuit. If $i_x$ = 3A and the 18 V source delivers 8A of current, what is the value of $R_A$ ? Use Ohm's law as well as KCL.	6
		$\begin{array}{c c} & & & & & & & & & \\ \hline  & & & & & & & \\ \hline  & & & & & & \\ \hline  & & & & \\$	
	b.	Reverse saturation current of Ge diode is 200uA at 27°C. If temperature is increased by 30°C find I <sub>S</sub> and I <sub>D</sub> for the bias voltage of 0.2V at new temperature. If it were Silicon diode what is the current at 27°C ideally.	6
	c.	Explain diode models with the help of equivalent circuits and V-I characteristics. Find $Vo_1$ , and $Vo_2$ for the circuit shown considering practical diodes.	8
		R <sub>1</sub> = 1.2 ks, R <sub>2</sub> = 3.3 ks10 Vo H 10 00 00 000 000	
		R <sub>2</sub> \( \frac{3.3462}{2}	
2.	a.	Explain the operation of the circuit shown along with the required equivalent circuits and waveforms. Calculate the output DC level and the required PIV of each diode.	8
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	b.	Draw the circuit diagram of a center tapped FWR with capacitor filter. If the filter capacitor is 120 uF and load current is 80mA calculate the % ripple of the output. The FWR is operating from 50Hz supply and develops a peak rectified voltage of 25V.	6
	c.	Design a Zener regulator that maintains $V_0$ at 10V for input voltage variation of $20V\pm10\%$ and load current variation of $30mA\pm20\%$ . Given Izmin= $2mA$ and Izmax= $50mA$ . Draw the circuit indicating the values of all the components.	6
	a.	Simplify the Boolean expression Y=A(B+C(AB+AC)) showing the steps involved, also implement the simplified expression using 2 input NAND gates.	6
	b.	Write Sum and Carry expression for Full Adder and implement it using 4:1 Multiplexer. Draw the circuit considering Cin as Data line and A,B as select lines. Write the data line input to D <sub>0</sub> , D <sub>1</sub> , D <sub>2</sub> , D <sub>3</sub>	8

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	c.	Starting from LSB load the data 1010 into SISO Shift register. Explain the operation using negative edge triggered D flip flop along with circuit, state table and timing diagrams.	6		
4.	a.	Draw and explain the input and output characteristics of transistor in CE configuration.  Mark all the regions of operation stating the biasing conditions for these regions.			
	b.	Draw and explain the structure of the N channel E- MOSFET.  Given ID(ON)=3mA at VGS(ON)=10V for an enhancement type of MOSFET with VT=3V.  Find K and the drain current for VGS= 8V indicating all the steps involved and formula used.	6		
-	c.	The input power to a device is 10,000 W at a voltage of 1000 V. The output power is 500 W, while the output impedance is $20\Omega$ . Find the power and voltage gain in decibels.	6		
	a.	Define and write ideal values along with the units of the following parameters of Operational Amplifier - i) CMRR, ii) GBW, iii) Slew rate.	6		
	b.	Name any one open loop application of Op Amp. Explain this application in detail.	6		
	c.	Identify the stages and find the output voltage at each stage. $V_{i,\eta} = 0.25V$ $V_{i} = 2V$ $V_{2} = 0.5V$ $V_{i,\eta} = 0.25V$ $V_{i,\eta} = 0.25V$ $V_{i,\eta} = 0.25V$ $V_{i,\eta} = 0.25V$	8		