Digital Design and Computer Organization

Muxes, Decoders, Shifters - 2

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
    - ★ **Muxes, Decoders, Shifters - 2**
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Tristate
- Decoders

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Floating Value (Z) / Tristate Buffer

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Floating Value (Z) / Tristate Buffer

- 0 and 1 values in logic circuits are implemented as voltage levels, typically:
  - 0 is represented by 0v
  - 1 is represented by a positive voltage, say 1.8v

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Floating Value (Z)

When a wire is electrically disconnected from voltage representing 0 as well as from voltage representing 1, it is said to be in **floating** state (also called high impedance state) and is denoted by the symbol Z

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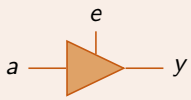
Tristate Buffer

- Tristate gate truth table:



e	a	y
0	0	Z
0	1	Z
1	0	0
1	1	1

  - When $e = 1$, output is same as input, and when $e = 0$, output is floating
  - Key application is shared bus

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1:2 Decoder

1:2 Decoder

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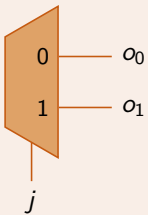
- 1:2 decoder symbol:



  - Inputs: j
  - Output: o_0, o_1

1:2 Decoder

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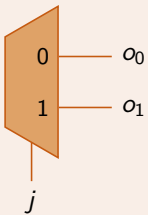

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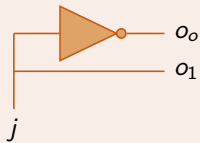
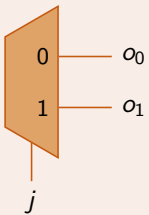
- 1:2 decoder logic circuit:



1:2 Decoder

1:2 Decoder

- 1:2 decoder symbol:



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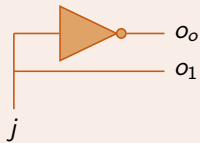

- 1:2 decoder truth table:

j	o_0	o_1
0	1	0
1	0	1

- 1:2 decoder Boolean formula:

$o_0 = \bar{j}$

$o_1 = j$

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1:4 Decoder

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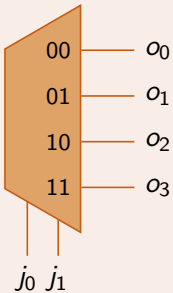
- 1:4 decoder symbol:



1:4 Decoder

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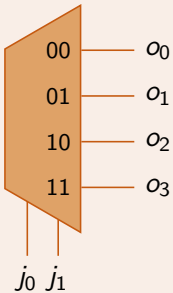
- 1:4 decoder symbol:



- 1:4 decoder Boolean formula:

$o_0 = \overline{j_1}\,\overline{j_0}$ $\quad o_1 = \overline{j_1}\,j_0$

$o_2 = j_1\,\overline{j_0}$ $\quad o = j_1\,j_0$

1:4 Decoder

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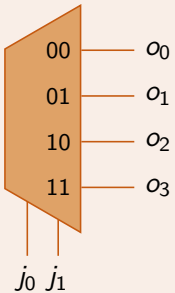
- 1:4 decoder symbol:



- 1:4 decoder truth table:

j_1	j_0	o_0	o_1	o_2	o_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- 1:4 decoder Boolean formula:

$o_0 = \overline{j_1}\,\overline{j_0}$ $\quad o_1 = \overline{j_1}\,j_0$

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1:4 Decoder

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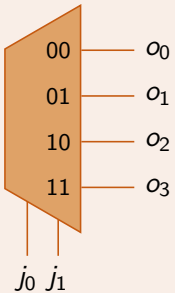
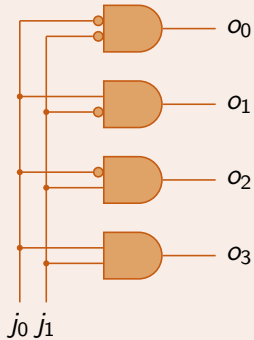


- 1:4 decoder truth table:

j_1	j_0	o_0	o_1	o_2	o_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- 1:4 decoder logic circuit:



- 1:4 decoder Boolean formula:

$o_0 = \overline{j_1}\,\overline{j_0}$ $\quad o_1 = \overline{j_1}\,j_0$

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1:n Decoder

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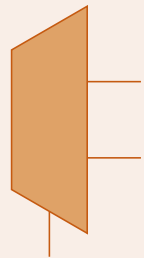
1:n Decoder

1:2 Decoder



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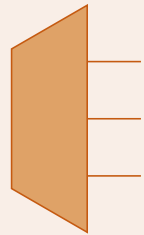
1:n Decoder

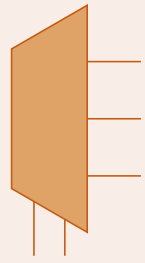
1:3 Decoder



Muxes, Decoders, Shifters - 2

1:n Decoder

1:3 Decoder



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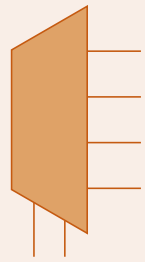
1:n Decoder

1:4 Decoder



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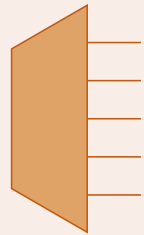
1:n Decoder

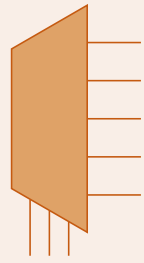
1:5 Decoder



Muxes, Decoders, Shifters - 2

1:n Decoder

1:5 Decoder



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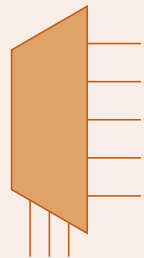
1:5 Decoder



n : 1 Decoder

A combinational logic circuit having n data outputs, and $\lceil \log_2 n \rceil$ control inputs that specify which one of the outputs is 1 (remaining outputs being 0)

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Think About It

- Construct a 2:1 mux using tristate buffers

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Think About It

- Construct a 2:1 mux using tristate buffers
- Is it possible for all output of a decoder to be zero in case of a:
  - 2:4 decoder?
  - 2:3 decoder?