DIGITAL DESIGN AND COMPUTER ORGANIZATION

Adder, Subtractor, Overflow - 4

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Course Outline

- Digital Design
  - Combinational logic design
    - ★ **Adder, Subtractor, Overflow - 4**
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered
- Overflow Logic
  - Unsigned Addition
  - Twos's Complement Addition

Why Overflow

- Logic circuits have fixed bit widths
  - ▸ Ex. 64-bit processor
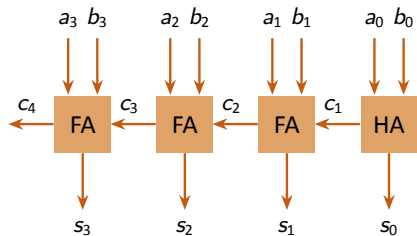 - ▸ Addition / Subtraction done on fixed bitwidth numbers

Overflow

When result of an operation does not fit in the fixed bitwidth, **overflow** is said to occur

Overflow (Unsigned Addition / Subtraction)
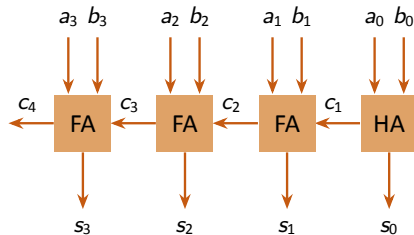
- **Addition** Carry out for msb is 1 indicates overflow

- ▶ For 4-bit adder above, whenever c_3 is 1, it indicates overflow
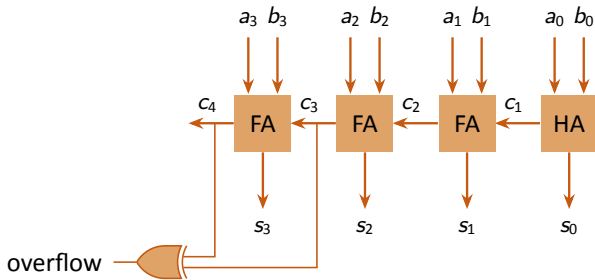
Two's complement addition

- No overflow when numbers have opposite signs (or one/both are zero)
- Overflow can occur when
  - When both positive
    - ★ msb is 1 (c_{msb-1} is 1)
    - ★ c_{msb-1} is 1 and c_{msb} is 0
  - When both negative
    - ★ msb is 0 (c_{msb-1} is 0)
    - ★ c_{msb-1} is 0 and c_{msb} is 1
  - overflow = $c_{msb} \oplus c_{msb-1}$

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Think About It

- Consider the 4-bit numbers 1100 and 0100
  - If the numbers are unsigned binary, then does the addition of the two numbers produce an overflow
  - If the numbers are two's complement binary, then does the subtraction of the latter number from the former result in an overflow?