2 Marks Questions:

1. Construct the logic circuit of a 2:1 mux using only two input NAND gates. How many gates are required? Briefly justify your answer.

Solution:

Function Table:

Selection Input (s)	Output
0	A
1	B

- **A and B are data input lines**

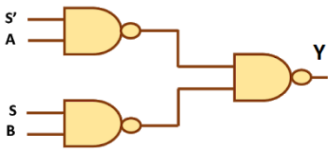
Equation

$$Y = (s' A + s B)$$

With NAND gates

$$Y = ((s'A)'(sB)')' = ((s' A)' (s B)')'$$

Circuit Diagram

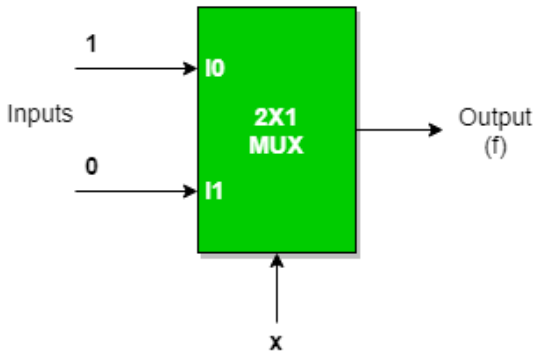


Number of NAND gates required are 3+1(to complement S)

2: Implement NOT gate, AND gate, and OR gate using 2:1 MUX. Show the truth table.

Solution:

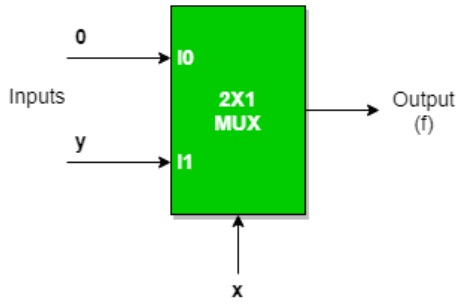
Implementation of NOT gate



Truth Table

x	f
0	1
1	0

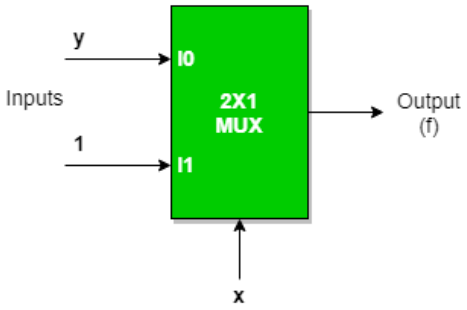
Implementation of AND gate:



Truth Table

x	y	f	f→y
0	0	0	f = 0
0	1	0	
1	0	0	f = y
1	1	1	

Implementation of OR Gate



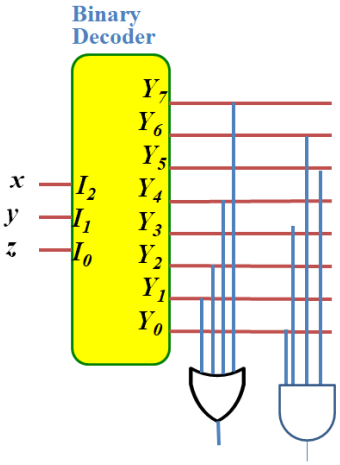
Truth Table

x	y	f	f→y
0	0	0	f = y
0	1	1	
1	0	1	f = 1
1	1	1	

3: Implement Decoder for the equation $f(x, y, z) = \sum(1, 2, 4, 7)$

Solution:

x y z	Output
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1



4: **List few comparison of Combinational logic circuit and sequential Logic Circuit**

Solution:

Combinational Logic Circuit

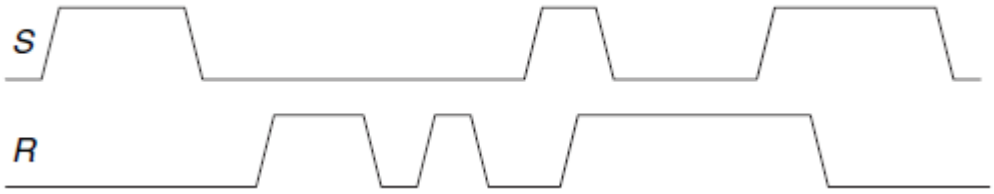
– It has one or more inputs and one or more outputs.
– Its output is determined by the present values of inputs only.
– It does not have a memory.
– It does not have a feedback path.
-Its operation can be described by the truth table.

– It does not have a clock signal.
– It does not depend upon clock transition.
– The circuit is more simpler.
– It is built usling basic gates like, NOT, NAND, AND , OR etc
– Its examples are substaractor, adders, Multilplexers and demultiplexers.

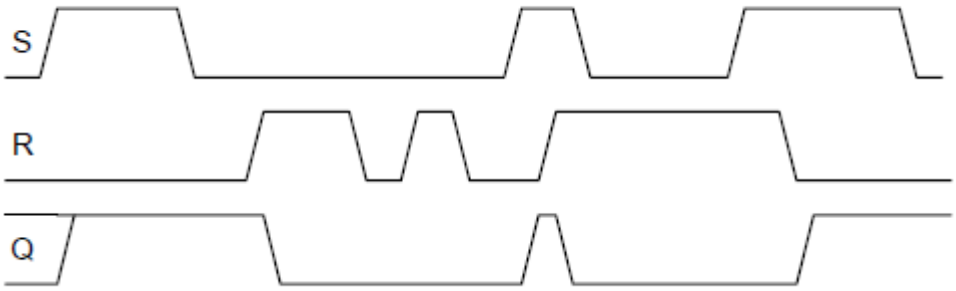
Sequential Logic Circuit :

-It has one or more inputs and one or more outputs.
– Its output is determined by the present values of input as well as the past values of output.
– It has a memory
– It has a feedback path
-Its operation can be described by truth table and timing diagram
– It may be or may not have a clock signal.
– Its action is governed by clock transition
– The circuit is more complex
– It is built using basic gates and combinational gates.
– Its examples include flip flops , shift registers.

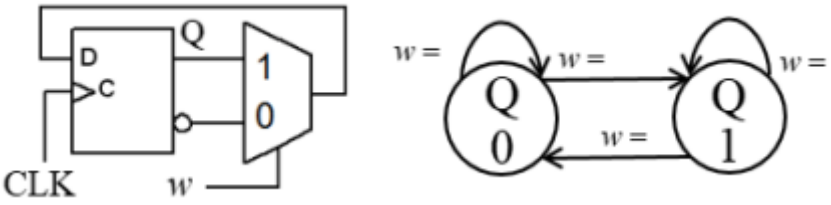
5: Given the input waveforms shown in Figure , sketch the output, Q, of an SR latch.



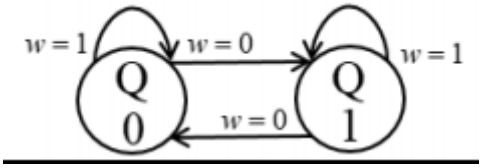
Solution:



6. Write the transition conditions for w at the arrows in the state diagram.



Solution:

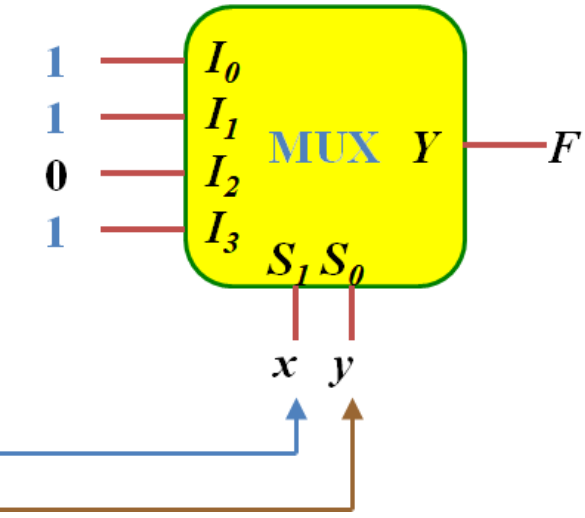


6 Marks

1: Implement MUX for the following equation $F(x, y) = \sum(0, 1, 3)$

Solution:

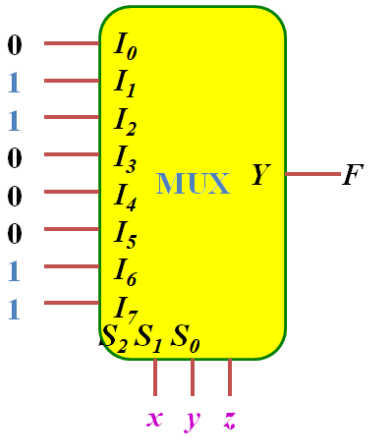
x	y	F
0	0	1
0	1	1
1	0	0
1	1	1



2: Implement MUX for the equation $F(x, y, z) = \sum(1, 2, 6, 7)$

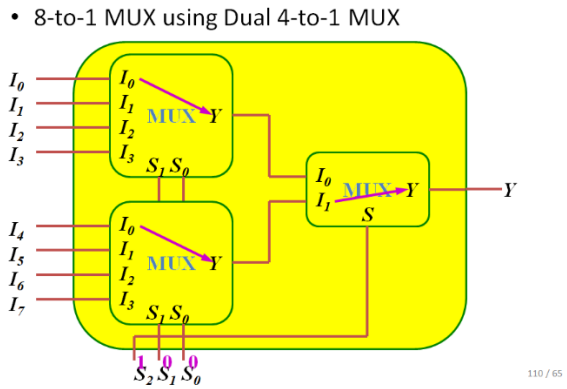
Solution:

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



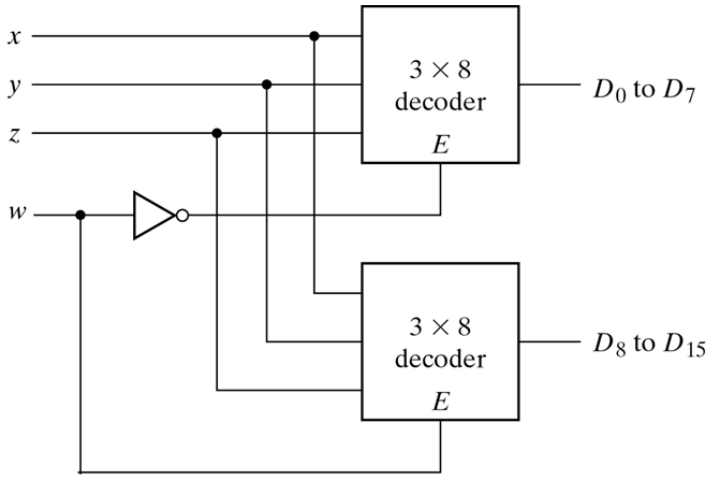
3: Construct 8:1 MUX using two-4:1 MUX and one 2:1 MUX

Solution:

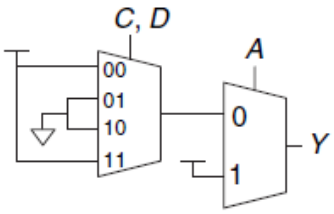


4: Design 4:16 decoder using two 3:2 decoder

Solution:



5: Write a minimized Boolean equation for the function performed by the circuit



Solution:

$$Y = A + \overline{C \oplus D} = A + CD + \overline{C}\,\overline{D}$$