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PES UNIVERSITY

PES University, Bangalore
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UE14CS253

MAY 2016: END SEMESTER ASSESSMENT (ESA) B.TECH. IV SEMESTER

UE14CS253- Microprocessors & Computer Architecture

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1. a) Is **FIQ exception or interrupt** accepted by the ARM processor, **while** the data abort exception is **currently** being serviced ? Explain. **04**

b) **06**

i. Mention the addressing mode used in the following instructions.

i. `LDR R0, [R1, R2] !`

ii. `STR R0, [ R1, #32]`

What is the effective address of the operand if **R1and R2 initial** contains are **0x00001048** and **32** respectively.

What does register **R0 and R1** contain after the execution of the every instruction?

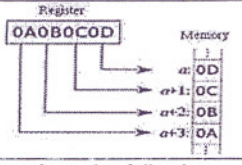
Consider memory location 0x1048, 0x1068 contains **0x2080** and **0x3080** respectively.

ii. Consider the following code snippet. Array A is stored from location **0x00001048.**

```
    ADR R5, A
LOOP: LDR R6, [R5]
    ADD R5, R5, #4
    SUB R6, R6, #1
    BNE LOOP
```

Rewrite the above code snippet to access the elements in the array A using post indexed addressing mode.

c) **04**



Consider the figure.

What **method of memory storage** is shown in the figure?

Does ARM processor support the other type also?

Show how the data **0x0A0B0C0D** is stored in both the methods.

d) Differentiate the following. **06**

LDMFD R13! , { R0,-R4, R12, PC } and **LDMFD R13! , {R0-R4, R12, PC}^ .**

BL Loop and **BGE Loop ,** Assume the condition to be true.

2. a) Write the ARM ALP conditional code snippet for the following statements written in C–language. Assume R1 to Rn as variables. **06**

Let R1, R2, R3 contain the starting addresses of arrays X, Y and Z respectively.

Use Register R4 for variable i. Display appropriate messages.

```
While ( i ++ <= 10 )
{
  If ( X [ i ] == Y [ i ] )
      Z [ i ] = X [ i ] * Y [ i ] ;
  else Z [ i ] = X [ i ] + Y [ i ] ;
}
```

b) i. Write a program to display a message **"This is an examination Question"** on the screen using a function sub program. **06**

Note the following:

Address of the string to be passed as a register parameter to the function.

Display one character at a time.

Use appropriate interrupt number to display a character.

Write the equivalent code snippet to display the above message using a single instruction in the subroutine by calling appropriate routine.

c) Consider the following **04**

1110 - AL, GE - 1010 , LE - 1101, RSB - 0011, AND - 0000.

What ARM instructions does this represent?

Inst	Condition	F (format)	I (immediate)	OPCODE	S (Set cond Code)	Rn	Rd	Operand2
i.	1010	0	0	3	0	0	1	2
ii.	1101	0	1	0	1	2	3	#12

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	d)	i. **Consider a 32 bit barrel shifter.** Write the diagonal lines that are activated when the following instructions are executed. i. SUB R0, R5, R7, LSR #6 ii. AND R5, R6, R7, ROR #12 ii. Use **only ADD / SUB / RSB** instructions to multiply a **number by 17.** {Assume the number in the register **R9, that is R9 = R9 x 17**}.	04
3.	a)	Consider a **Von Neumann architecture.** A machine may have only one register file write port, but under certain conditions, the pipeline might want to perform two writes in one clock cycle. **Is it possible?** What type of hazard is introduced? **How can this hazard be resolved?** Explain with a neat diagram.	06
	b)	Consider the following sequence of instructions. **LDR R1, # 0 [R2]** **SUB R4, R1, R5** **AND R6, R1, R7** **OR R8, R1, R9** During the execution of these instructions using a five stage pipeline architecture, **what hazards occur?** Which instructions are affected? How are those hazards resolved? Explain using diagram that shows various instructions being executed in different clock cycles. **Meaning : CC1 CC2 CC3 .....** **Instruction1 Fetch Decode Execute Memory-access Reg WB** **Instruction2 Fetch Decode Execute Memory-access Reg WB**	06
	c)	What is **pipeline scheduling**? Generate the ARM instruction code for the statements given below in C language. Assume A,B,C,D,E,F are in registers R1 to R6 respectively. Show which instructions have been scheduled and what is the advantage? **A = B + C ;** **D = E – F ;**	04
	d)	What happens when a **branch hazard** occur? Explain with an example.	04
4.	a)	Consider the following program written in **C-Language** for memory locality properties of matrix computation, where the elements are stored in **row major order.** **for (I = 0; I < 1000; I++)** **for (J = 0; J < 8; J++)** **A [I] [J] = B [J] [0] + A [J] [I].** How many **32-bit integers** can be stored in a **16 byte cache line**? References to which variables **exhibit temporal** locality? References to which variables **exhibit spatial** locality? Does the locality gets affected if the order of reference changes to **column major order** to access matrix elements?	04
	b)	Caches are important in providing a high performance memory hierarchy to processors. Consider the following sequence of memory references given as word addresses. **1, 134, 212, 1, 135, 213** For each of these references, identify **the binary address, the tag** and **the block** given a direct mapped cache with **16 two-word blocks.** Also, list if **each reference** is a **hit or a miss**, assuming the **cache is initially empty.**	06
	c)	What happens if the **data** in the disk and main memory **changes** and the **write-back protocol** is being used?	04
	d)	Consider the equation for computation of **Average memory Access Time.** Mention the parameters and discuss the **parameters** in the equation for **up gradation** of CPU performance.	06
5.	a)	Assume the memory system takes **105 clock cycles of overhead** and then delivers **32 bytes every 4 clock cycles.** Also, **hit time is 1 clock cycle** Compute the time taken to transfer **32 bytes and 64 bytes.** Compute **Average Memory Access Time** for the cache size 7.24% of 4K cache size.	03
	b)	What is an interrupt vector table? Explain IVT with respect to ARM processor.	03
	c)	How does user enable and disable FIQ and IRQ interrupts? **{ write the code only }**	05
	d)	**Write short notes on the following** i. Translation Look aside Buffer ii. Memory Hierarchy iii. Dirty or Modified bit used in cache memory.	09