QUESTIONS UNIT 3

1. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory.
2. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory.

3. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.
   (a)Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.
   (b) When a program is executed, the processor reads data sequentially from the following word addresses: **128, 144, 2176, 2180, 128, 2176**
   All the above addresses are shown in decimal values. Assume that the cache is initially empty.
   For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

4. Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag.

5. Consider a 8-way set associative cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find the Size of main memory.

6. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory

7. Consider a 4 way set associative cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory

8. A computer system uses 16-bit memory addresses. It has a 2K-byte

cache organized in a 2-way set associative manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

9. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

   (b) When a program is executed, the processor reads data sequentially from the following word addresses: **128, 144, 2176, 2180, 128, 2176**

   All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.