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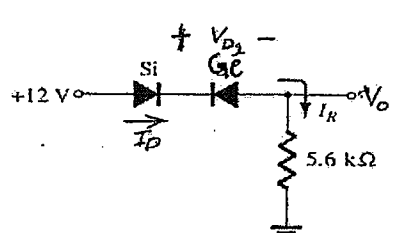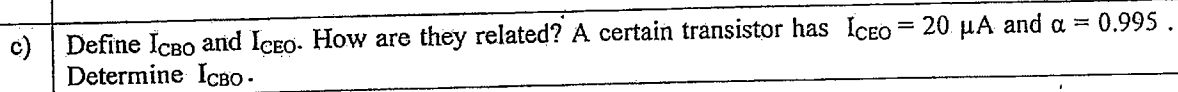
UE16EC101

MAY 2017: END SEMESTER ASSESSMENT (ESA) B.TECH. II SEMESTER
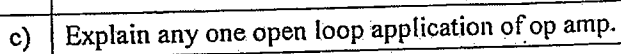
UE16EC 101- BASIC ELECTRONICS

Time: 3 Hrs	Answer All Questions	Max Marks: 100

1	a)	Name the 3 types of resistances associated with the diode? Derive the expression for the dynamic resistance of the diode.	6
	b)	The reverse saturation current of a Si diode is 5 nA at a temperature of 300K. Find the diode current and its dynamic resistance at 60^0C and $V_D = 0.5$ V.	4
	c)	With a neat diagram, explain the basic construction and working of an LED. Why is called IR LED? Justify. Given Energy gap for Ga As = 1.43 eV.	6
	d)	Determine I_D, V_{D2}, and V_O for the circuit shown.	4
2	a)	With neat Circuit diagram and waveforms explain the working of bridge rectifier. Write the expression for the output dc voltage V_{dc} and PIV rating of the diode.	8
	b)	Draw the circuit diagram of a center tapped FWR with capacitor filter. Calculate the percentage ripple for the voltage developed across a 120 µF filter capacitor when providing a load current of 80 mA. The full wave rectifier operating from 60 Hz supply develops a peak rectified voltage of 25 V.	7
	c)	Design a zener regulator that will maintain the output voltage at 20 V across a 1 KΩ resistor. Input varies between 30 V to 50 V. Find R_s and $I_{z max}$.	5
3	a)	Simplify the following Boolean expression and realize the simplified expression using NOR gates. $$Y = (\overline{A}\ \overline{C} + \overline{B}\ C)\ \overline{(A\overline{B} + AB\overline{C})}$$	5
	b)	Draw the circuit diagram of a Full-Adder using NAND gates. Write its output equations and its truth table.	5
	c)	Draw the logic diagram and the truth table of a clocked RS flip-flop. How to convert the same into a clocked D flip-flop and what is the advantage of it?	6
	d)	Realize a 3-input XOR gate using 4-to-1 MUX.	4
4	a)	Draw the output characteristics of CB configuration marking 3 regions of operation. State the biasing conditions for these regions and explain behavior of transistor in these regions along with the output current equation for active region.	9

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b)	Given that $I_{CQ} = 2$ mA and $V_{CEQ} = 10$ V, determine R_1 and R_C for the network shown.	7

c)	Define I_{CBO} and I_{CEO}. How are they related? A certain transistor has $I_{CEO} = 20$ µA and $\alpha = 0.995$. Determine I_{CBO}.	4

5	a)	Define the following parameters, write their ideal and typical values for IC741. 1. Input resistance 2. CMRR 3. Slew Rate	6

b)	Identify the stages and find the output voltage. Given $V_1 = 0.1$ V.	8

c)	Explain any one open loop application of op amp.	6