DIGITAL DESIGN AND COMPUTER ORGANIZATION

Dr. Reetinder Sidhu
Department of Computer Science and Engineering

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Multi-Cycle Processor - 3

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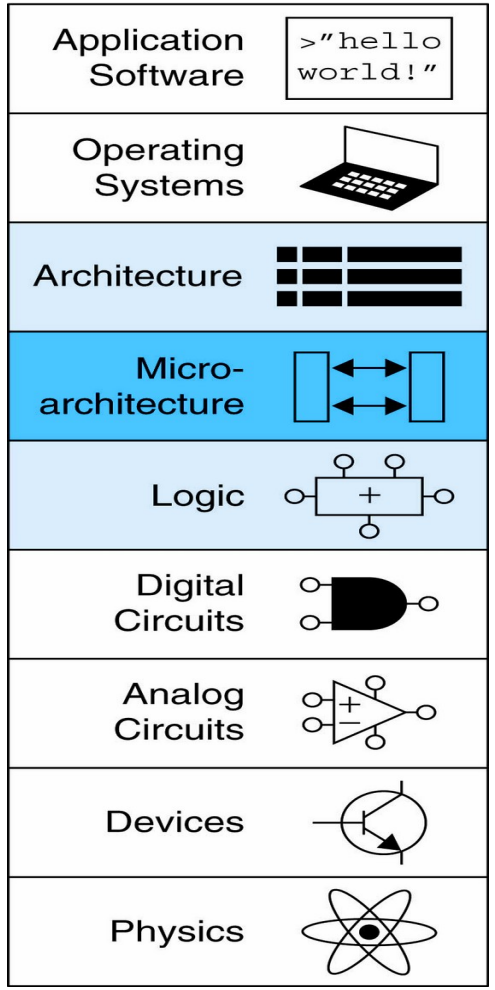
Outline

- **Introduction**
- **Performance Analysis**
- **Multicycle Processor Datapath**
- **Multicycle Processor Control Logic**



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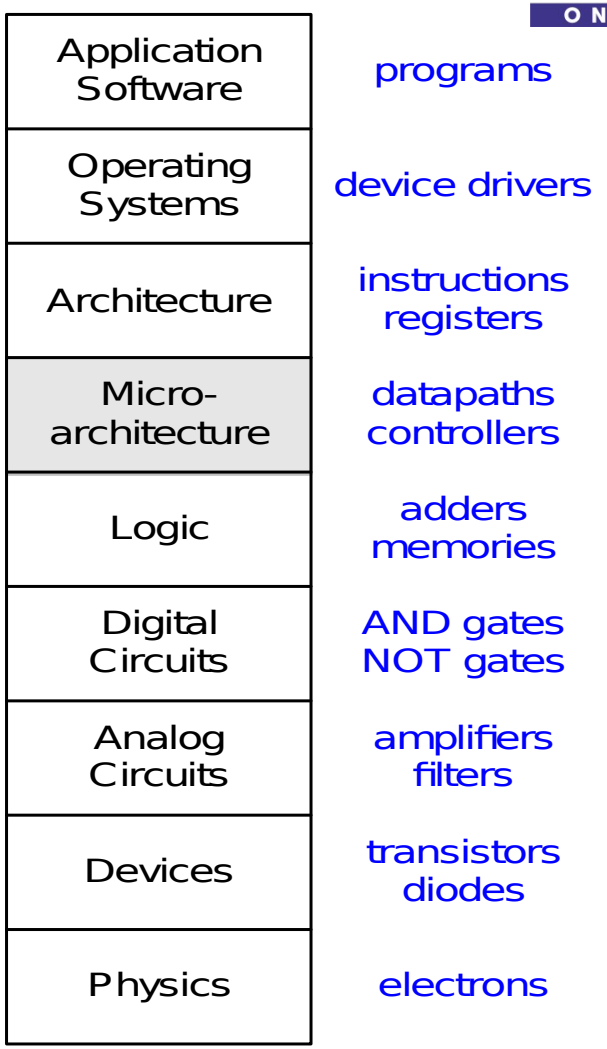
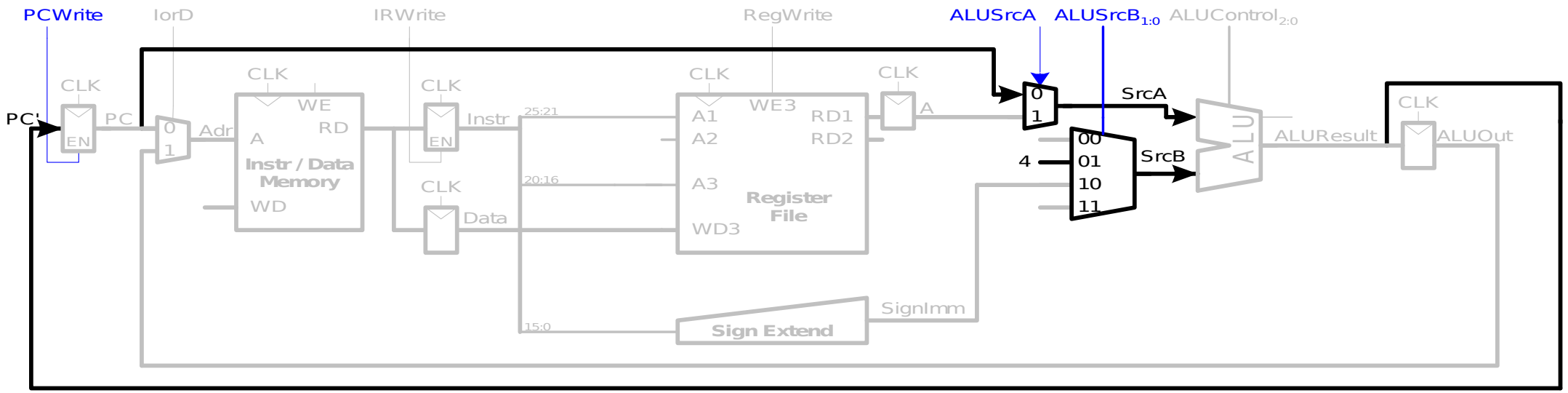
Introduction

- **Microarchitecture:** how to implement an architecture in hardware
- Processor:
  - **Datapath:** functional blocks
  - **Control:** control signals



lw Instruction Datapath

STEP 6: Increment PC



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Other Instructions

- sw
- R-type (add, sub, and, …)
- beq

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sw Instruction

- Address computation same as for lw
- Register contents to be written to main memory
- So steps 1, 2 and 3 same as for lw
- Step 4: Register contents to be written into computed memory address

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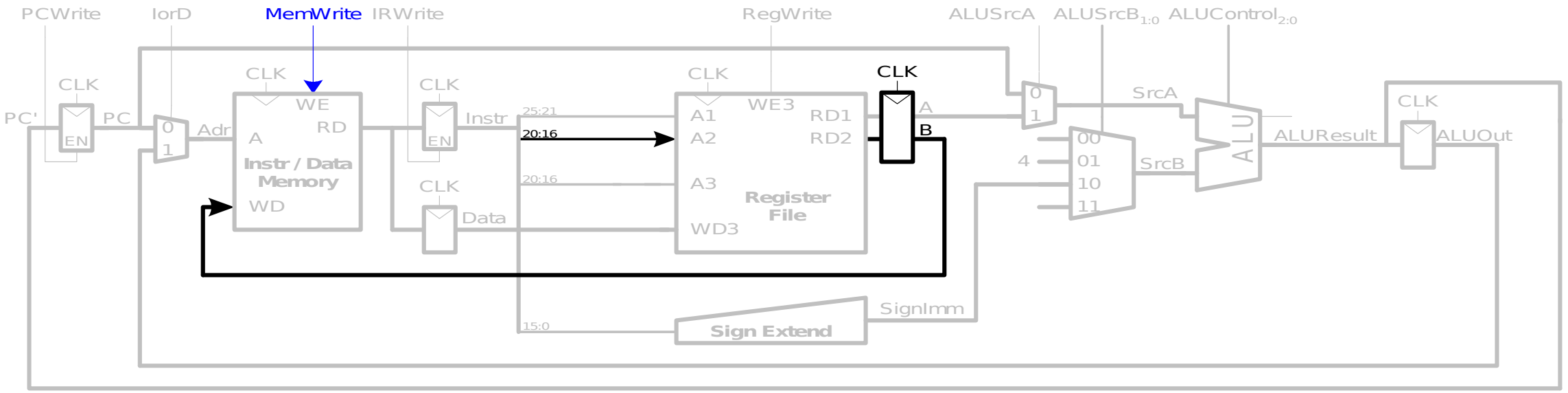
Multicycle Datapath: sw

Write data in rt to memory



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R-type Instruction

- Step 1 (fetch): Same as for lw
- Step 2: Similar to lw
- Step 3: Write ALU output into destination register

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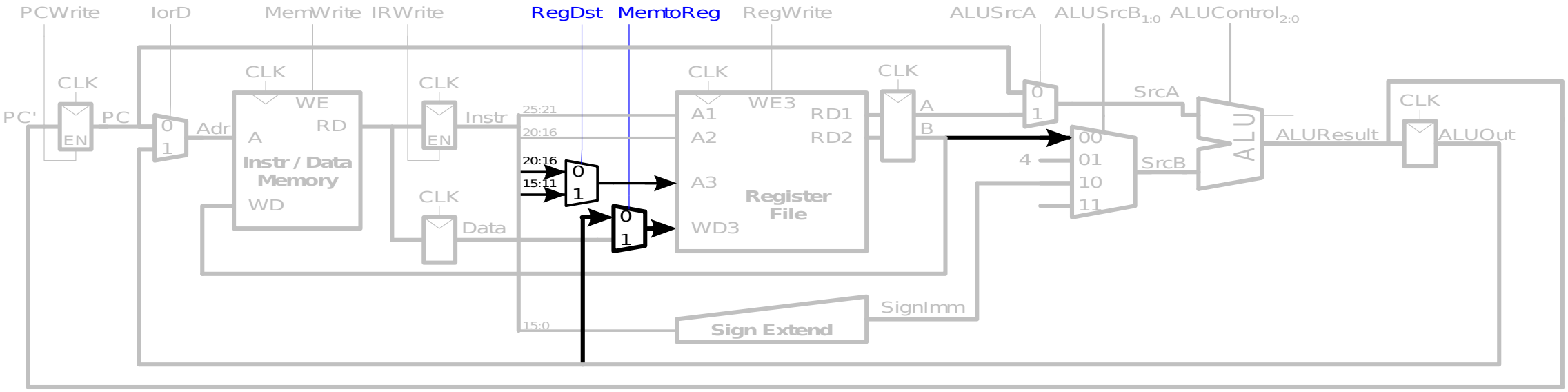
Multicycle Datapath: R-Type

- Read from `rs` and `rt`
- Write *ALUResult* to register file
- Write to `rd` (instead of `rt`)



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beq Instruction

- Step 1: Fetch
- Step 2: Compare register contents
- Step 3: Change PC contents (if registers equal)

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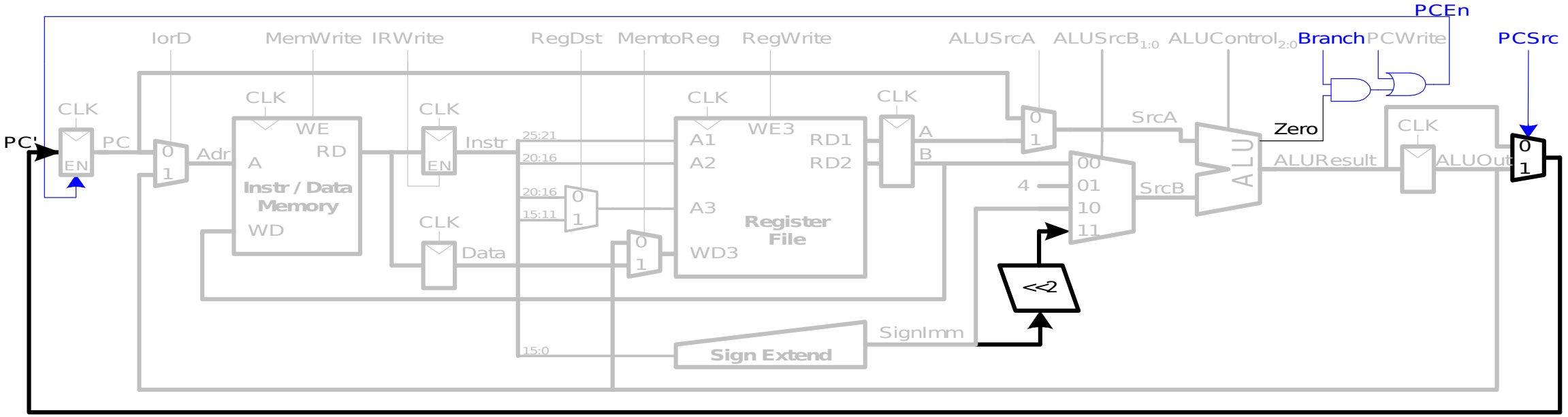
Multicycle Datapath: beq

- `rs == rt?`
- BTA = (sign-extended immediate << 2) + (PC+4)



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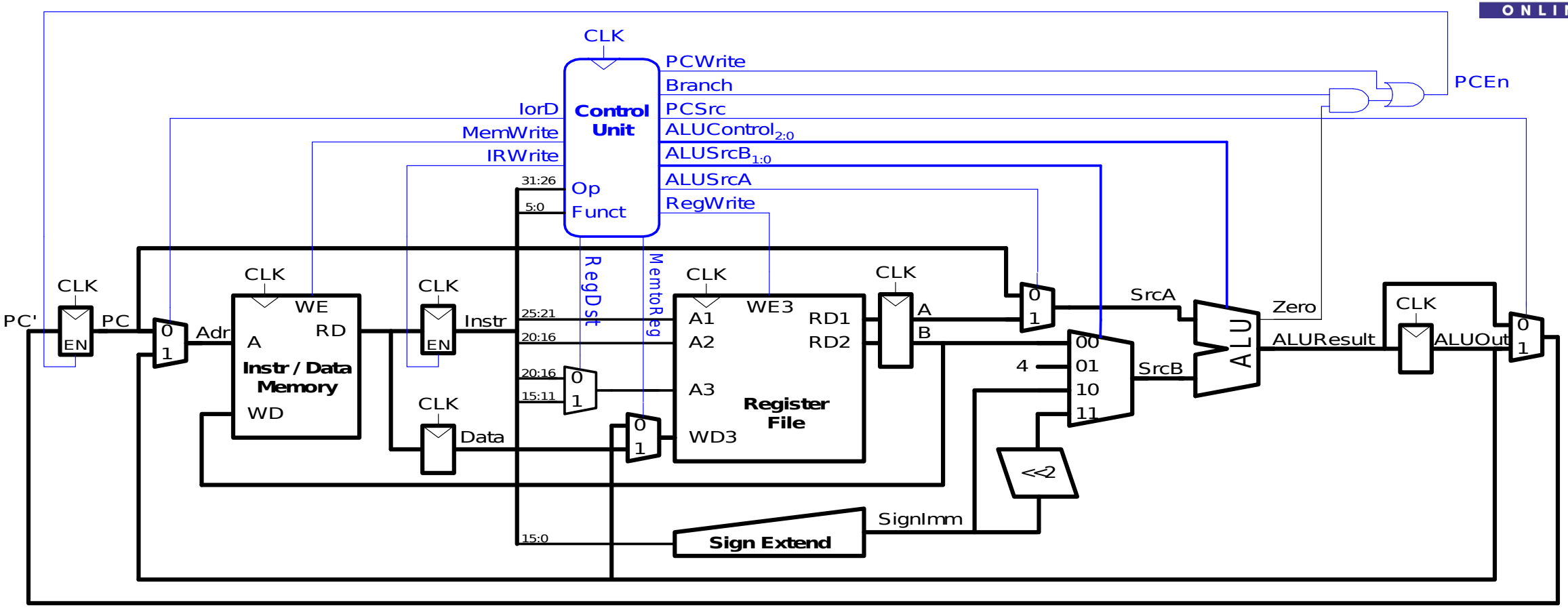
Multicycle Processor



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Multicycle Control