Digital Design and Computer Organization

Adder, Subtractor, Overflow - 2

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
    - **Adder, Subtractor, Overflow - 2**
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Logic Circuit for Addition
  - Half Adder
  - Full Adder

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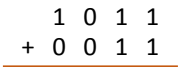

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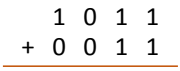

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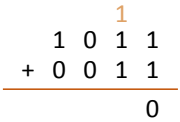

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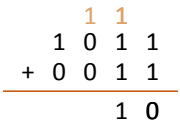

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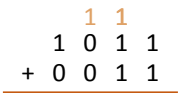

Adder, Subtractor, Overflow - 2

Adder, Subtractor, Overflow - 2

```
    1 1
  1 0 1 1
+ 0 0 1 1
-------
  1 1 1 0
```

- Inputs
  - Four inputs for one number
  - Four inputs for the other number
- Outputs
  - Four sum outputs
  - One carry output

Adder, Subtractor, Overflow - 2

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    1 1
  1 0 1 1
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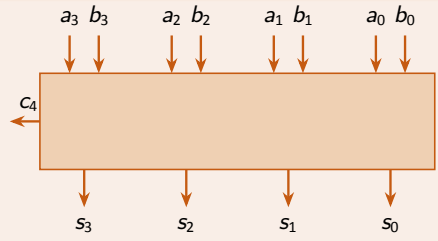
Structure of Logic for Addition



Adder, Subtractor, Overflow - 2

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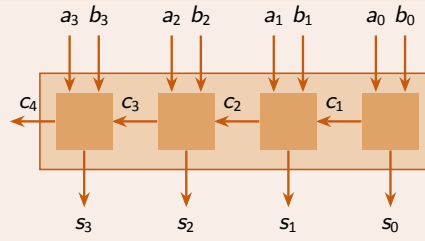

Adder, Subtractor, Overflow - 2

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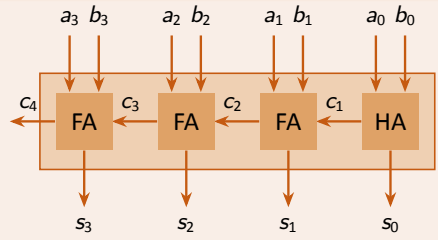
Structure of Logic for Addition



- Half Adder (HA) for least significant bit
- Full Adder (FA) for remaining three bits

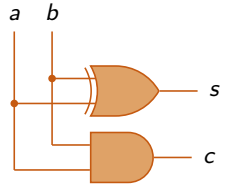
Adder, Subtractor, Overflow - 2

Half Adder

a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- SOP formulas:
  $s = \overline{a}b + a\overline{b}$
  $c = ab$
- Usually written in terms of XOR function as:
  $s = a \oplus b$
  $c = ab$

- Half adder logic circuit:



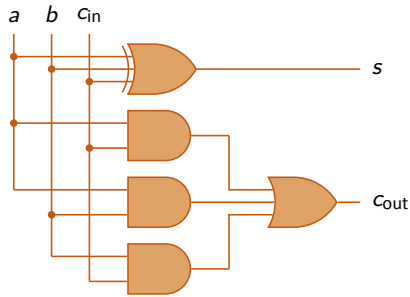
Adder, Subtractor, Overflow - 2

Full Adder

a	b	c_{in}	s	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- Minimizing (using Boolean identities or K-Maps) yields the SOP formulas:
  $s = \overline{a}\overline{b}c + \overline{a}b\overline{c} + a\overline{b}\overline{c} + abc$
  $c = ab + bc + ca$
- Usually written in terms of XOR function as:
  $s = a \oplus b \oplus c$
  $c = ab + bc + ca$

- Full adder logic circuit:



Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

$$\begin{array}{r} 1\ 0\ 0\ 1 \\ -\ 0\ 0\ 1\ 1 \\ \hline \end{array}$$

Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

$$\begin{array}{r} 1\ 0\ 0\ 1 \\ -\ 0\ 0\ 1\ 1 \\ \hline \end{array} \qquad \begin{array}{r} 9 \\ -\ 3 \\ \hline 6 \end{array}$$

Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

$$\begin{array}{r} 1\ 0\ 0\ 1 \\ -\ 0\ 0\ 1\ 1 \\ \hline 0 \end{array} \qquad \begin{array}{r} 9 \\ -\ 3 \\ \hline 6 \end{array}$$

Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

$$\begin{array}{r} \,1 \\ \,1\;0\;0\;1 \\ -\;0\;0\;1\;1 \\ \hline \,1\;0 \end{array} \qquad \begin{array}{r} \,9 \\ -\;3 \\ \hline \,6 \end{array}$$

Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

```
  1 1
  1 0 0 1
- 0 0 1 1
---------
    1 1 0
```

```
  9
- 3
---
  6
```

Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

```
  1 1
  1 0 0 1
- 0 0 1 1
---------
  0 1 1 0
```

```
  9
- 3
---
  6
```

Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

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  1 1
  1 0 0 1
- 0 0 1 1
---------
  0 1 1 0
```

```
  9
- 3
---
  6
```

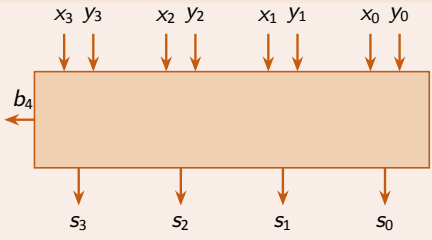
Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

$$\begin{array}{r} {\scriptstyle 1\ \ 1\ \ \ \ } \\ 1\ 0\ 0\ 1 \\ -\ 0\ 0\ 1\ 1 \\ \hline 0\ 1\ 1\ \mathbf{0} \end{array} \qquad \begin{array}{r} 9 \\ -\ 3 \\ \hline 6 \end{array}$$

Structure of Logic for Subtraction



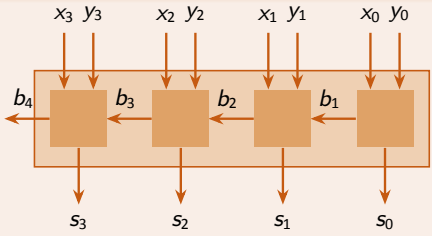
Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

```
  1 1
  1 0 0 1        9
- 0 0 1 1      - 3
-------------  ---
  0 1 1 0        6
```

Structure of Logic for Subtraction



Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

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  1 1
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-------------  ---
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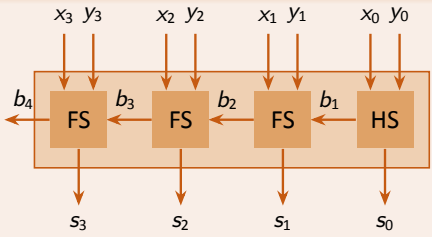
Structure of Logic for Subtraction



- Half Subtractor (HS) for least significant bit
- Full Subtractor (FS) for remaining three bits

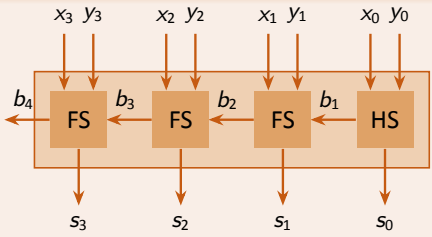
Adder, Subtractor, Overflow - 2

Think About It

Binary Subtraction Example

```
  1 1
  1 0 0 1        9
- 0 0 1 1      - 3
-------------  ---
  0 1 1 0        6
```

Structure of Logic for Subtraction



- Half Subtractor (HS) for least significant bit
- Full Subtractor (FS) for remaining three bits
- Construct logic circuits for HS and FS