SRN

PES UNIVERSITY

PES University, Bangalore

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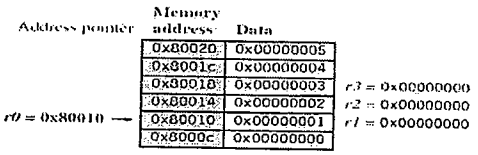
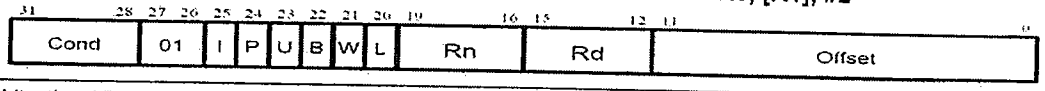
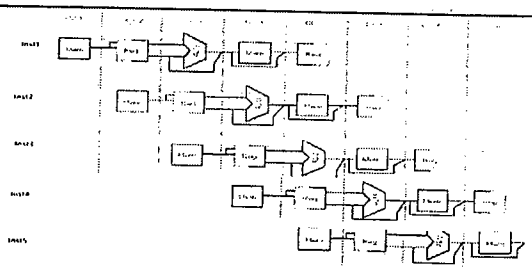
UE15CS253

MAY 2017: END SEMESTER ASSESSMENT (ESA) B.TECH. IV SEMESTER

UE15CS253- Microprocessors & Computer Architecture

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	Differentiate the following i. Microprocessors and Microcontrollers ii. RISC and CISC with respect to processor architecture	04
	b)	i. Write an instruction using ARM - ISA to demonstrate • 3-address data processing instruction • conditionally executable • Ability to perform general shift and general arithmetic operation. ii. "ADR and LDR are same".- True / False Justify accordingly.	06
	c)	Write an instruction sequence using ARM - ISA to multiply a number in register R4 with 124. Do not use multiply instruction.	04
	d)	Write a program using ARM - ISA to **compare two strings** STR1 AND STR2. Let the comparison be character by character in a **function sub program**. Pass the **parameters** STR1 and STR2 to the function. Use **post indexing addressing mode**. Use **conditional execution** instructions.	06
2.	a)	i. Consider the following as the initial content of the memory locations. What will be the final values of these registers after the execution of the instruction: **LDMIB r0!, {r1-r3}**  ii. Write the binary equivalent of the ARM instruction : **LDR R0, [R1], #2**  	03 + 02
	b)	Write the ARM datapath timing diagram representing 2 phase non overlap clock scheme in a CPU clock cycle time. Mention the operations performed during these clock cycle timing.	05
	c)	Mention the signals used for handshaking between a processor and a coprocessor. What are the 4 possible ways to handle once the coprocessor instruction has entered the ARM7TDMI and coprocessor pipelines.	05
	d)	"Every instruction is executed in a clock cycle time". Explain the statement with respect to five stage pipeline of a RISC processor.	05

3.	a)	Consider the following code fragment.
		LOOP: LD R1, 0 (R2)
		ADD R1, R1, #1
		ST R1, (R2, #0)
		ADD R2, R2, #4
		SUB R4, R3, R2
		BNE LOOP
		 
		Data hazards are caused by the data dependencies in the code. Use pipelining timing chart to list all the dependencies in the code above for a 5 stage pipeline RISC processor. How are these data dependencies resolved?
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	b)	Why will designer allow structural hazards?	04
	c)	Consider an unpipelined processor. Assume that it has a 4ns clock cycle and that it uses 16 cycles for ALU operations and branches and 20 cycles for memory operations. Assume that the relative frequencies of these operations are 30%, 40%, and 30%, respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.4 ns of overhead to the clock. Ignoring any latency impact, how much speedup in the instruction execution rate will we gain from a pipeline?	04
	d)	When a branch instruction occurs in a pipeline or a control hazard occurs in the form of an exception (interrupt), what additional hardware is required to overcome the hazard. Which architecture supports the same. What is done to the 5 stage pipeline to reduce two stall cycles?	04
4.	a)	Consider the use of a cache memory system with L1 data cache and main memory. The latencies (in CPU cycles) of different kinds of accesses is as follows. Cache hit: 1 cycle, cache miss : 105 cycles, Main memory access: 200 cycles. When the program with an overall miss rate of 5%, what will the average memory access time (in CPU cycles) be ?	04
	b)	Consider a 32 bit virtual address given by the CPU as 0x00001020. Determine the number of bits [TAG / SET/ BYTE] required to decode to a single memory location in a memory system that has a cache memory of 128 sets with 32 blocks in each set and 64 bytes in each block. Also, compute the capacity of cache memory. If the main memory capacity is 10MB, what is the mapping ratio between the main memory and the cache memory?	04
	c)	**i.** Demonstrate the usage of a write back protocol with buffers in a cache memory system for a read over write operation. **ii.** Read the following sequence of memory operations. Identify the type of cache miss. A. The cache cannot contain all the blocks needed during execution of a program. B. Misses due to flushes to keep multiple caches same in a multiprocessor environment. C. The very first access to block cannot be in the cache. D. A block may be discarded and later retrieved if too many blocks map to its set.	04 + 04
	d)	How can miss penalty be reduced? Explain with an example	04
5.	a)	Assume the memory system takes 100 clock cycles of overhead and then delivers 32 bytes every 2 clock cycles. That is, it can supply 32 bytes in102 clock cycles, 64 bytes in 104 clock cycles, and so on... Which block size has the smallest average memory access time for each cache size? Assume the data from the table shown. Also, mention the type of cache optimization that can be observed from the table. Cache size Block size | 4K 16 | 8.57% 32 | 7.24% 64 | 7.00% 128 | 7.78% 256 | 9.51% Cache size Block size | 4K | 16K | 64K | 256K 64 | 7.00% | 2.64% | 1.06% | 0.51%	06
	b)	Consider the following code sequence. Ex: STR R3, 512 (R0) LDR R1, 1024 (R0) LDR R2, 512 (R0) Assume Direct mapped cache. Write –through cache that maps 512 and 1024 to the same block. Four word write buffer that is not checked on a read miss. Will the value in R2 always be equal to the value in R3? Discuss.	05
	c)	Explain the interrupt handling scheme for a non-nested interrupt .	05
	d)	Identify the type of architecture in the statements mentioned below. " The ability to initiate multiple instructions during the same clock cycle" " Fetches and decodes the incoming instruction stream several instructions at a time" " The architecture exploits the potential of instruction level parallelism". " Data dependencies is the major problem of executing multiple instructions at the same time. " Out of order execution of instructions done with the help of the compiler"	04