Digital Design and Computer Organization

Multi-Cycle Processor - 5

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Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)
    - **Multi-Cycle Processor - 5**

Concepts covered

- Control Logic Structure
- Microarchitecture CPI

Multi-Cycle Processor - 5

Control FSM

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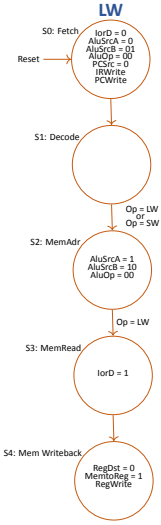
Multi-Cycle Processor - 5

Control FSM



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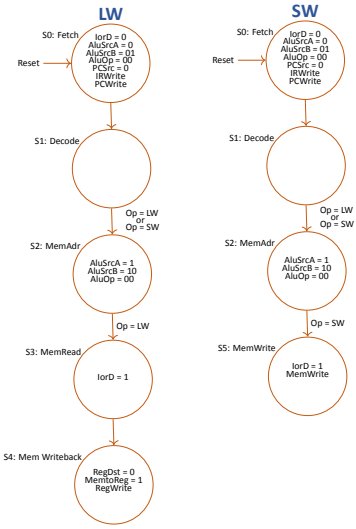
Control FSM



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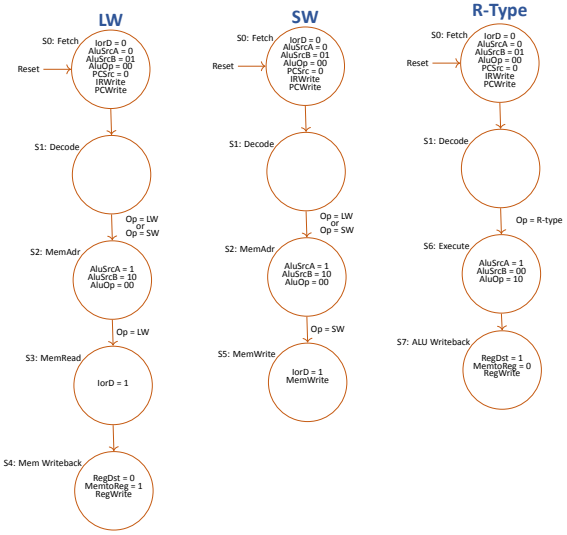

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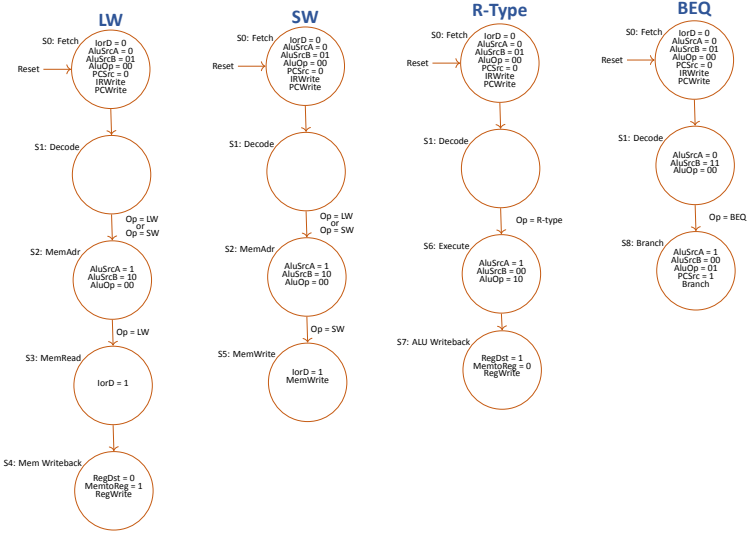

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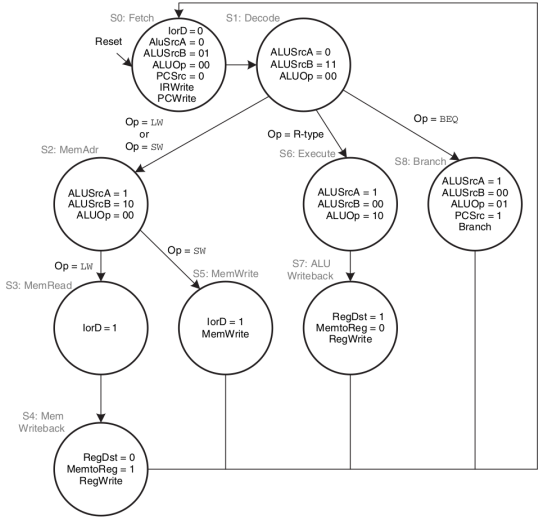
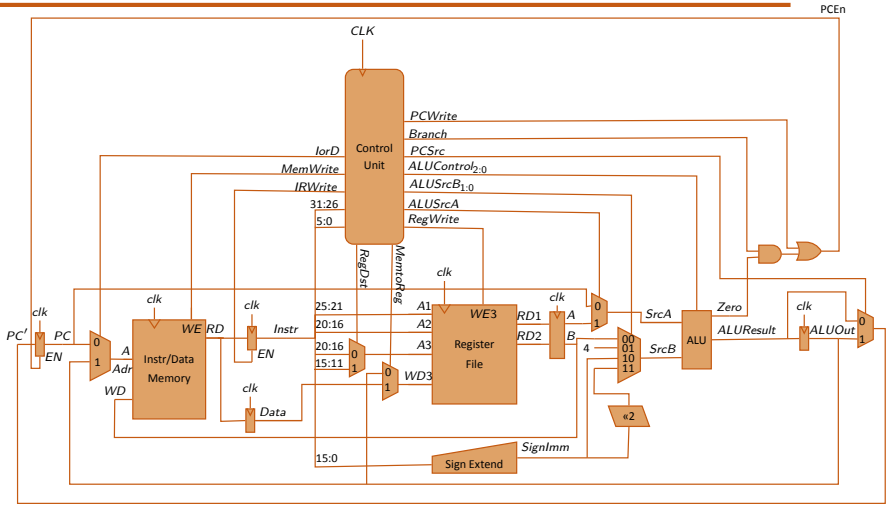
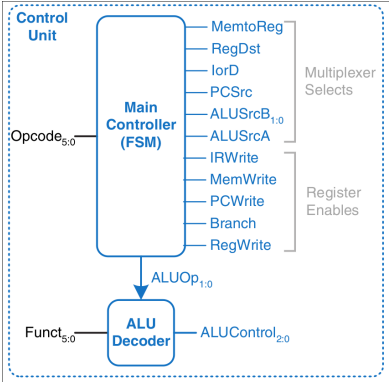


Multi-Cycle Processor - 5
MIPS Multi-Cycle Datapath



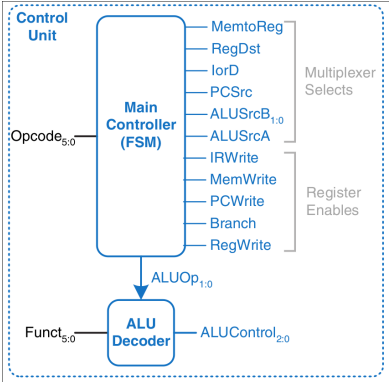
Multi-Cycle Processor - 5
Control Logic

- Control Unit:

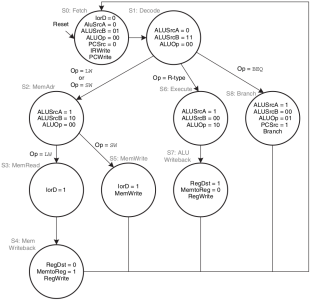


MULTI-CYCLE PROCESSOR - 5
Control Logic

- Control Unit:

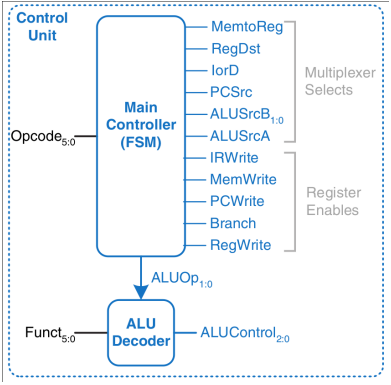


- Main Controller (FSM):



MULTI-CYCLE PROCESSOR - 5
Control Logic

- Control Unit:



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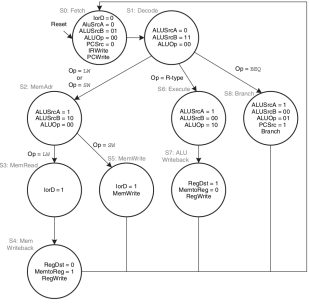

- ALU Decoder:

ALUOp	Funct	ALUControl
00	X	010 (add)
X1	X	110 (subtract)
1X	100000 (add)	010 (add)
1X	100010 (sub)	110 (subtract)
1X	100100 (and)	000 (and)
1X	100101 (or)	001 (or)
1X	101010 (slt)	111 (set less than)

Multi-Cycle Processor - 5
Cycles Per Instruction

Instruction	CPI
lw	5
sw	4
R-type	4
beq	3

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SPECINT2000 CPI

- The SPECINT2000 benchmark consists of approximately 25% loads, 10% stores, 11% branches, 2% jumps, and 52% R-type instructions. Determine the average CPI for this benchmark.

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- The SPECINT2000 benchmark consists of approximately 25% loads, 10% stores, 11% branches, 2% jumps, and 52% R-type instructions. Determine the average CPI for this benchmark.
  - Average CPI = (0.25)(5) + (0.52 + 0.10)(4) + (0.11 + 0.02)(3) = 4.12

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Think About It

- How can a multiplication instruction be supported?
  - Multiplication of two 32-bit registers would produce a 64-bit result
  - What changes to the datapath would be required?