Digital Design and Computer Organization

Memory Arrays - 2

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
    - ★ **Memory Arrays - 2**
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Memory Arrays

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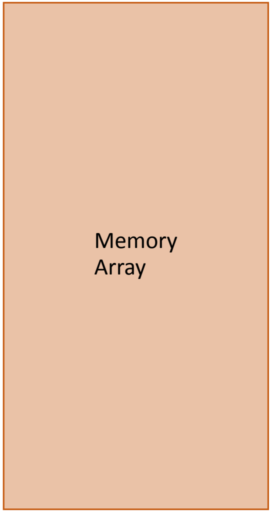

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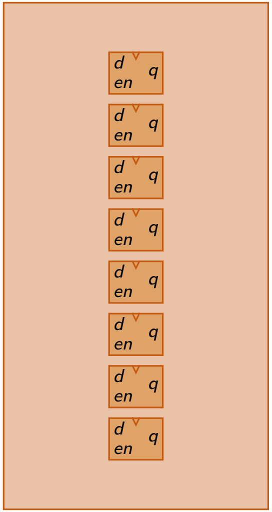

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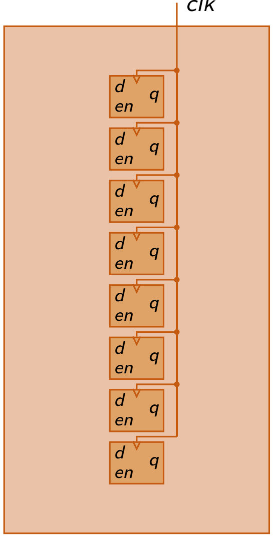

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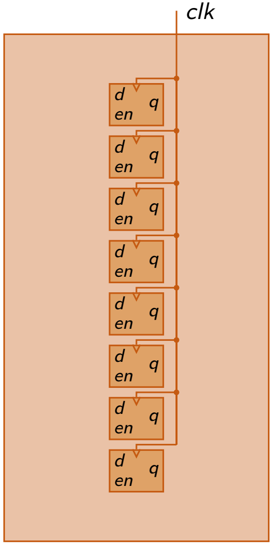
- Read an array location



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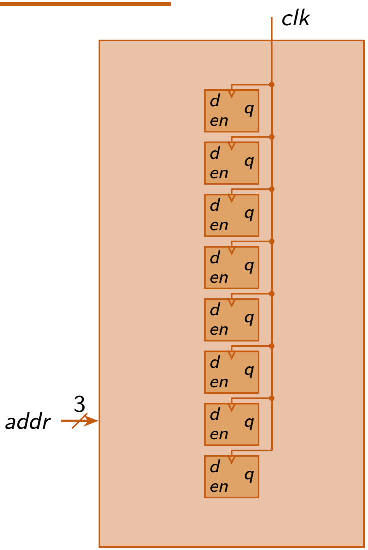

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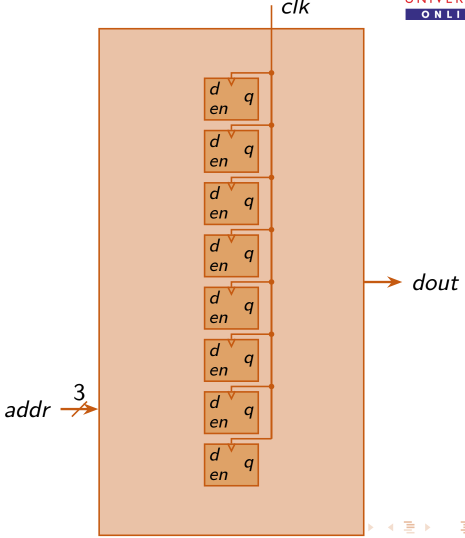

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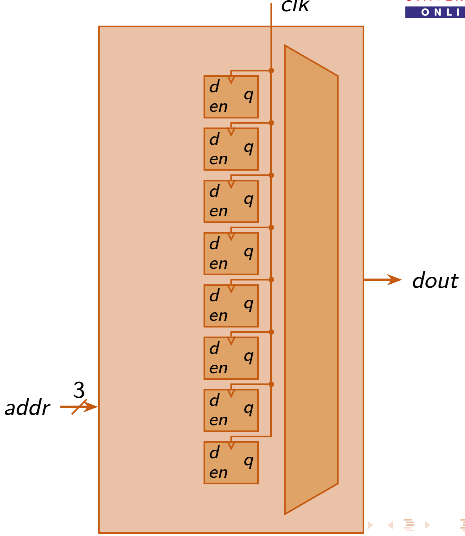

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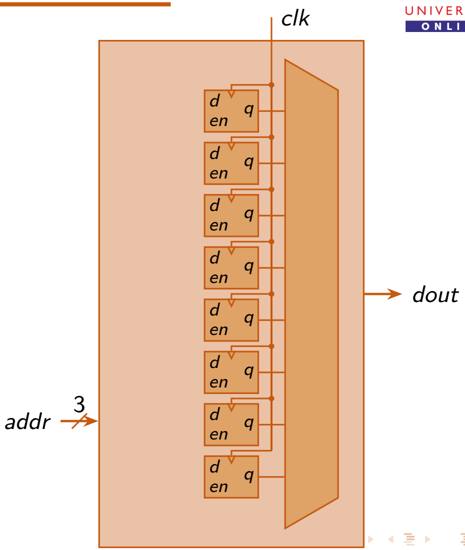

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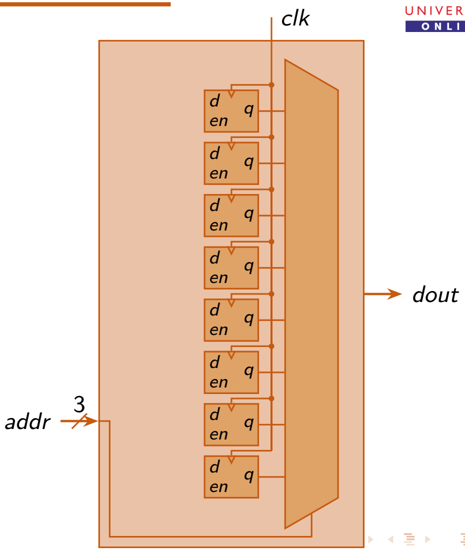

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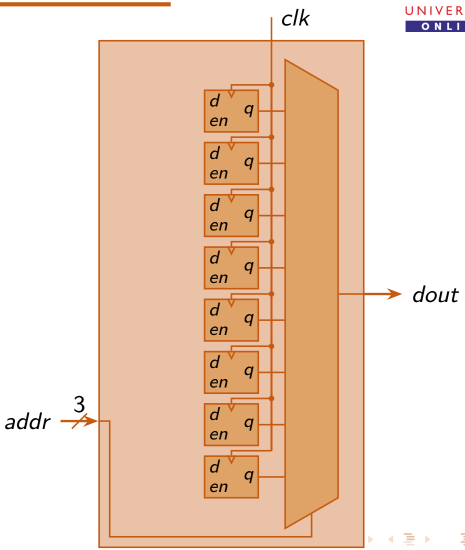

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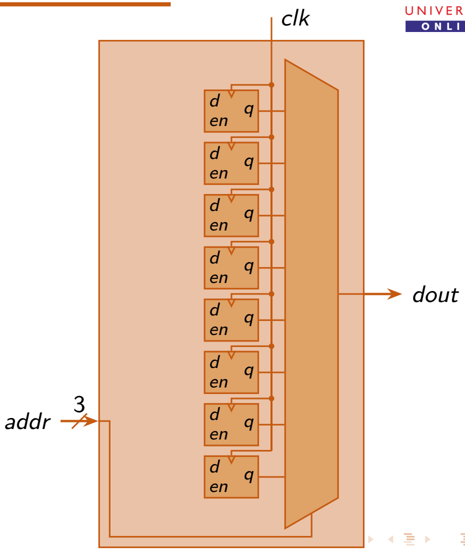

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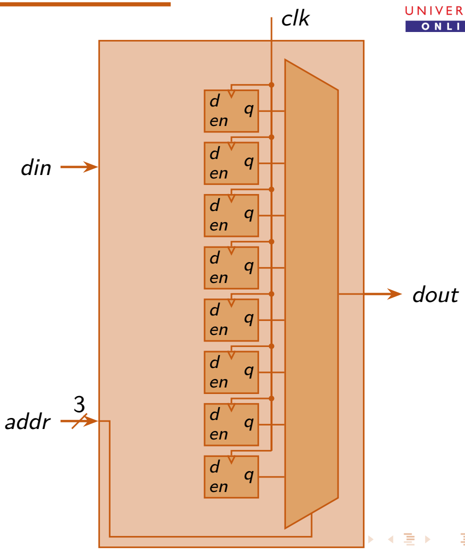

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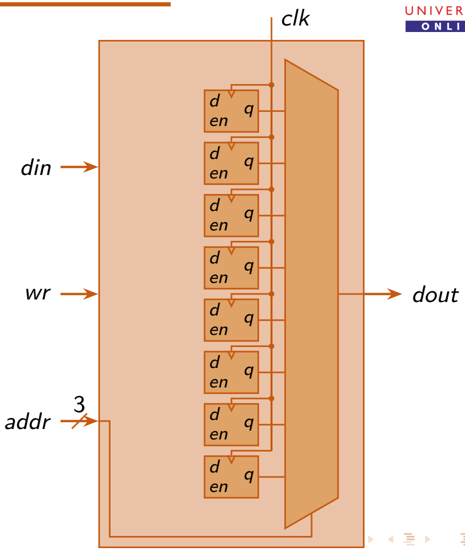

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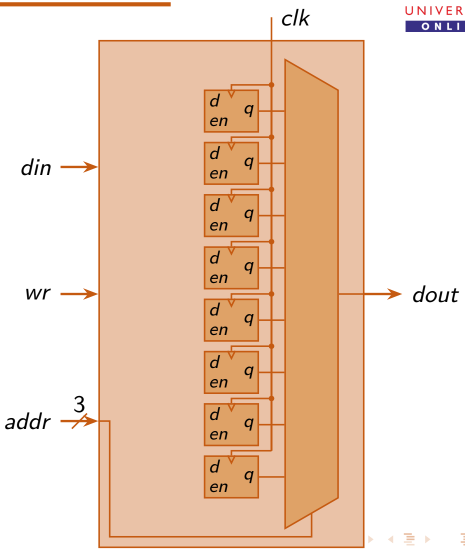

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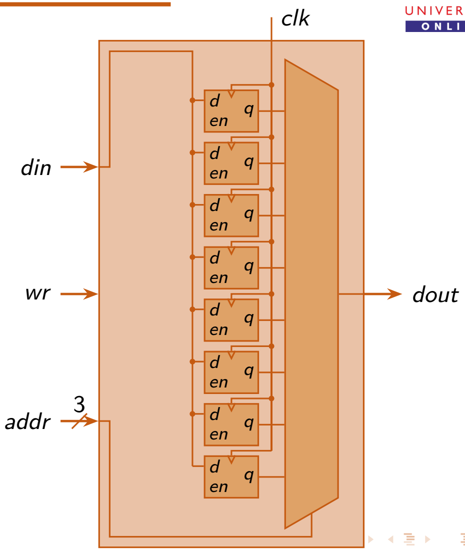

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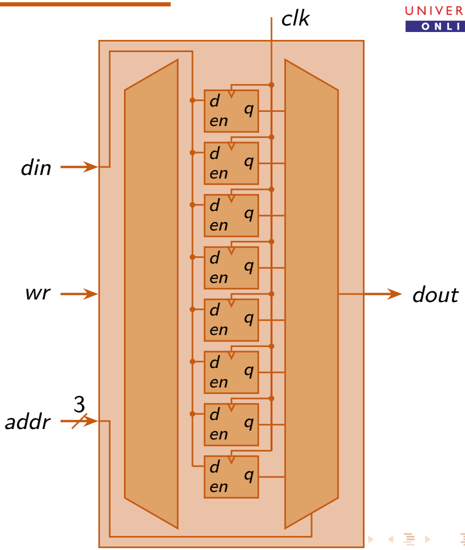

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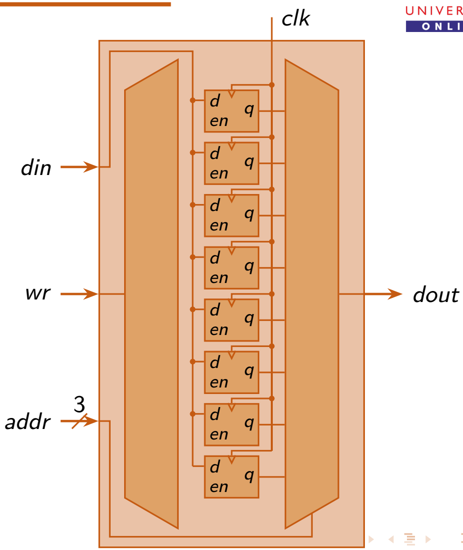

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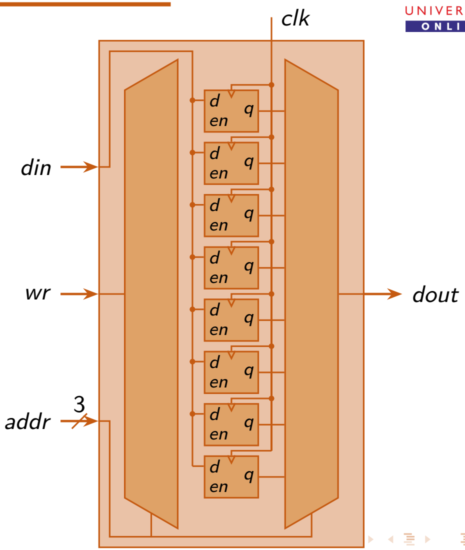

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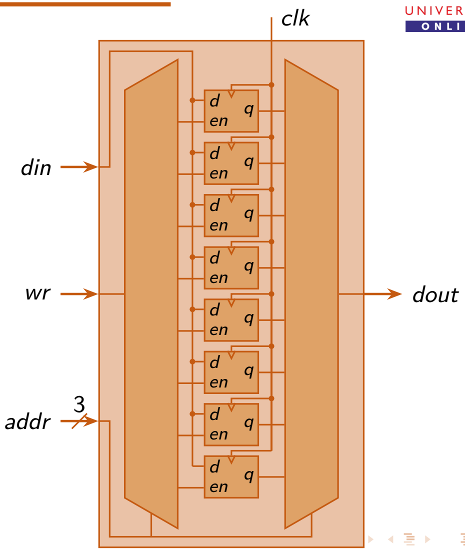

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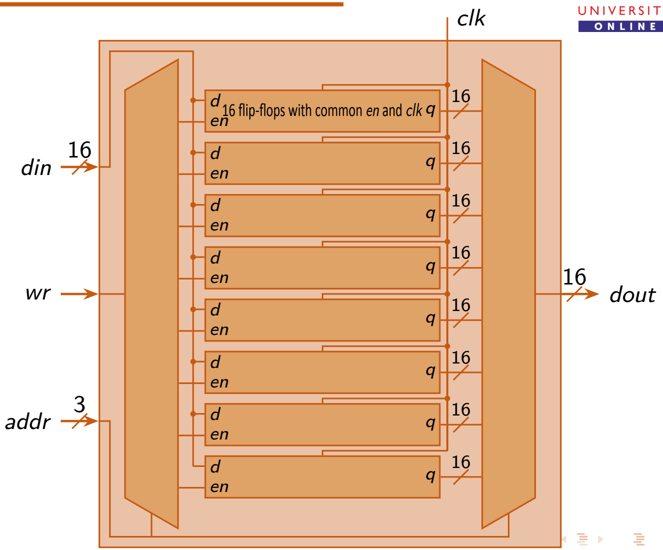

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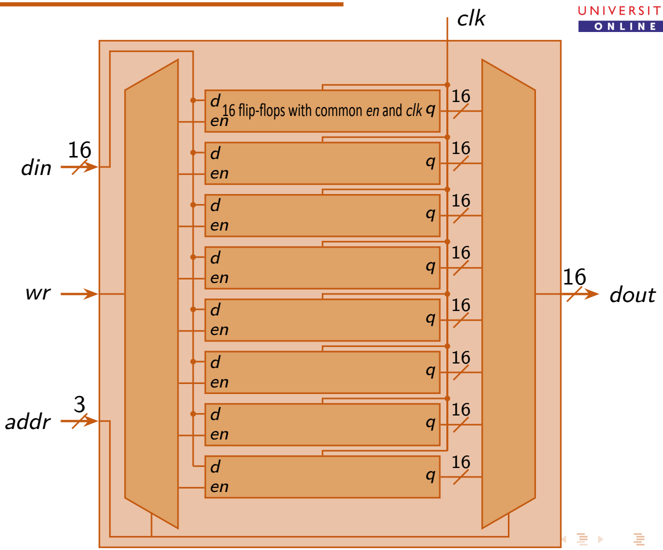

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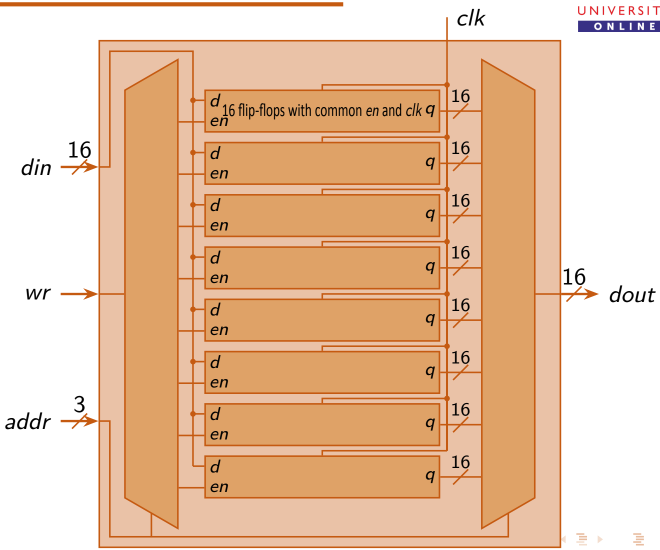
  - Each memory element is called a **bit cell**



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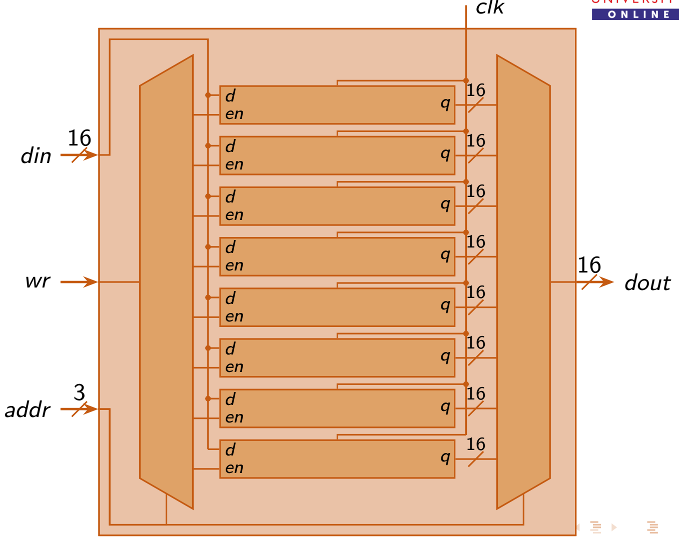
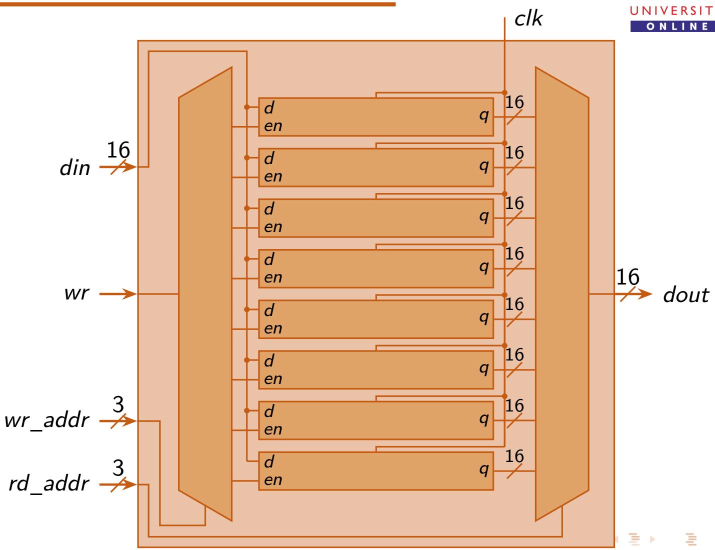
Memory Ports

- A memory **port** is a set of signals that provide read and/or write access to a memory address in the array
- One read / write port:
  - *addr*, *wr*, *din* and *dout*



Memory Arrays - 2
Memory Ports

- A memory **port** is a set of signals that provide read and/or write access to a memory address in the array
- Two ports
- One read port:
  - *rd_addr* and *dout*
- One write port:
  - *wr_addr*, *wr* and *din*



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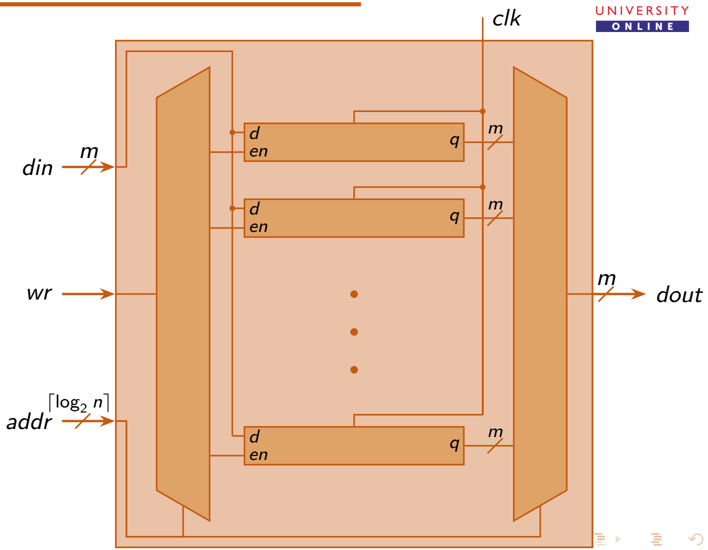
Memory Array Organization

- Structure of a memory array of n-word $\times$ m-bit is shown
- Implementation of a small register file would have similar structure
- Other larger arrays may have different internal structures
  - Such as using a decoder with wordlines and bitlines
  - Latches instead of flip-flops
- However, the internal structures of (random access) memory arrays are functionally equivalent to the shown structure



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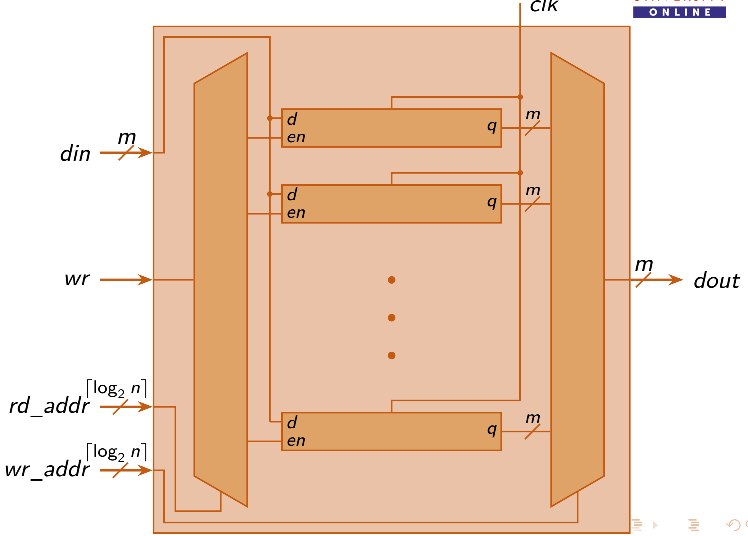

Memory Arrays - 2
Types of Memory Arrays

Memory type	Transistors per bit cell	Latency	Application
flip-flop	20	fast	Register file
SRAM[1]	6	medium	CPU cache
DRAM[2]	1	slow	Main memory

[1]Static Random Access Memory
[2]Dynamic Random Access Memory

Memory Arrays - 2

Think About It

- We have seen a memory array with one read port and one write port
- In a lab assignment, you implement a memory array with two read ports
- Can you design a memory array with two write ports?
    - What additional concerns, if any, would you need to handle?