



PES University, Bangalore
(established under Karnataka Act No. 16 of 2013)

In Semester Assessment - 1 (ISA-1) B. Tech. 3rd Semester, Oct. 2020

UE19CS201: Digital Design and Computer Organization

Time: 2 hours

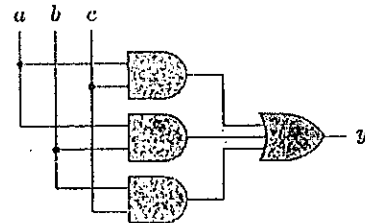
All questions to be answered

Max. marks: 60

1. (a) As we have studied in class, for Boolean functions, each input and output can only have a value of 0 or 1. What then is the total number of Boolean functions of n inputs? (2)

(b) (4)

- (i) As discussed in class, combinational logic circuits and truth tables are two ways of representing Boolean functions. We have also studied a technique for conversion of given logic circuit into corresponding truth table. Using above technique, write down the truth table for the logic circuit shown on the right.



- (ii) The truth table shown on the right is for one of the logic structures we have studied in class. Write down the SOP (Sum of Products) Boolean formula from the truth table (no need to minimize). Also write down the name of the logic structure it represents.

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

- (c) For the following Boolean function: (4)

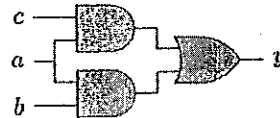
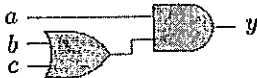
$$F(a, b, c, d) = \Sigma(0, 2, 5, 7, 8, 10, 12, 13, 14, 15)$$

draw the K-map, mark on the K-map only the required prime implicants, and write the minimized SOP formula obtained using the marked implicants.

2. (a) (4)

- (i) NAND gates, as we have studied, are universal gates using which any gate or logic circuit can be constructed. Use two input NAND gates to draw a logic circuit that is equivalent to a two input OR gate (that is, the constructed logic circuit should output a 0 only when both its inputs are 0). Use as few NAND gates as possible in your circuit diagram.
- (ii) Prove or disprove that the following two logic circuits represent the same Boolean function.

(Hint: A quick way to the answer is to use one or more of the Boolean Identities / Laws studied in class.)



- (b) Consider a ripple carry adder for adding two 16-bit numbers constructed out of 16 full adders, (no half adder used). Let the critical path delay for above ripple carry adder be 2.5 ns. Then what is the critical path delay for a ripple carry adder similarly constructed for adding two 32-bit numbers? (2)
- (c) Write down the Boolean formulas for the sum and carry outputs of a full adder. Both of above, naturally, represent Boolean functions. A *symmetric* Boolean function is a Boolean function whose value does not depend on the permutation (ordering) of its input bits, i.e., it depends only on the number of ones in the input. For example, a two input XOR gate is a symmetric Boolean function. As another example, for a four input symmetric boolean function, the output for inputs 0001, 0010, 0100 and 1000 must be the same. Which of the above two (sum and carry) Boolean functions (if any) are symmetrical Boolean functions? (4)
3. (a) In class we have studied various combinational logic structures such as muxes, decoders, encoders and adders. Some such structures studied in class have been implemented as gate level logic diagrams below. For each diagram, write the name of the logic structure and its size. For example, if there was a diagram of an mux having four inputs (and one output), the expected answer would simply be "4:1 mux". Hint: If not clear from the diagram, functionality could be inferred by writing the truth table for the logic. (4)

Diagram 1:

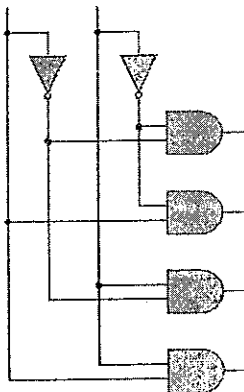
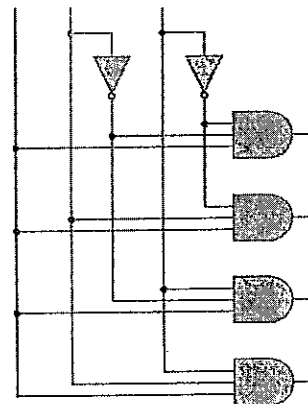


Diagram 2:



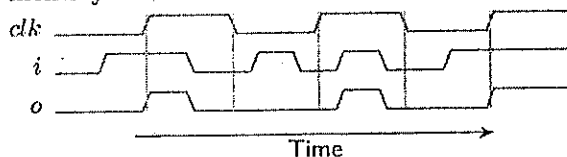
- (b) As we have studied, larger demuxes can be constructed using smaller demuxes. Draw the logic circuit diagram of a 1:5 demux constructed using 1:2 demuxes, using a minimum number of 1:2 demuxes. (2)
- (c) (4)
- (i) Draw the logic circuit diagram of a barrel shifter (composed of 2:1 muxes) with four data inputs, four data outputs (and two control inputs). (4)
- (ii) If the critical path delay of a 2:1 mux is 150 ps, then what is the critical path delay of the above barrel shifter?

4. (a) Draw the logic circuit diagram of a JK flip-flop constructed using a D flip-flop (no need to draw the internal logic circuit of the D flip-flop). (2)

(b) (4)

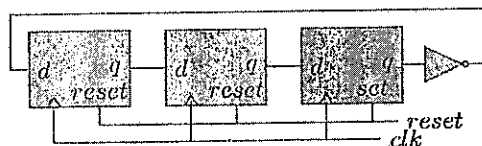
(i) Define critical path delay.

(ii) The timing waveform diagram below is for a memory element with i , o and clk signals being respectively the input, output and clock input to the memory element. Write down what type of memory element it is.



- (c) We have studied in class the FSM method for constructing sequential logic circuits from a problem specification. Consider a problem specification that specifies the number of inputs and outputs of the logic circuit to be n_i and n_o respectively (each input and output being a single bit signal). Also, the state transition diagram for the problem has 2^s states. Now consider the state transition table. If the state transition table is constructed for a Moore FSM implementation, how many rows will it have? How many rows will the state transition table have for a Mealy type implementation? Assume the transition tables have no don't cares on either input or output side. (4)

5. (a) As studied in class, the modulus of a counter is the number of states a counter sequences through before repeating (ex: modulus of a 3-bit binary counter is 8). What is the modulus of the counter shown: (3)



- (b) What is the key difference between Mealy type and Moore type Finite State Machines? (1)

- (c) A divide-by-3 counter is a sequential logic circuit that has one output and no inputs (except clock). The output is high for one clock cycle out of every 3. In other words, the output divides the frequency of the clock by 3. The output is high for the first clock cycle immediately after reset, low for the next two clock cycles, then high again for a clock cycle, and so on. Draw the state diagram, write the state encoding table, state transition table and the output table. Use Moore type FSM and binary encoding. (6)

6. (a) Consider a parallel prefix adder for adding two 16-bit numbers. Let its critical path delay be 1.8 ns. Also, a similarly constructed parallel prefix adder for adding two 32-bit numbers has a critical path delay of 1.9 ns. Then what would be the critical path delay for a similarly constructed parallel prefix adder for adding two 64-bit numbers? (3)
(Hint: Question can be answered without using the detailed critical path formulas derived in class.)

- (b) Draw the logic circuit diagram for a 4×1 (four locations each storing one bit) memory array, using D flip-flops for the bit cells. Appropriately label all the inputs and outputs. (3)
- (c) How many Boolean functions of a single input are there? Write the truth table for each. (4)