Digital Design and Computer Organization

Latches, Flip-flops - 2

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
  - Sequential logic design
    - **Latches, Flip-flops - 2**
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- D Latch
- D Flip-Flop

D Latch

- Problem with RS latch:
  - When $r = s = 1$, $q = \overline{q} = 0$
  - If above inputs change to $r = s = 0$, output is indeterminate

D Latch

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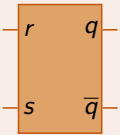
D Latch



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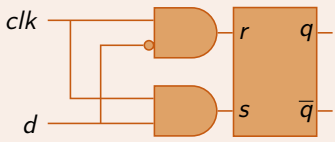

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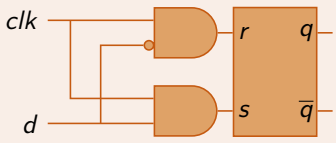

clk	d	s	r	q	$\overline{q}$

D Latch

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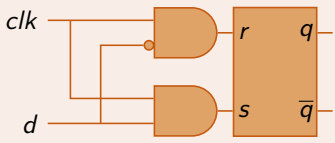

clk	d	s	r	q	$\overline{q}$
0	0				

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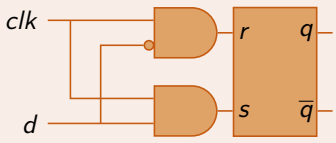

clk	d	s	r	q	$\overline{q}$
0	0	0	0		

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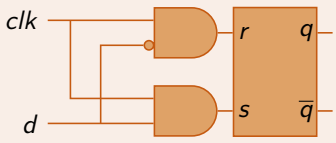

clk	d	s	r	q	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$

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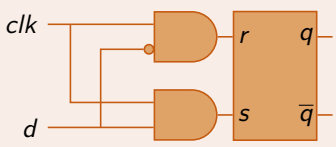

clk	*d*	*s*	*r*	*q*	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1				

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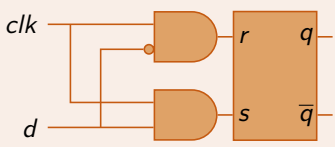

clk	d	s	r	q	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0		

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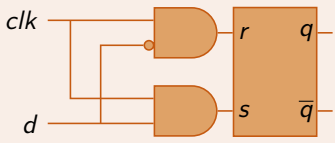

clk	d	s	r	q	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$

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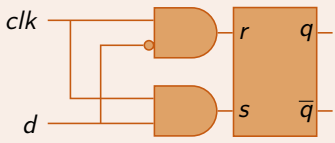

clk	*d*	*s*	*r*	*q*	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0				

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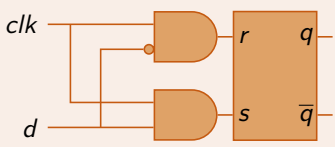

clk	*d*	*s*	*r*	*q*	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0	0	1		

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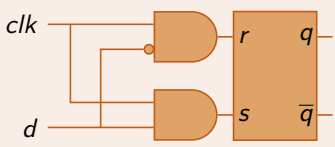

clk	*d*	*s*	*r*	*q*	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0	0	1	0	1

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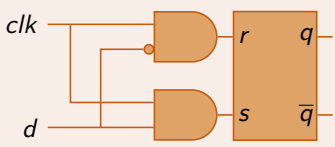

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0	0	0	0	q_{prev}	$\overline{q_{prev}}$
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1	0	0	1	0	1
1	1				

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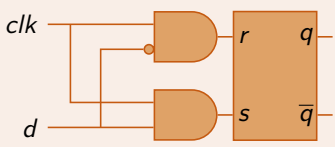

clk	*d*	*s*	*r*	*q*	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0	0	1	0	1
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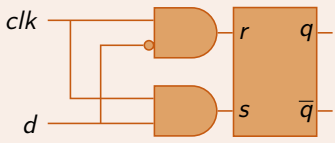

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0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0	0	1	0	1
1	1	1	0	1	0

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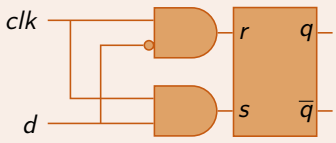
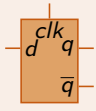


clk	*d*	*s*	*r*	*q*	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0	0	1	0	1
1	1	1	0	1	0

- Symbol:



Latches, Flip-flops - 2

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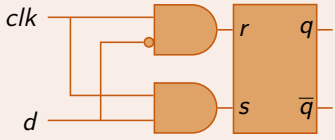
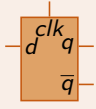


clk	d	s	r	q	$\overline{q}$
0	0	0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	0	q_{prev}	$\overline{q_{prev}}$
1	0	0	1	0	1
1	1	1	0	1	0

- Symbol:



- Eliminates $r = s = 1$ case
- Output same as input when $clk = 1$
- Called **transparent** or **level-sensitive** latch

Latches, Flip-flops - 2

D Flip-Flop

- **Latch** Level senstitive (ex: D latch)
- **Flip-flop** Edge triggered (ex: D flip-flop)

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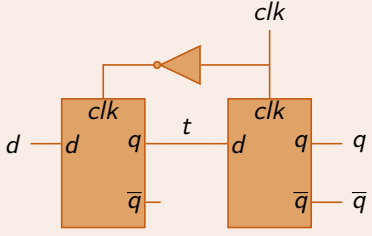

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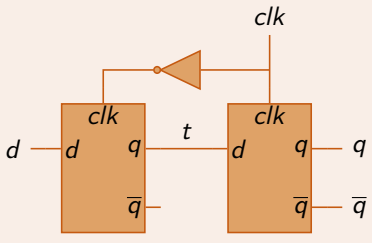

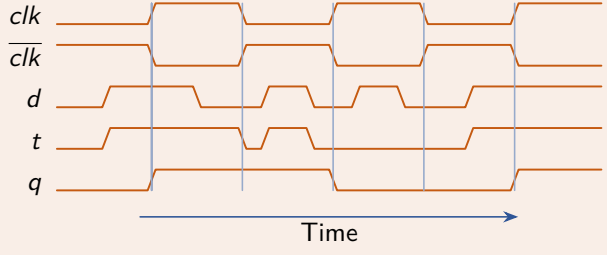

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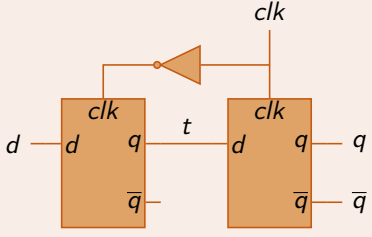

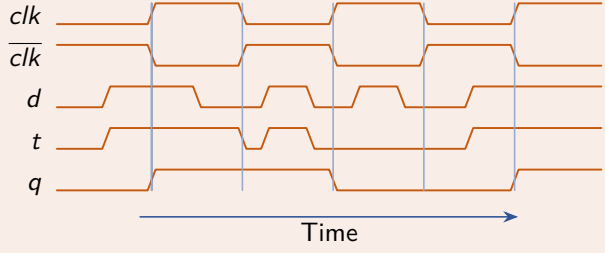

- *d* copied to *q* at rising edge of *clk*
- *q* unchanged at all other times

Latches, Flip-flops - 2

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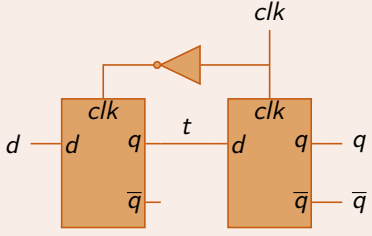

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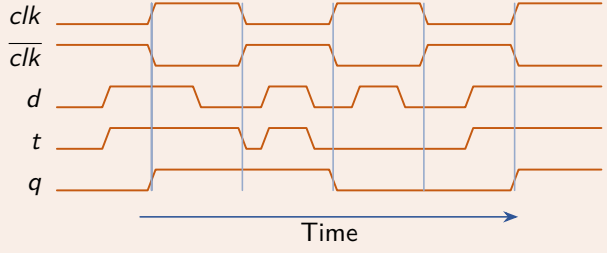


- At the rising edge of *clk*:

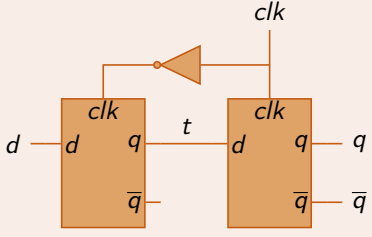
d	*q*
0	0
1	1

Latches, Flip-flops - 2

D Flip-Flop

- **Latch** Level senstitive (ex: D latch)
- **Flip-flop** Edge triggered (ex: D flip-flop)

D Flip-Flop



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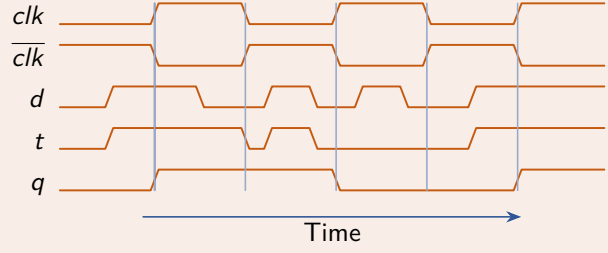
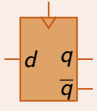


- At the rising edge of *clk*:

d	*q*
0	0
1	1

- Symbol:



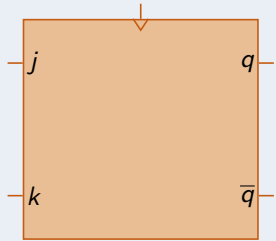
Think About It

JK Flip-Flop Example

- At the rising edge of *clk*:

j	k	q	$\overline{q}$
0	0	q_{prev}	$\overline{q_{prev}}$
0	1	0	1
1	0	1	0
1	1	$\overline{q_{prev}}$	q_{prev}

  - Output toggles when $j = k = 1$



Latches, Flip-flops - 2

Think About It

JK Flip-Flop Example

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j	k	q	$\overline{q}$
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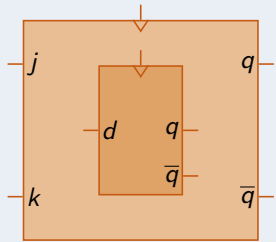
1	0	1	0
1	1	$\overline{q_{prev}}$	q_{prev}

  - Output toggles when $j = k = 1$



- Construct a *JK* flip-flop using a *D* flip-flop and some logic gates

Think About It

D Flip-Flop Chain

- What does the following logic circuit do?