PES UNIVERSITY

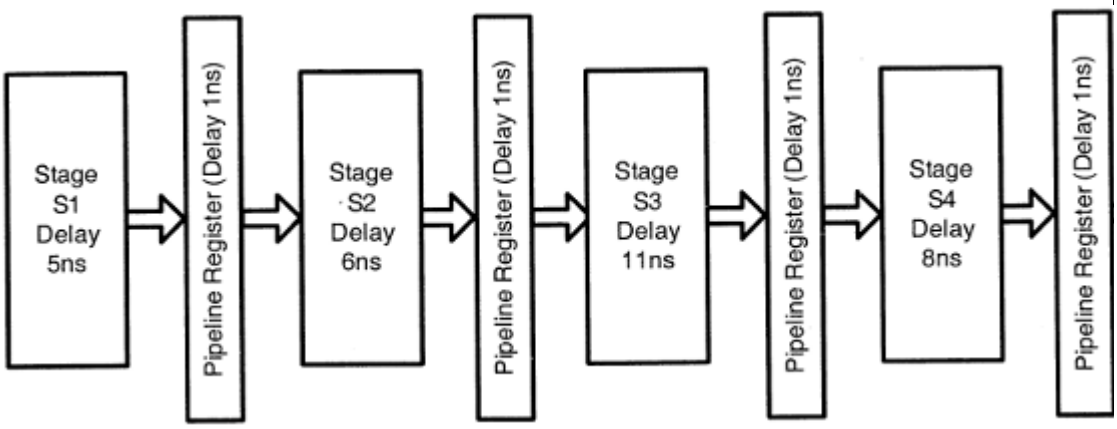
Department of Computer Science & Engineering
Microprocessor & Computer Architecture

UNIT 2 Question Bank

TOPIC: **PIPELINE**

1	Explain the implementation of the basic pipeline for MIPS with a neat diagram showing the data path.
2	Explain the different classes of pipeline hazards with examples in detail.
3	What do you mean by pipeline interlock ? How does exception make pipelining hard to implement? Discuss.
4	List pipeline hazards. How will you classify it ? Pipelining yields a reduction in the average execution time per instruction. Justify this.
5	Why is pipelining needed ? What is the goal of a pipeline designer ? Why is it difficult to implement a pipeline ?
6	With the help of neat diagram show the implementation of MIPS data path that allows every instruction to be executed in 4 or 5 clk cycles.
7	MIPS is based on a 5 stage RISC pipeline scheme. Give its implementation for all 5 clock cycles.
8	What do you mean by pipeline interlock? Explain in short basic performance issues in pipelining.
9	How RISC is implemented without pipelining? Explain the classic 5 stage pipeline for a RISC processor, with a neat diagram.
10	Draw the neat datapath of a simplified RISC architecture in a pipeline fashion & explain it.
11	What is the role of pipeline registers in RISC architecture, explain with a neat diagram.
12	What is a hazard? Discuss all the factors related to performance of pipelines with stalls.

13	Explain the stopping & restarting the execution of a pipeline instruction on an exception.
14	What steps of pipeline control are taken on an exception in order to save a pipeline state ?
15	Explain with a neat diagram all the events with associated registers on every pipe stage of the MIPS pipeline.
16	Explain implementation of a RISC Instruction set in the pipeline.
17	What is data hazard ? Explain with an example.
18	How data hazards are minimized using data forwarding in a 5 stage pipeline architecture? Explain with an Example.
19	Can data hazard be eliminated with data forwarding ? Under what situation it can not be eliminated ? Explain with an example.
20	Consider two instructions *i* and *j*, with *i* occurring before *j*. Explain the possible data hazards.
21	Explain Structural hazard with an example?(with diagrams)
22	What is control hazard ? Explain with an example?
23	When a branch instruction occurs in a pipeline in the form of an exception (interrupt), what additional hardware is required to overcome the hazard. Which architecture supports the same. What is done to the 5 stage pipeline to reduce two stall cycles?
24	What is delayed branch in pipeline?
25	What is delay slot in pipelining?
26	What is ment by branch prediction?
27	What are the different techniques for branch prediction? explain
28	What is static branch prediction?
29	What is dynamic branch prediction?
30	Consider the following RISC assembly code. load r1,45(r2) (1) add r7 <- r1, r5 (2) sub r8 <- r1, r6 (3) or r9 <- r5, r1 (4)

	brneq r7, target (5) add r10 <- r8, r5 (6) xor r2 <- r3, r4 (7) Identify each dependence; list the two instructions involved; identify which instruction is dependent; and, if there is one, name the storage location involved (register or memory).
31	What is branch branch penalty?
32	How the branch delay slot will occur?
33	Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipelined delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is _____.
34	Consider a 6-stage instruction pipeline, where all stages are perfectly balanced.Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is _____.
35	Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage.Delays for the stages and for the pipeline registers are as given in the figure.  What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation'?

36	Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate- 1. Pipeline cycle time 2. Non-pipeline execution time 3. Speed up ratio 4. Pipeline time for 1000 tasks 5. Sequential time for 1000 tasks 6. Throughput