UNIT-2

Pipelining

1	What is the role of pipeline registers in RISC architecture, explain with a neat diagram.
2	What is a hazard? Discuss all the factors related to performance of pipelines with stalls.
3	Explain the stopping & restarting the execution of a pipeline instruction on an exception.
4	What steps of pipeline control are taken on an exception in order to save a pipeline state ?
5	Explain with a neat diagram all the events with associated registers on every pipe stage of the MIPS pipeline.
6	Explain implementation of a RISC Instruction set in the pipeline.
7	What is data hazard ? Explain with an example.
8	How data hazards are minimized using data forwarding in a 5 stage pipeline architecture? Explain with an Example.
9	Can data hazard be eliminated with data forwarding ? Under what situation it can not be eliminated ? Explain with an example.
10	Consider two instructions *i* and *j*, with *i* occurring before *j*. Explain the possible data hazards.