Digital Design and Computer Organization

Logic Minimization, K-Maps - 1

Reetinder Sidhu

Department of Computer Science and Engineering

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Course Outline

- Digital Design
  - Combinational logic design
    - **Logic Minimization, K-Maps - 1**
  - Sequential logic design
- Computer Organization
  - Architecture (microprocessor instruction set)
  - Microarchitecure (microprocessor operation)

Concepts covered

- Boolean Formula Terminology
- Sum of Products and Product of Sums standard forms
- Truth Table to Boolean Formula / Logic Circuit
- Logic Minimization using Boolean Identities

From Truth Table to Boolean Formula and its Minimization

- Given a combinational logic circuit or Boolean formula, we have learnt to construct its truth table
- But, given a truth table, how to construct a Boolean formula (or combinational logic circuit) for it?
- Also, as there are multiple Boolean formulas / logic circuits for each truth table, how to pick the minimal one?
- Above problem is called **logic minimization**
  - many metrics: smallest, fastest, least power cosumption
  - our metric: smallest two level Sum of Products formula
  - may be more than one solution

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Sum of all minterms corresponding to a 1 output

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Logic Minimization

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Logic Minimization

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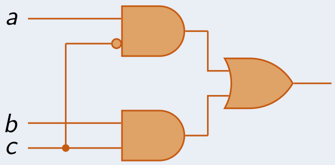
The three representations below are different ways of specifying **the same Boolean function:**

$$a \cdot \overline{c} + b \cdot c$$



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  - Hint:
    $y = (a(a + b + \bar{c}) + b(a + b + \bar{c}) + c(a + b + \bar{c}))(a(\bar{a} + b + \bar{c}) + \bar{b}(\bar{a} + b + \bar{c}) + c(\bar{a} + b + \bar{c}))$