

# **Super CDMS**

## **Detector Control and Readout Card**

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### **Assembly Specification**

**Design Rev. F.**

Updated: 2021-07-01

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U.S. DEPARTMENT OF  
**ENERGY**

Office of  
Science

## Contact Information

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## Documentation Location

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<https://supercdms-docdb.fnal.gov/cgi-bin/sso/ShowDocument?docid=4394>

username = review  
password = snowlab2015

## General Information

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The DCRC stands for "Detector Control and Readout Card". The current revision of this design is F. The board is a mixed signal design incorporating fairly high-speed digital backend electronics and sensitive low noise analog front-end electronic components.

## PCB Information

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The DCRC measures 11.0" x 6.0" x 0.093" FR4, 6-layer printed circuit board with approximately 1885 components of which 250 are unique. Most of the components on the board are surface mount consisting BGA (Cyclone 4 484 BGA), SOT23, MSOP, TSSOP, SQFP, with 20, 25 mils and 50 mil pitch packages. There are 0402 and 0603 discrete components and some thru-hole components. The PCB is not impedance controlled. Surface is SMOBC with ENIG plating. All PCBs will be 100% Netlist tested by the PCB vendor. Each PCB will be 1UP and have 0.500" process rails along the long edges.

## Quantity and Delivery Schedule

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42 assemblies total.

2 assemblies for first piece approval will be assembled in two weeks.

First piece inspection approval to be 1 week or less, then the approval will be given for the remainder.

After approval one unit will be returned to be used as the "golden sample" for the remainder of the build.

The remaining 40 assemblies after the first piece approval will be delivered after 4 weeks.

## Parts

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The BOM (Excel Spreadsheet) will contain all known components to be assembled including those to be supplied by Fermilab. Fermilab to supply PCBs and some parts as indicated in the BOM. The vendor will supply all remaining parts, subject to Fermilab approval.

### **Additions, Deletions, and Substitutions initiated by Fermilab before Parts Approval**

Additions, deletions, and substitutions to the parts list can occur for each assembly phase will be handled as follows: 1) Fermilab must approve all parts changes; 2) additional parts will be assigned a new Fermilab assigned number (F/N).

### **Additions, Deletions, and Substitutions initiated by Fermilab after Parts Approval**

Additions, deletions, and substitutions to the parts list can occur for each assembly phase and will be handled as follows: 1) vendor will notify Fermilab of parts shortages and Fermilab will procure them; 2) additional parts will be assigned a new Fermilab assigned number (F/N).

There are Do Not Install components (DNI). See BOM and pick-n-place file for details.

Please review the assembly drawings for other pertinent information.

## Applicable Standards

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Assembly must be ROHS compliant.

Vendor is required to fully conform to ANSI/IPC-A-610. Class 2.

## Serial Numbers

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All boards shall be serialized, and these serial numbers referenced by inspection documentation.

## Board Warpage

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Bare board warpage is specified at less than 0.005 inches per linear inch. Board warpage after assembly must be less than 0.010 inches per linear inch.

## Assembled Board Inspection and Rework

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Vendor is required to provide documentation of a thorough visual inspection using AOI. Vendor is required to provide documentation of X-Ray inspection of the BGA to insure proper solder reflow. BGA X-Ray images must reference the board serial number. Any misplaced, rotated, or parts with the wrong values should be identified and repaired by whatever inspection means used as a complementary inspection by vendor.

## Cleaning and Packaging

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Final assembled product must be free of any flux/chemicals. "no clean" flux shall not be used. We prefer a deionized water cleaning no matter which solder/flux is used. Vendor shall remove the process rails from the long edges of the PCB. Finished Boards to be packaged in ESD bags with appropriate protection to avoid shipping damage.

## Fabrication Files

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DCRC\_RevF\_Gerbers.zip contains:

### Gerber Files, 274X

Layer 1 = \*.TOP

Layer 2 = \*.IN1

Layer 3 = \*.GND (plane)

Layer 4 = \*.PWR (plane)

Layer 5 = \*.IN2

Layer 6 = \*.BOT

Solder Mask Top = \*.SMT

Solder Mask Bottom = \*.SMB

Silkscreen Top = \*.SST

Silkscreen Bottom = \*.SSB

Drill File = \*.DRD

Assembly Top Drawing = \*.ASB

Assembly Bottom Drawing = \*.ASB

Solder Paste Top = \*.SPT

Solder Paste Bottom = \*.SPB

### Other Files

Gerbtool Project File = \*.GTD

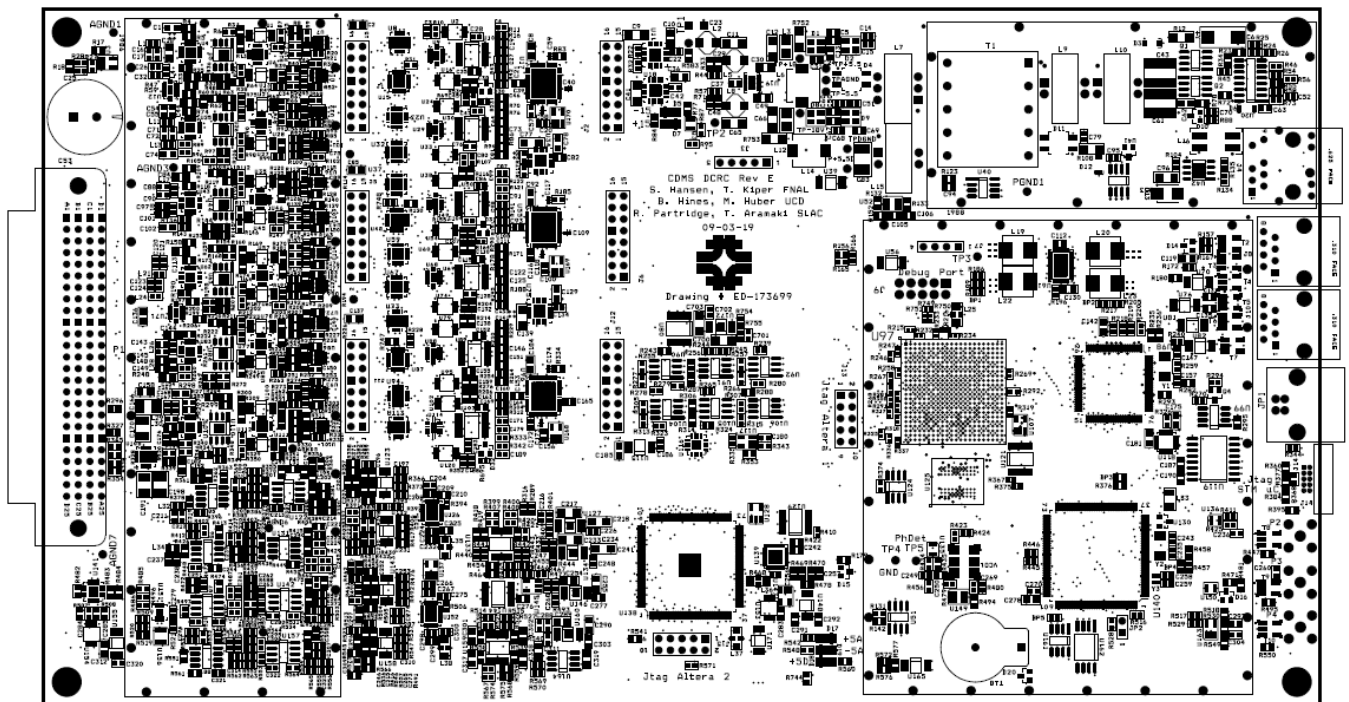
NC File = thruhole.tap

Pick and Place File = INSERT.TXT

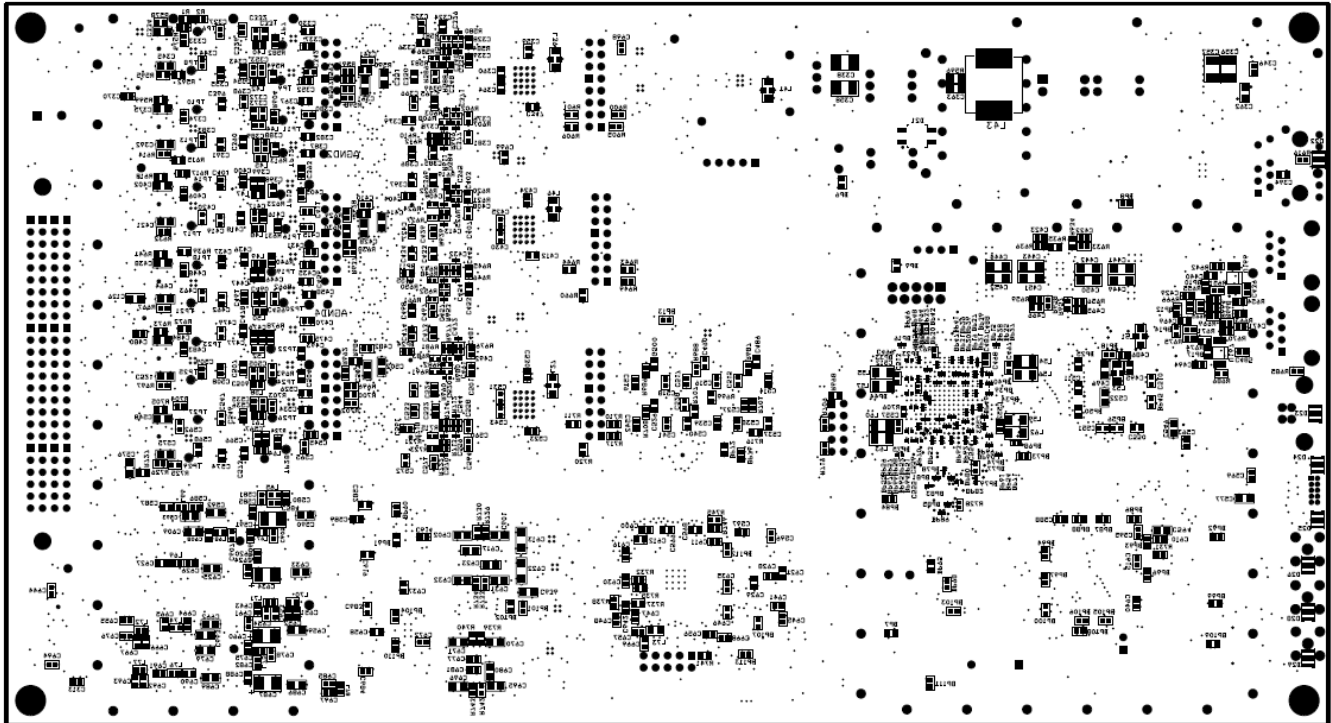
## Top and Bottom PCB Drawings

The following images are provided for reference only. Refer to the Gerber files for accurate high resolution drawings.

DCRC Top Solder Mask-Silkscreen



## DCRC Bottom Solder Mask-Silkscreen



## Assembly Drawings

The following images are provided for reference only. Refer to the Gerber files for accurate high resolution drawings.

Assembly Top Drawing

