2022-02-10 Electronics Review

Thursday, February 10, 2022 11:59

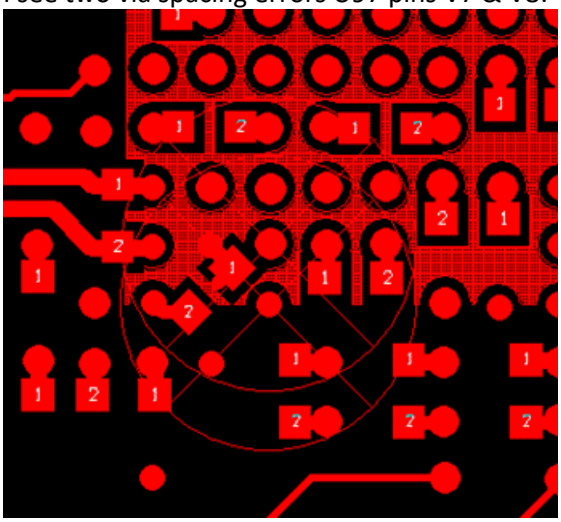
PCB review DCRC Rev G

External Reviewers: Greg Deuerling and Neal Wilcer (sent their comments via email, not on the call)

Neal didn't find any major issues looking at Gerbers.

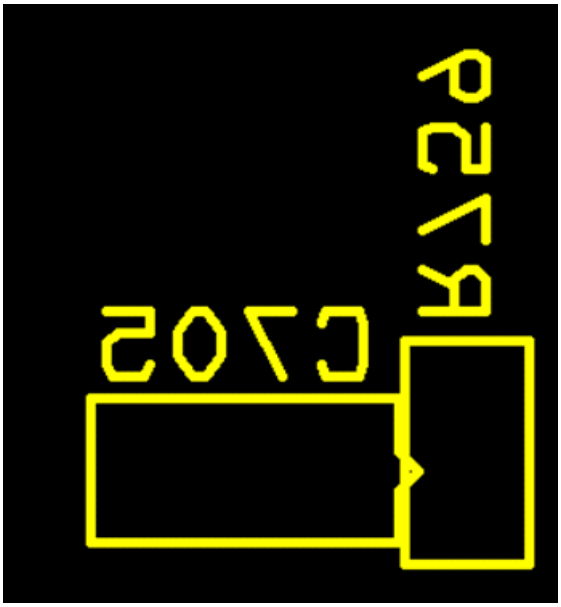
Greg Looked at ORCAD MAX file. His comments:

I see two via spacing errors U97 pins V7 & V8:



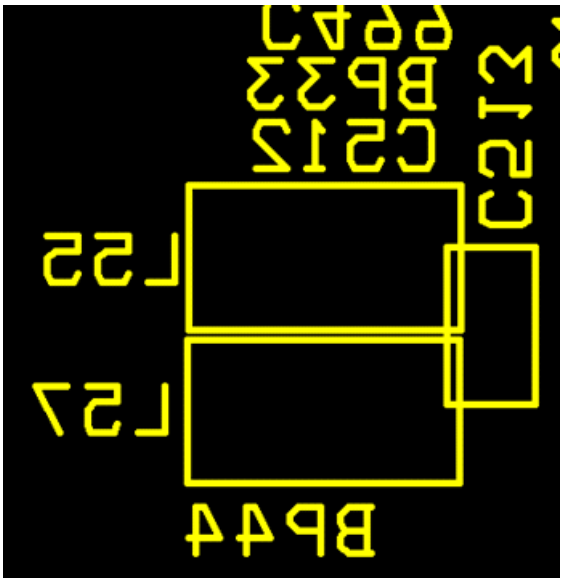
Checked -- this is OK, just some strangeness in how OrCAD calculates clearances on non-90 degree components. Clearances OK here.

The two added components R759 & C707 silkscreens are overlapping a bit:

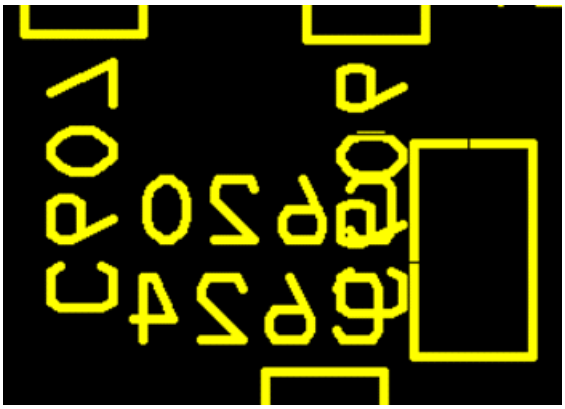


Shouldn’t be an issue, but it may pop up at the PCB house as an error.

Same here:



Just happed to see the silkscreen text below is on top of each other:



Discussion: These silkscreen issues are minor/cosmetic. OK to leave as is.

General Comments and Resolutions

Schematic dates, titleblock, Rev number, Drawing number OK

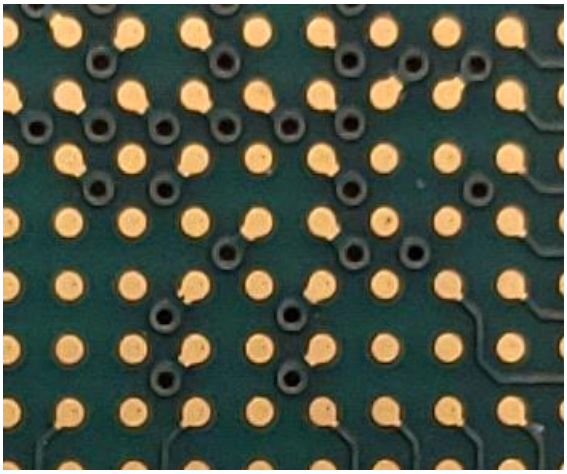
PCB silkscreen top with proper name, REV, names, Date, Drawing number OK

Fiducials added to assist pick-and-place. OK

All thru holes had thermals, this is OK.

Tent vias top and bottom -- confirmed, yes vias are covered by soldermask top and bottom DONE

This is correct, with the "dogbones" under the BGA looking like this. Vias covered by soldermask.



U108 filter the input to this chip, R and C on bottom layer. SLAC asked for this. Done.

Move power connector so it is outside of shield. Terry suggested. Done.

Move RJ45 for better clearance between metal jack component and metal shield. Done.
(this to fix the problem when the ethernet shielded cables were providing power betweeen boards. This was also fixed by switching to unshielded CAT5/6 ethernet cables).

Checked internal pours from board edge. Looks good.

Some footprints were changed from SSOP to DFN, but then changed back when parts were found.

We have:

TPS7A3001DGNR U127, U146, U172 SSOP8
TPS7A4901DGNR U134 U160 SSOP8

We confirm these footprints are OK on the PCB.
Johnny confirms these part numbers in BOM and with orders. OK

LEDs appear to all face same way on bottom layer. ALL LEDs should point towards the board EDGE. OK.

(Note: when boards go out for assembly make a drawing for the vendor to confirm proper LED orientation)

We confirm CPLD wire mods are correct.

Plating is ENIG (Electroless NIckel Gold). Johnny says typical shelf life is 2 years for this finish. Should be OK for this.

Recommend asking PCB fab house for plating coupons.

<u>WE ARE GO for 50 boards</u>. Johnny to quote 5 and 15 day delivery.

***** TO DO: TERRY print 1:1 and check the shield holes and traces**

***** TO DO: JAMIESON put THIS FILE in DocDB**

***** TO DO: JAMIESON place OrCAD *.DSN file (the project file and schematic sources) in DocDB**

***** TO DO: JAMIESON put Johnny's PCB bid package document / README file in DocDB when it's ready**