Nanvix

A Distributed Operating System for Lightweight Manycores

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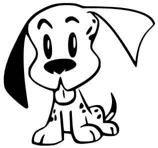

Introduction

Lightweight (LW) Manycores: Performance Scalability and Energy Efficiency

- Hundreds of Low-Power Cores
  - MIMD workloads
  - Massive thread-level parallelism
  - Low-power consumption
- Distributed Memory Architecture
  - Grants performance scalability
  - Delivers predictability
- On-Chip Heterogeneity
  - Adaptability to computing demands
  - Enables high-energy efficiency
- Rich On-Chip Interconnects
  - Enable QoS
  - Expose asynchronous communications

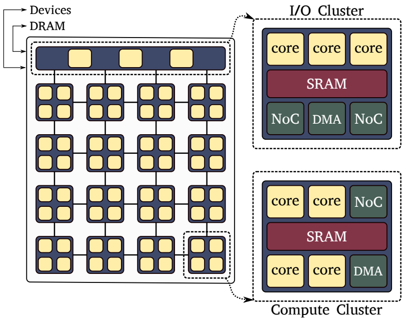

Figure: A 67-core lightweight manycore.

It Is A Distributed Architecture in a Single Chip!

Introduction

Lightweight (LW) Manycores: Programmability Challenges

- High Density Circuit Integration
  - Heat dissipation
  - Dark silicon
- Distributed Memory Architecture
  - Data tiling (small local memories)
  - Message passing communication
- On-Chip Heterogeneity
  - Thread scheduling
  - Data placement
- Rich On-Chip Interconnects
  - Network congestion
  - Security checking

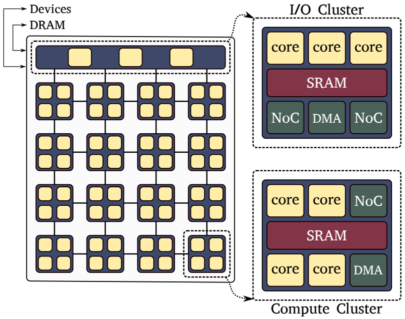

Figure: A 67-core lightweight manycore.

Performance vs Programmability vs Portability

Introduction

Centralized vs Distributed Operating Systems

- Centralized Operating Systems
  - One Full-weight OS is deployed in each cluster
  - User library exposes message-passing API
  - Distributed applications run on the OS

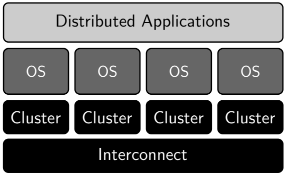

Figure: Centralized OS architecture.

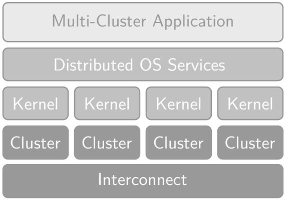

Figure: Distributed OS architecture.

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Centralized vs Distributed Operating Systems

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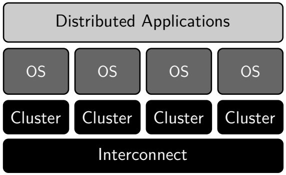
  - One kernel runs in each cluster
  - Subsystems are distributed across the kernels
  - Multi-cluster applications run on the OS



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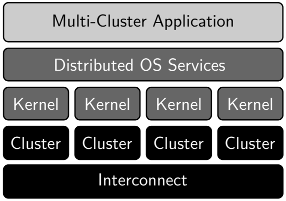

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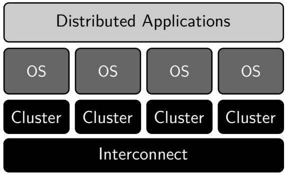
- What is the difference?
  - Scalability
  - Adaptability
  - Composability
  - Transparency
  - Fault tolerance



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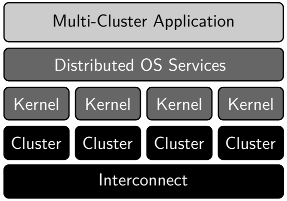

Figure: Distributed OS architecture.

Presentation Outline

1 Introduction
- LW Manycores
- Distributed OSes

2 Nanvix
- Project Overview
- System Architecture
- Multikernel
- Microkernel
- HAL

3 Perspectives
- Roadmap
- Research Ideas

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The Nanvix Operating System
Project Overview

- Re-Engineered Version of Nanvix to LW Manycores
  - Home-grown research OS
  - 4 Professors (Brazil and France)
  - 1 PhD, 2 MSc and 4 BSc Students
  - +10 past contributors
  - UGA, PUC Minas, UFSC and Grenoble INP
- Project Guidelines
  - Be Open: invite others to collaborate
  - Be Permissive: enable free adaptability
- Design Principles
  - Be Portable: run on multiple architectures
  - Be Scalable: embrace distributed configuration
  - Be Flexible: expose multiple APIs

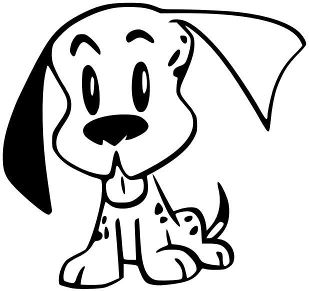
Figure: Bingo, our mascot.

https://github.com/nanvix

The Nanvix Operating System
Internals – System Architecture

- **Architectural Model**
  - Cores are grouped into clusters
  - Each cluster has its own physical address space
  - Shared memory is used for intra-cluster communication
  - Inter-cluster communication is achieved through the NoC
- **Multikernel with Three-Layers**
  - Kernels 🟦
    - Run (self-consciously) on each cluster
    - Provide minimum abstractions
    - Ensure policies and security
  - System Servers 🟥
    - Run on top of kernels at user-level
    - Provide traditional abstractions
    - Collaboratively implement subsystems
  - Runtime Libraries
    - Run alongside with user-applications
    - Interface with system servers
    - Expose standard APIs (i.e., POSIX)

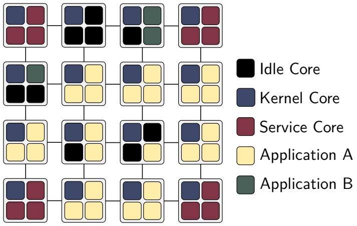

Figure: The multikernel OS structure.

The Nanvix Operating System

Internals – Multikernel

- Processor Management Fleet
  - Spawn Server
  - Name Server
- File System Management Fleet
  - VFS Server
  - Disk Driver
- Memory Management Fleet
  - Remote Memory (RMem) Server
  - Shared Memory (SHM) Server

https://github.com/nanvix/multikernel

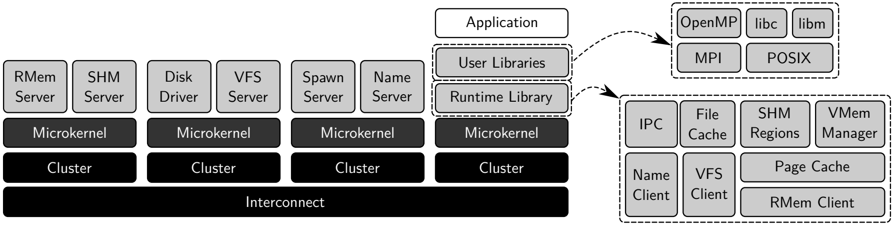

Figure: An overview of the Nanvix multikernel.

The Nanvix Operating System

Internals – Microkernel

- Microkernel Design
  - Asymmetric: runs on a dedicated core of a cluster
  - Small: provides only essential abstractions (about 5k LoC)
  - Portable: supports Bostan, RISC-V, OpenRISC and x86 based manycores
- IKC Facility
  - Inter-cluster synchronization
  - Inter-cluster communication
- Thread Management System
  - Non-interruptible kernel threads
  - Sleep/wakeup primitives
  - Exception handling forwarding
- Memory Management System
  - Single address space
  - Two-level paging scheme

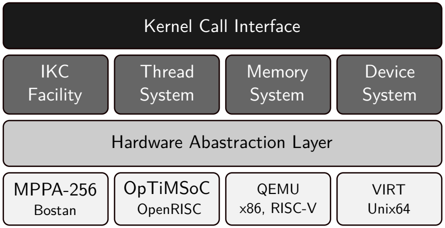

Figure: An overview of the Nanvix kernel.

https://github.com/nanvix/microkernel

The Nanvix Operating System
Internals – HAL

- Provide a standard interface across multiple platforms
- Enable portability of Nanvix
- Core Abstraction Layer
  - Core setup and shutdown
  - Interrupt and exception hooking
  - Trap forwarding
  - Memory cache manipulation
  - MMU and TLB management
- Cluster Abstraction Layer
  - Remote core start and stop
  - Events (inter-core interrupts)
  - Virtual memory
  - DMA driver
- Processor Abstraction Layer
  - Uniform cluster numbering
  - Inter-cluster communication

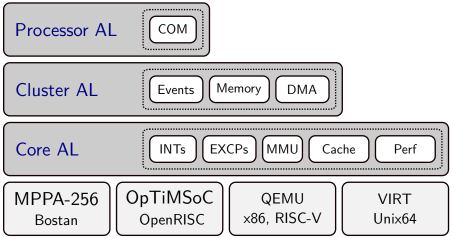

Figure: An overview of the Nanvix HAL.

https://github.com/nanvix/hal

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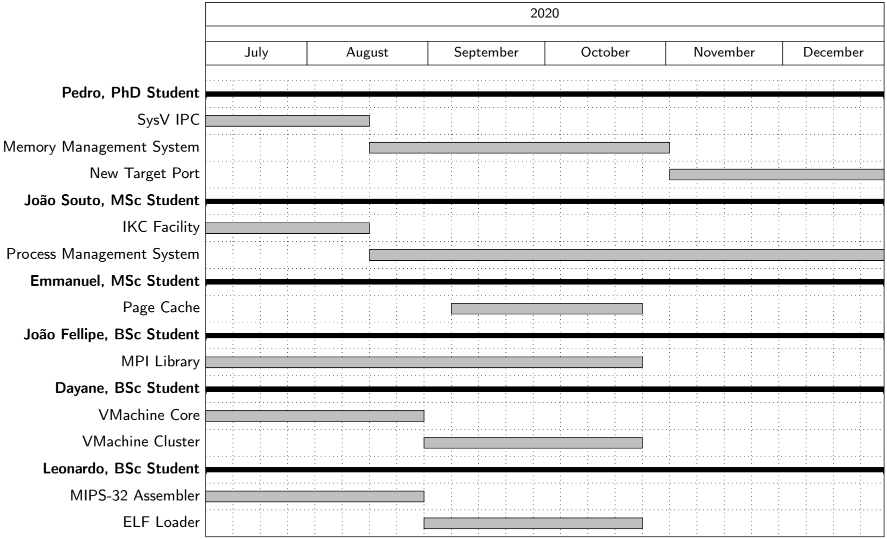
Perspectives

Roadmap



Perspectives
Research Ideas

- User-Level Thread Library
  - Enable support for core multiplexing
- Lightweight Containers
  - Enable dynamic process scheduling & migration
- x86 Multicore Support
  - Introduce multicore support to our vintage target
- Nanvix + Ariane
  - Deploy RISC-V Port of Nanvix on a baremetal platform
- Nanvix + Bluedragon
  - Deploy Nanvix in multi-cluster OpTiMSoC (FPGA) configuration

Thank You!

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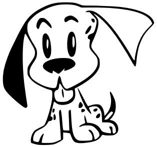

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