BM II

ROS MODULE USED ON PALM

JUNE AVAIL 1971

4/72
4 modules programmed from list?

1024 BIPOLAR READ ONLY MEMORY IM5603

FEATURES

- Programmable—No additional masks
- High Speed: Access time—40 nsec.
- High Fan-out—20 mA
- DTL/T^2L Compatible—Inputs one T^2L load
- OR-Tie capability—open collector outputs
- Simple Memory Expansion—chip enable Input
- Standard Packaging—16 pin dual-in-line/flat pack

GENERAL DESCRIPTION

The Intersil IM5603 integrated circuit is a high speed, electrically programmable, fully decoded T^2L Bipolar 1024-bit read only memory, organized as 256 words by 4 bits. On chip address decoding, along with chip enable, and uncommitted collector outputs provide for simplified memory expansion. The memory is fabricated with all logic level zeros (low); logic level ones (high) can be electrically programmed in the selected bit locations through proper addressing. The same address inputs are used for both programming and reading. This memory is compatible with other DTL and T^2L circuits.

APPLICATIONS

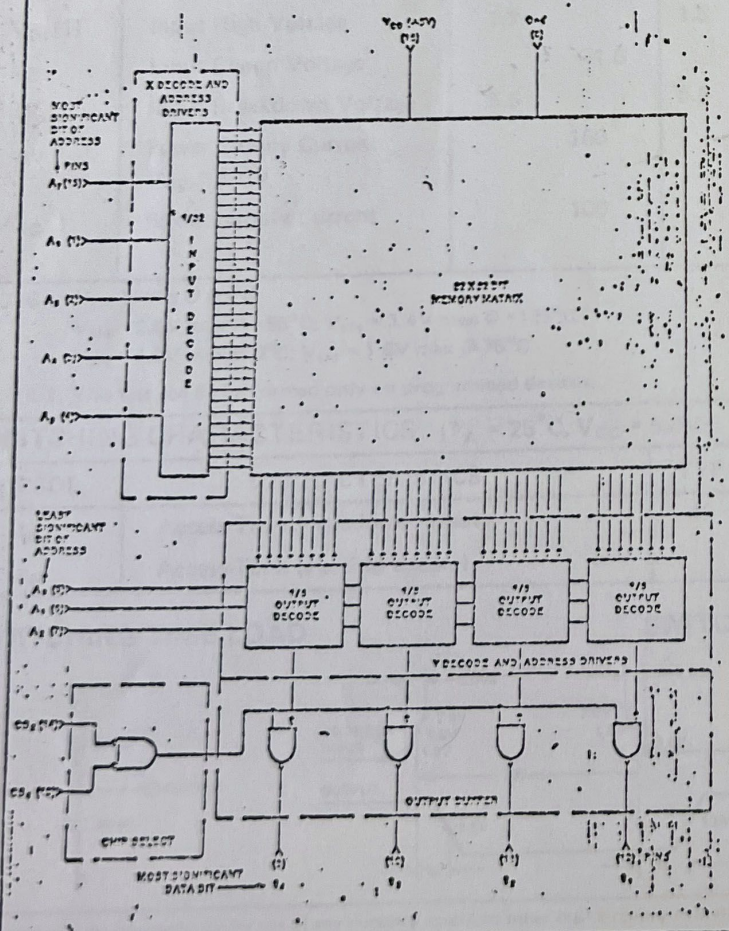
- Code Conversion
- Microprogramming
- Logic Implementation
- Arithmetic Functions

OPERATION

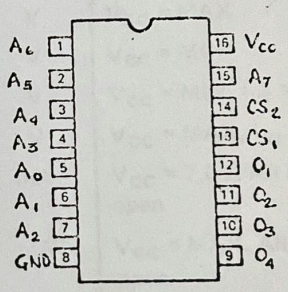
Ones can be programmed into the memory by selecting the desired word, using the five address inputs and applying a high current pulse to the output for the desired bit. The chip enable input must be high when the programming pulse is applied. After the program pulse is removed, the bit is checked. If it is still a zero, another program pulse is applied. If it is a one, the programming of that bit is complete. The programming can be easily automated for volume production. Complete programming information is contained in the "Intersil Electrically Programmable ROM Manual" available on request.

To read the memory the enable input is held low. The outputs then correspond to the data programmed in the selected word. With the enable input high, all outputs are floating.

LOGIC DIAGRAM

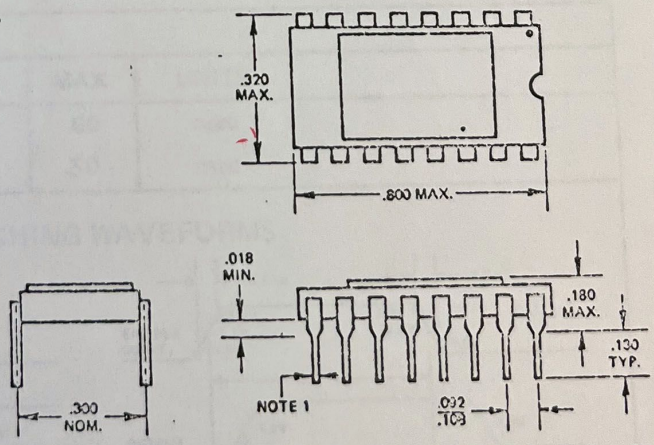


CONNECTION DIAGRAM



Pin 1 is designated either by a dot or a notch.

PACKAGE OUTLINE



NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Current into Output (Programming Only)	250mA
Input Voltage Applied	−1.5V to +5.5V	Operating Temperature	−55°C to +125°C 0°C to +75°C
Output Voltage Applied	−0.5V to +V_{CC}		
Output Voltage Applied (Programming Only)	40V	Storage Temperature	−65°C to +150°C

DC CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%), (T_A = 0°C to +75°C, V_{CC} = 5.0V ± 5%)

SYMBOL	CHARACTERISTICS	Limits −55°C to +125°C MIN	Limits −55°C to +125°C MAX	Limits 0°C to +75°C MIN	Limits 0°C to +75°C MAX	UNITS	CONDITIONS
I_{FA}	Address-Input Load Current		-1.00		-1.00	mA	V_{CC} = MAX, V_A = 0V
I_{FE}	Chip Enable-Input Load Current		-1.00		-1.00	mA	V_{CC} = MAX, V_E = 0
I_{RA}	Address-Input Leakage Current		100		60	μA	V_{CC} = MAX, V_A = 4.5V
I_{RE}	Chip Enable-Input Leakage Current		100		60	μA	V_{CC} = MAX, V_E = 4.5V
I_{OLK}	Output Leakage Current		100		100	μA	V_{CC} = V_O = MAX V_{CC}, VE = 2.0V
I_{OLK}	Output Leakage Current		100		100	μA	V_{CC} = V_O = MAX V_{CC}, V_E = 0 Word containing a "1" bit is selected. See Note 2.
V_{OL}	Output Low Voltage		0.4		0.45	V	V_{CC} = MIN, I_{OL} = 20 mA, VE = 0. Word containing a "0" bit is selected.
V_{IL}	Input Low Voltage		.85		.85	V	V_{CC} = MAX
V_{IH} (1)	Input High Voltage	1.7		1.8		V	V_{CC} = MIN
V_C	Input Clamp Voltage		−1.5		−1.5	V	V_{CC} = MIN, I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5		5.5		V	V_{CC} = MAX, I_{IN} = 1.0 mA
I_{BV}	Power Supply Current V_{CC} = 7.0V		160		160	mA	V_{CC} = 7.0V. All inputs open
I_{CC}	Power Supply Current		100		125	mA	V_{CC} = MAX. All inputs open

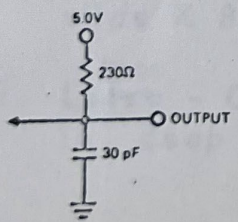
NOTE 1: V_{IH} Limits @ 25°C
V_{IH} = 2.0V max @ −55°C; V_{IH} = 1.4V max @ +125°C
V_{IH} = 1.9V max @ 0°C; V_{IH} = 1.6V max @ 75°C

NOTE 2: This test can be performed only on programmed devices.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS
t_A	Access Time (via address inputs)	40	60	nsec
t_A	Access Time (via chip enable)		30	nsec

SWITCHING TIME LOAD



SWITCHING WAVEFORMS