

2/2/73.

Cool to Bill Firth

FSU / palm compatibility

FSU spec - access 450. cycle times

X y select: CSX 6x66.2

CSY 4x66.2

FSU = 1 module select line

FSU storage card 2x18 (4)

(1 module = 1Kx9)

1 card = 4x9 (size 2w 3h1)

Includes 2 dutch modules for interfacing

Dutch modules not received yet - Expect to get modules from fishkill sometime.

Storage card they have designed will only go to 32K - capacity, loading, etc -

Would have to go to 16x9 on large card for practical application.

FSU modules - Fishkill -

Chet Engleby

532-8314

suggest 4 wide 6 hi. 16x9

16 storage modules + VTL.
must consider worse case timing.
(Module select line very critical)

S/I Tape - attachment - George Heel worth
capacity
organization

Programmer Don Williams - has 1130 assembler; writes tapes on some.

Pat Raymond for ALD's.

AA, AB, TP.

2/1/73

Noelco Model 150 - Out of Production
Noelco Tape recorder 550 0746 ?

RPQ

Case	5500749
safety label	5500748
cable	2703633 ✓
Read R/W	5131568 ✓

Recorder \approx \$50 -

logic page FT100 - 200

Users guide 2700392 ✓

Power requirement from host system
+5 to 8V 150mA max -

Gordon Thornton, FE Tech Ops - 4014
~~George Hellwath~~

2/22/73

Noelco 1420 - Uses European connector -
Sony recorder has different connector -

Input from Thornton - Have encountered
difficulty after a few months -
S/3 - alternate device -

Justified 1 year throwaway

Ral. TDAT 1200 Terminal diag. analysis -

Dick Loring - FE 8-442-5359

Have done life listing - Use for error trap -

Write scheme redone - Read amp. modified. - George Hellwath
Head azimuth big problem.

RPQ low power for S/3 cassette wk. ~~55008~~ 365008 - (\$275
one time charge)

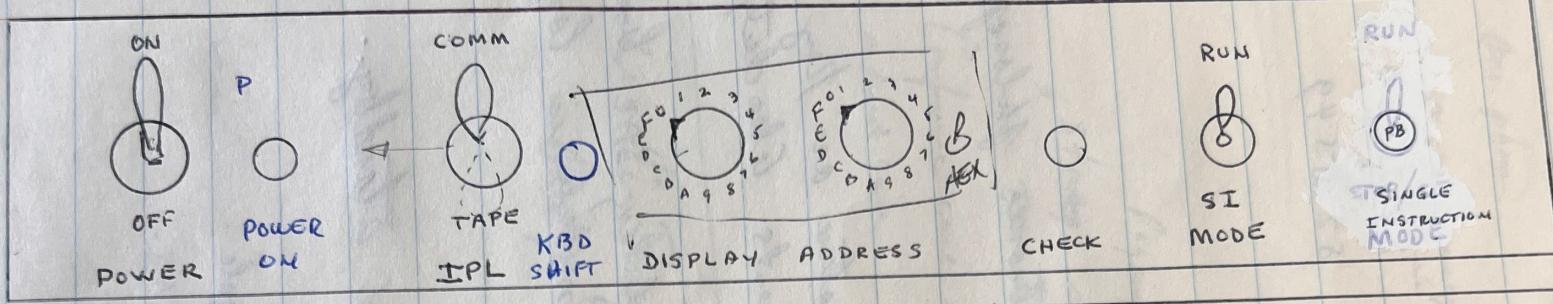
Tape S/3 - IPT

2/6/73 -

Group lites for m80 ease -

2/1/73
Jdg

1/2 scale



UPPER SHIFT CHECK TX ? ? ?
O O O O O O O

2/5/13

Pinto - display - ROS + logic - 1 chip - CD.
Thor

Al McBride

in House Expertise ~~∅~~ - also assessment.

1971 level - need update -

Computer time - big question -

Jack Bagley - planner -

Would like to add hand scanner to SCAMP I.

2/5/13 - JG

J. D. GEORGE

FEB 05 1973

Need some method to reduce amount
of RAM for SCAMP I - Ed Suggests we explore
possibility of restructuring 1130 APL program to
make all unmodified instructions in ROS -

Pat Smith 8-624-3252

(Sue Lucy)

360 PALM assembler, Rel.

1130 .. "

" PALM emulator

Ron Helmick - Knows APL / PALM

442-5352

FEB 06 1973

Source of SCAMP I parts & Post-

- progressive searchers to make use of PALMs.
1. PALM / new engine - (need shift instruction).
 2. Power Supply - L.G.
 3. Storage Reisling - Germany (interface)
 4. Celico Raleigh - attachment - Consider new design or use present Bahia modules -
 5. Bahia Boca - attachment - Use my design - ditchen 7/13
 6. Cassette - 345/3-7 attachment - ?
 7. Acoustic Coupler attachment ?
 8. TV (RF) (monitor)
 9. Hand scanner ?
 10. Console requirements .
 11. Packaging philosophy - Integrated units.
 12. Programming - System, diagnostic, application -
 13. Need 1130 or SY 7 for assembler -

Palm software interface should discourage peripheral rope -

Pat. Smith

J. D. GEORGE

FEB 06 1973

Shift instruction.

shift left, right, rotate -

~~shift~~

Pat - think about shift bit states.

May be able to get by with hardware

shift left & rotate -

Tyrametic Keys? Question to Pat Smith -

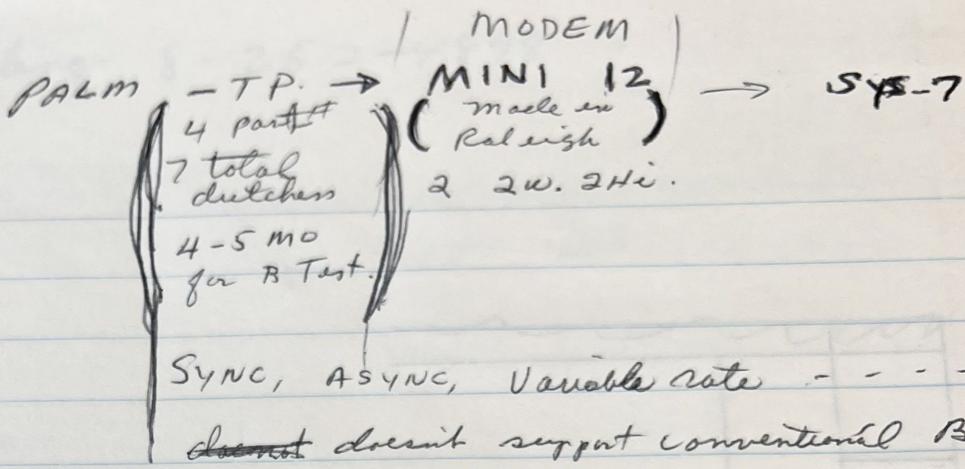
OK - ? questionable use -

SCAMP II - 1130 on a card -

much faster -

Can then do basic, cobal, etc.

J. D. GEORGE
FEB 07 1973



Chet Rataski 442-5678 Bi Sync - Acc Co
schedule.
operation.
size & packaging.

1200 baud bi Sync -
micro programmed 2K bytes of
VTL $2\frac{1}{2}$ 4x3 → programs written
Hardware running mid - March

APL can be only start loop

Latest thing in comm. SDLC o

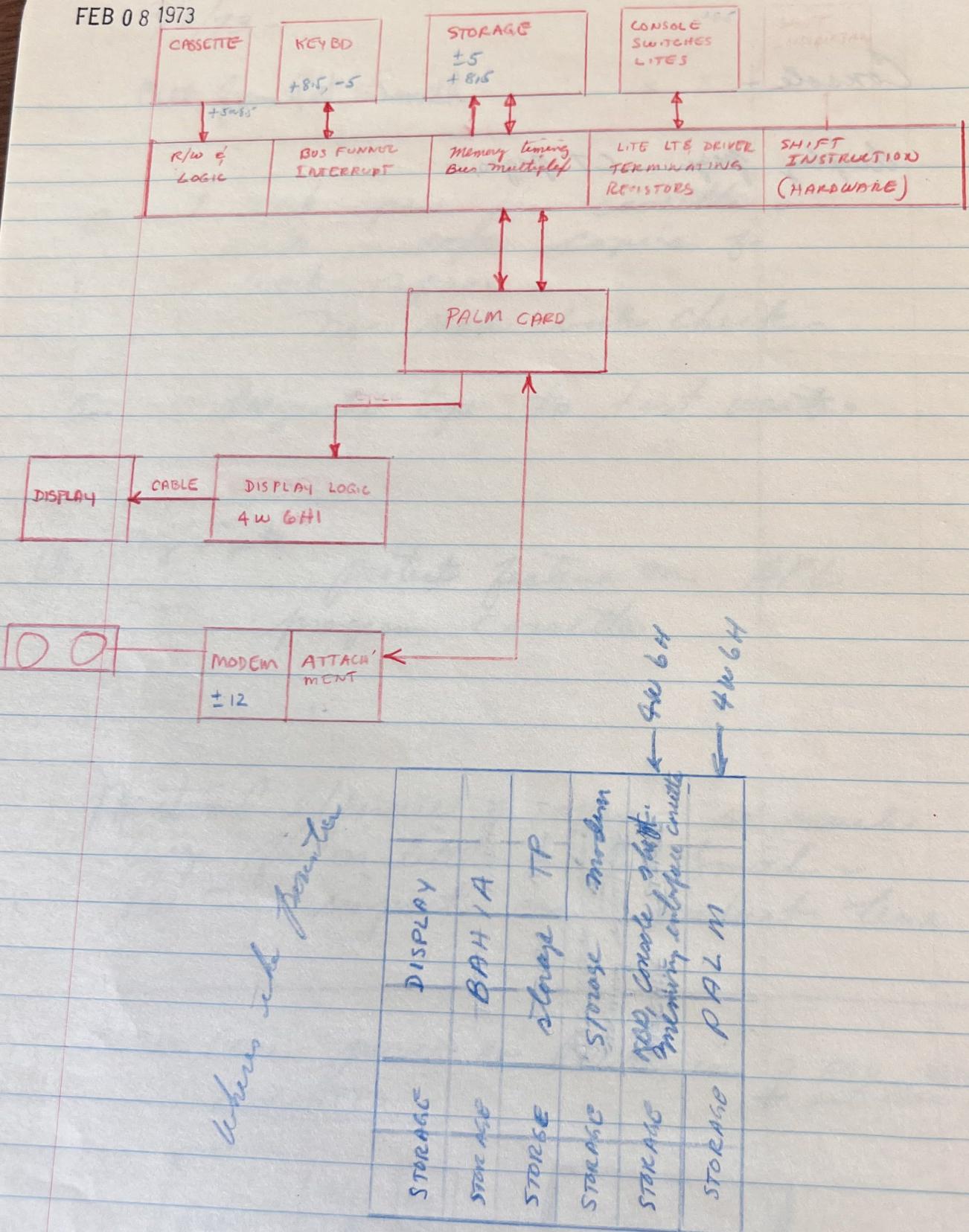
Architecture paper being circulated.

B1

(C)

J. D. GEORGE

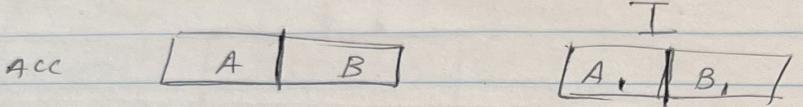
FEB 08 1973



Rat Smith

2/8/73

left
shift, & Rotate
shift left + zero low order
shift right + zero hi order.



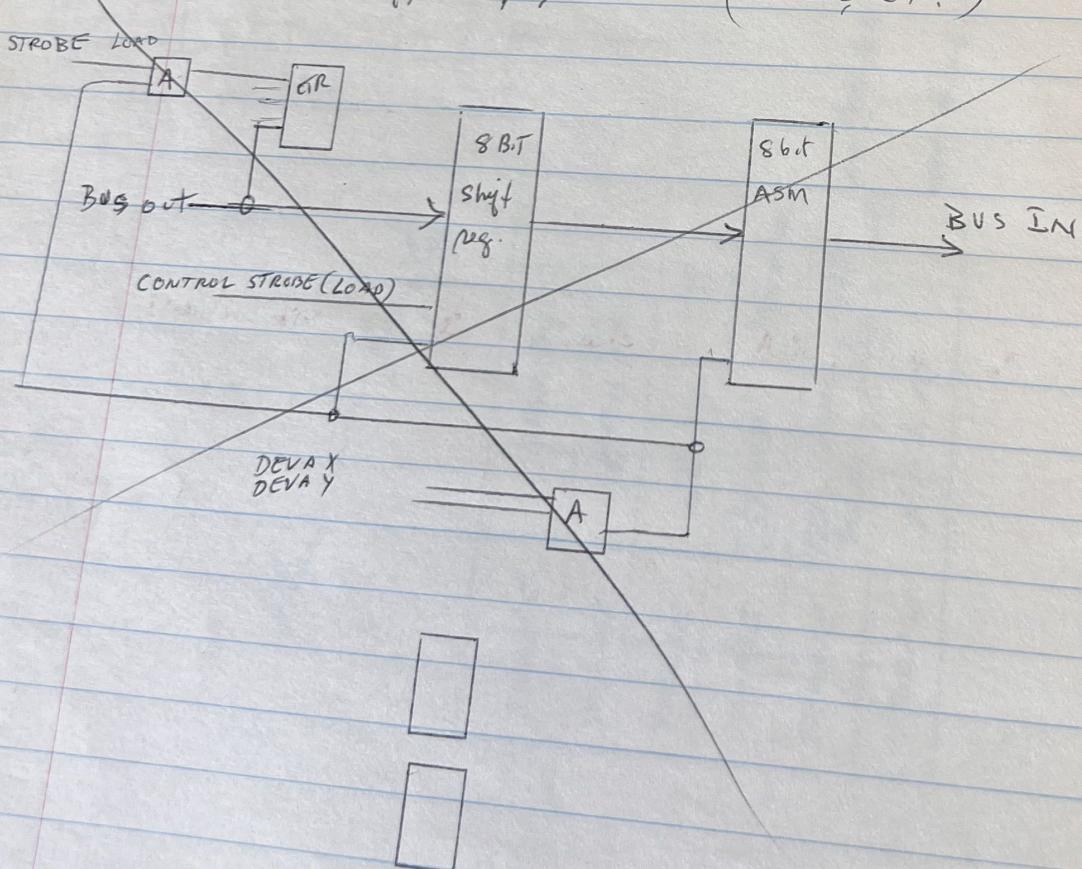
{ Shift L 3 & cla.
both bytes. Shift

Shift L & Rot

Shift L & φ

Shift R & φ

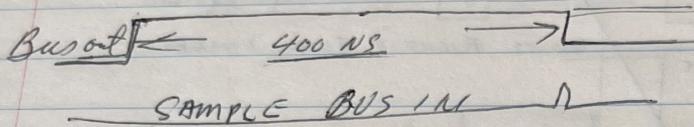
(S L & CT.) ?



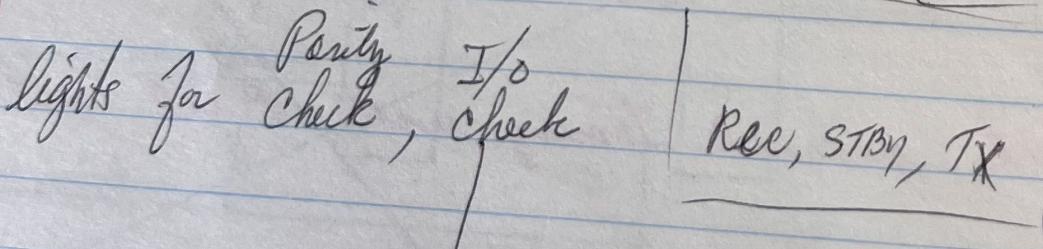
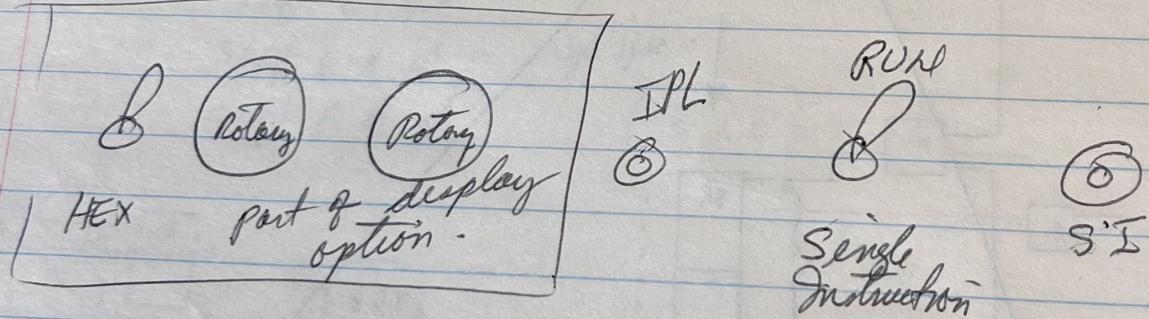
J. D. GEORGE
FEB 09 1973

Reel to Bill Tull.

Timing of get to Register instruction -
Re shift instruction -



Console :



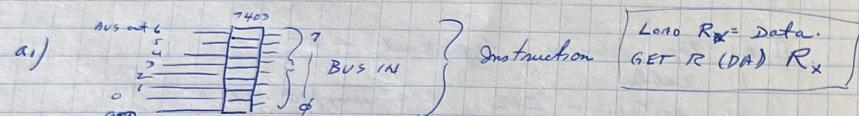
in paper
Cassette not ready
?

Premarley
for Troubleshooting.

7/11/93 Shift instruction - See page 8

Possible methods to implement requirement for faster shift.

- all left + 8 left rotate in software and shift right one by hardware (Byte only) -
- Right shift; left shift, left shift + rotate in Hardware. (Byte only) - software for multi byte shift.
- 16 bit hardware shift.



additional shifts per instruction -
GP Routine for shift right -
Set count R_n
Load data R_{n+1}
GETR (DA) R_{n+1}
Jump $R_n = \phi$
Return to loop
~~return~~ shift routine.

Exp shift 3 = 10 instructions -

a2) Shift 16 bits 3 positions to right.

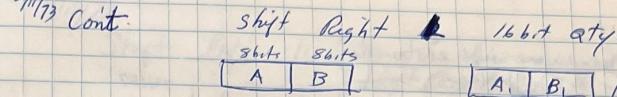
A	B
---	---

A ₁	B ₁
----------------	----------------

- a) SAV A $\rightarrow A_1$
b) Load AB to work Reg (~~RA~~) R_{n+1}
c. Set count = 3 ($R_n = 3$)
GETR (RA) R_{n+1}
Jump $R_n = \phi$
Return
Move B to B_1
~~RA \rightarrow Lo A₁ $\rightarrow R_{n+2}$~~
CL

- ① Shift B_1 -3R
② Shift A_1 5 left
③ OR $A_1 + B$
④ SHIFT A 3R

7/11/93 Cont.



Shift B₁
a Transfer AB to A₁B₁
b set count = 1
Get R B₁
Decr. count
Jump count = ϕ
return

Shift Left A₁
Load SR value:
Load SR complement value 8⁵ compl. (or load SR value & Count to 8.)
Get high 8 bits
HTL A₁ $\rightarrow R_{n+2}$
add $R_{n+2} \rightarrow R_{n+2}$
Add count + 1
Jump count ≥ 8
return.
345678

Shift R₁, A₁
HTL A $\rightarrow R_{n+2}$
set count = 1
GETR R_{n+2}
decr count
Jump count = ϕ
return..

LTH $R_{n+2} \rightarrow A_1$ (A₁B₁ shift by ~~Left~~ Right 1.)

45 instruction times to shift right 1.

21 instructions for shift right ~~1 to 7~~.

48 instruction times for shift right 16 bits 2 positions -
51 " " " " " 3 positions

hardware register for 16 bit shift right or shift left.
3 bits of ~~ctrl~~ low bit of address for Put instruction

CTRL = set count & ~~left~~ right mode, + SLR byte load LT
put Byte (DA) = Load Low ORDER byte and Set Load byte Z LT
put byte (DA) = Load Hi ORDER byte + start shift:
~~GETR~~

Clr Low Byte R_n

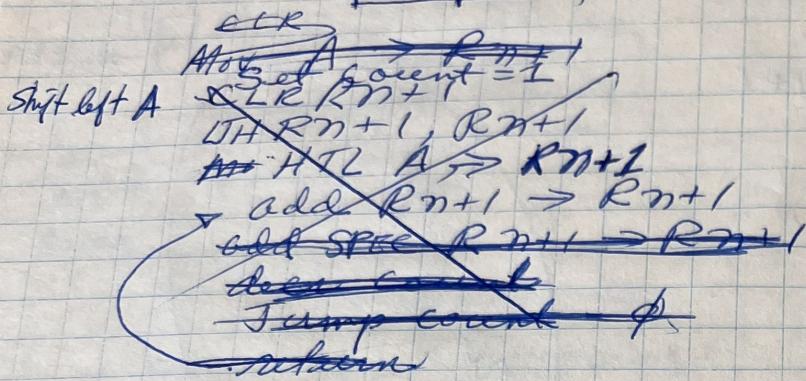
GETR (DA) R_n = get high order byte to R_n.
Set Low byte R_n = see over
GETR (DA) R_n = get low byte to R_n.

2/11/73

Shift left & rotate 16 bits. Hardware shift right by 1.

A	B
---	---

A ₁	B ₁
----------------	----------------



Shift left A -

set count
~~Mov A B~~ → R_{n+2}
clr R_{n+1}

LTH R_{n+1} → R_{n+1}

LTH R_{n+1} → R_{n+2}

HTL A → R_{n+1}

~~HTL A~~

→ add R_{n+1} → R_{n+1}

add R_{n+2} → R_{n+2}

add SPL R_{n+1} → R_{n+2}

add SPL R_{n+2} → R_{n+1}

clear count

Jump count = φ

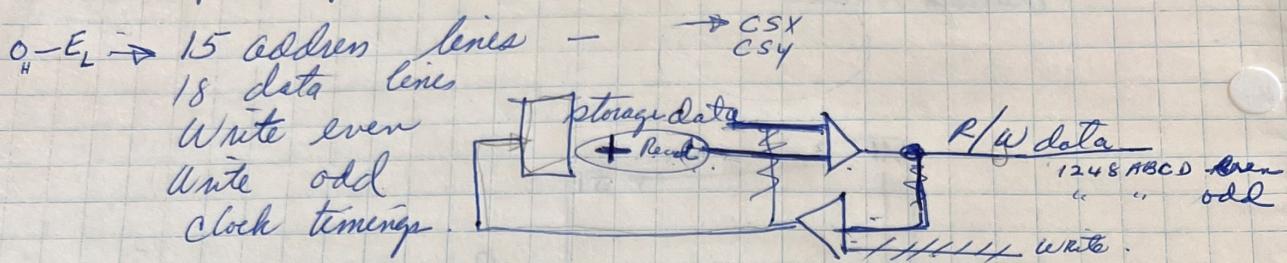
return

LTH R_{n+1} → R_{n+2} (R_{n+2} = shifted n=16)

R _{n+1}	00	A
------------------	----	---

R _{n+2}	00	B
------------------	----	---

Memory interface



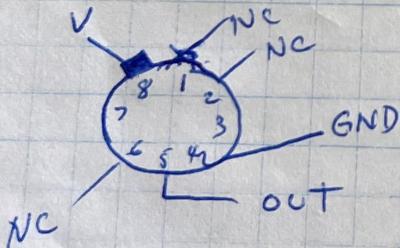
Data bus must be + when not in use.

IPL:

Program ROS to support KBD-
ROS .., Cassette.

1/2 SLD board - 812457 - VTL manual
12-3

OSC 2410055 15.0912 MC.



Bottom View.

391-0500 IBM, BOCA

X4176

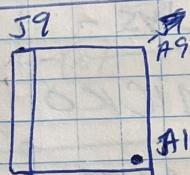
2/12/72 Module # 2706503

1	6512
2	6504
3	6505
4	6506
5	6507
6	6508
7	6509
8	6510
9	6511

PACM Modules

Gene Hopp ~~2388~~

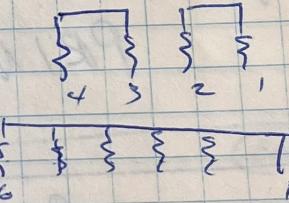
~~Dick Cicone.~~



R PAC

R, PACS 2392484

270-2



8 - 2392700

2K

6 PAC. AS ABOVE

11 2392712

750-2

2392699

7.32K

6 PAC as above

2392500

