

9-19-73

To: J. George
For your information.

V. Kendrick
28C/031-3, Boca Raton

IBM CONFIDENTIAL

September 10, 1973

IBM

Proposed SCAMP ROS Schema

Reference:

54K bytes of Emerald ROS will be available on one 4W x 3H card. ROS will be used as an I/O device. Transfer of data from ROS to RAM will be accomplished in groups of 256 bytes per page. The last two bytes of the page transferred from ROS will contain a 16 bit hardware CRC counting register which must be read after completion of transfer of the page (256 bytes). Reading the CRC Register and comparing this count with the last two bytes transferred from ROS provides for error detection.

Two programming restrictions apply when transferring data from ROS to RAM:

- 1) The least significant byte of the first RAM address to which a ROS page is to be transferred must be /00.
- 2) A fixed program sequence, not including housekeeping must be followed to insure proper data transfer. This sequence is as follows:

Put Byte -

Identifies to ROS the page to be transferred.

Clear Bit -

Sets the low order byte of the RAM address to /00 and allows adequate time for the first ROS byte to be available.

Get Byte -

Transfers a ROS byte to RAM.

Jump -

Test for end of page and jumps if page transfer is complete.

File

-2-

September 10, 1973

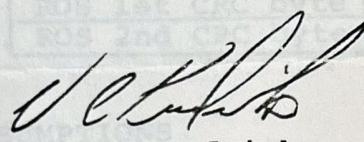
Submitted - 1 -

Branches back to get byte instruction if page transfer
is not complete.

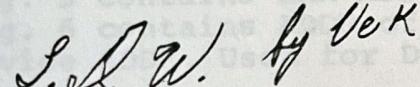
Get to Reg

Transfers the two bytes of CRC Register.

NOTE: See attachments for examples of software and hardware.



V. C. Kendrick



L. D. Willson

:evh

Attachments

Determine Page, Set Registers, etc.

cc: Mr. R. E. Abernathy

Programmer (4) Use Reg. 6 and POS Device ADDR.

Clear Bit - Clear Low order Byte of Reg. 5 to /FF.

Get Byte - Use Reg. 5, modified @ POS Device ADDR.

Jump All Data Bits Present - Test Low Order Byte of Reg. 5 for /FF

Submitted - 1 - BRANCH BACK TO Step 1

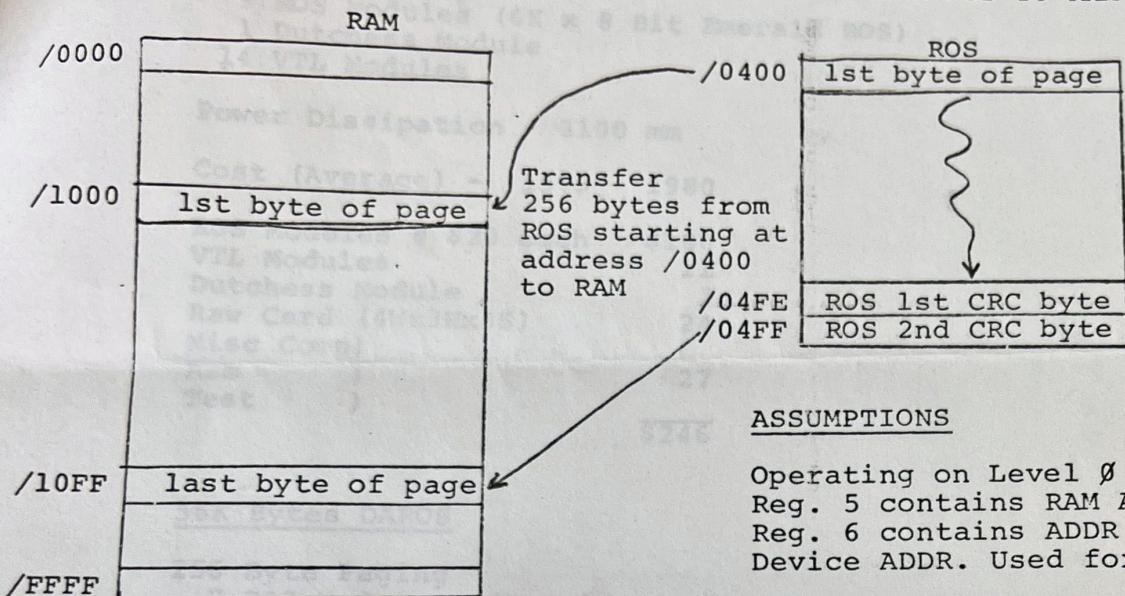
Get To Reg. 1 - Use POS Device ADDR.

Get to Reg. 2

Housekeeping - Compare CRC Characters for Error, Determine if all
Required Pages Have Been Transferred, etc.

548 Bytes

EXAMPLE OF PAGE TRANSFER FROM ROS TO RAM

ASSUMPTIONS

Operating on Level 0
 Reg. 5 contains RAM ADDR.
 Reg. 6 contains ADDR of ROS ADDR.
 Device ADDR. Used for Data Transfer

INSTRUCTION SEQUENCE

- 1) Housekeeping - Determine Page, Set Registers, etc.
- 2) Put Byte - (/04) Use Reg. 6 and ROS Device ADDR.
- 3) Clear Bit - Clear Low order Byte of Reg. 5 to /00.
- 4) Get Byte - Use Reg. 5, modifier 0 ROS Device ADDR.
- 5) Jump All Data Bits Present - Test Low Order Byte of Reg. 5 for /FF
- 6) Subimmed - 1 - Branch Back to Step 4
- 7) Get To Reg 1 - Use ROS Device ADDR.
- 8) Get to Reg 2
- 9) Housekeeping - Compare CRC Characters for Error, Determine if all Required Pages Have Been Transferred, etc.

54K Bytes ROS

256 Byte Paging
 9 ROS Modules (6K x 8 Bit Emerald ROS)
 1 Dutches Module
 14 VTL Modules

Power Dissipation - 3100 mw

Cost (Average) - 1975 - 1980

ROS Modules @ \$20 each	\$180
VTL Modules	11
Dutches Module	3
Raw Card (4Wx3Hx3S)	24
Misc Comp)	
Asm)	27
Test)	
	<u>\$246</u>

56K Bytes DAROS

256 Byte Paging
 7 ROS Modules (4K x 18 Bit DAROS)
 6 VTL Modules
 1 Dutches Module

Power Dissipation - 2800 mw

Cost (Ultimate)

ROS Modules @\$50 each	\$350
VTL Modules	5
Dutches Module	3
Raw Card	24
Misc Comp)	
Asm)	26
Test)	
	<u>\$408</u>

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	<u>\$246</u>

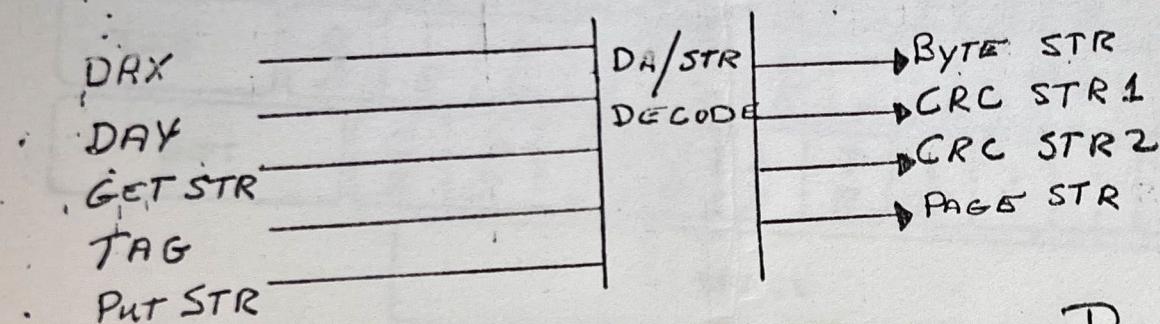
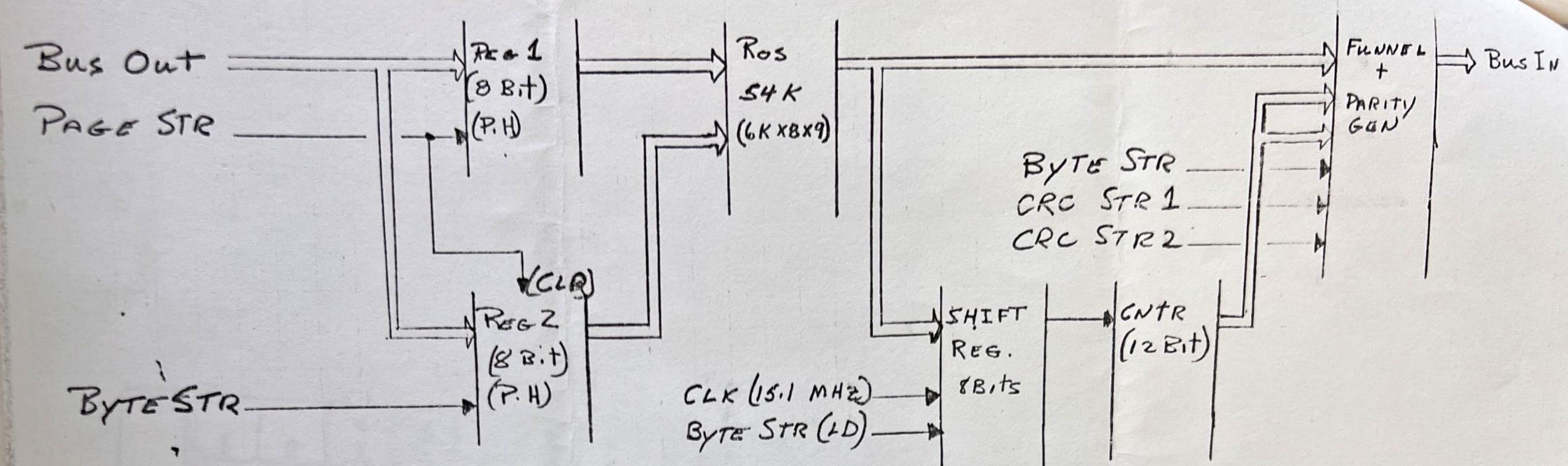
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Ros Block Diagram

VCK 9/6/73