

# Distributed/Cluster Computing for Data Stream Mining: Draft Notes

A thesis  
submitted in partial fulfilment  
of the requirements for the Degree  
of  
Master of Science  
at the  
University of Waikato  
by  
Vladimir Petko

University of Waikato  
2016

# Abstract

The thesis is focused on elucidating GPU computing feasibility for clustering tasks

# Acknowledgements

# Contents

Abstract	i
Acknowledgements	iii
1 General Purpose GPU Computing	2
2 System Architecture	12
3 k-Nearest Neighbours	15
4 Stochastic Gradient Descent	30
5 Experimental Results	33
6 Conclusions and Future Work	37

# List of Figures

1.1	CPU versus GPU hardware architecture. Reproduced from NVIDIA GPU ARCHITECTURE and CUDA PROGRAMMING ENVIRONMENT by Alan Tatourian[65] . . . . .	3
1.2	GPU Memory Tiers. Reproduced from NVIDIA GPU ARCHITECTURE and CUDA PROGRAMMING ENVIRONMENT by Alan Tatourian[65] . . . . .	4
1.3	GP GPU technologies tree. Reproduced from C. Nugteren, Improving the Programmability of GPU Architecture, p. 21 [53]	5
2.1	SGD classifier training activity. . . . .	13
3.1	Left; Four matrix-vector multiplication kernels designed to perform well at different shapes $m \times n$ of $A$ . Middle; Tuning mesh. Right; Best kernel in practice. The dashed line indicates the minimum 21504 rows needed in $A$ for full occupancy of the Nvidia Tesla C2050 card in a one-thread-per-row kernel. Note the logarithmic axes. Reproduced from High-Performance Matrix-Vector Multiplication on the GPU by Hans Henrik Brandenborg Sørensen[63] . . . . .	17
3.2	Selection Algorithm Performance for $K=128$ . Test configuration GPU R9 390, CPU AMD A8-7600, AMD Catalyst version 15.20.	18
3.3	k-d tree construction and NN-search pseudocode . . . . .	20

3.4	Distributions with low intrinsic dimension. The purple areas in these figures indicate regions in which the density of the data is significant, while the complementary white areas indicate areas where data density is very low. The left figure depicts data concentrated near a one-dimensional manifold. The ellipses represent mean+PCA approximations to subsets of the data. Our goal is to partition data into small diameter regions so that the data in each region is well-approximated by its mean+PCA. The right figure depicts a situation where the dimension of the data is variable. Some of the data lies close to a one-dimensional manifold, some of the data spans two dimensions, and some of the data (represented by the red dot) is concentrated around a single point (a zero-dimensional manifold). Reproduced from Learning the structure of manifolds using random projections by Freund Yoav et al.[39]	21
3.5	Left: Partitioning produced by k-d tree. Right: Partitioning produced by Random Projection Tree. Reproduced from Learning the structure of manifolds using random projections by Freund Yoav et al.[39]	22
3.6	Random Projection Tree Pseudocode - Random Tree Max [35]	22
3.7	Random Projection Tree Pseudocode - Random Tree Median[35]	23
3.8	Fast Johnson-Lindenstrauss transform[22] vs. sparse matrix implementation[20] using ViennaCL. Test configuration GPU R9 390, CPU AMD A8-7600, AMD Catalyst version 15.20.	26
3.9	Z-Order Curve. Red lines highlight some region jumps. Green shows locality-preserving region.	28
4.1	Kernel calls for SGD classifier training	31
5.1	Naive KNN implementation (Radeon Mobility HD5730)	34

---

5.2	Stochastic Gradient Descent Training Speedup (AMD R9 390, Spectre vs MOA implementation on AMD A8-7600)	35
5.3	Stochastic Gradient Descent Training Latency (AMD R9 390 vs MOA implementation on AMD A8-7600)	36

# List of Tables

1.1	Input Size and Execution Time . . . . .	7
-----	---	---



# Introduction

In real world applications such as industrial monitoring, sensor networks, financial data generate large unbounded streams of data which has to be processed with pre-defined response time. The processors capabilities limit the bandwidth of the stream which can be processed. Parallelizing processing algorithm will increase maximum bandwidth while maintaining the response time requirement.

# Chapter 1

## General Purpose GPU Computing

### Introduction

The modern Graphical Processing Units (GPU) greatly outpace CPUs in arithmetic throughput and memory bandwidth for data-parallel tasks. Since 2001 the efforts were made to port data parallel algorithms to GPUs - first using shader languages such as HLSL, then with the release of Nvidia G80 in 2006 using extensions to C programming language - CUDA[12]. Presently there is a number of programming frameworks targetting specifically GPU architecture such as CUDA[51], OpenCL[11], RenderScript[16], DirectCompute[5] and more generic parallel-processing frameworks such as OpenMP[14] and AMP[3] which provide GPU backend as one of the targets. The differences in the hardware architecture between CPU and GPU is reflected in the programming model of the traditional GPU-specific languages which contain hardware architecture specific language constructs. This chapter provides an overview of GPU architecture, most known programming frameworks, lists limitations of the traditional GP GPU programming, discusses OpenCL 2.0 standard which addresses some of the limitations and Heterogenous System Architecture (HSA) an optimized platform architecture for OpenCL 2.0.

## GPU Architecture

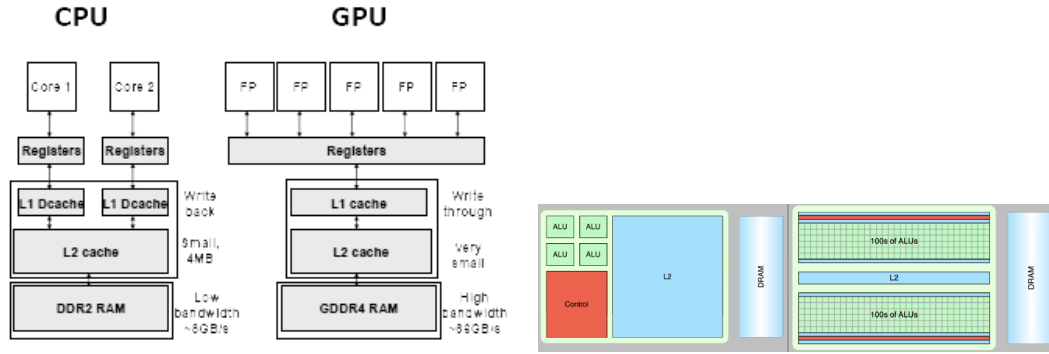


Figure 1.1: CPU versus GPU hardware architecture. Reproduced from NVIDIA GPU ARCHITECTURE and CUDA PROGRAMMING ENVIRONMENT by Alan Tatourian[65]

The main differences between modern CPU and GPU architectures are the level of parallelism and ability to directly address tiered memory. Modern CPU with 2 hex-cores support maximum of 12 threads (24 with hyperthreading) and minimal unit of execution for the NVIDIA GPU (called *wavefront*) is 32 threads. Modern GPUs implement SIMT (Single Instruction - Multiple Thread) execution model (AMD/NVIDIA desktop GPUs) first introduced by NVIDIA in G80 model[12]. The single unit of scalar instructions called *kernel* is scheduled to execute in blocks of data-parallel threads on SIMT hardware. Each instruction in a block is executed in a lock-step. The control divergence is emulated by *masking* - the device executes instructions from both branches of the conditional statement[17][51]. The CPU thread is a heavy-weight entity which is centered around execution of a specific task for an extended period of time. Whenever CPU needs to preempt the thread, the register state is stored and another thread takes over. This makes a context switch a costly operation and operating systems attempt to minimize number of context switches per second. The GPU context switch is an extremely lightweight operation and is routinely used for the latency-hiding - whenever the wavefront is waiting on data, the GPU schedules another wavefront for execution. The GPU registers are private for each thread and are not reallocated until thread execution completes.

Modern CPUs provide a flat view of the operating system memory while GPUs divide memory in tiers based on the access speed:

- *private/register* - private to the current thread
- *local* - shared within a *threadblock*
- *global* - accessible by every thread

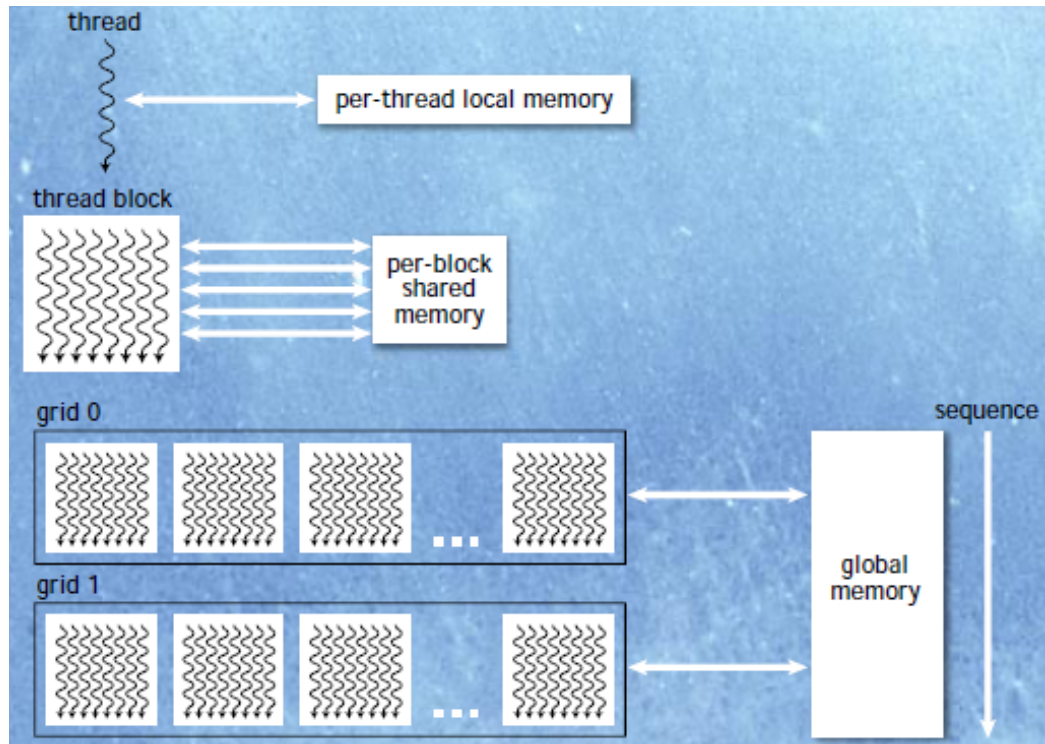


Figure 1.2: GPU Memory Tiers. Reproduced from NVIDIA GPU ARCHITECTURE and CUDA PROGRAMMING ENVIRONMENT by Alan Tatourian[65]

The GPU programming following abstractions:

- *Kernel* - a unit of execution
- *Thread* - a single unit of processed data
- *Threadblock* - a group of *threads* sharing same *kernel* and *local* memory.

The unit of scheduling is called *wavefront* in AMD terminology or *warp* in NVIDIA and typically consists of 32 threads on NVIDIA and 64 on AMD hardware. The GPU chip is equipped with a number of SIMT cores which

execute same instruction for each *warp*. Divergence of control results in under-load of the processing units and reduces performance. The branching should be reduced to wavefront granularity to avoid wasting execution cycles[62][51] It should be noted that the wavefront size is a hardware specific feature and the optimization should be performed at the run-time.

## General Purpose GPU Computing Frameworks

Existing General Purpose GPU (GP GPU) computing frameworks can be classified by the level of provided hardware abstraction: high-level frameworks integrate with existing high-level programming language such as Java to provide parallel computing capabilities without exposing any hardware details[13], traditional GPU languages such as CUDA[51] expose task scheduling and memory management giving the expert user fine-tuning capabilities, low level languages provide intermediate binary format compatible with multiple hardware targets. The tree of the GP-GPU technologies is presented in the Figure 1.

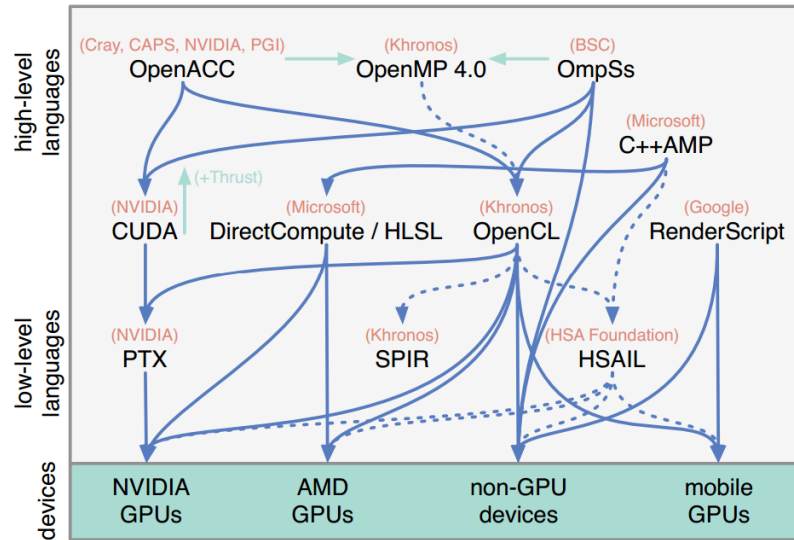


Figure 1.3: GP GPU technologies tree. Reproduced from C. Nugteren, Improving the Programmability of GPU Architecture, p. 21 [53]

## High Level Languages

OpenACC and OpenMP are high level parallel programming frameworks that specify a set of annotations, environment variables and library routines for shared memory parallelism in C/C++ and Fortran programs[?][14]. Microsoft C++ AMP[3] is a C++ library which enables parallel computations for CPU and GPUs (using Microsoft DirectX Shading Language) Rootbear GPU compiler provides a transparent compilation of Java code into CUDA[56]. Aparapi provides a way to generate OpenCL kernel code from Java, theoretically allowing code which can be executed on CPU and offloaded to GPU if needed[1]. Project Sumatra is a OpenJDK project which focuses on development of the Hotspot virtual machine capable of offloading JDK 8 Stream API[10] computations to the GPU[13].

## GPU-specific Languages

GPU-specific languages provide a programming model consistent with the GPU hardware implementation.

- CUDA - A programming language for NVIDIA hardware based on C language. Kernels are expressed as C-functions for one thread with parallelism defined at run-time by specifying dimensions of execution grid and thread blocks[51]
- OpenCL 1.X builds upon ideas implemented in CUDA by adding device management APIs and providing hardware-agnostic programming specification. OpenCL gives *write once-run anywhere* guarantee but does not give any performance consistency guarantees across different hardware[64].
- RenderScript - Android GPU computing component which uses OpenCL with Java binding programming model - C-style kernels and Java-based control code. RenderScript does not provide any APIs for the *work-*

*group* size control in the bid to provide performance portability between different devices[16].

- DirectCompute/HLSL - Microsoft Parallel Computing.

## Low-Level Languages

The low level assembly representation is used to abstract compiler implementation from the actual hardware since each model or even revision may have a different instruction set. The translation is performed by *Just-In-Time* compiler before the kernel execution. Each vendor provides different low level specifications: NVIDIA CUDA uses Parallel Thread Execution and Instruction Set Architecture (PTX ISA)[15], Khronos Group specifies Standard Portable Intermediate Representation(SPIR)[18], and HSA Foundation specifies Heterogenous System Architecture Intermediate Language (HSAIL)[19].

## Limitations

**Input Size** The massively parallel nature of GPU platforms require a certain amount of data to be passed to the kernel to achieve maximum performance. Table 1.1 shows execution time of a kernel which assigns index to each array element  $X_i = i$  on AMD A8-7600. The execution time starts to increase when input size is above 1024 and remains constant for lower values. To maximum performance on AMD A8-7600 will be achieved when input size will exceed 1024 elements.

Global Size	256	512	768	1024	1280	2560	3072	3584	4608	4864
Execution Time ( $\mu$ sec)	8	8	8	8	9	9	10	11	11	12

Table 1.1: Input Size and Execution Time

**GPU Memory Size and Host-GPU Transfer** The discrete GPU requires transfer of data from the host to the GPU memory which adds additional overhead to the computations and requires task partitioning according to the mem-

ory specification of GPU[61]. Memory transfer is a bottleneck for Aparapi and its developers allow explicit memory management[1]. This effectively reduces framework which promises CPU-GPU interoperability to the Java wrapper of the OpenCL API.

**Kernel Launch** There is a constant time needed to setup kernel launch which might offset any gain from parallelization if the data can be processed sequentially faster.(NB. Amdahl's law) It is impossible to schedule kernel execution from within the kernel itself requiring a mix of kernel and host code if several iterations are required.

## OpenCL 2.0

OpenCL 2.0 standard[11] introduces several features which attempt to address limitations of GPU programming:

- Shared Virtual Memory - both host and kernel code share same address space thus either hiding memory transfers (discreet GPU driver stack) or if backed by the hardware architecture such as HSA eliminate its need[19]
- Dynamic Parallelism - OpenCL 2.0 allows scheduling of kernels from within a kernel without host interaction reducing host CPU bottleneck.
- Pipes - pipes feature allows passing data from kernel to kernel without processing the whole input which allows to obtain the results of computation faster.

## HSA Platform

AMD introduced Heterogeneous System Architecture platform as an optimized platform architecture for OpenCL 2.0. Its specification introduces a set of requirements that allow both GPUs and CPU share same memory space, synchronize execution using signals and atomics and schedule execution both from



GPU and CPU[19]. Task execution is performed by *agents* which represent CPU or GPU nodes. The task execution is scheduled via *queues* and synchronized using *signals*. HSA memory model guarantees sequential consistency for the correctly synchronized programs.

*Software Available:* At the moment (Feb 2014) there is a OpenCL 2.0- $\dot{\iota}$ HSA IL compiler available[8] and a Linux-based runtime environment[7].

## HSA Queues

HSA uses queues to schedule code execution. A HSA *queue* is a ringbuffer which contains *packets* with either call or synchronization parameters. The queue maintains two indexes - read index and write index. Write index is modified by the user and used to submit packets to the queue. The read index is updated by the packet processor whenever the packet is taken for execution. As soon as packet is written to the queue the ownership is taken by the HSA packet processor and it may change packet contents at any time[19]. Compared to traditional dispatch where the execution is scheduled via user-mode and kernel-mode driver layers the HSA dispatch intends to be lightweight and source-agnostic way of scheduling execution. The HSA Queues support work-stealing that is several HSA agents may be attached to the queue to share the workload.

## HSA Signals

HSA uses *signals* to perform synchronization between host and kernels being executed or to signal completion of the task. A *signal* is essentially a shared memory variable modified by the HSA agent. Runtime environment provides a way to check the value of the signal or wait for the specific value.

## HSA Memory Model

The sequential consistency was first defined by L. Lamport as “..the result of any execution is the same as if the operations of all the processors were

executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program.” Modern processors (ARM, x86, Itanium, POWER) introduce relaxed memory model to allow a range of the hardware optimizations to provide better performance by reordering load and store operations[49]. Platform specification states

The HSA memory consistency model is a relaxed model based around RCsc semantics on a set of synchronizing operations. The standard RCsc model is extended to include fences and relaxed atomic operations. In addition HSA includes concepts of memory segments and scopes.

[19] Similiar to Java Memory Model[?] it guarantees sequential consistency for the correctly synchronized programs, that is 'synchronizing operations meet the requirements for sequential consistency within each scope/segment instance'[19]. The specification introduces several memory segments: “

- Global segment, shared between all agents.
- Group segment, shared between work-items in the same work-group in a HSAIL kernel dispatch.
- Private, private to a single work-item in a HSAIL kernel dispatch.
- Kernarg, read-only memory visible to all work-items in a HSAIL kernel dispatch.
- Readonly, read-only memory visible to all agents

” Each particular memory location is always associated with one and only one segment and all operations apply to only one segment with the exception of fence operations[19]. In addition to memory segments HSA memory model introduces *scopes* : wavefront, work-group, component and system. They can be used to reduce visibility of the memory operation compared to the default supported by the segment. The global segment may use any of the specified scopes and group segment is limited to wavefront and workgroup scopes[19]. Different workgroups accessing a global variable with the workgroup scope

will work with different instances of the variable. The write serialization only applies to the operations within the segment/scope that they specify.

## Implementation Notes

Sequential execution of several packets sometimes may be faster than submission of all packets and waiting for the barrier packet. For instance first scenario runs in 8  $\mu\text{sec}$  per packet on AMD A8-7600 and second results in 193  $\mu\text{sec}$  per packet. According to AMD support this is caused by the CPU going into power-saving mode while kernel is running. There is a constant time needed to setup kernel launch, e.g. for AMD A8-7600, it is 6  $\mu\text{sec}$  using HSA.

## Conclusion

The modern specifications such as OpenCL 2.0 and HSA attempt to address some of the latency issues of the GPU programming by introduction of the shared memory and lightweight dispatch and data passing mechanisms. This work will focus on the evaluation of suitability of those technologies for the latency-sensitive data stream processing.

# Chapter 2

## System Architecture

The implemented data stream processing library provides a set of classification algorithms for Massively Online Analysis(MOA)[28]. The library uses existing linear algebra package ViennaCL[66] which allows multiple backends such as CUDA, OpenCL, CPU and extends it with the machine learning algorithms such as nearest neighbours search and stochastic gradient descent.

**MOA interface** The ViennaCL library is implemented in C++ and as such requires Java Native Interface[9] to be used to interface from the Java Virtual Machine. Java Virtual Machine manages its own memory space and garbage collector may move the data at any time. JNI provides two mechanisms to access the array data from the native code. First is copying - the java pointer is locked by the critical section and array content is copied to the native array. Second skips the copying and provides direct access to the java pointer. Both involve entering and exiting a critical section and impose significant performance loss due to the copying and locking overhead. Those costs can not be avoided but can be minimized by moving them to the instance creation/-modification time - the object constructor will call the native method which allocates the native data structures and moves data from the Java storage to the native one.

The alternative solution uses *java.misc.Unsafe* class to manipulate offheap memory directly. The native code allocates GPU shared virtual memory and

passes the pointer to the Java implementation. Java code uses *java.misc.Unsafe* methods to update data in parallel to training. Figure 2.1 shows the training process of the Stochastic Gradient Descent classifier. The instances are accumulated in batches on the main thread of execution, the batches are passed to the data transfer thread that handles CPU-GPU transfer and then the training thread is triggered to run GPU kernels. Whenever the evaluation ( *getVotesForInstance*) is called the threads process the last available batch and meet at the synchronization point stopping execution.

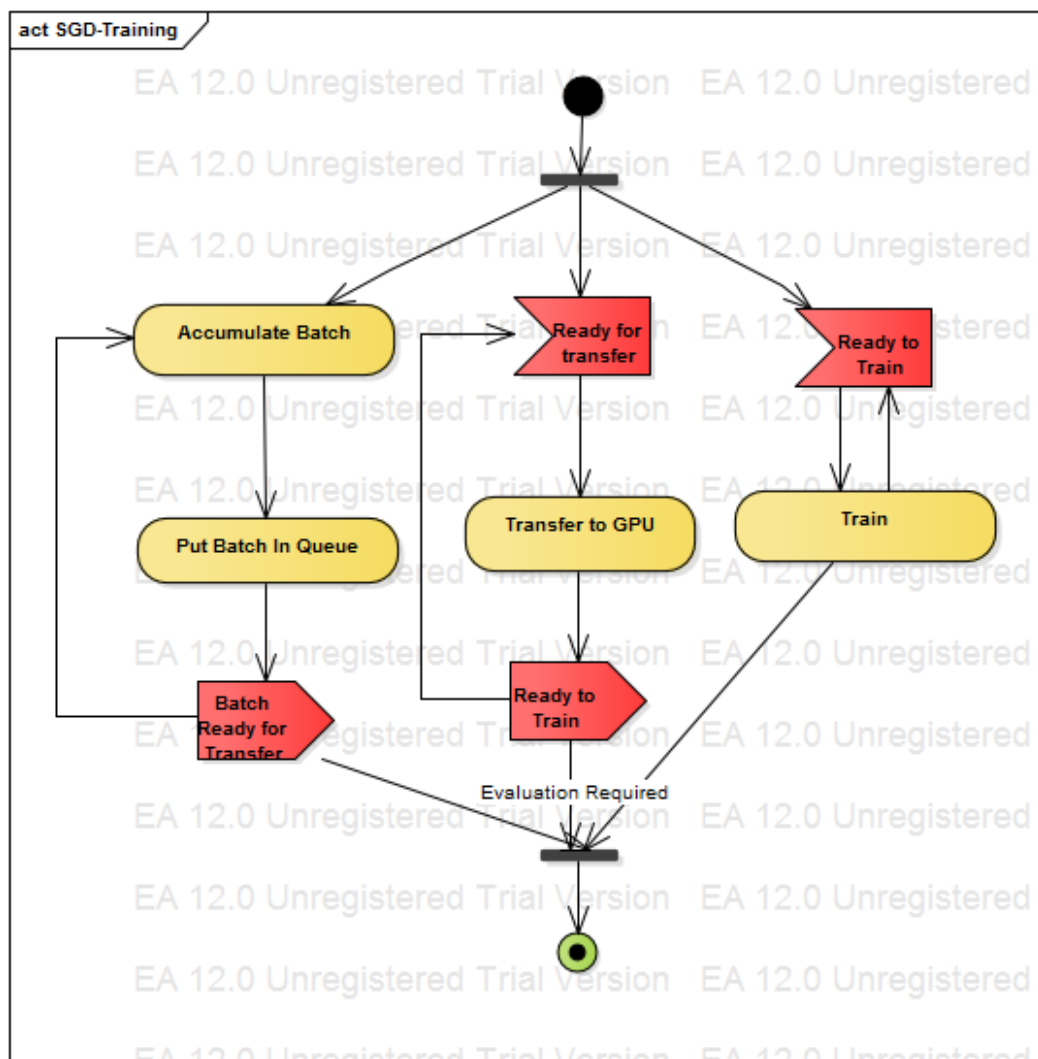


Figure 2.1: SGD classifier training activity.

**GPU Memory Limits** The library implementation stores the instance data as the native ViennaCL types. This implies that for GPU ViennaCL backends the data will be stored in GPU memory that may be insufficient for the larger

problems. In such case the partitioning will be used - the problem data is kept in the Java memory as collection of *weka.core.Instance* objects and offloaded to GPU-backed context on as needed basis. The *weka.core.Instance* class represents the attribute values as a vector of double precision numbers. Modern consumer GPUs provide far better floating point performance than double performance. For instance modern AMD GPUs have 8x scale that is floating point performance is 8x better than double one (R390, R290). NVIDIA GPUs have 32x scale *TODO citation*. There are several works that explore using fixed precision numbers to reduce memory requirements of the machine learning tasks[58][43]. The alternate precision implementation will impose the overhead costs of double to fixed/floating point conversion if the GPU classifier will be used for instance as a part of the meta-classifier ensemble.

**HSA Backend** This work adds a new HSA backend to the ViennaCL library based on the HSA Runtime[19]. This implementation is tuned for Kaveri AMD APU and uses the same set of OpenCL kernels as the OpenCL backend. In HSA backend the main system memory is transparently mapped to GPU and vice-versa, allowing to use vector or matrix element-addressing operations without first copying data to the CPU memory space.

**OpenCL 2.0 features** At the time of writing (driver version 1642.5) the OpenCL 2.0 features such as workgroup functions and device enqueue impose significant performance impact. Atomic locks do not result in significant performance impact. The library uses Shared Virtual Memory buffers to facilitate easy switch between OpenCL and HSA backends. The ViennaCL types are constructed from *cl\_mem* representation of the SVM buffers.

# Chapter 3

## k-Nearest Neighbours

### Introduction

k-Nearest Neighbours method[34] is a non-parametric method used for the classification and regression. It computes a given instance distance to the examples with the known label and either provides a class membership for the classification which is a class most common among nearest neighbours or an object property value which is an average of the nearest neighbours. The error rate bound by twice the Bayes error if the number of examples approaches infinity. Online implementation of the algorithm uses a sliding window of example instances updated by the data stream. Window size, instance dimensionality and allowed error bounds define the optimal approach to solving k-Nearest neighbours problem. The *Exhaustive Search* has a high computational complexity of the queries but provides a constant update time. *Exact Clustering Methods* partition the search space to achieve logarithmic query complexity at expense of the window update time. *Approximate Clustering Methods* reduce search space dimensionality to provide an approximate result with a given error bound. The GP GPU computing may be used to accelerate their runtime though success for discrete GPUs depends on developer ability to eliminate branching, optimize memory access, and avoid excessive Host-GPU transfers. The latter poses a most significant problem for online k-Nearest neighbours

implementations. This chapter reviews the *Exhaustive Search*, some of the *Exact Clustering Methods* and *Approximate Clustering Methods*, provides notes on GP GPU implementation.

## Exhaustive Search

The exhaustive approach to Nearest Neighbour search is to compute distance to each instance present in the sliding window. The computational complexity of the query  $O(N^d)$  where N - number of instances and d - number of attributes. The GP GPU implementation of the exhaustive search consists of distance calculation and selection phase. The distances to the query are computed as a vector-matrix multiplication or if several queries are processed at once as a matrix-matrix multiplication. GPU implementation of those routines is available as a part of libraries implementing Basic Linear Algebra Subroutines (BLAS) [6][4][66]. The selection phase finds nearest to the query out of all the computed distances. Sismanis et. al [61] provide time complexity of reduced sort algorithms, evaluate their performance on GPU and propose to interleave distance calculation and sorting phases to hide latency. The data for the distance calculation should be offloaded to GPU while it performs the sorting phase. The sliding window is partitioned if needed across multiple GPUs according to the GPU memory capabilities and does not use instances spatial information.

## Distance Calculation

The optimal implementation depends on the size of the window and number of attributes present [63]. For the small instance size ( $\leq 100$ ) and windows less than  $10^4$  elements one thread per instance implementation will provide the best solution. Best all around distance calculation should apply different strategies depending on the window size and number of attributes [63]. The alternatives are presented in the Figure 3.1.



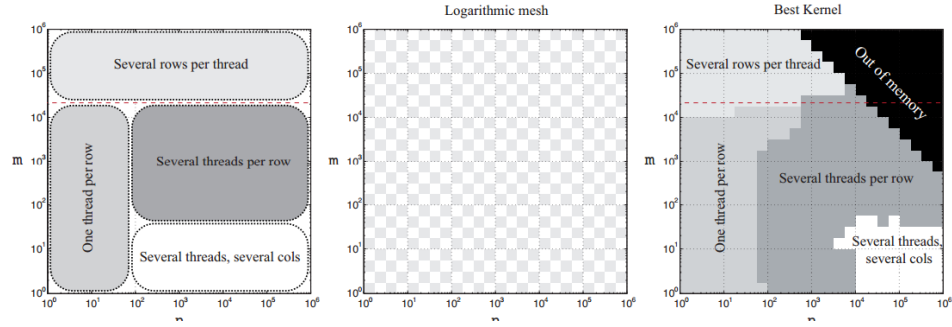


Figure 3.1: Left; Four matrix-vector multiplication kernels designed to perform well at different shapes  $m \times n$  of  $A$ . Middle; Tuning mesh. Right; Best kernel in practice. The dashed line indicates the minimum 21504 rows needed in  $A$  for full occupancy of the Nvidia Tesla C2050 card in a one-thread-per-row kernel. Note the logarithmic axes. Reproduced from High-Performance Matrix-Vector Multiplication on the GPU by Hans Henrik Brandenburg Sørensen[63]

The distance calculation primitive provided as part of the master thesis uses one thread per row approach.

## Selection

Alabi, et.al evaluated different selection strategies based on bucket sort algorithm and Merrill-Grimshaw implementation of radix sort[23].

The selection phase may be interleaved with the distance calculation to utilize both CPU and GPU cores and benefit from the better sort performance on low window sizes[50].

Figure 3.2 shows measured performance of different selection strategies - merge sort from AMD Bolt library[2], bitonic sort similar to reference AMD implementation and radix select based on Alabi, et. al. implementation[23]. The CPU sort and choose is a clear winner for small ( $\leq 65535$ ) window sizes. The merge sort should be applied to sub 2<sup>25</sup> windows and radix select (with data copy) should be used for larger window sizes. *update with clogs - i have it implemented*

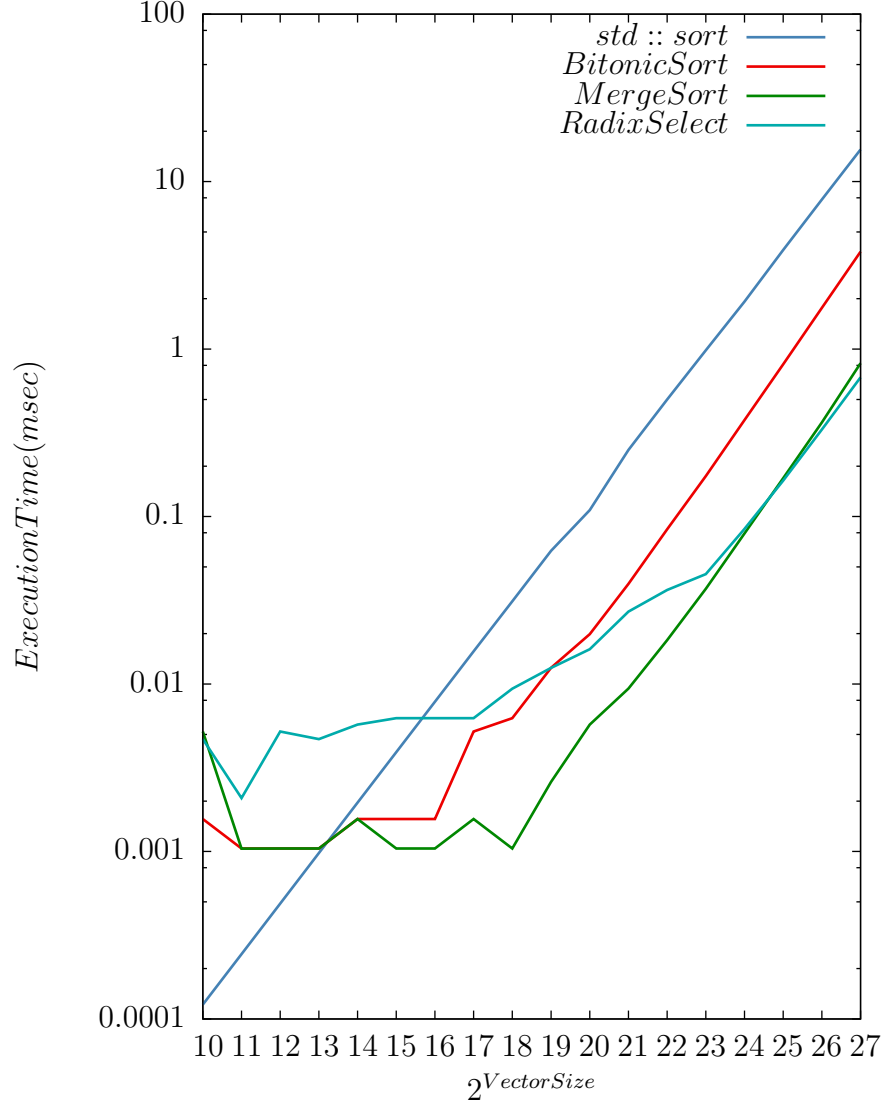


Figure 3.2: Selection Algorithm Performance for K=128. Test configuration GPU R9 390, CPU AMD A8-7600, AMD Catalyst version 15.20.

## Conclusion

The *Exhaustive Search* is a basic building block of the k-nearest neighbours algorithms. It is unavoidable if we need to obtain exact solution and is used to refine approximate methods results.

## Exact Clustering Methods

The clustering techniques are widely used to limit number of distance calculations needed for nearest neighbour search. Space partitioning by vector

dimensions is used by  $k - d$  tree method[40], random projection tree[39] provides a data structure splitting search space along random vectors. Metric trees such as ball tree[54], cover tree[27], nearest ancestor tree[?], random ball cover[31] provide solution for finding nearest neighbours in general metric space by organizing data points in groups around some centroids.

## k-d Tree

The  $k - d$  tree [40] is a balanced binary tree where each node represents a set of points  $P \in \langle p_1 \cdot p_n \rangle$  and its children are disjoint and almost equals sized subsets of  $P$ . The tree is constructed top-down, the initial set of points is split along the widest dimension or using other criteria until the predefined number of points in child nodes is reached. The tree can be constructed in  $O(n \log n)$  time and occupies linear space. Weber *etal*[67] have shown that  $k - d$  tree is outperformed by the exact calculation at moderate dimensionality (  $n > 10$  ) and results in full processing of the data points if the number of dimensions is large enough. The  $k - d$  tree requires  $N \gg 2^k$  points to be more effective than exhaustive search.

The listing of the  $k - d$  tree construction and nearest neighbours search pseudocode is shown in the Figure 3.3. The parallel  $k - d$  tree construction on GPU utilizes breadth-first approach[68][59] - the  $k - d$  tree is constructed top-down with the split criteria computed in parallel for all nodes at the specific level. The priority queue based nearest neighbours search using k-d trees as shown in Figure 3.3 does not benefit much from the GP GPU parallelism due to the branch divergence and irregular memory access patterns[42]. The  $k - d$  tree search approach presented by Gieske et. al focuses on parallel execution of nearest neighbour queries in a lazy fashion. The query points are accumulated in the leaf nodes of the kd-tree until enough of them is present and then processed as a batch. This solves an issue of the GPU underutilization and low performance if leaf nodes are processed sequentially for each example[42]. Other approach would be to compute distances to the leaf nodes split planes[68]

---

```

1  tree_node create_tree(pointList, level)
2  {
3      int dim = select_dim(pointList); // select split dimension according to
4      // pre-defined criteria, e.g. level mod total_dimensions
5      splitVal = select_split_value( pointList, dim); // select split value
6      // according to pre-defined criteria
7      // e.g. median value of point[dim]
8
9      left = {};
10     right = {}
11     for (point : pointList )
12     {
13         if (point[dim] > splitVal)
14             right += point;
15         else
16             left += point;
17     }
18     node = {
19         .location = splitVal,
20         .dim = dim,
21         .left = create_tree(left, level + 1),
22         .right = create_tree(right, level + 1)
23     };
24     return node;
25 }
26
27 void search(Heap nearest_neighbours, tree_node root, point p)
28 {
29     if (root.is_leaf())
30         nearest_neighbours.update(root);
31     else
32     {
33         split = root.location;
34         dim = root.dim;
35         if (p[dim] < split ) // search "closest" node
36             search(nearest_neighbours, root.left, p)
37         else
38             search(nearest_neighbours, root.right, p)
39
40         distance_to_split_plane = abs(split-p[dim]);
41         distance_to_point = abs(nearest_neighbours.furthest_point()[dim]-p[dim])
42         if (distance_to_point >= distance_to_split_plane) // outer radius of NN heap
43             intersects the split plane
44             {
45                 if (p[dim] < split )
46                     search(nearest_neighbours, root.right p)
47                 else
48                     search(nearest_neighbours, root.left, p)
49             }
50     }
51 }

```

---

Figure 3.3: k-d tree construction and NN-search pseudocode

to provide a short-list of the leaf nodes for  $k$ -nearest neighbours search.

## Random Projection Trees

The  $k - d$  tree provides an effective partitioning mechanism for low data dimensionality but suffers in higher dimensions[67]. Many machine learning problems that are expressed in high dimensional space has lower intrinsic dimension as shown in Figure 3.4. Random projection tree exploits this fact

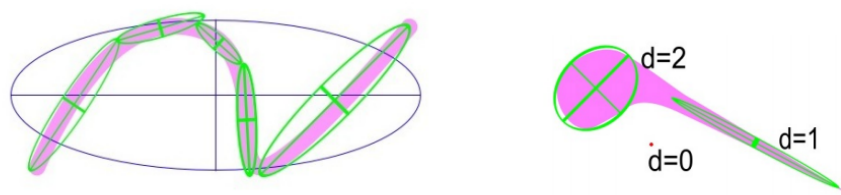


Figure 3.4: Distributions with low intrinsic dimension. The purple areas in these figures indicate regions in which the density of the data is significant, while the complementary white areas indicate areas where data density is very low. The left figure depicts data concentrated near a one-dimensional manifold. The ellipses represent mean+PCA approximations to subsets of the data. Our goal is to partition data into small diameter regions so that the data in each region is well-approximated by its mean+PCA. The right figure depicts a situation where the dimension of the data is variable. Some of the data lies close to a one-dimensional manifold, some of the data spans two dimensions, and some of the data (represented by the red dot) is concentrated around a single point (a zero-dimensional manifold). Reproduced from Learning the structure of manifolds using random projections by Freund Yoav et al.[39]

by splitting data along randomly chosen unit vectors as opposed to splitting along dimension axes in  $k - d$  tree method as shown in Figure 3.5[39]. The method performs a one dimensional random projection of the data points and splits them at the median of the projections.

The random projection tree split rules are presented in Figures 3.6, 3.7.

The efficient implementation of the Random Projection Tree depends on the ability to perform random projections with low computational complexity as it is both required for tree construction and queries.

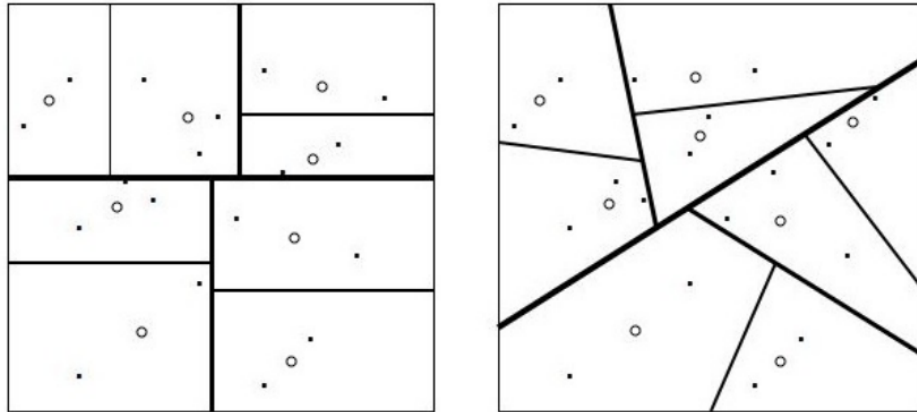


Figure 3.5: Left: Partitioning produced by k-d tree. Right: Partitioning produced by Random Projection Tree. Reproduced from Learning the structure of manifolds using random projections by Freund Yoav et al.[39]

---

```

1  tree_node random_tree_max(pointList, num_dimensions)
2  {
3      v = random_vector(num_dimensions);
4
5      x = pointList[ random() ];
6      y = max (distance( y in pointList, x ) );
7      sigma = uniform_random(-1;1) * 6 * distance(x,y) / sqrt(num_dimensions);
8      split = median ( dot(v, x in pointList)+ sigma ) ;
9      left = {}
10     right = {}
11     for (x in pointList)
12     {
13         if (dot(v,x) <= split)
14             left += x;
15         else
16             right +=x;
17     }
18     node = {
19         .vector = v,
20         .split = split,
21         .left = create_tree(left, num_dimensions),
22         .right = create_tree(right, num_dimensions)
23     };
24     return node;
25 }

```

---

Figure 3.6: Random Projection Tree Pseudocode - Random Tree Max [35]

---

```

1
2  tree_node random_tree_mid(pointList, num_dimensions, c)
3  {
4      diameter = max( distance(x in pointList, y in pointList));
5      avg_diameter = mean(distance(x in pointList, y in pointList));
6      if ( diameter <= c* avg_diameter)
7      {
8          v = random_vector(num_dimensions);
9          split = median( dot(x in pointList, v) );
10         left = {}
11         right = {}
12         for (x in pointList)
13         {
14             if (dot(v,x) <= split)
15                 left += x;
16             else
17                 right +=x;
18         }
19         node = {
20             .rule_type = dotproduct
21             .vector = v,
22             .split = split,
23             .left = create_tree(left, num_dimensions),
24             .right = create_tree(right, num_dimensions)
25         };
26         return node;
27     }
28     else
29     {
30         meanPoint = mean(x in pointList)
31         split = median( distance(x in pointList, meanPoint));
32         left = {}
33         right = {}
34         for (x in pointList)
35         {
36             if (distance(x, meanPoint) <= split)
37                 left += x;
38             else
39                 right +=x;
40         }
41         node = {
42             .rule_type = distance
43             .mean = meanPoint,
44             .split = split,
45             .left = create_tree(left, num_dimensions),
46             .right = create_tree(right, num_dimensions)
47         };
48         return node;
49     }
50 }
51 }

```

---

Figure 3.7: Random Projection Tree Pseudocode - Random Tree Median[35]

**Random Projection** Seminal paper by Johnson and Lindenstrauss[45] established that for euclidian spaces any  $x \in \mathbb{R}^n$  can be embedded into  $\mathbb{R}^k$  with  $k = O(\log n / \epsilon^2)$  by projecting  $x$  in  $\mathbb{R}^k$  using projection  $k \times n$  matrix  $\Phi$  without distorting inter-point distances by more than  $(1 \pm \epsilon)$  and  $k \geq O(\log n)$ . Johnson and Lindenstrauss[45] has shown that Johnson-Lindenstrauss condition holds for matrices with following properties: “S”pherical symmetry - For any orthogonal matrix  $A \in O(d)$ ,  $\phi A$  and  $\phi$  have the same distribution. Orthogonality - rows are orthogonal to each other Normality - the rows are unit-length vectors [21]

The lower bound of  $k$  was refined by in several papers[38][36][44][20] and with Dasgupta and Gupta[36] proving it to be  $k \geq 4(\epsilon^2/2 - \epsilon^3/3)^{-1} \ln n$  for  $\epsilon \in (0, 1)$ . For high  $n$  this bound will still be too large to effectively employ low dimensionality search methods such as  $k - d$  tree. An alternative would be to utilize very low dimensional space and then use disjunction to find desired result. This approach is essentially an iterative random projection tree search where the dataset is split along leaf nodes.

The efficient implementation of the random projection-based algorithms requires a simple approach to construct  $\phi$  and a way to compute projection faster than naive multiplication of data point by  $k \times n$  matrix. Achlioptas[20] achieved relatively sparse transformation matrix for random projection by proving that Johnson-Lindenstrauss condition holds if elements of the projection matrix are chosen independently according to the following distribution:

$$\begin{cases} +(n/3)^{-1/2}, P = 1/6 \\ 0, P = 2/3 \\ -(n/3)^{-1/2}, P = 1/6 \end{cases}$$

This method provides a 3-fold speedup over originally proposed[45] since 2/3 of the transformation matrix elements are zero. Nir Ailon and Edo Liberty[22] have developed an almost optimal random projection transformation with runtime of  $O(n \log n)$  as opposed to  $O(kn)$  of the naive implementation. The



main idea of the method is the application of the Heisenberg principle in its signal processing interpretation that both signal and its spectrum can not be both sharply localized. *TODO:finish description of 2013 method - multiply by  $+1$  diagonal matrix, apply FFT and normalization constant and then randomly select  $k$  results to obtain projection. Reference implementation: <https://github.com/gabobert/fast-jlt/tree/master/fjlt>*

This implementation is well suited for GPU implementation as it consists of FFT followed by element-wise operation. The last step (select random  $D$  elements) introduces irregular memory access that can not be worked around unless multiple transformations are performed in parallel. Figure 3.8 shows comparative performance of dense matrix multiplication for random projection and Fast Johnson-Lindenstrauss transform. For the selected hardware configuration the latter starts to outperform matrix multiplication starting from  $N \geq 16384$ . It should be noted that FLJT has lower memory requirements than  $O(kd)$  as it does not require to store dense transformation matrix and thus capable of projecting higher dimensional data on the same hardware.

## Approximate Clustering Methods

The nearest neighbours search methods in high dimensional space provides little benefit over exhaustive search where an exact distance is computed to each point in the database[67][25]. The approximate methods provide means to overcome this limitation by solving the problem of finding neighbours whose distance from the query point are at most  $c > 1$  times greater than distance to the closest neighbour. The approximate solution can be used to find exact one by computing distance to each approximate nearest neighbour and choosing closest ones. Modern approximate method use dimensionality reducing techniques such as random projection[55] and data set ordering using space filling curves[55][46][47] to improve query performance.

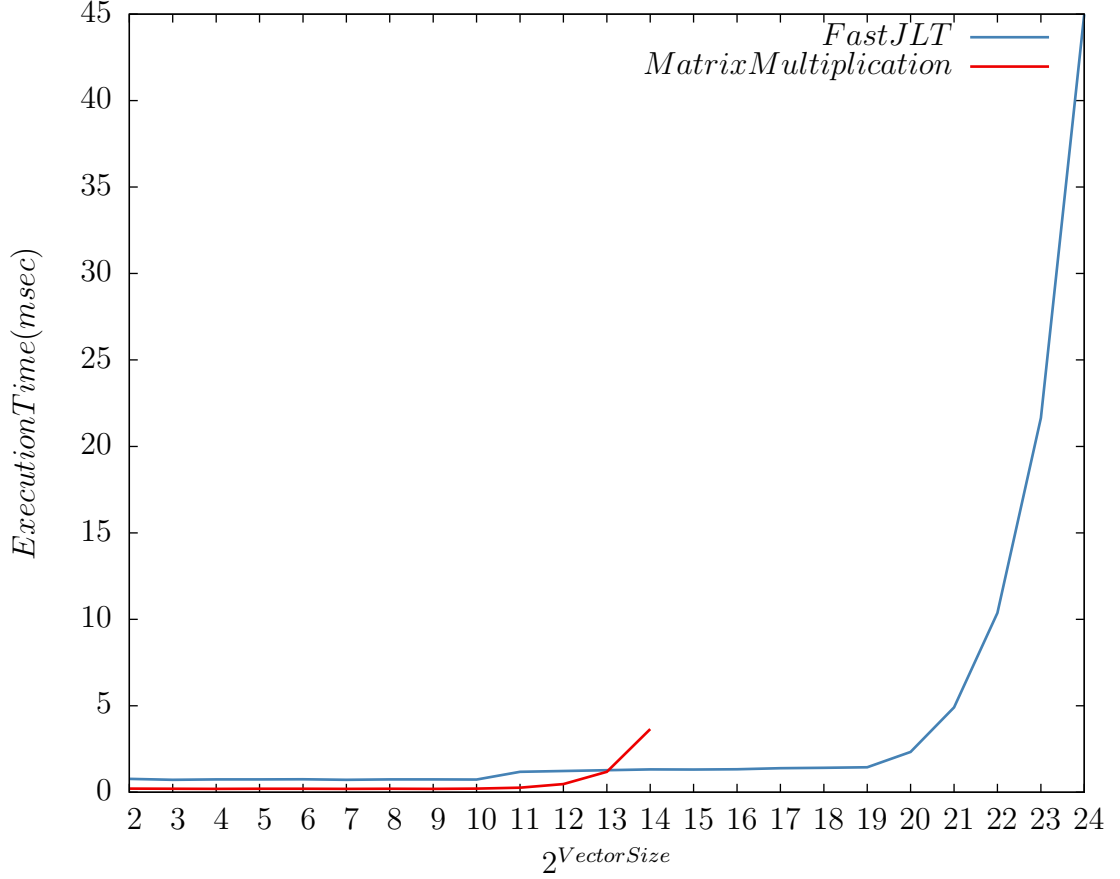


Figure 3.8: Fast Johnson-Lindenstrauss transform[22] vs. sparse matrix implementation[20] using ViennaCL. Test configuration GPU R9 390, CPU AMD A8-7600, AMD Catalyst version 15.20.

## Locality Sensivity Hashing

Locality Sensivity Hashing[44] is a method that capitalizes on the idea that exist such hash functions  $h(x), x \in \mathbb{R}^d$  that for points  $p, q \in \mathbb{R}^d$ , radius  $R$  and approximation constant  $c$

$$\begin{cases} \|p - q\| \leq R, P[h(p) = h(q)] \geq P_1 \\ \|p - q\| \geq cR, P[h(p) = h(q)] \leq P_2 \end{cases}$$

where probability  $P_1 > P_2$ . The LSH algorithm uses a concatenation of  $M \ll d$  such functions to increase difference between  $P_1$  and  $P_2$ [44]. Initially it was proposed to use Hamming distance as this function satisfies required properties[44]. Later it was shown that other families of hash functions

such as  $l_p$  distance[37], Jaccard coefficient [29][30], angular distance(random projection)[32] are locally sensitive. The algorithms selects  $L$  concatenations of the hash functions and uses them to transform input dataset points  $v \in \mathbb{R}^d$  into lattice space  $\mathbb{Z}^M$  storing them as  $L$  hash tables. The exact query is performed by concatenating contents of the  $L$  bins corresponding to the hash codes of the query and computing exact distance. The approximation is obtained by stopping as soon as  $k$  points in  $cR$  distance from the query point is found. The method is GP GPU friendly as hash codes of the data points can be computed in massively parallel manner. The state of art GP GPU hash maps use *cockoo hashing*[24] a robust data structure allowing constant time retrieval and eliminate hash collisions that lead to the branch divergence due to the need to iterate over items in the hash bucket but require full hash map rebuild to resolve a collision.

## Space Filling Curves

The space filling curves[57] are curves that traverse all points of n-dimensional space in a given region providing a mapping from n-dimensional to 1-dimensional space. The GP GPU nearest neighbours algorithms[47][46][55] utilize z-order curve introduced by G. Morton in 1966 - an ordered list of numbers composed by interleaving bits of instance attributes[?]. This curve is used due to the fact that mapping can be constructed in  $O(d)$  time and is easily implemented on GPU. The sample z-order curve is shown in Figure 3.9. The z-order curve mostly preserves data locality - points that are close in the n-dimensional space are also close together along the curve, but as shown in Figure 3.9 the z-order curve has jumps and to compensate for them existing GP GPU algorithms generate several curves from the input data shifted several times by some random vector[47][46] to move the points into its locality-preserving regions. Shift search method by Li et al.[46] experimentally quantifies the shift value.

Sieranoja S.[60] proposed a z-order lookup table mapping algorithm for ar-

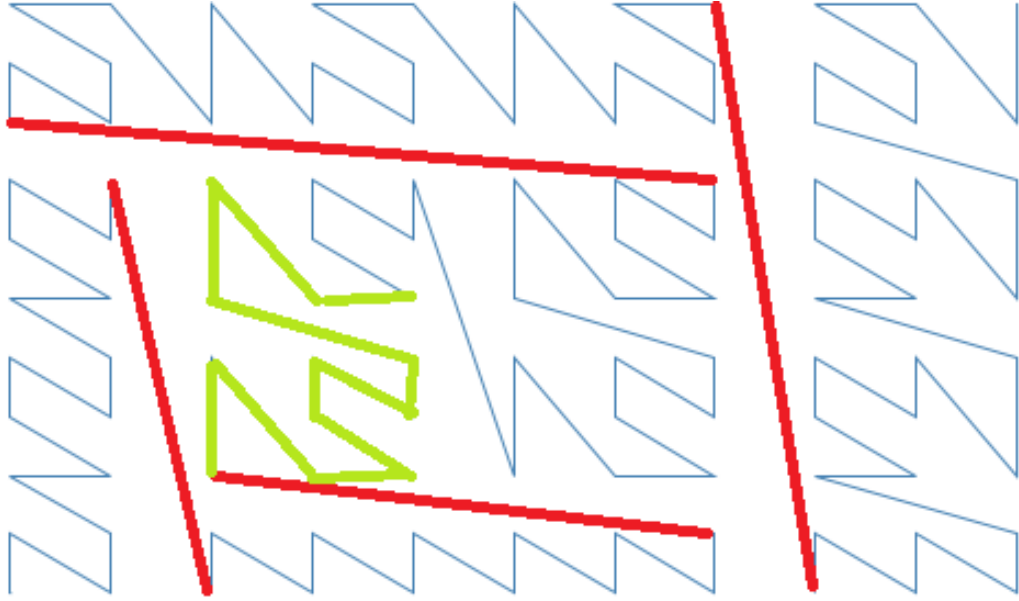


Figure 3.9: Z-Order Curve. Red lines highlight some region jumps. Green shows locality-preserving region.

bitrary number of dimensions. It can be translated into GPU implementation with minimal changes.

## HSA-based k-nearest neighbours

The HSA architecture opens new possibilities for GP GPU acceleration of the nearest neighbours search by embedding parallel primitives such as FJLT and exhaustive search into existing algorithms without redesigning them to conform to the GPU architecture.

**k-d tree queries** The k-d tree queries require all or nothing approach[68][42] - the algorithm design and data structures should be implemented in GP GPU specific manner to obtain higher throughput and expense of the latency. HSA allows to insert *exhaustive search* parallel primitive to search the tree leaves in an efficient manner. The discrete GPU would not achieve same computing node/speedup ratio due to the irregular memory access to the instance data. *TODO: make a figure* For instance a test performed in MOA[28] *EvaluatePeriodicHeldOutTest* -  $l(gpu.kdtree.TreeKNN - w16384 - nK DTree) -$

*s*generators.*RandomRBFGenerator* yielded following results (HSA Spectre device/CPU = 4.175 speedup, OpenCL Spectre device = 3.34 speedup, OpenCL R390 device = 5.0 speedup).

**Random Tree Construction and Queries** *TODO: phrasing - construction and queries - we use existing DFS and embed FJLT/radius calculation*  
 For instance it depends on the calculation of the node diameter for the *rp-mean* split criteria. The diameter calculation is a computationally expensive operation and it is often approximated by the iterative method that picks an anchor point, finds point furthest from it and then repeats the process until it converges[?]. For GPU acceleration it requires multiple Host-GPU transfers to evaluate the stop criteria and pick next anchor point that would hinder the method performance.

**Z-Order-based queries** The significant problem in z-order query evaluation is a maintenance of the candidate lists for large  $k$ [46]. The cost of GPU-host transfer in this case is prohibitive and Li et al[46] work around it by executing multiple queries at once so that it is more beneficial to perform sort as opposed to search. The HSA implementation may keep the candidate list on CPU and perform n-ary GPU searches thus reducing query latency.

The approximate z-order based method can utilize random projections to shorten morton code length while preserving the relative distances. *TODO phrasing: 2-3 sentences - zero-copy, lower latency, best of both worlds*

# Chapter 4

## Stochastic Gradient Descent

### Problem Statement

The stochastic gradient descent is a iterative optimization method which approximates a gradient of the function by a gradient of a single example. The stochastic gradient descent is widely in many machine learning tasks and is a standard algorithm used in training neural networks.

The parallel implementations of the algorithm use either assumption that data in the training batch is loosely coupled and it is possible to loose some of the individual updates thus the batch can processed in parallel - Hogwild! algorithm [52] or extract independent data blocks from the traing batch - DSGD[41], FPSGD[33] or arbitrary divide the examples into parts processed in parallel and approximate the direction of the gradient descent [48] using weight update vectors produced by them.

### Algorithm Implementations

#### Hogwild-based

This GP-GPU implementation for sparse instances uses Hogwild[52] approach to training. A sparse matrix containing the training batch is constructed and the training is performed on the assumption that the data race between

individual updates to the same weight can be ignored.

The algorithm is implemented as MOA[28] classifier with the native ViennaCL[?]-based part performing the GPU calculations.

The training batch is represented as a sparse matrix in Compressed Row Storage format[26], that is all non-zero elements of the matrix are stored sequentially in the elements vector in row major format, the row information vector contains indices of the first and last elements of each matrix row, and columns vector contains column indices of the matrix elements.

**OpenCL implementation** Figure 2.1 shows the training process - the classifier training and CPU-GPU data transfer are performed in parallel.

OpenCL implementation structure is shown in Figure 4.1. The device-side enqueue is used to launch kernels for individual instance update to simplify implementation. The device-side enqueue kernel call latency is  $2x$  higher than that of the host-side kernel enqueue (e.g.  $1.68 \mu\text{sec}$   $0.91 \mu\text{sec}$  on the Spectre device) but its cost is hidden by the row processing time as the parent kernel would not return until all the child kernels has finished execution and `CLK_ENQUEUE_FLAGS_KERNEL_NOWAIT` flag is used to inform OpenCL runtime to start execution immediatly while parent kernel is still queueing row kernel. The atomic update operation is implemented using

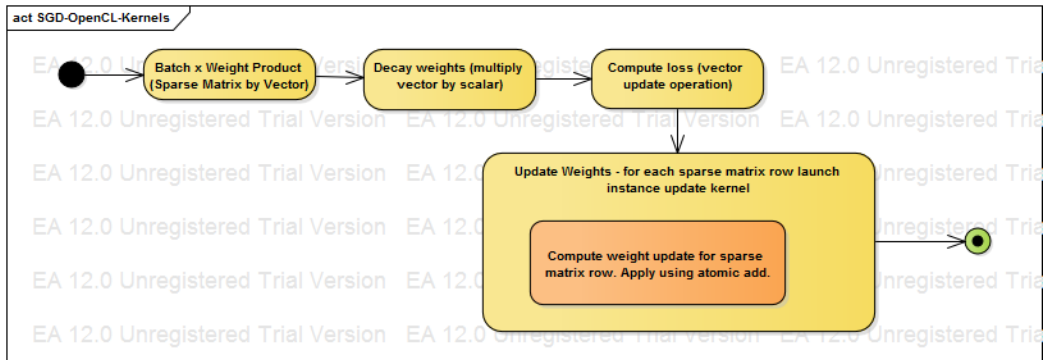


Figure 4.1: Kernel calls for SGD classifier training

*compare – and – swap* primitive of OpenCL. It should be noted that the loop condition should be explicitly declared *volatile* to force runtime to re-evalutate the *compareandswap* expression.

**HSA implementation** The HSA implementation shares Java interface most of the native implementation with OpenCL SGD. The notable differences are:

- Memory management. The HSA implementation constructs ViennaCL container classes directly from the host pointers. The memory updates are fine-grained and global memory update done by kernel is immediately visible by the host as opposed to the coarse-grained updates of OpenCL implementation.
- Device enqueue. The device enqueue is a largely untested functionality in the current HSA runtime and since the sparse matrix row information pointer containing indexes of row bounds is directly accessible by the CPU the individual row update kernels are scheduled from the host.

**Datatype Selection** The implementation can use either *double* or *float* precision numbers for the calculations.



# Chapter 5

## Experimental Results

### k-Nearest Neighbours

#### kNN Naive implementation

The first version of k-NN algorithm used Java implementation with JavaCL library. The results in Figure 5.1 provide overview of the achieved speedups.

#### Stochastic Gradient Descent

The SGD implementation training speedup for sparse instances with the double data type is presented in the Figures 5.2, 5.3. The CPU sampling profiling showed that most of the time is spent inside buffer commit function responsible for copying data from WEKA instance class into the sparse matrix. As the GPU implementation uses batching to achieve training speedup the latency is  $5-10x$  worse than CPU. The profiling of the sample run on a Spectre device of OpenCL algorithm implementation with 1024 non-null attributes in an instance and 8192 instances in a batch shows that only 32% is spent training the classifier, rest is spent in the CPU-GPU data transfer.

The sparse matrix OpenCL SGD implementation is bounded by the memory copy operation as shown by the profiling data and provides a limited speedup.

*TODO* Provide zero-copy (HSA) speedups *TODO* Provide float speedups

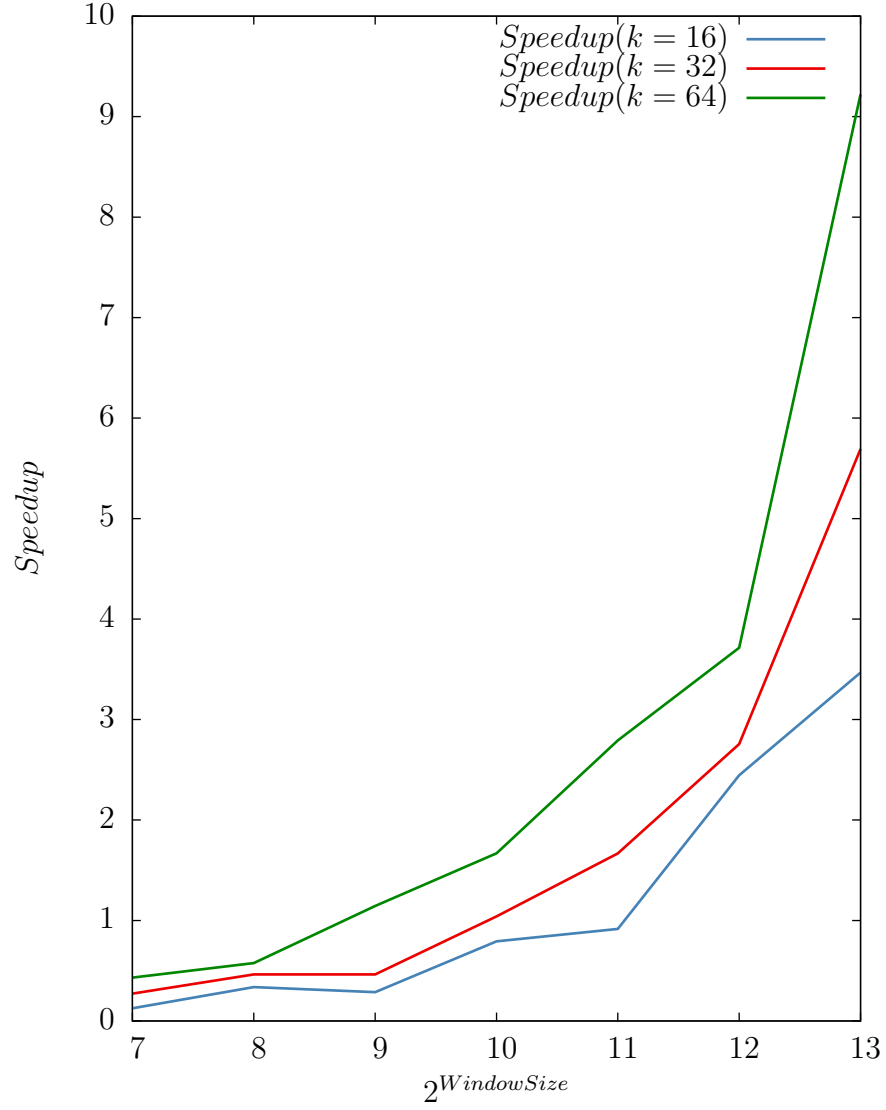


Figure 5.1: Naive KNN implementation (Radeon Mobility HD5730)

and impact on the accuracy of the algorithm for the known data sets.

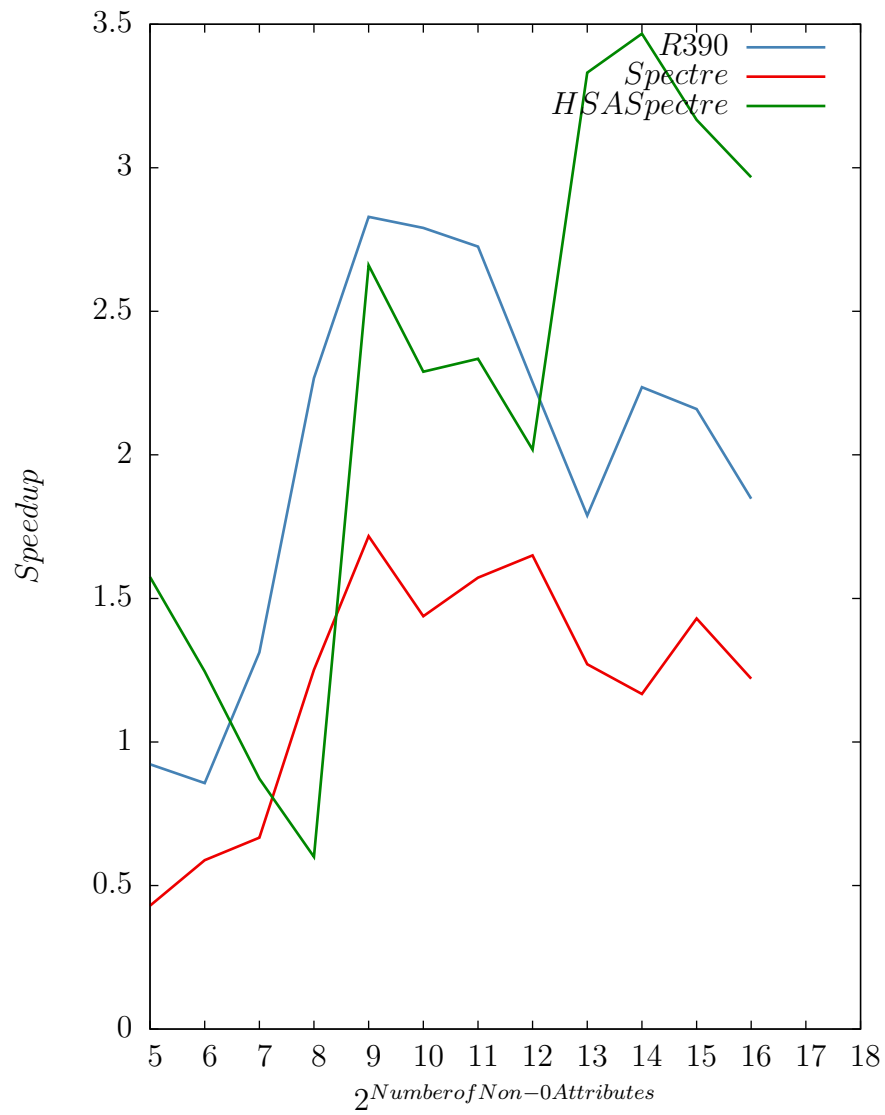


Figure 5.2: Stochastic Gradient Descent Training Speedup (AMD R9 390, Spectre vs MOA implementation on AMD A8-7600)

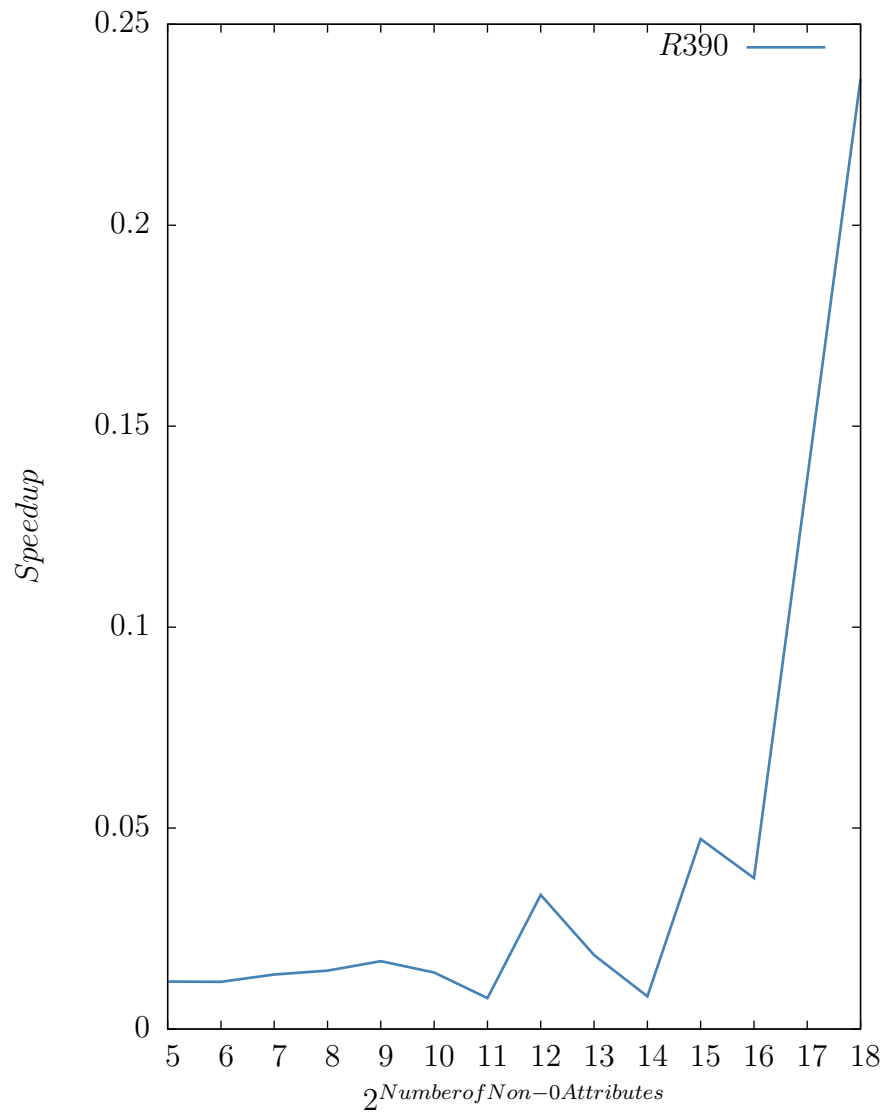


Figure 5.3: Stochastic Gradient Descent Training Latency (AMD R9 390 vs MOA implementation on AMD A8-7600)

# Chapter 6

## Conclusions and Future Work

*TODO*

# References

- [1] aparapi - api for data parallel java. allows suitable code to be executed on gpu via opencl. <https://code.google.com/p/aparapi/>.
- [2] Bolt c++ template library. <http://developer.amd.com/tools-and-sdks/opencl-zone/bolt-c-template-library>.
- [3] C++ amp overview. <https://msdn.microsoft.com/en-us/library/hh265136.aspx>.
- [4] clmath - amd. <http://developer.amd.com/tools-and-sdks/opencl-zone/amd-accelerated-parallel-processing-math-libraries/>.
- [5] Compute shader overview. <https://msdn.microsoft.com/en-us/library/windows/desktop/ff476331%28v=vs.85%29.aspx>.
- [6] cublas. <https://developer.nvidia.com/cuBLAS>.
- [7] Hsafoundation. <https://github.com/HSAFoundation>.
- [8] Hsafoundation/cloc. <https://github.com/HSAFoundation/CLOC>.
- [9] Java se 7 java native interface-related apis and developer guides. <http://docs.oracle.com/javase/7/docs/technotes/guides/jni/>.
- [10] java.util.stream (java platform se 8). <http://docs.oracle.com/javase/8/docs/api/java/util/stream/package-summary.html>.
- [11] Khronos opencl registry. <https://www.khronos.org/registry/cl/>.
- [12] Nvidias next generation cuda(tm) compute architecture:fermi. [http://www.nvidia.com/content/PDF/fermi\\_white\\_papers/NVIDIA\\_Fermi\\_Compute\\_Architecture\\_Whitepaper.pdf](http://www.nvidia.com/content/PDF/fermi_white_papers/NVIDIA_Fermi_Compute_Architecture_Whitepaper.pdf).
- [13] Openjdk: Project sumatra. <http://openjdk.java.net/projects/sumatra/>.
- [14] Openmp.org. <http://openmp.org/wp/>.

- 
- [15] Ptx isa :: Cuda toolkit documentation. <http://docs.nvidia.com/cuda/parallel-thread-execution/index.html>.
  - [16] Renderscript—android developers. <http://developer.android.com/guide/topics/renderscript/compute.html>.
  - [17] Single instruction, multiple threads. [http://en.wikipedia.org/wiki/Single\\_instruction,\\_multiple\\_threads#cite\\_note-spp-1](http://en.wikipedia.org/wiki/Single_instruction,_multiple_threads#cite_note-spp-1).
  - [18] Spir - the first open standard intermediate language for parallel compute and graphics. <https://www.khronos.org/spir>.
  - [19] Hsa platform system architecture specification. <http://www.hsafoundation.com/?ddownload=4944>, 2014.
  - [20] Dimitris Achlioptas. Database-friendly random projections: Johnson-lindenstrauss with binary coins. *J. Comput. Syst. Sci.*, 66(4):671–687, June 2003.
  - [21] Nir Ailon and Bernard Chazelle. The fast johnson-lindenstrauss transform and approximate nearest neighbors. *SIAM Journal on Computing*, 39(1):302–322, 2009.
  - [22] Nir Ailon and Edo Liberty. An almost optimal unrestricted fast johnson-lindenstrauss transform. *ACM Transactions on Algorithms (TALG)*, 9(3):21, 2013.
  - [23] Tolu Alabi, Jeffrey D. Blanchard, Bradley Gordon, and Russel Steinbach. Fast k-selection algorithms for graphics processing units. *J. Exp. Algorithms*, 17:4.2:4.1–4.2:4.29, October 2012.
  - [24] Dan Anthony Feliciano Alcantara. *Efficient hash tables on the gpu*. University of California at Davis, 2011.
  - [25] Alexandr Andoni and Piotr Indyk. Near-optimal hashing algorithms for approximate nearest neighbor in high dimensions. *Commun. ACM*, 51(1):117–122, January 2008.
  - [26] Richard Barrett, Michael Berry, Tony F. Chan, James Demmel, June M. Donato, Jack Dongarra, Victor Eijkhout, Roldan Pozo, Charles Romine, and Henk Van Der Vorst. Templates for the solution of linear systems: Building blocks for iterative methods, 1994.
  - [27] Alina Beygelzimer, Sham Kakade, and John Langford. Cover trees for nearest neighbor. In *Proceedings of the 23rd international conference on Machine learning*, pages 97–104. ACM, 2006.

- 
- [28] Albert Bifet, Geoff Holmes, Richard Kirkby, and Bernhard Pfahringer. Moa: Massive online analysis. *J. Mach. Learn. Res.*, 11:1601–1604, August 2010.
- [29] Andrei Z. Broder, Steven C. Glassman, Mark S. Manasse, and Geoffrey Zweig. Syntactic clustering of the web. In *Selected Papers from the Sixth International Conference on World Wide Web*, pages 1157–1166, Essex, UK, 1997. Elsevier Science Publishers Ltd.
- [30] Andrei Z. Broder, Steven C. Glassman, Mark S. Manasse, and Geoffrey Zweig. Syntactic clustering of the web. *Comput. Netw. ISDN Syst.*, 29(8-13):1157–1166, September 1997.
- [31] L. Cayton. Accelerating nearest neighbor search on manycore systems. In *Parallel Distributed Processing Symposium (IPDPS), 2012 IEEE 26th International*, pages 402–413, May 2012.
- [32] Moses S. Charikar. Similarity estimation techniques from rounding algorithms. In *Proceedings of the Thiry-fourth Annual ACM Symposium on Theory of Computing*, STOC '02, pages 380–388, New York, NY, USA, 2002. ACM.
- [33] Wei-Sheng Chin, Yong Zhuang, Yu-Chin Juan, and Chih-Jen Lin. A fast parallel stochastic gradient method for matrix factorization in shared memory systems. *ACM Trans. Intell. Syst. Technol.*, 6(1):2:1–2:24, March 2015.
- [34] T. Cover and P. Hart. Nearest neighbor pattern classification. *IEEE Trans. Inf. Theor.*, 13(1):21–27, September 2006.
- [35] Sanjoy Dasgupta and Yoav Freund. Random projection trees and low dimensional manifolds. In *Proceedings of the Fortieth Annual ACM Symposium on Theory of Computing*, STOC '08, pages 537–546, New York, NY, USA, 2008. ACM.
- [36] Sanjoy Dasgupta and Anupam Gupta. An elementary proof of a theorem of johnson and lindenstrauss. *Random Struct. Algorithms*, 22(1):60–65, January 2003.
- [37] Mayur Datar, Nicole Immorlica, Piotr Indyk, and Vahab S. Mirrokni. Locality-sensitive hashing scheme based on p-stable distributions. In *Proceedings of the Twentieth Annual Symposium on Computational Geometry*, SCG '04, pages 253–262, New York, NY, USA, 2004. ACM.



- 
- [38] Peter Frankl and Hiroshi Maehara. The johnson-lindenstrauss lemma and the sphericity of some graphs. *Journal of Combinatorial Theory, Series B*, 44(3):355–362, 1988.
  - [39] Yoav Freund, Sanjoy Dasgupta, Mayank Kabra, and Nakul Verma. Learning the structure of manifolds using random projections. In *Advances in Neural Information Processing Systems*, volume 20, 2007.
  - [40] Jerome H. Friedman, Jon Louis Bentley, and Raphael Ari Finkel. An algorithm for finding best matches in logarithmic expected time. *ACM Trans. Math. Softw.*, 3(3):209–226, September 1977.
  - [41] Rainer Gemulla, Erik Nijkamp, Peter J. Haas, and Yannis Sismanis. Large-scale matrix factorization with distributed stochastic gradient descent. In *Proceedings of the 17th ACM SIGKDD International Conference on Knowledge Discovery and Data Mining*, KDD '11, pages 69–77, New York, NY, USA, 2011. ACM.
  - [42] Fabian Gieseke, Justin Heineremann, Cosmin Oancea, and Christian Igel. Buffer kd trees: Processing massive nearest neighbor queries on gpus. In *Proceedings of The 31st International Conference on Machine Learning*, page 172180, 2014.
  - [43] Suyog Gupta, Ankur Agrawal, Kailash Gopalakrishnan, and Pritish Narayanan. Deep learning with limited numerical precision. *CoRR*, abs/1502.02551, 2015.
  - [44] Piotr Indyk and Rajeev Motwani. Approximate nearest neighbors: Towards removing the curse of dimensionality. In *Proceedings of the Thirtieth Annual ACM Symposium on Theory of Computing*, STOC '98, pages 604–613, New York, NY, USA, 1998. ACM.
  - [45] William Johnson and Joram Lindenstrauss. Extensions of Lipschitz mappings into a Hilbert space. In *Conference in modern analysis and probability (New Haven, Conn., 1982)*, volume 26 of *Contemporary Mathematics*, pages 189–206. American Mathematical Society, 1984.
  - [46] Shengren Li, Lance Simons, Jagadeesh Bhaskar Pakaravoor, Fatemeh Abbasi-nejad, John D Owens, and Nina Amenta. kann on the gpu with shifted sorting. In *Proceedings of the Fourth ACM SIGGRAPH/Eurographics conference on High-Performance Graphics*, pages 39–47. Eurographics Association, 2012.
  - [47] Michael D Lieberman, Jagan Sankaranarayanan, and Hanan Samet. A fast similarity join algorithm using graphics processing units. In *Data*

- Engineering, 2008. ICDE 2008. IEEE 24th International Conference on*, pages 1111–1120. IEEE, 2008.
- [48] Dhruv Mahajan, S. Sathiya Keerthi, S. Sundararajan, and Léon Bottou. A parallel SGD method with strong convergence. *CoRR*, abs/1311.0636, 2013.
  - [49] Luc Maranget, Susmit Sarkar, and Peter Sewell. A tutorial introduction to the arm and power relaxed memory models, 2012.
  - [50] Jatin Chhugani Anthony D. Nguyen Victor W. Lee Daehyun Kim Pradeep Dubey Nadathur Satish, Changkyu Kim. Fast sort on cpus,gpus and intel mic architectures. <http://www.intel.com/content/dam/www/public/us/en/documents/technology-briefs/intel-labs-radix-sort-mic-report.pdf>.
  - [51] John Nickolls, Ian Buck, Michael Garland, and Kevin Skadron. Scalable parallel programming with cuda. *Queue*, 6(2):40–53, March 2008.
  - [52] Feng Niu, Benjamin Recht, Christopher R, and Stephen J. Wright. Hogwild: A lock-free approach to parallelizing stochastic gradient descent. In *In NIPS*, 2011.
  - [53] C. Nugteren. Improving the programmability of gpu architectures, 2014.
  - [54] Stephen Malvern Omohundro. *Five balltree construction algorithms*. International Computer Science Institute Berkeley, 1989.
  - [55] Jia Pan and Dinesh Manocha. Bi-level locality sensitive hashing for k-nearest neighbor computation. In *Proceedings of the 2012 IEEE 28th International Conference on Data Engineering, ICDE '12*, pages 378–389, Washington, DC, USA, 2012. IEEE Computer Society.
  - [56] P.C. Pratt-Szeliga, J.W. Fawcett, and R.D. Welch. Rootbeer: Seamlessly using gpus from java. In *High Performance Computing and Communication 2012 IEEE 9th International Conference on Embedded Software and Systems (HPCC-ICESS), 2012 IEEE 14th International Conference on*, pages 375–380, June 2012.
  - [57] Hans Sagan. Space-filling curves, 1994.
  - [58] D. Sculley, Daniel Golovin, and Michael Young. Big learning with little ram. <http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.298.2337&rep=rep1&type=pdf>.

- 
- [59] Maxim Shevtsov, Alexei Soupikov, and Er Kapustin. Highly parallel fast kd-tree construction for interactive ray tracing of dynamic scenes.
- [60] Sami Sieranoja. High dimensional knn-graph construction using space filling curves. <http://urn.fi/urn:nbn:fi:uef-20150325>, 2015.
- [61] N. Sismanis, N. Pitsianis, and Xiaobai Sun. Parallel search of k-nearest neighbors with synchronous operations. In *High Performance Extreme Computing (HPEC), 2012 IEEE Conference on*, pages 1–6, Sept 2012.
- [62] T. Aila S.Laine, T. Karras. Megakernels considered harmful: Wavefront path tracing on gpus. [https://research.nvidia.com/sites/default/files/publications/laine2013hpg\\_paper.pdf](https://research.nvidia.com/sites/default/files/publications/laine2013hpg_paper.pdf).
- [63] Hans Henrik Brandenborg Sørensen. High-performance matrix-vector multiplication on the gpu. In *Proceedings of the 2011 International Conference on Parallel Processing, Euro-Par’11*, pages 377–386, Berlin, Heidelberg, 2012. Springer-Verlag.
- [64] John E Stone, David Gohara, and Guochun Shi. Opencl: A parallel programming standard for heterogeneous computing systems. *Computing in science & engineering*, 12(1-3):66–73, 2010.
- [65] Alan Tatourian. Nvidia gpu architecture and cuda programming environment. <http://tatourian.com/2013/09/03/nvidia-gpu-architecture-cuda-programming-environment/>.
- [66] Philippe Tillet, Karl Rupp, Siegfried Selberherr, and Chin-Teng Lin. Towards performance-portable, scalable, and convenient linear algebra. In *Presented as part of the 5th USENIX Workshop on Hot Topics in Parallelism*, Berkeley, CA, 2013. USENIX.
- [67] Roger Weber, Hans-Jörg Schek, and Stephen Blott. A quantitative analysis and performance study for similarity-search methods in high-dimensional spaces. In *Proceedings of the 24rd International Conference on Very Large Data Bases, VLDB ’98*, pages 194–205, San Francisco, CA, USA, 1998. Morgan Kaufmann Publishers Inc.
- [68] Kun Zhou, Qiming Hou, Rui Wang, and Baining Guo. Real-time kd-tree construction on graphics hardware. *ACM Trans. Graph.*, 27(5):126:1–126:11, December 2008.