1. Description

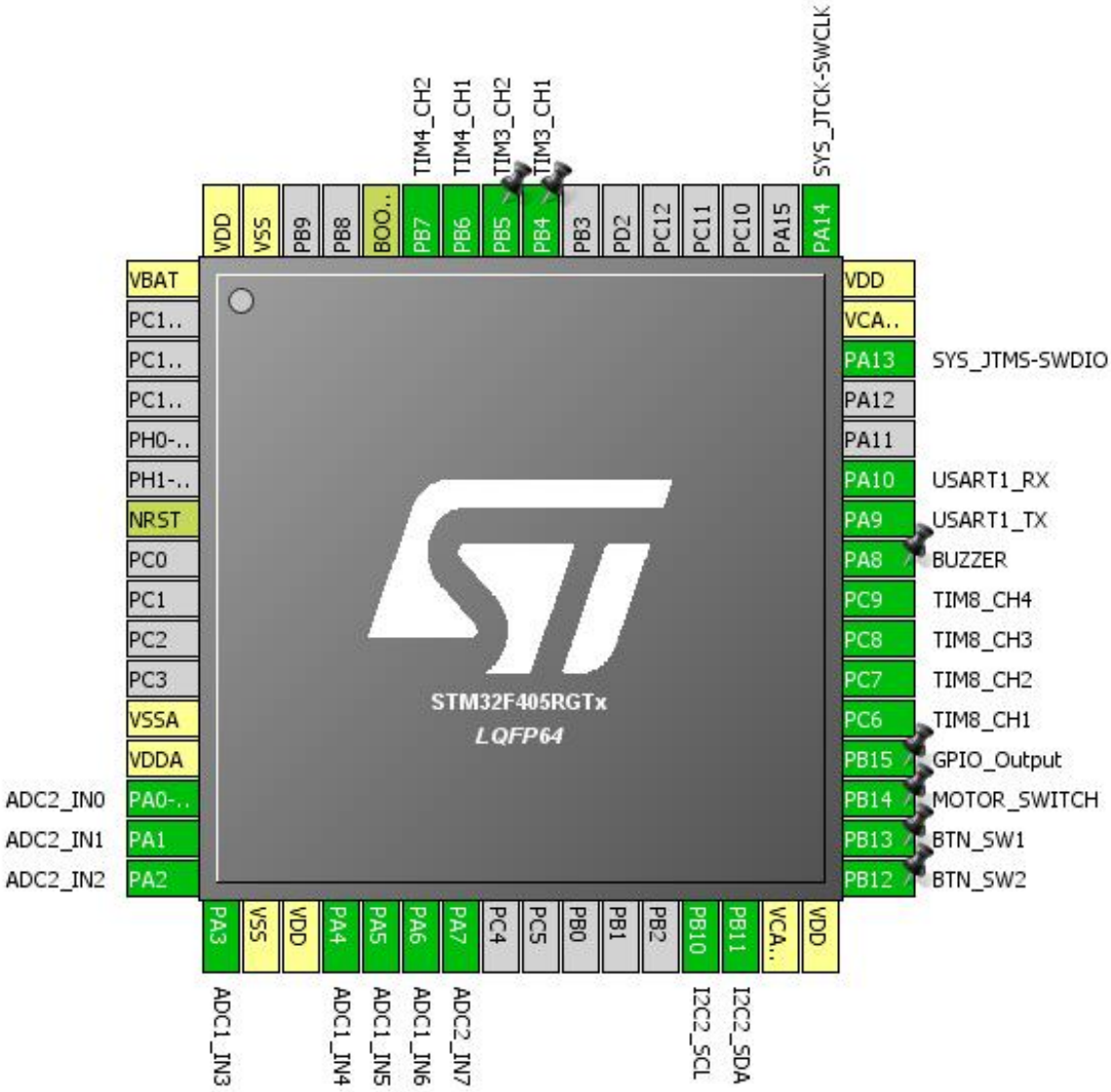
1.1. Project

Project Name	NYP
Board Name	NYP
Generated with:	STM32CubeMX 4.12.0
Date	02/04/2016

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



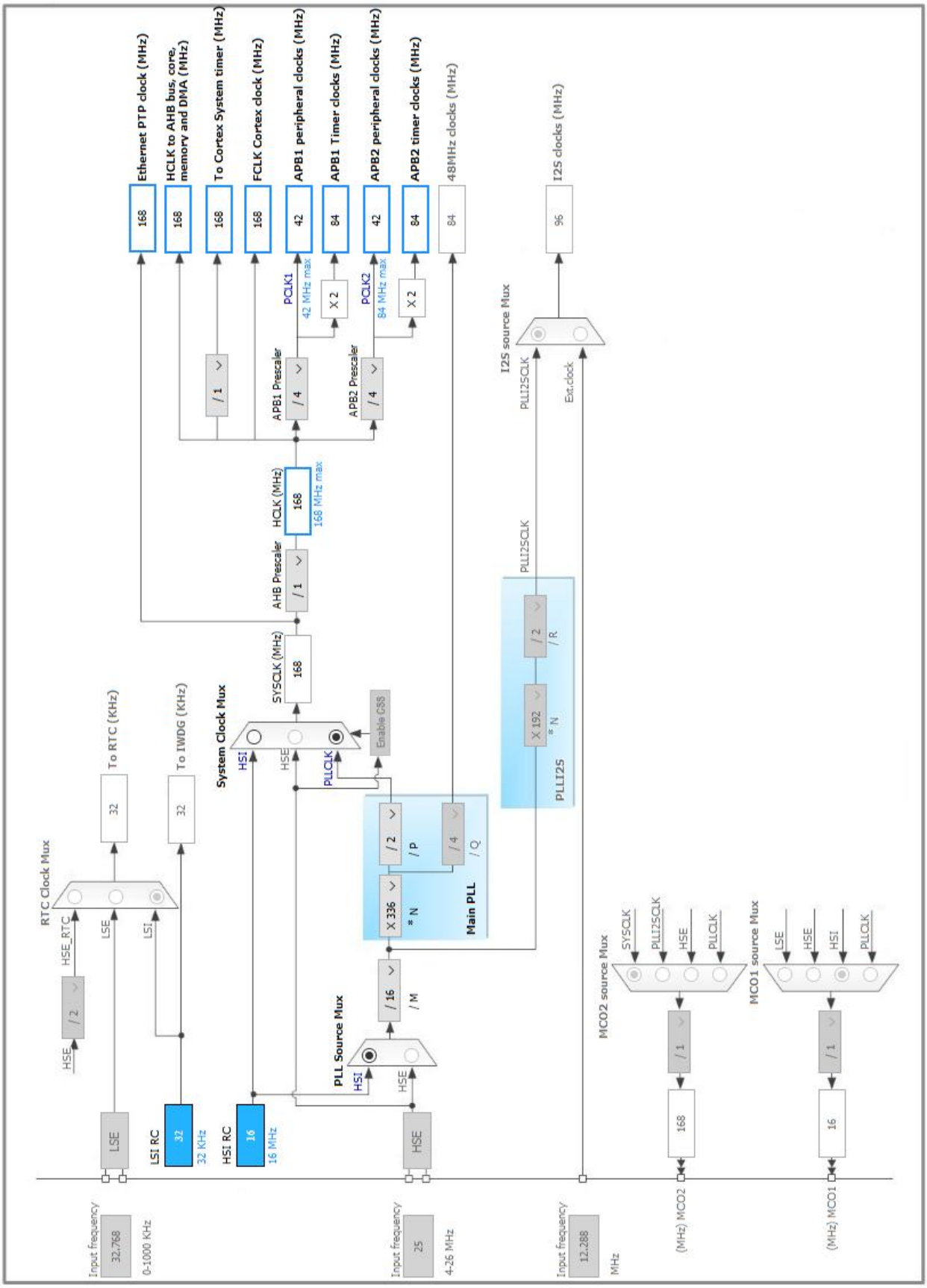
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC2_IN0	
15	PA1	I/O	ADC2_IN1	
16	PA2	I/O	ADC2_IN2	
17	PA3	I/O	ADC1_IN3	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5	I/O	ADC1_IN5	
22	PA6	I/O	ADC1_IN6	
23	PA7	I/O	ADC2_IN7	
29	PB10	I/O	I2C2_SCL	
30	PB11	I/O	I2C2_SDA	
31	VCAP_1	Power		
32	VDD	Power		
33	PB12	I/O	GPIO_EXTI12	BTN_SW2
34	PB13	I/O	GPIO_EXTI13	BTN_SW1
35	PB14 *	I/O	GPIO_Output	MOTOR_SWITCH
36	PB15 *	I/O	GPIO_Output	
37	PC6	I/O	TIM8_CH1	
38	PC7	I/O	TIM8_CH2	
39	PC8	I/O	TIM8_CH3	
40	PC9	I/O	TIM8_CH4	
41	PA8 *	I/O	GPIO_Output	BUZZER
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
56	PB4	I/O	TIM3_CH1	
57	PB5	I/O	TIM3_CH2	
58	PB6	I/O	TIM4_CH1	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
59	PB7	I/O	TIM4_CH2	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN3

mode: IN4

mode: IN5

mode: IN6

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode 2
Delay between 2 sampling phases	**20 Cycles ***

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	**Left alignment ***
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 5 ***
Sampling Time	3 Cycles
Rank	**2 ***
Channel	**Channel 4 ***
Sampling Time	3 Cycles
Rank	**3 ***
Channel	Channel 3
Sampling Time	3 Cycles
Rank	**4 ***
Channel	**Channel 6 ***

Sampling Time	3 Cycles

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN0

mode: IN1

mode: IN2

mode: IN7

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	**DMA access mode 2 ***
Delay between 2 sampling phases	**20 Cycles ***

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	3 Cycles
Rank	**3 ***
Channel	**Channel 2 ***
Sampling Time	3 Cycles
Rank	**4 ***

Channel	**Channel 7 ***
Sampling Time	3 Cycles

WatchDog:

Enable Analog WatchDog Mode	false

5.3. I2C2

I2C: I2C

5.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.4. SYS

Debug: Serial Wire Debug (SWD)

5.5. TIM3

Clock Source : Internal Clock

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**6 ***

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**6 ***

5.6. TIM4

mode: Clock Source

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**6 ***

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter (4 bits value)	**6 ***

5.7. TIM8

Clock Source : Internal Clock

Channel1: Output Compare CH1

Channel2: Output Compare CH2

Channel3: Output Compare CH3

Channel4: Output Compare CH4

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 2:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 4:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. FREERTOS

mode: Enabled

5.9.1. Config parameters:

Versions:

CMSIS-RTOS version	1.02
FreeRTOS version	8.2.1

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000

MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4
USE_ALTERNATIVE_API	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY	Enabled
GENERATE_RUN_TIME_STATS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.9.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled

vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA0-WKUP	ADC2_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC2_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC2_IN7	Analog mode	No pull-up and no pull-down	n/a	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PB12	GPIO_EXTI12	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	BTN_SW2
	PB13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	BTN_SW1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_SWITCH
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUZZER

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	**Half Full ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	15	0
EXTI line[15:10] interrupts	true	5	0
DMA2 stream0 global interrupt	true	5	0
Non maskable interrupt	unused		
Hard fault interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	022152_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	NYP
Project Folder	C:\Users\Vergil\Documents\Projects\NYP
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.10.1

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No