4-Bit Carry Lookahead Adder Design

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***Abstract*—This paper describes the design of a 4-Bit (CLA) Carry Look Ahead Adder circuit. It is a basic Boolean Arithmetic circuit that is used in the ALU of modern digital computers and microcontrollers to perform arithmetic operations. The basic advantage of a CLA over a generic RCA (Ripple Carry Adder) is that it takes much less time to computer the addition results that is Sum bits and carry out bits. Which is one of the very important metrics to characterize the performance of any digital circuit.**

Keywords—delay, RCA, Full Adder, XOR

I. Description

Adder circuits are very essential digital circuits, as they perform the task of addition which is an Arithmetic operation needed to be performed in modern digital signal processors and microcontrollers. The unit of a computer processor that performs all the arithmetic operations is called an ALU (Arithmetic Logic Unit). So naturally Adders become an integral part of the ALU. Now the most general form of a n-bit adder is constructed by cascading n Full Adders in conjunction. This is the simplest type of adder circuit also known as RCA (Ripple Carry Adder). It is called so because one i^{th} stage of RCA is i^{th} Full Adder that is producing the carry out for the next i.e. $(i+1)^{th}$ stage as it's carry input. So the output of each $(i+1)^{th}$ stage is a function of the carry output of its previous i.e. i^{th} stage. In this way the carry out propagates in the form of ripples through the starting stage to the last stage, and until this rippling completes the final output i.e. the sum and the Cout bits are not certain to be correct. This delay of the RCA circuits increases with the increase in bits or stages. So for complex n-bit additions the delay of RCA increases too much to be affordable. In this case, we need to find a faster and efficient method of computer the additions of bits which optimises the performance of the ALU. One such implementation is a CLA (Carry Look Ahead) Adder also called Fast Adder.

CLA removes the dependency of carry of each stage to the output of next stage. It makes use of generator bits g_i and propagate bits p_i which are independent of the carry bit. So, the full adder in RCA can be represented as shown below.

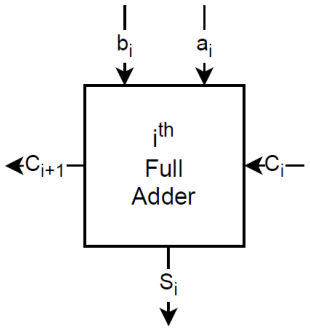

Figure 1 i^{th} Full Adder Bock in RCA

In CLA, this i^{th} block is replaced by these three components:

a) p_i and g_i generator
b) CGN (C_{i+1} generator network)
c) S_i (Sum generator)

Each term in CLA is expressed as:

$$C_{i+1} = a_i b_i + C_i(a_i \text{ xor } b_i)$$
$$g_i = a_i b_i$$
$$p_i = a_i \text{ xor } b_i$$
$$\mathbf{C_{i+1} = g_i + C_i p_i}$$
$$S_i = a_i + b_i + C_i$$
$$\mathbf{S_i = p_i \text{ xor } C_i}$$

II. Block Diagram

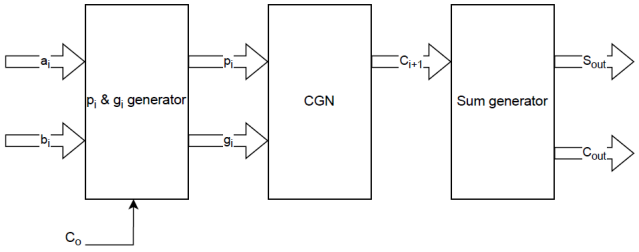

Figure 2 Block Diagram of CLA

As shown in the diagram above, the CLA work in 3 steps:
Step 1: To find all the p_i and g_i signals
Step 2: Find the carry of each stage
Step 3: using the carrys & propagate signals, generate sum.

III. Waveform

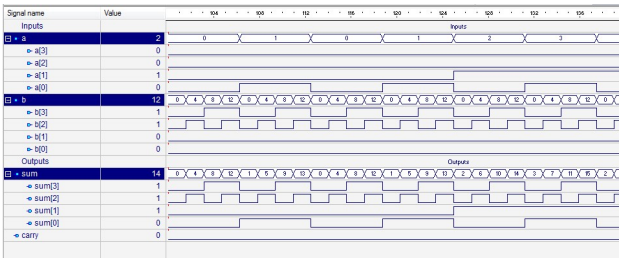

Figure 3 Reference Waveform for 4-bit addition

IV. References

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[2] Wikipedia reference: https://en.wikipedia.org/wiki/Carry-lookahead_adder