

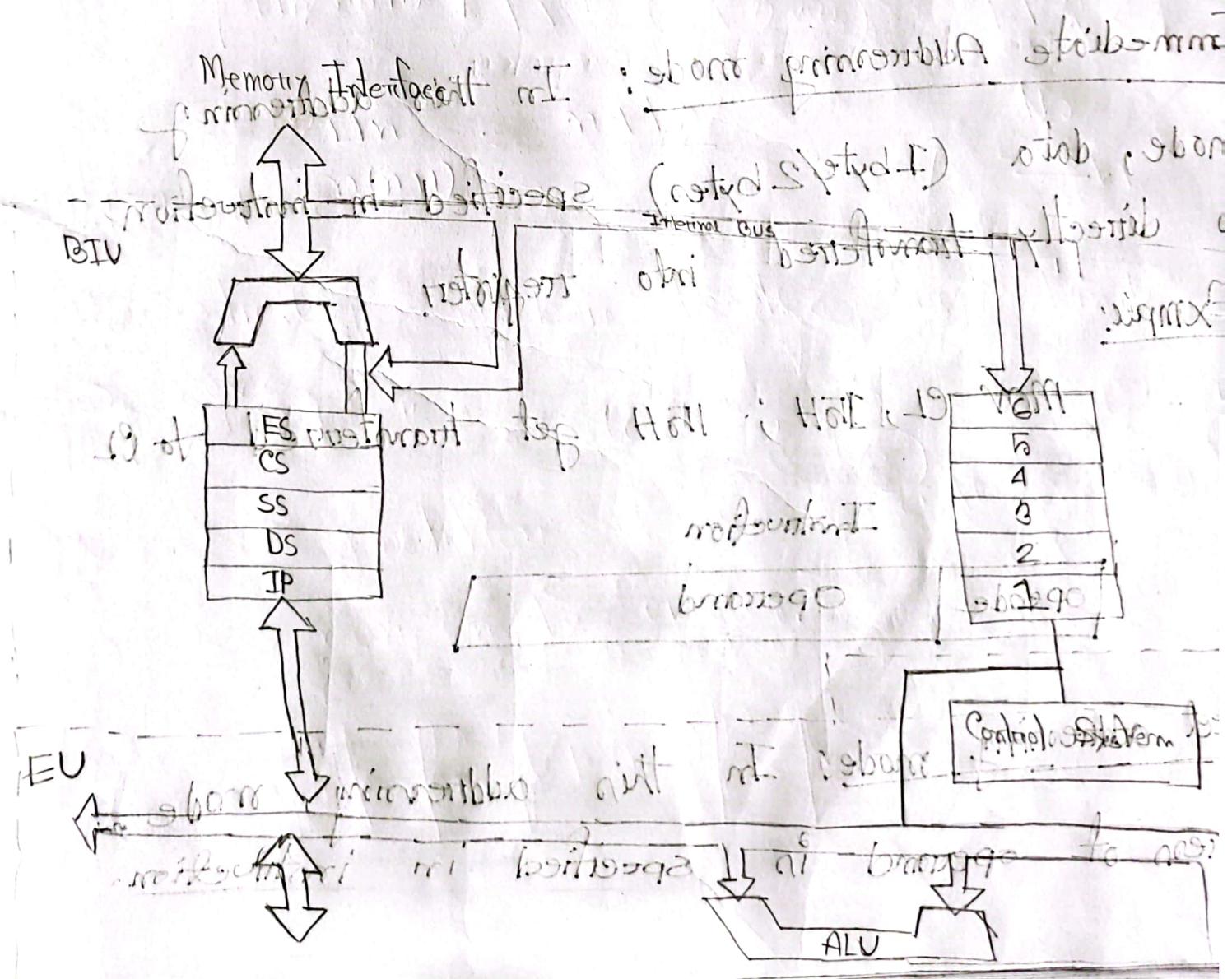
# Microprocessor

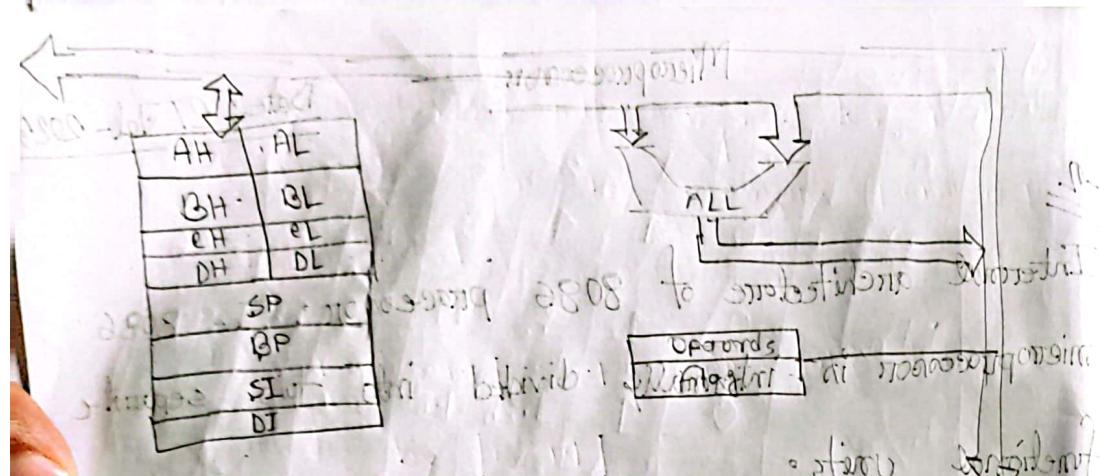
Date: 27 Oct.

L-0

Internal architecture of 8086 processor: The 8086 microprocessor is internally divided into two separate functional units:

- ① Bus interface unit (BIU) : 0808
  - ② Execution unit (EU)





Addressing modes of 8086:

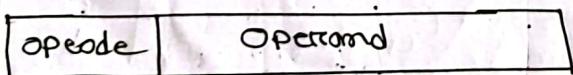
(U.S) Immediate addressing (1)  
(U.I) Indirect addressing (2)

Immediate Addressing mode: In this addressing mode, data (1-byte/2 bytes) specified in instruction is directly transferred into register.

Example:

MOV CL, 15H ; 15H get transferred to CL

Instruction

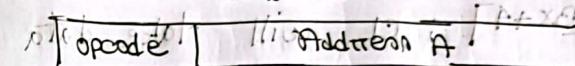


Direct addressing mode: In this addressing mode, address of operand is specified in instruction.

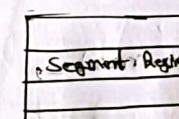
Example

MOV CL, [BX]  
In this addressing mode, the value at the address CL will take data pointed by BX addressing.

Instruction



Registers



+10

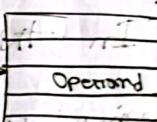
0

nat. HI

0

nat. LO

0



+10

0

nat. HI

0

nat. LO

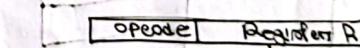
Register Indirect: In this addressing mode, operand address will be given by memory pointer.

Example:

MOV CL, [BX]

CL will take data pointed by BX address

Instruction



Registers

Pointer to Operand

Segment Register

+10

0

nat. HI

0

nat. LO

0



Register Relative: In this addressing mode, operand address will be given by memory pointer + 8 bit displacement. (16 bits add 16 bits)

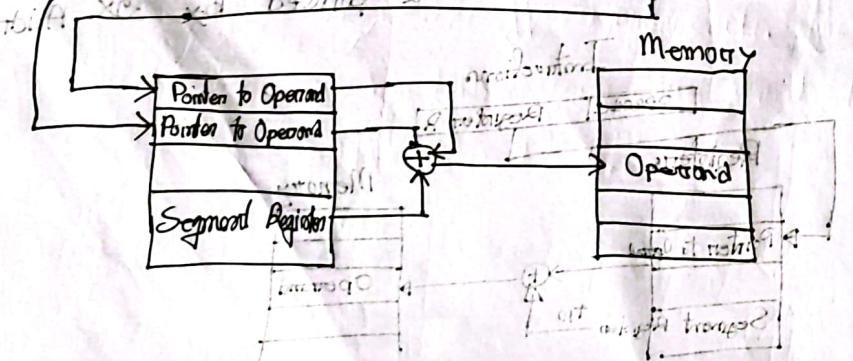
Ex:  $\text{MOV CL}, [\text{BX}+4]$  ; CL will take data pointed by  $[\text{BX}+4]$

Based Indexed: In this addressing mode, operand addressing will be given by

Base Register + Index Register.

Ex:  $\text{MOV DL}, [\text{BX}+\text{SI}]$

Op code | Base Register | Index Register



# Differences between microprocessor and microcontroller.

Microprocessor	Microcontroller
① Microprocessor is the heart of Computer System.	① Micro controller is the heart of an embedded system
② It is only a processor, so memory and I/O components need to be connected externally.	② Micro Controller has a processor along with internal memory and I/O components
③ Memory and I/O has to be connected externally, so the circuits becomes large.	③ Memory and I/O components are already present and the internal circuit is small.
④ Cost of entire system is high.	④ Cost of entire system is low.
⑤ It is complex and expensive.	⑤ It is simple and inexpensive

non maskable interrupt	marked nonmaskable

- Legend:  $\rightarrow$  sets 0 signal to 1 state.  $\leftarrow$  sets 1 signal to 0 state.
- Pins of 8086 Microprocessor:
- ① NMI: non maskable interrupt line with active low logic.
  - ② BHE: bus high enable.
  - ③ TEST: tested by the WAIT instruction.
  - ④ HLDA: hold of 8086.
  - ⑤ ALE: address latch enable.
- Description: shows in schematic block :  $f10.44$  (b)
- ① NMI: The non maskable interrupt input (NMI) is similar to INTR except that the NMI interrupt does not check to see if the "If" flag bit is at logic 1.
- This interrupt cannot be masked (not disabled) and no acknowledgement is required. It should be issued in case of "catastrophic" events such as power failure or memory errors.
- ② BHE: bus high enable: enables the most significant data bus bits (D15-D8) during a read or write operation.
- ③ TEST: The TEST pin is an input that is tested by the WAIT instruction.

If TEST is at logic 0, the WAIT instruction function as a NOP. And if TEST is at logic 1 then the wait instruction causes the 8086 to idle.

ACTION

TEST

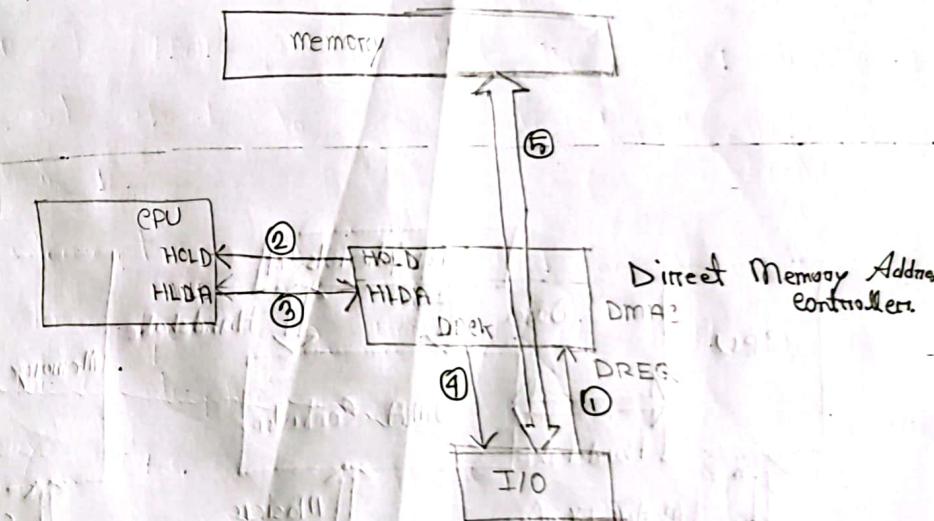
④ HLDA: Hold acknowledge is made high to indicate to the DMA controller that the processor has entered hold state and it can take control over the system bus for DMA operation. "HOLD" is one of the signals to

⑤ ALE: The ALE pin in the 8086 microprocessor is an address latch enable pin. The ALE pin is used in 8086 microprocessor because the address/data is multiplexed in the 8086 microprocessor. This means that the same bus lines are used to carry both the address and the data.

at least begin in a high TEST with TEST

# Describe the basic operations of DMA with appropriate figure.

Direct Memory Access (DMA): DMA is a method that allows an input/output (I/O) device to send or receive data directly to or from the main memory bypassing the CPU to speed up memory operation.



① DREQ → DMA Request

② HOLD → Hold signal

③ HLDA → Hold Acknowledgement

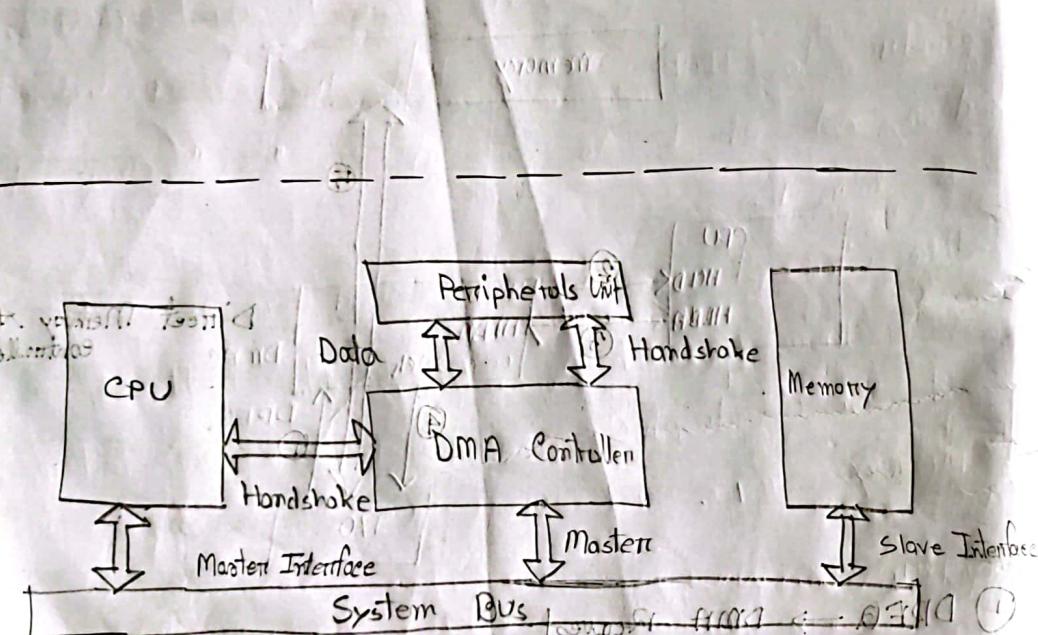
④ DMA → DMA Acknowledgement

## 3 modes of DMA controller:

① Burst Mode:

② Cycle stealing Mode:

③ Transparent Mode:



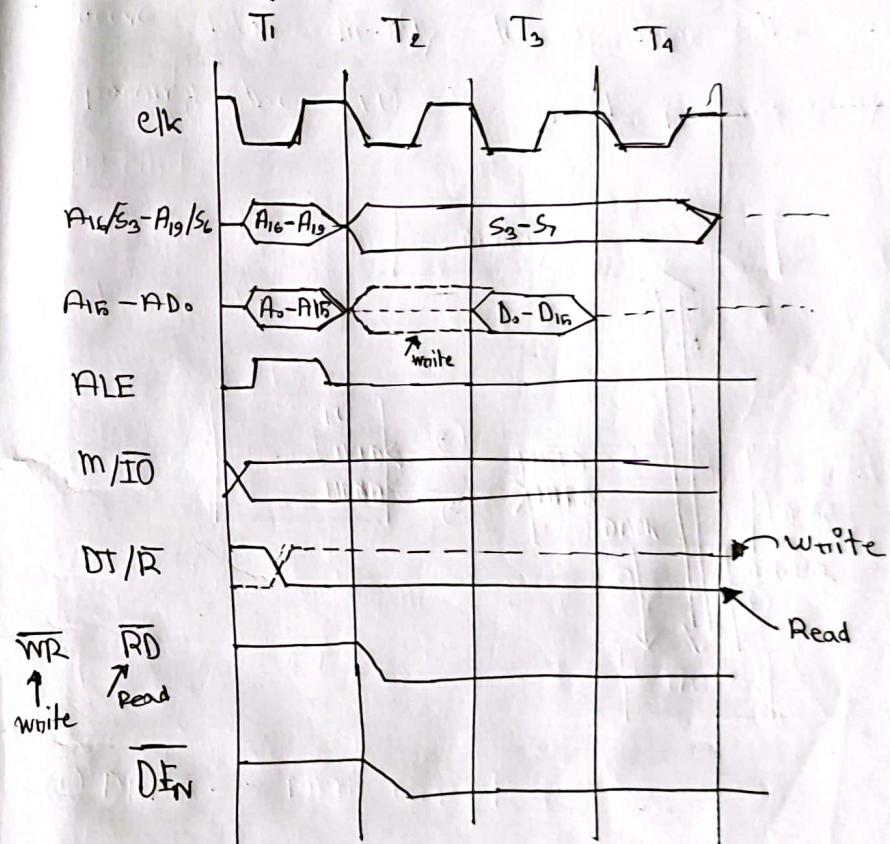
longie blotl  $\leftarrow$  C10H ⑧

Transf. word A blotl  $\leftarrow$  F11H ⑨

# Explain the read and writing cycle timing diagram for maximum mode/minimum mode.

Minimum mode:

Read timing diagram of 8086 minmode



10th batch

3

② Explain how microprocessor receives data from the memory?

① STOSB: The "STOSB" instruction stands for "Store String Byte". It is used to store a byte of data at the address pointed to by the DI register.

② MOVSB: The "MOVSB" instruction stands for "Move String Byte". It is used to move a byte of data from the address pointed to by the SI register to the address pointed to by the DI register.

③ SEASW: The "SEASW" stands for "Scan String for Word". It is used to scan a string for a word that matches the value in the AX register.

④ CBW: The "CBW" stands for "Convert Byte to Word". It is used to convert the byte in the AL register to a word in the AX register.

(3)

(a) Microprocessor access data from memory by following these steps:

① The microprocessor generates a memory address representing the data location.

② It communicates with the memory subsystem through the memory bus.

③ The microprocessor initiates a memory read operation by putting the address bus and asserting control signals.

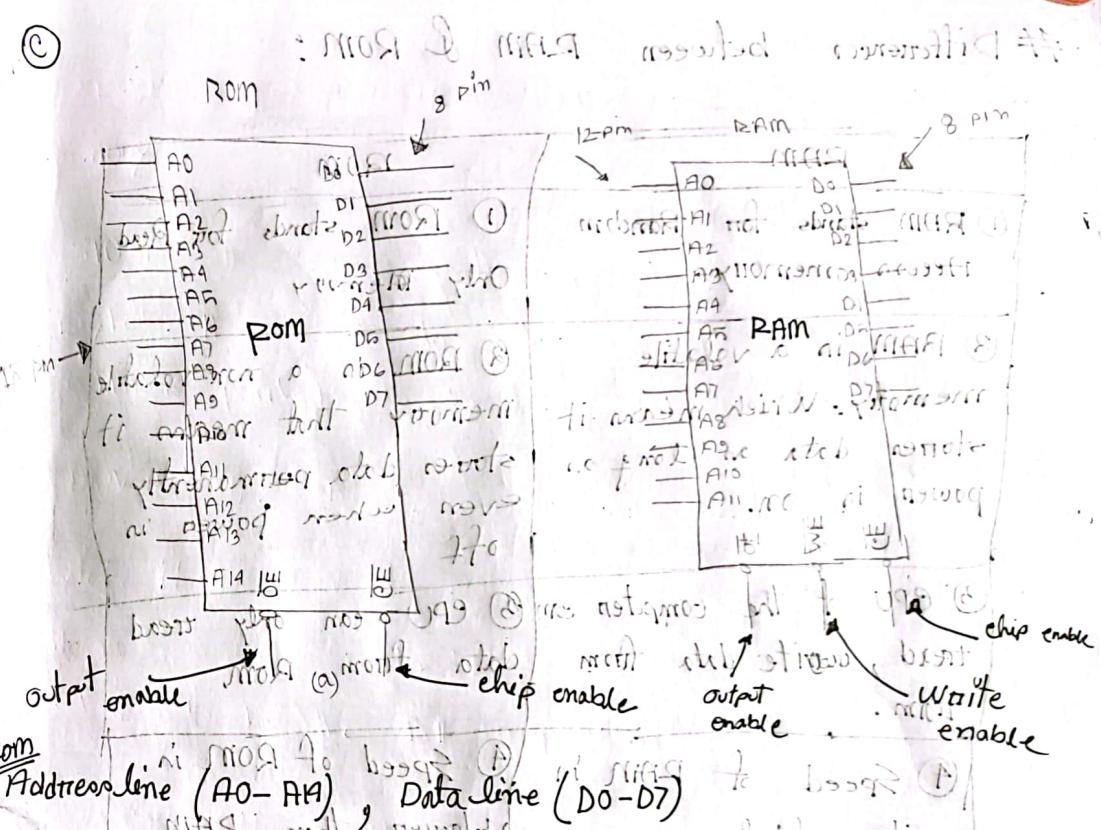
④ The memory controller processes the request, translates the address if necessary, and selects the appropriate memory module.

⑤ The requested data is read from the memory cell and placed on the data bus.

⑥ The microprocessor receives the data from the data bus and loads it into a register.

⑦ The memory access cycle is completed.

(c)



ROM

Address line (A0-A15)

Data line (D0-D7)

Pin

Setup

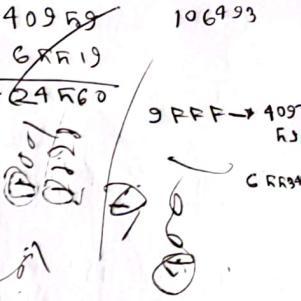
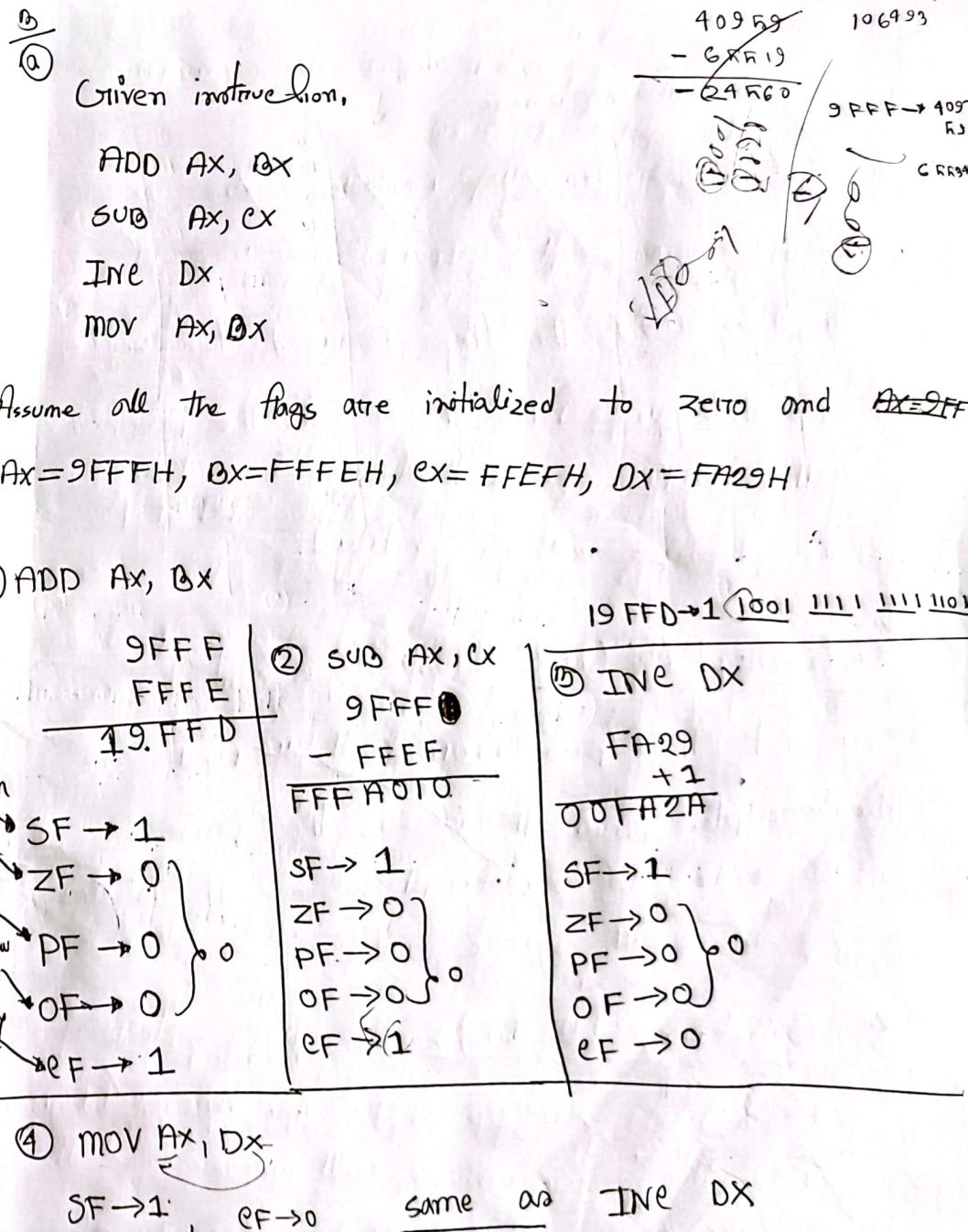
Since the device has 15 address lines and 8 data lines, it

has  $2^{15}$  (32k) memory locations and each memory location

stores 8 bit data.

## # Differences between RAM & ROM:

RAM	ROM
① RAM stands for Random Access memory.	① ROM stands for Read Only Memory
② RAM is a volatile memory. Which means it stores data as long as power is on.	② ROM is a non-volatile memory that means it stores data permanently even when power is off
③ CPU of the computer can read, write data from RAM.	③ CPU can only read data from ROM.
④ Speed of RAM is quite high.	④ Speed of ROM is slower than RAM
⑤ RAM is costly.	⑤ ROM is not so expensive



⑥

Discuss the following flags:

① Trap flag: This flag controls whether or not the processor will respond to interrupts.

② Trap flag (TF): This flag is used for single-step debugging. When TF is set, the processor will execute one instruction at a time and the debugger will be notified.

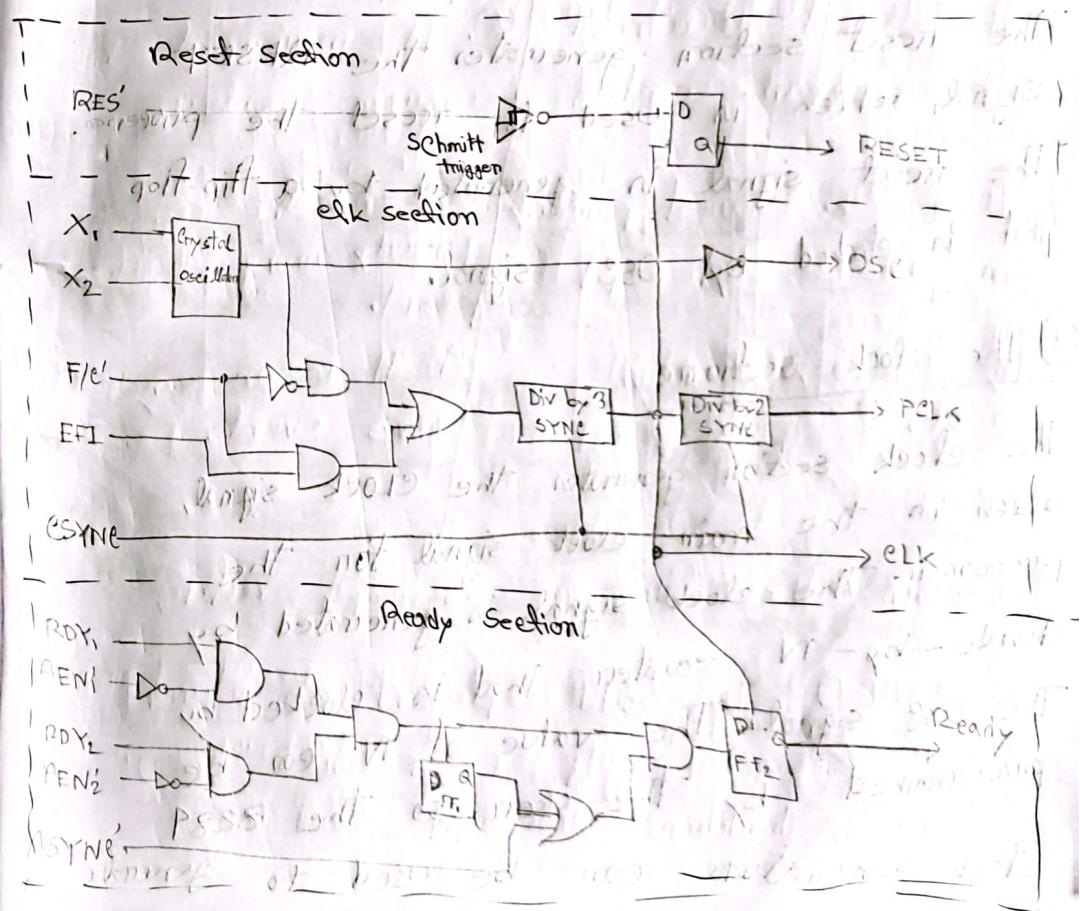
③ Interrupt flag (IF): This flag controls whether or not the processor will respond to interrupts. When IF is set, the processor will respond to interrupts. When IF is cleared, the processor will ignore interrupts.

④ Direction flag (DF): This flag controls the direction of string operations. When DF is set, string operations will increment the pointer. When DF is cleared, string operations will decrement the pointer.

⑤ Overflow flag: The overflow flag (OF) is a single bit in a system status register used to indicate when an arithmetic overflow has occurred in an operation.

⑥

8084 clock generator:



The 8284 clock generator has three main sections, ~~the clock section~~

① The reset section

② The clock section

③ The ready section

### ① The reset section:

The reset section generates the 'RESET' signal, which is used to reset the processor.

The reset signal is generated by a flip-flop that is clocked by OSC signal.

### ② The clock section:

The clock section generates the CLOCK signal, which is the main clock signal for the processor. The clock signal is generated by divide-by-N counter that is clocked by the OSC signal. The value of N can be programmed by the user, so the 8284

o variety of clock frequencies.

### ③ The Ready Section:

The ready section generates the ready signal, which is used to indicate to the processor that the bus is in ready state for access. The ready signal is generated by a flip-flop that is clocked by the clock signal.

### ④ Purpose of interrupt:

The purpose of interrupt is to allow an external device to request the attention of the processor. When an interrupt occurs, the processor will suspend the current instruction and execute the interrupt service routine (ISR) to service the interrupt.

## Differences between hardware interrupt and software interrupt:

Hardware interrupt	Software interrupt
① Hardware interrupt is an interrupt generated from an external device or hardware.	② Software interrupt is the interrupt that is generated by any internal system of the computer.
② It does not increment the program counter.	③ It increments the program counter.
③ It has the lowest priority than software interrupt	④ It has the highest priority among all interrupts.
⑤ It is an asynchronous event.	⑤ It is an synchronous event.

Q) Explain the following interrupt vectors:

① TYPE0: This could represent an interrupt vector associated with a specific "type 0" event. In traditional interrupt handling,

type 0 interrupts are often reserved for processor specific purposes.

② Type 1: In some systems, type 1 interrupts are used for hardware-related exceptions or traps.

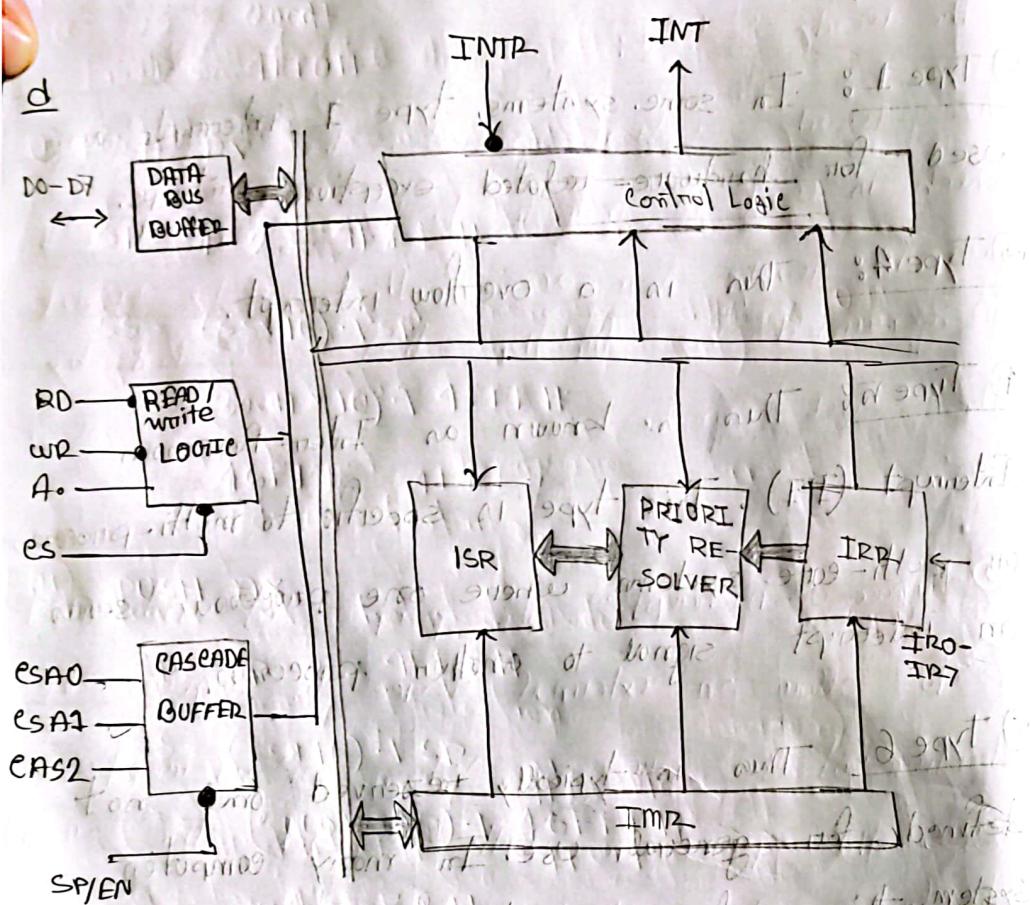
③ Type 4: This is a overflow interrupt.

④ Type 5: This is known as Inter-processor Interrupt (IPI). This type is specific to multi-processor or multi-core systems where one processor sends an interrupt signal to another processor.

⑤ Type 6: This is typically reserved and not defined for general use. In many computer systems, this vector is not allocated for any specific purpose or function.

⑥ Type7: This interrupt is a software interrupt that is used to call a subroutine. It is also known as software interrupt or software trap.

generated interrupt.



The 8259A PIC has four registers:

IMR: The interrupt mask register is used to mask interrupts.

IRR: The interrupt request register is used to store the pending interrupts.

ISR: The interrupt service register is used to store the address of the interrupt service routine.

PIC1: The PIC1 register is used to communicate with the first PIC.

9th batch

A①

$$SS = 3000H$$

$$SP = 4FF0H$$

① PUSH BX

$$SP = SP - 2 = 4FEEH$$

$$SS = (SS * 16) + SP -$$

$$16 \rightarrow \underline{\underline{10H}}$$

$$= (3000H * 10) + 4FEEH$$

$$= \underline{\underline{34FEEH}}$$

⑪ PUSH AX

$$SP = SP - 2 = 4FECCH$$

$$SS = (SS * 16) + SP$$

$$= (3000H * 10) + \underline{\underline{4FEEH}}$$

$$= \underline{\underline{4FECCH}}$$

⑫ PUSH DX

$$SP = SP - 2 = 4FEAH$$

$$SS = (3000H * 10) + 4FEAH = 46FEAH$$

4(c)

① MOV BX, A536H: Directly loads the value 'A536H' into the BX register.

② MOV BX, [A536H]: Indirectly loads the value stored at memory address 'A536H' into the BX register.

⑬

Code

model small

stack 100h

.data

n dw 10

sum dw 0

.code

main proc

mov bx, @data

mov ds, bx

mov bx, 1

mov ex, n

sum-loop:

mov ax, bx

mul ax

add sum, ax

inc bx

94R

⑥

⑦

Limitations of Real Mode:

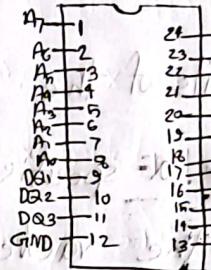
- ① Limited memory addressing
- ② No memory protection
- ③ Complicated memory addressing
- ④ No multitasking.
- ⑤ Lack of hardware support for modern features.

Features of Protected Mode:

- ① Memory protection
- ② Flat memory addressing
- ③ Multitasking support
- ④ Virtual memory
- ⑤ Enhanced addressing mode

6

⑥



Pin	Description
A0-A9	Address
DQ0-DQ7	Data In
S(CS)	chip select
EN(COE)	Read Enable
W(WE)	Write Enable

6 ⑥ Differences between 80286 and 80386 microprocessors:

from 80286 to 80386  
soft part of 80286 will be same

80286	80386
① 16 bit instruction set.	① 32 bit instruction set
② 16-bit addressing mode	② 32-bit addressing mode
③ Segmented memory model.	③ flat memory model
④ no built in cache	④ 8kB on chip cache.

other notable differences  
program manager, windows interface

③

(iii) SHL (Shift Left): Shifts bits of the destination operand left by a specific number of bits, filling the vacated bits with zeros.

(iv) RCR (Rotate through Carry Right): Rotates bits of the destination operand right through the carry flag carrying the least significant bit to the most significant bit.

(v) AAD (ASCII Adjust for Division):

Adjusts the contents of AL after a signed division to convert the results into a valid ASCII representation.

(vi) LEA (Load Effective Address): Loads the effective memory address into a register without accessing memory.

section .data

str db 'Hi', 0

section .bss

reversed\_str resb 100

section .text

global \_start

\_start :

mov esi, str

find\_length:

cmp byte [esi], 0

jne reverse\_string

inc esi

jmp find\_length

reverse\_string:

dec esi

mov edi, reversed\_str

reverse\_loop:

mov al, [esi]

mov [edi], al

inc edi

dec esi

cmp esi, str

jge reverse\_loop

mov byte [edi], 0

Features of Pentium Processor:

① Superscalar Architecture: