

## Assignment 7

*Out: 04/22/2013**Due: 04/30/2013*

1. **(10 Points)** Consider a logical address space of 64 pages of 1024 words each, mapped onto a physical memory of 32 frames.
  - (a) **(5 Points)** How many bits are there in the logical address?
  - (b) **(5 Points)** How many bits are there in the physical address?
2. **(10 Points)** Describe a mechanism by which one segment could belong to the address space of two different processes.
3. **(10 Points)** Under what circumstances do page faults occur? Describe the actions taken by the operating system when a page fault occurs.
4. **(10 Points)** We have an operating system for a machine that uses base and limit registers, but we have modified the machine to provide a page table. Can the page tables be set up to simulate base and limit registers? How can they be, or why can they not be?
5. **(10 Points)** Explain the usefulness of a modify bit.
6. **(10 Points)** Explain why SSTF scheduling tends to favor middle cylinders over the innermost and outermost cylinders.
7. **(10 Points)** Could you simulate a multilevel directory structure with a single-level directory structure in which arbitrarily long names can be used? If your answer is yes, explain how you can do so, and contrast this scheme with the multilevel directory scheme. If your answer is no, explain what prevents your simulations success. How would your answer change if file names were limited to seven characters?
8. **(10 Points)** Why is it advantageous for the user for an operating system to dynamically allocate its internal tables? What are the penalties to the operating system for doing so?
9. **(10 Points)** How does DMA increase system concurrency? How does it complicate hardware design?
10. **(10 Points)** What are the main differences between capability lists and access lists?