The 8255 (PPI) Programmable Peripheral Interface

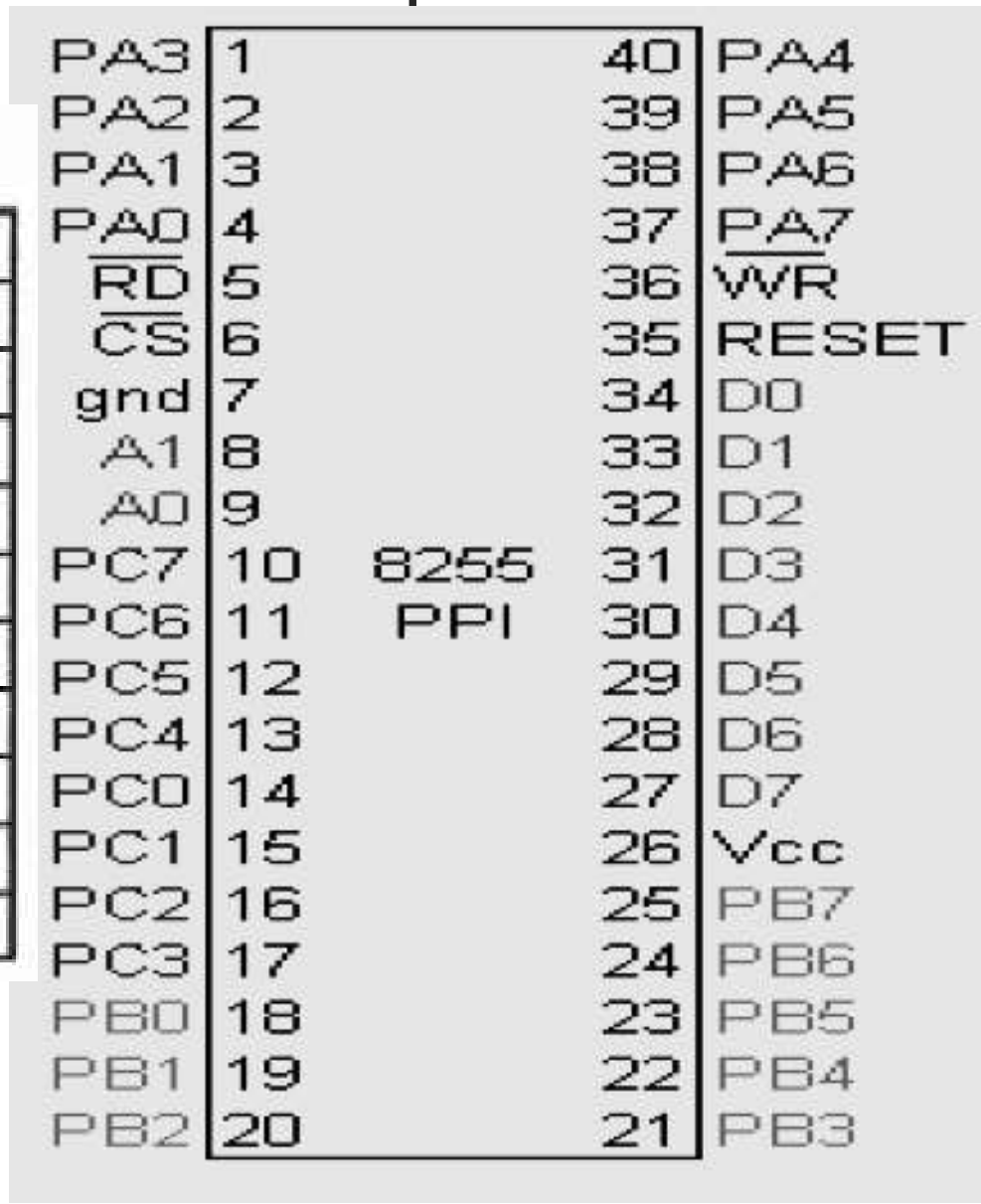
Features of 8255

- It is programmable parallel I/O device
- It is 40 pin IC
- 24 I/O lines arranged as
  - 3, 8-bit ports (port A, B, C).
  - Port C can be used as 2, 4-bit ports.
- Direct bit set/reset capability is at port C
- 8255 can operate in 3 modes :
  - Mode 0 – simple i/o
  - Mode 1 – strobed i/o
  - Mode 2 – strobed bidirectional i/o

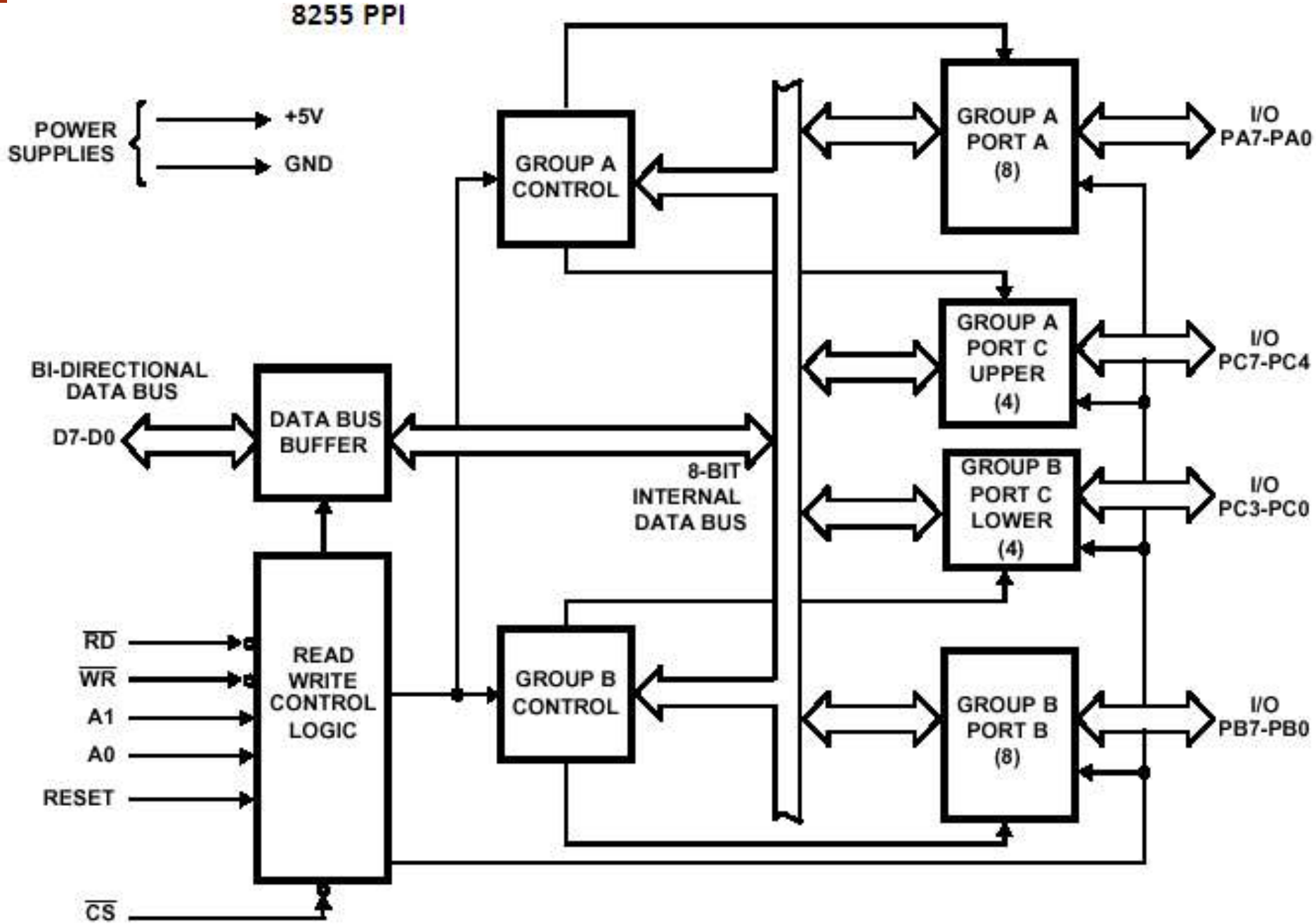
PIN Diagram and description

Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0, A1	Port Address
PA7–PA0	Port A (bit)
PB7–PB0	Port B (bit)
PC7–PC0	Port C (bit)
V_{cc}	+5V
GND	0V



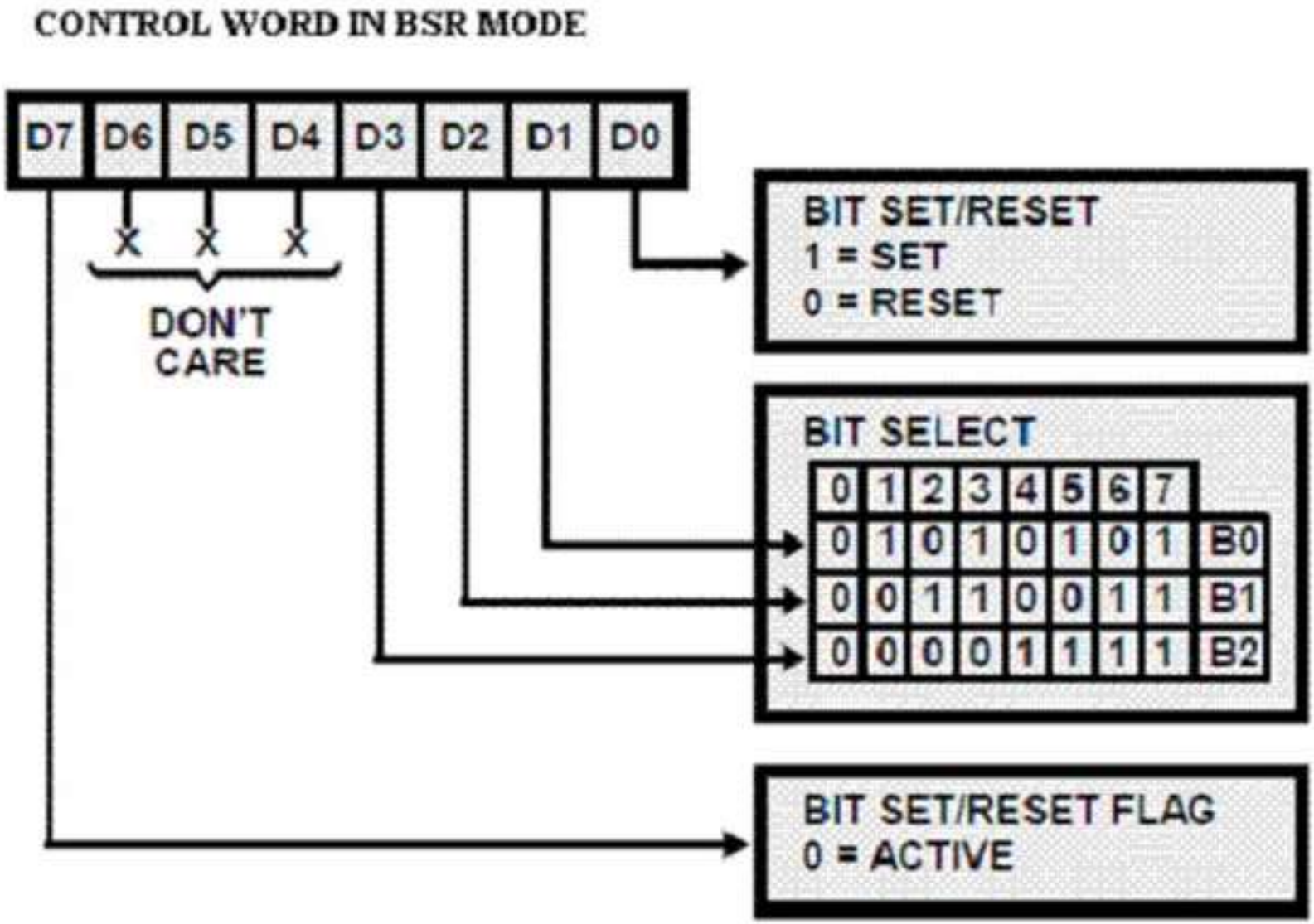
Block Diagram



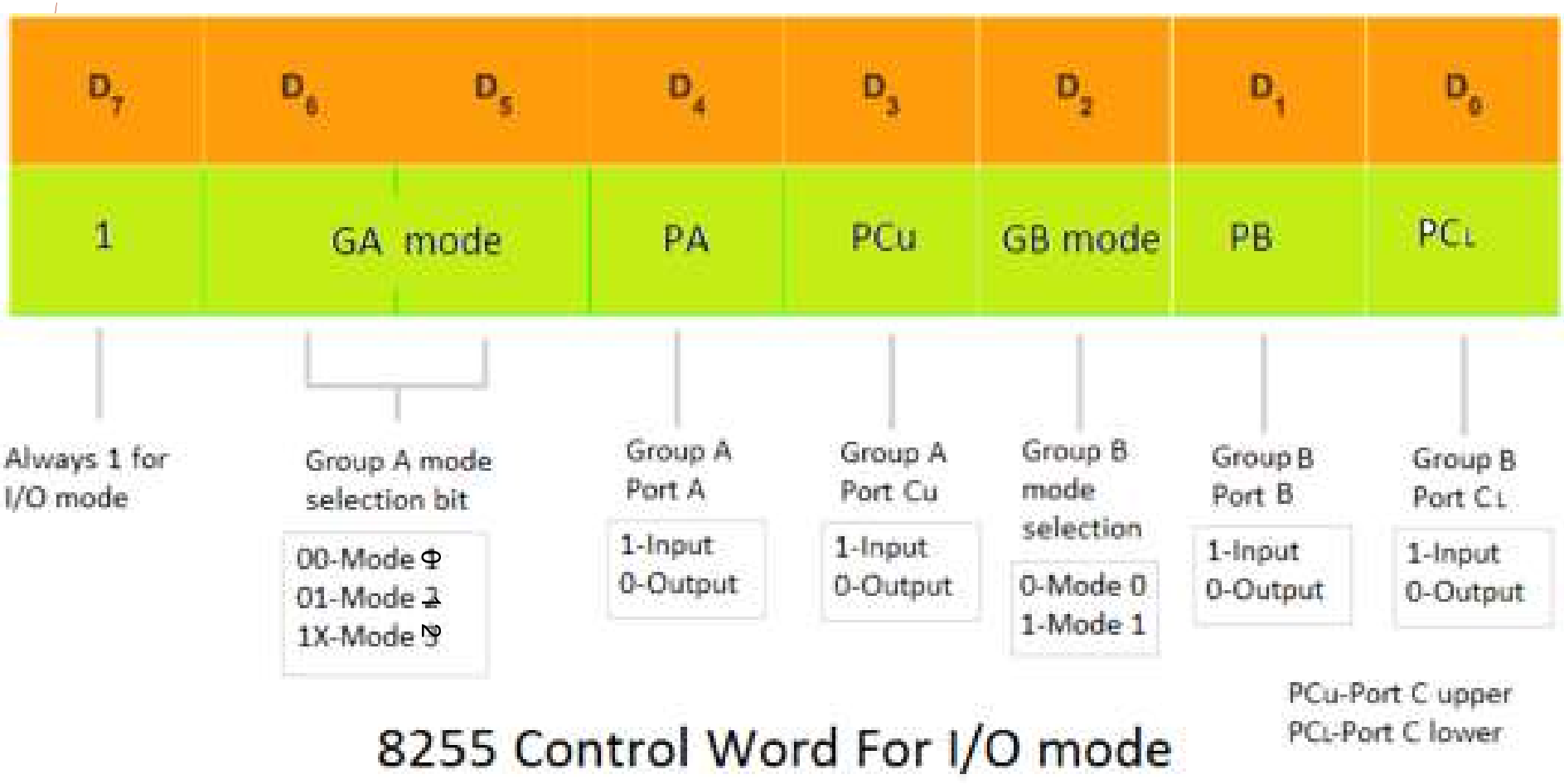
8255 Truth Table

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Operations
					Input (Read) Operation
0	0	0	1	0	Port A to Data Bus
0	1	0	1	0	Port B to Data Bus
1	0	0	1	0	Port C to Data Bus
					Output (Write) Operation
0	0	1	0	0	Data Bus to Port A
0	1	1	0	0	Data Bus to Port B
1	0	1	0	0	Data Bus to Port C
1	1	1	0	0	Data Bus to Control Register
					Disable Function
X	X	X	X	1	Data Bus Tri-stated
1	1	0	1	0	Illegal Condition
X	X	1	1	0	Data Bus Tri-stated

8255 BSR mode



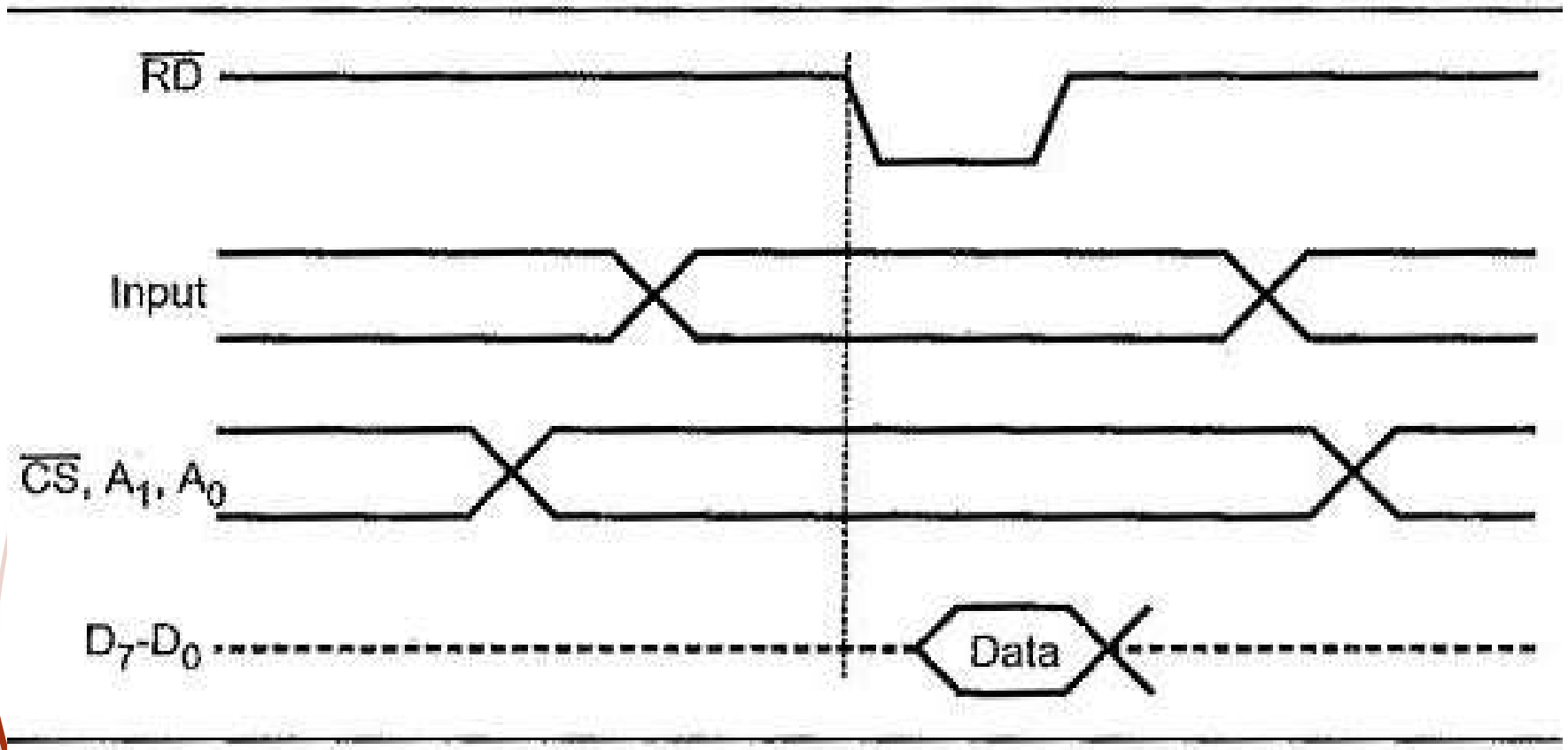
8255 I/O mode



8255 Control Word For I/O mode

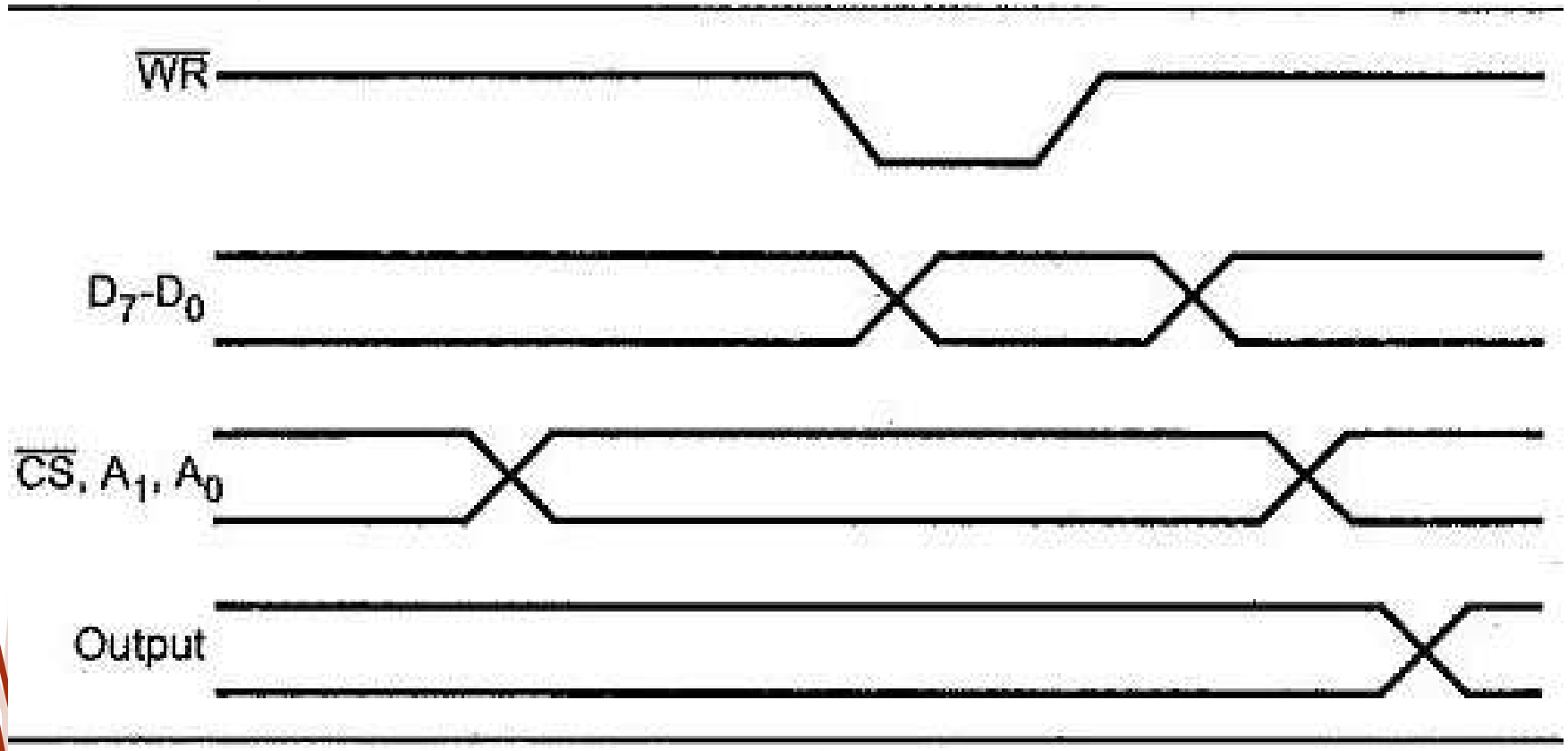
I/O operating modes

- Mode 0 – input mode

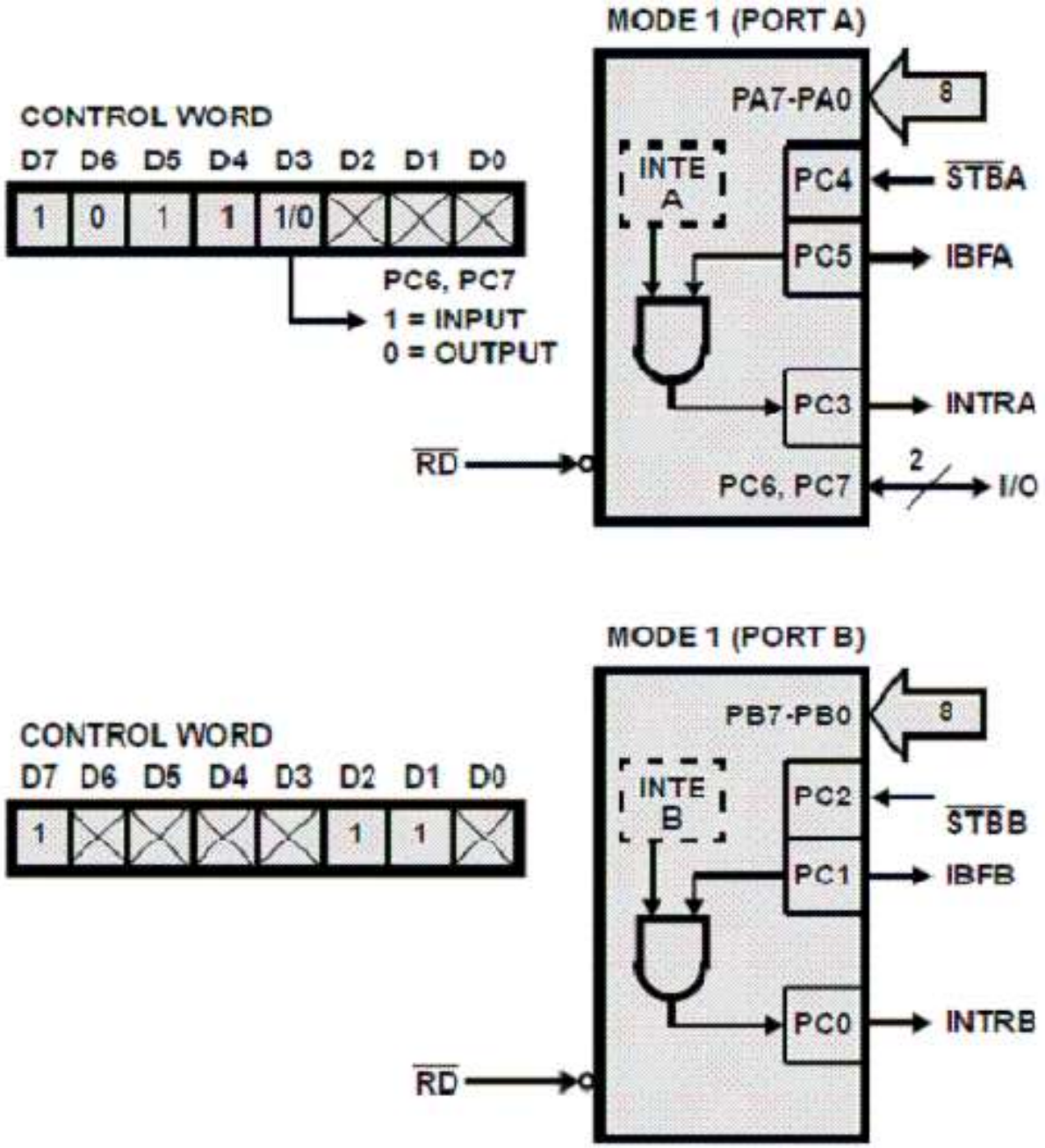


I/O operating modes

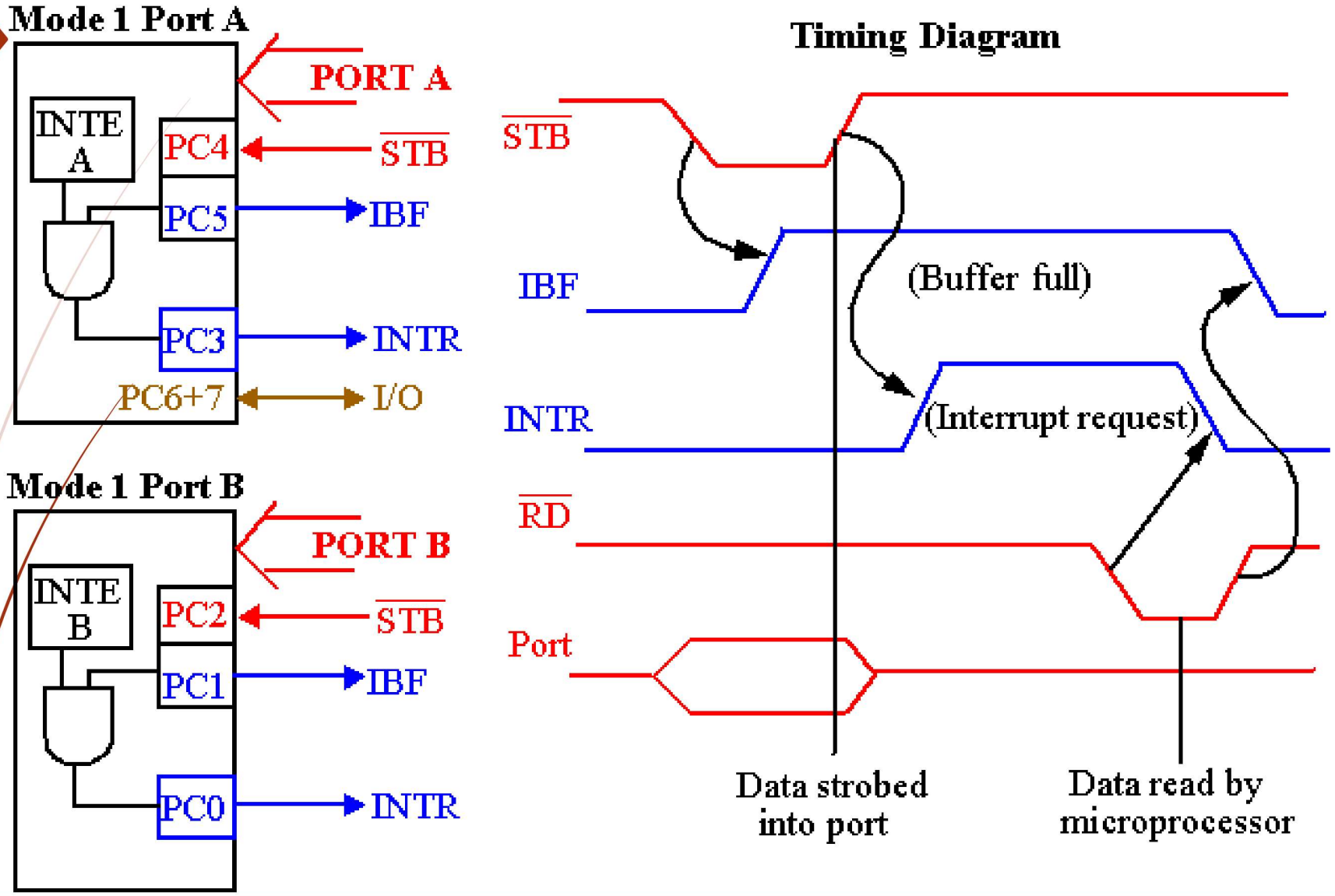
- Mode 0 – output mode



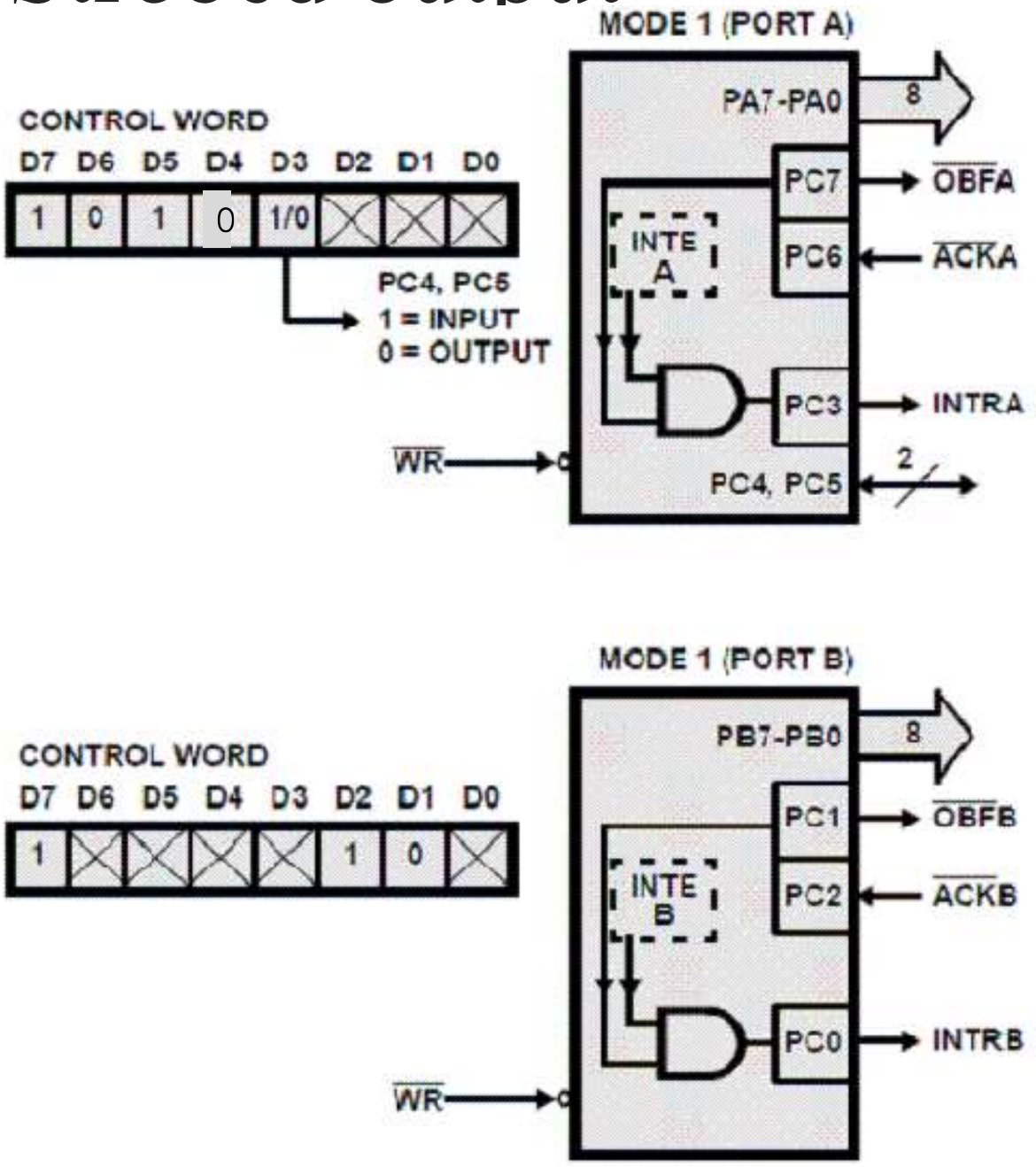
Port A,B – Strobed input



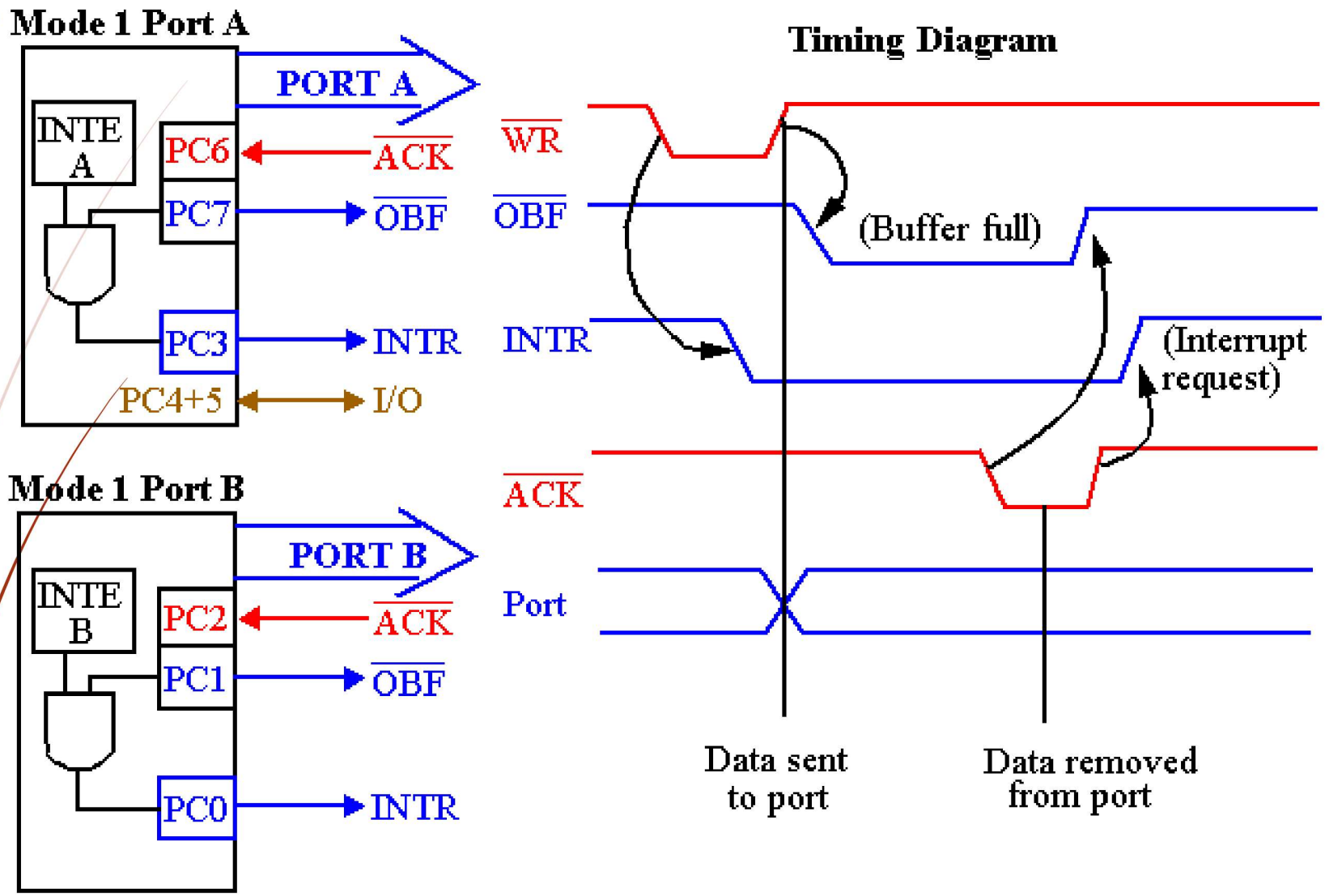
Port A,B – Strobed input



Port A,B – Strobed output

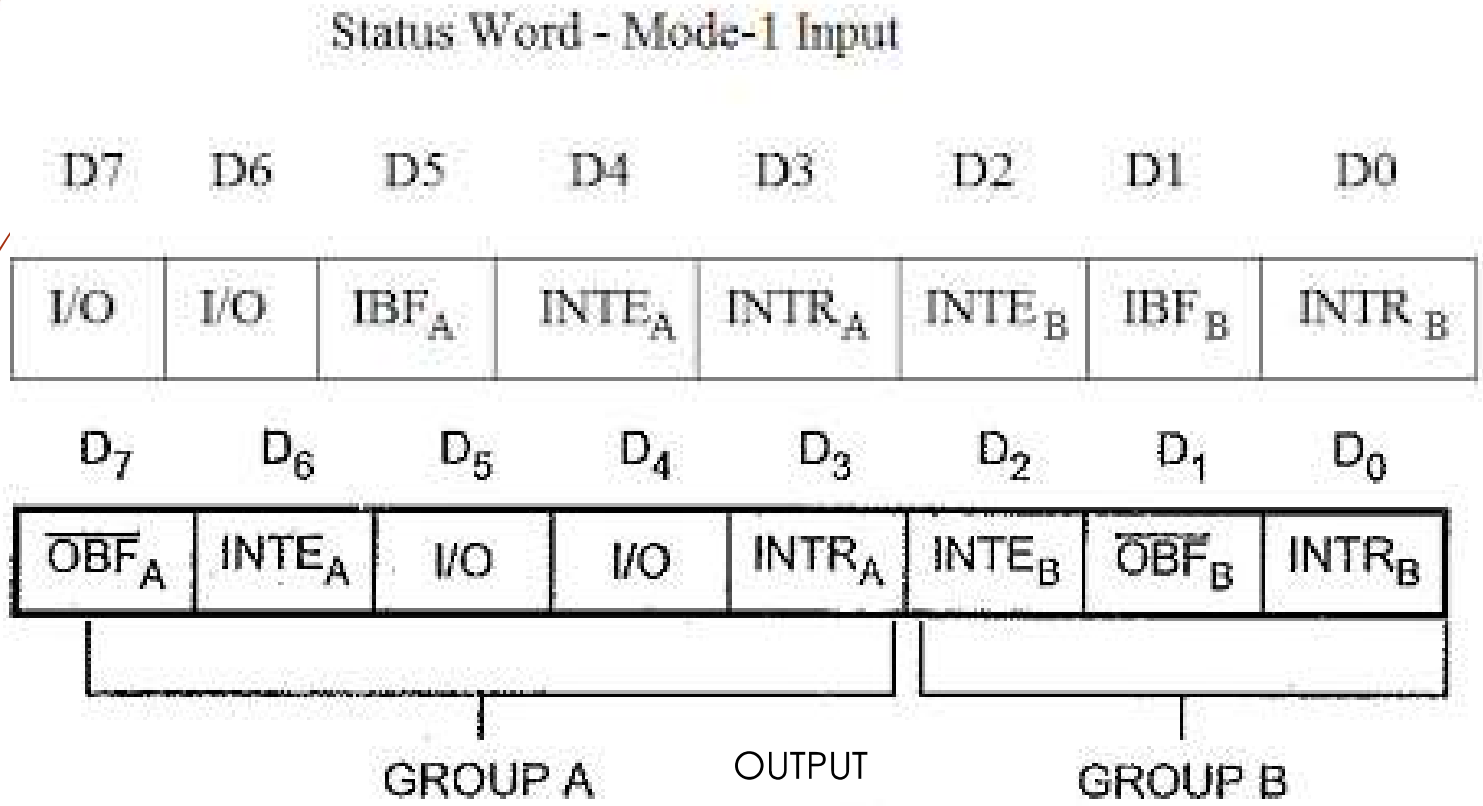


Port A,B – Strobed output

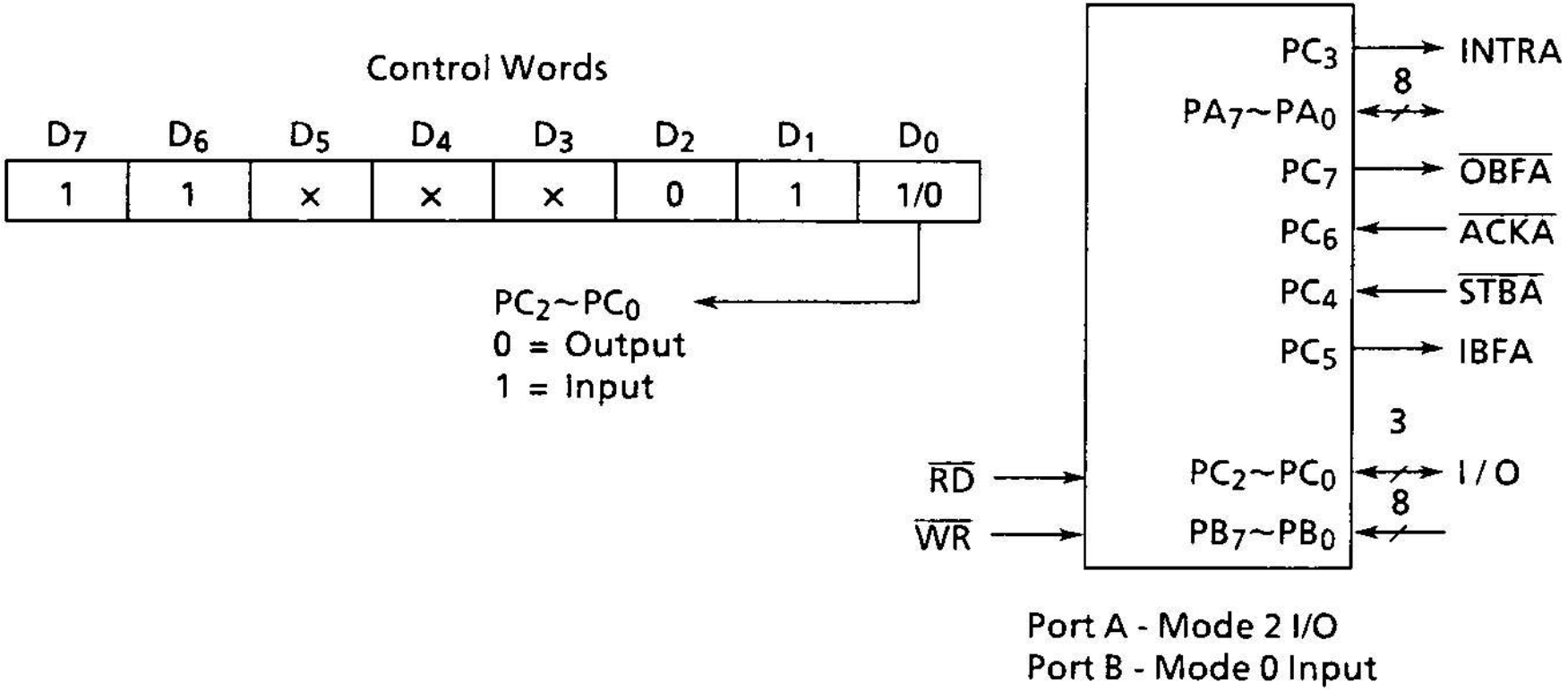


Polling versus interrupts

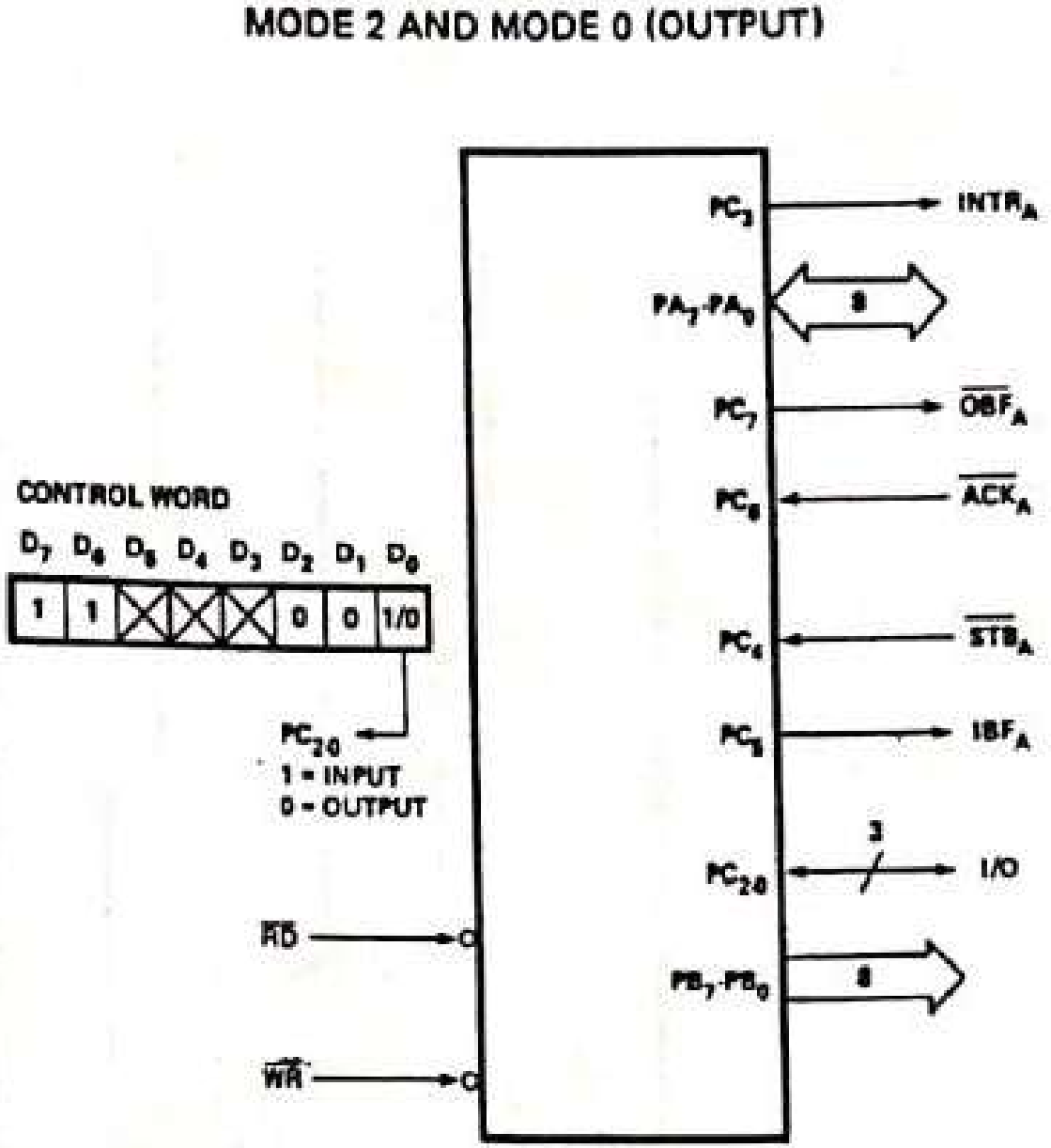
- 8255 mode 1 status word format
  - This byte is read via an input read from port C



8255 – mode 2


Control Words
D7 D6 D5 D4 D3 D2 D1 D0
1 1 × × × 0 1 1/0
PC2~PC0
0 = Output
1 = Input
PC3
INTRA
8
PA7~PA0
PC7
OBFA
PC6
ACKA
PC4
STBA
PC5
IBFA
3
RD
PC2~PC0
I / O
8
WR
PB7~PB0
Port A - Mode 2 I/O
Port B - Mode 0 Input

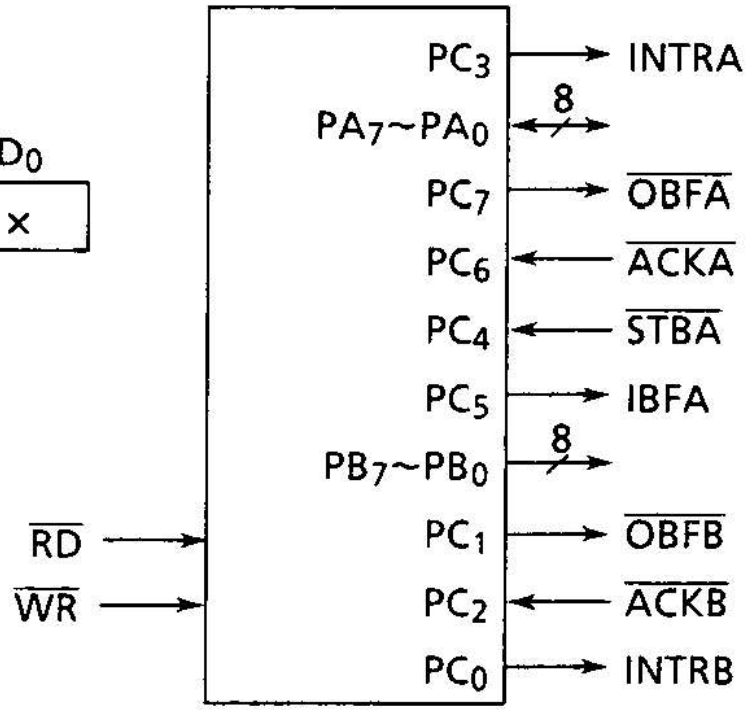
8255 – mode 2


MODE 2 AND MODE 0 (OUTPUT)
CONTROL WORD
D7 D6 D5 D4 D3 D2 D1 D0
1 1 X X X 0 0 1/0
PC2-0
1 = INPUT
0 = OUTPUT
RD
WR
PC3
INTRA
PA7-PA0
8
PC7
OBFA
PC6
ACKA
PC4
STBA
PC1
IBFA
3
PC2-0
I/O
PB7-PB0
8

8255 – mode 2

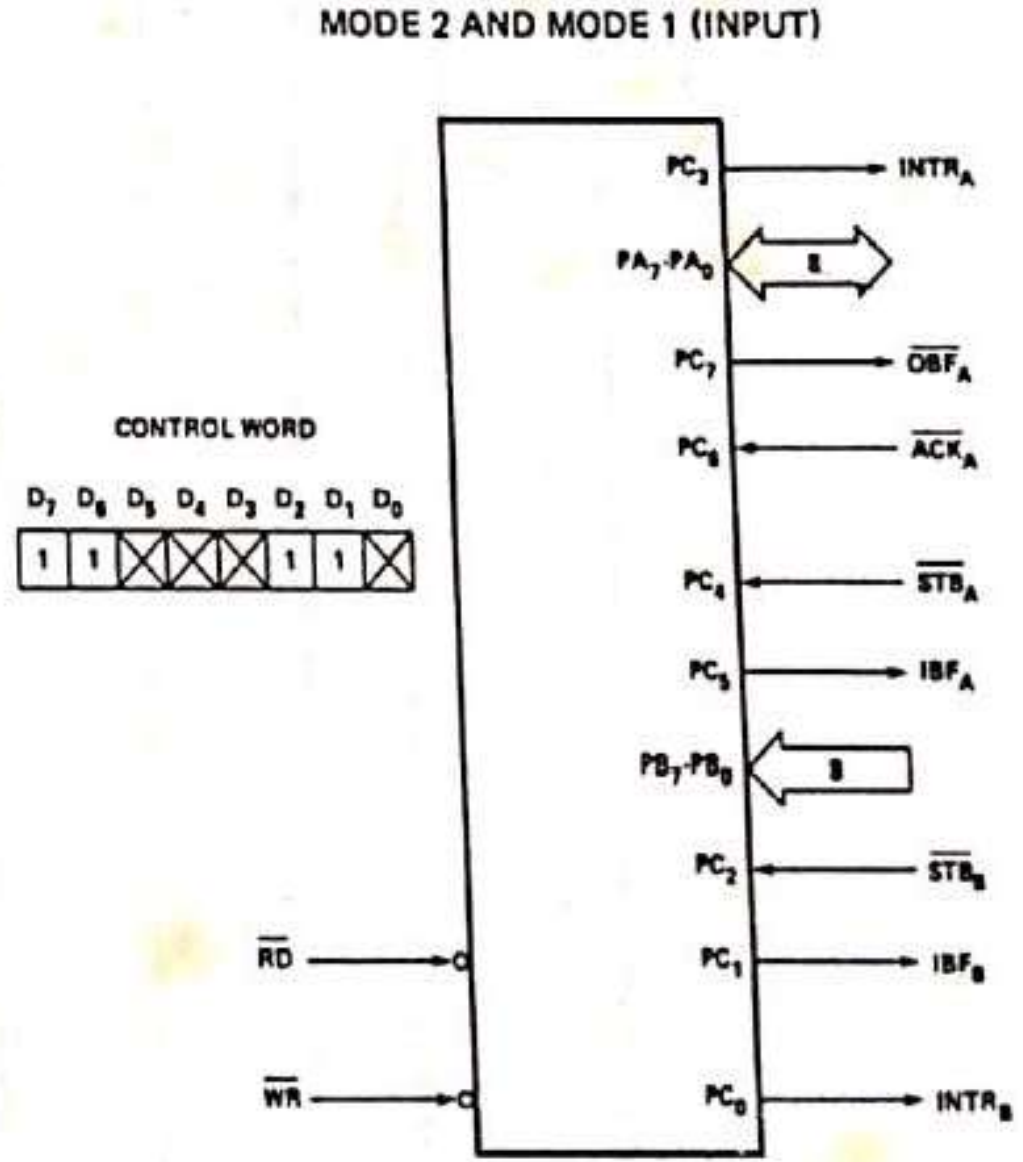
Control Words

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	×	×	×	1	0	×

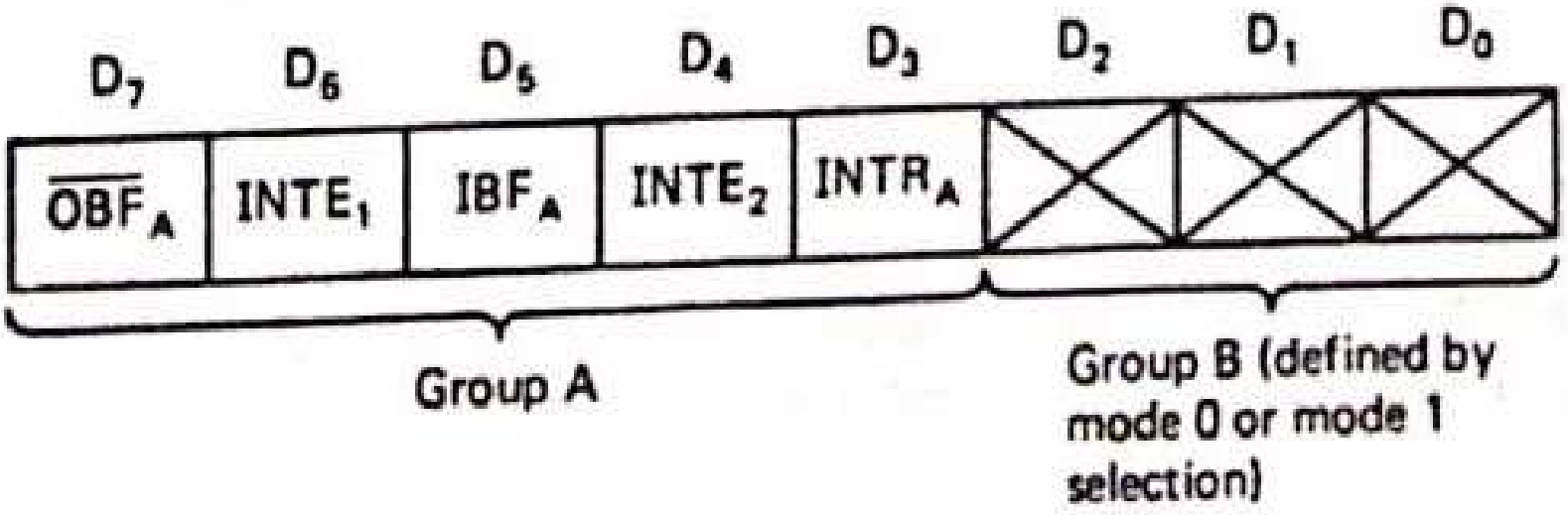


Port A - Mode 2 I/O
Port B - Mode 1 Output

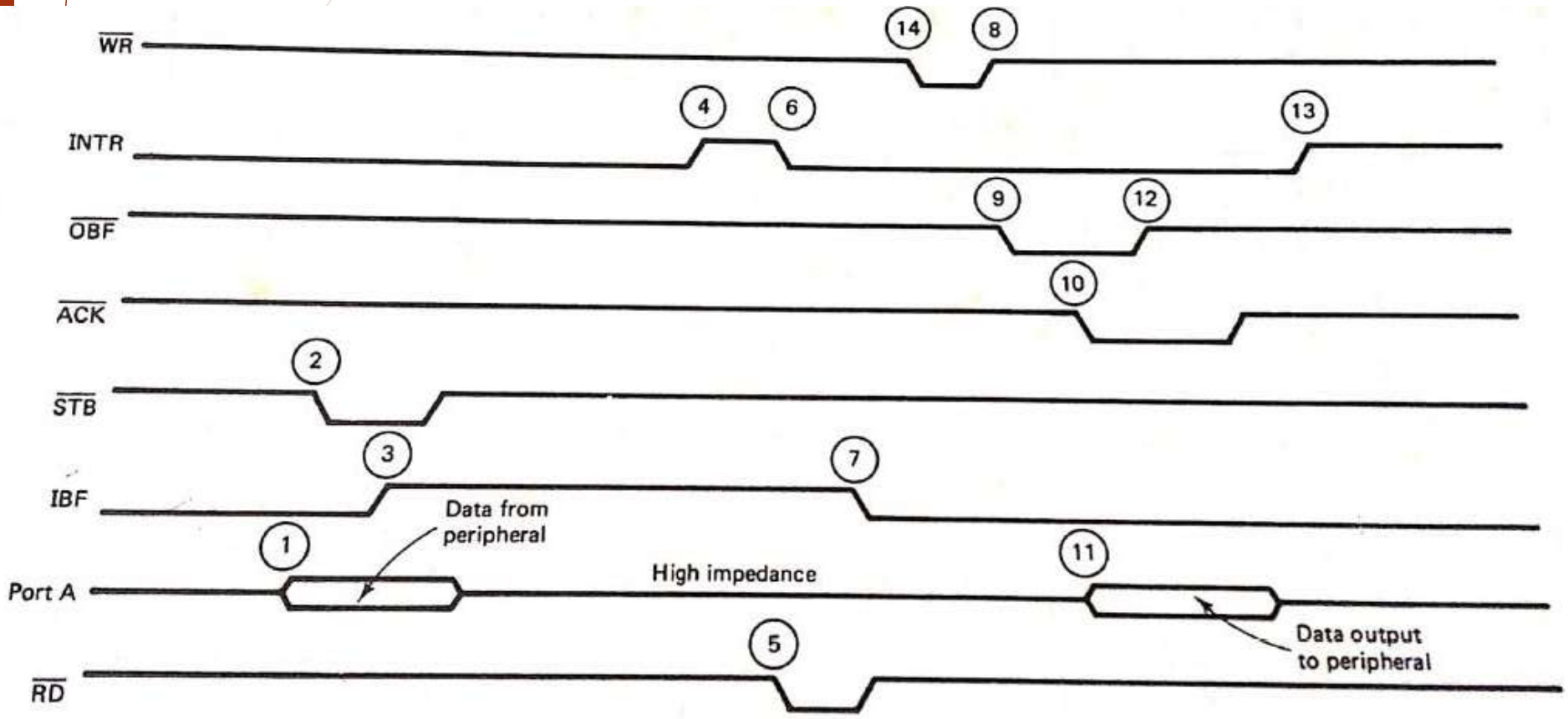
8255 – mode 2


MODE 2 AND MODE 1 (INPUT)
CONTROL WORD
D7 D6 D5 D4 D3 D2 D1 D0
1 1 1 1
PC3
INTRA
PA7-PA0
8
PC7
OBFA
PC6
ACKA
PC4
STBA
PC5
IBFA
PB7-PB0
8
PC2
STBB
RD
PC1
IBFB
WR
PC0
INTRB

8255 – mode 2 status word



8255 – mode 2 timing diagram



8255 – mode 2

Input port timing. Figure 9.16 is a timing diagram for mode 2 illustrating the sequence of events as a data byte is first transferred to the 8255 by the peripheral and then back to the peripheral by the 8255. The numbers in the diagram are keyed to the explanation. We begin with the peripheral outputting a byte to the 8255.

1. Data is output by the peripheral.
2. The peripheral applies a $\overline{\text{STB}}$ pulse to the 8255.
3. When the data is latched, IBF goes high.
4. After $\overline{\text{STB}}$ returns high with IBF still set, INTR goes high, requesting an interrupt if this feature is used.
5. Polling or interrupts can now be used to service the peripheral. The 8255 buffer is read when $\overline{\text{RD}}$ goes low.
6. The falling edge of $\overline{\text{RD}}$ resets INTR.
7. The rising edge of $\overline{\text{RD}}$ resets IBF.

8255 – mode 2

Output port timing. The following sequence occurs as the processor outputs a byte of data to the peripheral through the 8255.

8. Data is output by the processor and latched by the 8255 (note that the peripheral bus is in a high-impedance state at this time).
9. The rising edge of $\overline{WR}$ causes $\overline{OBF}$ to switch low ("the output buffer is full").
10. The peripheral acknowledges $\overline{OBF}$ by causing $\overline{ACK}$ to go low.
11. On the falling edge of $\overline{ACK}$ the 8255 releases its data onto the bus.
12. $\overline{OBF}$ returns high ("the output buffer is empty").
13. The rising edge of $\overline{ACK}$ sets INTR, requesting an interrupt if this feature is used.
14. Polling or interrupts can now be used to write the next data byte to the 8255.