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SECOND YEAR ENGINEERING

**Microprocessor Previous Year Question Paper from
December 2014 to May 22**

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(3 Hours)

[Total Marks : 80]

- N. B. : (1) Q. 1 is **compulsory**.
 (2) From remaining answer any **three** questions.
 (3) Draw neat diagram wherever necessary.

1. (a) Draw and explain timing diagram for read operation in minimum mode of 8086. 5
 (b) Explain I/O related addressing mode of 8086. 5
 (c) Write down features of super SPARC processor. 5
 (d) Enlist the instruction pairing rules for U and V pipeline in Pentium. 5
2. (a) Explain address translation mechanism used in protected mode of 80386. 10
 (b) Write assembly language program for 8086 to exchange contents of two memory blocks. 10
3. (A) Design 8086 microprocessor based system with following specifications 10
 - (a) Microprocessor 8086 working at 10 MHz in minimum mode
 - (b) 32 KB EPROM using 8 KB chips
 - (c) 16 KB SRAM using 4 KB chips
 Explain the design along with memory address map.
 (B) Explain how the flushing of pipeline problem is minimized in Pentium architecture. 10
4. (a) Interface DMA controller 8237 with 8086 microprocessor. Explain different data transfer modes of 8237 DMA controller. 10
 (b) Differentiate between real mode and protected mode. 10
5. (a) Draw & explain block diagram of 8259 PIC. 10
 (b) Draw a segment descriptor format and explain different fields. 10
6. Write short note on any **four** :- 20
 - (a) Code cache organization of Pentium.
 - (b) State the use of RF, TF, VM, NT, IOPL flag bits
 - (c) Data types supported by SPARC processor
 - (d) Advantages of memory segmentation in 8086.
 - (e) Maximum mode of 8086
 - (f) Control word register of 8255.

T.E.(V)(CBG3) (Computer's)
Microprocessor

19/5/15

QP Code : 3321

Time 3 hrs

Max Marks 80

Notes: 1. Q. 1 is compulsory

2. From remaining answer any 3 questions.

3. Draw neat diagram wherever necessary

- Q.1 A) Draw and explain timing diagram for write operation in minimum mode of 8086. 5
B) List operating modes of 8253. 5
C) Write down features of Pentium processor. 5
D) Write the instruction issue algorithm used in Pentium. 5
- Q.2 A) Explain protection mechanism used in 80386. 10
B) Write assembly language program for 8086 to reverse a string of 10 characters. 10
- Q.3 A) Design 8086 microprocessor based system with following specification 10
a) Microprocessor 8086 working at 8 MHz in maximum mode
b) 32 KB EPROM using 16 KB chips
c) 16 KB SRAM using 8 KB chips
Explain the design along with memory address map.
B) Explain branch prediction logic used in Pentium. 10
- Q.4 A) i. Explain different data transfer modes of 8237 DMA controller. 05
A) ii. Explain Interfacing of 8259 with 8086 in minimum mode. 05
B) Differentiate between real mode and protected mode. 10
- Q.5 A) Compare 8086, 80386 and Pentium. 10
B) Draw architecture of Super SPARC processor and explain in short. 10
- Q.6 Write note on any 4. 20
a) Data cache organization of Pentium.
b) State use of control flags of 8086
c) Data types supported by SPARC processor
d) Advantages of memory segmentation in 8086.
e) Mode 1 of 8255 for input operation

(3 Hours)

QP Code : 5609
[Total Marks : 80]

Note the following instructions.

1. Question no.1 is compulsory.
2. Solve any three questions out of remaining five questions.
3. Assume suitable data if necessary.

-
1. (a) Write short note on 8288 Bus Controller. (5)
(b) Explain the following instructions in 8086 : LAHF and STOSB (5)
(c) Design interfacing of 8282 latches to 8086 system. (5)
(d) Explain in brief Protection Mechanism in 80386DX Processor. (5)
 2. (a) Explain Memory Management in details in 80386DX processor (10)
(b) Design 8086 based system with following specifications (10)
 - (i) 8086 in minimum mode working at 8MHz
 - (ii) 32KB EPROM using 16KB devices.
 - (iii) 64KB SRAM using 32KB devices.
 3. (a) Explain with block diagram working of 8255 PPI. (10)
(b) What is segmentation? What are the advantages of segmentation? (5)
(c) Differentiate between minimum mode and maximum mode in 8086. (5)
 4. (a) Explain branch prediction logic used in Pentium. (10)
(b) Compare Pentium 2, Pentium 3 and Pentium 4 processors. (10)
 5. (a) Explain different data transfer modes of 8237 DMA controller. (10)
(b) Explain the architecture of Super SPARC processor with a neat diagram. (10)
 6. Write short note on (5)
 - (a) 8087 Math Coprocessor.
 - (b) Generation of Reset signals in 8086 based system. (5)
 - (c) Comparative Study of multicore i3, i5 and i7 processors. (5)
 - (d) Mixed Language Programming. (5)
-

Sem: II (Comp) CB45
Microprocessor

17/5/16

QP Code : 31091

(80 Marks) (3 Hours)

- Question no. 1 is compulsory.
- Answer any three questions from question no. 2 – 6.
- Assume suitable data, if necessary.

- Q.1. Answer following questions in brief.
- a. Explain programming model of 8086. (05)
 - b. Explain V86 mode of 80386DX. (05)
 - c. Explain, in brief, pipeline stages on Pentium processor. (05)
 - d. Explain, in brief, data format supported by SuperSparc processor. (05)
- Q.2. a. Explain memory segmentation with pros and cons. (08)
- b. Draw and explain the block diagram of 8255. Also, explain different operating modes of 8255. (12)
- Q.3. a. Design 8086 based minimum mode system for following requirements: (12)
- I. 256 KB of RAM using 64 KB x 8-bit device
 - II. 128 KB of RAM using 64 KB x 8-bit device
 - III. Three 8-bit parallel ports using 8255
 - IV. Support for 8 interrupts
- b. Explain, in brief, cache organization of Pentium processor. (08)
- Q.4. a. Draw and explain architecture of SuperSparc processor. (12)
- b. Discuss, in brief, protection mechanism of 80386DX. (08)
- Q.5. a. Draw and explain architecture of Pentium processor. (10)
- b. Draw timing diagram of read operation on 8086 based system. (10)
- Q.6. Write short notes on (05)
- a. 8089 I/O Processor (05)
 - b. Comparison between i5 and i7 (05)
 - c. SuperSparc registers (05)
 - d. 8259 – PIC (05)

Computer Networks.

QP Code : 31134

(3 Hours)

Total marks : 80

Note:

- Question No. 1 is compulsory.
- Attempt any Three questions out of remaining questions.
- Make suitable assumptions whenever necessary.

Q 1:

[4 X 5]

- a) Compare connection oriented and connectionless services.
- b) Explain in short Subnetting.
- c) Explain in short different framing Methods.
- d) Explain in short TCP/IP Model.
- e) What is the use of SSH ?

Q 2:

[10]

- a) Explain any four functions of Data Link layer with example.
- b) What is IPv4 protocol? Explain the IPv4 Header format with diagram.

[10]

Q 3:

[10]

- a) Explain Classless Inter Domain Routing (CIDR).
- b) Discuss the quality of service parameters in computer network.

[10]

Q 4:

- a) What are the steps involved in link state routing. Explain the contents and requirements of link state packets.

[10]

- b) Compare Open Loop congestion control, Closed Loop congestion control.

[10]

Q 5:

- a) Write a Program for client-server application using Socket Programming(TCP).

[10]

- b) An ISP is granted a block of addresses starting with 150.80.0.0/16.

The ISP wants to distribute these blocks to 2600 customers as follows.

a. The first group has 200 medium-size businesses; each needs 128

b. The second group has 400 small businesses; each needs 16

c. The third group has 2000 households; each needs 4 addresses. Design the subblocks and give the slash notation for each subblock. Find out how many addresses are still available after these allocations.

[10]

Q 6: Write short notes on the following.

[5 X 4]

- a) Virtual LAN
- b) FDDI
- c) BGP
- d) SNMP

(3 Hours)

[Total Marks : 100] 80



- N.B. :**
- (1) Question No.1 is compulsory.
 - (2) Answer ~~any four~~^{Three} questions from Q.No.1 to Q.No.7.
 - (3) Figures to the right indicate full marks.
 - (4) Assume suitable data if required.

1. (a) What is purpose of maximum mode of 8086? Give suitable example. 5
 (b) Explain flag register of 80386DX. 5
 (c) Compare Pentium, Pentium II and Pentium III processors. 5
 (d) List different addressing modes of 8086. 5
2. (a) Design 8086 based system for following requirements : 10
 - (i) Clock frequency 5 MHz
 - (ii) 512 KB RAM using 32 KB x 8
 - (iii) 256 KB ROM using 32 KB x 8
 (b) Draw and explain block diagram of 8253. 10
3. (a) Draw and explain interfacing of math coprocessor (8087) with 8086. 10
 (b) Explain data segment descriptor with neat diagram. 10
4. (a) Explain, in brief, branch prediction mechanism is on Pentium processor. 10
 (b) Explain, with neat diagram, cache memory organization is supported by Pentium processor. 10
5. (a) Explain, in brief, data formats supported by SuperSparc processor. 10
 (b) Explain the need of DRAM controller for interfacing DRAM with 8086. 10
 Draw and explain interfacing of DRAM controller with 8086.
6. Write short note on : 10
 - (a) Mixed language programming 5
 - (b) Virtual 86 mode of 80386DX 5
 - (c) 82888 Bus Controller 5
 - (d) Control registers of 80386DX 5

Q.P. Code : 581201**(3 Hours)****[Total Marks : 100]**

N.B. : (1) Question No.1 is **compulsory**.

- (2) Answer **any four** questions from Q.No.2 to Q.No.7.
- (3) **Figures to the right** indicate **full marks**.
- (4) Assume suitable **data if required**.

- | | |
|---|-----------|
| 1. (a) What is memory segmentation? State advantages of memory segmentation. | 5 |
| (b) What is GDT? Explain structure of GDT. | 5 |
| (c) Explain integer pipeline of Pentium processor? | 5 |
| (d) Briefly explain string instructions of 8086. | 5 |
| 2. (a) Design 8086 based system for following requirements : | 10 |
| (i) Clock frequency 5 MHz | |
| (ii) 512 KB RAM using 32 KB x 8 | |
| (iii) 256 KB ROM using 32 KB x 8 | |
| (b) Draw and explain block diagram of 8253. | 10 |
| 3. (a) Explain DMA data transfer modes in brief. | 10 |
| (b) Explain, with neat diagram, address translation mechanism implemented on 80386DX. | 10 |
| 4. (a) Explain, with neat diagram, cache memory organization is supported by Pentium processor. | 10 |
| (b) Draw and explain block diagram of Pentium processor. | 10 |
| 5. (a) Draw and explain block diagram of SuperSparc processor. | 10 |
| (b) Explain interrupt structure of 8086. | 10 |
| 6. Write short note on : | |
| (a) Mixed language programming | 5 |
| (b) Virtual 86 mode of 80386DX | 5 |
| (c) Branch prediction logic | 5 |
| (d) Control registers of 80386DX | 5 |

Time 3 hrs.

Max Marks: 80

Notes: 1. Q. 1 is compulsory
2. From remaining answer any 3 questions.
3. Draw neat diagram wherever necessary

- | | | |
|------|---|------------------|
| Q.1 | a) Write instruction issue algorithm used in Pentium.
b) Draw format of selector and explain its field.
c) Explain power on reset circuit used in 8086 system.
d) Discuss control word format for Bit Set Reset (BSR) mode of 8255 PPI. | 5
5
5
5 |
| Q.2 | a) Explain maximum mode of 8086 microprocessor.
b) Interface three 8259s with 8086 in minimum mode and explain its functionality in fully nested mode. | 10
10 |
| Q.3 | a) How flushing problem is minimised in Pentium? Explain.
b) Draw block diagram of Super SPARC and explain in brief. | 10
10 |
| Q.4. | a) Discuss data cache organisation of Pentium.
b) Explain address translation mechanism used in 80386 DX. | 10
10 |
| Q.5 | a) Design 8086 based system with following specifications.

i) 8086 is working in minimum mode at 10 MHz.
ii) 8KB EPROM using 2 KB chips.
iii) 16 KB SRAM using 8 KB chips.

Discuss system with memory address map.

b) Draw and explain EFLAG register format of 80386 DX. | 10
10 |
| Q.6 | Answer any four.

a) Write addressing modes of following instructions of 8086.

i) MOV al, [bx + si] ii) AND cl, [2000]
iii) ADD ax, [bx + si + 2000] iv) IN al, dx
v) POP BX

b) Draw and discuss timing diagram for read operation in minimum mode of 8086.
c) Explain memory segmentation of 8086.
d) Explain in short data types of SPARC.
e) List features of 8253. | 20 |

(Time: 3Hrs)

Max Marks: 80



- NB: 1. Question No.1 Compulsory.
 2. Solve any THREE from Q.2 to Q.6
 3. Assume suitable data whenever necessary with justification.

- Q1. Solve any FOUR.
- (A) Explain Memory banks for 8086 Processor (5)
 - (B) Draw and Explain Floating Point Pipeline for Pentium Processor. (5)
 - (C) Explain Multitasking and Protection for 80386 processor (5)
 - (D) Explain Flag Register bits of 8086. (5)
 - (E) Explain Virtual Mode (VM86) 80386 Processor. (5)
- Q2. (A) Explain Interrupt Structure of 8086 Processor. (10)
 (B) Explain PPI 8255 with block diagram. (10)
- Q3. (A) Draw and Explain write operation timing diagram for maximum mode. (10)
 (B) Explain Operating Modes of PIC 8259. (10)
- Q4. (A) Explain following instructions.
 DAA, AAA, XLAT, LAHF (10)
 (B) Explain Segment Descriptor of 80386 Processor. (10)
- Q5. (A) Explain Gate type of descriptors. (10)
 (B) Explain Data Cache architecture for Pentium Processor. (10)
- Q6. (A) Explain SPARC Processor with block diagram. (10)
 (B) Explain with block diagram PIT 8254 (10)

-----XXX-----

(3Hrs)

Max Marks: 80



- NB: 1. Question No.1 Compulsory.
2. Solve any THREE from Q.2 to Q.6
3. Assume suitable data whenever necessary with justification.

Q1 Answer any FOUR questions

- | | |
|---|----|
| (A) Explain programming model of 8086. | 05 |
| (B) Explain DAA and XLAT instructions of 8086 Processor. | 05 |
| (C) Explain control registers of 80386. | 05 |
| (D) Explain assembler directives. | 05 |
| (E) Draw and Explain Floating Point Pipeline for Pentium Processor. | 05 |
| 2. (A) Explain PPI 8255 with block diagram. | 10 |
| (B) Draw and explain block diagram of 8254 – PIT. | 10 |
| Q3. (A) Design 8086 based system with following specifications. | 10 |
| (1) 8086 working at 8MHz at minimum mode | |
| (2) 256KB RAM using 64KB X 8 device | |
| (3) 128KB EPROM using IC 27128. | |
| (B) Explain architecture of 8086 Processor with example. | 10 |
| Q4. (A) What is multitasking? Explain how task switching is implemented on 80386 processor. | 10 |
| (B) Explain, in brief, protection mechanism implemented on 80386. | 10 |
| Q5. (A) Explain, with neat diagram, register window implementation on Sun Supersparc processor. | 10 |
| (B) Explain branch prediction logic of Pentium processor. | 10 |
| Q6. Write short notes on | |
| (A) Page translation mechanism on 80386DX | 05 |
| (B) Register window on Supersparc processor | 05 |
| (C) Operating modes of 8254 | 05 |
| (D) 8086 addressing modes | 05 |

(3Hrs)

Max Marks: 80

- NB: 1. Question No.1 Compulsory.
2. Solve any THREE from Q.2 to Q.6
3. Assume suitable data whenever necessary with justification.

Q1 Answer any FOUR questions

- (A) Explain Memory Bank in 8086 Processor. **05**
- (B) Give different bits of Control Register-0 (CRO) of 80386. **05**
- (C) Draw and Explain Floating Point Pipeline for Pentium Processor. **05**
- (D) Explain assembler directives. **05**
- (E) Explain DAA and XLAT instructions of 8086 Processor. **05**

- Q2.** (A) Explain architecture of 8086 Processor with example. **10**
- (B) Explain PPI 8255 with block diagram. **10**

- Q3.** (A) Design 8086 based system with following specifications. **10**
(1) 8086 working at 8MHz at minimum mode
(2) 64KB RAM using 32KB X 8 device
(3) 64KB EPROM using IC 27128.

- (B) Explain Operating Modes of PIC 8259. **10**

- Q4.** (A) Explain 80386 Processor descriptor and it's content. **10**
- (B) Explain Superscalar and Branch Prediction for Pentium Processor. **10**

- Q5.** (A) Write details note on Multitasking and Protection. **10**
- (B) Explain Instructions pairing rules for Pentium Processor. **10**

- Q6.** (A) Explain SPARC Processor with block diagram. **10**
- (B) Explain with block diagram PIT 8254. **10**

MICROPROCESSORS

30 MAY 2022

University of Mumbai
Examination Summer 2022

QP: 93977

SEN: IV

Time: 2 hour 30 minutes

COMPUTER ENGG

Max. Marks: 80

Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	8086 supports software Interrupts
Option A:	2
Option B:	64K
Option C:	256
Option D:	8
2.	In 8086 size of pre fetch queue is
Option A:	6 Byte
Option B:	4 Byte
Option C:	4 Bit
Option D:	2 Byte
3.	The instruction that unconditionally transfers the control of execution to the specified address is
Option A:	JMP
Option B:	IRET
Option C:	RET
Option D:	CALL
4.	In PUSH instruction, after each execution of the instruction, the stack pointer is
Option A:	incremented by 1
Option B:	decremented by 1
Option C:	incremented by 2
Option D:	decremented by 2
5.	stores the bits required to mask the IR lines of 8259
Option A:	ISR
Option B:	IMR
Option C:	IRR
Option D:	PR
6.	The bus is available when the DMA controller receives the signal
Option A:	HRQ
Option B:	HLDA
Option C:	DACK
Option D:	INTA
7.	Which control registers of 80385 are associated with paging mechanism?
Option A:	CR0, CR2, CR3
Option B:	CR1, CR2, CR3
Option C:	CR0, CR1 CR2

Option D:	CR0, CR1 CR2, CR3
8.	How many flags are active in flag register of 80386?
Option A:	9
Option B:	12
Option C:	13 .
Option D:	10
9.	What lead to the development of MESI and MEI protocol ?
Option A:	Cache size
Option B:	Cache Coherency
Option C:	Bus snooping
Option D:	Number of caches
10.	Hyperthreading uses the concept of
Option A:	Simultaneous multithreading .
Option B:	Distributed decoding
Option C:	Multiple switching
Option D:	Pipelining

Q2	Solve any Two Questions out of Three	10 marks each
A	Explain and draw IVT? Differentiate between hardware and software interrupts?	
B	Explain descriptors and paging mechanism in protected mode of 80386 ?	
C	Explain the Initialization command words (ICWs) and Operational command words(OCWs) of the 8259 PIC.	

Q3	Solve any Two Questions out of Three	10 marks each
A	Write an 8086 assembly language program to print the flag registers	
B	Design 8086 microprocessor based system working in minimum mode with the following specifications. I) 8086 microprocessor working at 8 MHz. II) 16 KB EPROM using 8K devices. Clearly show memory map with address range. Draw a neat schematic.	
C	Explain protection mechanism of 80386 with diagram.	

Q4	Solve any Two Questions out of Three	10 marks each
A	Draw and explain timing diagram of memory read and memory write operation in minimum mode.	
B	Explain Pentium 4 Net burst micro architecture and write a note on hyperthreading	
C	Explain Integer and Floating-Point Pipeline of Pentium.	