8085 CLASSIFICATION OF INSTRUCTIONS

The Instruction Set of 8085 is classified into the following 5 groups:

1) Data Transfer Group

This group of instructions transfer data from one place to another place.
The data can be transferred from Register to Register, Memory to Register & Register to Memory

Eg: **MOV A, B** ; Content of B register is transferred to accumulator.
MVI A, 03H ; Move immediately 03 into the accumulator.

2) Arithmetic Group

This group of instructions performs arithmetic operation on the data.
The arithmetic operation may be data addition, subtraction, increment, decrement etc.

Eg: **ADI 03H** ; Add immediately 03 with the content of accumulator, store
; result in accumulator.
SUB B ; Subtract content of B Register from the accumulator, store
; result in accumulator.

3) Logic Group

This group of instructions performs logical operations on the data.
These instructions include AND, OR, EX-OR etc.

Eg: **ANI 03H** ; AND logically 03 with the content of accumulator, store result
; in accumulator.
ORA B ; OR logically content of B Register with the accumulator, store
; result in accumulator.

4) Branch Group

These instructions change the sequence of flow of the program.
There are two types of Branch Instructions

Conditional Branch instructions
In this type, control is transferred to another memory location only if a particular condition is satisfied.
Eg: **JNZ 4000** ; Program Control is transferred to memory location 4000 provided result of
; the previous operation is non-zero else control continues sequentially.

Unconditional Branch instruction
In this type, control is transferred to another memory location without any condition.
Eg: **JMP 4000** ; Simply control is transferred to the memory location 4000.

5) Stack, IO and Machine Control Instruction

These instructions control the STACK (Push and Pop), I/O (Input and Output) and Machine hardware.

Eg: **PUSH B** ; The content of BC register pair is pushed to the stack, at the
; location pointed by SP.
IN 80H ; The data from the input device at port address 80 is placed in
; accumulator.

INSTRUCTION SET OF 8085

Common Notations:

1) Addr → 16 bit address.
2) Data → 8 or 16 bit data.
3) R → one of the registers.
4) Rp → register pair. BC pair is called B, DE → D and HL → L

Special Notes:
In the explanation of every instruction, I have mentioned its machine cycles and T-states. You will understand this part once you watch the two videos of timing diagrams

DATA TRANSFER GROUP

1) MOV $R_{Destination}$, R_{source}

The contents of register $\mathbf{R}_{source}$ is copied into register $\mathbf{R}_{Destination}$.
Eg: MOV A,B ; A ← B

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Addr. Mode	Flags Affected	Cycles	T-States
Register	None	1	4

2) MOV R, M

The contents of the memory location pointed by HL (memory pointer) is copied into register R.
Eg: MOV B,M ; B ← [[HL]] i.e. B ← M

Addr. Mode	Flags Affected	Cycles	T-States
Indirect	None	2	7

3) MOV M, R

The contents of register R is copied into the memory location pointed by HL (memory pointer).
Eg: MOV M,B ; [[HL]] ← B i.e. M ← B

Addr. Mode	Flags Affected	Cycles	T-States
Register	None	2	7

4) MVI R, 8-bit data

The 8-bit data is immidiately moved into the register specified in the instruction.
Eg: MVI C, 23 ; C ← 23H

Addr. Mode	Flags Affected	Cycles	T-States
Immidiate	None	2	7

5) LXI Rp, 16-bit data

The 16-bit data is immidiately moved into the register pair specified in the instruction.
Eg: MVI B, 2300H ; BC ← 2300H i.e. B← 23, C← 00

Addr. Mode	Flags Affected	Cycles	T-States
Immidiate	None	3	10

6) MVI M, 8-bit data

The 8-bit data is immidiately moved into the memory location pointed by HL (memory pointer).
Eg: MVI M, 23 ; [[HL]] ← 23H

Addr. Mode	Flags Affected	Cycles	T-States
Immediate	None	3	10

7) LDA 16-bit address

The accumulator is loaded withb the contents of the memory location having the given address.
Eg: LDA 2000H ; A ← [2000]

Addr. Mode	Flags Affected	Cycles	T-States
Direct	None	4	13

8) STA 16-bit address

The accumulator is stored into the memory location having the given address.
Eg: STA 2000H ; [2000] ← A

Addr. Mode	Flags Affected	Cycles	T-States
Direct	None	4	13

9) LHLD 16-bit address

The HL pair is loaded with the contents of the loactions ppointed by the given address and address + 1. ☺ In case of doubts, contact Bharat Sir: - 98204 08217.
Eg: LHLD 2000 ; HL ← [2000] & [2001] i.e. L ← [2000], H ← [2001]

Addr. Mode	Flags Affected	Cycles	T-States
Direct	None	5	16

10) SHLD 16-bit address

The HL pair is stored into the loactions ppointed by the given address and address + 1.
Eg: SHLD 2000 ; [2000] & [2001] ← HL i.e. [2000] ← L, [2001] ← H

Addr. Mode	Flags Affected	Cycles	T-States
Direct	None	5	16

11) LDAX rp

The accumulator is loaded with the contents of memory location pointed by value of the given register.

Eg: LDAX B ; A ← [[BC]] i.e. if [BC] = 2000, A gets the value from location
; 2000 i.e. A ← [2000]

Addr. Mode	Flags Affected	Cycles	T-States
Indirect	None	2	7

12) STAX rp

The accumulator is stored into the location pointed by value of the given register.

Eg: STAX B ; [[BC]] ← A i.e. if [BC] = 2000, location 2000 will get the
; value of A i.e. [2000] ← A.

Addr. Mode	Flags Affected	Cycles	T-States
Indirect	None	2	7

13) PCHL

The Program Counter gets the contents of the HL register pair.
This statement causes a branch in the sequence of the program.

Eg: PCHL ; PC ← HL

Addr. Mode	Flags Affected	Cycles	T-States
Register	None	1	**6**

14) SPHL

The Stack Pointer gets the contents of the HL register pair.
This statement reloates the stack in the 64 KB memory.

Eg: SPHL ; SP ← HL

Addr. Mode	Flags Affected	Cycles	T-States
Register	None	1	**6**

15) XCHG

This instruction exchanges the contents of HL pair and DE pair.

Eg: XCHG ; HL ←→ DE
#Please refer Bharat Sir's Lecture Notes for this ...

Addr. Mode	Flags Affected	Cycles	T-States
Register	None	1	4

16) XTHL

This instruction exchanges the DE pair with the contents of location pointed by the SP and SP+1.

Eg: XTHL ; HL ←→ [[SP]] and [[SP]+1]
; i.e. if [SP]=2000 then L ←→ [2000] and H ←→ [2001]
#Please refer Bharat Sir's Video fo rmore on this ...

Addr. Mode	Flags Affected	Cycles	T-States
Register	None	5	16