1	**The Intel Microprocessors 8086 Architecture**		8
	1.1	8086CPU Architecture,	
	1.2	Programmer's Model	
	1.3	Functional Pin Diagram	
	1.4	Memory Segmentation	
	1.5	Banking in 8086	
	1.6	Demultiplexing of Address/Data bus	
	1.7	Functioning of 8086 in Minimum mode and Maximum mode	
	1.8	Timing diagrams for Read and Write operations in minimum and maximum mode	
	1.9	Interrupt structure and its servicing	

1. Draw and explain timing diagram for read operation in minimum mode of 8086
2. Draw a segment descriptor format and explain different fields
3. Advantages of memory segmentation in 8086
4. Maximum mode of 8086
5. Draw and explain timing diagram for write operation in minimum mode of 8086
6. State use of control flags in 8086
7. Explain the following instructions in 8086 : LAHF and STOSB.
8. Design interfacing of 8282 latches in 8086 system.
9. What is segmentation? What are the advantages of segmentation.
10. Differentiate between minimum and maximum mode in 8086
11. Explain programming model of 8086
12. Explain memory segmentation with pros and cons
13. Design 8086 based minimum mode system for following requirements: a. 256kb of ram using 64 kb x 8 bit device. B. 128kb of ram using 64kb x 8 bit device c. three 8 bit parallel ports using 8255 d. support of 8 interrupts
14. Explain power on reset circuit used in 8086 system
15.

2	**Instruction Set and Programming**		**6**
	2.1	Addressing Modes	
	2.2	Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions	
	2.3	Assembler Directives and Assembly Language Programming, Macros, Procedures	

1. Explain i/o related addressing mode of 8086
2. Write assembly language program for 8086 to reverse a string of 10 characters.
3. Generation of reset signals in 8086 based systems.
4. Mixed language programming

3	**Memory and Peripherals interfacing**		8
	3.1	Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute	
	3.2	8255-PPI-Block diagram, CWR, operating modes, interfacing with 8086.	
	3.3	8257-DMAC-Block diagram, DMA operations and transfer modes.	
	3.4	Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.	

1. Write assembly language program for 8086 to exchange contents of two memory blocks
2. Design 8086 microprocessor based system with foll specification a. microprocessor 8086 working at 10 MHz in minimum mode b. 32KB EPROM using 8kb chips c. 16KB SRAM using 4kb chips. Explain the design along with memory address map.
3. Draw and explain block diagram of 8259 PIC
4. Control word register of 8255
5. Explain different data transfer modes of 8257 DMA controller.
6. Explain interfacing of 8259with 8086 minimum mode
7. Explain with block diagram working of 8255PPI
8. Mode 1 of 8255 for input operation
9. Draw and explain the block diagram of 8255. Also, explain different operating modes of 8255
10. 8259 pic
11. Discuss control word format for bit set reset (bsr) mode of 8255 PPI
12. Interface three 8259s with 8086 in minimum mode and explain its functionality in fully nested mode.

4	**Intel 80386DX Processor**		7
	4.1	Architecture of 80386 microprocessor	
	4.2	80386 registers–General purpose Registers, EFLAGS and Control registers	
	4.3	Real mode, Protected mode, virtual 8086 mode	
	4.4	80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory paging mechanism	

1. Write down features of super SPARC processor.
2. Explain address translation mechanism used in protected mode of 80386
3. State the use of RF, TF, VM, NT, IOPL flag bits
4. Explain protection mechanism used in 80386
5. Differentiate between real mode and protected mode
6. Explain in detail Protection Mechanism in 80386DX Processor.
7. Explain memory management in details in 80386DX processor.
8. Explain v86 mode of 80386DX
9. Draw format of selector and explain its field
10. Draw and explain Eflag register formatt of 80386 DX

5	**Pentium Processor**		**6**
	5.1	Pentium Architecture	
	5.2	Superscalar Operation,	
	5.3	Integer &Floating-Point Pipeline Stages,	
	5.4	Branch Prediction Logic,	
	5.5	Cache Organization and	
	5.6	MESI protocol	

1. Enlist the instruction pairing rules for U and V pipeline in Pentinum.
2. Explain how the flushing of pipeline problem is minimized in Pentinum architecture.
3. Code cache organization of Pentinum
4. Write down features of pentinum processor
5. Explain branch prediction logic used in pentinum
6. Data cache organization of pentium
7. Explain,in brief, pipeline stages on pentium processor
8. Explain in bbrief cache organization of pentium processor
9. Draw and explain architectur of Pentium processor

6	**Pentium 4**		**4**
	6.1	Comparative study of 8086, 80386, Pentium I, Pentium II and Pentium III	
	6.2	Pentium 4: Net burst micro architecture.	
	6.3	Instruction translation look aside buffer and branch prediction	
	6.4	Hyper threading technology and its use in Pentium 4	

1. Write the instruction issue algorithm used in Pentium
2. Compare 8086,80386 and pentium
3. Compare Pentium 2 , Pentium 3 and Pentium 4 processors.
4. Write instruction issue algorithm used in Pentium
5. How flushing problem is minimised in Pentium? Explain.