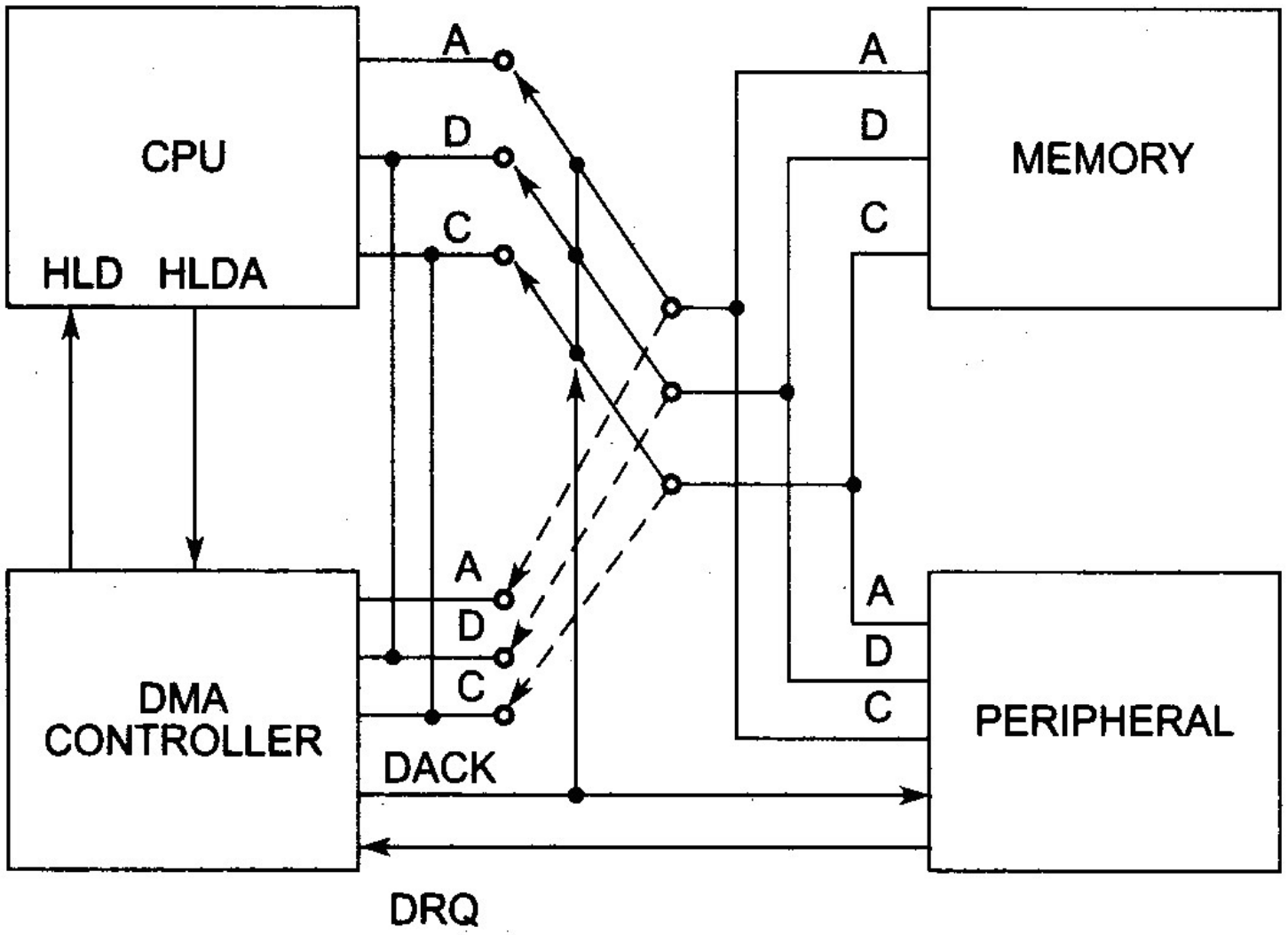
8257 DMA Controller

Interfacing of 8257 with 8086



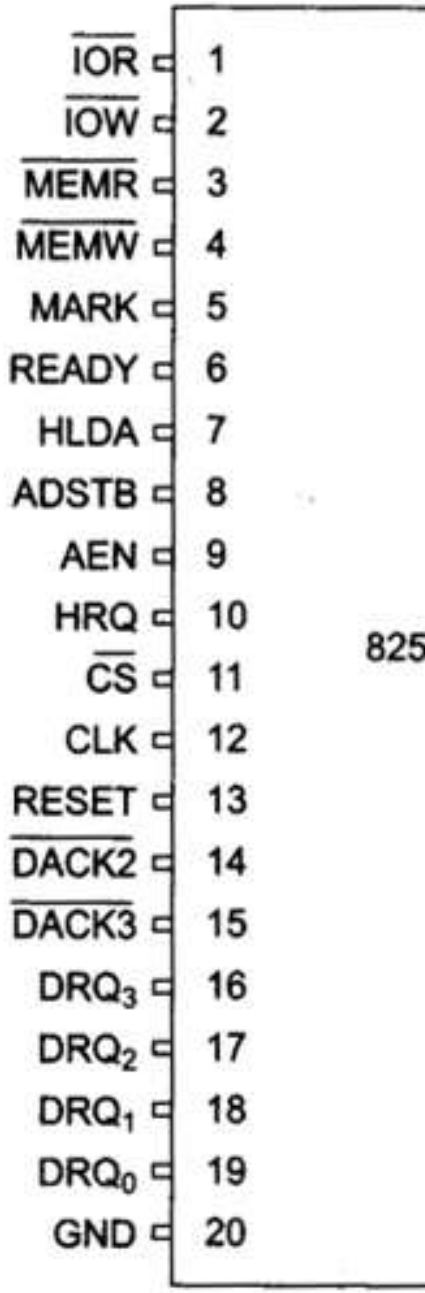
Interfacing a Typical DMA Controller with a System

Data Transfer Modes of 8257

1. Single Byte Transfer Mode/ Cycle Stealing
2. Block Transfer Mode.
3. Demand Transfer Mode
4. Cascade Transfer Mode

8257: Pin Diagram

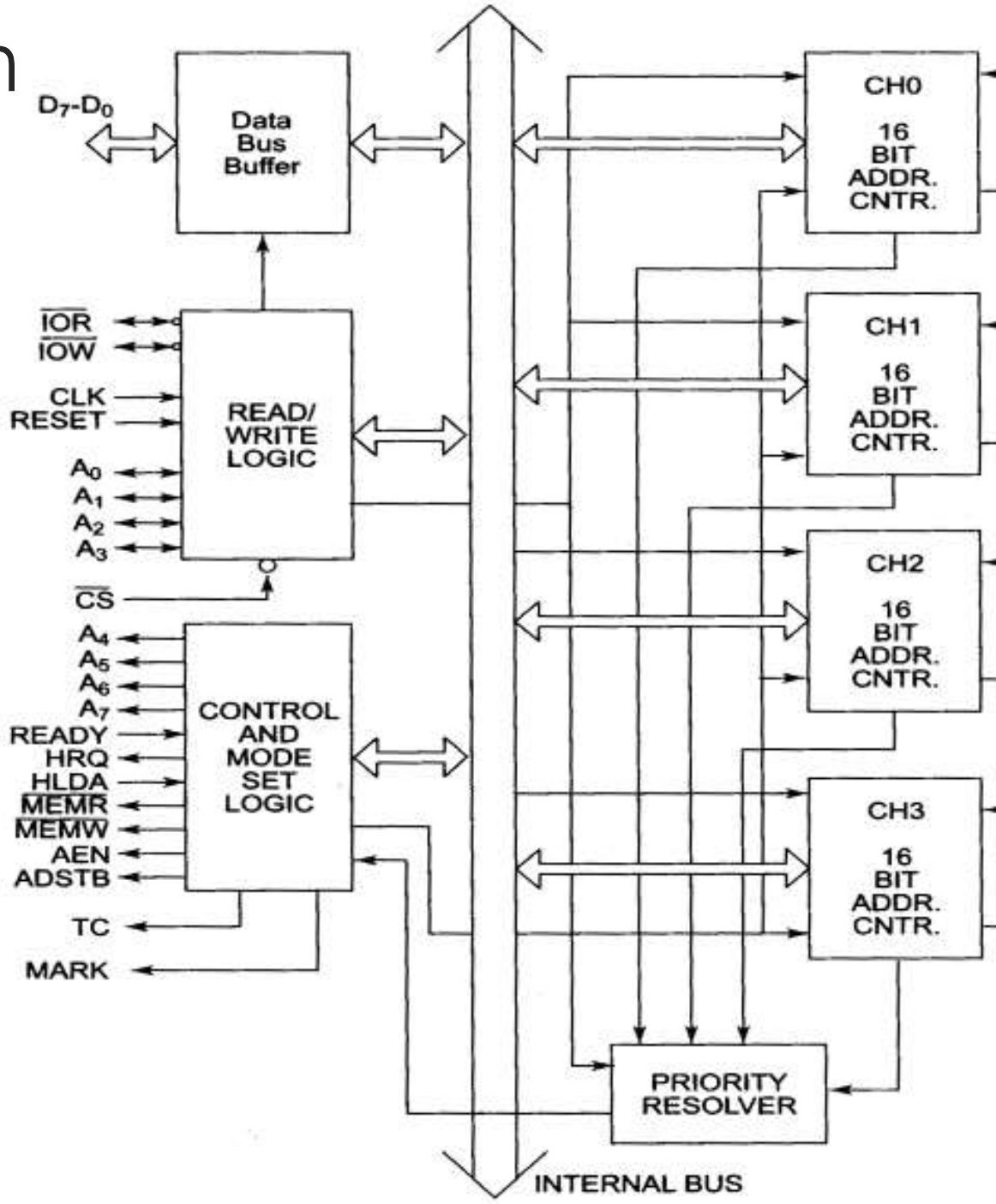
- D7 – D0
- $\overline{IOR}$
- $\overline{IOW}$
- CLK
- $\overline{MEMR}$
- $\overline{MEMW}$
- A0-A3
- A4 – A7
- RESET
- READY
- HRQ
- HLDA
- AEN
- ADSTB
- TC
- MARK
- DRQ0 – DRQ3
- $\overline{DACK0}$ – $\overline{DACK3}$
- $\overline{CS}$
- Vcc/Vss
- GND



Pin Di

8257 Block Diagram

1. Data bus buffer
2. Read/Write logic
3. Control logic block
4. Priority resolver
5. DMA channels.



8257: DMA CONTROLLER

- Intel's 8251 is a four channel DMA controller designed to be interfaced w
  family of microprocessors.
- The 8257 performs the DMA operation over four independent DMA chan
- Each of the four channels of 8257 has a pair of two 16 bit registers, viz. DM
  register and terminal count register.
- Also, there are two common registers for all the channels, namely, mode
  status register.
- Thus there are a total of ten registers. The CPU selects one of these ten re
  address lines A0 – A3.

8257: DMA CONTROLLER

8257 Register Selection

Register	Byte	Address Inputs				F/L	BI-Directional Data				
		A_3	A_2	A_1	A_0		D_7	D_6	D_5	D_4	D_3
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3
	MSB	0	0	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}
CH-1 DMA Address	LSB	0	0	1	0	0	A_7	A_6	A_5	A_4	A_3
	MSB	0	0	1	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}
CH-1 Terminal Count	LSB	0	0	1	1	0	C_7	C_6	C_5	C_4	C_3
	MSB	0	0	1	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}
CH-2 DMA Address	LSB	0	1	0	0	0	A_7	A_6	A_5	A_4	A_3
	MSB	0	1	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}
CH-2 Terminal Count	LSB	0	1	0	1	0	C_7	C_6	C_5	C_4	C_3
	MSB	0	1	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}
CH-3 DMA Address	LSB	0	1	1	0	0	A_7	A_6	A_5	A_4	A_3
	MSB	0	1	1	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}
CH-3 Terminal Count	LSB	0	1	1	1	0	C_7	C_6	C_5	C_4	C_3
	MSB	0	1	1	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}
MODE SET (Programme only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3
STATUS (Read only)	—	1	0	0	0	1	0	0	0	UP	TC3

8257 Block Diagram

MODE SET REGISTERS:

- It is a write only registers.
- It is used to set the operating modes.
- This registers is programmed after initialization of DMA channel.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
AL	TCS	EW	RP	EN_3	EN_2	EN_1	EN_0

D_7	D_6	D_5	D_4	D_3	D_2
AL	TCS	EW	RP	EN_3	EN

- EN_3=1=Enable DMA CH-3
- EN_3=0=Disable DMA CH-3

- EN_2=1=Enable DMA CH-2
- EN_2=0=Disable DMA CH-2

- EN_1=1=Enable DMA CH-1
- EN_1=0=Disable DMA CH-1

- EN_0=1=Enable DMA CH-0
- EN_0=0=Disable DMA CH-0

D_7	D_6	D_5	D_4	D_3	D_2
AL	TCS	EW	RP	EN_3	EN_2

- AL=1=Auto load mode
- TCS=1=Stop after TC (Disable Channel)
- EW=1=Extended write mode
- RP=1=Rotating priority

STATUS REGISTERS:

- It is read only registers.
- It tells the status of DMA channels
- TC status bits are set when TC signal is activated for that channel.
- Update flag is not affected during read operation.
- The UP bit is set during update cycle . It is cleared after completion of update cycle.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	UP	TC_3	TC_2	TC_1	TC_O

- UP=Update flag
- UP=1=8257 executing update cycle
- UP=0=8257 executing DMA cycle

- TC_3=1=TC activated CH-3
- TC_3=0=TC activated CH-3

- TC_2=1=TC activated CH-2
- TC_2=0=TC activated CH-2

- TC_1=1=TC activated CH-1
- TC_1=0=TC activated CH-1

- TC_0=1=TC activated CH-0
- TC_0=0=TC activated CH-0

- The address of status register is $A_3A_2A_1A_0$=1000.

FIRST/LAST FLIP FLOP:

- 8257 have 8bit data line and 16 bit address line.
- 8085 it is getting 8-bit data in simultaneously.
- 8085 can not access 16-bit address in simultaneously.

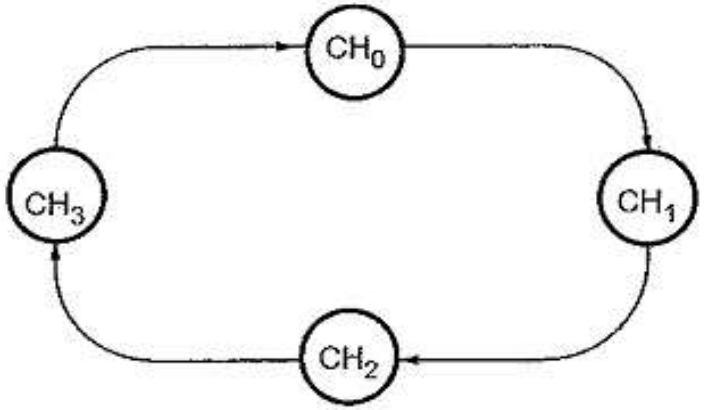
- A0-A3 lines are used to distinguish between registers ,bu they are not distinguish lower and higher address.
- It is reset by external RESET signal.
- It is also reset by whenever mode set register is loaded.
- So program initialization with a dummy (00 H).
- FF=1=Higher byte of address
- FF=0=Lower byte of address.

Modes of Operation

- Rotating priority Mode:
- The priority of the channels has a circular sequence.
- Fixed Priority Mode:
- The priority is fixed.
- TC Stop Mode
- Auto Load mode
- Extended Write mode

Rotating Priority Mode

- In rotating priority mode, the priority of the channels has a circular sequence.
- In this, channel being serviced gets the lowest priority and the channel next to it gets the highest priority as shown in Fig.



Rotating Priority Mode

- Thus, with rotating priority in a single chip DMA system, any device reque is guaranteed to be recognized after no more than three higher pri have occurred.
- This prevents any one channel from monopolizing the system. The rot mode can be set by writing logic '1' in the bit 4 of the mode set register.

Fixed Priority Mode

- In the fixed priority, channel 0 has the highest priority and channel 3 has the lowest priority.
- In the fixed priority, after recognition of any one channel for service, the other channels are prevented from interfering with that service until it is completed.
- If bit 4 of mode set register is logic 0, Operating Modes of 8257 operates in fixed priority mode

	Priority	Cl
Highest	1	
	2	
	3	
Lowest	4	

Priority rating

Extended Write Mode

- Microcomputer systems allow use of various types of memory and I/O devices with different access time.
- If a device can not be accessed within a specific amount of time it returns a “not ready” indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing.
- The extended write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the Operating Modes of 8257.
- It does this by activating MEMW and IOW signals earlier in the DMA cycle, giving more setup time.

TC STOP Mode

- If the TC stop bit is set, a channel is disabled (i.e. its enable bit is reset) af terminal count (TC) output goes high, thus automatically preventing furthe operation on that channel.
- To enable DMA operation on the channel it is necessary to set enable bit corresponding channel in the mode set register. If the TC STOP bit is not s occurrence of the TC output has no effect on the channel enable bits.

Auto Load Mode

- Auto load Mode when enabled, permits block chaining operations immediate software intervention between blocks.
- In this mode, channel 2 parameters (DMA starting address, termin and DMA transfer mode) are initialized as usual for the first data blo
- These parameters are automatically duplicated in the channel 3 when channel 2 is initialized.
- After the first block of DMA cycles is executed by channel 2 (i.e., TC output goes high), the parameters stored in the channel 3 regi transferred to channel 2 during an 'update' cycle and next block cycle is executed.
- This repeat block operations can be used in applications such refreshing.