CSC405 Microprocessor

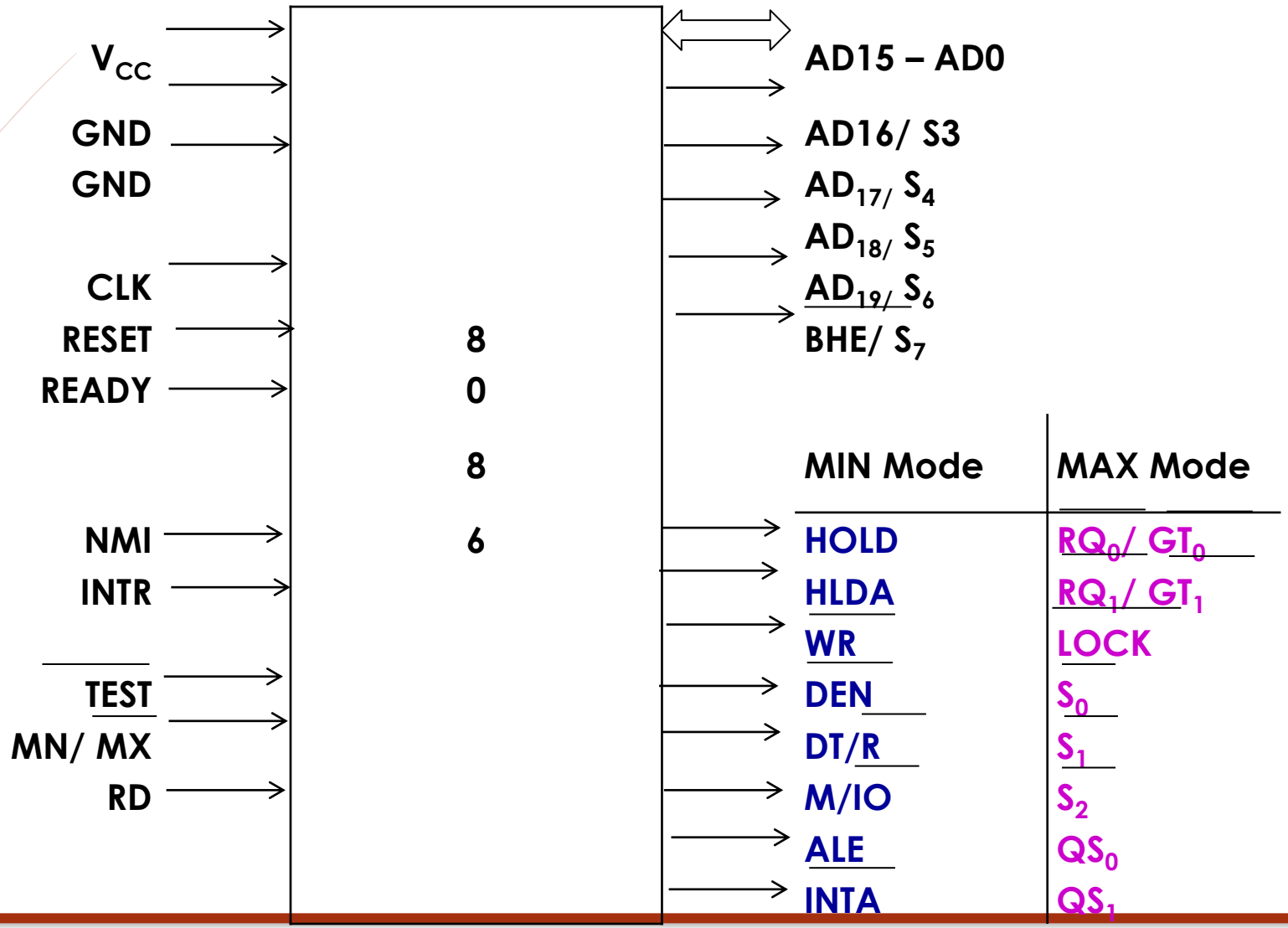
8086 Microprocessor

Modes of Operation

8086 – Pin Diagram

- 8086 operates in 2 modes:
  i. Minimum Mode
  ii. Maximum Mode
- The minimum mode is used for a small system with a single processor
- The maximum mode is for medium size to large systems with 2 or more processors.

8086 – Functional Pin Diagram



8086 – Pin Configuration

Pin Definitions:

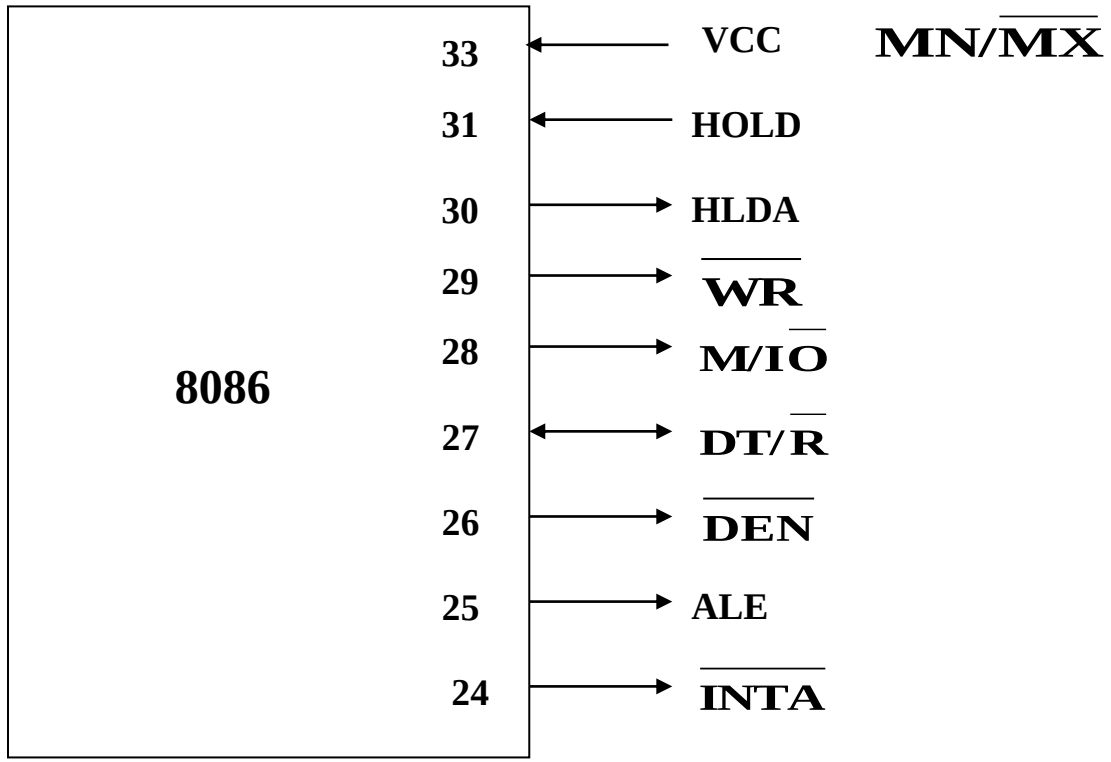
1) Supply pins (3 pins)
2) Clock related pins (3 pins)
3) Address & Data pins (21 pins)
4) Interrupt pins (2 pins)
5) Other Control pins (3 pins)
6) Mode Multiplexed signals (8 pins)

8086 – Pin Configuration

Pin Definitions:

Mode Multiplexed signals (8 pins)

MIN Mode	MIN Mode
HOLD	DT/$\overline{R}$
HLDA	M/$\overline{IO}$
$\overline{WR}$	ALE
$\overline{DEN}$	$\overline{INTA}$

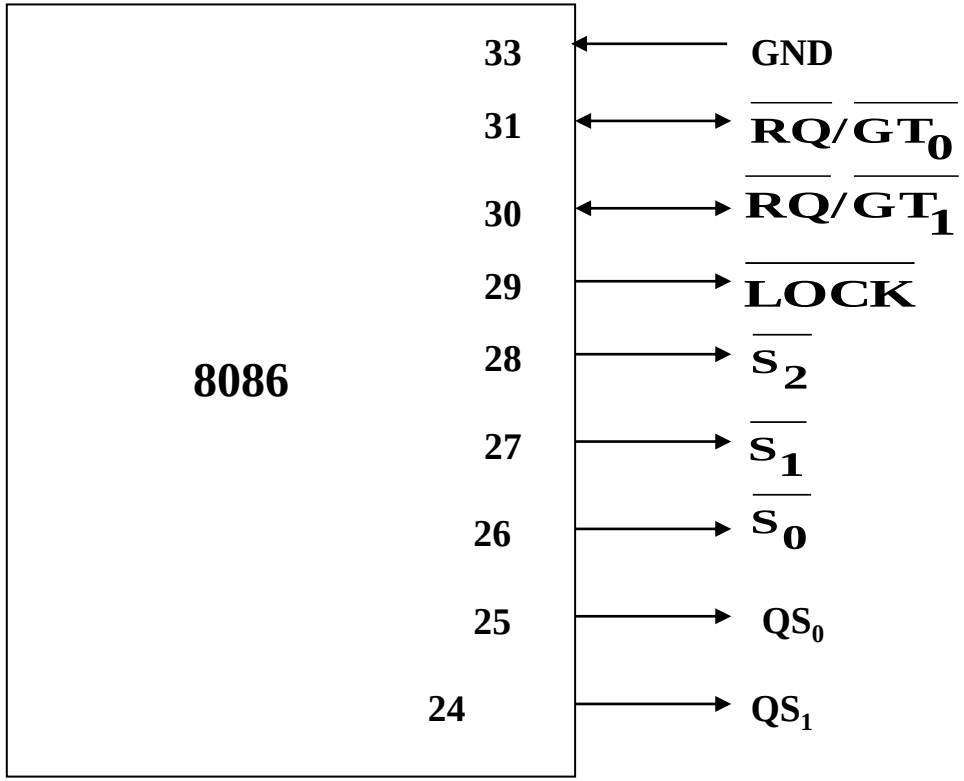


8086 – Pin Configuration

Pin Definitions:

Mode Multiplexed signals (8 pins)

MAX Mode	MAX Mode
$\overline{RQ_0}/GT_0$	S_1
$\overline{RQ_1}/GT_1$	S_2
$\overline{LOCK}$	QS_0
S_0	QS_1

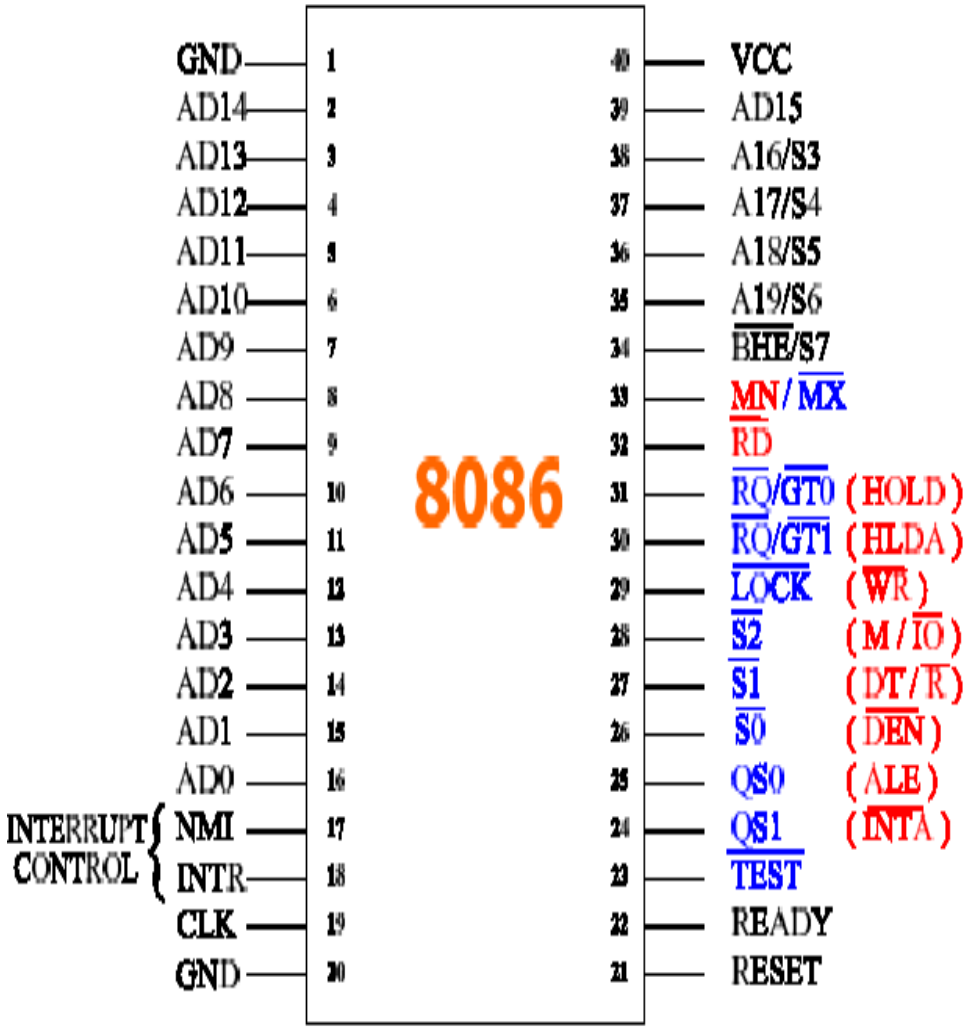


8086

Some common components of 8086 circuit in MIN or MAX mode are:

1. 8282: (8 – bit) Octal Latch
2. 8286: (8 – bit) Octal bus Transreceiver
3. 8284: Clock Generator.
4. 8288: Bus Controller

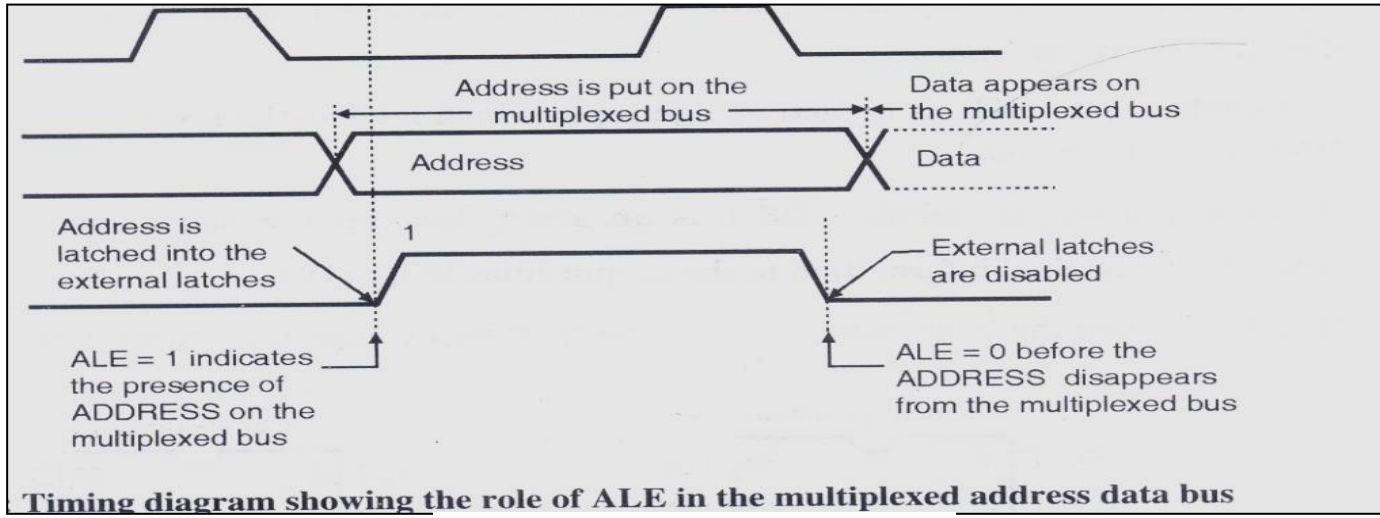
8086


8086
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
INTERRUPT CONTROL
NMI 17
INTR 18
CLK 19
GND 20
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET

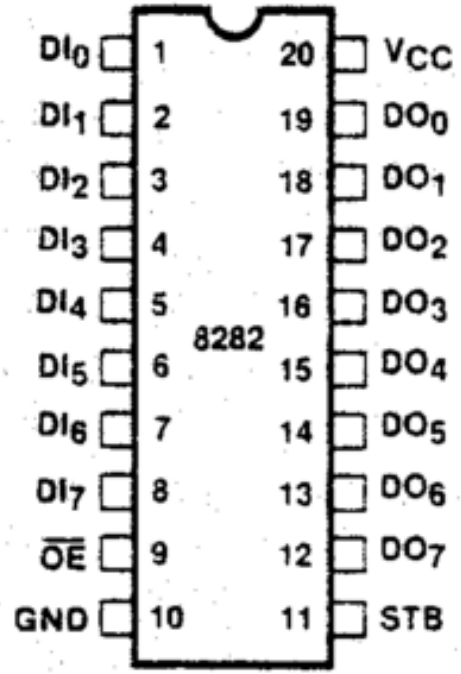
8282: (8 – bit) Octal Latch

8282: 8 bit latch

- The address data bus AD15-AD0 is time multiplexed
- The address lines A16 – A19 are multiplexed with S_3 -S_6
- Also $\overline{BHE}$ & S7 is multiplexed.
- The address bus and the BHE signal are demultiplexed using the ALE signal and then latched into 8282

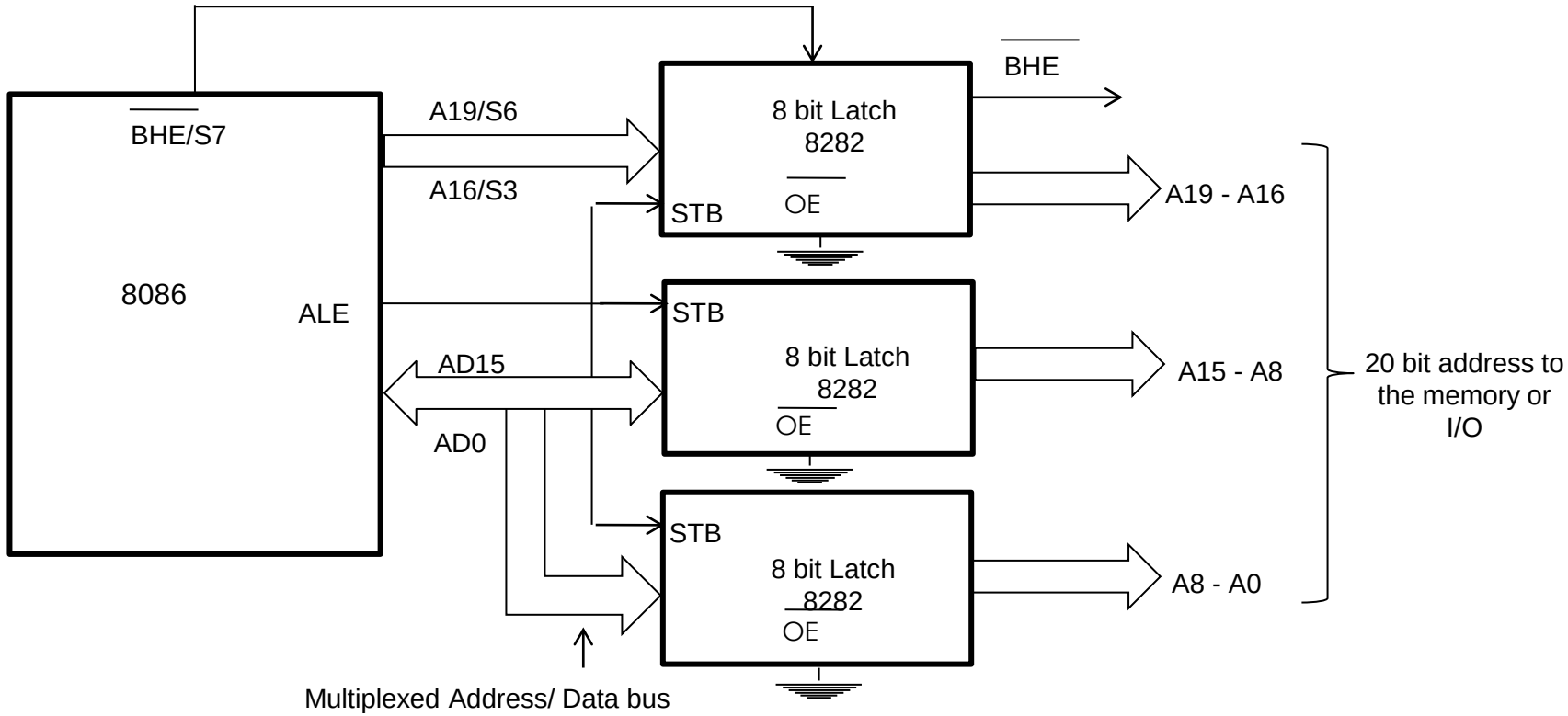


Timing diagram showing the role of ALE in the multiplexed address data bus



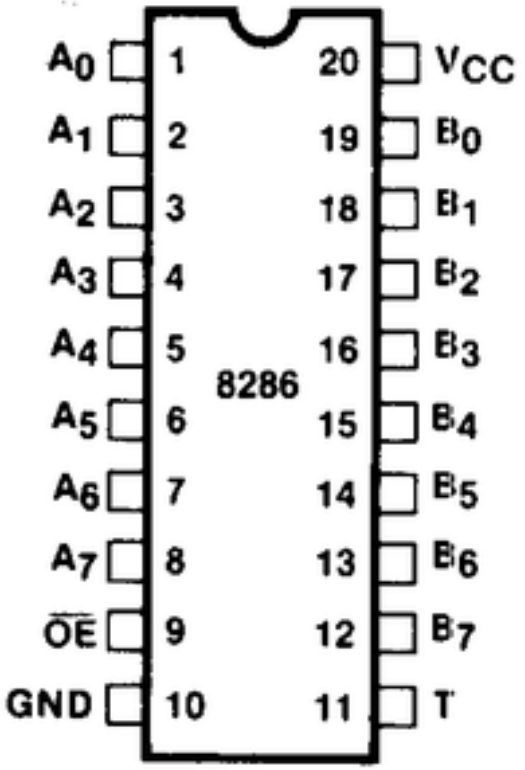
8282: 8 bit latch

- The high ALE asserts the STB of 8282, It enables the external latches to store the address.
- Thus to get the 20 bit address (A0-A7, A8-A15,A16-A19) and the $\overline{\text{BHE}}$ signal, 3 - 8282's are reqd (8 bit latch & 21 lines, so 3 latches reqd).



8086

8286: (8 – bit) Octal bus Transreceiver



8286: Octal trans-receiver (Transmitters & Receivers)

i. Contains fully parallel 8 bit bus trans- receiver. ∴ 2 transceivers are required as data bus is 16 – bits.

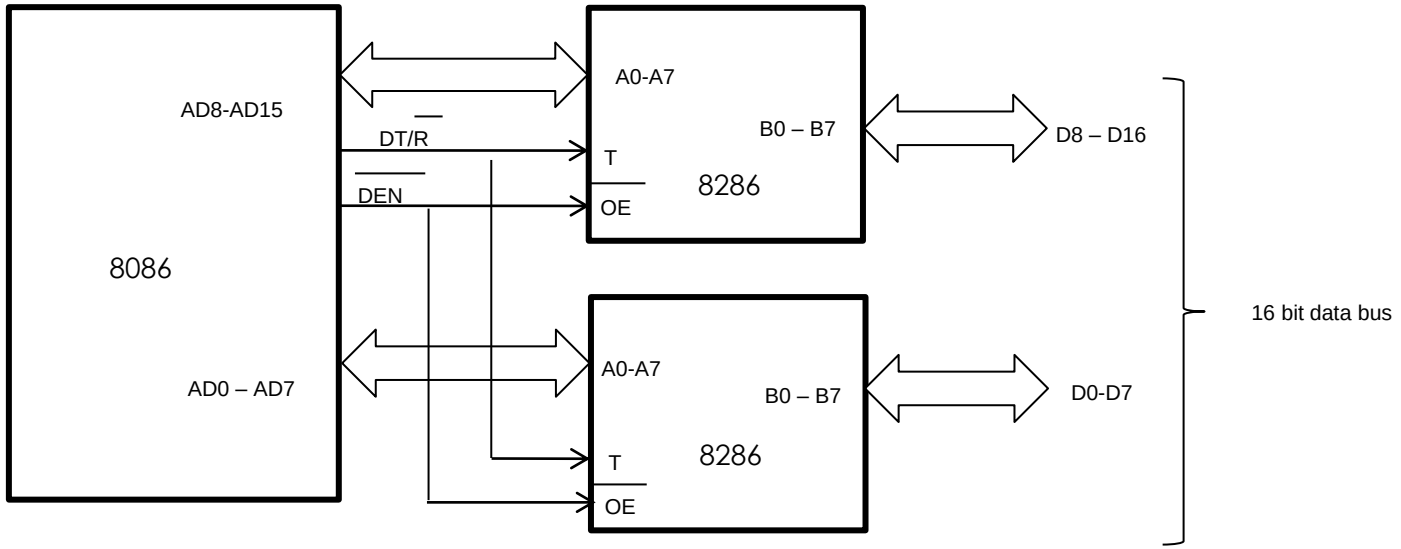
ii. Tri-state (high impedance outputs)

iii. Acts as bidirectional buffer and increases the driving capacity of the data bus.

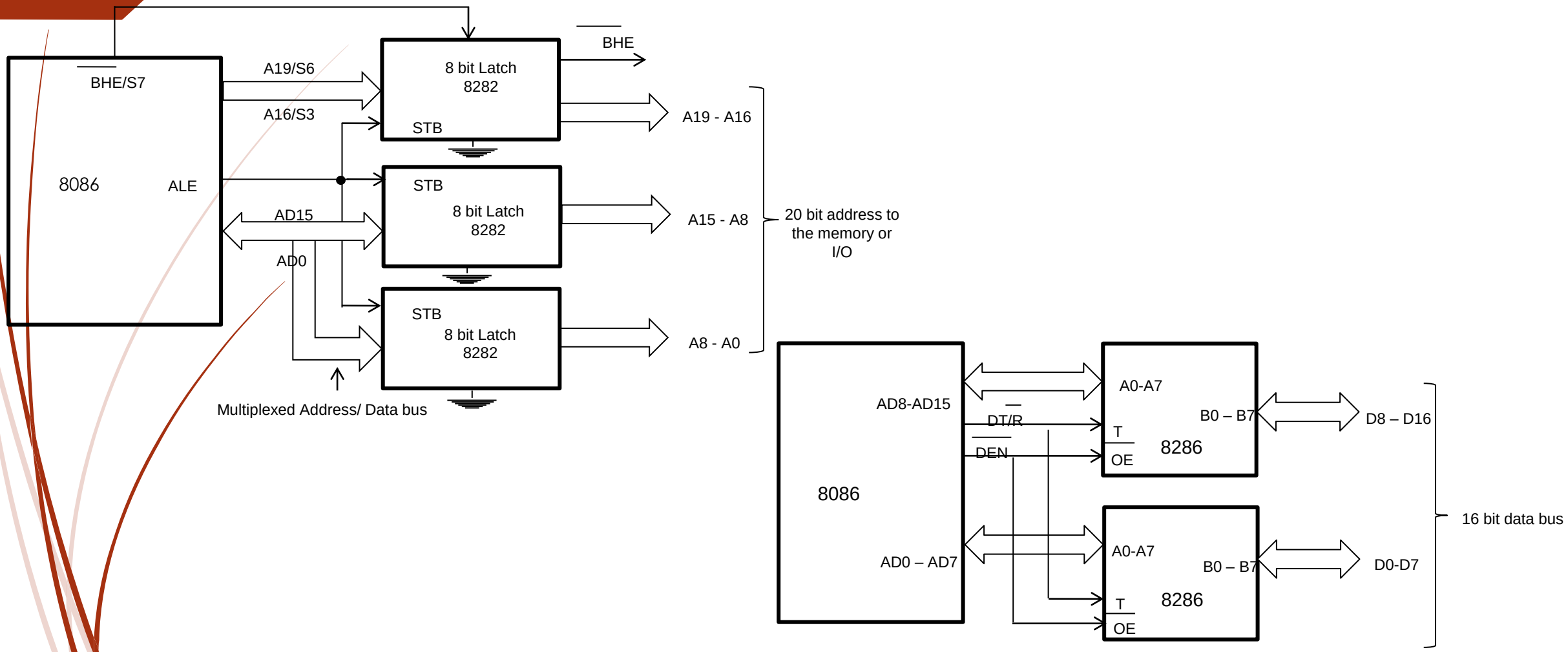
iv. It is enabled when $\overline{OE}$ is low

T controls the direction of flow of data

- T =1 ⟶ data is transmitted
- T = 0⟶ data is received



8086 – Demultiplexing Address and Data Bus



8284: Clock Generator

8284: Clock Generator & Driver

i. Provides CLOCK (C LK) signal, a train of pulses at a constant frequency

ii. It synchronizes the READY (RDY) signal which indicates that an interface is ready for data.

iii. Also synchronizes the RESET (RST) signal which is used to initialize the system

iv. 2 ways :

EFI - (External Frequency Input)

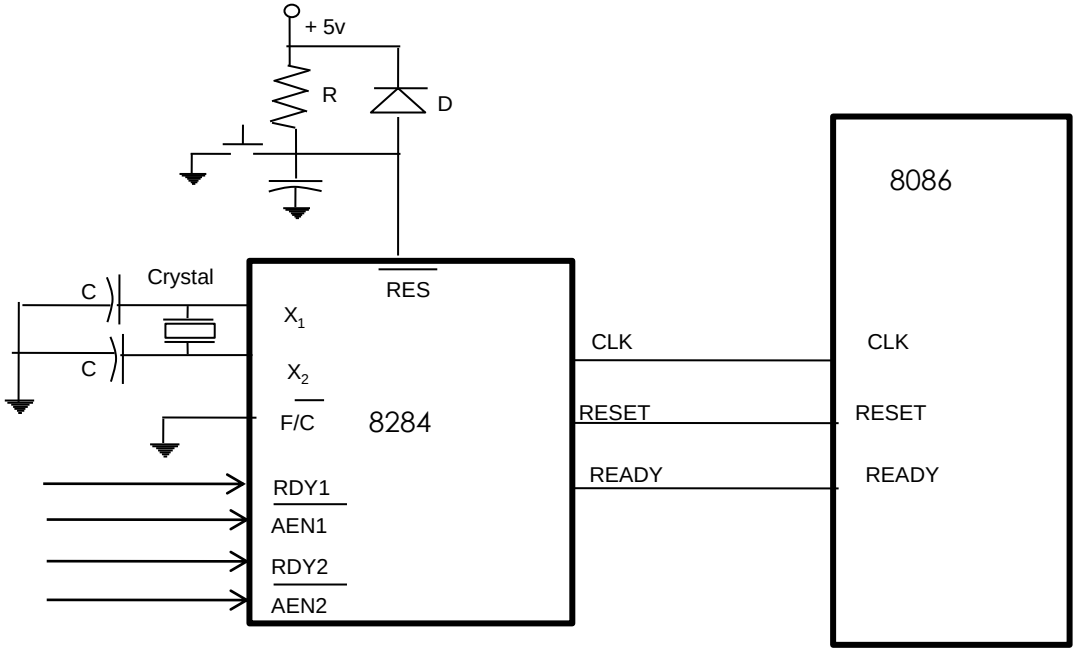
X1,X2 –Oscillator Clock Input)

Clock Input selection

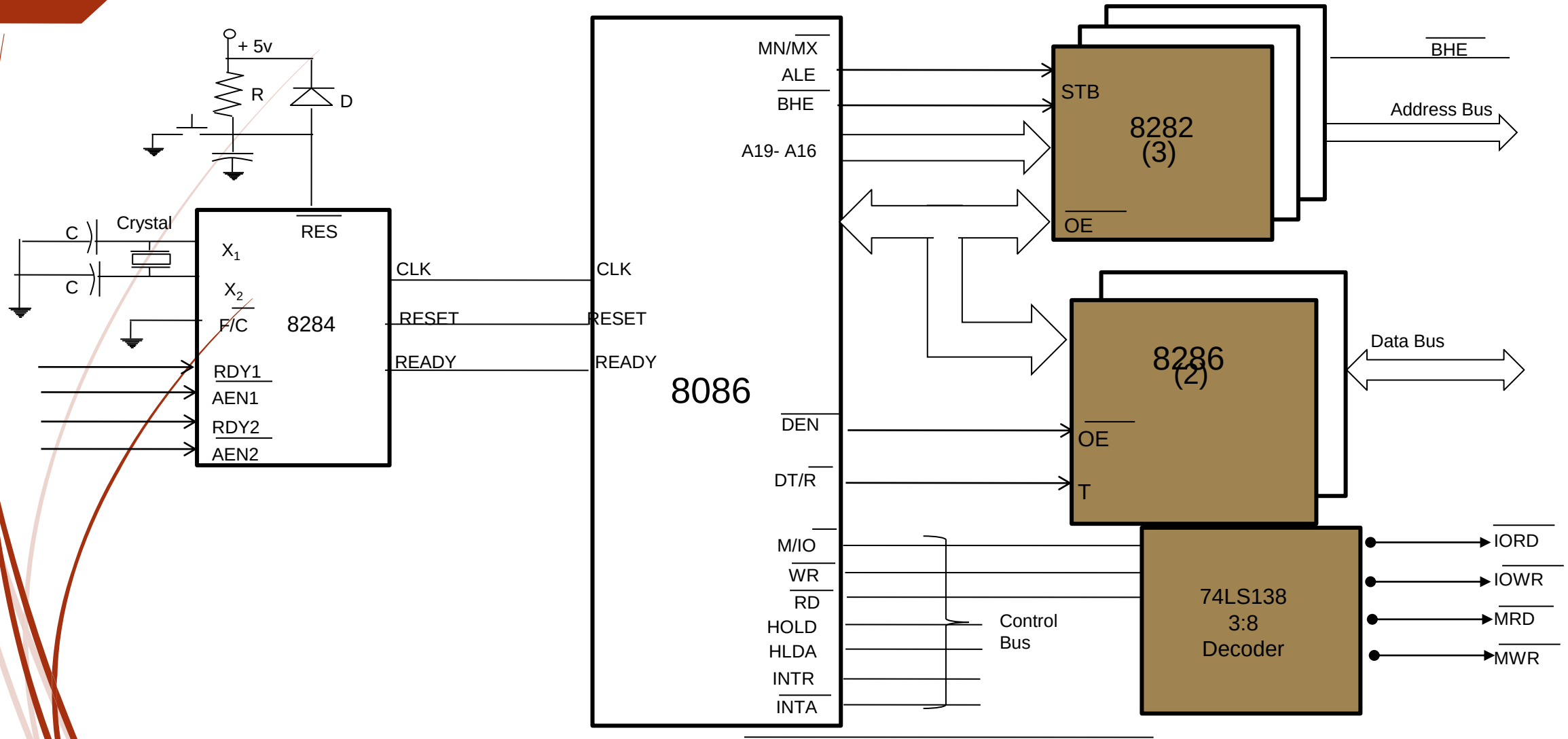
F/$\overline{C}$ = 1 ⟶ clock given through EFI

F/$\overline{C}$ = 0 ⟶ clock given through Crystal

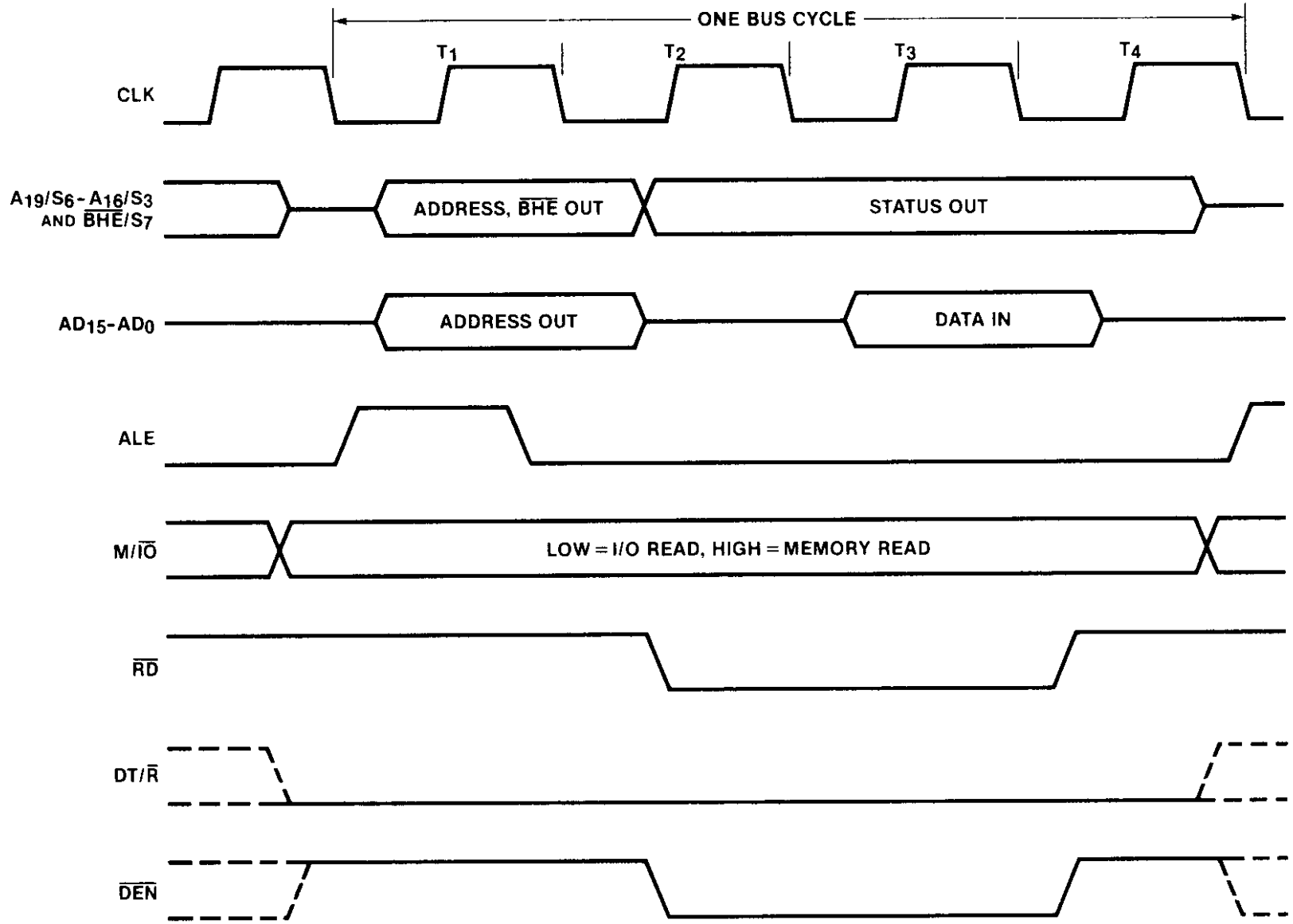
(Oscillator inputs X1,X2 pins)



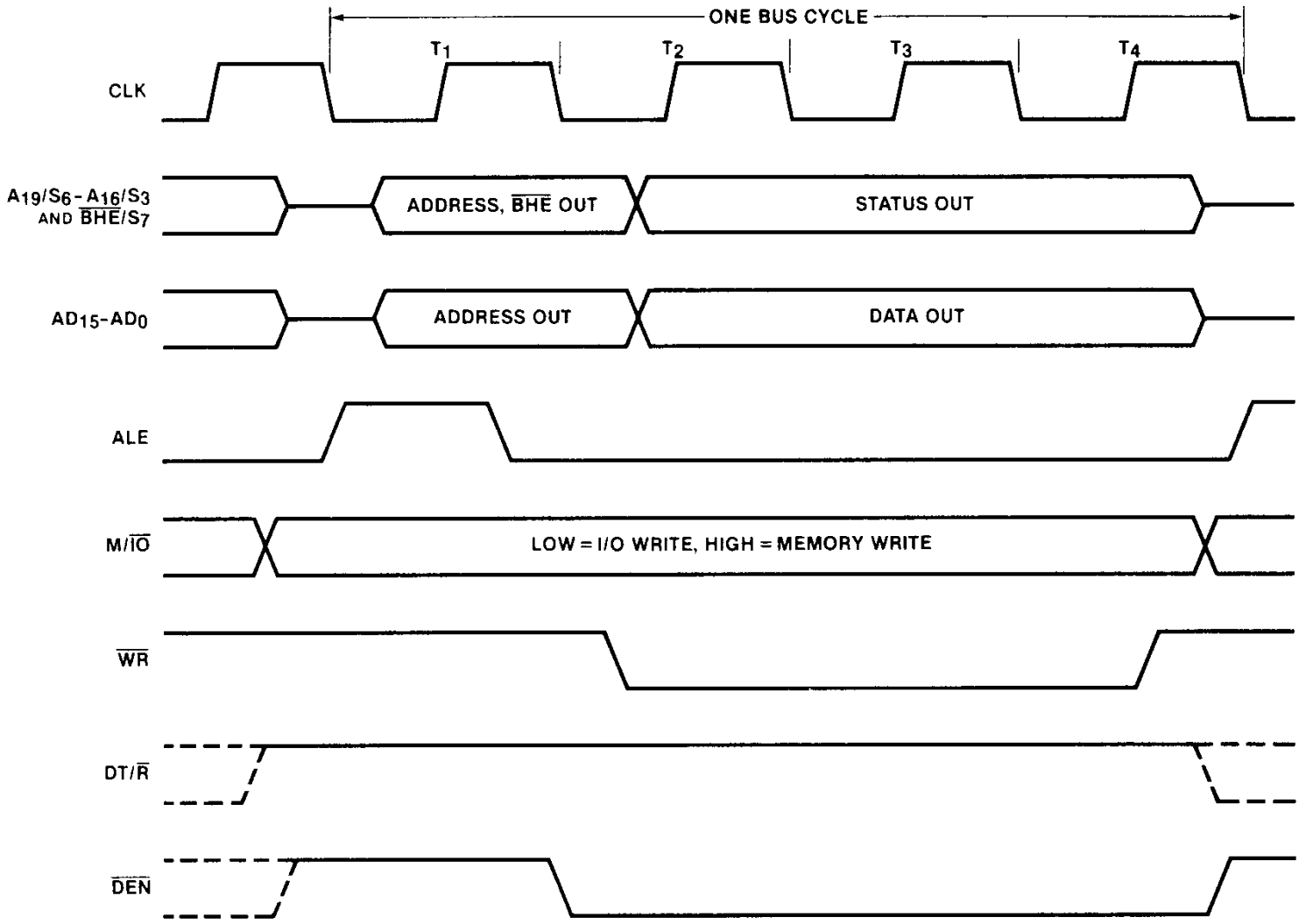
8086 - Minimum Mode Minimum System Block Diagram



Read M/Cycle in Min Mode



Write M/Cycle in Min Mode



8086		
Pin	Mode	
	Minimum	Maximum
31	HOLD	$\overline{RQ}/\overline{GT0}$
30	HLDA	$\overline{RQ}/\overline{GT1}$
29	$\overline{WR}$	$\overline{LOCK}$
28	$M/\overline{IO}$	$\overline{S2}$
27	$DT/\overline{R}$	$\overline{S1}$
26	$\overline{DEN}$	$\overline{S0}$
25	ALE	QS0
24	$\overline{INTA}$	QS1

8288: Bus Controller

8086 : Operating Modes

- When the Minimum mode operation is selected, the **8086 provides all control signals** needed to implement the memory and I/O interface.

- While in Maximum mode operation, the **8288 provides all control signals** needed to implement the memory and I/O interface.

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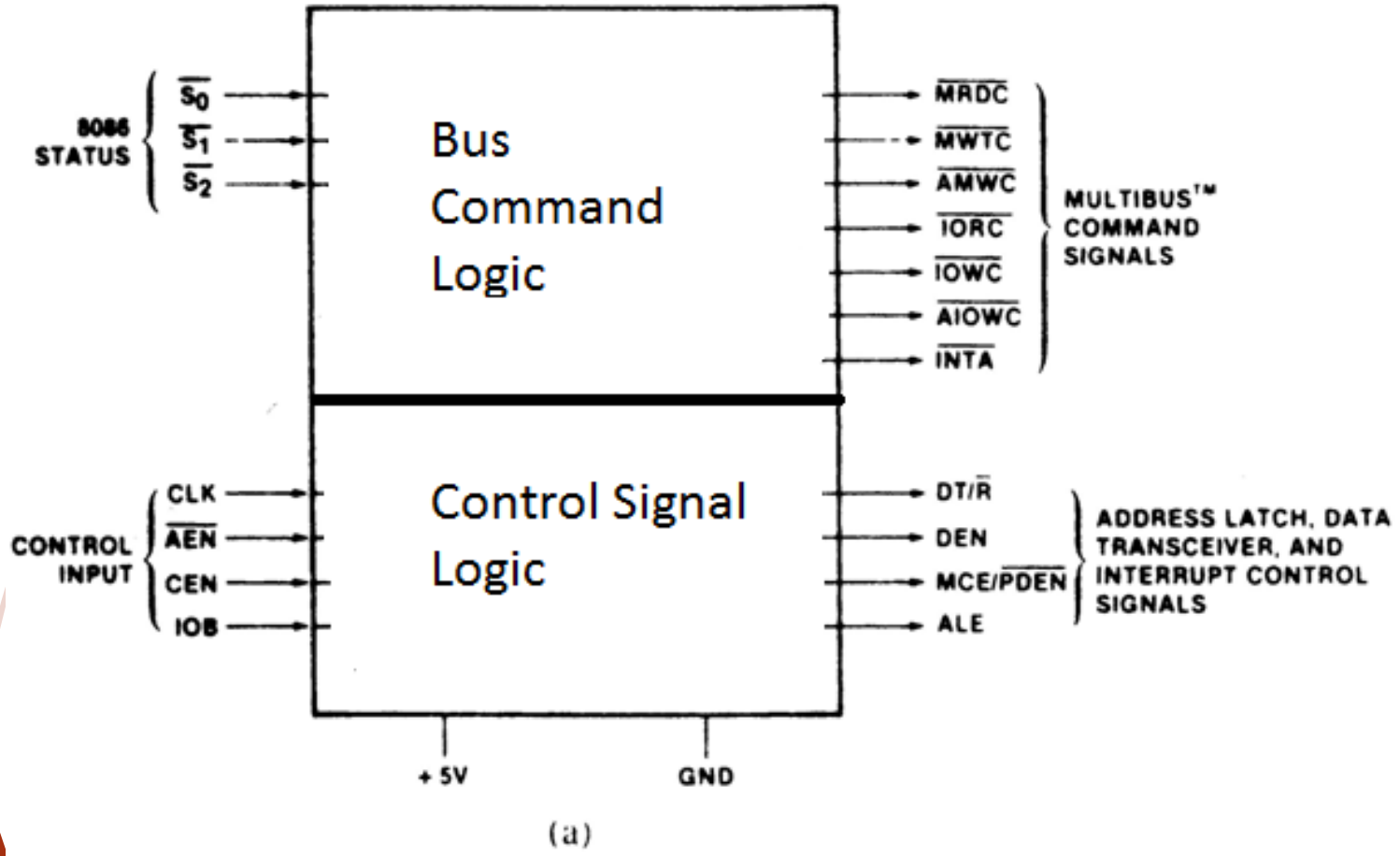
8288: Bus Controller

i. It is used in maximum mode configuration

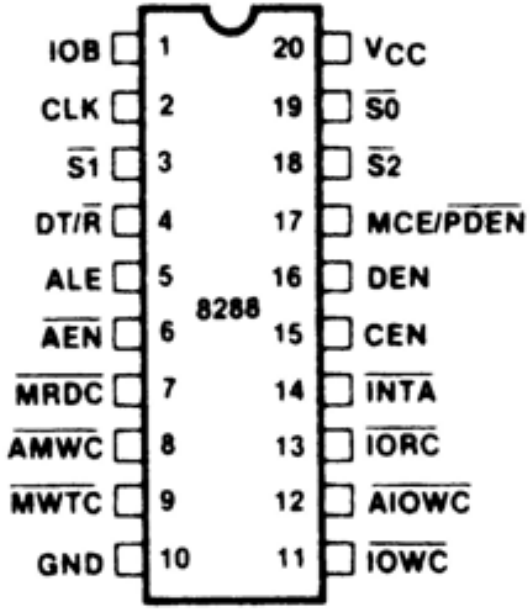
ii. It accepts the CLK signal along with S_0, S_1, S_2

iii. It generates the command, control & timing signals at its output

8288: Bus Controller

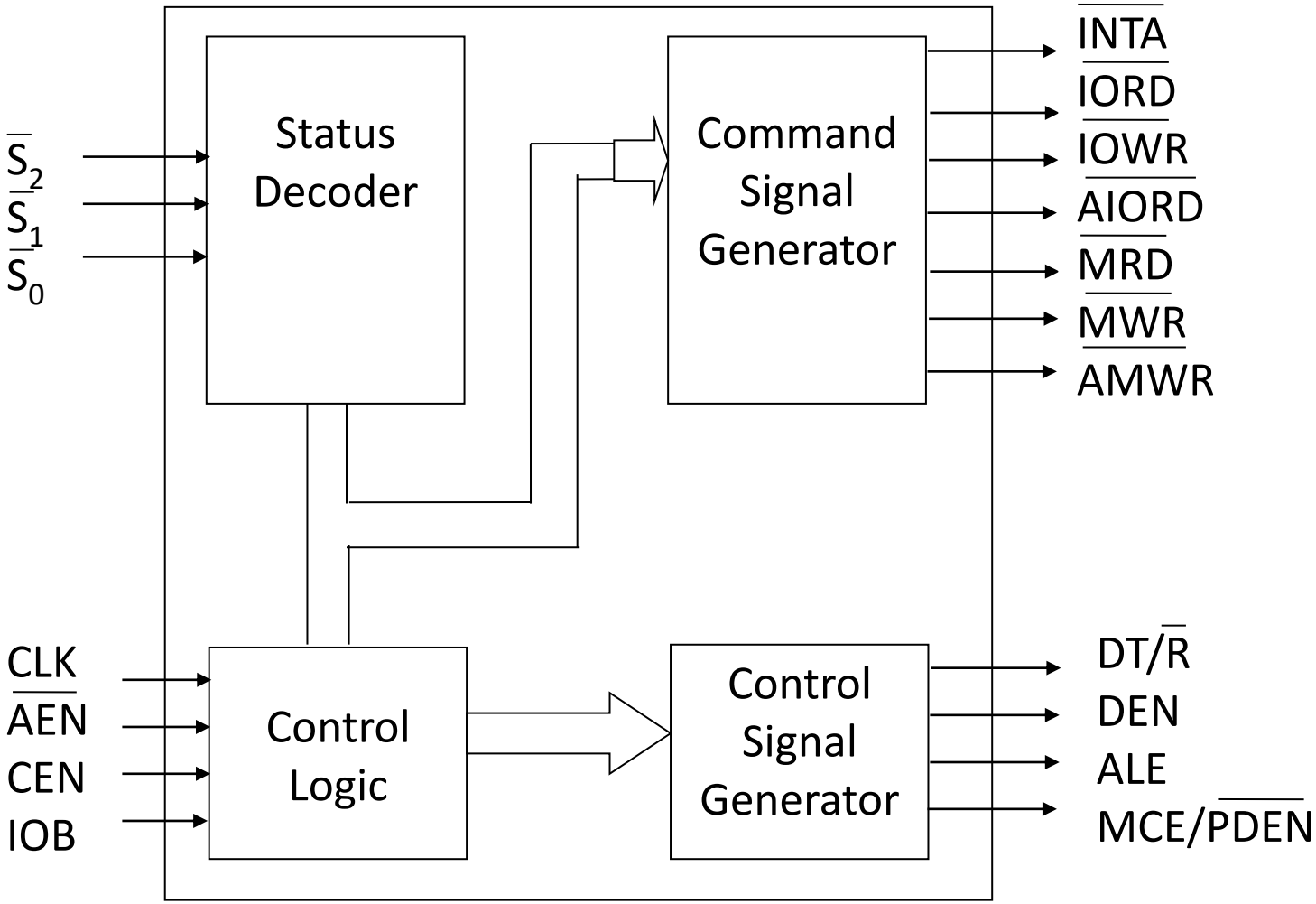


(a)



(b)

8288: Bus Controller



CEN	IOB	$\overline{AEN}$	Description
1	1	X	I//O bus Mode; all control lines enabled; MCE/$\overline{PDEN}$ = $\overline{PDEN}$
1	0	1	System Bus Mode but all control signals disabled the bus is busy i.e. controlled by another bus master
1	0	0	System Bus Mode, all control signals active; the bus is free for use; MCE/$\overline{PDEN}$ = MCE
0	X	X	All command outputs and DEN and PDEN outputs are disabled

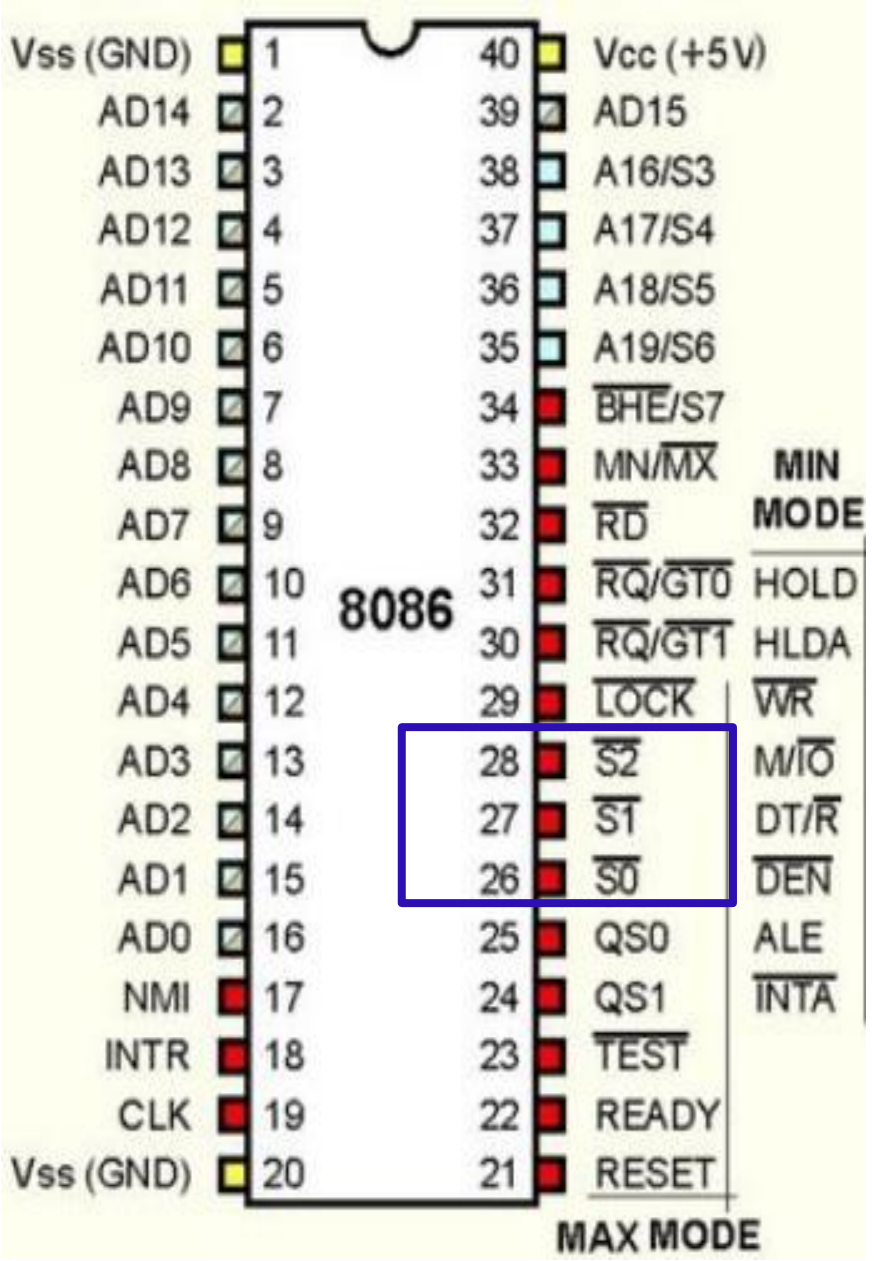
- **MCE: master cascade enable**
- **PDEN: Peripheral Data Enable**

CEN: Command Enable

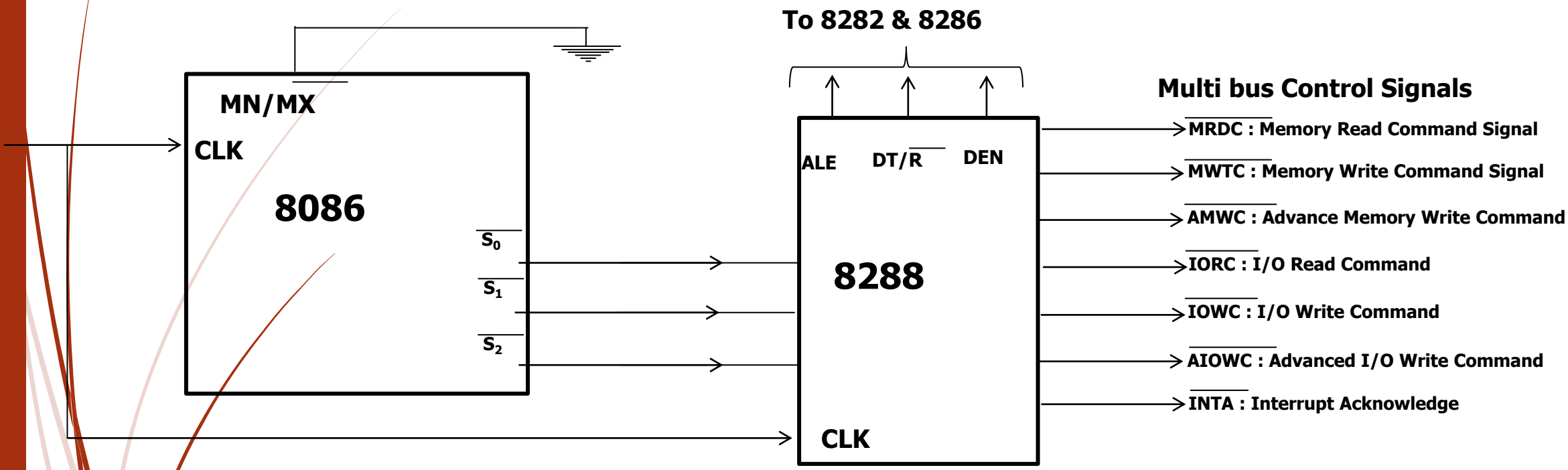
AEN: address enable

Intended for the 8288 bus controller

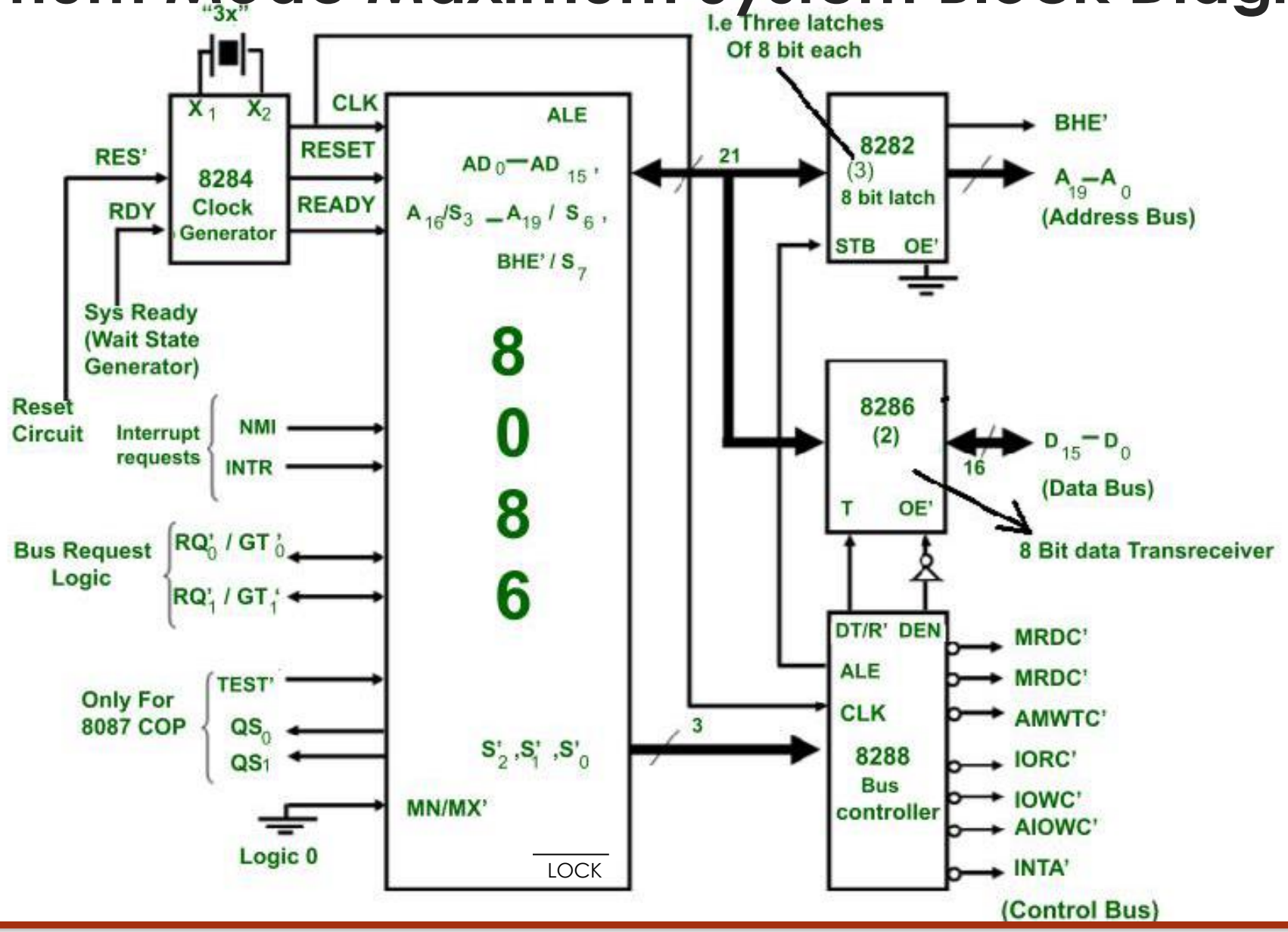
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	**Processor State**
0	0	0	Interrupt acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	code access
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	passive



8288: Bus Controller



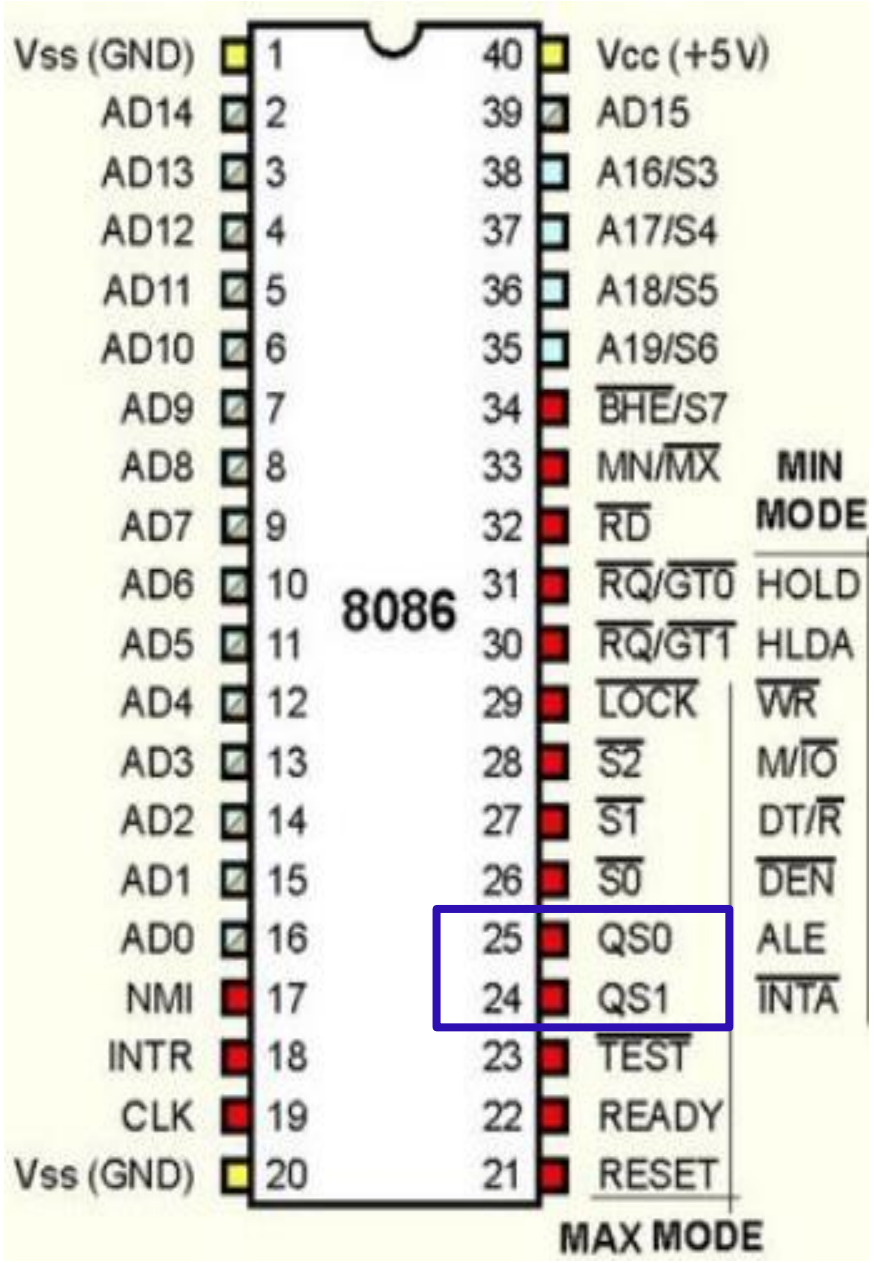
8086 – **Maximum Mode Maximum System Block Diagram**



8086 – Queue Operation

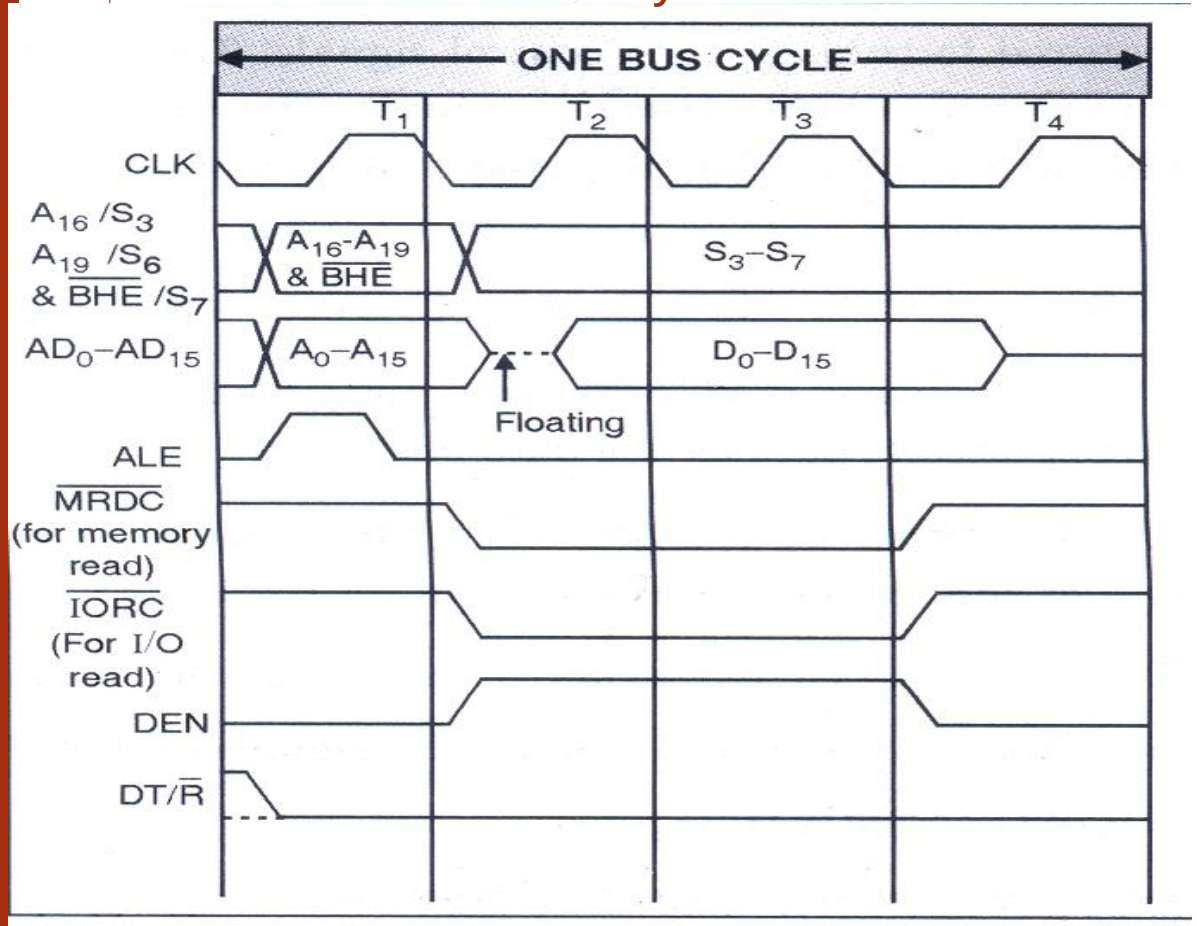
Queue Status

QS_1	QS_0	**Current Instruction**
0	0	NOP
0	1	First byte of Opcode from Queue
1	0	Empty the queue
1	1	Subsequent byte from Queue.

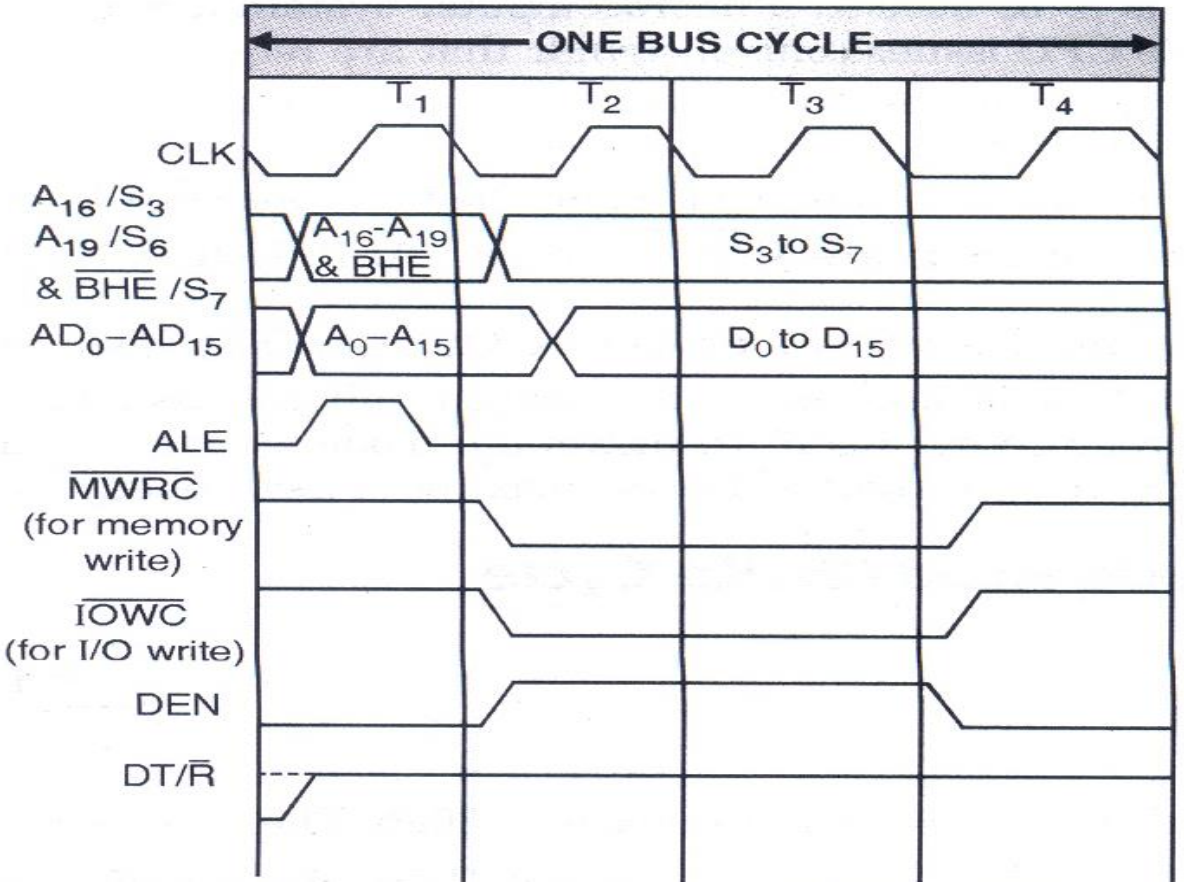


8086

Read M/Cycle in Max Mode



Write M/Cycle in Max Mode



8086

Comparison between Min and Max mode