

RPi SPI

NOTE: Similar documentation can be found on the official [Raspberry Pi Documentation Project \(http://www.raspberrypi.org/documentation/hardware/raspberrypi/spi/README.md\)](http://www.raspberrypi.org/documentation/hardware/raspberrypi/spi/README.md) page.

The BCM2835 on the Raspberry Pi has 3 SPI (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus) Controllers. The main SPI (with two slave selects) is available on the header of all Pis with Linux kernel support. The second SPI (with the option of up to three slave selects) is available on 40-pin versions of Pis, with kernel support from Raspbian Jessie 2016-05-10 distribution and up.

Chapter 10 in the [BCM2835 ARM Peripherals \(http://www.raspberrypi.org/wp-content/uploads/2012/02/BCM2835-ARM-Peripherals.pdf\)](http://www.raspberrypi.org/wp-content/uploads/2012/02/BCM2835-ARM-Peripherals.pdf) datasheet describes the main controller. Chapter 2.3 describes the auxiliary controller.

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Hardware

The main SPI interface is referred to as SPI0 in the documentation. The second is SPI1.

SPI0 (available on P1 headers on all RPi versions)

SPI Function	Header Pin	Broadcom Pin Name	Broadcom Pin Name
MOSI	P1-19	GPIO10	SPI0_MOSI
MISO	P1-21	GPIO09	SPI0_MISO
SCLK	P1-23	GPIO11	SPI0_SCLK

CE0	P1-24	GPIO08	SPI0_CE0_N
CE1	P1-26	GPIO07	SPI0_CE1_N

SPI1 (available only on 40-pins P1 header)

SPI Function	Header Pin	Broadcom Pin Name	Broadcom Pin Function
MOSI	P1-38	GPIO20	SPI1_MOSI
MISO	P1-35	GPIO19	SPI1_MISO
SCLK	P1-40	GPIO21	SPI1_SCLK
CE0	P1-12	GPIO18	SPI1_CE0_N
CE1	P1-11	GPIO17	SPI1_CE1_N
CE2	P1-36	GPIO16	SPI1_CE2_N

Linux driver

The default Linux driver is `spi_bcm2708` (<https://github.com/raspberrypi/linux/blob/rpi-3.6.y/drivers/spi/spi-bcm2708.c>).

SPIo is disabled by default. To enable manually you must add

```
dtparam=spi=on
```

on `/boot/config.txt` file.

To enable SPI1, you can use 1, 2 or 3 chip select lines, adding in each case:

```
dtoverlay=spi1-1cs #1 chip select
dtoverlay=spi1-2cs #2 chip select
dtoverlay=spi1-3cs #3 chip select
```

on `/boot/config.txt` file.

The following information was valid from 2013-05-15.

Master modes

▪ Standard mode

In Standard SPI master mode the peripheral implements the standard 3 wire serial protocol. Signal names: Clock=CLK, ChipSelect=CE, SerialOut=MOSI (Master Out Slave In), SerialIn=MISO (Master In Slave Out)

▪ Bidirectional mode

In bidirectional SPI master mode the same SPI standard is implemented except that a single wire is used for the data (MIMO) instead of the two as in standard mode (MISO and MOSI). Signal names: Clock=CLK, ChipSelect=CE, SerialInOut=MOMI (Master Out Master In) or MIMO (Master In Master Out)

- **LoSSI mode** (Low Speed Serial Interface)

The LoSSI standard allows us to issue commands to peripherals and to transfer data to and from them.

LoSSI commands and parameters are 8 bits long, but an extra bit is used to indicate whether the byte is a command or data.

This extra bit is set high for a parameter and low for a command. The resulting 9-bit value is serialized to the output.

When reading from a LoSSI peripheral the standard allows us to read bytes of data, as well as 24 and 32 bit words.

Signal names: Clock=SCL, ChipSelect=CS, SerialOut=SDA (Serial DAtA)

The signal name SDA indicates that this could be a bidirectional bus.

The Nokia 5800 [schematics](http://www.shrak-mobile.com/eng/schem_nokia.html) (http://www.shrak-mobile.com/eng/schem_nokia.html) shows LoSSI Data In and LoSSI Data Out as connected.

This [post](http://www.raspberrypi.org/phpBB3/viewtopic.php?p=262818#p262818) (<http://www.raspberrypi.org/phpBB3/viewtopic.php?p=262818#p262818>) also supports this.

Transfer modes

- Polled
- Interrupt
- DMA

Speed

The CDIV (Clock Divider) field of the CLK register sets the SPI clock speed

$SCLK = \text{Core Clock} / CDIV$
 If CDIV is set to 0, the divisor is 65536. The divisor must be a power of 2. Odd numbers rounded down. The maximum SPI clock rate is of the APB clock.

Errata (http://elinux.org/BCM2835_datasheet_errata): "must be a power of 2" probably should be "must be a multiple of 2"

Chip Select

The main controller SPI0 supports 3 Chip selects, but only 2 are available on the header (GPIO08 for SPI0_CEO_N and GPIO07 for SPI0_CE1_N). For SPI1 are 3 chip selects on the P1 header (GPIO18 for SPI1_CEO_N, GPIO17 for SPI1_CE1_N and GPIO16 for SPI1_CE2_N), but you can use 2 or 3 pin overlay versions.

Setup and Hold times related to the automatic assertion and de-assertion of the CS lines when operating in **DMA** mode (DMAEN and ADCS set) are as follows:

- The CS line will be asserted at least 3 core clock cycles before the msb of the first byte of the transfer.
- The CS line will be de-asserted no earlier than 1 core clock cycle after the trailing edge of the final clock pulse.

Speed

The driver supports the following speeds

cdiv	speed
2	125.0 MHz
4	62.5 MHz
8	31.2 MHz
16	15.6 MHz
32	7.8 MHz
64	3.9 MHz
128	1953 kHz
256	976 kHz
512	488 kHz
1024	244 kHz
2048	122 kHz
4096	61 kHz
8192	30.5 kHz
16384	15.2 kHz
32768	7629 Hz

When asking for say 24 MHz, the actual speed will be 15.6 MHz. The fastest reported working speed is 32 MHz.

SPI has more speeds (<http://www.raspberrypi.org/phpBB3/viewtopic.php?f=44&t=43442&p=347073>)

Supported Mode bits

- SPI_CPOL - Clock polarity
- SPI_CPHA - Clock phase
- SPI_CS_HIGH - Chip Select active high
- SPI_NO_CS - 1 dev/bus, no chipselect

Supported bits per word

- 8 - Normal
- 9 - This is supported using LoSSI mode.

Transfer modes

Only interrupt mode is supported.

Deprecated

The following appears in the kernel log on Linux version 3.6.11+

```
bcm2708_spi bcm2708_spi.0: master is unqueued, this is deprecated
```

SPI driver latency

This [thread](http://www.raspberrypi.org/phpBB3/viewtopic.php?f=44&t=19489) (<http://www.raspberrypi.org/phpBB3/viewtopic.php?f=44&t=19489>) discusses latency problems.

This [driver](https://github.com/msperl/linux/blob/rpi-3.6.y/drivers/spi/spi-bcm2708.c) (<https://github.com/msperl/linux/blob/rpi-3.6.y/drivers/spi/spi-bcm2708.c>) proposes a solution to those problems ([Pull Request](https://github.com/raspberrypi/linux/pull/147) (<https://github.com/raspberrypi/linux/pull/147>)). It also solves the deprecation problem.

DMA capable driver

<https://github.com/notro/spi-bcm2708> (wiki (<https://github.com/notro/spi-bcm2708/wiki>))

Loopback test

This can be used to test SPI send and receive. Put a wire between MOSI and MISO. It does not test CEO and CE1.

```
wget https://raw.githubusercontent.com/torvalds/linux/master/tools/spi/spidev_test.c
gcc -o spidev_test spidev_test.c
./spidev_test -D /dev/spidev0.0
```

If you get SPI_TX_QUAD undeclared, use this instead

```
wget https://raw.githubusercontent.com/raspberrypi/linux/rpi-3.10.y/Documentation/spi/spidev_test.c
```

Software

- [pigpio](http://abyz.co.uk/rpi/pigpio/index.html) (<http://abyz.co.uk/rpi/pigpio/index.html>) provides access to both the main and auxiliary SPI interfaces available on Pi's with the 40 pin expansion header.
- [wiringPi](http://wiringpi.com/) (<http://wiringpi.com/>)
- Shell

```
# Write binary 1, 2 and 3
echo -ne "\x01\x02\x03" > /dev/spidev0.0
```

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