Feature

- Timing may be based on seconds 32.768kHz crystal, minutes, hours, weeks, days, months and years
- With century mark
- Wide operating voltage range: 2.0 ~ 5.5V
- Low Sleep Current: typ 0.25μA (V_{DD} = 3.0V, T_A = 25 ℃)
- I2C-bus slave address: read, 0A3H; write, 0A2H
- Programmable clock output frequency: 32.768kHz, 1024Hz, 32Hz, 1Hz
- Alarm and timer
- Brownout detector
- Integrated internal oscillation capacitor
- Package: DIP8 , SOP8 with MSOP8
- Open-drain interrupt pin

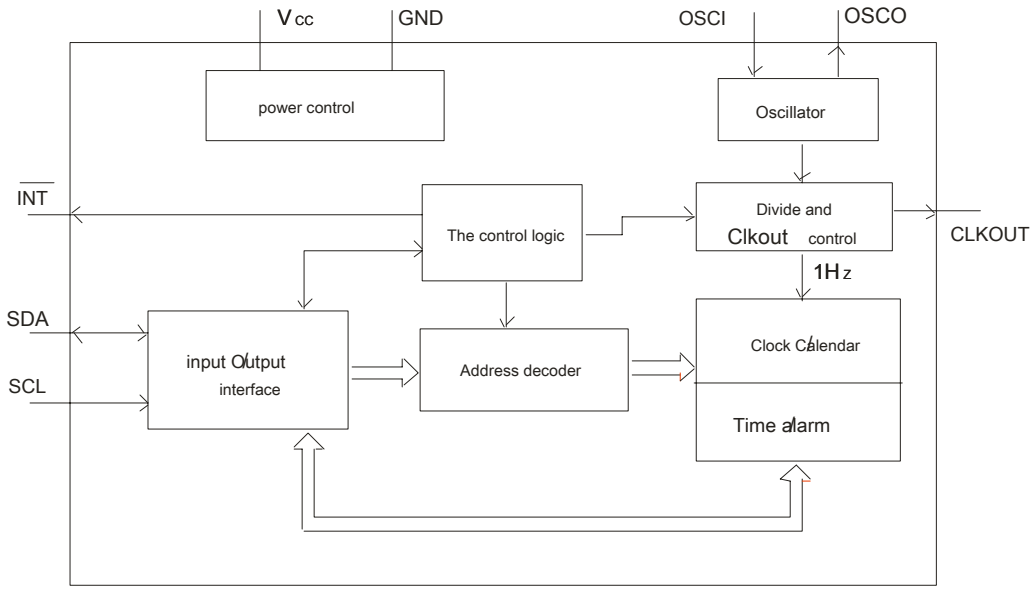
application

- Portable Instruments
- mobile phone
- Access
- Multi-rate meter, IC cards meters, IC card gas meter
- fax machine

Outline

HYM8563 is a low power CMOS real-time clock / calendar chip, which provides a programmable clock output, and an interrupt output of a brown-out detector, all address and data through I2C bus interface serial transmission. The maximum speed of the bus 400Kbits / s, after each read and write data, the embedded word address is automatically incremented.

Function block diagram and pin



Map 1. Block diagram

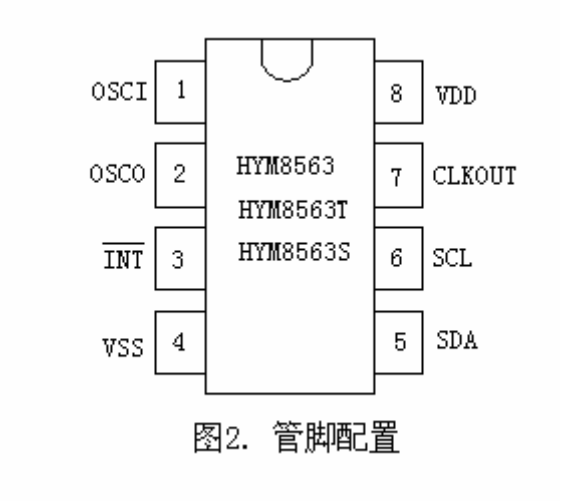


图2. 管脚配置

Pin Description

Pin No.	Symbol	Functional Description	Pin No.	Symbol	Functional Description
1	OSCI	oscillator input	5	SDA	Serial Data I / O
2	OSCO	Oscillator output	6	SCL	Serial clock input
3	$\overline{INT}$	Interrupt output (open drain)	7	CLKOUT	clock output (open drain)
4	V_{SS}	Ground	8	V_{DD}	Positive supply

Maximum Ratings

parameter	symbol	Minimum	Maximum	unit
voltage	V_{DD}	-0.5	+6.5	V
Supply Current	I_{DD}	--50	+ 50	mA
SCL with SDA Pin input voltage	V_I	-0.5	+6.5	V
OSCI Pin input voltage		-0.5	V_{DD} + 0.5	V
CLKOUT with Pin output voltage $\overline{INT}$	V_O	-0.5	+6.5	V
All input DC input current	I_I	--10	+ 10	mA
DC output current of all output ports	I_O	--10	+ 10	mA
The total power loss	P	-	300	mW
Operating temperature	T_A	- 40	+ 85	℃
Storage temperature	T_S	- 65	+150	℃

Electrical Characteristics

DC characteristics (Unless otherwise specified, V_{DD} = 1.8 ~ 5.5V , V_{SS} = 0V ; T_A = - 40 ~ + 85 Deg.] C; F_{osc} = 32.768kHz; quartz wafer Rs = 40kΩ, C_L = 8pF)

parameter	symbol	Test Conditions	Min	Typ	Max	Units
power supply						
Operating Voltage	V_{DD}	I^2C Bus failure, T_A = 25 Deg.] C [1]	1.8	-	5.5	V
		I^2C Bus effective, f = 400kHz [1]	2.0	-	5.5	V
When providing a reliable clock / calendar data operating voltage		T_A = 25 ℃	V_{low}	-	5.5	V
Working current 1	I_{DD1}	f_{SCL} = 400kHz	-	-	800	μA

CLKOUT effective(FE = 1)		f SCL = 100kHz	-	-	200	μ A
Working current 2 CLKOUT Prohibition (FE = 0)	I DD2	f SCL = 0Hz , T A = 25 Deg.] C [2]				
		V DD = 5.0V	-	275	550	nA
		V DD = 3.0V	-	250	500	nA
		V DD = 2.0V	-	225	450	nA
		f SCL = 0Hz , T A = - 40 ~ + 85 Deg.] C [2]				
		V DD = 5.0V	-	500	750	nA
		V DD = 3.0V	-	400	650	nA
		V DD = 2.0V	-	400	600	nA
Working current 3 CLKOUT = 32.768kHz	I DD3	f SCL = 0Hz , T A = 25 Deg.] C [2]				
		V DD = 5.0V	-	825	1600	nA
		V DD = 3.0V	-	550	1000	nA
		V DD = 2.0V	-	425	800	nA
		f SCL = 0Hz , T A = - 40 ~ + 85 Deg.] C [2]				
		V DD = 5.0V	-	950	1700	nA
		V DD = 3.0V	-	650	1100	nA
		V DD = 2.0V	-	500	900	nA
Entry						
Low level input voltage	V IL		V SS	-	0.3V DD	V
High-level input voltage	V IH		0.7V DD	-	V DD	V
Input leakage current	I LI	V I = V DD or V SS	- 1	0	+ 1	μ A
Input capacitance	C I	[3]	-	-	8	pF
Export						
SDA low level output current	I OLS	V OL = 0.4V , V DD = 5.0V	--3	-	-	m A
$\overline{INT}$ Low Output Current	I OLI	V OL = 0.4V , V DD = 5.0V	- 1	-	-	m A
CLKOUT low level output current I OLC		V OL = 0.4V , V DD = 5.0V	- 1	-	-	m A
High CLKOUT output current I OHC		V OL = 4.6V , V DD = 5.0V	1	-	-	m A
Output leakage current	I LO	VO = V DD or V SS	- 1	0	+ 1	μ A
Voltage detector						
Brownout detection voltage	V LOW	T A = 25 ℃	-	0.9	1.0 V	

1 When reliable starting power oscillator: V DD (Minimum at power) = V DD (Min) + 0.3V 2 , The timer clock source

= 1 / 60Hz ; SCL with SDA Are V DD

3 , On the basis of the test sample

AC Characteristics (Unless otherwise specified, V DD = 1.8 ~ 5.5V , V SS = 0V ; T A = - 40 ~ + 85 Deg.] C; F osc = 32.768kHz; quartz Rs = 40k

Ω, C L = 8pF)

parameter	symbol	Test Conditions	Min	Typ	Max	Units
Oscillator						
Precise load capacitance	C INT		15	25	35	pF
Oscillator stability	Δf OSC / f OSC	ΔV DD = 200mV, T A = 25 ℃ -		2 × 10- 7	-	-
Quartz crystal parameters (f = 32.768kHz)						
Series resistance	R S		-	-	40	k Ω
Parallel load capacitance	C L		-	10	-	pF

Trimmer	C_T		5	-	25	pF
CLKOUT Export						
CLKOUT Duty cycle δ_{CLKOUT}		[1]	-	50	-	%
I2C Bus timing characteristics [twenty three]						
SCL Clock cycle	f_{SCL}	[4]	-	-	400	kHz
Retention time starting conditions	t_{HDSTA}		0.6	-	-	μs
Repeat start condition setup time	t_{SUSTA}		0.6	-	-	μs
SCL Low Time	t_{LOW}		1.3	-	-	μs
SCL High Time	t_{HIGH}		0.6	-	-	μs
SCL with SDA The rising edge time	t_r		-	-	0.3	μs
SCL with SDA Of falling time	t_f		-	-	0.3	μs
Bus load capacitance	C_b		-	-	400	pF
Data setup time	t_{SUDAT}		100	-	-	ns
Data Hold Time	t_{HDDAT}		0	-	-	ns
Stop Condition Setup Time	t_{SUSTO}		0.6	-	-	μs
Acceptable bus spike width	t_{SW}		-	-	50	ns

1 No special instructions f_{CLKOUT} = 32.768kHz 2 , The timing of all values within the operating voltage range (T_A) Under the conditions valid, the reference voltage input V_{SS} To V_{DD} Change is between V_{IL} with V_{IH} The value

3 , I2C Bus access time at a start and a stop two conditions must be less than 1s

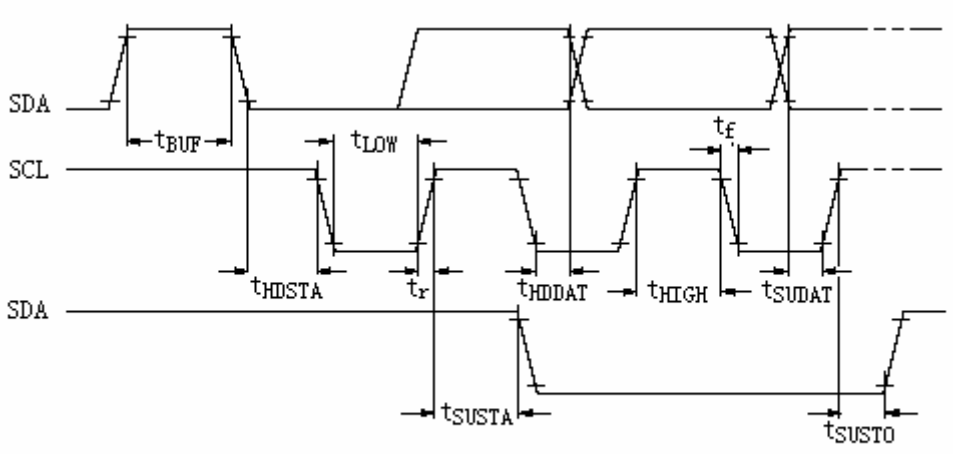


图3. I^2C总线时序波形

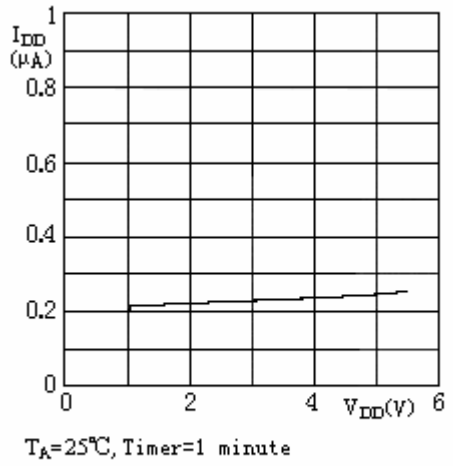


图4. CLKOUT禁止时，IDD与VDD的关系图

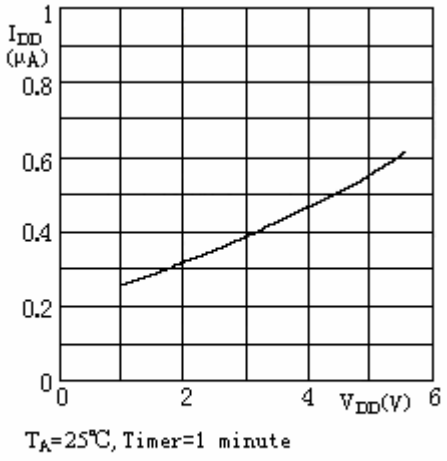


图5. CLKOUT=32.768kHz，
IDD与VDD的关系图

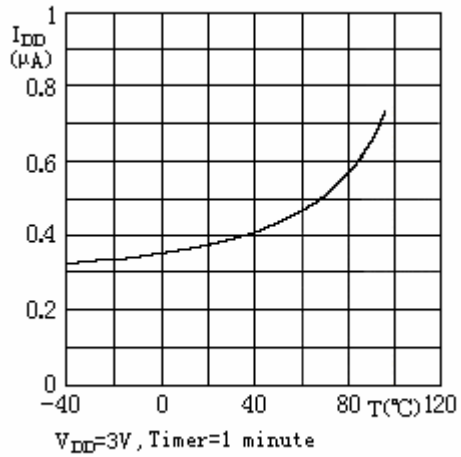


图6. CLKOUT=32.768kHz，IDD与TA关系图

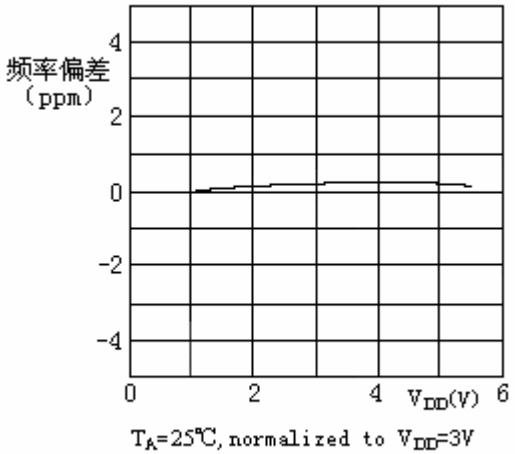


图7. 频率偏差与VDD的关系图

Functional Description

HYM8563 Have 16 More 8 Bit registers, an auto increment address register, a built- 32.768kHz Oscillator (with a Internal integrated capacitor), a divider (for the real-time clock RTC Providing the clock source), a programmable clock output, a timer, An alarm, a detector and a brownout 400kHz of I^2C Bus interface.

all 16 Registers designed to be addressable 8 Bit parallel register, but not all bits are used. Second register (internal address 00H , 01H) As a control and status registers, address 02H ~ 08H A clock counter (counter seconds to years), the address 09H ~ 0CH For alarm registers (defined alarm condition), the address 0DH For control CLKOUT Frequency output pins, the address 0EH with 0FH They are used as the timer control register and timer register. Second, minute, hour, day, month, year, alarm minute, alarm hour, daily Police encoding format register is BCD Code, weeks and days of the alarm registers are not to BCD Format encoding.

Alarm mode

One or more alarm registers MSB (AE = Alarm Enable Alarm Enable bit) clear 0 , The corresponding alarm conditions effective so that, An alarm is generated once in every minute to every week range. Set the alarm flag AF (Control / Status Register 2 Bit 3) For production Generate an interrupt, AF It can only be cleared by software.

Timer

8-bit down counter (address 0FH) by a timer control register (address 0EH, see Table 22) control, timer control register The frequency (4096Hz, 64Hz, 1Hz or 1 / 60Hz) set timer, setting the timer and a valid or invalid. Timer set from the software When set, 8-bit binary countdown, each end count down, timer flag TF (see Table 4), TF for generating an interrupt (), Each countdown period to generate a pulse as an interrupt signal, the timer flag TF can only be cleared by software. TI / TP (see Table 4) control condition interrupt generation. When reading the timer, it returns the value of the current countdown.

CLKOUT output

CLKOUT output pin may be a programmable square wave. CLKOUT frequency register (address 0DH, see Table 20) determines the output frequency of the square wave Rate may be output 32.768kHz (default value), 1024Hz, 32Hz, and the square wave of 1Hz. When the open-drain output pin CLKOUT, the energization Effective, high impedance invalid.

Reset

Built HYM8563 a reset circuit, when the oscillator is stopped, the reset circuit to work. In the reset state, I^2C bus is early Initialization, all registers (including address pointer) in addition to TF, VL, TD1, TD0, TESTC, AE bit is set to logic 1, but will be cleared.

Register Structure

Table 1. Overview Register

Marked "-" invalid bit marked "0" bit shall be set to logic 0.

address	Register Name	Bit7	Bit6	Bit5		Bit4	Bit3	Bit2	Bit1	Bit0	
00H	Control / Status Register 1	1	0	0		0	0	0	0	0	0
01H	control / status register 2	0	0	0		TI / TP	AF	TF	AIE		TIE
0DH	CLKOUT frequency register FE		-	-		-	-	- FD1			FD0
0EH	timer control register	TE	-	-		-	-	- TD1			TD0
Countdown timer register 0FH		Countdown timer value									

Table 2.BCD pattern register before

Marked "-" bit is invalid

address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02H	second	-	00 ~ 59BCD yardage format						
03H	minute	-	00 ~ 59BCD yardage format						
04H	hour	-	-	00 ~ 23BCD yardage format					
05H	day	-	-	01 ~ 31BCD code number format					
06H	week	-	-	-	-	-	0-6		
07H	Month / century	C	-	-	01 ~ 12BCD Code number format				
08H	year	00 ~ 99BCD yardage format							
09H	Minute alarm	AE	00 ~ 59BCD yardage format						
0AH	Hour alarm	AE	-	00 ~ 23BCD yardage format					
0BH	Day Alarm	AE	-	01 ~ 31BCD code number format					
0CH	Alarm week	AE	-	-	-	-	0-6		

Register 1

Table 3 1 register (address 00H) bit description

Bit No.	Symbol	description
7	1	Often read as 1
6 ~ 0		The default value of logic 0

Control / Status Register 2

TF bit and AF: When an alarm occurs, AF is set to logic 1. Similarly, at the end of the countdown timer, TF is set to Logic 1. These bits can only be modified by software. If both need to use timer and alarm interrupts in the application, you can read this Two bytes to determine the interrupt source. Bit is cleared in a write cycle, in order to prevent dirty bit needs to perform a logical AND operation.

Bits TIE and AIE: The two used to generate the active interrupt. When the AIE and TIE is set, the interrupt logic or two.

Table 4. Control / Status Register 2 (address 01H) bit description

Bit No.	Symbol	description
7,6,5		The default value of logic 0
4	TI / TP	TI / TP = 0: when TF valid, the INT active (depending on the state of TIE) TI / TP = 1: INT, pulse valid Table 5 (depending on the state of TIE) Note: If the AF and are valid AIE the INT has been effective
3	AF	AF = 0: read, the alarm flag is invalid; write operation, the alarm flag is cleared AF = 1: read operation, the alarm flag is enabled; write operation, the alarm flag remains unchanged
2	TF	TF = 0: read, the timer flag is invalid; write operation, the timer flag is cleared TF = 1: read operation, the timer flag valid; write operation, the timer flag remains unchanged
1	AIE	AIE = 0: alarm interrupt is disabled AIE = 1: alarm interrupt is enabled
0	TIE	TIE = 0: timer interrupts are disabled TIE = 1: Timer interrupt is enabled

Table 5. $\overline{INT}$ operation (bit TI / TP = 1)

Clock Source (Hz)	~ INT period [1]	
	n = 1 [2]	n> 1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1], and at the same time effective TF $\overline{INT}$

[2], n is the value of the timer countdown, when n = 0, the timer is stopped

Seconds, minutes and hours registers

Table 6. sec / VL register (address 02H) bit description

Bit No.	Symbol	description
6 ~ 0 (sec) represents the value of the current second BCD format, is 00 to 99, for example: 59 seconds 7 1011001 representatives		
	-	invalid

Table 7. min register (address 03H) bit description

Tag	symbol	description
7	-	invalid
6 ~ 0 (minute) Values represent the current minute BCD format, is 00 to 59		

Table 8. hour register (address 04H) bit description

Tag	symbol	description
7,6	-	invalid
5-0 (hour) BCD format representative of the current value of h, is 00 to 23		

Day, week, month / century and in register

9. epitope date register (address 05H) Description

Tag	symbol	description
7,6	-	invalid
5-0	Current date value (day) represents BCD format, is 01 to 31. Then the value of the counter is a leap year, the HYM8583 automatically increased to a value in February, making it 29 days	

10. epitope week register (address 06H) Description

Bit No.	Symbol	description
7 ~ 3	-	invalid
2 ~ 0	(week)	Value represents the current week, value of 0 to 6. Table 11, these bits may reallocate users

Table 11. week allocation table

day	Bit 2	Bit 1	Bit 0
on Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
on Saturday	1	1	0

12. epitope month / century register (address 07H) Description

Tag	Symbol	Description
7	C	Bit Century: C = 0 is specified centuries 20XX; C = 1 is designated centuries 19XX, "XX" is the value of the register, see Table 14. When the year changed from 99 00 Century will change.
6,5	-	invalid
4 ~ 0	(Month)	represents the value of the current month in BCD format, the value of 01 to 12, see Table 13

Table 13. month allocation table

month	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 14. In register (address 08H) bit description

Tag	symbol	description
7-0	(Years)	represents the value of the current year BCD format, is 00 to 99

Alarm Control Register

When one or more alarms minutes register write legitimate, hours, days or weeks and their respective value AE (Alarm Enable)

Bit is a logic 0, and these values and the current minute hours, days or weeks value equal to, flag AF (Alarm Flag) is set,

AF is eliminated until the setting values are saved until the software, the AF is cleared only when the alarm time increments that match the criteria is set again before then

Home. Alarm registers to logic 1 will be ignored in their respective AE bit is set.

Table 15. minute alarm register (address 09H) bit description

Tag	symbol	description
7	AE	AE = 0, the effective alarm min; AE = 1, the alarm minute Invalid
6 ~ 0	Minute alarm	Representative BCD format minutes alarm value is 00 to 59

Table 16. Bit hours alarm register (address 0AH) Description

Tag	symbol	description
7	AE	AE = 0, the alarm hour effective; AE = 1, the alarm hour invalid
twenty three	Hour alarm	Representative hours in BCD alarm value is 00 to 59

Table 17. Day alarm register (address 0BH) bit description

Tag	symbol	description
7	AE	AE = 0, the effective daily alarm; AE = 1, the date is invalid alarm
6 ~ 0	Day	Day BCD format representative of the alarm the alarm value is 00 to 31

Table 18. Alarm week register (address 0CH) bit description

Tag	symbol	description
7	AE	AE = 0, Alarm week effective; AE = 1, the alarm Invalid week
6 ~ 0	Alarm week	Representative BCD format week alarm value is 00 to 59

CLKOUT frequency register

Table 19.CLKOUT frequency register (address 0DH) bit description

Tag	symbol	description
7	FE	FE = 0: CLKOUT output is disabled and a high impedance FE = 1: CLKOUT output valid
6 ~ 2	-	invalid
1	FD1	Frequency output pin (f for controlling the CLKOUT $_{CLKOUT}$), See Table 20
0	FD0	Frequency output pin (f for controlling the CLKOUT $_{CLKOUT}$), See Table 20

Table 20.CLKOUT frequency selection table

FD1	FD0	f_{CLKOUT}
0	0	32.768kHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

Countdown timer register

Timer register is an 8-bit byte count down timer, which timer TE is determined by the position controller valid or invalid, the timer

Clock timer may be selected by the controller, the other timer functions, such as interrupt generation, 2 controlled by the control / status register. In order to

Accurate readback countdown value, I 2 C SCL bus clock frequency should be at least twice the clock frequency of the selected timer.

Table 21. Timer Control Register (address 0EH) Description

Tag	symbol	description
7	TE	TE = 0: timer is invalid; TE = 1: Timer Active
6 ~ 2	-	useless
1	TD1 0	Timer clock frequency select bits, the clock frequency determines the countdown timer, see Table 22, when not TD1
		and TD0 should be set to "11" (1 / 60Hz), to reduce power consumption

Table 22. Timer selected clock frequency

TD1	TD0	Timer clock frequency (Hz)
0	0	4096
0	1	64
1	0	1
1	1	1/60

Table 23. countdown timer value register (address 0FH) Bit Description

Tag	symbol	description
7-0	Countdown timer value	Down count number "n", the count down period = n / clock frequency

Serial Interface

HYM8563 uses a serial I 2 C bus interface.

I 2 C Bus Characteristics

I 2 C bus to transfer information between different chips and modules via two lines SDA and SCL. SDA serial data line, the SCL for the serial clock line,

Two lines have pull-up resistor is connected with a positive supply. Data transmission is only available when the bus is not busy.

System configuration Referring to FIG 10, the information generating device is a transmitter, the device is a receiver receiving information, device control information is a master device,

The device is controlled from the device.

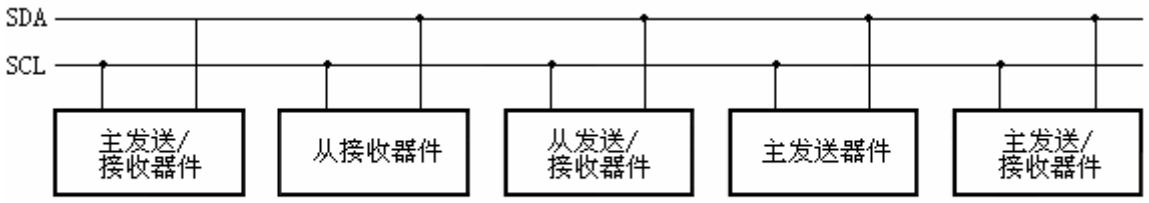


图10. I2C总线系统配置图

Start (START) and stop (STOP) conditions

When the bus is not busy, data and clock lines remain high, the data line is high for the start condition (S) at the falling edge, the clock line, the number of

The rising edge of the data line, clock line stop condition (P) see FIG. 11 at a high level.

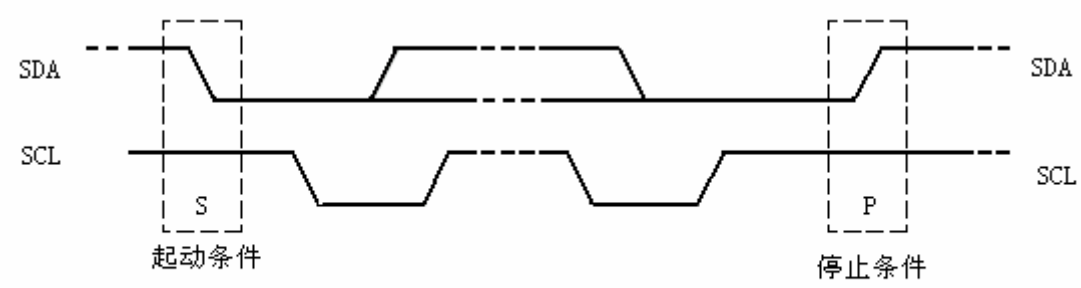


图11：I2C总线的起动（START）和停止（STOP）条件定义

Bit transfer

Each bit of a data transfer clock pulse, the data on the SDA line is stable when the clock pulse is high, or the number of the SDA line

It will be the above-mentioned control signals, see Figure 12.

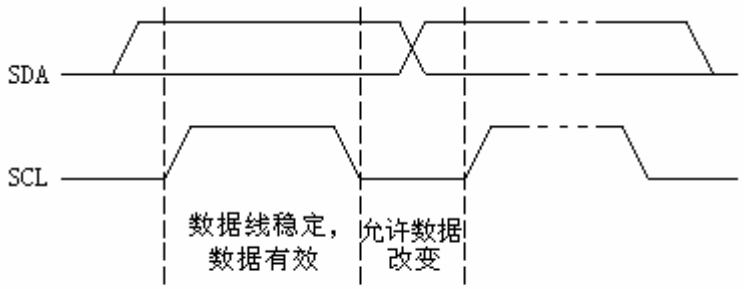


图12. I2C总线上的位传送

Acknowledge bit

Between the start and stop conditions is sent to the transmitter number data receiver is not limited. Plus a response after each 8-bit byte flag

Bit, the transmitter generates a response flag high, then the master generates a clock pulse additional marker responses. Receiving from the receiver must be in the

To generate an acknowledge after each byte flag, a main receiver must be generated after the reception of each byte transmitted from the transmitter a response flag

Bit. When the response flag bit clock pulses, SDA line should be kept low (start-up and hold time should be considered). The transmitter should be in the feeder

From the device receives the last byte to the low level, so that the receiver generates a response flag, then the master may generate a stop condition.

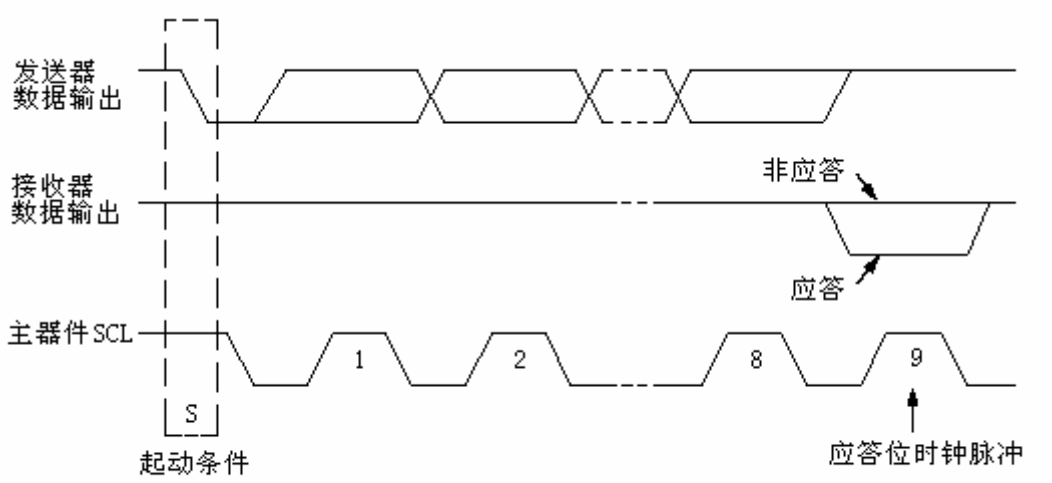


图13. I2C总线的应答位

I 2 C bus protocol

Note: I use 2 C-bus before data transmission, the receiving device should indicate the address in the I 2 After starting C-bus, the first transfer word address

Section are transmitted together. HYM8563 as from a receiver or from the transmitter, this time, only the clock signal line SCL line is an input signal, the number of

According to the signal line SDA is a bidirectional signal line.

Referring to FIG HYM8563 from address 14.

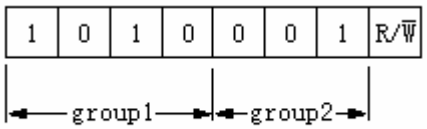


图14. 从地址

Read a clock / calendar / write cycles

HYM8563 Serial I 2 C Bus read / write cycle in three configurations, see Fig. 15 , 16 , 17 FIG address word 4 A number of bits, with

Pointing out the high-bit register to access the next word address useless.

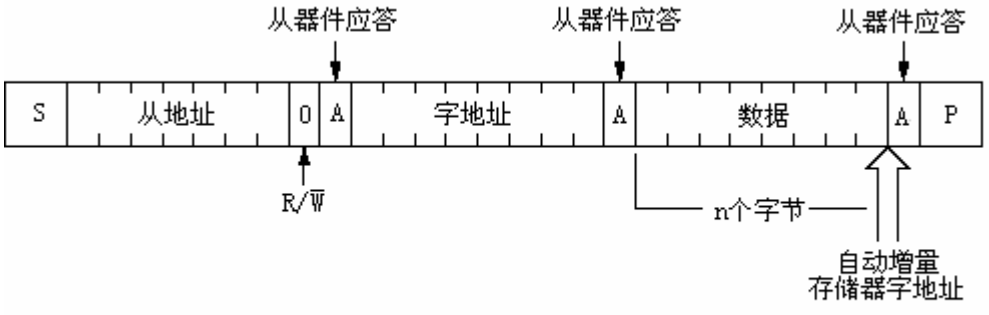


图15. 主发送器到从接收器（写模式）

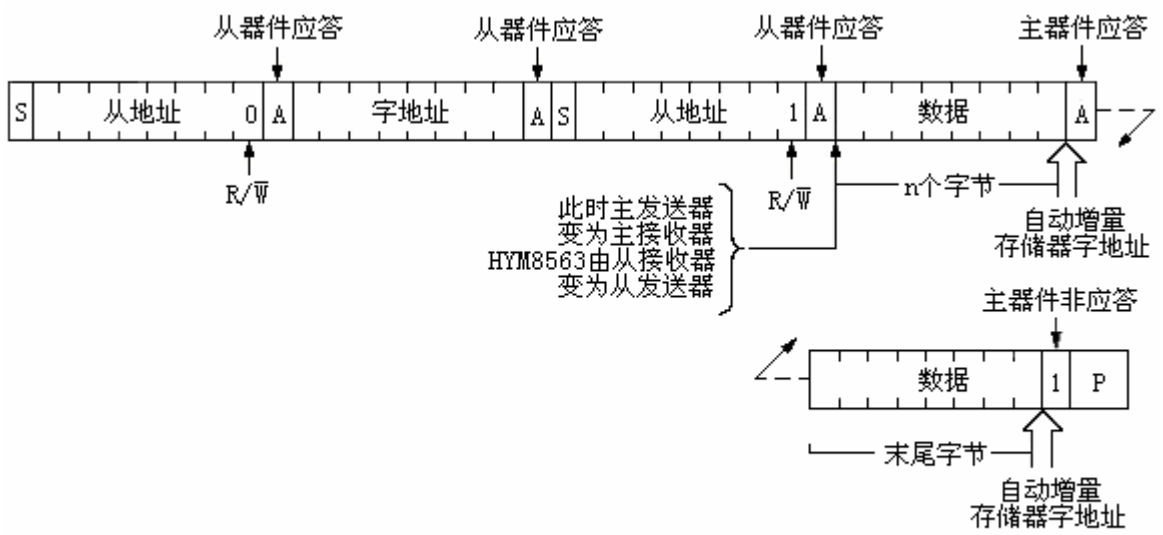


图16.设置字地址后主器件读数据（写地址，读数据）

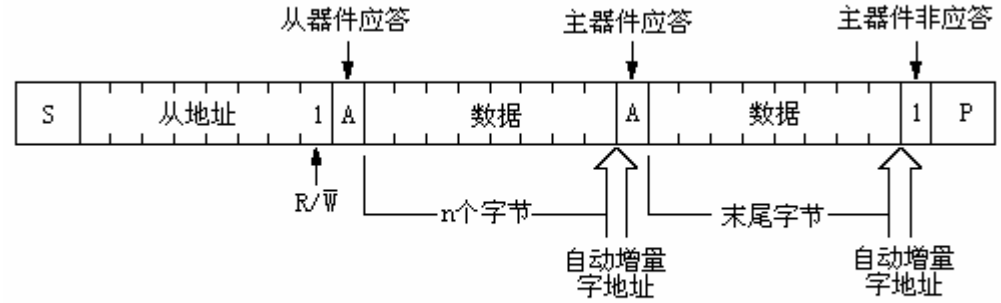
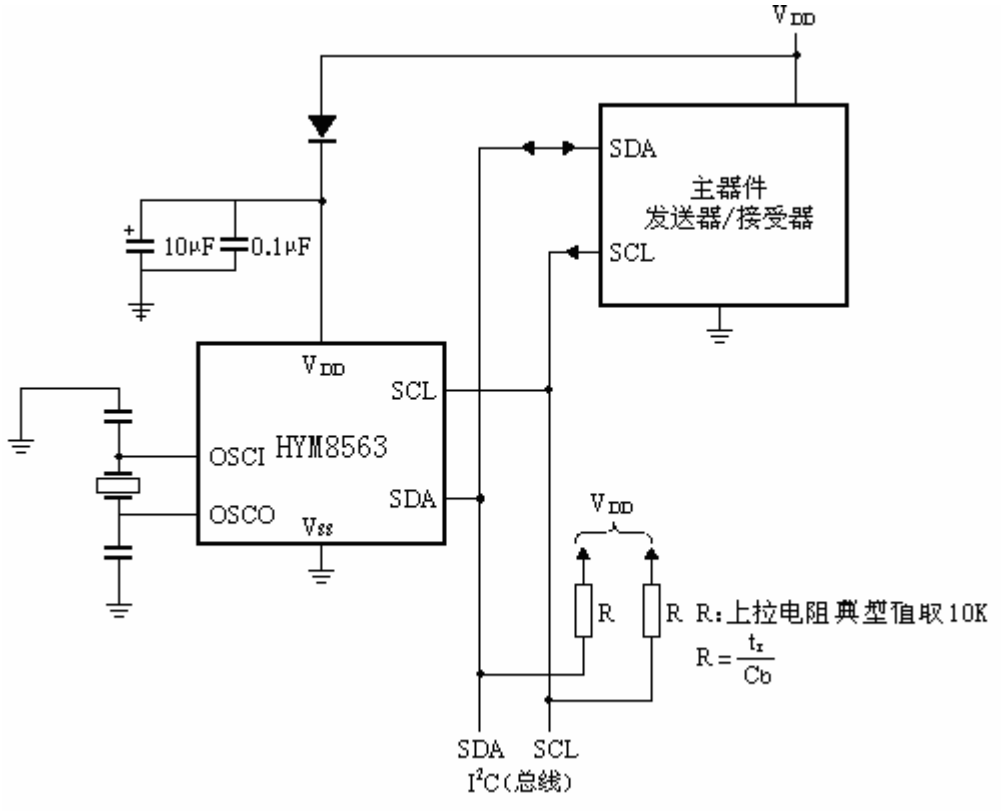


图17. 主器件读从器件第一个字节数据后的数据（读模式）

Typical application circuit



Quartz crystal frequency adjustment

Method 1: OSCI capacitance value - average value of capacitance required for the calculation, by setting the value of the capacitance measured after power on pin CLKOUT The frequency should be 32.768kHz, the measured frequency deviation depends on the difference between the quartz crystal, and the device capacitance deviation (mean ± 5 × 10-6). The average deviation can be controlled within ± 5 min / years.

Method 2: OSCI trimmer - trimming capacitance by adjusting the oscillator frequency so that pin OSCI achieve precise value can be measured when energized The frequency of the CLKOUT pin is 32.768kHz.

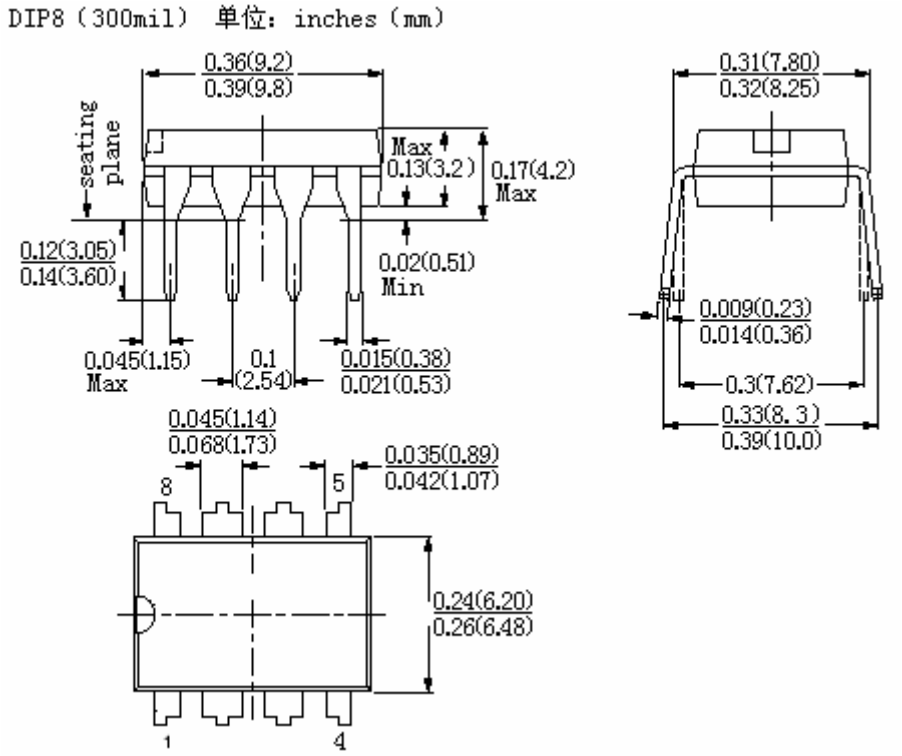
Method 3: OSCO Output - OSCO measured directly (taking into account the capacitance test probe).

Ordering Information

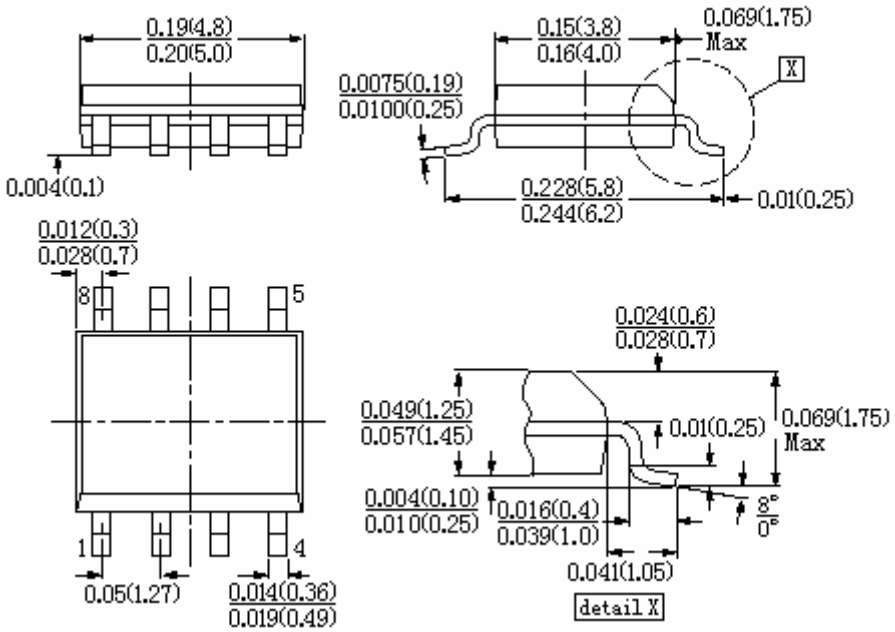
model	temperature range	Package
HYM8563	- 40 ~ + 85 ℃	DIP8
HYM8563T		SOP8
HYM8563S		MSOP8

Package size

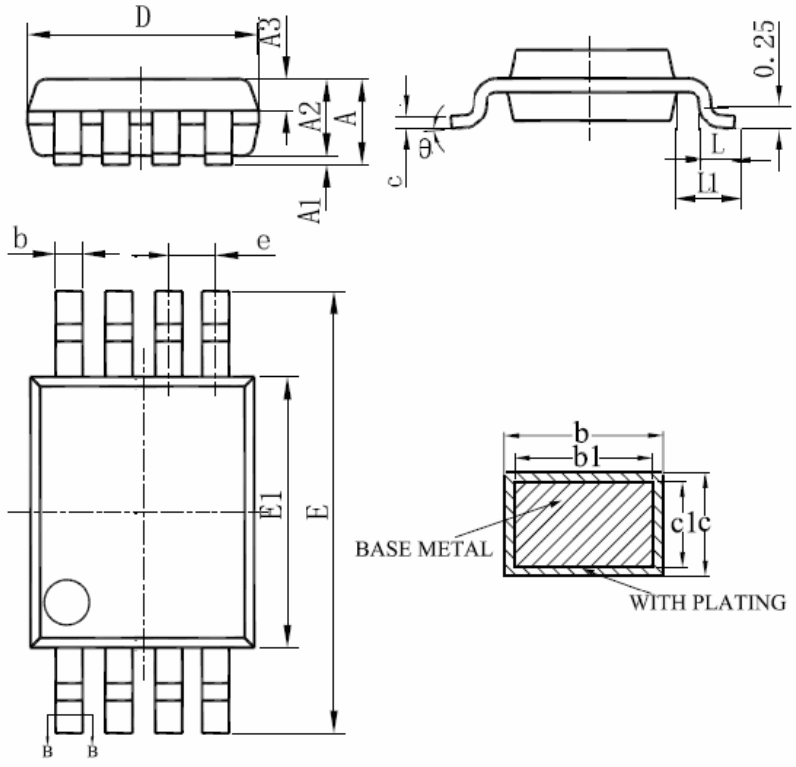
DIP8（300mil） 单位：inches（mm）



SOP8 单位：inches（mm）



MSOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.29	—	0.38
b1	0.28	0.30	0.33
c	0.15	—	0.20
c1	0.14	0.152	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	71*96		