AiP8563 I 2 C Real-time

clock / calendar circuit

Pr uct M ual

Instructions issuance records:

version	publish time Fresh / amendments	
trial version	2016-06	New system

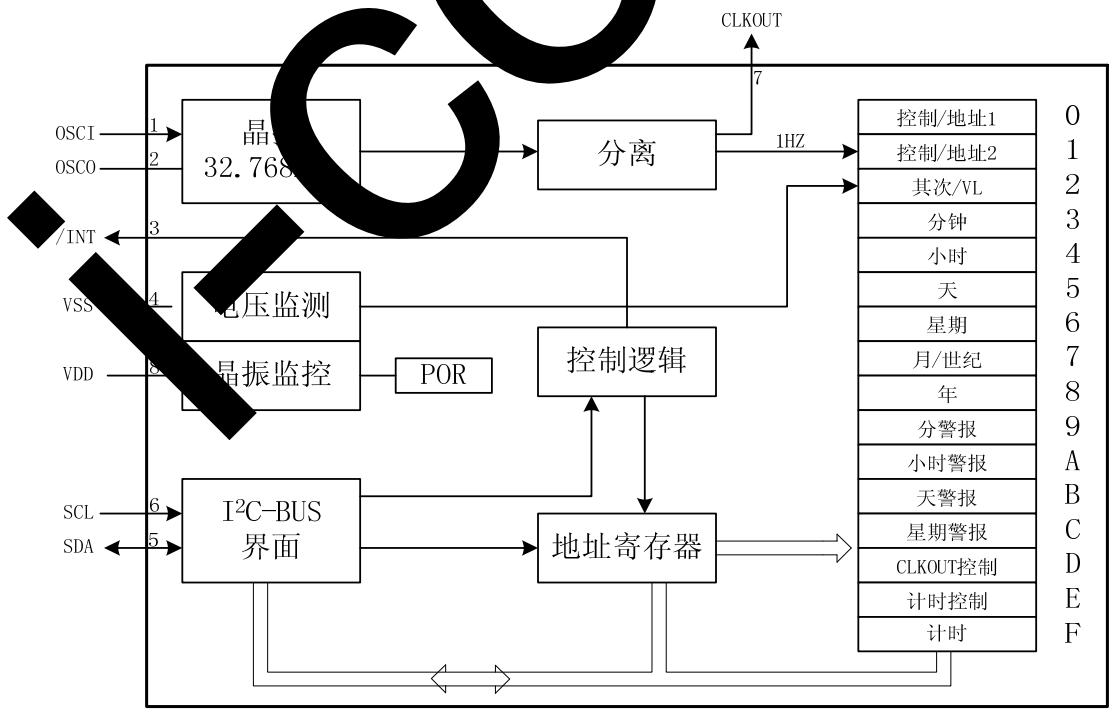
1 An overview

AiP8563 Low power consumption CMOS Real-time clock / calendar chip, which provides a programmable clock output, interrupt output and a brown-out detector, all address and data I 2 C Transmitting serial bus interface. The maximum bus speed 400Kbits / s After each read and write data, the embedded word address register automatically increments generated. Widely used in mobile phones, portable devices, fax machines, battery power products. Its main features are as follows:

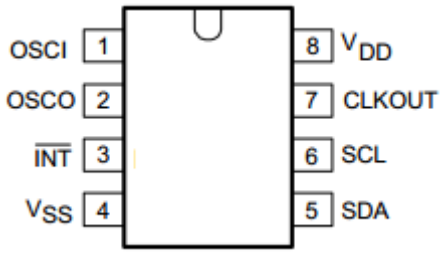
- Low Operating Current: typ 0.25μ A (VDD = 3.0V , Tamb = 25 ℃ Time)
- Century mark
- Large operating voltage range: 1.0 ~ 5.5V
- Low current sleep; typical value 0.25μA (VDD = 3.0V, Tamb = 25) ℃
- 400KHz of I 2 C Bus Interface (VDD = 1.8 ~ 5.5V Time)
- Programmable clock output frequency is: 32.768KHz , 1024Hz , 32Hz , 1Hz
- Alarm and timer
- Brownout detector
- Internally integrated oscillator capacitor
- Power chip reset
- I 2 C Bus from Address: Reading, 0A3H ;write, 0A2H
- Open-drain interrupt pin
- Package: DIP8 SOP8

2 Functional block diagram and pin description

2.1 Functional block diagram



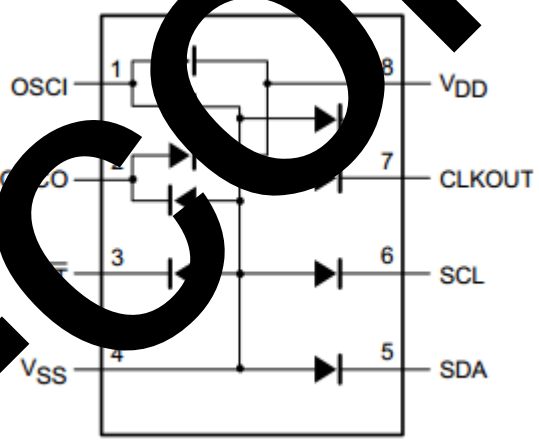
2.2 Pinout FIG.



Map 1 : Pin Figure

2.3 , And pin diode protection described in FIG.

Pin	symbol	Features
1	OSCI	Oscillator input
2	OSCO	Oscillator output
3	/ INT	Interrupt outp in: active low)
4	VSS	G
5	SDA	Ser ta I / O
6	SCL	al clock input
7	CLKOUT	Clo m)
8	VDD	Positive supply



Map 2 : FIG diode protection

3 Electrical characteristics

3 , 1 Limit parameters

Unless otherwise specified, T_{amb} = 25 ℃

parameter name	Symbol maximum		Minimum Units	
voltage	V_{DD}	-0.5	+6.5	V
Supply Current	I_{DD}	--50	+ 50	mA

SCL with SDA Input voltage input pin	V_I	-0.5	+6.5	V
OSCI Output voltage input pin		-0.5	V_{DD} + 0.5	V
CLKOUT with/ INT The output voltage output pin	V_O	-0.5	+6.5	V
All input DC input current	I_I	--10	+ 10	mA
DC output current of all output ports	I_O	--10	+ 10	mA
Power	P_D	-	300	mW
Working temperature	T_{amb}	- 40	+ 85	℃
Storage temperature	T_{stg}	- 65	+150	℃

3.2 Electrical Characteristics

3.2.1. Static characteristics (Unless otherwise specified, T_{amb} = - 40 + 85 ℃, V_{DD} = 1.8 ~ 5.5V , V_{SS} = 0V; Fosc = 32.768KHZ; Quartz wafers

R_S = 40KΩ; C_1 = 8pF)

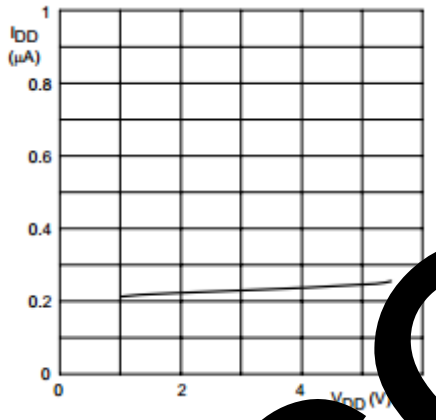
parameter name	symbol	Test Conditions		ical Minimum	Units	
Operating Voltage	VDD	I2 C Bus invalid T_{amb} = 25 ℃ 1.(			5.5 V	
		I2 C Bus effective f_{SCL} = 400(		(1)	5.5 V	
Provide reliable clock, calendar data When operating voltage		T_{amb} = 2(		-	5.5 V	
Working current: CLOCK Failure (FE = 0)	I_{DD1}	f SCL 400KHZ	-(2)	- 800		uA
		SCL = T(Z	-	- 200		uA
		L = 0KHZ T_{amb} = C	(2)			
		VDD = 5V	-	275	550	nA
		VDD = 3V	-	250	500	nA
			-	225	450	nA
		f_{SCL} = 0KHZ	(2)			
		VDD = 5V	-	500	750	nA
		VDD = 3V	-	400	650	nA
		VDD = 2V	-	400	600	nA
Working current: CLOCKOUT effective $F_{CLOCKOUT}$ = 32KHZ (FE = 1)	I_{DD2}	f_{SCL} = 0KHZ T_{amb} = 25 ℃	(2)			
		VDD = 5V	-	825	1600	nA
		VDD = 3V	-	550	1000	nA
		VDD = 2V	-	425	800	nA
		f_{SCL} = 0KHZ	(2)			
		VDD = 5V	-	950	1700	nA
		VDD = 3V	-	650	1100	nA
		VDD = 2V	-	500	900	nA
Entry						
Low level input voltage	V_{IL}		VSS	-	0.3VDD V	
High-level input voltage	V_{IH}		0.7VDD	- VDD		V

Input leakage current	I_{LI}	V_I = VDD or VSS	- 1	-	+ 1	uA
Input capacitance	C_I		-(3)	--7		pF
Export						
Low Output Current SDA	I_{OL}	V_{OL} = 0.4V VDD = 5V	--3	-	- mA	
Low output current / INT	I_{OL}		- 1	-	- mA	
Low Output Current CLKOUT	I_{OL}		- 1	-	- mA	
High Output Current CLKOUT	I_{OH}	V_{OH} = 4.6V VDD = 5V	1	-	- mA	
Output leakage current	I_{LO}	V_o = VDD or VSS	- 1	-	+ 1	uA
Voltage detector						
Brownout detection value	V_{LOW}	T_{amb} = 25 ℃	-	0.9	1.0 V	

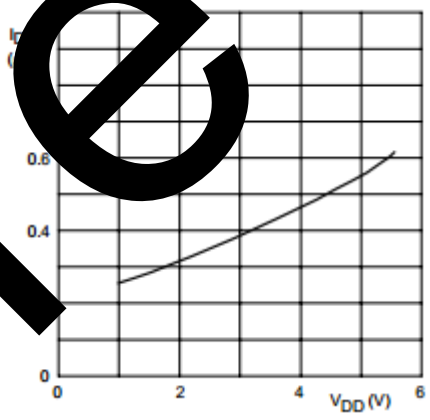
Remarks :(1) Reliable starting oscillator is powered: $V_{DD\ (Minimum;\ power\ up)} = V_{DD\ (Minimum)} + 0.3V$

(2) = Timer Source Clock 1 / 60HZ ; SCL with SDA = V_{DD}

(3) On the basis of the test sample



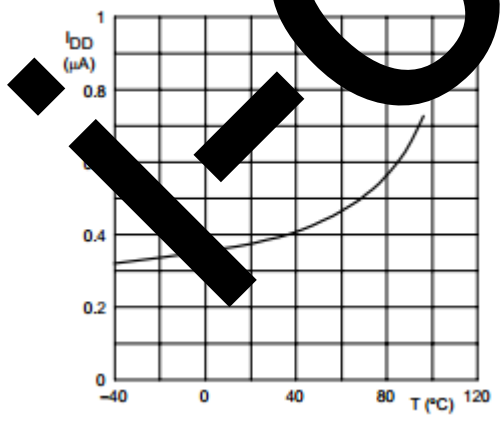
Map 3 : T_{AMB} = 25 ℃ ...e = 1 minute



Map 4 : T_{AMB} = 25; ℃ Time = 1 minute

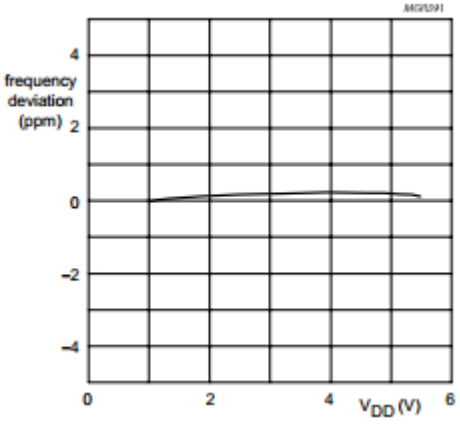
CLKOUT When failure; Note: IDD v... VDD relation chart

CLKOUT = 32kHz ;Note: IDD versus VDD relation chart



Map 5 : T_{AMB} = 25; ℃ Time = 1 minute

CLKOUT = 32kHz ;Note: IDD versus VDD relation chart



Map 6 : T_{AMB} = 25; ℃ Time = 1 minute

NOTE: Frequency deviation VDD The diagram

3.2.2. Dynamic characteristic (Unless otherwise specified, T_{amb} = - 40 + 85 ℃, V_{DD} = 1.8 ~ 5.5V , V_{SS} = 0V; Fosc = 32.768KHZ; Quartz wafers

R_S = 40KΩ; C_1 = 8pF)

parameter name	symbol	Test Conditions	Minimum	Typical	Maximum	Units
Oscillator						
Precise load capacitance	C_L		15	25	35	pF
Oscillator stability	Δ OfSC	Δ DbV = 200mV T = 25 ℃	-	2 * 10-7	-	
Quartz crystal parameters (Fosc = 32.768KHZ) Series						
resistance	R_S		-	- 40		KΩ
Parallel resistance	C_L		--10		- pF	
Adjustable capacitor	C_T		5	--25		pF
CLKOUT Export						
CLKOUT Function factor	δ_{CLKOUT}		-(1)	50	-%	
I2C Bus timing characteristics(2)						
SCL Clock frequency	f_{SCL}		-(3)	- 400		KHz
Start Condition Hold Time	$T_{HD;STA}$				- uS	
Repeat start generation time	$T_{SU;STA}$		0.6		- uS	
SCL Low Time	T_{LOW}			-	- uS	
SCL High Time	T_{HIGH}		0.6	-	- uS	
SCL with SDA Rise time	T_R		-	-	0.3 uS	
SCL with SDA Fall time	T_F		-	-	0.3 uS	
SD Bus load capacitance	C_b		-	- 400		pF
Data generated time	$T_{SU;DAT}$		100	-	-	ns
Time to keep data	$T_{HD;DAT}$		0	-	-	ns
Stop condition occurs time	$T_{SU;STO}$		4.0	-	- uS	
Acceptable bus width spike	T_{SW}		-	--50		ns

Remarks :(1) No special instructions f_{CLKOUT} = 3

(2) All timing values in the op voltage range (T_{amb} Under conditions) effective at the reference input voltage VSS with VDD between

n changes th V_{IH} Value.

(3) I2C Bu ss time must be less than one second in a two start or stop and start conditions

4 ,Features

AiP8563 Have 16 More 8 Bit registers: an auto increment address register, a built- 32.768KHz Oscillator (internal integrated with a capacitor), a frequency divider (real-time clock is used to RTC Providing a source clock), the output of a programmable clock, a timer, an alarm, a detector and a brownout 400KHz I2C Bus interface.

all 16 Registers designed to be addressable 8 Bit parallel register, but not all bits are used. The first two registers (memory address 00H , 01H) For control and status registers, memory address 02H ~ 08H A clock counter (counter seconds to years), the address 09H ~ 0CH For alarm registers (defined alarm condition), the address 0DH control CLKOUT Output pins

The frequency, address 0EH with 0FH Respectively for the timer control register and timer register. Seconds, minutes, hours, days, months, years, the alarm minute, alarm hour, day alarm registers, coding format BCD , Weeks and days of the alarm registers are not to BCD Format encoding.

When a RTC When the register is read, the contents of all counters are latched, therefore, under the transfer conditions can prohibit wrong reading of the clock / calendar chip.

4.1 Alarm mode

One or more alarm registers MSB (AE = Alarm Enable Alarm Enable bit) clear 0 , The corresponding alarm conditions effective so that an alarm will be generated once in every minute to every week range. Set the alarm flag AF (Control / Status Register 2 Bit 3) Used to generate an interrupt, AF It can only be cleared by software.

4.2 Timer

8 Bit down counter (address 0FH) Control register (address by the timer 0EH See Table twenty two) Control, timer control register for setting the timer frequency (4096 , 64 , 1 ,or 1 / 60Hz), And set a timer valid or invalid. Timer from the software settings 8 Bit binary number counts down every time down the end of the count, the timer setting flag TF (See Table 4), The timer flag TF Can only be cleared by software, TF Used to generate an i[illegible]pt (y IN[illegible]h cycle generating a count-down pulse as an interrupt signal. TI / TP (See Table 4) Control condition interrupt generation. When reading the timer [illegible]turns the va[illegible] the current countdown.

4.3CLKOUT Export

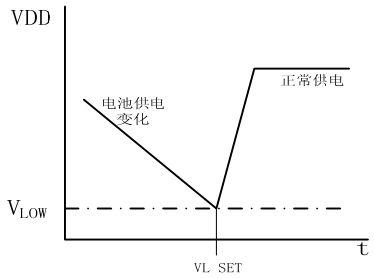
Pin CLKOUT Programmable square wave can be output. CLKOUT Frequency regis[illegible]ress 0DH ; See Table 26) Determines the frequency of the square wave, CLKOUT Can output 32.768KHz (The default value), 1024 , 32 , 1Hz The square wave. CLKOUT An open-[illegible]utput pins, when the effective power, high impedance invalid.

4.4 Reset

AiP8563 Comprising an on-chip reset circuit, when the o[illegible]r is stopped, the r[illegible] circuit to work. In the reset state, I2C Bus initialization, register TF , VL , TD1 , T[illegible]TEST[illegible], AE It is [illegible] registers are cleared and the address pointer 0 .

4.5 Brownout detector and clock monitor

Ai[illegible]563 Embedded brownout detector, whe[illegible]wer th[illegible]w When the bit VL (Voltage Low, Bit second register 7) Is set 1 For indicating possible inaccurate [illegible]calendar information, VL Flag can only be cleared by software. when VDD Slow decay (e.g., battery powered) reaches Vlow Fl[illegible]L Is set, [illegible]t may generate an interrupt.



Map 7 : Brownout detection

4.6 Register Structure

Note: marked " - " Bit invalid, indicating "0" Bit should be set to logic 0 .

table 1 : Register overview

address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
00H	Control / Status Register 1	TEST	0	STOP	0	TESTC	0	0	0	
01H	Control / Status Register 2	0	0	0	TI / TP	AF	TF	AIE	TIE	
0DH CLKOUT Frequency register		FE	-	-	-	-	-	FD1	FD0	
0EH	Timer control register	TE	-	-	-	-	-	TD1	TD0	
0FH Send a countdown timer value Register		Countdown timer value								

table 2 : BCD Format register Overview

address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	second	VL	00 ~ 59BCD Code number format						
03h	minute	-	00 ~ 59BCD Code number format						
04h	hour	-		00 ~ 23BCD Code number format					
05h	day	-		01 ~ 31BCD Code number format					
06h	week	-	-	-	-	-	0-6		
07h	Month / century	C		-	01 ~ 12BCD Code number format				
08h	year	00 ~ 99BCD Code number format							
09h	Minute alarm	AE	00 ~ 59BCD Code number format						
0Ah	Hour alarm	AE	-	00 ~ 23BCD Code number format					
0Bh	Day Alarm	AE	-	01 ~ 31BCD Code number format					
0Ch	Alarm week	AE		-	-	-	0-6		

4.6.1 Control / Status Register 1

table 3 : Control / Status Register 1 Bit description (address 00H)

Bit	symbol	description
7	TEST1	TEST1 = 0; Normal mode TEST1 = 1; EXT_CLK Test Mode
5	STOP	STOP = 0; Chip clock running STOP = 1; All logic chips divider asynchronous set 0; Chip clock will be stopped (CLKOUT in 32.768kHz When available)
3	TESTC	TESTC = 0; Reset function is set when the power fail logic (normal mode 0)

		TESTC = 1 ; Power Reset function effectively
6,4,2,1,0	0	The default value is set to logic 0

4.6.2 Control / Status Register 2

table 4 : Control / Status Register 2 Bit description (address 01H)

Bit	symbol description	
7,6,5	0	The default value is set to logic 0
4	TI / TF	TI / TP = 0: when TF Effective when INT Effective (depending on TIE status) TI / TP = 1: INT Effective pulse, see Table 8 (depending on TIE State) Note: if AF with AIE When are valid, INT It remains in effect
3	AF	When an alarm occurs, AF It is set to logic 1 ;
2	TF	At the end of the countdown timer, TF It is set to logic 1 They have maintained original valu ore being rewritten software, if the request timer and alarm interrupts, interrupt sources AF with TF Decision, to make cle lag ar vent anoth is rewritten, should use logic instructions AND , Flag AF with TF Value Description Table 9 .
1	AIE	Flag AIE with TIE We decided to request an interrupt valid lid, when AF or TF One is "1"
0	TIE	When the interruption is AIE with TIE A AE = 0 : Alarm interrupt invalid; AIE Alarm interrupt act TIE = 0 : Timer interrupt is invalid = 1 : Timer interrup id

table 5 : / INT operating(bit TI / TP = 1)

Source clock (Hz	/ INT cycle	
	n = 1	n> 1
4096	1/8192	1/4096
64	1/128	1/64
	1/64	1/64
1/60	1/64	1/64

Note 1 : TF with/ INT While eff

Note 2 : n For the value of the timer countdown, when n = 0 When the timer is stopped

table 6 : AF with TF Value Description

R / W	Bit : AF		Bit : TF	
	value	description	value	description
Read read	0	Alarm flag is invalid	0	Timer flag is invalid
	1	Alarm flag is valid	1	Timer flag is valid

Write write	0	Alarm flag is cleared	0	Timer flag is cleared
	1	Alarm flag remains unchanged	1	Timer flag remains unchanged

4.6.3 Seconds, minutes and hours registers

table 7 :second/ VL Description register bit (address 02H)

Bit	symbol	description
7	-	VL = 0 : To ensure accurate clock / calendar data VL = 1 : Does not guarantee an accurate clock / calendar data
6 ~ 0	< S>	representative BCD The current format of the second value, the value of 00 ~ 99 For example: <s> = 1011001 ,representative 59 second

table 8 : Min Register Bit Description (Address 03H)

Bit	symbol	description
7	-	alid
6 ~ 0	< Minutes>	representative BCD Curren utes valu at, the of 00 to 59

table 9 : H Register Bit Description (Address 04H)

Bit	symbol	d
7-6	-	invalid
5-0	< Minutes>	repres BCD The t format of the hour, the value of 00 to 23

4.6.4 Days, weeks, months, and years registers century

table 10 : Japanese Register bits description (address 05H)

Bit	symbol	description
7-6	-	invalid
5-0	< Day>	entative BCD Cur inutes value format, the value of 01 to 31. The year when the value of the counter leap year, Automatic increase in February to a value, making it 29 day

table 11 : Descripti Star register bit (s 06H)

Bit	ymbol	description
7 ~ 3		invalid
2 ~ 0	< Week>	Value represents the current week 0 ~ 6 See Table 12 These bits can be user reassigned

table 12 : Week Allocation Table

day(Day)	Bit2	Bit1	Bit0
on Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0

Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
on Saturday	1	1	0

table 13 : May / century register bit description (address 07H)

Bit	symbol	description
7	C	Century-bit; C = 0 Specifies the number of century 20 ×× , C = 1 Specifies the number of century 19 ×× , "××" The value of the register, see Table 15 . Then the value from the register 99 Changes to 00 When, centuries-bit change.
6 ~ 5	-	useless
4 ~ 0	< May>	representative BCD The current format of the month, the value of 01 ~ 12 ; See Table 14 .

table 14 : Monthly Allocation Table

month	Bit4	Bit5	Bit2		Bit0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August			0	0	0
September			0	0	1
October		0	0	0	0
ember	1	0	0	0	1
Decem	1	0	0	1	0

table 15 : In register bit ion (address 08H)

Bit	symbol	description
7-0	< 2008>	representative BCD The current format of the annual value, value 00 ~ 99 .

4.6.5 Alarm Register

When one or more alarms minutes register write legitimate, hours, days or weeks and their respective values AE (Alarm Enable) Bit is a logic 0 And these values with the current minute hour, day or week values are equal,, flag AF (Alarm Flag) be set to, AF Save settings until it is cleared up software, AF After being cleared, the time increments only when an alarm condition is again set to match the available again. Alarm registers at their respective bit AE To a logical 1 When it will be ignored.

table 16 : Min Description Alarm register bit (address 09H)

Bit	symbol	description
7	AE	AE = 0 , Effective alarm min; AE = 1 , Minute alarm invalid
6 ~ 0	< Minute alarm>	representative BCD Min values alarm format, the value of 00 ~ 59

table 17 : Description Alarm hour register bit (address 0AH)

Bit	symbol	description
7AE	AE = 0	AE = 0 , Effective alarm hour; AE = 1 , Hour alarms are disabled
6 ~ 0	< Hour alarm>	representative BCD Min values alarm format, the value of 00 ~ twenty three

table 18 : Day described alarm register bit (address 0BH)

Bit	symbol	description
7	AE	AE = 0 Japanese police effectivel = 1 Japan invalid
6 ~ 0	< Day Alarm>	representative BCD Min values alarm mat, the v 00 ~

table 19 : Description Alarm week register bit (address OCH)

Bit	symbol	descri
7	AE	AE = 0 , Effective ala k; AE = 1 , The alarm Invalid week
6 ~ 0	< Alarm week>	presenta Min valu m format, the value of 0 ~ 6

4.6.6 CLKOUT Frequency register

table 20 : CLKOUT Description bit frequency re (address 0DH)

Bit	symbol	description
7	FE	FE CLKOUT Output is disabled and set to high impedance FE = 1 , CLKOUT Effective output
6 ~ 2	-	invalid
1	0	For control CLKOUT Frequency output pin (f CLKOUT)
	FD0	Table twenty one

table twenty one : CLKOUT Frequency election table

FD1	FD0	f CLKOUT
0	0	32.768KHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

4.6.7 Countdown timer register

It is a timer register 8 Bit byte count down timer, which by the Timer Controller TE Determined valid or invalid, the timer may be selected by the clock timer controller, the other timer functions, such as interrupt generation, the control / status register 2 control. For accurate read back value counted down, I2 C Bus clock SCL The frequency should be at least twice the frequency of the selected clock timer.

table twenty two : Timer Controller Register Bit Description (Address 0EH)

Bit	symbol	description
7	TE	TE = 0 The timer is invalid; TE = 1 Timer effective
6 ~ 2	-	useless
1	TD1 0	Timer clock frequency select bits, the clock frequency determines the count down timer, see Table twenty three When not in use TD1 with TD0 Should be set "11" (1 / 60Hz), In order to reduce power consumption.
	TD0	

table twenty three : Timer clock frequency selection

TD1	TD0	Timer clock f z)
0	0	4096
0	1	6
1	0	1
1	1	1/6

table twenty four : Countdown timer value register bit description (address 0FH)

Bit	symbol	description
7-0	< Countdown timer value>	Numerical countdown "N" Countdown period = n / Clock frequency

4.7 EXT_CLK Test Mode

Online test mode for the test, create mode and contr C Operation.

ode register by a control / s 1 Bit en CLKOUT Pin becomes an input pin. In the test mode state, CLKOUT In place of the frequency signal input pin s 64Hz Freque nals, each 64 Will produce a rising edge 1 Time increments of seconds.

Note: Enter EXT _ C n the test mode and the on-chip clock is not 64Hz Always clock synchronization is also determined not state prescaler.

4.7.1 Example Operation

1) enter EXT _ CLK A test mode; setting control / status register 1 Bit 7 (TEST = 1)

2) Set Control / Status Register 1 Bit 5 (STOP = 1)

3) Purge control / status register 1 Bit 5 (STOP = 0)

4) Set the time register (seconds, minutes, hours, days, weeks, months / years and centuries) to the desired value

5) provide 32 Clock pulses to CLKOUT

6) Read the time register changes were observed for the first time

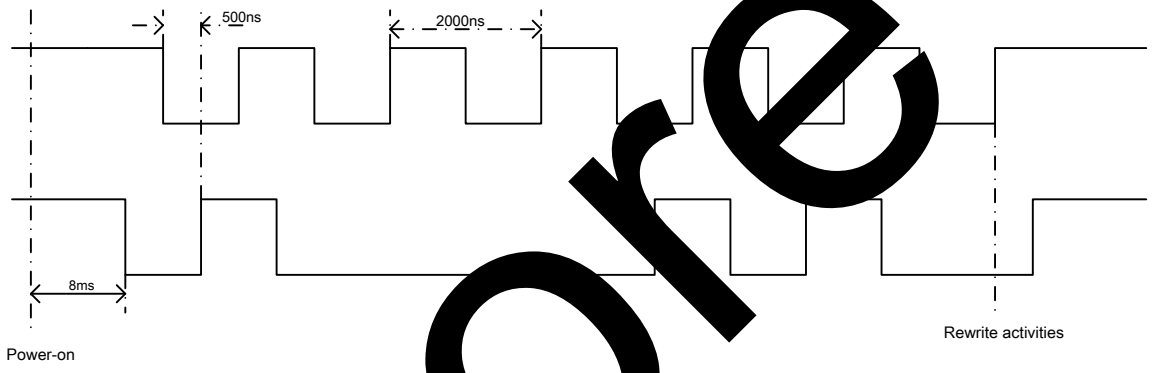
7) provide 64 Clock pulses to CLKOUT

8) Reading second change observed time register; When the need for additional time to read the increment register, repeating steps 7 with 8 .

4.8 Power On Reset (POR) Failure mode

POR Directly related to the duration from the start time of the oscillator. The starting time of an embedded circuit can POR Fail, it will give the equipment to test the acceleration. This mode requires setting I2C Bus pins SDA with SCL A signal waveform as shown below, the minimum value of the time all of the figures required.

When entering the failure mode, Chip reset immediately stop operation by I2C Into the bus EXT _ CLK Test mode. Set bit TESTC logic 0 Can eliminate failure modes, failure mode only enter the settings again TESTC The logic 1 After. Set in the normal mode TESTC The logic 0 It does not make sense, unless you want to block access POR Failure mode.



Map POR Failed timing di m

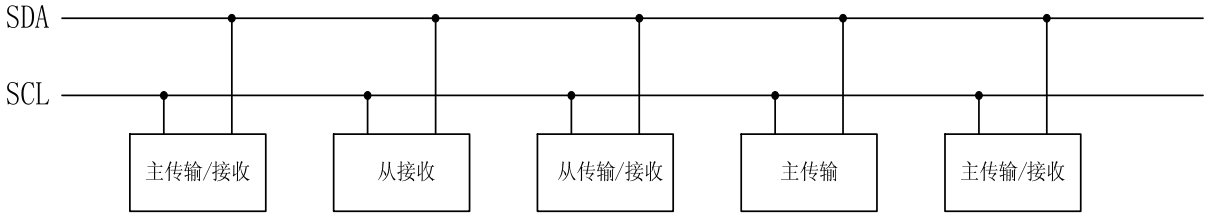
4.9 Serial Interface

AiP8563 Serial interface I2C s.

4.9.1 I2C Bus Characteristics

I2 n two bus lines (SDA with S To trans n between chips and modules. SDA A serial data line, SCL A serial clock line, two lines have pull-up resistor is connec ith a positive pply, its data transfer only when the bus is not busy before.

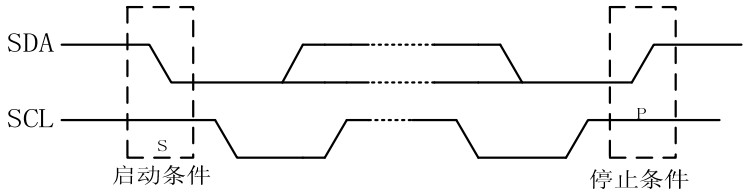
Referring next ystem configuration, the signal generating device is a transmitter, the device is a receiver receiving signals, the device control signal is a master device, the device is c d by a signal from the device.



Map 9 : I2C Bus System configuration FIG.

4.9.2 start up(START) And stop (STOP)condition

When the bus is not busy, data and clock lines remain high. Noted in the number of lines and the clock line is high on the falling edge of start conditions (S), Noted in the number of lines on the rising edge clock line is high and the stop condition (P), See figure.

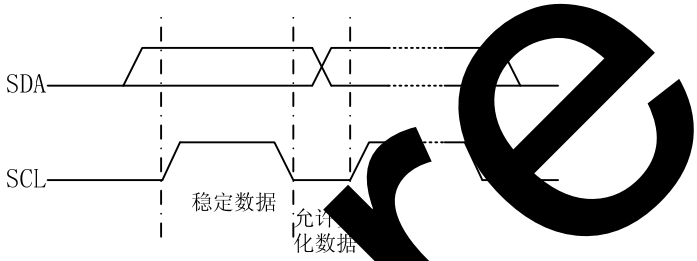


Map 10 : I 2 C Bus start (START) And stop (STOP)condition

4.9.3 Bit transfer

Each bit of a data transfer clock pulse, SDA Data line is stable when the clock pulse high, or SDA

The data line will be the above-mentioned control signal, see figure.

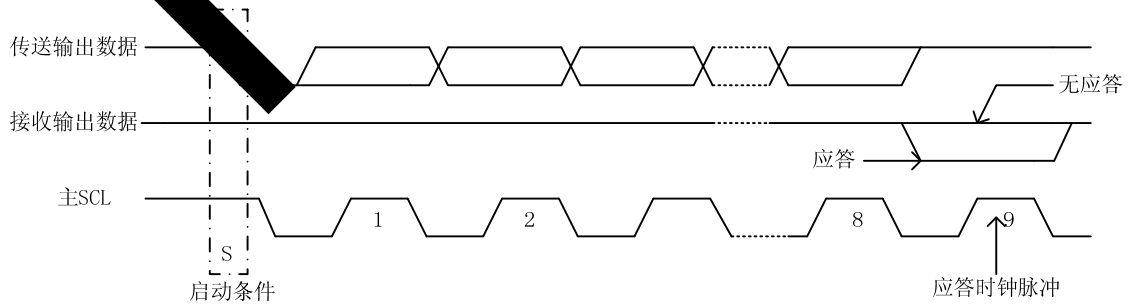


Map 11 : I 2 C on the bus

4.9.4 Flag

The number of data transfer between the start and conditions is limited to the receiver. Each 8 After adding a flag byte, flag transmitter generates a high level, then the master generates a clock notation.

Must generate a flag bit after each byte received from the receiver. Primary receiver must also generates a flag bit after the reception of each byte transmitted from the transmitter. When flag clock pulse occurs, SDA should be held (start-up and hold time should be considered). Upon reception of the transmitter should be changed to the last byte of the device low, the receiving flag, when the host device may generate a stop condition.



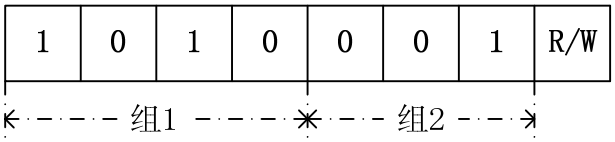
Map 12 : I 2 C Flag on the bus

4.9.5 I 2 C Bus Protocol

Note: Use I2C Bus before data transmission, the received device address should be indicated, in I2C After the start bus, the address of the first byte is transmitted along a transmission. AiP8563 As from a receiver or from the transmitter, then the clock signal line SCL

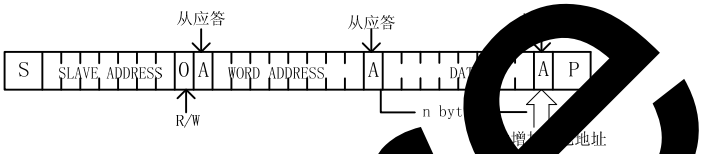
Only the input signal line, a data signal line SDA Is a bidirectional signal line.

AiP8563 Referring next address from FIG.

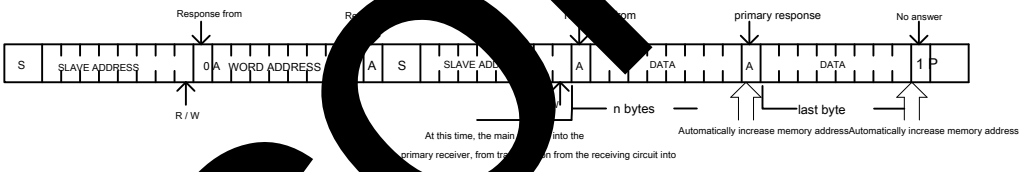


Map 13 : Address

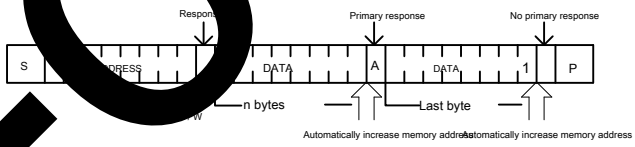
Clock / calendar chip read / write cycles: Three AiP8563 Read / write cycle I2C Configuration Referring to FIG three bus, FIG word address number is four bits, high-bit register is used to indicate a next access, the word address useless.



Map 14 : From the main conveyor to ver (write mode)



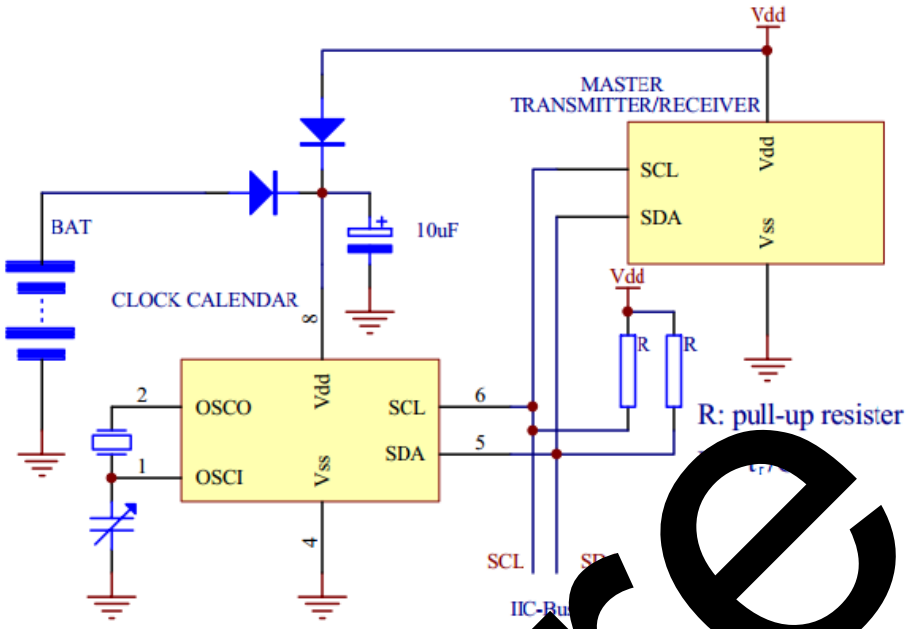
Map 15 : S g the read data word then th dress (write address: read data)



Map 16 : Read data from the master device after the first byte of data (read mode)

5 Typical applications for line and instructions

5.1 Application line



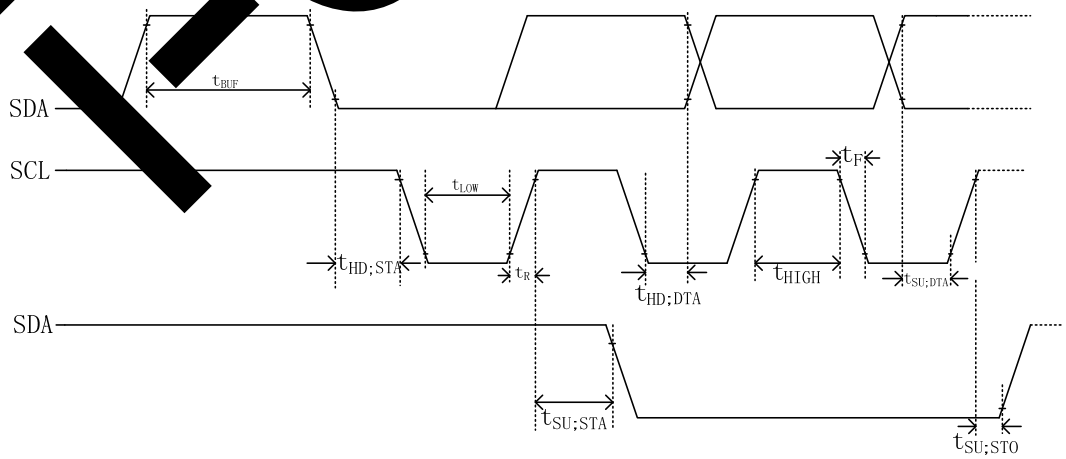
Map 17 : Typical A n Diagram

5.2 Frequency adjustment quartz wafer

Method 1: SETTINGS OSCI capacitance - Calculating the rage desired capaci the capacitance value with this value, the energization CLKOUT Measured frequency should be on pins 32.768kHz , Depending o eviation between the z to wafer, and device capacitance deviation frequency deviation measured (average ± 5 × 10-6). The average dev 5 Mi

Method 2: OSCI Trimmer - By adj g OSCI Pin trimmer capacitor oscillator frequency of exact values, then the pins can be measured energized CLKOUT Up 32.768kHz signal

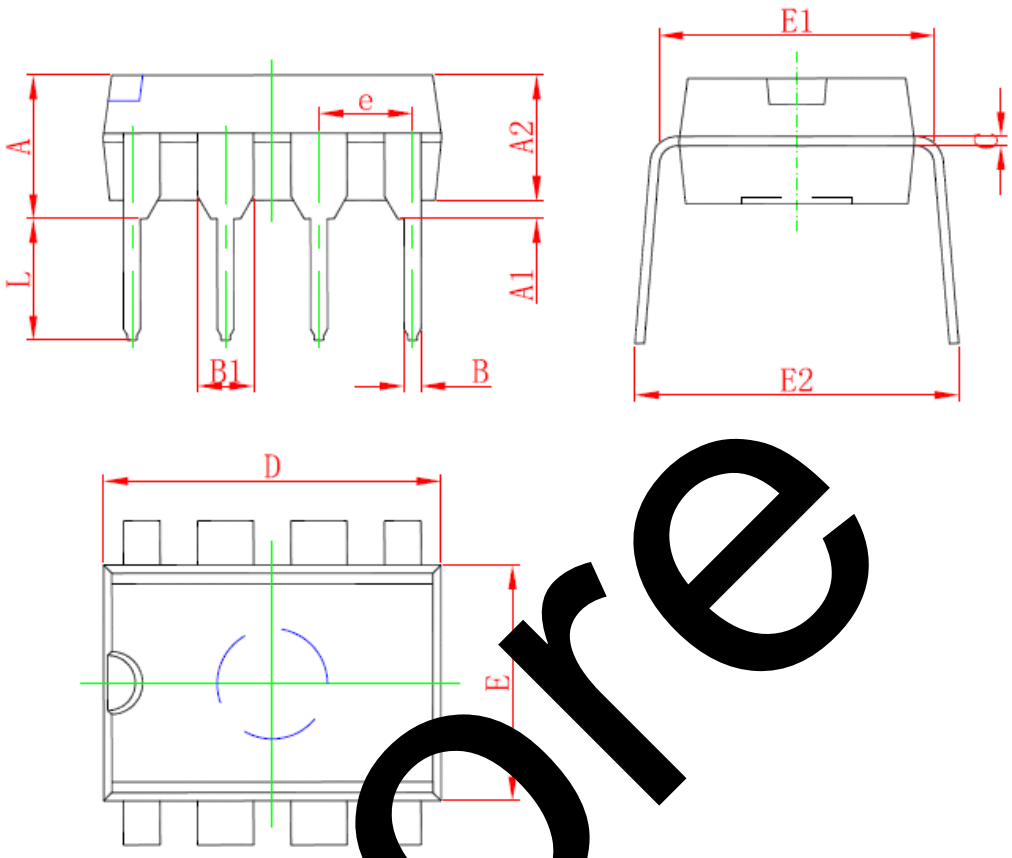
method 3 : OSCI Export - Direct meas t pin OS tput.



Map 18 : I 2 C Bus Timing Figure

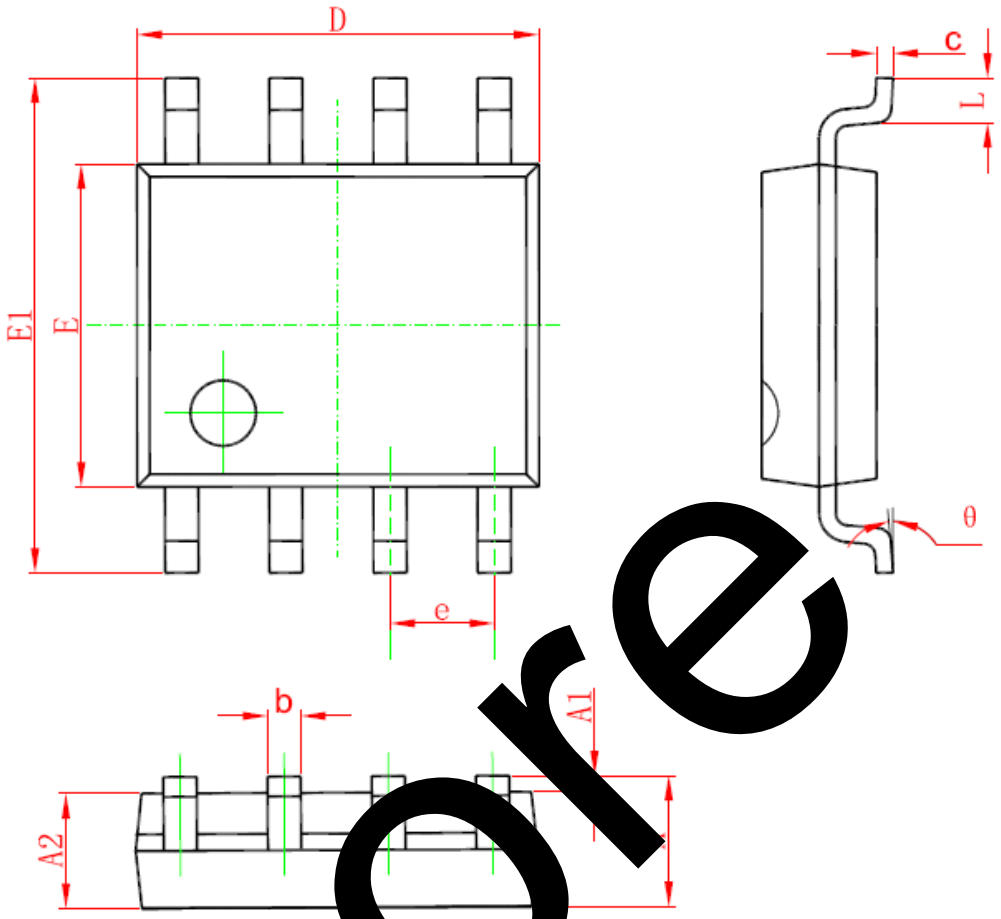
6 , Package size and outline in FIG.

6.1 , DIP8 FIG package size and shape



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

6.2 , SOP8 FIG package size and shape



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

7 Statement and notes:

7.1 The name and content of hazardous substances in products or toxic elements

Part Name lead(Pb)	Toxic and hazardous substances or elements					
	HG(Hg)	Cadmium (Cd)	Order six chromium (Cr (VI))		Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
Leadframe	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○
chip	○	○	○	○	○	○
In the lead	○	○	○	○	○	○
Attach paste	○	○	○	○	○	○
Explanation	○ : Indicates that this toxic or hazardous substances or elements in SJ / T11363-2006 Standard detection limit. × : Indicates that this toxic or hazardous substances or elements beyond SJ / T11363-2006 The standard limit requirements.					

7.2 note

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information in this document is subject to change without notice;

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