

William J. Snow

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OBJECTIVE	To design and test hardware, to develop software, and to problem solve my way through exciting projects and collaborative environments that challenge me.		
EDUCATION	B.S., Computer Engineering Purdue University, West Lafayette, IN		May 2014
PROJECTS	Chance the Rapper	<i>Freelance</i>	September 2016
	<ul style="list-style-type: none">Served as lead engineer for costume electronics on Chance the Rapper's <i>Magnificent Coloring Tour</i>Developed software in C++ using Arduino toolchain to display lighting effects on 366 sewn-in LEDs		
	Jeco Plastic Products	<i>Consultant</i>	June-August 2016
	<ul style="list-style-type: none">Designed temperature monitoring system using Raspberry Pi boards and web app interfaceProgrammed in C for thermocouple driver and unix socket API, Javascript for Node web app		
	Pricesourcing.com	<i>Lead Developer</i>	July-October 2013
	<ul style="list-style-type: none">Prototyped a front and back end for vendor-to-customer online aggregatorCollaborated with a professional graphic web designer for UX and SEOImplemented scalable back end in PHP and MySQL		
	Target Acquisition and Retrieval	<i>Senior Design Lab</i>	Fall 2013
	<ul style="list-style-type: none">Automated embedded system found targets and directed crane to retrieve them one at a timeDevised a custom bidirectional serial bus for all subsystems using commodity TTL parts and PLDsUtilized a live NTSC signal from CCD camera sensor converted to digital x-y coordinatesDrove stepper motors to move crane and pick targets with electromagnet		
	Safecam	<i>Embedded Systems Lab</i>	Spring 2014
	<ul style="list-style-type: none">Consumer home safe fitted with keypad and camera that connects to home wifi networkInterfaced electronic keypad and camera to Raspberry Pi development boardProvided web user interface with programmable key code and photo capture		
	MIPS Dual Core Microprocessor	<i>Computer Architecture Lab</i>	Fall 2013
	<ul style="list-style-type: none">Synthesized MIPS ISA subset onto Altera Cyclone II FPGA development boardImplemented 2-way associative caches with write-back cache coherency and ll/sc atomic instructionsWrote full block level test benches as well as benchmarks measuring real world performance		
	Alarm Clock	<i>Microcontrollers Lab</i>	Fall 2012
	<ul style="list-style-type: none">Freescale microcontroller (state machine loop w/ periodic interrupts) kept full calendar timeIncorporated full peripheral suite (DAC, ADC, SPI, TIM)		
	Picture Frame Viewer	<i>ASIC Design Lab</i>	Fall 2010
	<ul style="list-style-type: none">Digital ASIC converted bitmap images from SD card over SPI to LCD display over DVIDesign and verification for interfaces, constraints, RTL, synthesis map, and layout		
SKILLS	Commercial Software Mentor Graphics (ModelSim, HDL Designer), Cadence (SOC Encounter, Virtuoso, OrCad Capture/Pspice A/D), Synopsys Design Compiler Ultra, Altera Quartus II, EagleCAD, Altium Designer, Freescale Codewarrior, TI Code Composer Studio, Arduino IDE, Matlab, Catia V5. Languages C, C++, Java, VHDL, Verilog, ABEL, Assembler (x86, MIPS & 68HC11), ksh93/bash/tcsh, Python, PHP, Javascript, Go, Ruby.		
AWARDS	Eaton Award for Best Senior Design Semester Honors Fall 2013 and Spring 2014 Eagle Scout		