

## ARM's processor lines

- 1. Evolution of ARM
- 2. Evolution of the ARM ISA
- 3. Approaches to circuit design
- 4. Overview of ARM's processor families
- 5. Overview of ARM's Cortex-A series
- 6. Overview of ARM's Mali graphics series
- 7. ARM's 64-bit Cortex-A series
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## 1. Evolution of ARM

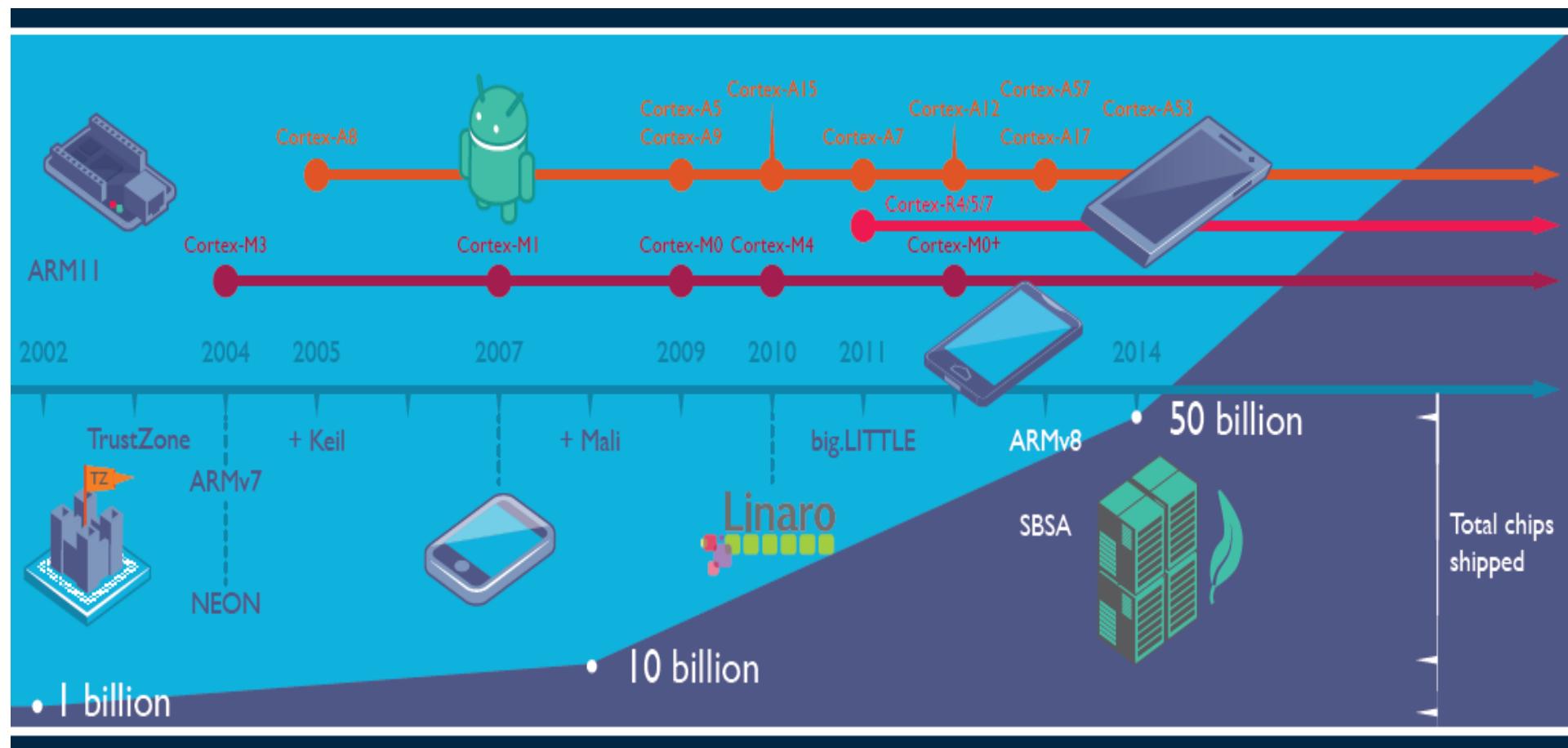
# 1. Evolution of ARM (1)

## 1. Evolution of ARM

- ARM (ARM Holdings plc) is a British multinational semiconductor company with its head office in Cambridge.
- The company designs and licenses low power embedded and mobile ARM processors as well as mobile GPUs (termed as Mali GPUs) along with the appropriate design tools but does not fabricate semiconductors.
- ARM designs dominate recently the embedded and the mobile market (including smartphones and tablets).
- As of 2014 more than 50 billion ARM based processors have been produced in total, up from 10 billion in 2008 [59], [19], as indicated in the next Figure.

# 1. Evolution of ARM (2)

Total number of ARM based chips shipped [19]



Keil: Software development tool for embedded processors

Linaro: Nonprofit company, established by ARM, Freescale, IBM, Samsung, ST-Ericsson and TI to support open source software developers using Linux on SoCs.

SBSA: Server Base System Architecture, a standardized server platform for 64-bit ARM processors.

## 1. Evolution of ARM (3)

ARM's approach for taking part in the processor business

- There are
  - semiconductor foundries without own processor designs, like TSMC, Global Foundries
  - chipmakers with own foundries, like Intel, Samsung
  - chipmakers without own foundries, like Apple, IBM, AMD, MediaTek, Qualcomm
  - a processor IP designing and licensing firm: ARM.
- Chipmakers of mobile application processors (except Intel and AMD who use x86 ISA) typically license the ARM ISA and develop their processors partly in-house and partly based on ARM IP.

E.g. Apple developed their first application processors based on ARM IP (the Cortex-A8/A9 cores), later they designed their processor cores in-house (like the Swift or Cyclone cores).

- ARM possesses the license of the ARM ISA and develops tools for designing and manufacturing ARM ISA based processors and licenses these for a large number of chipmakers for smartphone application processors.

# 1. Evolution of ARM (4)

## Historical remarks [60], [61] -1

- ARM's parent company is **Acorn Computers** (UK).
- Acorn Computers started their *Acorn RISC Machine* project in October 1983 (two years after the introduction of the IBM PC) to develop an own powerful processor for a line of business computers.
- The acronym **ARM** was coined originally at this time (1983) from the designation *Acorn RISC Machine*.
- In 1990 the company **Advanced RISC Machines Ltd. (ARM Ltd.)** was founded as a joint venture of **Acorn Computers**, **Apple Computers** and **VLSI Technology**.
- Accordingly, also the interpretation of **ARM** was changed to “**Advanced RISC Machines**”.

# 1. Evolution of ARM (5)

## Historical remarks -2



Figure: The headquarters of ARM Ltd. about 1990 [62]

## 1. Evolution of ARM (6)

### Historical remarks -3

Finally, in 1998 the company [went to the stock exchange](#) and its name was changed to **ARM Holdings plc**, to its current designation.

## 1. Evolution of ARM (7)

Historical remarks -4



Figure: ARM's recent headquarters in Cambridge (UK) [78]

## 2. Evolution of the ARM ISA

- 2.1 Overview
- 2.2 ISA extensions introduced to enhance compute capabilities
- 2.3 ISA extensions introduced to reduce the code size
- 2.4 ISA extensions introduced to enhance security

## 2.1 Overview

### 2.1 Overview

- There are 8 ARM ISA versions, designated as ARMv1 to ARMv8.  
These are described in the related Architecture Reference Manuals.
- The earliest versions (ARMv1 and ARMv2) provided an address range of only 26 bits, the first ISA version with 32 bit address range was the ARMv3.
- Accordingly, we consider the ISA version ARMv3 as ARM's basic ISA and discuss its evolution subsequently.

### Key features of ARM's basic ISA

- It is a **32-bit RISC ISA** capable to process basically **32-bit FX or logical data**.
- The ISA has **16 32-bit registers**, called the **core registers**.
- **13** out of them are used as **general purpose registers (GPRs)**, the remaining three are **dedicated registers**, as shown below.

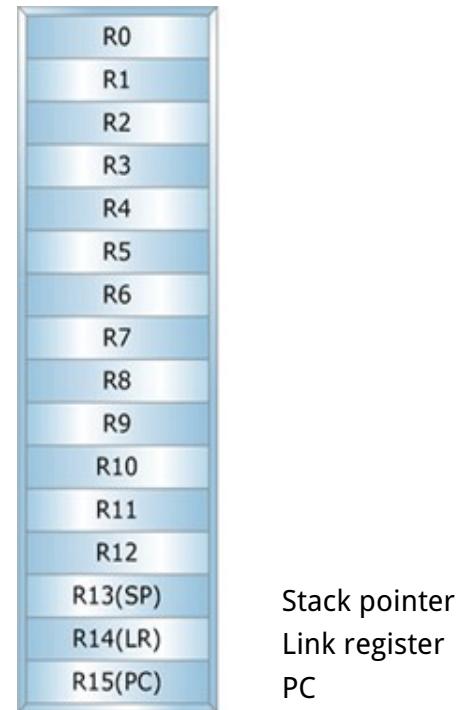
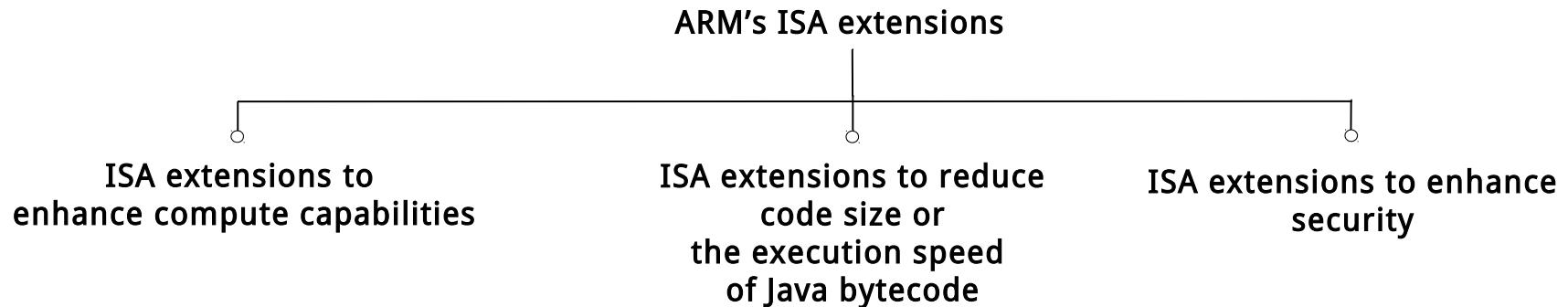


Figure: The core registers of the ARM ISA (in the ISA versions ARMv3-ARMv7) [63]

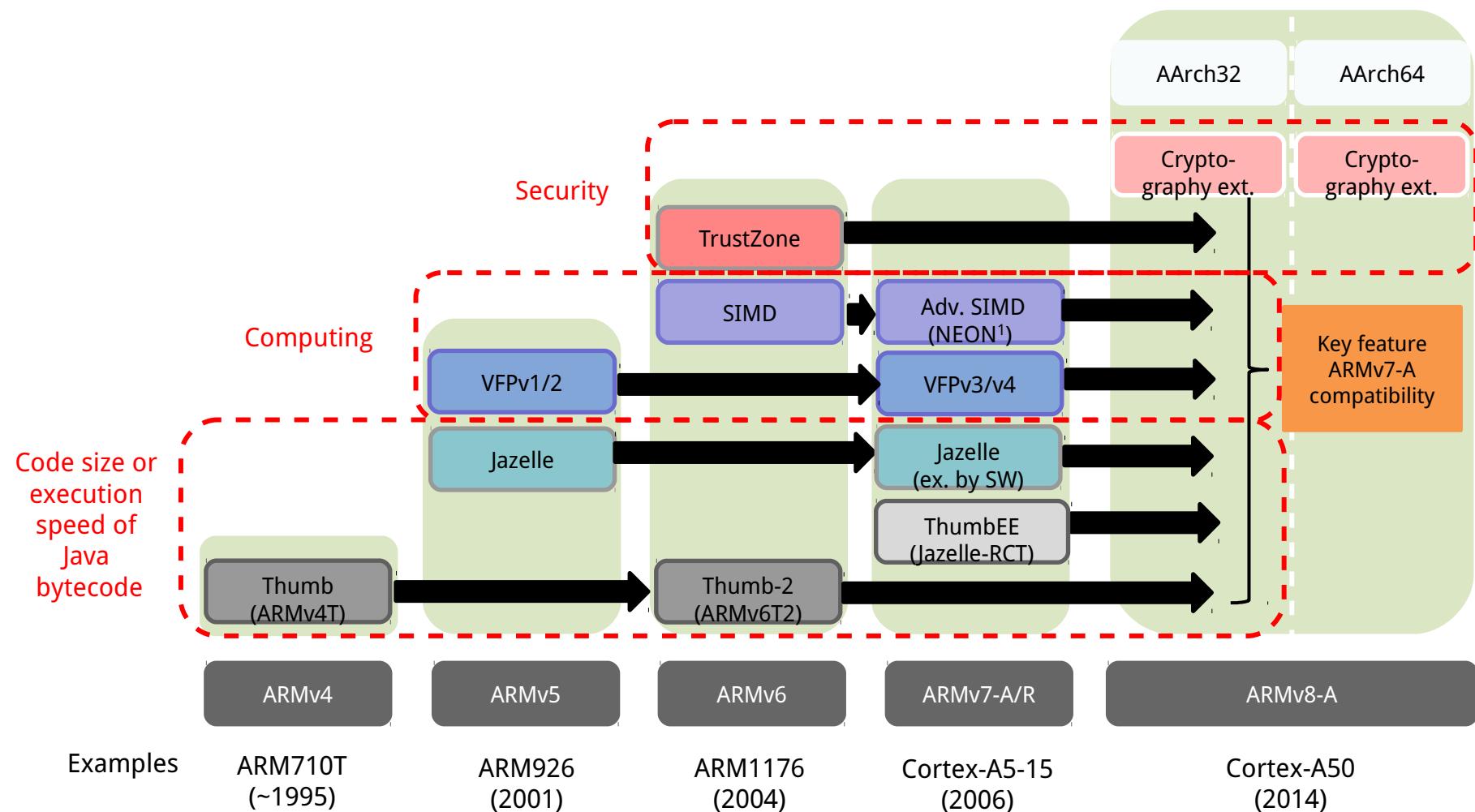
## 2.1 Overview (3)

### Main extensions introduced to ARM's basic ISA (simplified) -1



## 2.1 Overview (4)

Main extensions introduced to ARM's basic ISA (simplified) -2 (Based on [64])



<sup>1</sup>The Advanced SIMD architecture extension is commonly referred to as the NEON technology.

## 2.2 ISA extensions introduced to enhance compute capabilities

## 2.2.1 Overview (1)

### 2.2 ISA extensions introduced to enhance compute capabilities -1

#### 2.2.1 Overview

##### ARM's ISA extensions

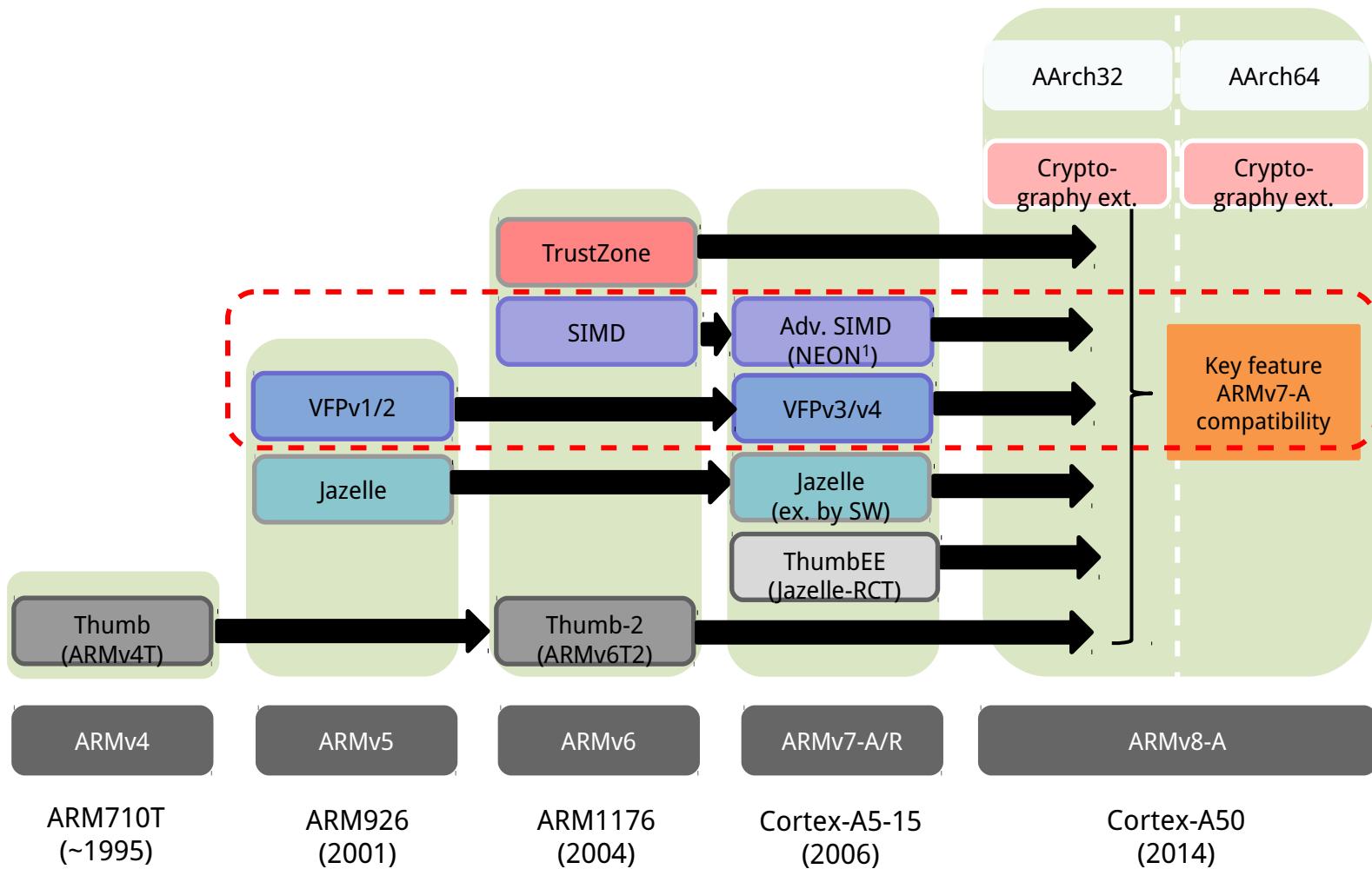
ISA extensions introduced  
to enhance compute capabilities

ISA extensions introduced  
to reduce code size or  
the execution speed  
of Java bytecode

ISA extensions introduced  
to enhance security

## 2.2.1 Overview (2)

ISA extensions introduced to enhance the compute capabilities -2  
(Based on [64])

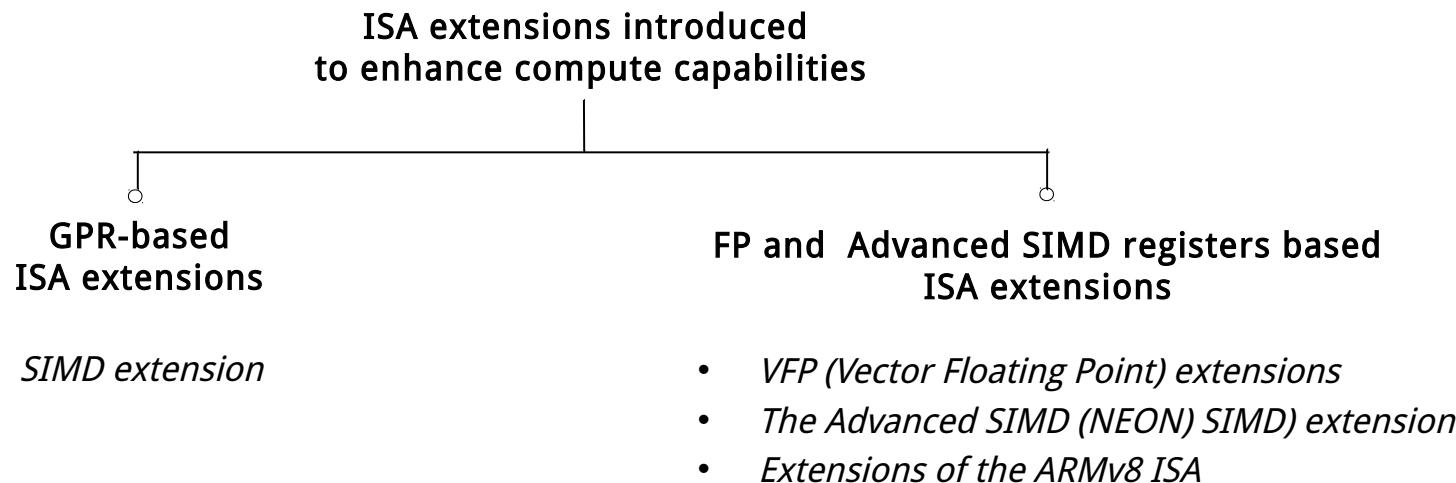


<sup>1</sup>The Advanced SIMD architecture extension is commonly referred to as the NEON technology.

## 2.2.1 Overview (3)

### ISA extensions introduced to enhance the compute capabilities -3

- As far as the extension for enhancing the compute capabilities are concerned we have to take into account **two distinct register sets**;
  - the **basic GPR register set** and
  - the **FP and advanced SIMD register set** (since ARMv5).
- In line with this, the compute oriented ISA extensions may be discussed in **two groups** according to **which instruction set is referred to** by a specific extension, as shown below.



## 2.2.1 Overview (4)

### Overview of ISA extensions introduced to enhance compute capabilities

• ARM ISA	• Basic arch.	• Name of the extensions	• GPR-based extension	• FP/SIMD register based extension	
• Name	• GPRs	• Data type	• FP/adv. SIMD reg. set	• Scalar data types	• Vector data types
• Year	•	•	•	•	•
• ARMv1	• 1986	• n.a.	•	•	•
• ARMv2	• 1989	• n.a.	•	•	•
• ARMv3	• 1991	• 13x32	• FX32	•	•
• ARMv4	• 1996	•	•	•	•
• ARMv5	• 2000	• VFP(v1) <sup>1</sup>	• 32x32/16x64	FP32/64	• Serially executed
	• 2001	• VFP2 <sup>1</sup>	•	•	•
• ARMv6	• 2004	• SIMD	• 32-bit w. FX8/16	•	•
• ARMv7	• 2006	• VFPv3 <sup>2</sup> VFPv4 <sup>2</sup>	• 32x64/32x32 or 16x64/32x32	+FP 16 <sup>4</sup> + FMA	• Serially executed
	•	• Adv. SIMD • (NEON) <sup>3</sup>	• 32x64/16x128	• FX8/16/32/ • 64 • FP16 <sup>3</sup> /32/64	• 64/128-bit wide • FX 8/16/32/64, FP16 <sup>3</sup> /32 +FMA <sup>3</sup>
• ARMv8	• 2014	• 31x64	• A32	• FP32/64	• As for ARMv7
		• FX32/64	• Adv. SIMD	•	•
			• A64	• FP32/64	•
			• Adv. SIMD	• FX 8/.../64 • FP 32/64	• As for ARMv7 • + FP 64

w: wide

## 2.2.1 Overview (5)

### Remarks

<sup>1</sup>VFPv2 vs. VFP(v1)

VFPv2 adds some instruction set enhancements and modifications to VFPv1

<sup>2</sup>VFPv3/v4 register space

Some processors implement 32 64-wide registers, with the option of using these registers as 32 32-wide registers.

Other implementations provide only 16 64-bit wide registers with the option to use the register space as 32x32-wide registers.

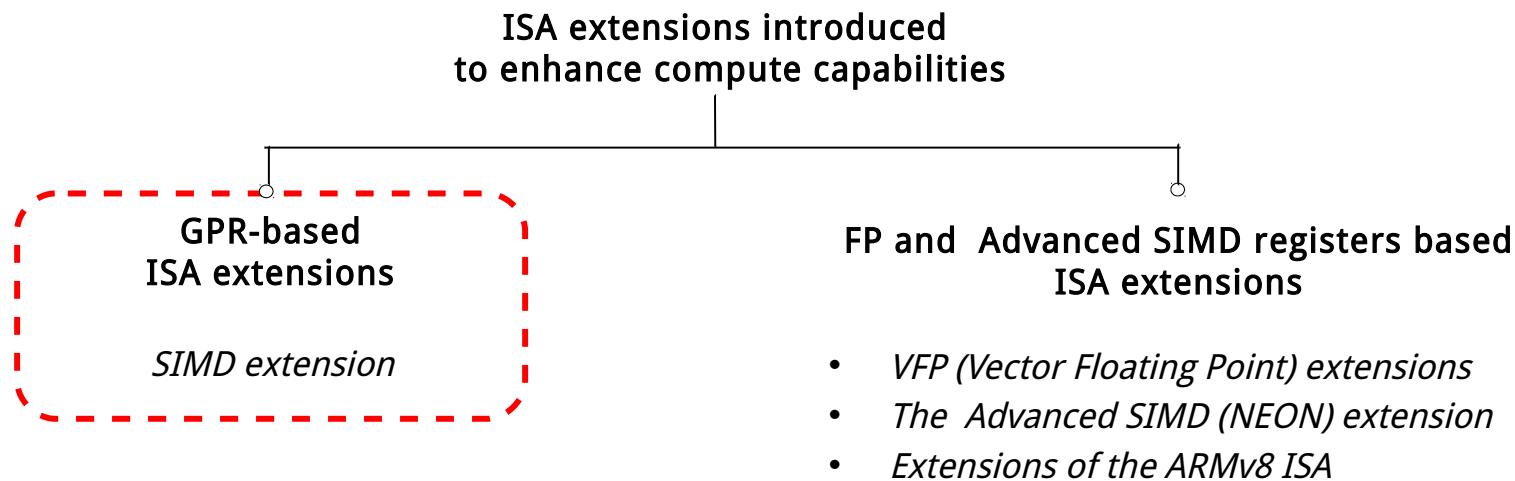
<sup>3</sup>Along with the Advanced SIMD (NEON) extension FP16 and FMA are supported only in the Advanced SIMDv2 alternative.

FP16 supports only data conversion between FP16 and FP32

<sup>4</sup>FP16 supports only data conversion between FP16 and FP32

## 2.2.2 GPR-based ISA extensions (1)

### 2.2.2 GPR-based ISA extensions



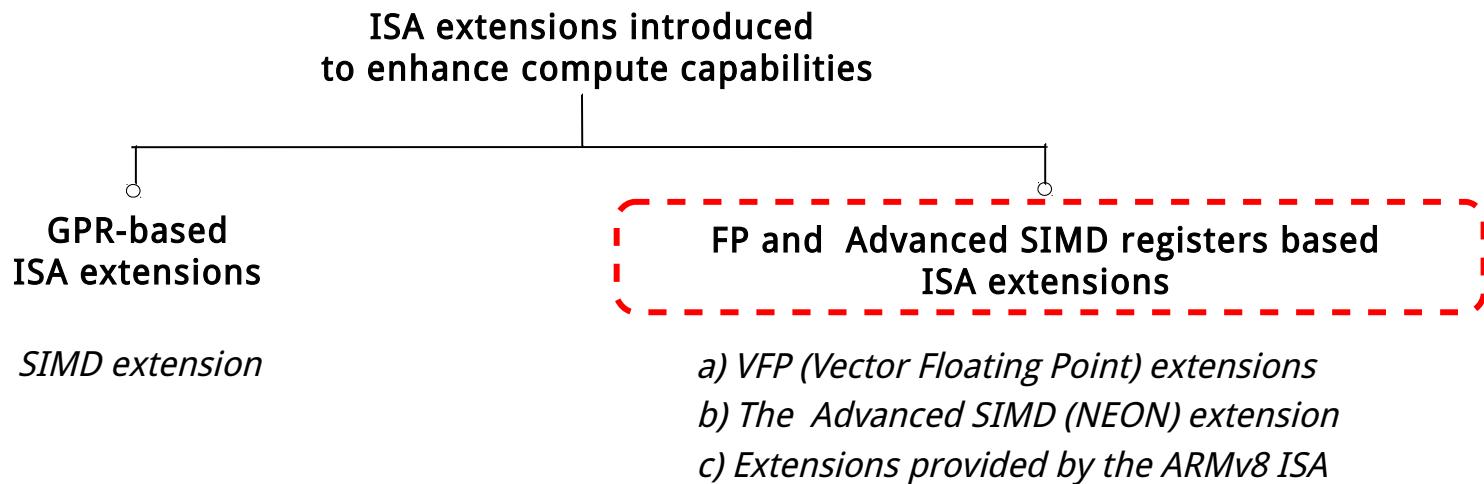
## 2.2.2 GPR-based ISA extensions (2)

### The SIMD extension (introduced in the ARMv6)

- It is based on the 13 32-bit wide GPR register set and provides instructions to be performed on 4xFX8 or 2xFX16 data in parallel.  
It is similar to Intel's MMX x86 ISA extension from 1997.
- The SIMD extensions as introduced into the ISA version ARMv6 have only a modest performance boosting potential and became obsolete by the advanced SIMD (NEON) extension of the next ISA version.

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (1)

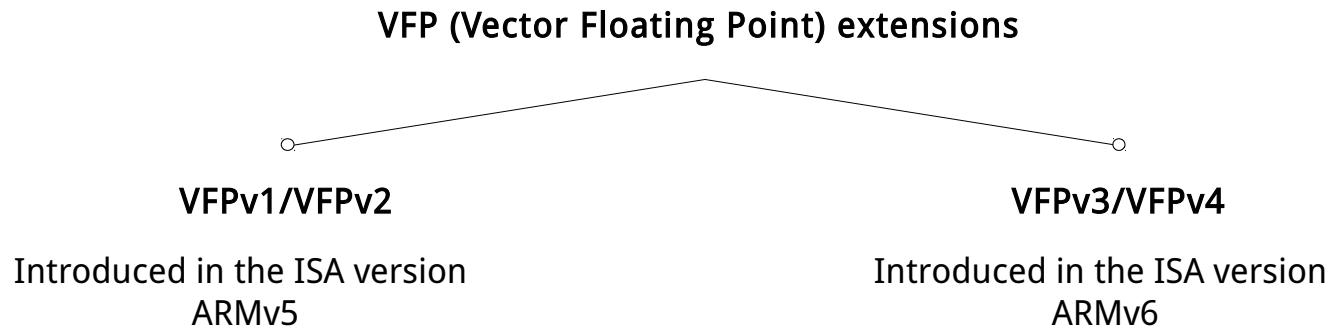
### 2.2.3 FP and Advanced SIMD registers based ISA extensions



## 2.2.3 FP and Advanced SIMD registers based ISA extensions (2)

### a) VFP (Vector Floating Point) ISA extensions

We will discuss the VFP (Vector Floating Point) extensions subsequently [in two parts](#), [in accordance with their introduction in the ARMv5 and ARMv6 ISA versions](#), as shown below:



## 2.2.3 FP and Advanced SIMD registers based ISA extensions (3)

### a1) VFP (Vector Floating Point) extensions VFP(v1)/v2 [65] -1

- It is a **co-processor based extension to speed up scalar and vector FP32/64 operations**, introduced along with the ARMv5 ISA version.
- This extension is **based on the new 32 32-bit wide VFP register file**, organized as **four register banks**, each including 8 registers, as seen below.

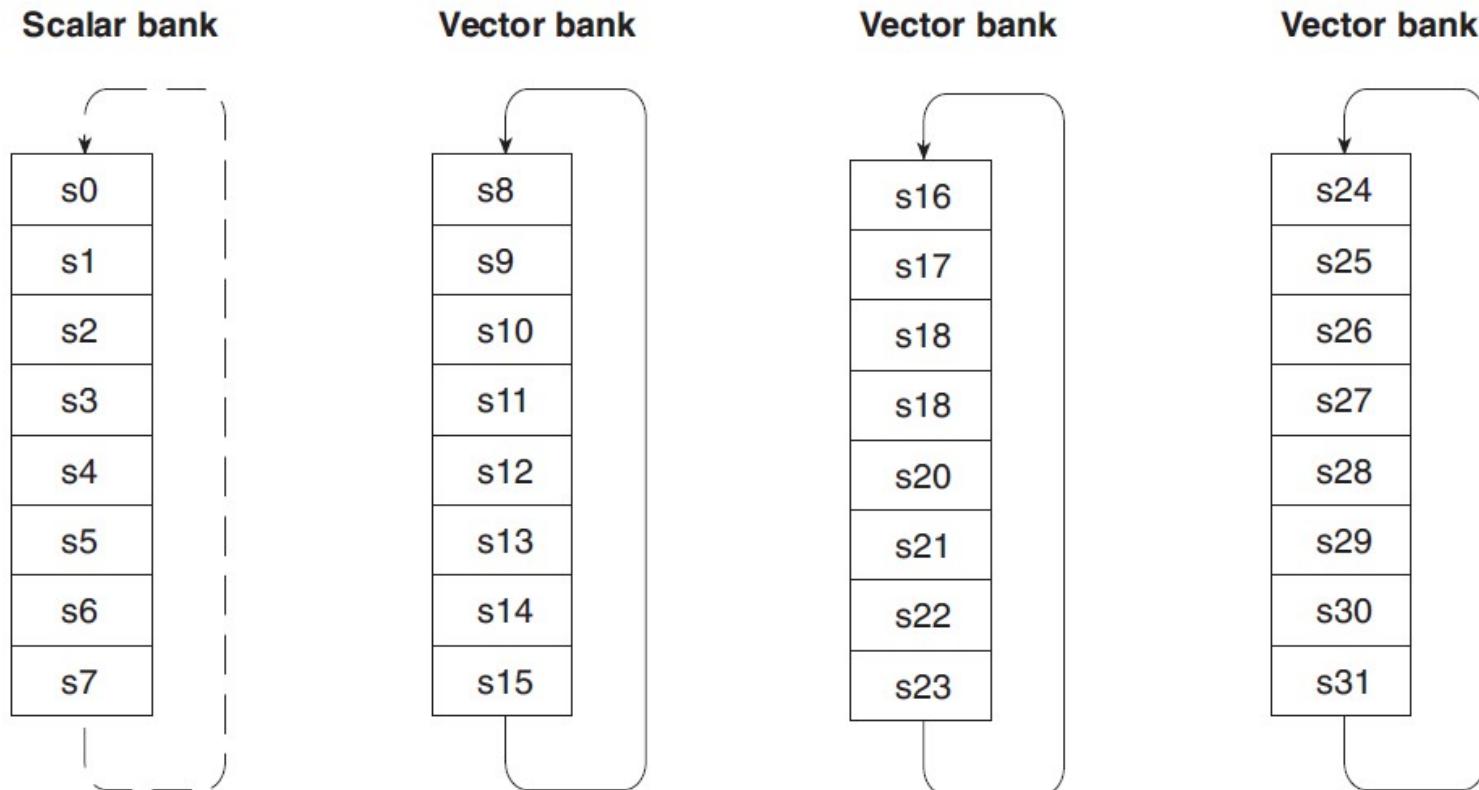


Figure: Register banks of the VFP extensions [65]

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (4)

### VFP (Vector Floating Point) extensions [65] -2

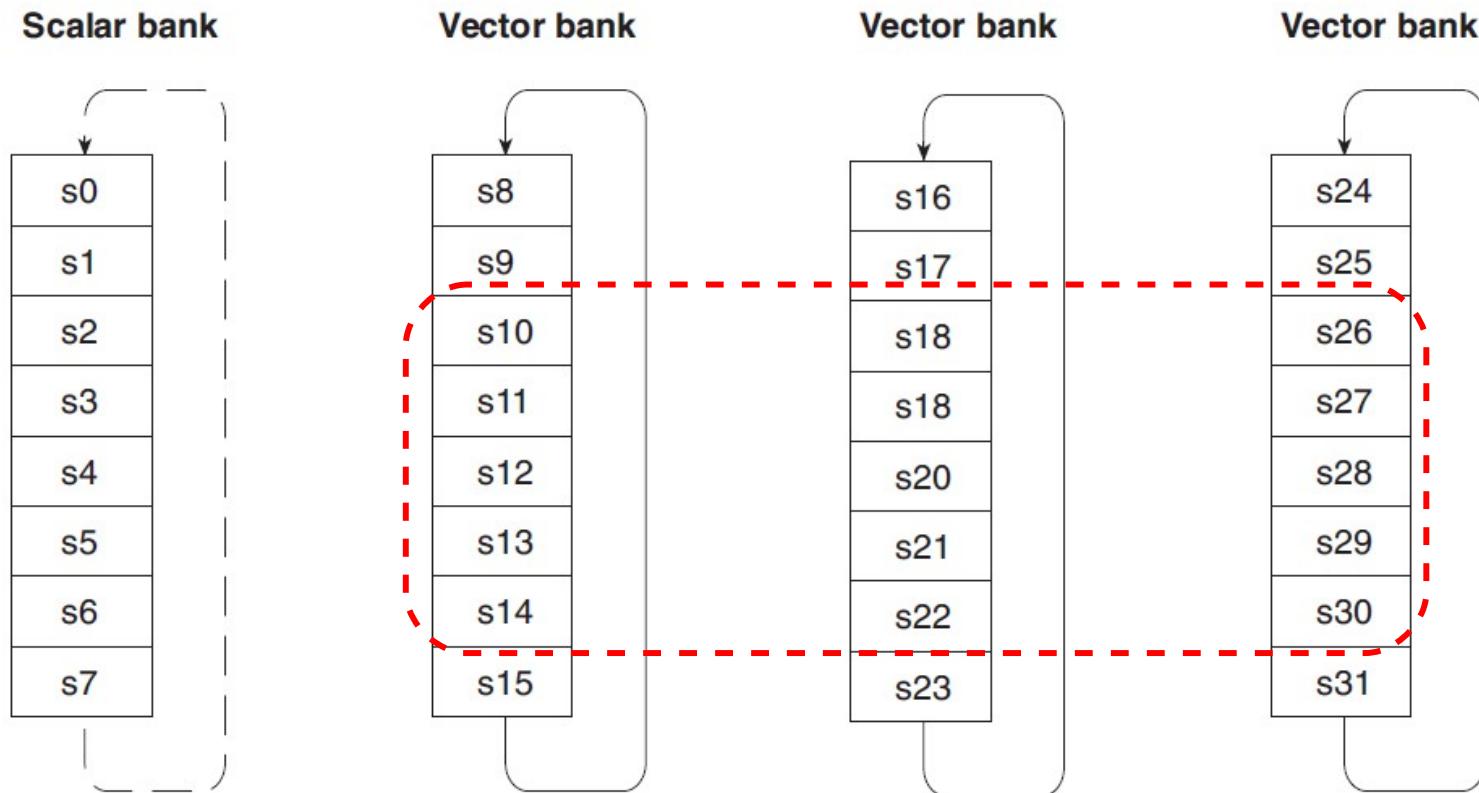
- The first bank is used to hold scalar operands whereas the remaining three banks hold vector operands.
- A vector operand may refer to 2 to 8 registers from the same bank.
- The vector length is given in a specific field of a control register.
- The register numbers given in the instruction specify the first registers that contain the first operands and specify the first destination register.

Each successive element of the vector is taken by incrementing appropriately the register numbers.

- The peculiarity of the VFP extension is that the elements of the vector are processed sequentially rather than parallel as for usual SIMD execution.

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (5)

Example: Vector operation with 5 elements [65]



- In the example the input operands are taken from the registers s10...s14 and s18...s22, and the result is written into the registers s26...s30.
- The execution is sequential (like a hardware implemented subroutine).

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (6)

### a2) The VFPv3/v4 extension

- It is an enhancement to the VFPv2 technology.
- New features include
  - doubling the size of the register space to 32x64 bit registers, and
  - the introduction of instructions that perform conversions between FX and FP data.

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (7)

### b) The Advanced SIMD (NEON) extension (introduced in the ARMv7 ISA) [11]

- It is a **64/128-bit SIMD extension** intended to accelerate multimedia and signal processing algorithms such as video encode/decode, 2D/3D graphics, gaming, speech or image processing.
- NEON **extends the 32x32-bit VFP register file to 32x64-bit**, called the **FP and advanced SIMD register file**, that may be used also as **16 128-bit wide registers**, and is **shared with the VFP3/VFP4 extension**.
- NEON instructions operate on data held in the FP and advanced SIMD registers.
- They perform the same operation on the data elements, as shown below.

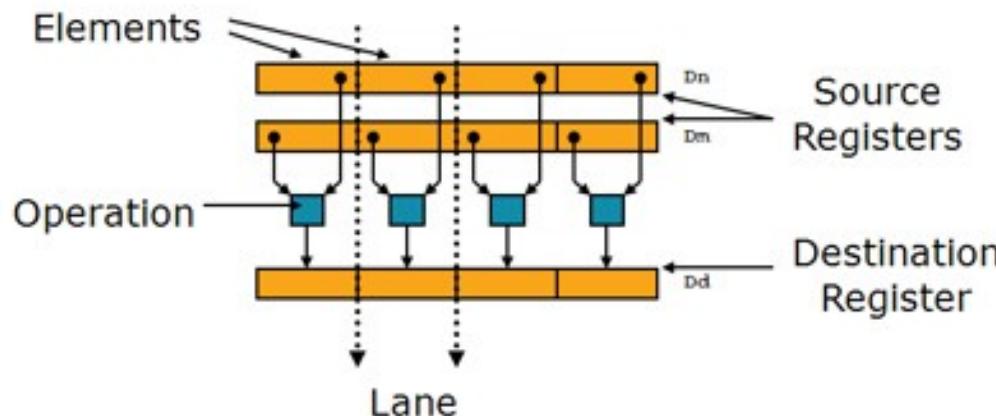


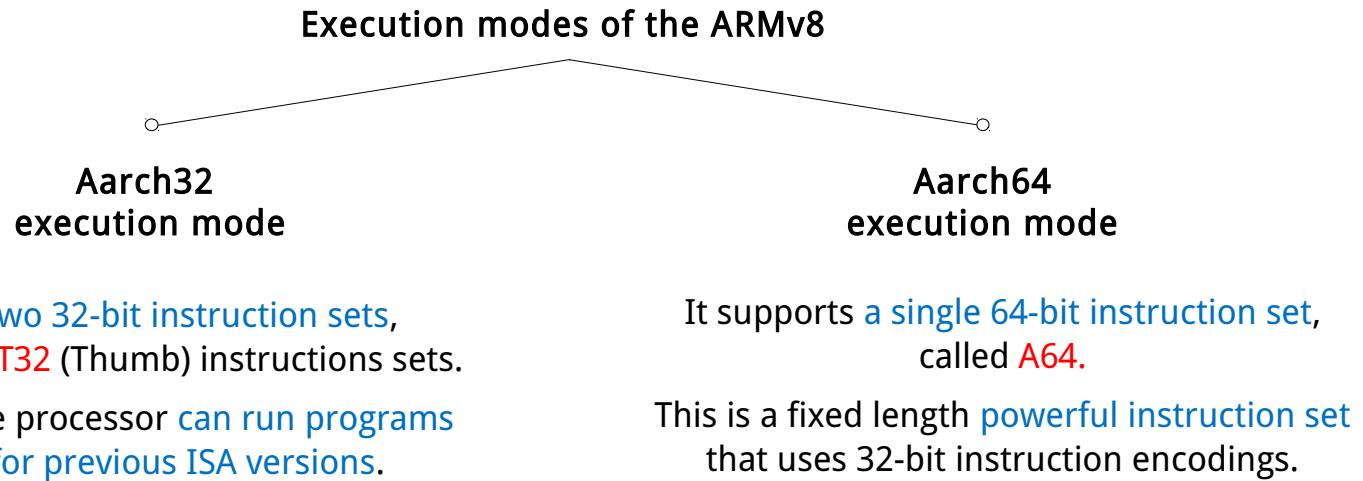
Figure: SIMD data [11]

- NEON instructions **operate on 64 or 128-bit packed vectors of signed/unsigned 8-bit, 16-bit, 32-bit or 64-bit FX as well as on FP16 or FP32 data elements**.
- For FP16 data there are only conversion (FP16-FP32) operations supported.
- FP16 data and FMA operations are supported only in the Advanced SIMDv2 option.

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (8)

### c) Extensions provided by the ARMv8 ISA [66]

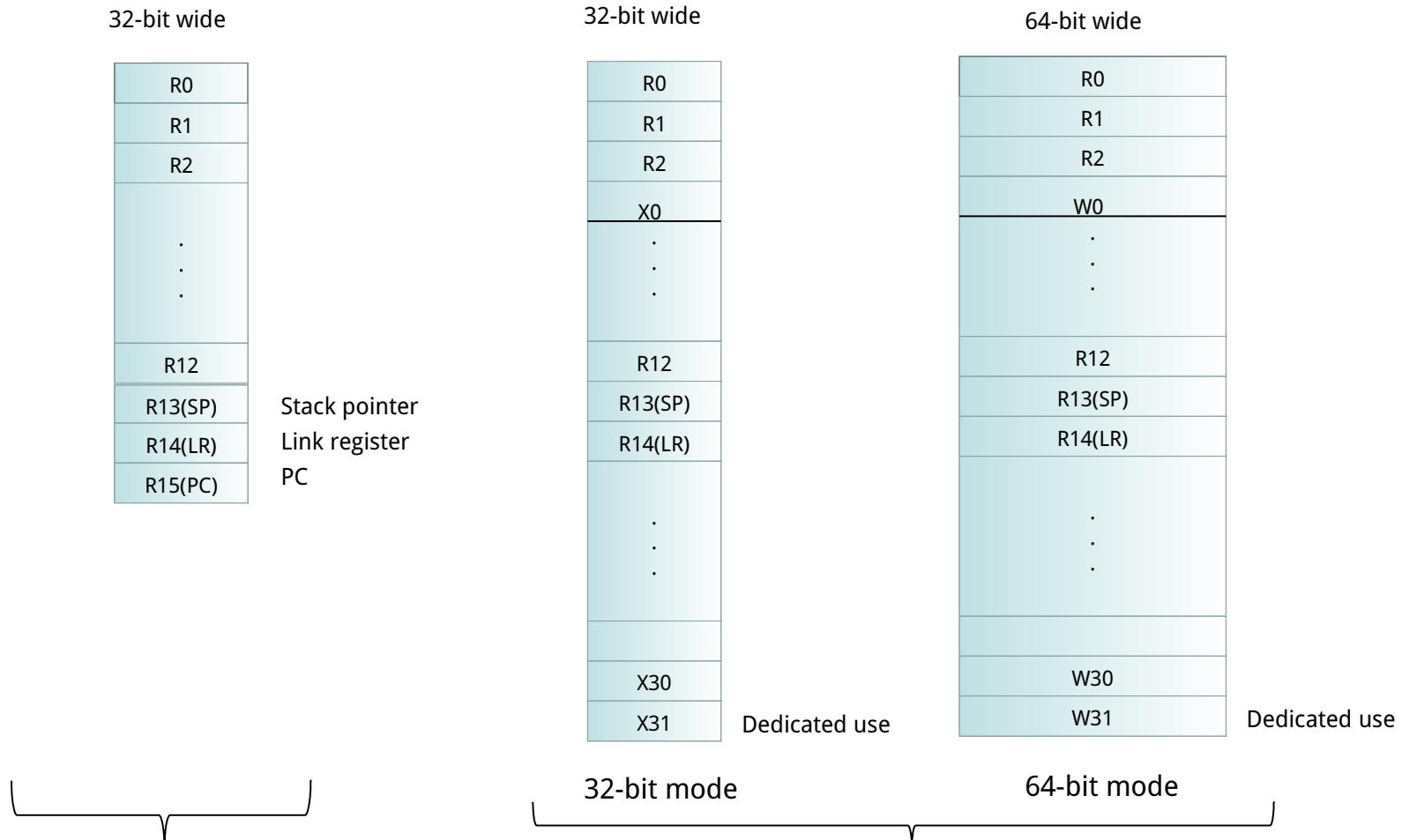
- The ARMv8 ISA version introduces **major changes** in the ARM architecture while maintaining a high level of consistency with previous versions of the architecture.
- **ARMv8 has two distinct execution modes**, as indicated below.



## 2.2.3 FP and Advanced SIMD registers based ISA extensions (9)

### Extension of the GPRs in the ARMv8 ISA [63], [66]

In the AArch64 mode the ARMv8 ISA version expands the **number of GPRs** from **13 32-bit registers to 31 64-bit wide registers**, as shown in the next Figure.



GPRs in the ARMv7 and the AArch32 execution mode of the ARMv8 ISA

GPRs in the AArch64 execution mode of the ARMv8 ISA

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (10)

Extension of the FP and advanced SIMD registers in the ARMv8 ISA [66]

In the AArch64 mode the ARMv8 ISA version expands the **number of FP and advanced SIMD registers from 16 (available in the ARMv7 ISA) to 32**, as seen below.

128-bit wide

V0
V1
V2
.
.
V12
V13
V14
V15

128-bit wide

V0
V1
V2
V3
.
.
V12
V13
V14
.
.
V30
V31

FP and advanced SIMD registers  
in ARMv7 and the AArch32 execution  
mode of the ARMv8 ISA

FP and advanced SIMD registers  
in the AArch64 execution mode of the  
ARMv8 ISA

## 2.2.3 FP and Advanced SIMD registers based ISA extensions (11)

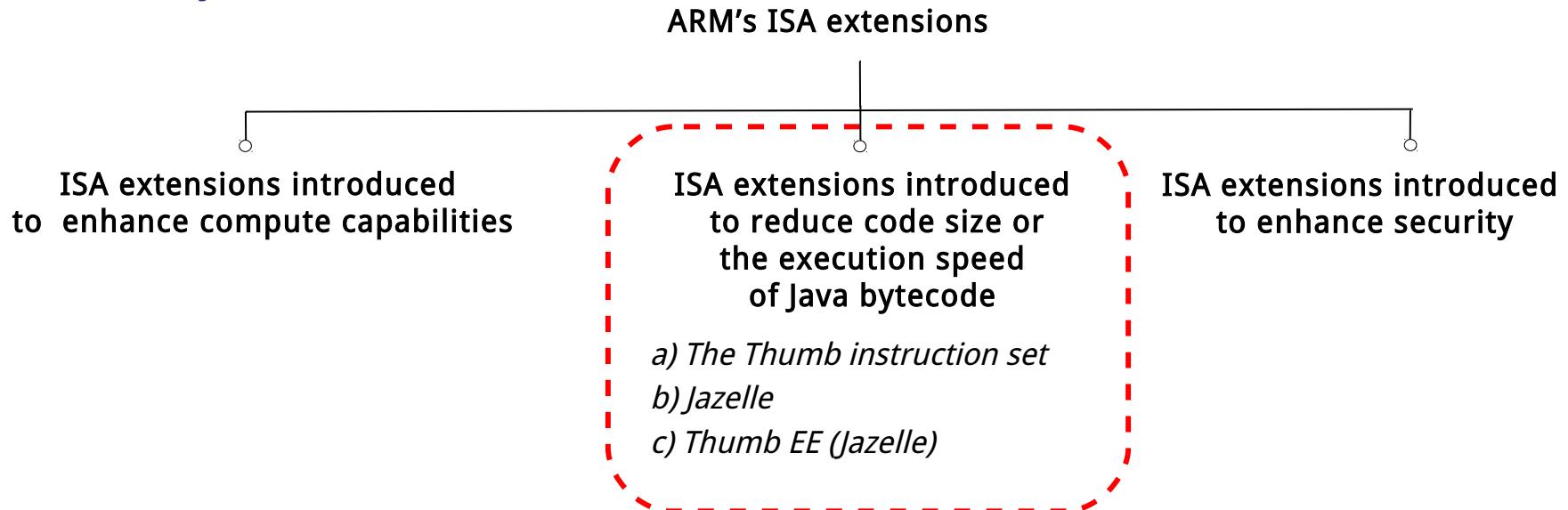
### Use of the FP and Advanced SIMD registers in the AArch64 execution mode [66]

	127	112	111	96	95	80	79	64	63	48	47	32	31	16	15	0										
32 128-bit registers	Vn																									
128-bit vector of 64-bit elements (.2D)	.D								.D																	
	[1]				[0]																					
128-bit vector of 32-bit elements (.4S)	.S				.S				.S				.S													
	[3]				[2]				[1]				[0]													
128-bit vector of 16-bit elements (.8H)	.H		.H		.H		.H		.H		.H		.H		.H											
	[7]		[6]		[5]		[4]		[3]		[2]		[1]		[0]											
128-bit vector of 8-bit elements (.16B)	.B		.B		.B		.B		.B		.B		.B		.B											
	[15]		[14]		[13]		[12]		[11]		[10]		[9]		[8]		[7] [6] [5] [4] [3] [2] [1] [0]									
32 64-bit registers	Vn																									
64-bit vector of 32-bit elements (.2S)	.S								.S																	
	[1]				[0]																					
64-bit vector of 16-bit elements (.4H)	.H				.H				.H				.H													
	[3]				[2]				[1]				[0]													
64-bit vector of 8-bit elements (.8B)	.B		.B		.B		.B		.B		.B		.B		.B											
	[7]		[6]		[5]		[4]		[3]		[2]		[1]		[0]											

2.3 ISA extensions introduced to reduce code size or  
the execution speed of Java bytecode

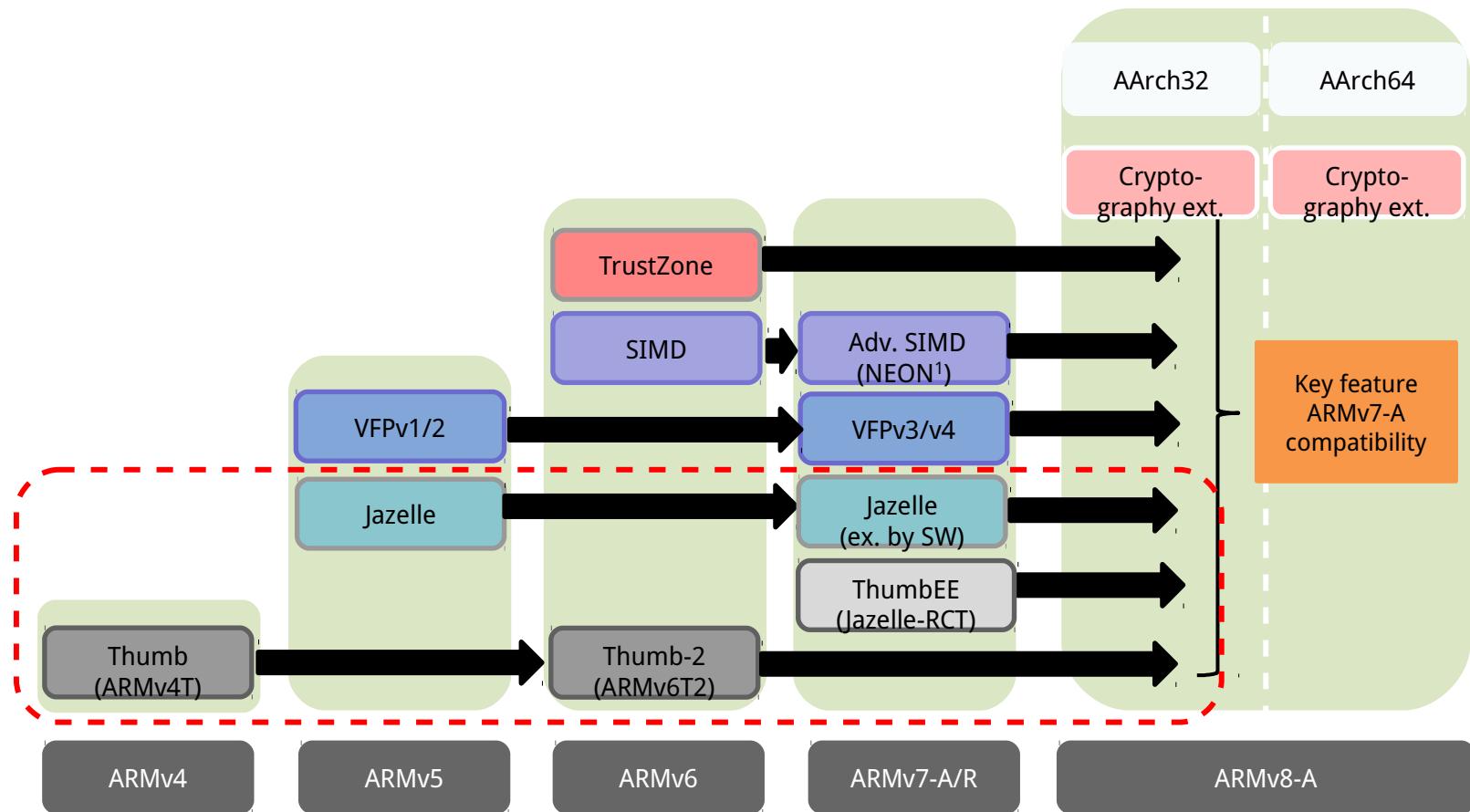
## 2.3 ISA extensions introduced to reduce code size (1)

### 2.3 ISA extensions introduced to reduce code size or the execution speed of Java bytecode -1



## 2.3 ISA extensions introduced to reduce code size (2)

### ISA extensions introduced to reduce code size -2 (Based on [64])



<sup>1</sup>The Advanced SIMD architecture extension is commonly referred to as the NEON technology.

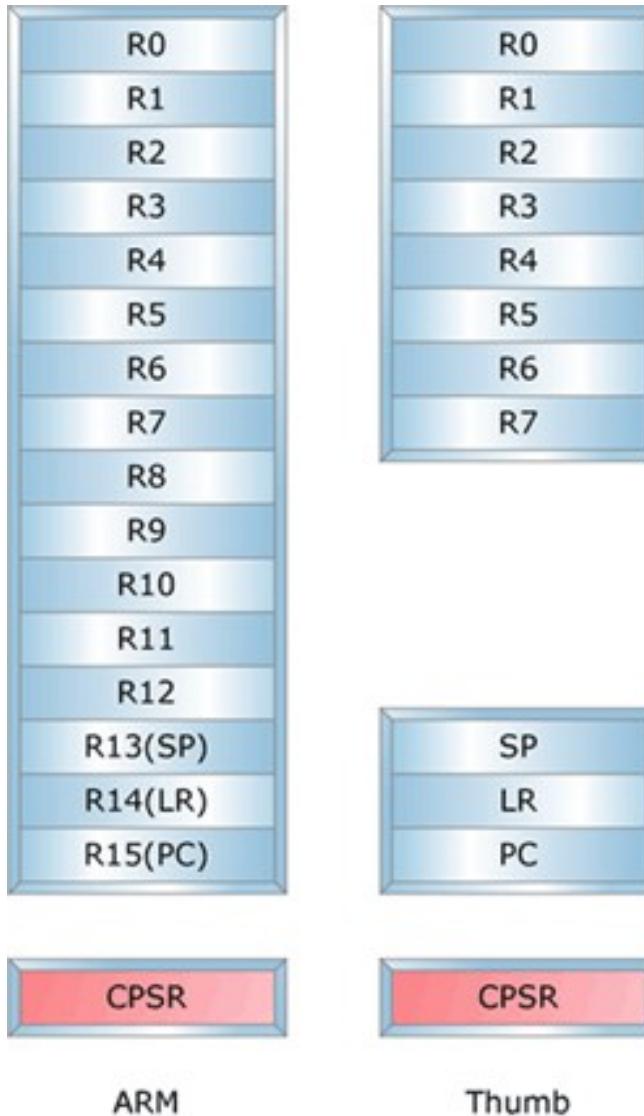
## 2.3 ISA extensions introduced to reduce code size (3)

### a) The Thumb instruction set

- This is an **alternative instruction set** that provides **better code density**.
- It has been introduced in the ARMv4 ISA.
- Processors with the **T suffix** provide beyond the default 32-bit ARM **also the 16-bit Thumb instruction set**.
- **Every Thumb instruction** is encoded in **16-bits**.
- The Thumb instruction set is a **subset** of the ARM instruction set.
- In the Thumb instruction set there are **only 8 GPRs** available for the programmer, as shown in the next Figure.

## 2.3 ISA extensions introduced to reduce code size (4)

Available GPR register sets in the ARM and the Thumb ISA [63]



## 2.3 ISA extensions introduced to reduce code size (5)

### b) Jazelle

It is ARM's [third ISA option](#), introduced in the ARMv5 ISA, as indicated below.

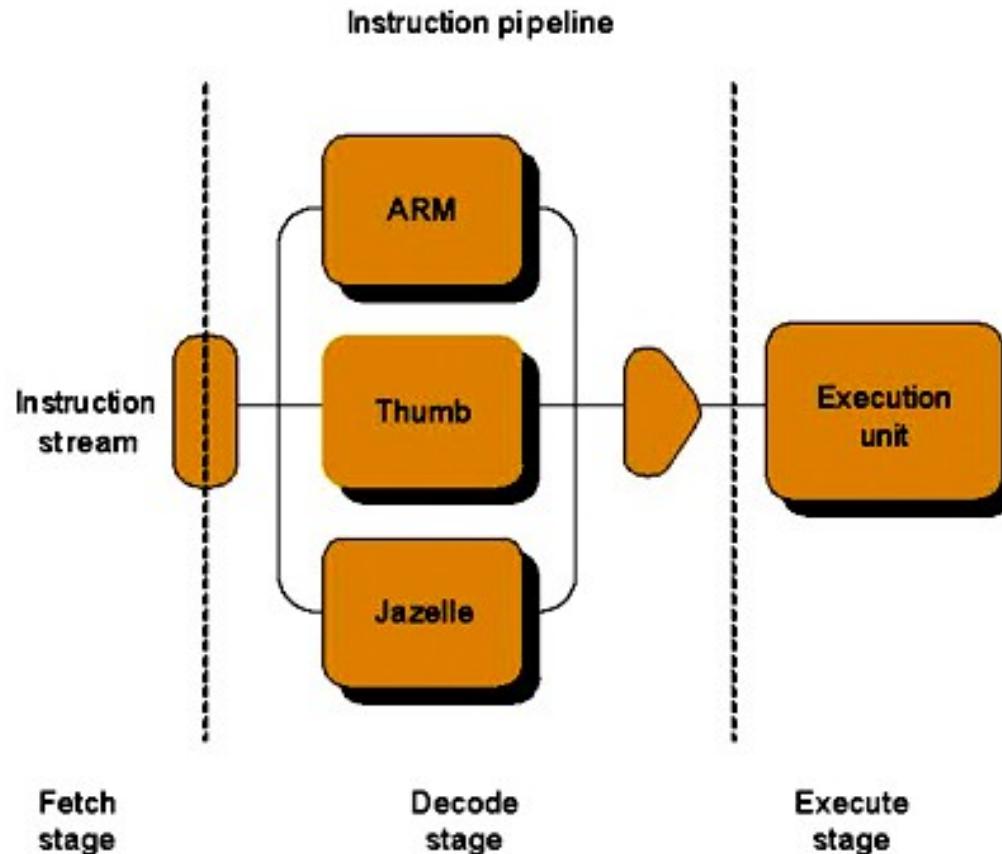


Figure: The Jazelle ISA extension as ARM's third ISA alternative [67]

It aims at [accelerating the execution of Java bytecode](#).

## 2.3 ISA extensions introduced to reduce code size (6)

### c) ThumbEE (Jazelle RCT)

- ThumbEE (JazelleRCT) is a Thumb like instruction set to efficiently execute bytecode for a virtual machine, like the Java Virtual Machine (JVM).
- It is beneficial e.g. **for just-in-time compilation from a portable bytecode in Java execution environment** as the compiled binary will have smaller code size than the code compiled for the ARM or the Thumb 2 instruction set.
- Thumb EE was introduced in the ARMv6 ISA.

RCT: Runtime Compilation Target

## 2.3 ISA extensions introduced to reduce code size (7)

Remark: Just-in-time (JIT) compilation in Java environment -1 [73]

- Java *bytecode* is a platform neutral intermediate language.
- Java bytecode programs are loaded and run by a Java Virtual Machine (JVM), also known as a Java Runtime Environment (JRE).

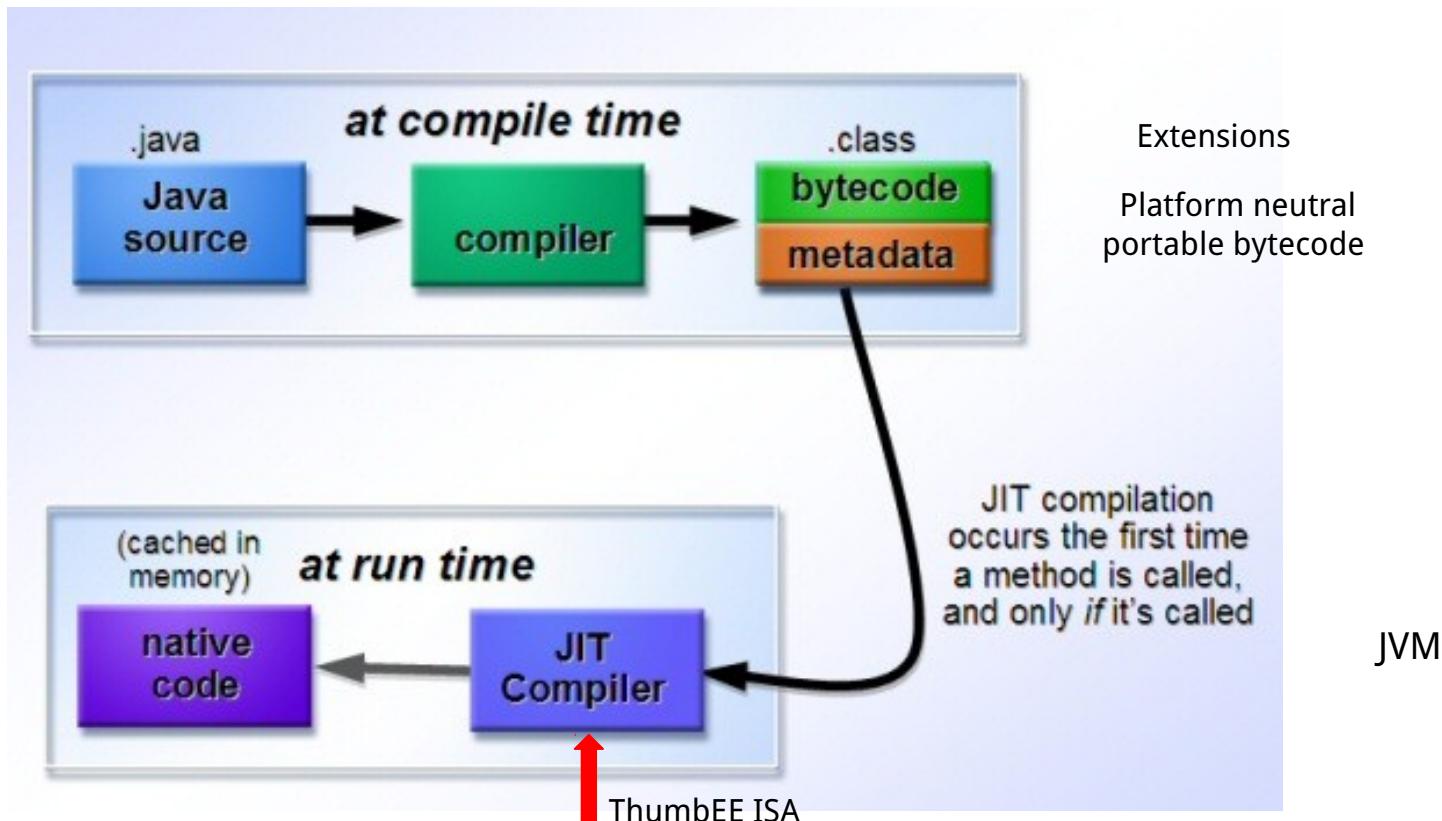


Figure: Just-in-time compilation in Java environment [73]

## 2.3 ISA extensions introduced to reduce code size (8)

Remark: Just-in-time (JIT) compilation in Java environment -2 [73]

- The *JIT compiler* at runtime converts bytecode into native machine code.
- JIT compilation occurs when each method is called at the first time, after which the native code for that method remains cached in memory; this means that subsequent executions of that method run as fast as native programs.

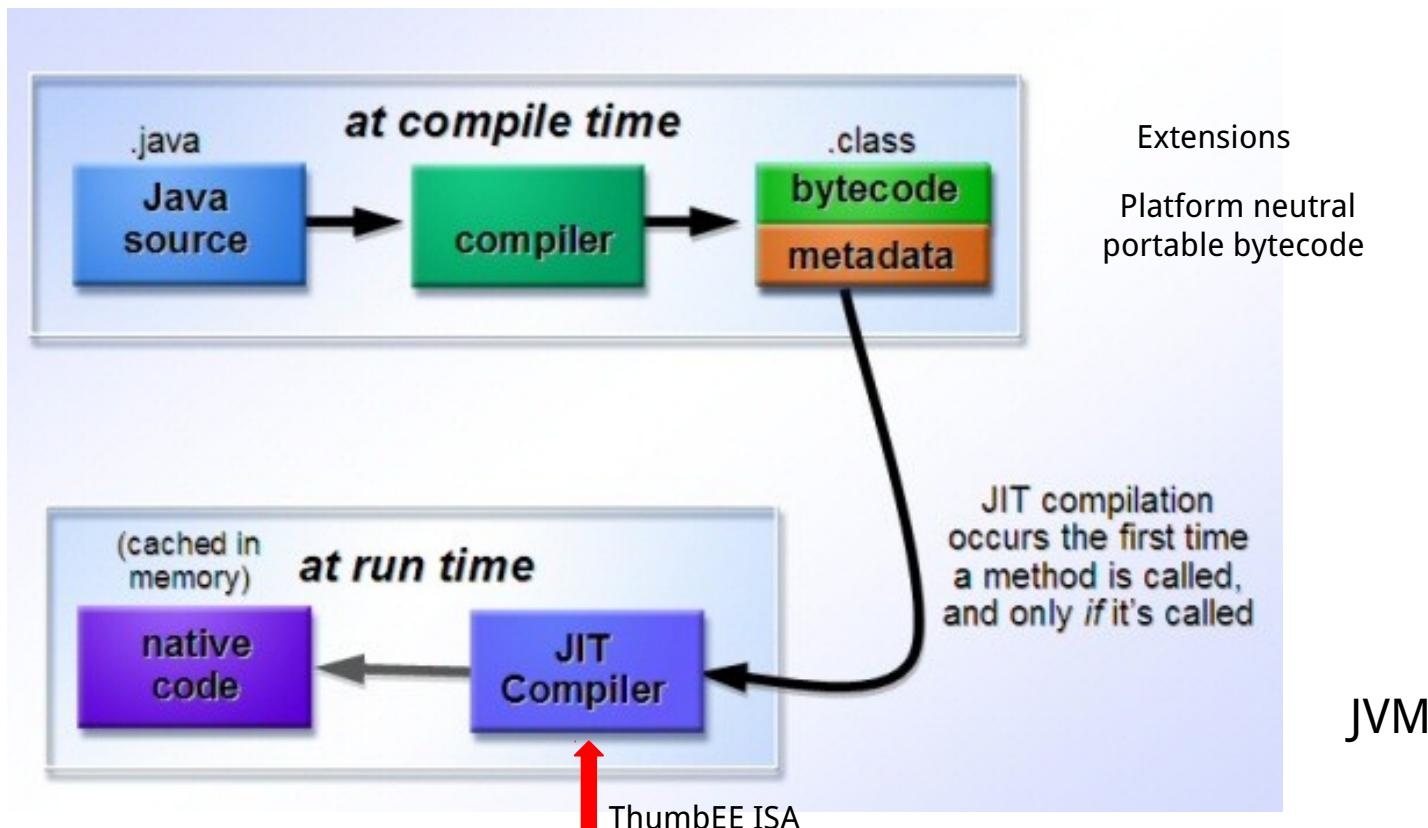
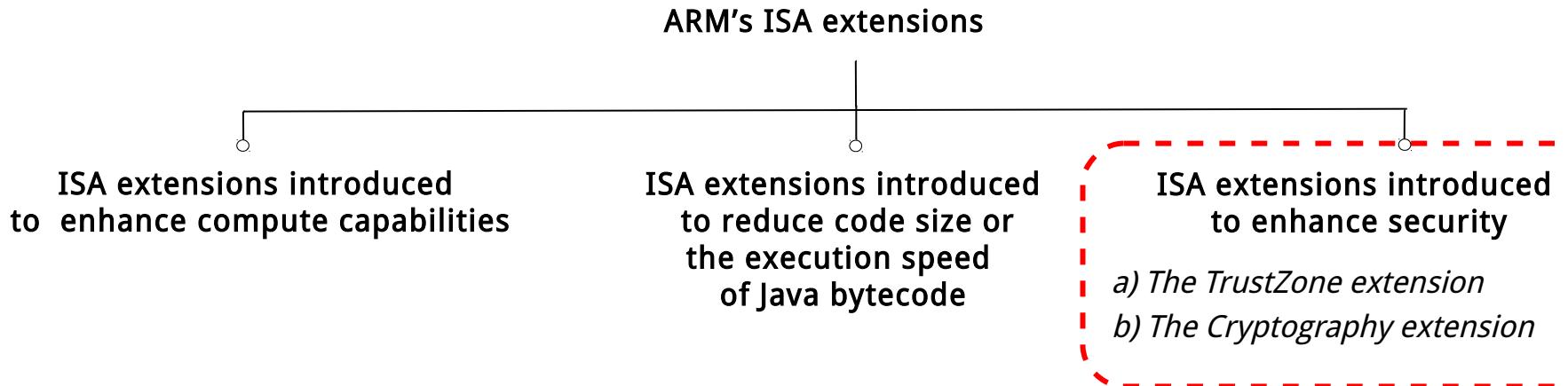


Figure: Just-in-time compilation in Java environment [73]

## 2.4 ISA extensions introduced to enhance security

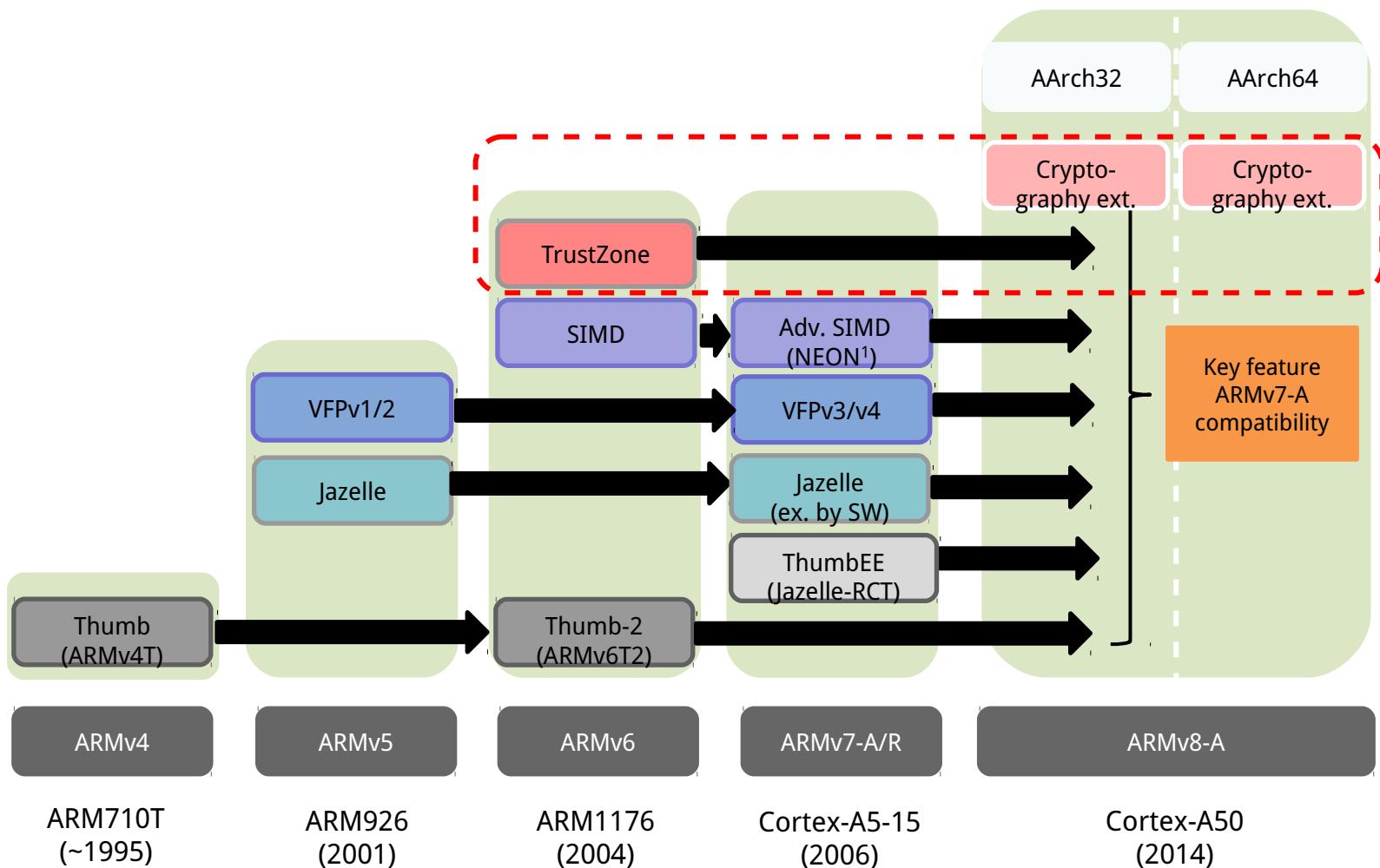
## 2.4 ISA extensions introduced to enhance security (1)

### 2.4 ISA extensions introduced to enhance security -1



## 2.4 ISA extensions introduced to enhance security (2)

### ISA extensions introduced to enhance security -2 (Based on [64])



<sup>1</sup>The Advanced SIMD architecture extension is commonly referred to as the NEON technology.

## 2.4 ISA extensions introduced to enhance security (3)

### a) The TrustZone extension [68]

- It provides a **system-wide protection** against possible attacks.
- It is achieved **by partitioning system wide hardware and software resources** so that **they exist in one of two worlds**;
  - in the **Secure world** for the security subsystem and
  - the **Normal world** for everything else.
- Hardware logic of the TrustZone ensures that no Secure world resources can be accessed from the Normal world.
- The trustZone extension was introduced as part of the ARMv6 ISA.
- For details see e.g. [68].

## 2.4 ISA extensions introduced to enhance security (4)

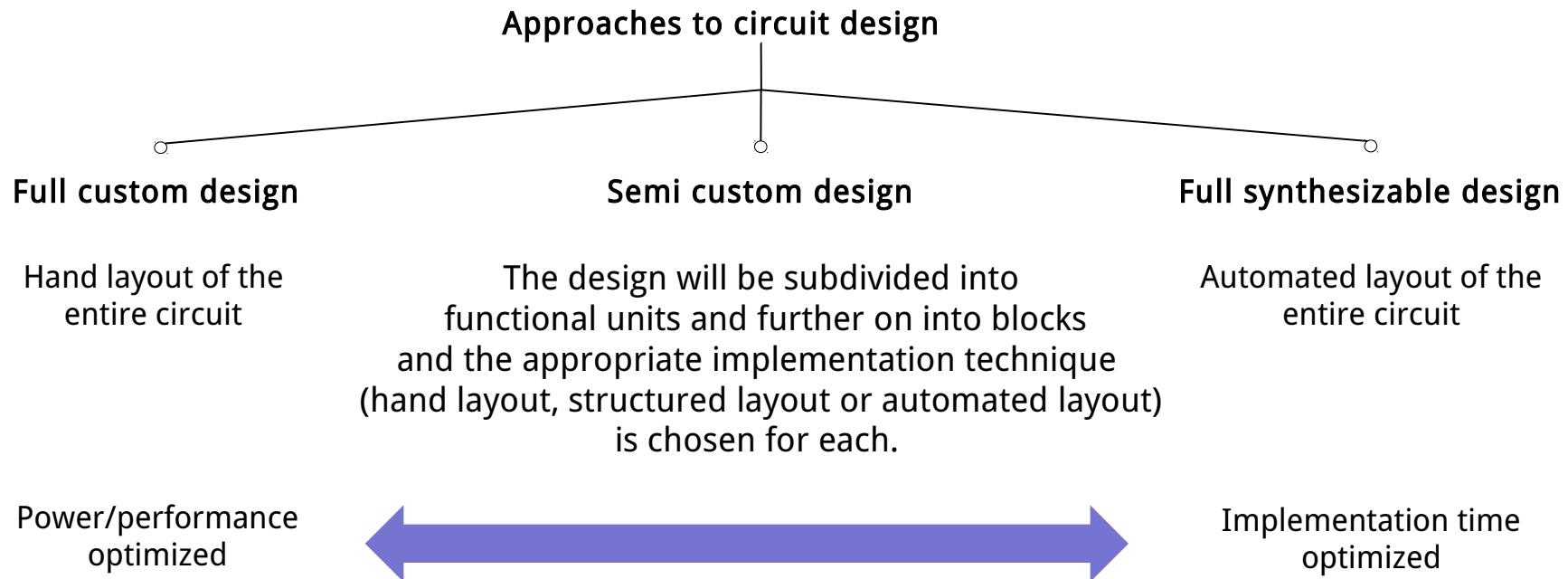
### b) The Cryptography extension [69]

- It adds new instructions to accelerate the execution of cryptographic algorithms, like
  - Encryption/decryption according to the Advanced Encryption Standard (AES),
  - Secure Hash Algorithm (SHA) functions SHA-1, SHA-224, and SHA-256.
- It was introduced as part of the ARMv8 ISA.
- It is similar to Intel's AES-NI ISA extension introduced along with the Westmere basic architecture (2009).

### 3. Approaches to circuit design

### 3. Approaches to circuit design (1)

#### 3. Approaches to circuit design



### 3. Approaches to circuit design (2)

#### Full custom design approach [1]

- It is the traditional way to design circuits, like processors.
- It means manual fine tuning the design for optimizing power consumption and or performance.
- Nevertheless, it implies long design times and costs thus most recent designs use a semi custom or full automated approach.

### 3. Approaches to circuit design (3)

#### Semi custom design approach [1]

- In this case the design will be subdivided into functional units and further on into blocks and the appropriate implementation technique (hand layout, structured layout or automated layout) is chosen for each.

### 3. Approaches to circuit design (4)

#### a) Hand layout of blocks [2]

- Hand layout is deserved for data paths and queues which are regular structures that allow a circuit designer to spot the regularity and benefit of which typically results in a better design than would be achieved by automated layout.
- By contrast, the layout of control logic is a very complex task where automated tools cannot be beaten by custom layout.

### 3. Approaches to circuit design (5)

#### b) Structured layout of blocks [1]

- The structured approach is typically used for regular structures, like datapaths.
- In this approach the blocks will be manually mapped into the gate level and also the logic gates of the blocks are manually placed to maintain a regular data-flow within the blocks instead of generating a random gate structure by synthesis.

Nevertheless, the routing of the circuit elements is done automatically.

- This approach offers more control over the design than an automated synthesis approach and leads to a more predictable timing behavior.

On the other hand it yields better performance and less area than traditional techniques.

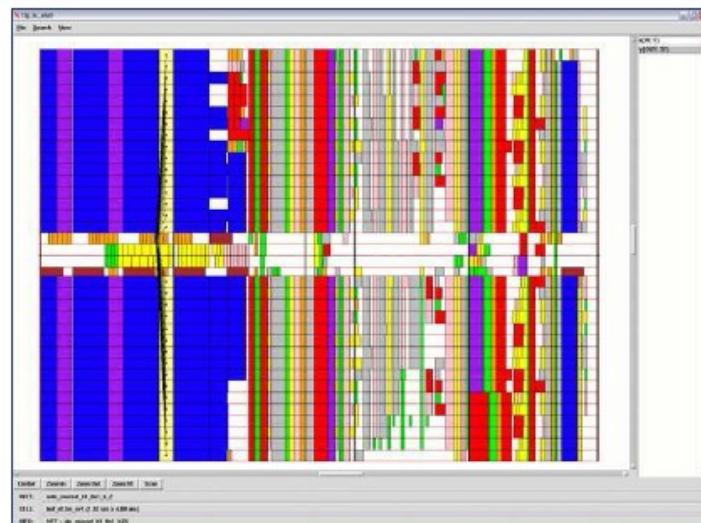


Figure: Regular datapath structure [3]

### 3. Approaches to circuit design (6)

Benefits of the structured layout vs. fully synthesized layout [3]

Results of detailed comparison of structured vs synthesis for one unit:

Structured vs. Synthesis	Structured Improvement
Cycle time (nvt only)	18%
Cycle time (mixed vt)	8%*
Area	-5%
Dynamic Power	6%
Static Power	53%
Cell Count	2%

Gains most apparent only after RTL optimized from synthesis feedback

\*Synthesized had 27% LVT cells. Structured 0.7%

### 3. Approaches to circuit design (7)

#### c) Automated layout of blocks [1]

The layout of control logic is a very complex task where automated tools cannot be beaten by custom or semicustom layout if time and design cost is of consideration.

### 3. Approaches to circuit design (8)

Final words about the partition of a semi custom design [1]

The decision which parts should be designed by hand layout and which parts by semi-custom or automated layout is a design trade-off between performance and power requirements vs.design time (cost).

### 3. Approaches to circuit design (9)

Example for a semi custom design: The Cortex-A8 [3]

- The Cortex-A8 processor is partitioned at the microarchitecture level into:
  - Synthesis: Non-critical areas
  - Structured: Timing/Power critical areas
  - Customs (with clean interfaces): RAM/Regfile

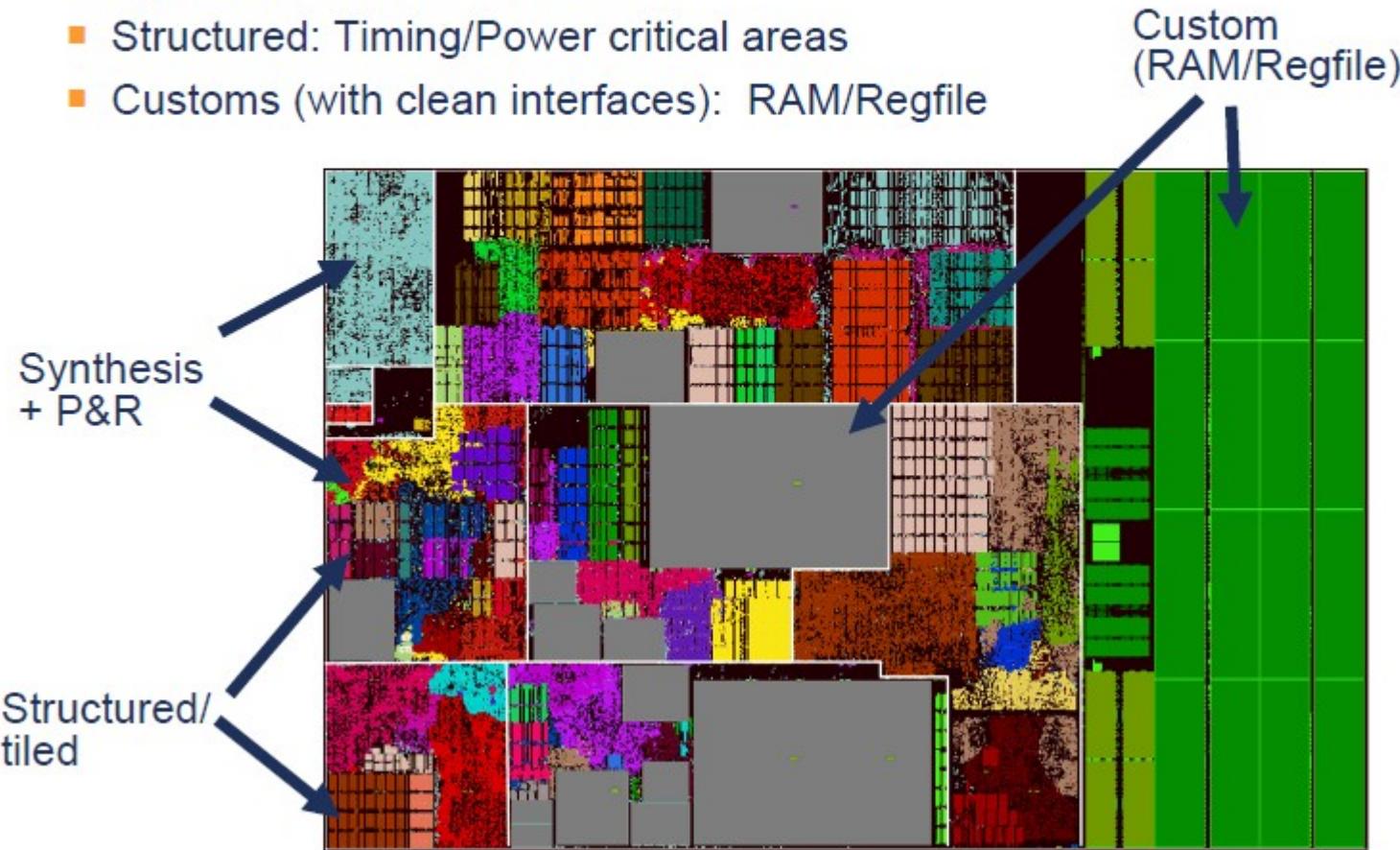


Figure: Partitioning the Cortex-A8 into blocks implemented by different design approaches [3]

### 3. Approaches to circuit design (10)

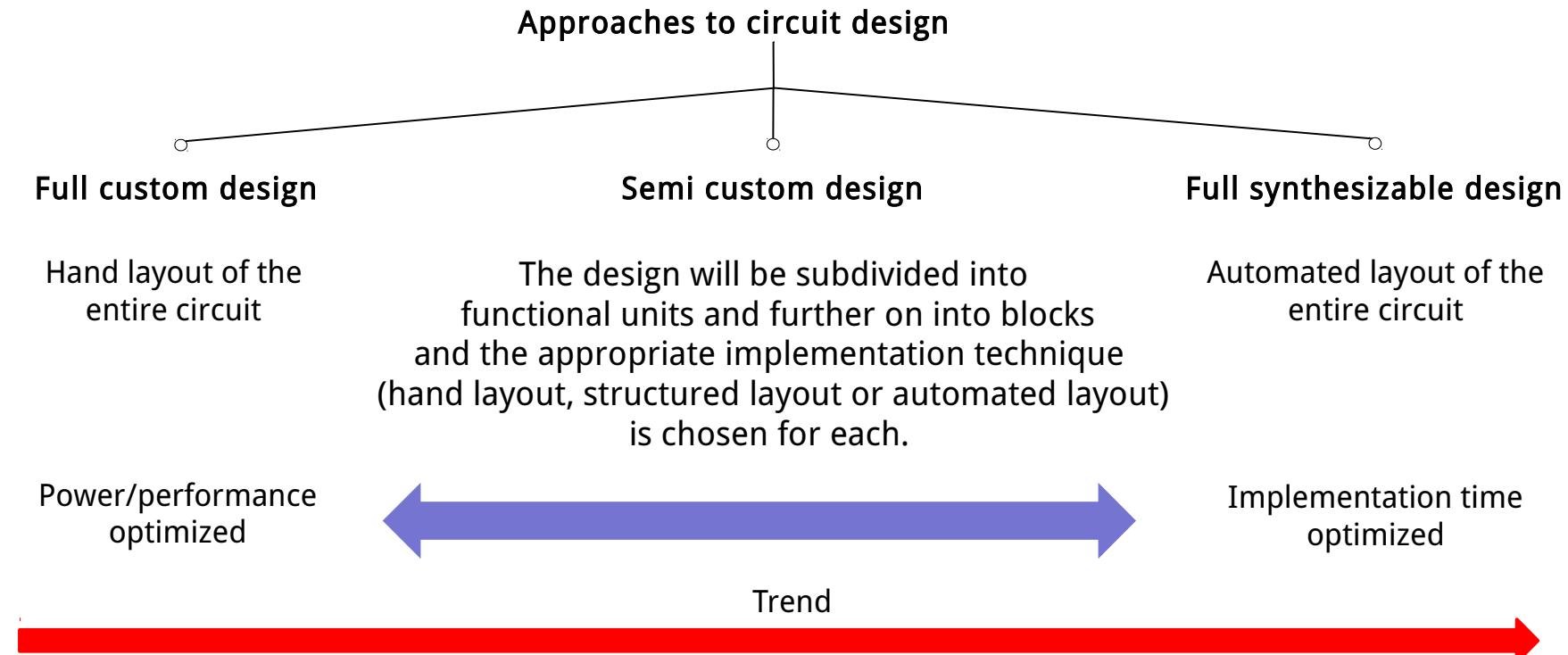
#### Fully synthesizable design approach [1]

- Recent tools allow already a **fully synthesizable design**, meaning that there is **no need to go to a hand-layout approach** for some critical parts of the design.
- **Key benefits** of a fully synthesizable design
  - Fully synthesizable designs allow a **simple scaling of the design** for various various geometries, e.g. from 28 nm to 16nm.
  - In addition, such designs **shorten the design process** and allow licensees to get to market earlier.
- ARM's **first fully synthesizable design** was the **Cortex-A9** processor (announced in 2007).
- Previous designs, like that for the Cortex-A8, included partly hand layout and partly automated layout.

### 3. Approaches to circuit design (11)

#### Evolution of the approaches used to circuit design [1]

- Over time more and more advanced standard cell libraries were developed that have a large variety of cell types and drive strengths which lessens the need for custom design.
- This is the reason why recently automated design tools are typically used for processor design.



## 4. Overview of ARM's processor series

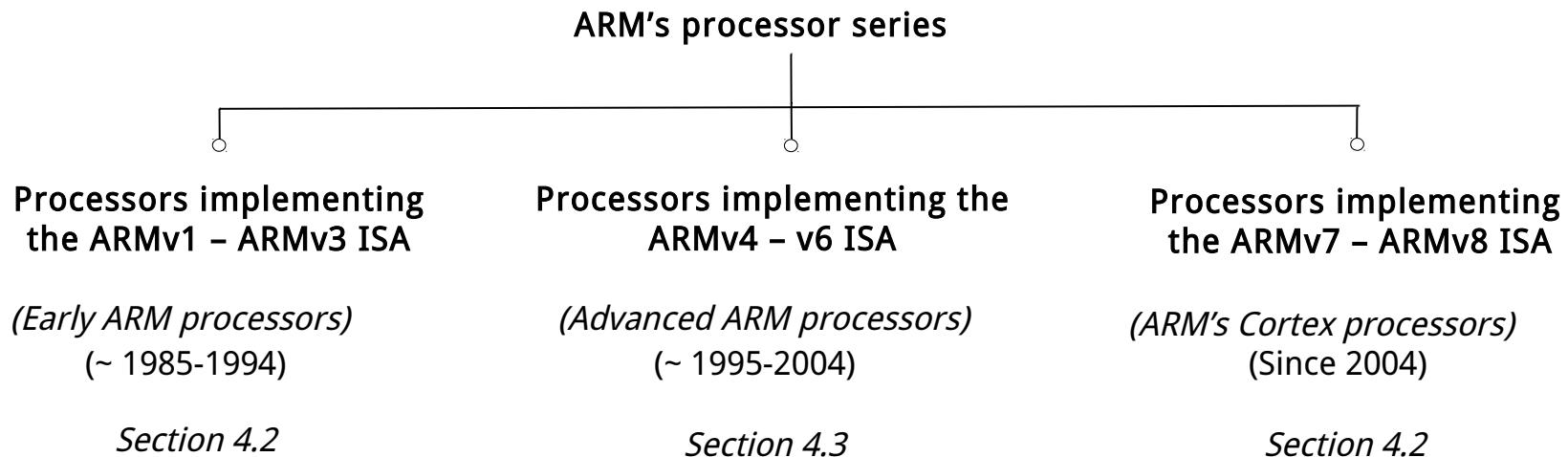
- 4.1 Introduction
- 4.2 Processors implementing the ARMv1 – ARMv3 ISA
- 4.3 Processors implementing the ARMv4 – ARMv6 ISA
- 4.4 Processors implementing the ARMv7 – ARMv8 ISA

## 4.1 Overview of ARM's processor series

## 4.1 Overview of ARM's processor lines (1)

### 4.1 Introduction

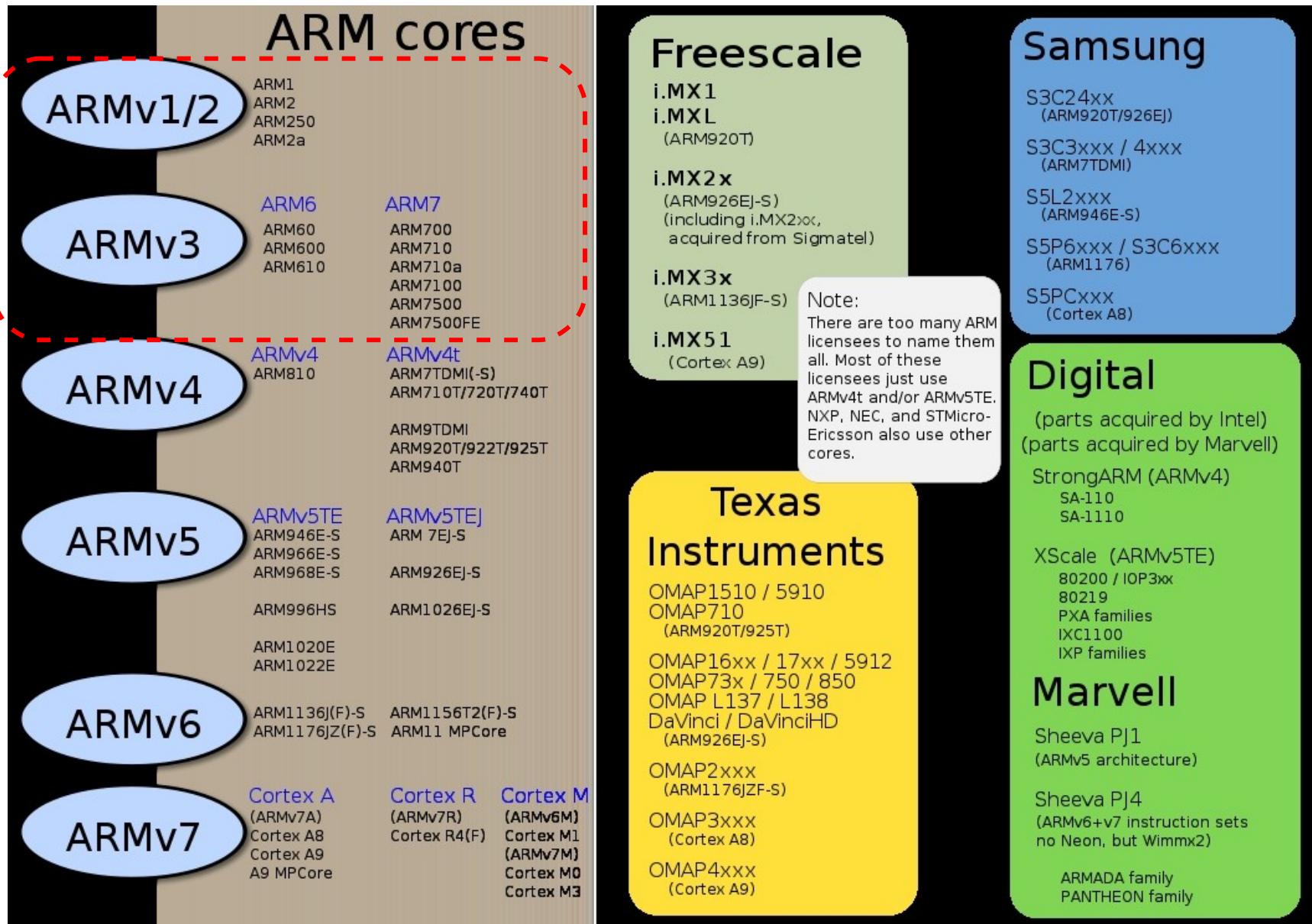
Subsequently, we give an overview of ARM's processor series subdivided into three sections, according their underlying ISAs, as follows.



## 4.2 Processors implementing the ARM v1 - ARM v3 ISA

## 4.2 Processors implementing the ARM v1 - ARM v3 ISA (1)

### 4.2 Processors implementing the ARMv1 – ARMv3 ISA [5]



## 4.2 Processors implementing the ARM v1 - ARM v3 ISA (2)

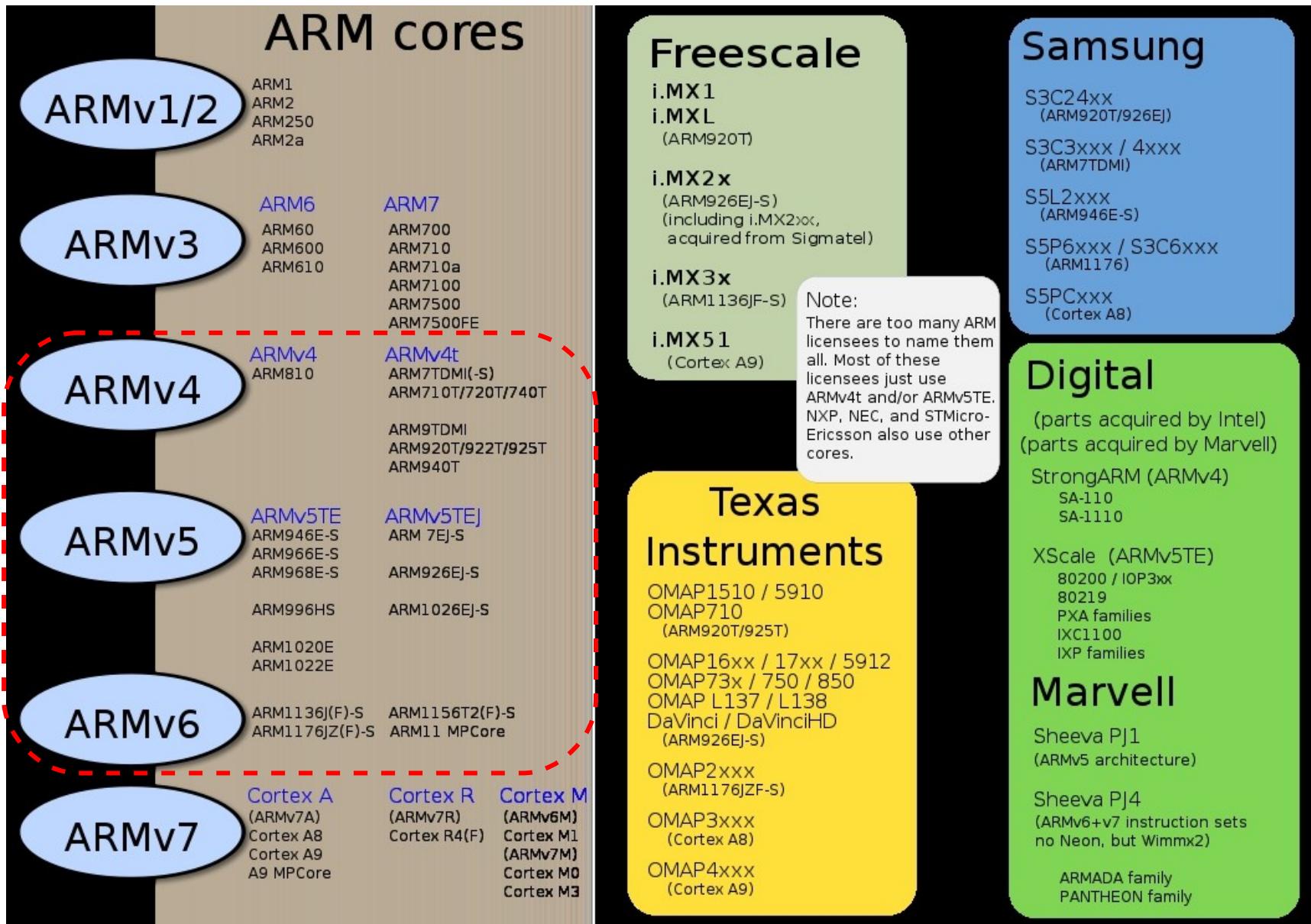
### Remarks

- As already discussed in Section 2.1
  - processors based on the ARM ISA versions ARMv1 and ARMv2 (like ARM1, ARM2 or ARM3) implement only a 26-bit address bus and a 32-bit data bus.
  - They are called **26-bit architectures**.
  - By contrast, processors based on the ARMv3 or higher ISA version support already a 32-bit address space and are known as **32-bit architectures up to the ARMv7 ISA**.
  - In the **ARMv8 ISA** the AArch64 mode supports already **64-bit addressing**.

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (1)

### 4.3 Processors implementing the ARMv4 – ARMv6 ISA [5]



## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (2)

Main extensions introduced in the ARMv4 – ARM v6 ISA versions (simplified)

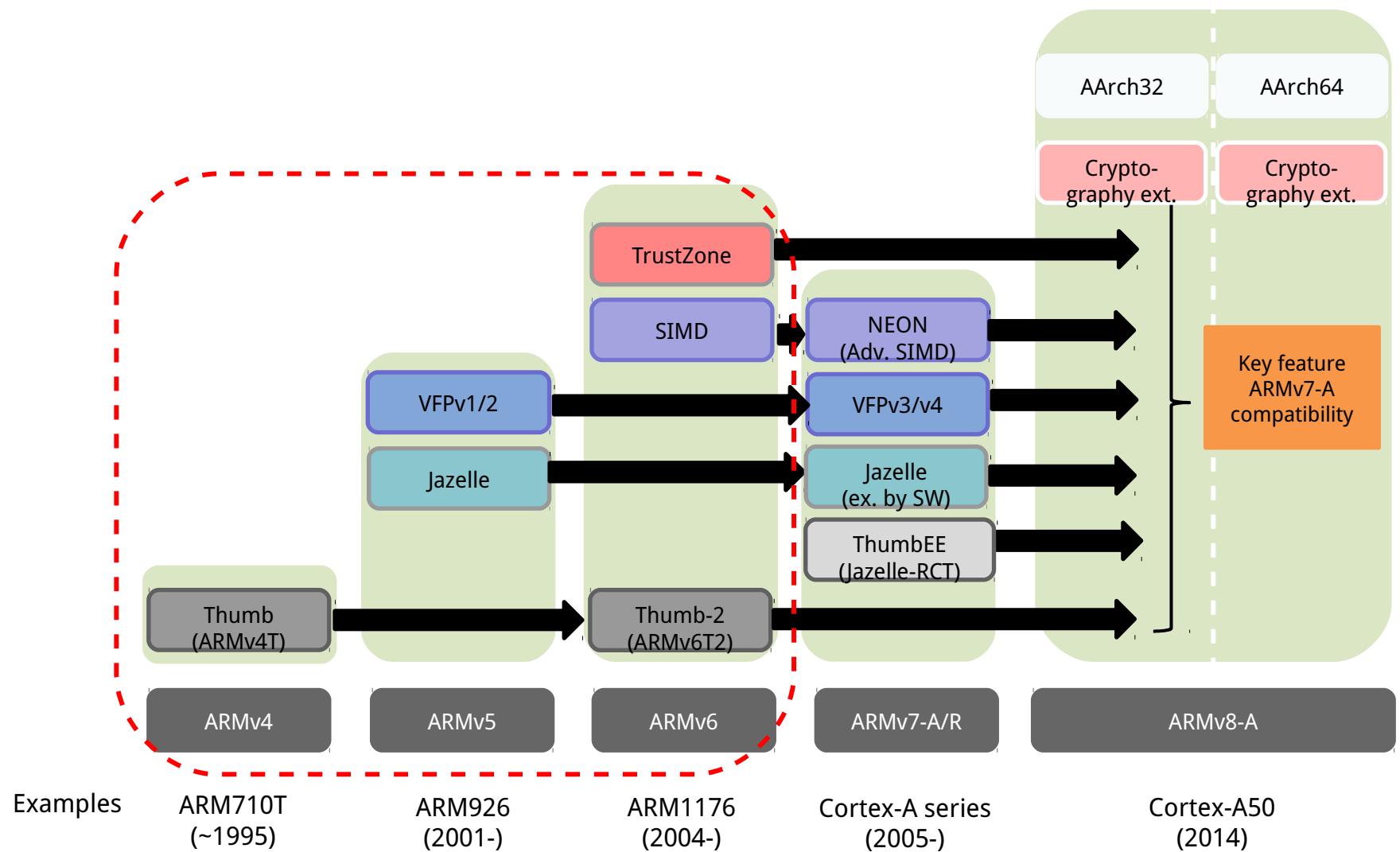
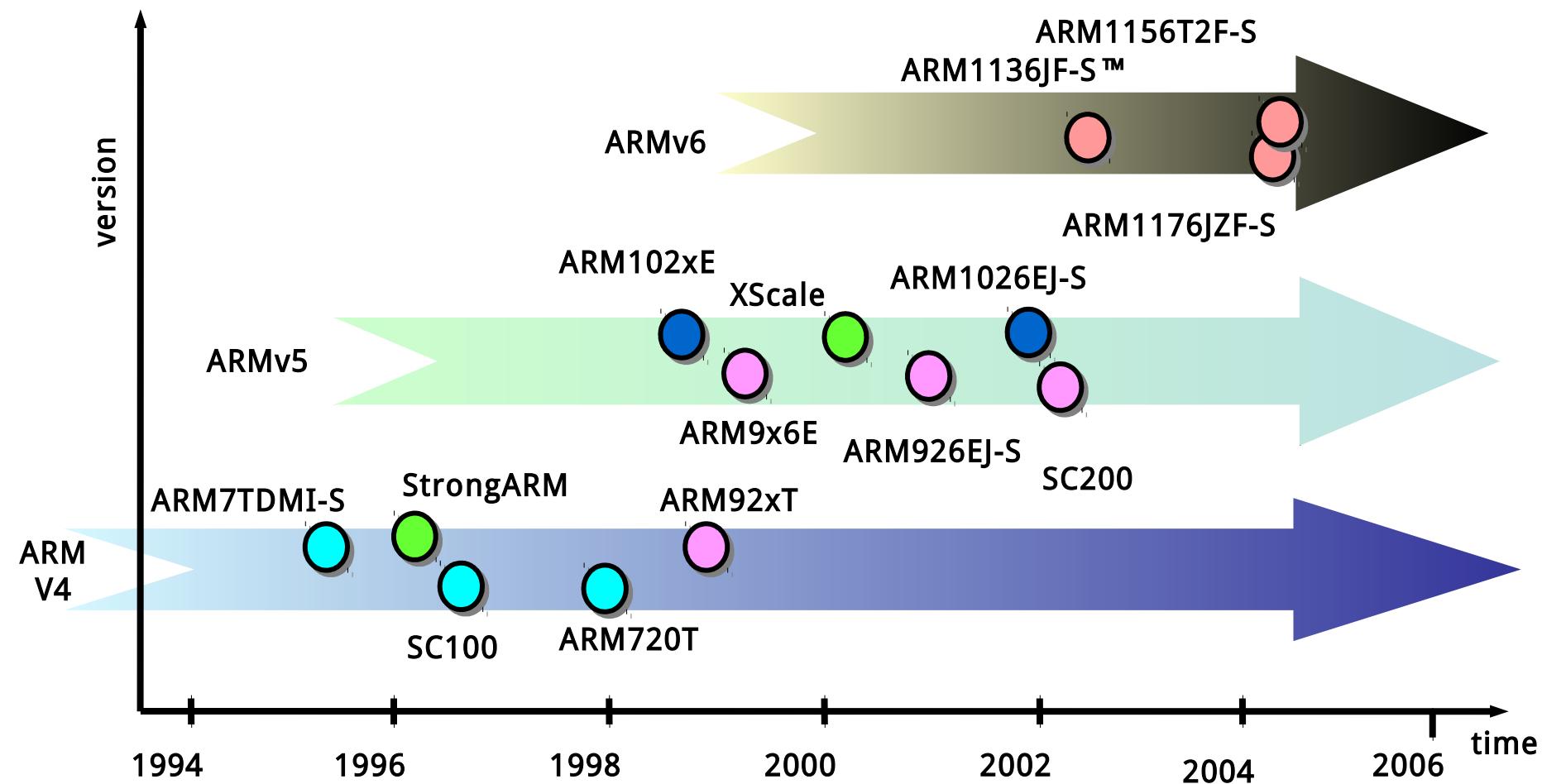


Figure: Enhancements of the ARMv6 ISA

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (3)

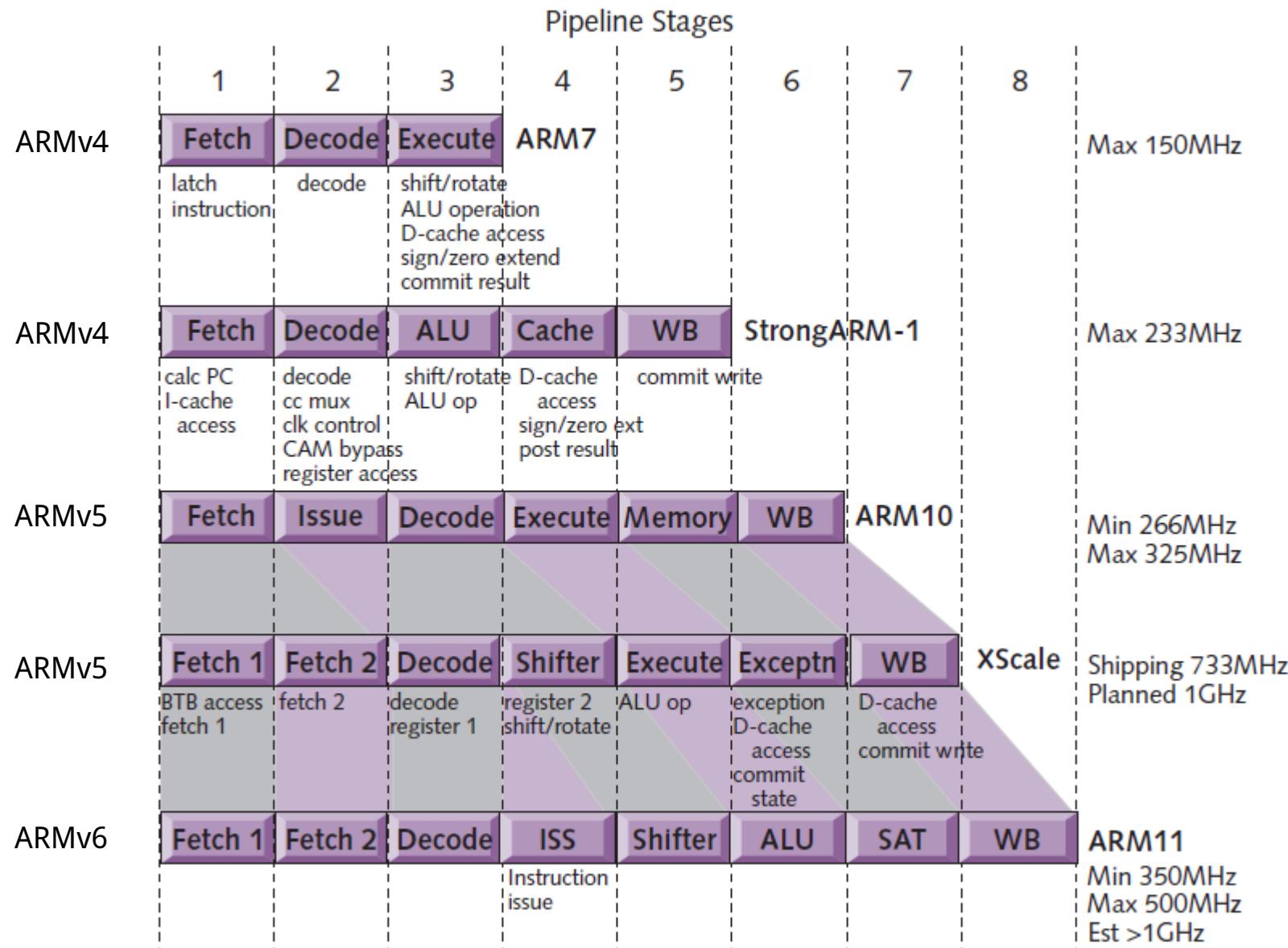
Overview of ARM's processors implementing the ARMv4 – ARMv6 ISA [5]



XScale is a trademark of Intel Corporation

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (4)

### Evolution of the pipeline length of ARM v4 – ARM v6 based processors [8]



## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (5)

Main features of the ARMv5 – ARMv6 processors (≈ 1999-2003) [57]

Feature	ARM9E™	ARM10E™	Intel® XScale™	ARM11™
Architecture	ARMv5TE(J)	ARMv5TE(J)	ARMv5TE	ARMv6
Pipeline Length	5	6	7	8
Java Decode	(ARM926EJ)	(ARM1026EJ)	No	Yes
V6 SIMD Instructions	No	No	No	Yes
MIA Instructions	No	No	Yes	Available as coprocessor
Branch Prediction	No	Static	Dynamic	Dynamic
Independent Load-Store Unit	No	Yes	Yes	Yes
Instruction Issue	Scalar, in-order	Scalar, in-order	Scalar, in-order	Scalar, in-order
Concurrency	None	ALU/MAC, LSU	ALU, MAC, LSU	ALU/MAC, LSU
Out-of-order completion	No	Yes	Yes	Yes
Target Implementation	Synthesizable	Synthesizable	Custom chip	Synthesizable and Hard macro
Performance Range	Up to 250MHz	Up to 325MHz	200MHz – >1GHz	350MHz - >1GHz

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (6)

Example: The ARM11/ARM11 MPCore processor

It implements the [ARMv6 ISA](#) and precedes the ARMv7 based Cortex line.

The evolution of the ARM11 line

10/2001: Disclosure of the ARMv6 ISA specification at the Microprocessor Forum

04/2002: ARM11 launched and details revealed at the Embedded Processor Forum

ARM11 is the first implementation of the ARMv6.

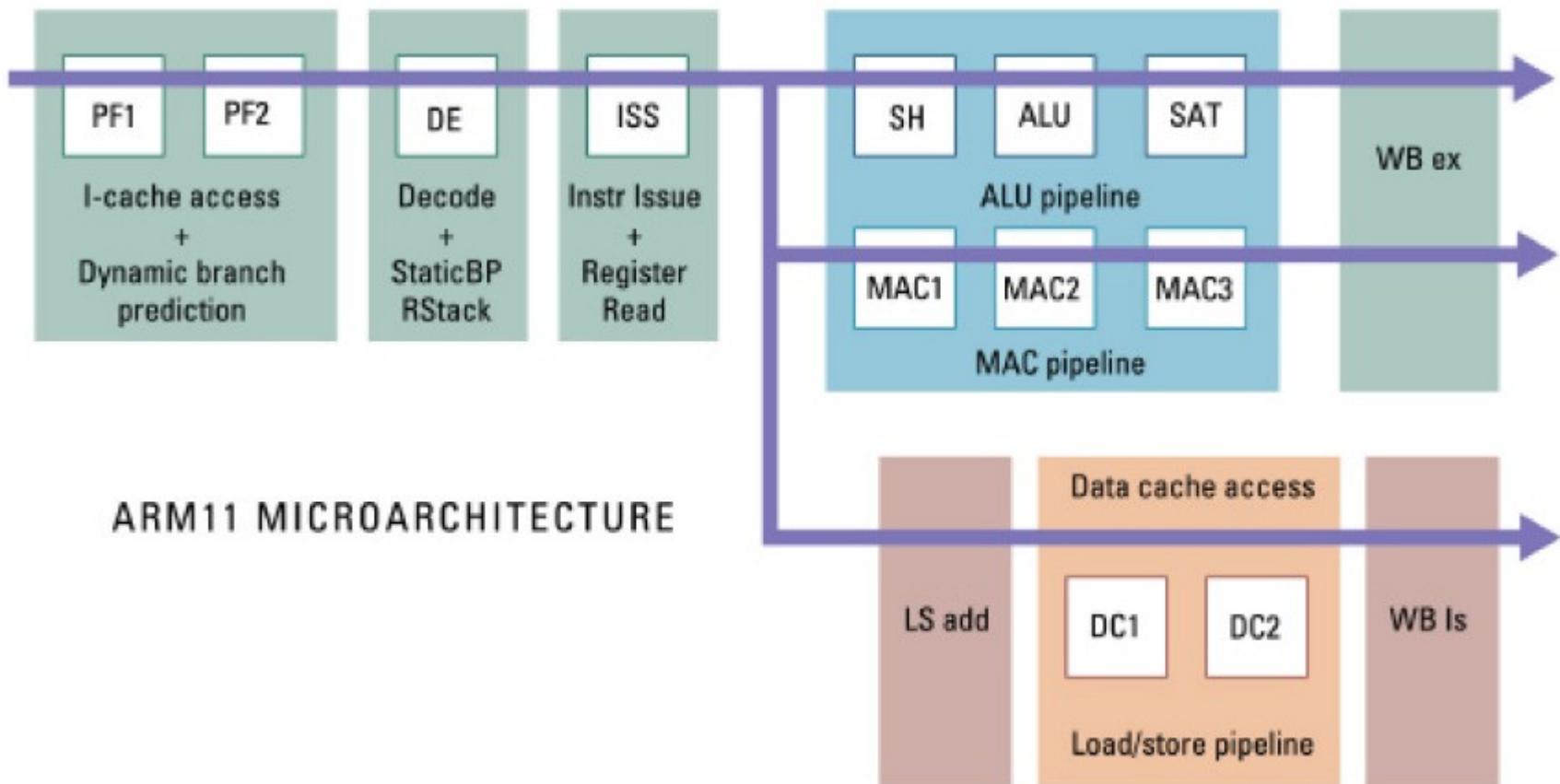
## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (7)

Key microarchitecture features of the ARM11

It is a **single issue in-order processor** with **three simultaneous operating pipelines** and a pipeline length of 8 stages, as indicated in the next Figure.

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (8)

### Pipeline structure of the ARM11 [57]



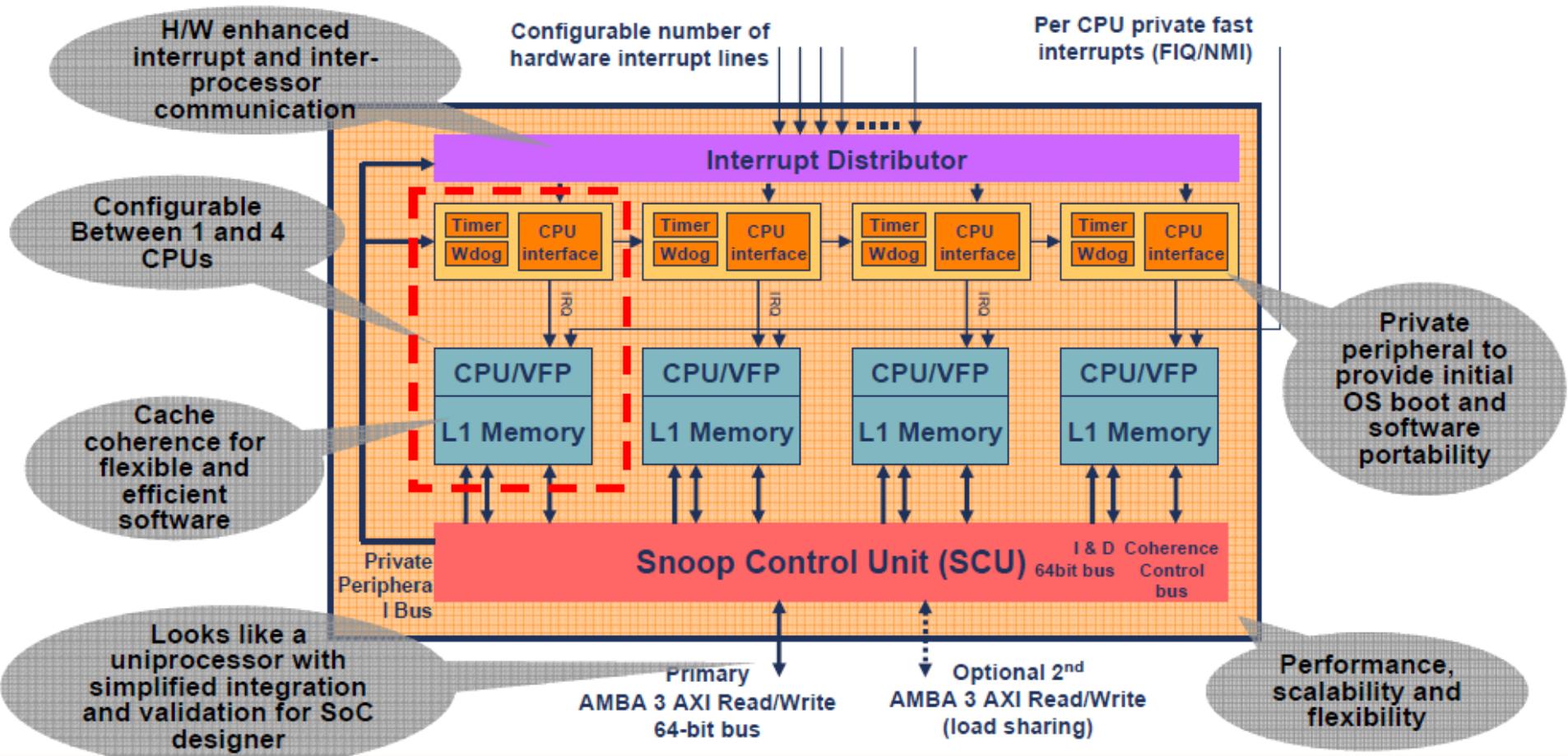
## 4.3 Processors implementing the ARM v4 - ARM v6 ISA (9)

### The ARM11 MPCore

- 07/2003: First public disclosure of the ARM11 MPCore.
- 05/2004: ARM11 MPCore (multi core ARM11 with 1-4 cores) available for licensing with an evaluation system for early software development.
- It is basically an up to four way cache coherent symmetric multicore processor using a modified MESI protocol.
- The ARM11 MPCore incorporates:
- IEM (Intelligent Energy Manager)  
It dynamically predicts the required performance and lowers the voltage and frequency accordingly.
- We note that issues of cache coherency are discussed in a separate Chapter.

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA 10)

### Block diagram of the ARM11 MPCore [9]



Note that the ARM11 MPCore **does not include an L2**.

## 4.3 Processors implementing the ARM v4 - ARM v6 ISA 11)

### Remark: Emergence of dual core processors

- Year of launching
- Dual core design
- 10/2001 IBM launches dual core POWER4
- 11/2002 IBM launches dual core POWER4+
- 05/2004 ARM announces the availability of the synthesisable ARM11 MPCore quad core processor
- 05/2004 IBM launches dual core POWER5
- 08/2004 AMD demonstrates first x86 dual core (Opteron) processor
- 04/2005 ARM demonstrates the ARM11 MPCore quad core test chip
  - in cooperation with NEC
- 04/2005 Intel launches dual core Pentium processors (Pentium D)
- 04/2005 AMD launches dual core Opteron server processors
- 06/2006 Intel launches the dual core Core 2 family
- 10/2007 ARM launches their first multicore Cortex model (the quad core Cortex A9 MPcore)

## 4.4 Processors implementing the ARM v7 - ARM v8 ISA

## 4.4 Processors implementing the ARM v7 - ARM v8 ISA (1)

### 4.4 Processors implementing the ARM v7 - ARM v8 ISA

- 10/2004 ARM introduced the **Cortex family** based on the ARMv7 ISA.
- It remained still a **32-bit architecture**.

## 4.4 Processors implementing the ARM v7 - ARM v8 ISA (2)

### Profiles of ARM's Cortex family [6], [7]

In 3/2005 ARM revealed technical specifications for the ARMv7 ISA and introduced **three family profiles** to optimize processors of their Cortex family for specific market segments:

#### The Cortex-A profile

It aims at **application processors for complex OS and user applications**, like processors in smartphones, tablets, netbooks, eBook readers etc.

#### The Cortex-R profile

It marks **embedded processors for real time applications**, like mass storage or printer controllers.

#### The Cortex-M profile

Processors of the M profile are optimized **for deeply embedded processors aimed at microcontroller and cost sensitive applications**, like automotive body electronics, or smart sensors.

## 4.4 Processors implementing the ARM v7 - ARM v8 ISA (3)

Extending the ARM Cortex family with the SecurCore profile in 10/2007

- In 10/2007 ARM introduced the **SecurCore profile**.
- It is optimized **for smart card and secure applications**.

## 4.4 Processors implementing the ARM v7 - ARM v8 ISA (4)

Recent ARM profiles  
and processors [6]

Cortex-A72
Cortex-A57
Cortex-A53
Cortex-A17
Cortex-A15
Cortex-A9
Cortex-A7
Cortex-A5
Cortex-R7
Cortex-R5
Cortex-R4
Cortex-M7
Cortex-M4
Cortex-M3
Cortex-M1
Cortex-M0+
Cortex-M0
SC000
SC100
SC300

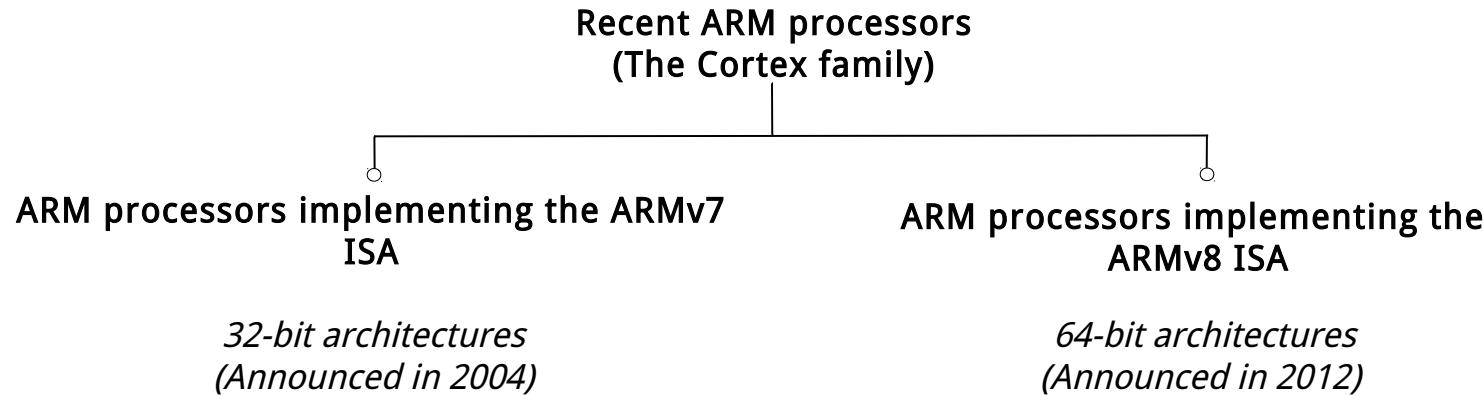
The diagram illustrates the recent ARM processor profiles and their corresponding models. It features four main sections: CORTEX-A (teal), CORTEX-R (blue), CORTEX-M (pink), and SECURCORE (cyan). Each section contains a list of processor models to its right.

- CORTEX-A:** Cortex-A72, Cortex-A57, Cortex-A53, Cortex-A17, Cortex-A15, Cortex-A9, Cortex-A7, Cortex-A5.
- CORTEX-R:** Cortex-R7, Cortex-R5, Cortex-R4.
- CORTEX-M:** Cortex-M7, Cortex-M4, Cortex-M3, Cortex-M1, Cortex-M0+, Cortex-M0.
- SECURCORE:** SC000, SC100, SC300.

## 4.4 Processors implementing the ARM v7 - ARM v8 ISA (1)

### Introducing the 64-bit ARM v8 ISA and related processors

- In 2012 ARM expanded their Cortex family by processors implementing the 64-bit ARMv8 ISA, as indicated below.

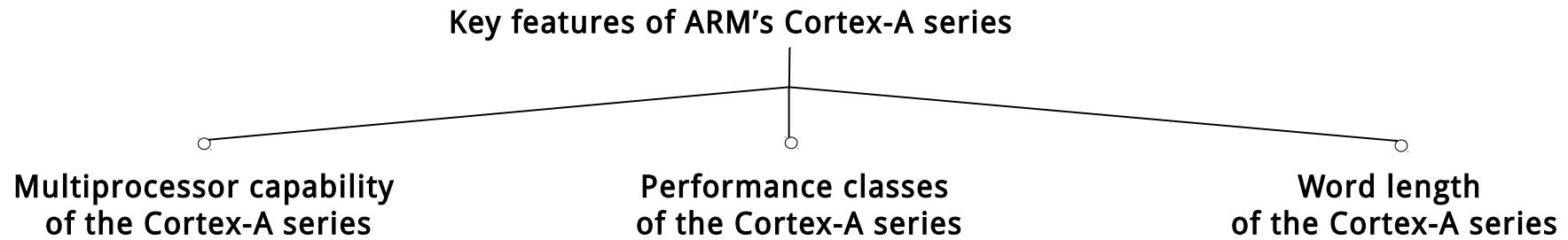


## 5. Overview of ARM's Cortex-A series

## 5. Overview of ARM's Cortex-A series (1)

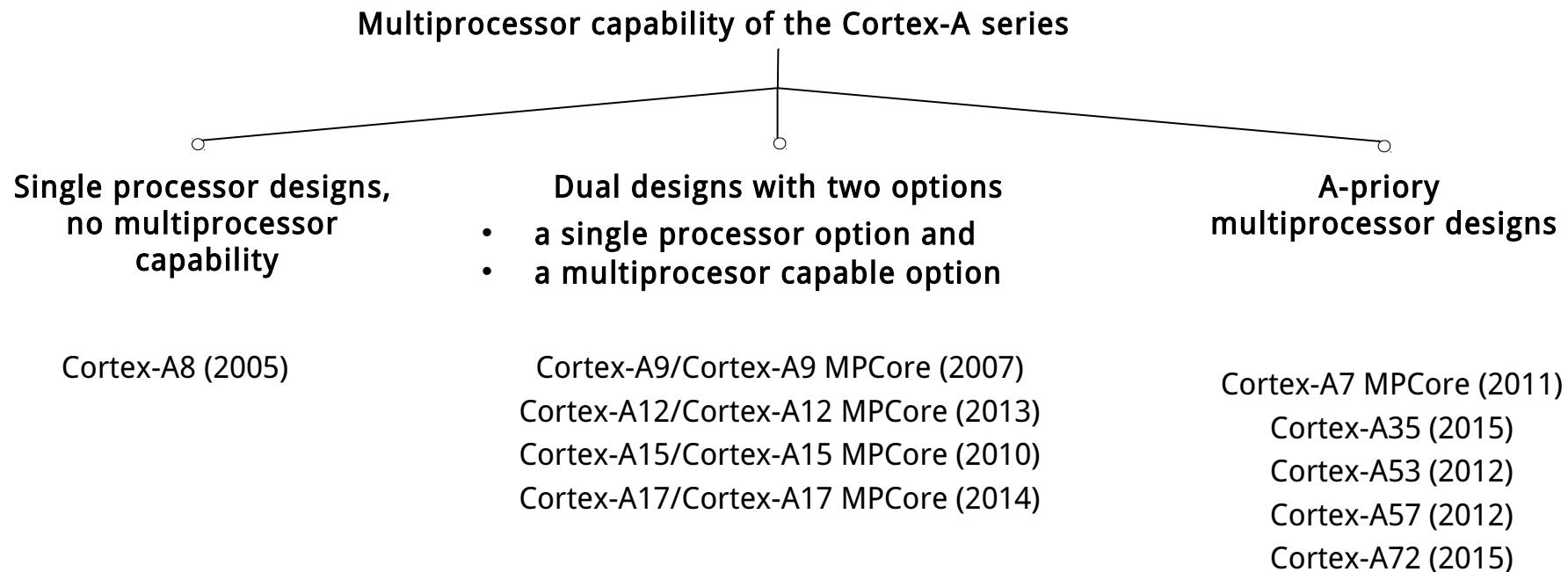
### 5. Overview of ARM's Cortex-A series

According to the general scope of this Lecture Notes, subsequently **we will be concerned only with the Cortex-A series.**



## 5. Overview of ARM's Cortex-A series (2)

### Multiprocessor capability of the Cortex-A series



Here we note that **in figures or tables we often omit the MPCore tag for the sake of brevity.**

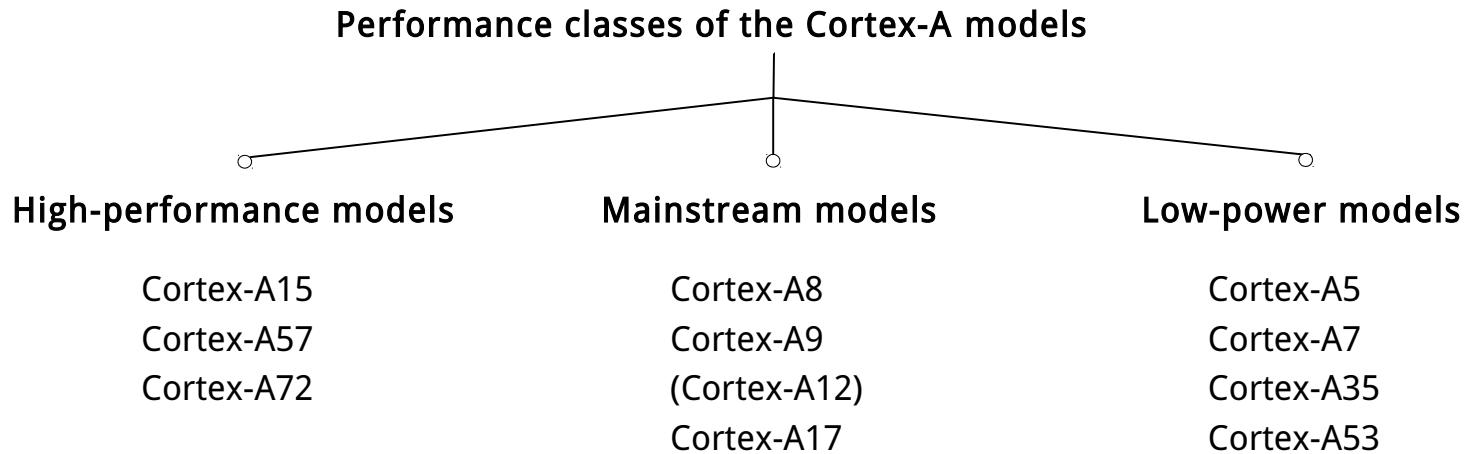
## 5. Overview of ARM's Cortex-A series (3)

### Remarks on the interpretation of the term MPCore by ARM

- ARM introduced the term **MPCore** in connection with the announcement of the [ARM11 MPCore](#) in 2004 and interpreted it as **multicore implementation** (actually including up to 4 cores).
- Along with the [ARM Cortex-A9 MPCore](#) ARM re-interpreted this term such that it indicates now the **multiprocessor capability** of the processor.

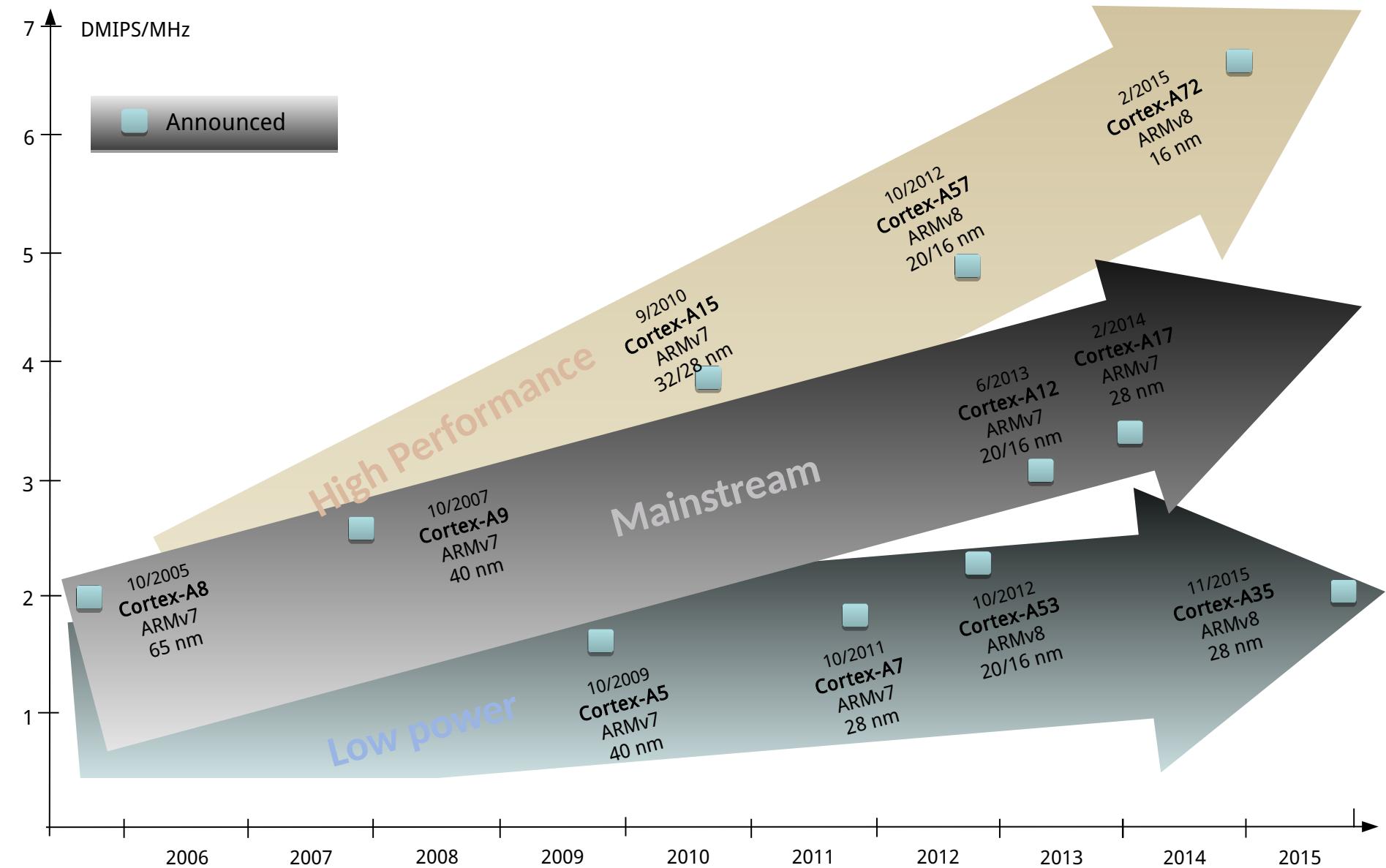
## 5. Overview of ARM's Cortex-A series (4)

### Performance classes of the Cortex-A series -1 [12]



## 5. Overview of ARM's Cortex-A series (5)

### Performance classes of the Cortex-A series -2 (based on [12])



## 5. Overview of ARM's Cortex-A series (6)

### Announcement dates and efficiency (DMIPS/MHz) of the Cortex-A models

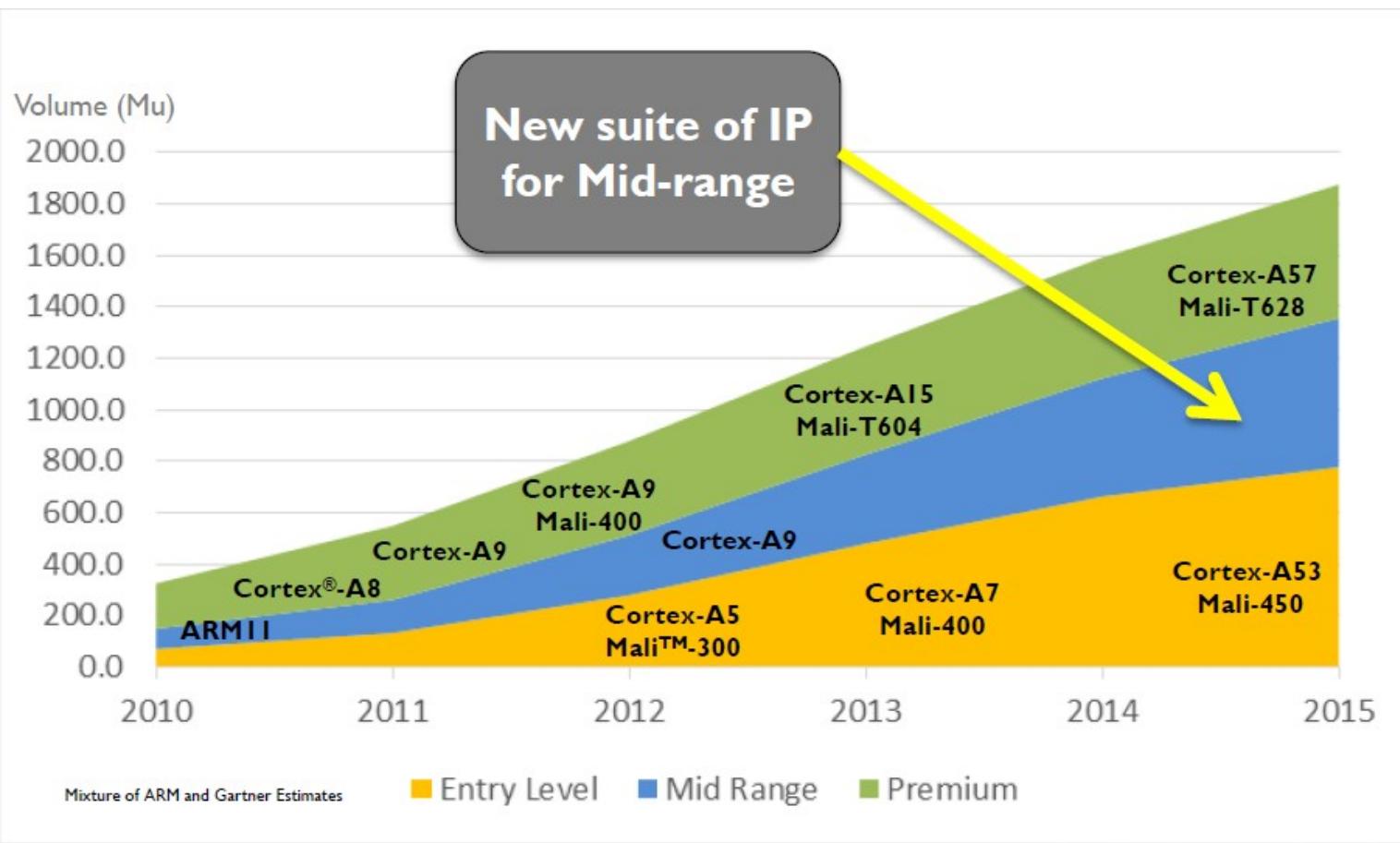
Announced	Cortex-A model	DMIPS/MHz
10/2005	Cortex-A8	2.0
10/2007	Cortex-A9/A9 MPCore	2.5
10/2009	Cortex-A5/A5 MPCore	1.6
9/2010	Cortex-A15/A15 MPCore	3.5-4.0
10/2011	Cortex-A7 MP Core	1.7
6/2013	Cortex-A12/A12 MPCore	3.0
2/2014	Cortex-A17/A17 MPCore	3.1-3.3
11/2015	Cortex-A35	~2.1
10/2012	Cortex-A53	2.3
10/2012	Cortex-A57	4.1-4.7
2/2015	Cortex-A72	6.3-7.35

Source: ARM

DMIPS: Dhrystone MIPS (A synthetic benchmark that indicates integer performance)

## 5. Overview of ARM's Cortex-A series (7)

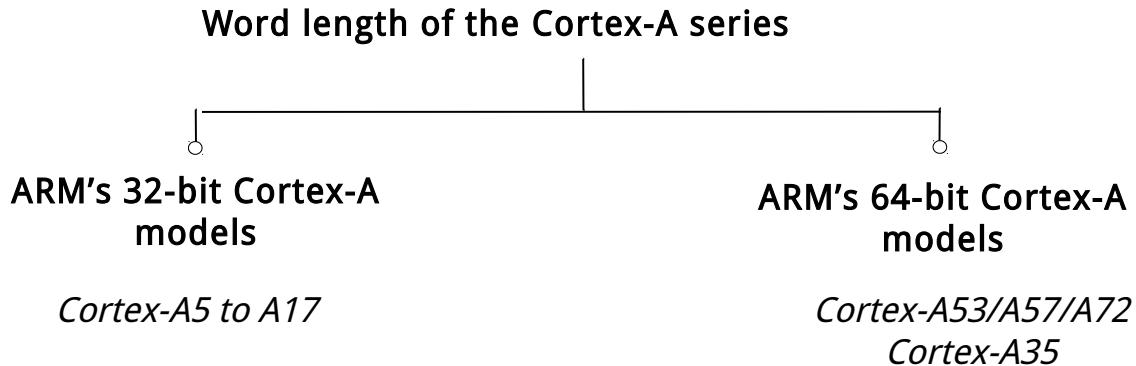
Yearly shipment of ARM Cortex-A chips in different performance classes  
(data from 2013) [13]



**Relative  
SoC Die  
Sizes**

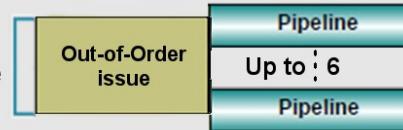
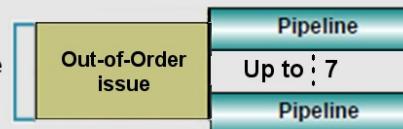
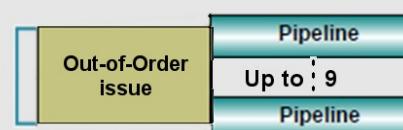
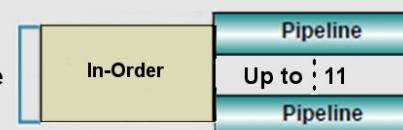
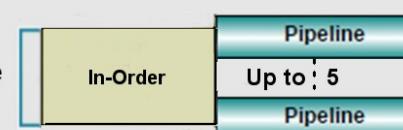
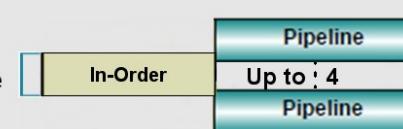
## 5. Overview of ARM's Cortex-A series (8)

# Word length of the Cortex-A series



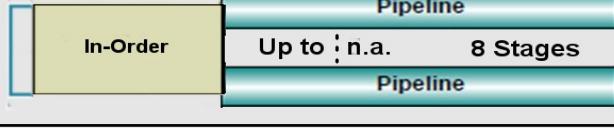
## 5. Overview of ARM's Cortex-A series (9)

### Key features of ARM's 32-bit microarchitectures -1 (based on [14])

2014 (Enhanced A12)	Cortex-A17	2-wide	2 decode		1-4 cores	3.1-3.3 DMIPS/MHz 2+ GHz 28nm
2010	Cortex-A15	2-wide	3 decode		1-4 cores	3.5-4.0 DMIPS/MHz 2+ GHz 32/28/22nm
2013	Cortex-A12	2-wide	2 decode		1-4 cores	3.0 DMIPS/MHz 2+ GHz 28nm
2007	Cortex-A9	2-wide	2 decode		1-4 cores	2.5 DMIPS/MHz 2+ GHz 45/40/32/28nm
2005	Cortex-A8	2-wide	2 decode		1 core	2 DMIPS/MHz 1 GHz 65/45nm
2011	Cortex-A7	2-wide	2 decode		1-4 cores	1.9 DMIPS/MHz 1.7 GHz 28nm
2009 (A9 replacement for low-end devices)	Cortex-A5	1-wide	1 decode		1-4 cores	1.6 DMIPS/MHz 1 GHz 28nm

## 5. Overview of ARM's Cortex-A series (10)

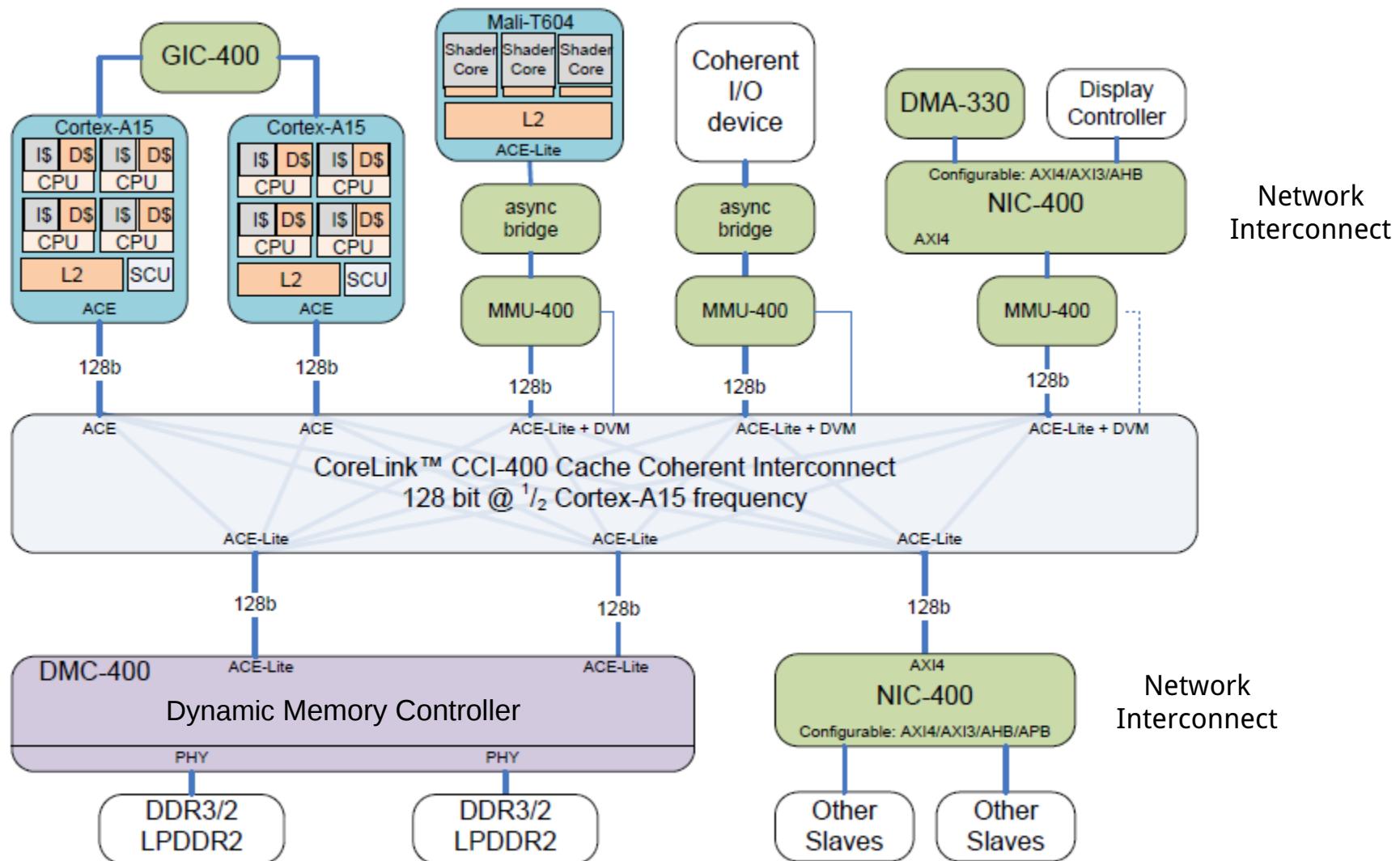
### Key features of ARM's 64-bit microarchitectures -2 (based on [14])

64-bit						
2013	Cortex-A57	3-wide	3 decode		1-4 cores	4.1-4.7 DMIPS/MHz 1.5-2.5 GHz 20/16 nm
2013	Cortex-A53	2-wide	2 decode		1-4 cores	2.3 DMIPS/MHz 1.2+ GHz 28/20 nm
2015	Cortex-A72	3-wide	3 decode		1-4 cores	6.3-7.35 DMIPS/MHz 2.5 GHz 16 nm
2015	Cortex-A35	2-wide	2 decode		1-4 cores	~2.1 DMIPS/MHz 1+ GHz 28/16/14 nm

Remark: In the Cortex-A9 the NEON FP operates in order.

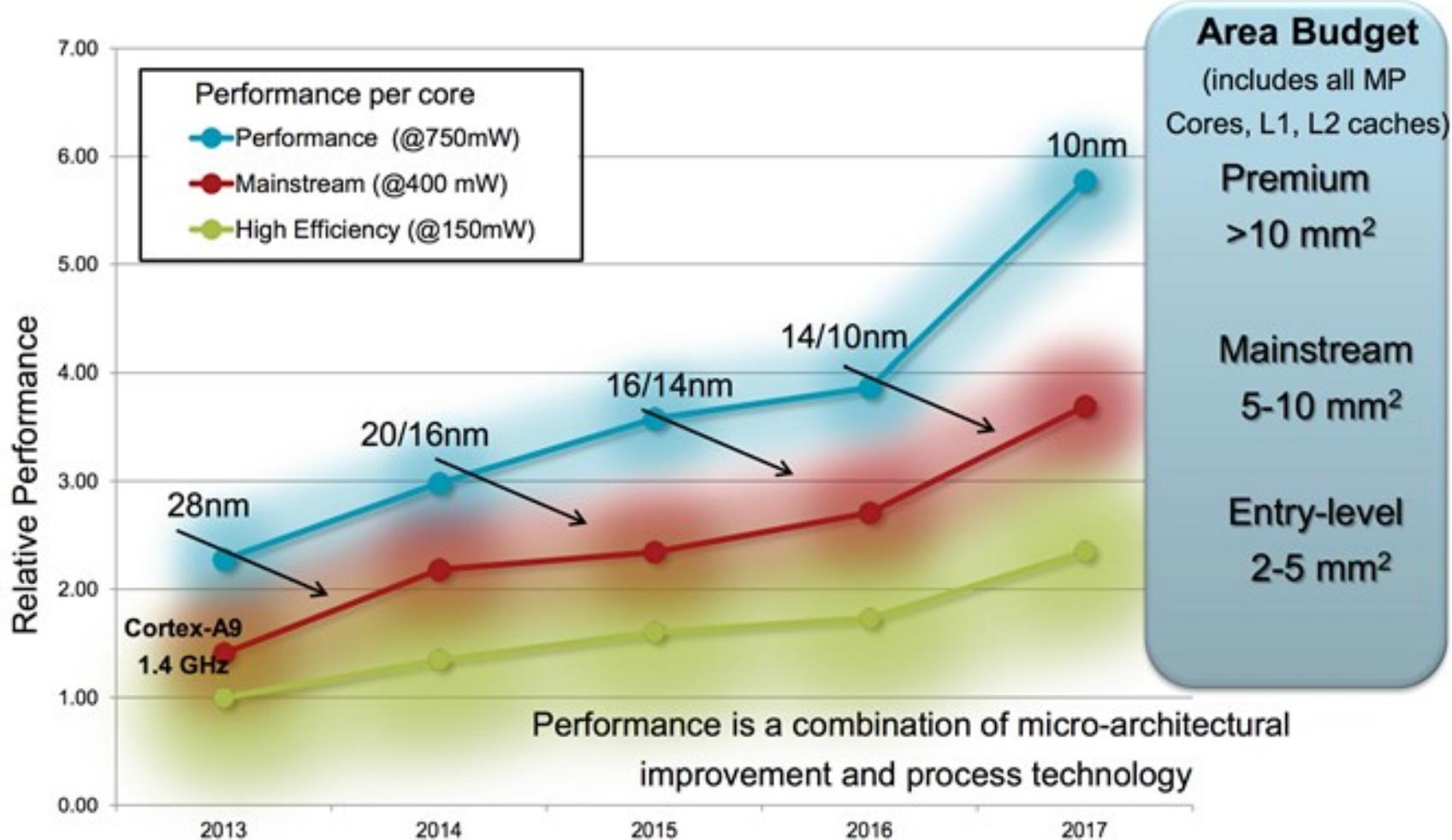
## 5. Overview of ARM's Cortex-A series (11)

Example: Dual-core A15-based high performance cache coherent system [15]



## 5. Overview of ARM's Cortex-A series (12)

Relative per core performance of Cortex-A processors with different power budget [16]



## 5. Overview of ARM's Cortex-A series (13)

Die area requirement of different applications [17]

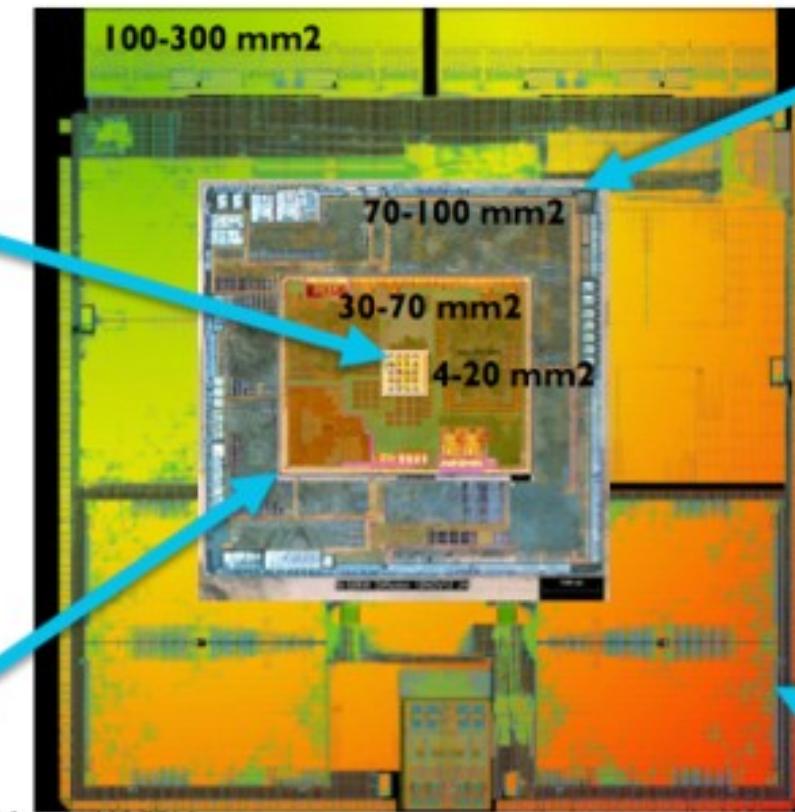
### Right SoC for the Required Task – Sensors to Servers



Sensors, IoT, wearables and  
real-time embedded



Mid-range mobile, consumer  
electronics and wearables



Premium mobile devices



Network infrastructure,  
storage and servers

**ARM**

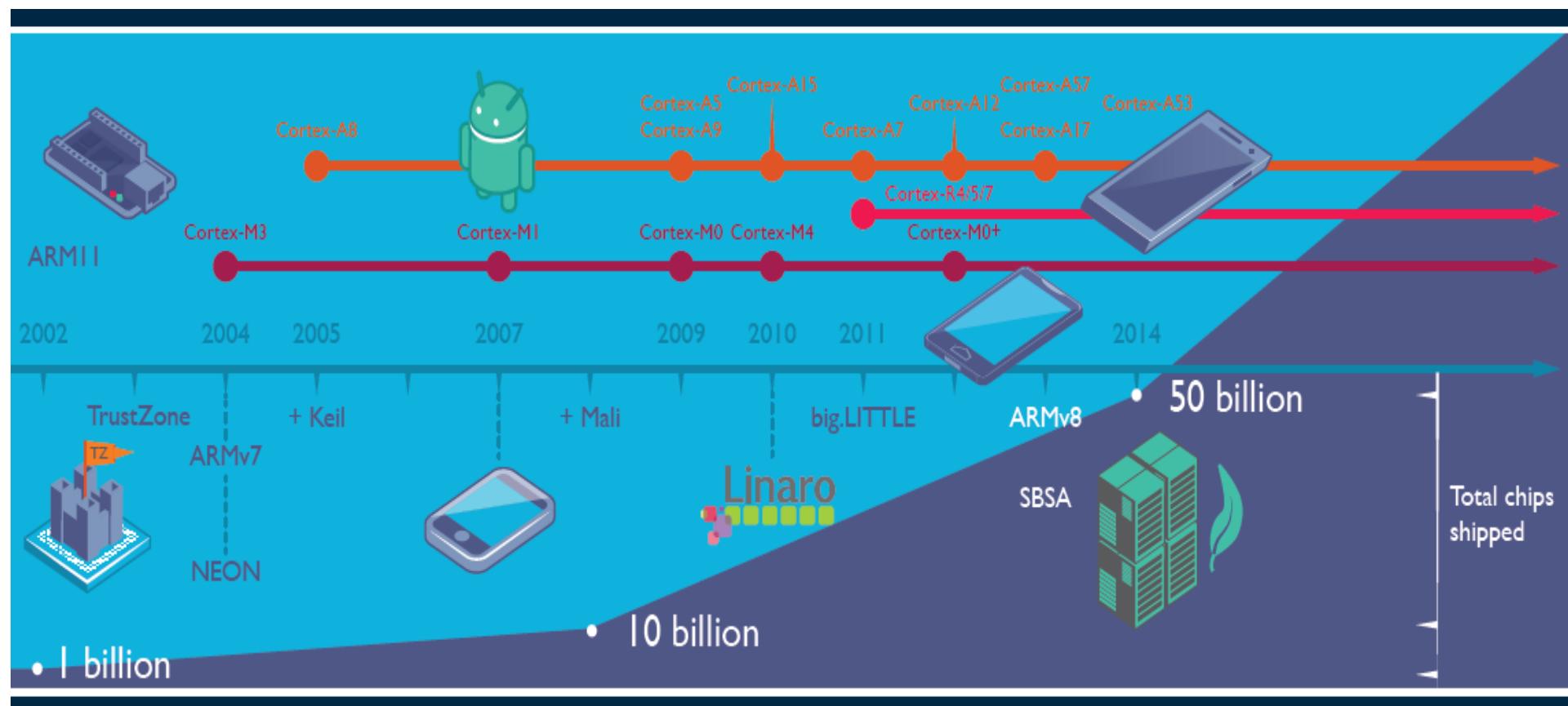
## 5. Overview of ARM's Cortex-A series (14)

### Use of 32-bit ARM Cortex-A models in mobiles [18]

		<ul style="list-style-type: none"> <li>• (SOC)</li> <li>• System-on-a-Chip</li> </ul>	<ul style="list-style-type: none"> <li>• Notable Product(s) Containing</li> </ul>	<ul style="list-style-type: none"> <li>• ARM Cortex-A model</li> </ul>	<ul style="list-style-type: none"> <li>• No. of Cores</li> </ul>
• Apple	• A4		<ul style="list-style-type: none"> <li>• iPhone 4, iPod Touch (4th Gen), iPad (1st Gen), AppleTV (2nd Gen)</li> </ul>	• Cortex-A8	• 1
	• A5		<ul style="list-style-type: none"> <li>• iPhone 4S, iPad 2, AppleTV (3rd Gen)</li> </ul>	• Cortex-A9	• 2
	• A5X		<ul style="list-style-type: none"> <li>• iPad (3rd Gen, Retina Display)</li> </ul>	• Cortex-A9	• 2
• Samsung	• Exynos 3 Single		<ul style="list-style-type: none"> <li>• Samsung Galaxy S, Samsung Galaxy Nexus S,</li> </ul>	• Cortex-A8	• 1
	• Exynos 4 Dual		<ul style="list-style-type: none"> <li>• Samsung Galaxy SII, Samsung Galaxy Note (International)</li> </ul>	• Cortex-A9	• 2
	• Exynos 4 Quad		<ul style="list-style-type: none"> <li>• Samsung Galaxy SIII</li> </ul>	• Cortex-A9	• 4
	• Exynos 5 Dual		<ul style="list-style-type: none"> <li>• Chrombook</li> </ul>	• Cortex-A15	• 2
• Nvidia	• Tegra		<ul style="list-style-type: none"> <li>• Microsoft Zune HD</li> </ul>	• (ARM11)	• 1
	• Tegra 2		<ul style="list-style-type: none"> <li>• ASUS Eee Pad Transformer, Samsung Galaxy Tab 10.1, Motorola Xoom, Dell Streak 7 &amp; Pro, Sony Tablet S</li> </ul>	• Cortex-A9	• 2
	• Tegra 3		<ul style="list-style-type: none"> <li>• ASUS Transformer Pad 300, ASUS Nexus 7, Acer Iconia Tab A510 &amp; A700, HTC One X</li> </ul>	• Cortex-A9	• 4
• Qualcomm	• Snapdragon S1		<ul style="list-style-type: none"> <li>• Large number of devices</li> </ul>	• (ARM11)/A5	• 1
• Texas Instruments	• OMAP 3		<ul style="list-style-type: none"> <li>• Barnes and Noble Nook Color</li> </ul>	• Cortex-A8	• 1
	• OMAP 4		<ul style="list-style-type: none"> <li>• Amazon Kindle Fire, Samsung Galaxy Tab 2, Blackberry Playbook, Samsung Galaxy Nexus, Barnes and Noble Nook Tablet</li> </ul>	• Cortex-A9	• 2
	• OMAP 5		<ul style="list-style-type: none"> <li>• N/A</li> </ul>	• Cortex-A15	• 2

## 5. Overview of ARM's Cortex-A series (15)

Total number of ARM chips shipped [19]



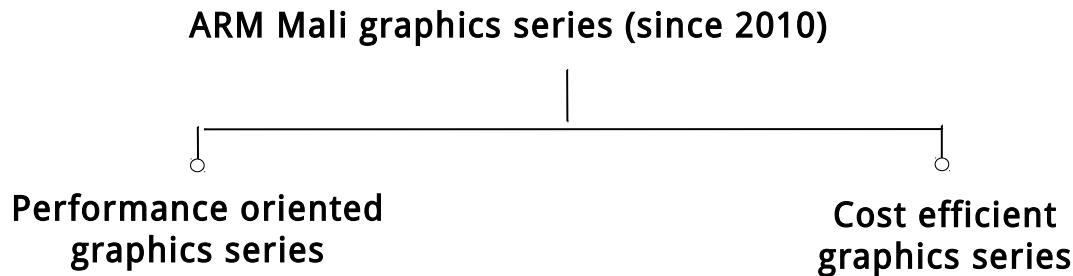
SBSA: Server Base System Architecture, it is a standardized platform for servers built on 64-bit ARM processors

## 6. Overview of ARM's Mali graphics series

## 6. Overview or ARM's Mali graphics series (1)

### 6. Overview of ARM's Mali graphics series (since 2010)

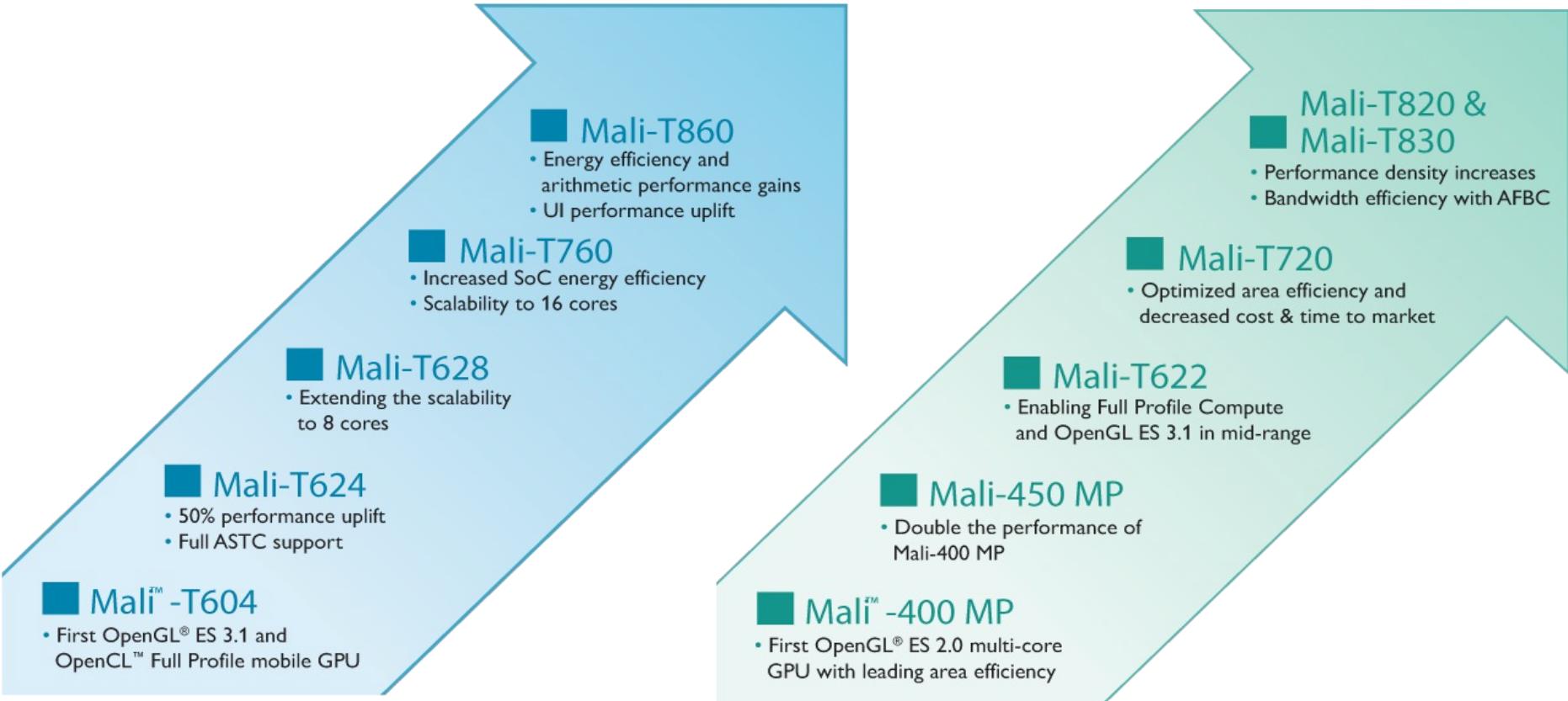
- ARM also designs and licenses **GPUs** to be used **as companion chips** to their **CPU chips**.
- ARM's GPU lines are designated as **Mali graphicd series**.



## 6. Overview of ARM's Mali graphics lines (2)

### Overview of ARM's Mali graphics series

Only GPU parts announced since about 2010 will be discussed [20]



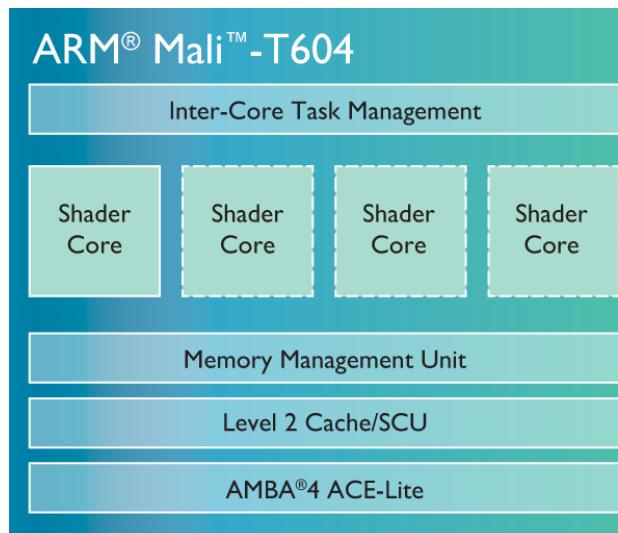
**Performance oriented  
graphics series**  
*Mali-T6xx - Mali-T8xx*

**Cost efficient  
graphics series**  
*Mali-T4xx - Mali-T8xx*

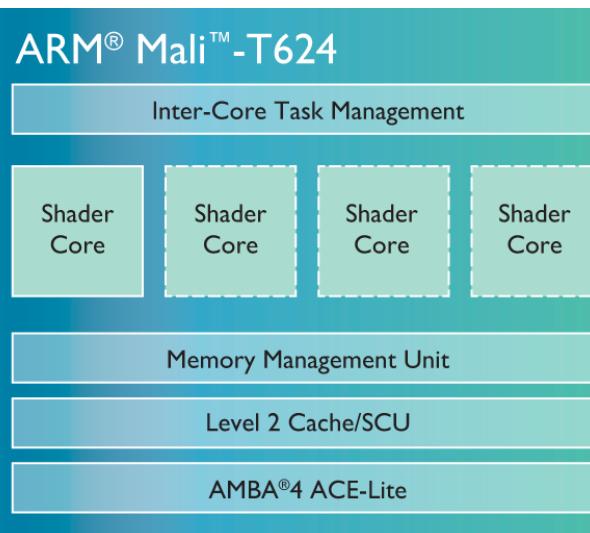
## 6. Overview of ARM's Mali graphics lines (3)

### ARM's performance oriented Mali graphics series [20]

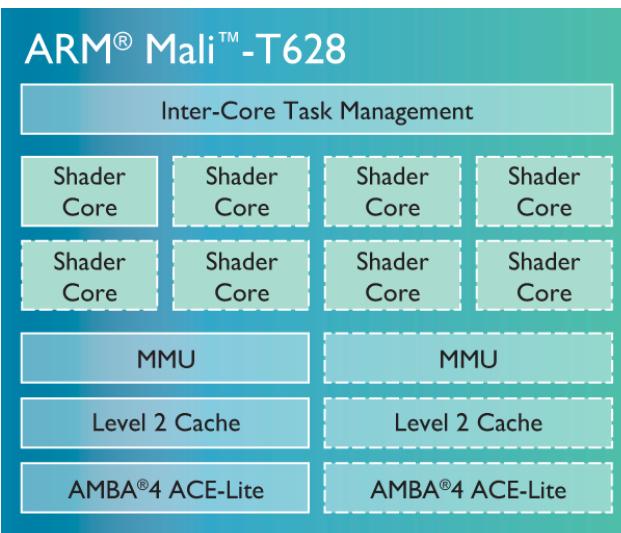
ARM® Mali™-T604



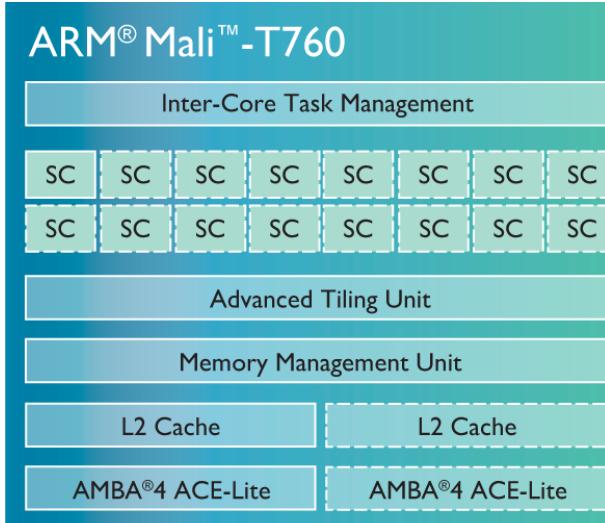
ARM® Mali™-T624



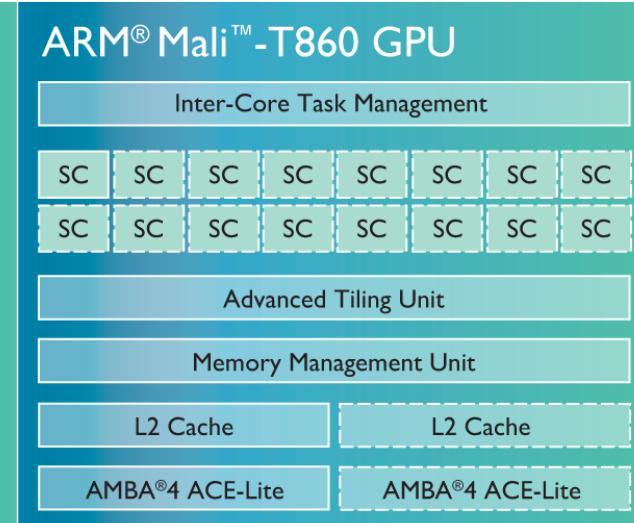
ARM® Mali™-T628



ARM® Mali™-T760



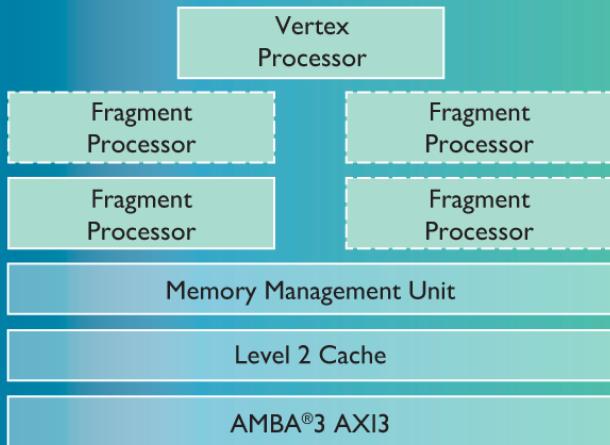
ARM® Mali™-T860 GPU



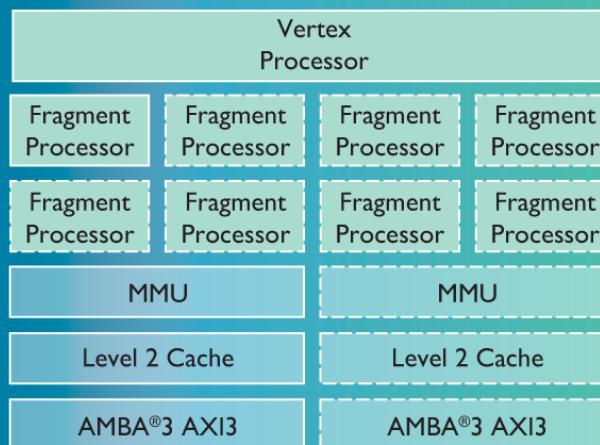
## 6. Overview of ARM's Mali graphics lines (4)

### ARM's cost efficient Mali graphics series [20]

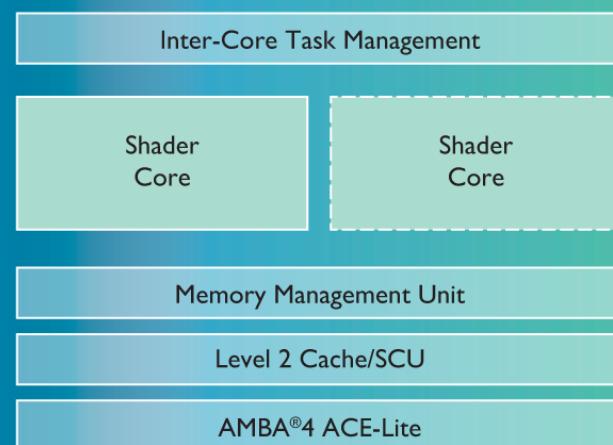
ARM® Mali™ -400



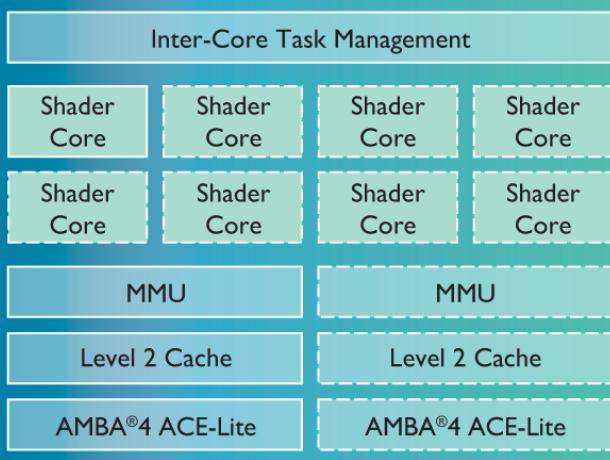
ARM® Mali™ -450 MP



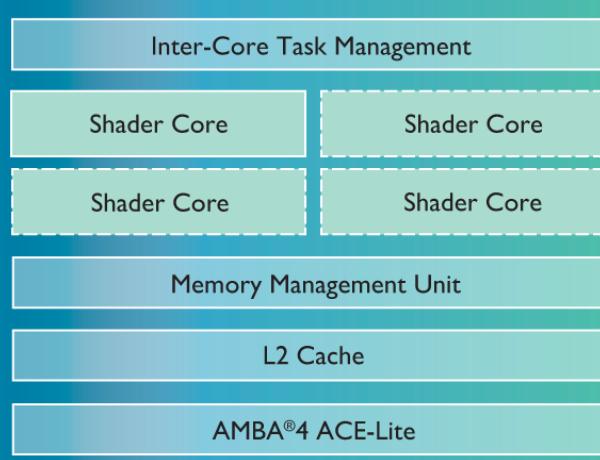
ARM® Mali™ -T622



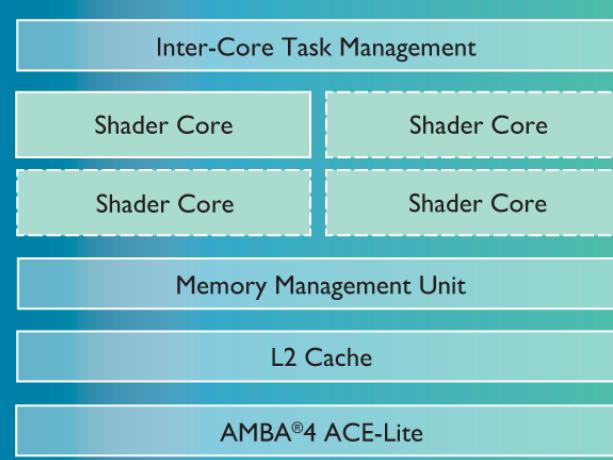
ARM® Mali™ -T720



ARM® Mali™ -T820 GPU

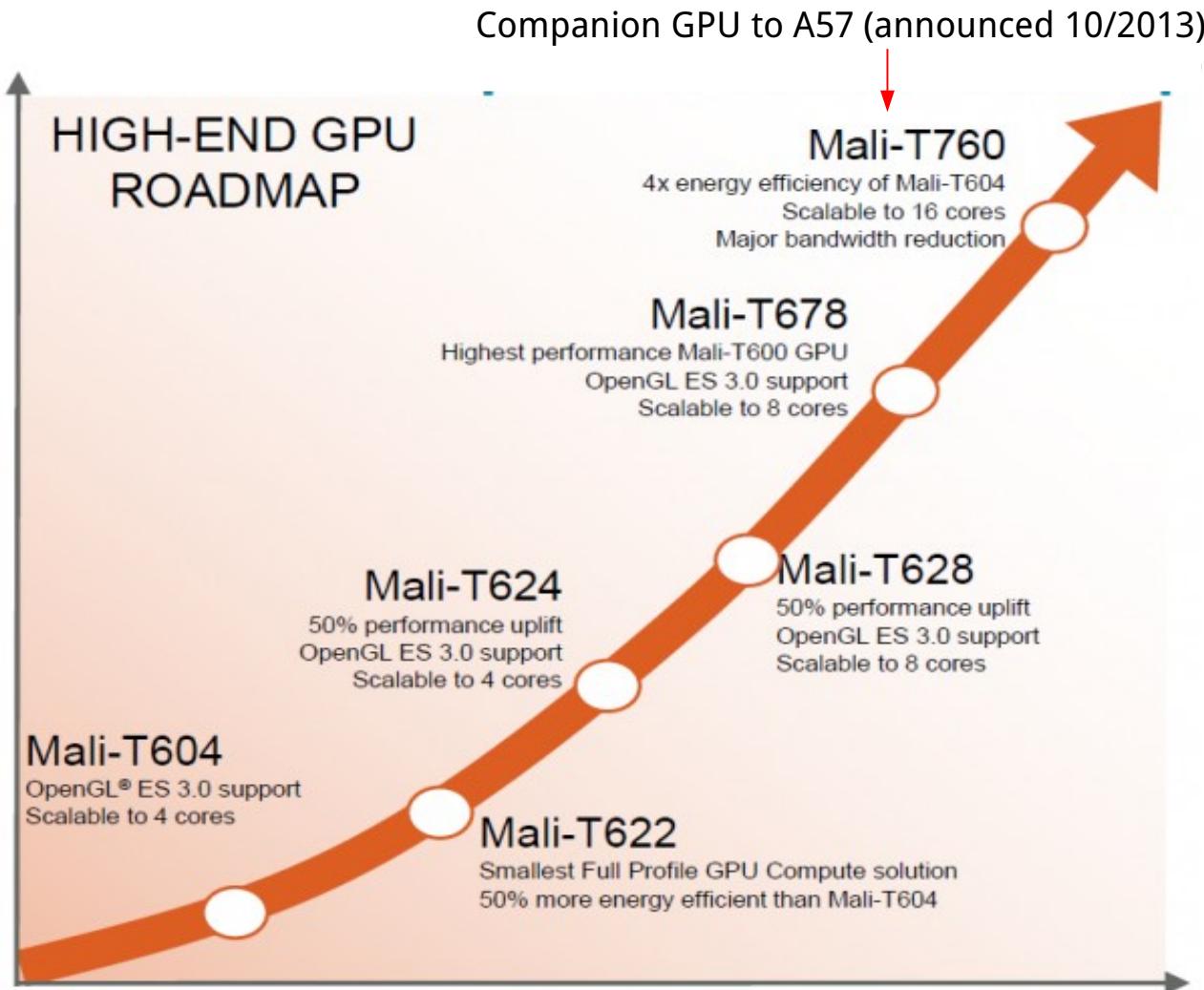


ARM® Mali™ -T830 GPU



## 6. Overview of ARM's Mali graphics lines (5)

### ARM's high-end GPU roadmap [51]



## 7. The 64-bit Cortex-A series

- 7.1 Overview of ARM's 64-bit Cortex-A series
- 7.2 The 64-bit high performance Cortex-A57
- 7.3 The 64-bit low power Cortex-A53
- 7.4 The 64-bit low power Cortex-A35
- 7.5 The 64-bit high performance Cortex-A72

## 7.1 Overview of ARM's 64-bit Cortex-A series

## 7.1 Overview of ARM's 64-bit Cortex-A series (1)

### 7.1 Overview of ARM's 64-bit Cortex-A series -1 [64]

10/2011 ARM disclosed the **64-bit ARMv8** architecture  
with enhancements as indicated in the Figure below  
and discussed in Section 2.

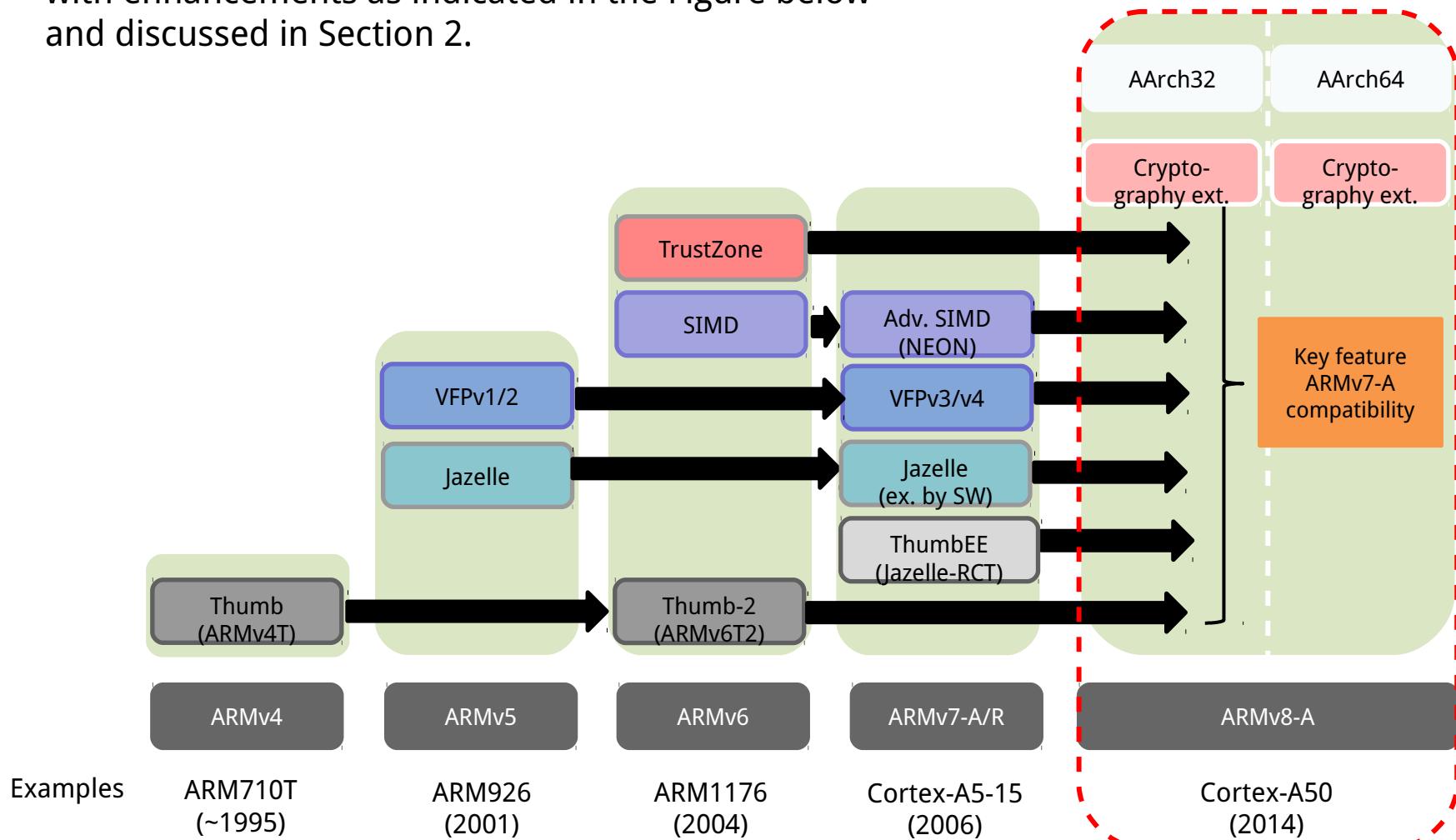
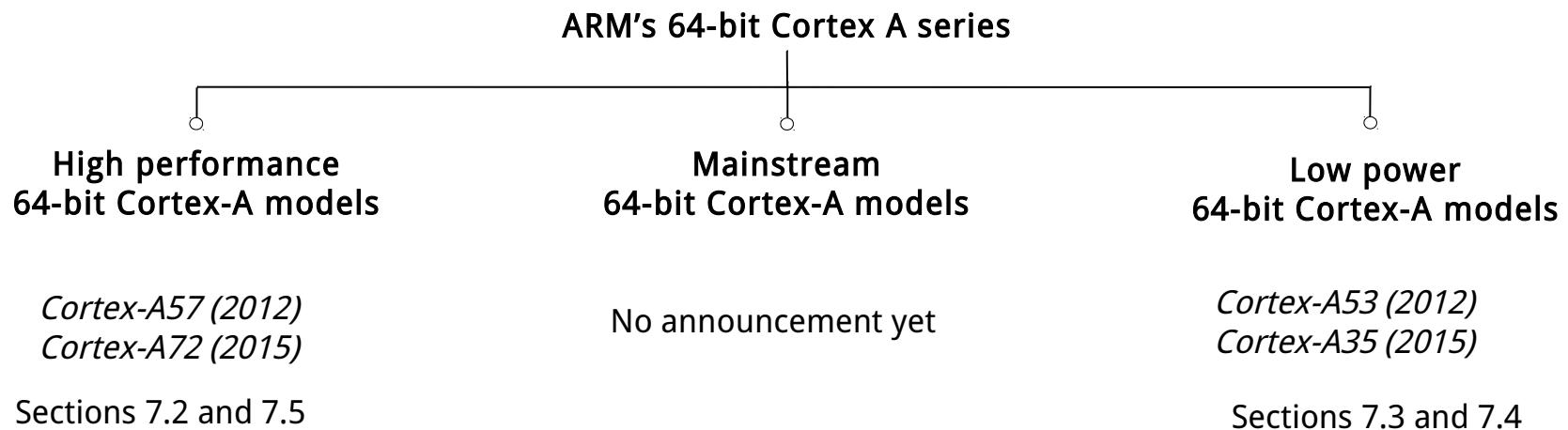


Figure: Enhancements of the ARM architecture (based on [64])

## 7.1 Overview of ARM's 64-bit Cortex-A series (2)

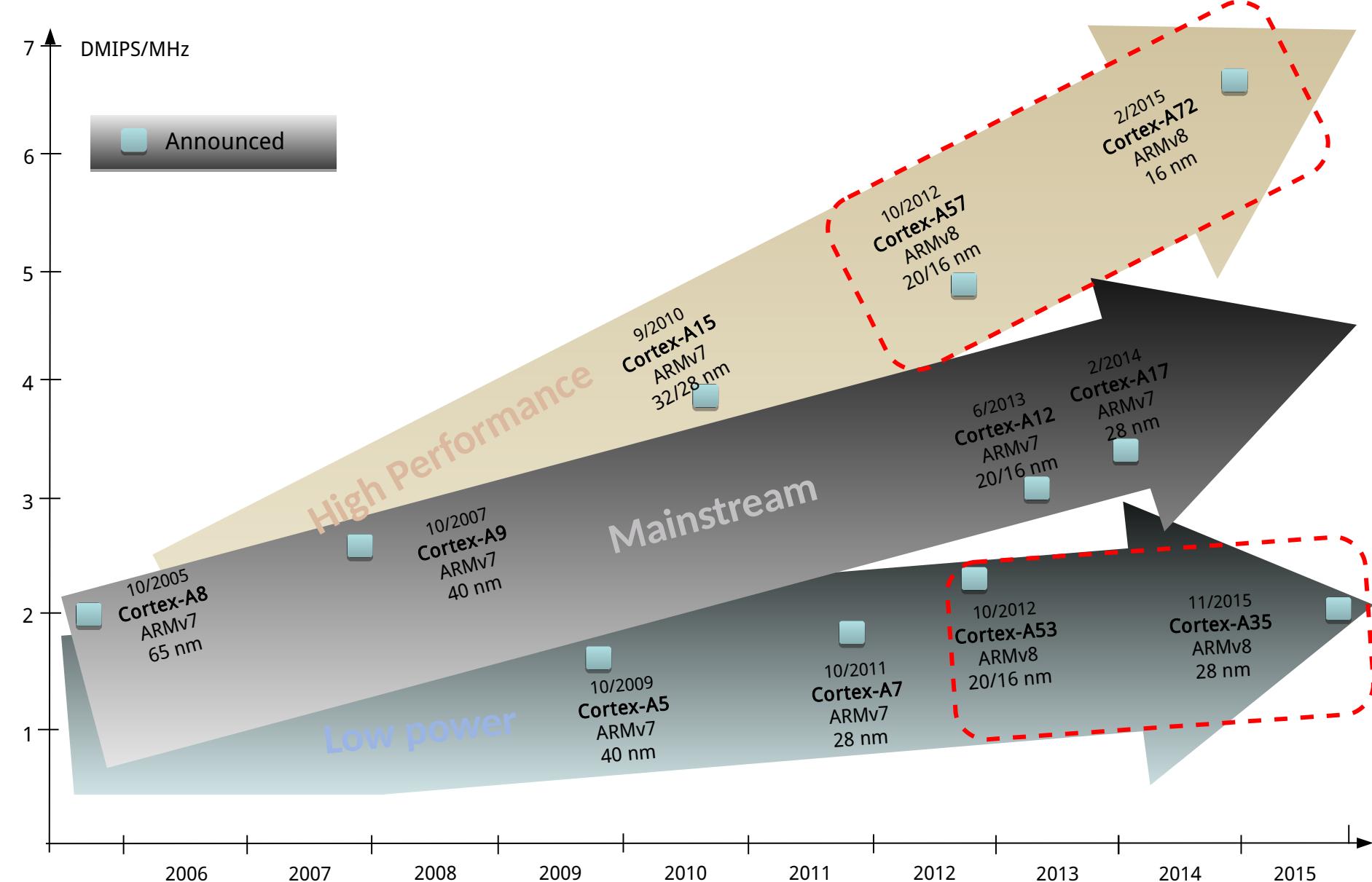
### Overview of ARM's 64-bit Cortex-A series -2

- 10/2012: ARM announced the 64-bit **high performance Cortex-A-57** and the **low power Cortex-A-53** processors, as first implementations of the ARMv8 architecture, with immediate availability.
- 02/2015 ARM extended their 64-bit Cortex-A series by the **high performance Cortex-A72** model, as shown below.



## 5. Overview of ARM's Cortex-A series (6)

Overview or ARM's 64-bit Cortex-A series -3 (based on [12])



## 7.1 Overview of ARM's 64-bit Cortex-A series (4)

The 64-bit Cortex-A series as the basis for scalable applications [48]



## 7.1 Overview of ARM's 64-bit Cortex-A series (5)

### Target markets of the 64-bit Cortex-A series [49]

#### Entry-level Computing

Extend OS capabilities to sub-\$100 devices



#### 'Desktop Class' Computing

Performance apps  
Enhanced multimedia processing



#### High-end Enterprise

64-bit memory addressing  
Virtualisation  
High bandwidth  
Enable innovation for hyperscale operators



## 7.1 Overview of ARM's 64-bit Cortex-A series (6)

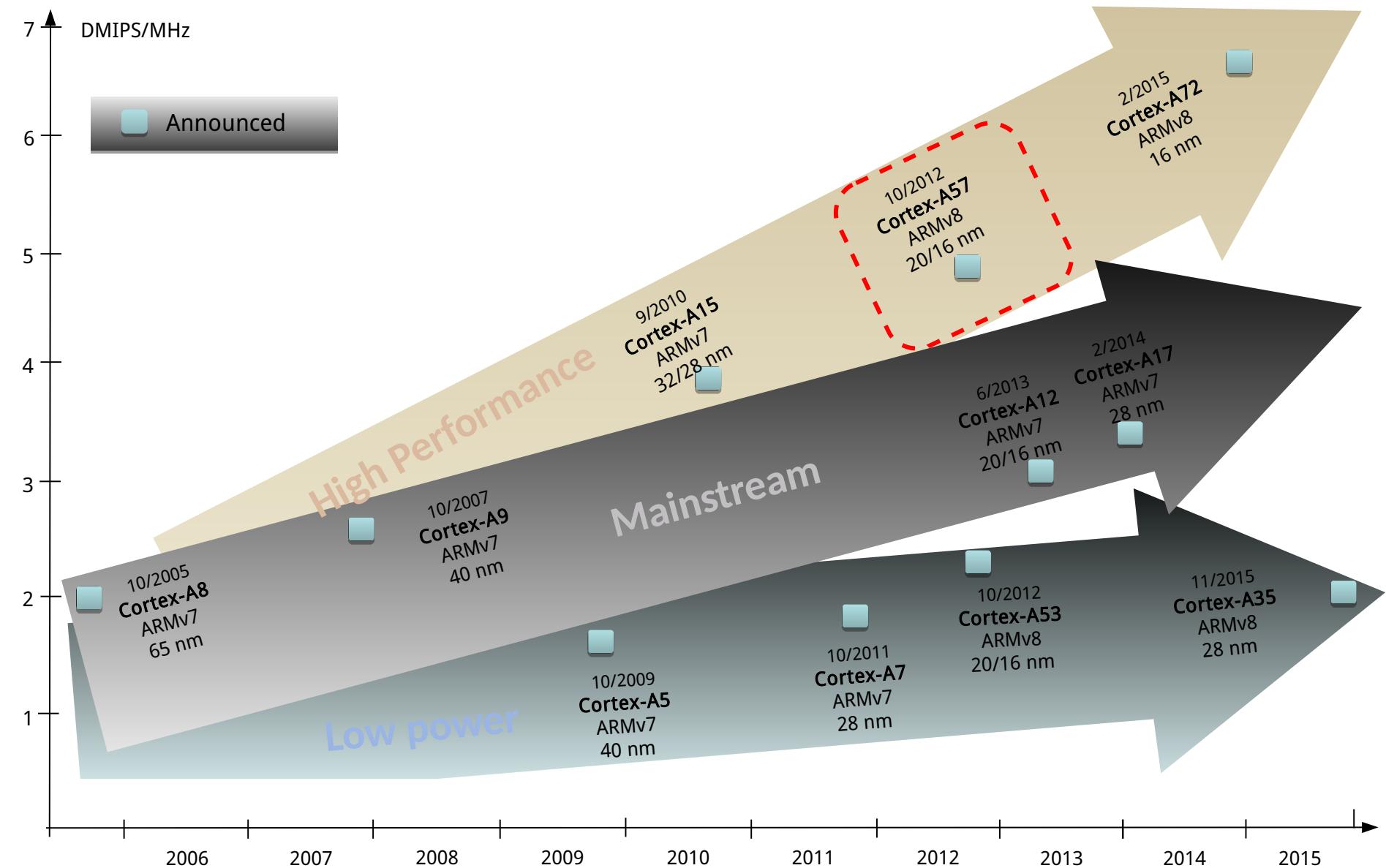
### Main features of ARM's 64-bit Cortex-A series [51]

• CPU Core	• Architecture	• Efficiency	• big.LITTLE	• Announced	• Available in devices	• Target
• <b>Cortex-A72</b>	• ARMv8 (64-bit)	• 6,3-7,3 DMIPS/MHz	• Yes • (with A53/A35)	• 2015	• n.a.	• High-end
• <b>Cortex-A57</b>	• ARMv8 (64-bit)	• 4,8 DMIPS/MHz	• Yes • (with A53)	• 2012	• 2015	• High-end
• <b>Cortex-A53</b>	• ARMv8 (64-bit)	• 2,3 DMIPS/MHz	• Yes (with A57)	• 2012	• 2H 2014	• Low power
• <b>Cortex-A35</b>	• ARMv8 (64-bit)	• 2,1 DMIPS/MHz	• Yes • (with A57/A72)	• 2015	• 2H 2016	• Low power
• <b>Cortex-A17</b>	• ARMv7 (32-bit)	• 4,0 DMIPS/MHz	• Yes (with A7)	• 2014	• 2015	• Mainstream
• <b>Cortex-A15</b>	• ARMv7 (32-bit)	• 4,0 DMIPS/MHz	• Yes (with A7)	• 2010	• Now	• High-end
• <b>Cortex-A12</b>	• ARMv7 (32-bit)	• 3,0 DMIPS/MHz	• -	• 2013	• 2H 2015	• Mainstream
• <b>Cortex-A9</b>	• ARMv7 (32-bit)	• 2,5 DMIPS/MHz	• -	• 2007	• Now (EOL)	• High-end
• <b>Cortex-A8</b>	• ARMv7 (32-bit)	• 2,0 DMIPS/MHz	• -	• 2005	• Now (EOL)	• High-end
• <b>Cortex-A7</b>	• ARMv7 (32-bit)	• 1,9 DMIPS/MHz	• Yes (A15/A17)	• 2011	• Now	• Low power
• <b>Cortex-A5</b>	• ARMv7 (32-bit)	• 1,6 DMIPS/MHz	• -	• 2009	• Now	• Low power

## 7.2 The 64-bit high performance Cortex-A57

## 5. Overview of ARM's Cortex-A series (6)

### 7.2 The 64-bit high performance Cortex-A57 -1 (based on [12])



## 7.2 The 64-bit high performance Cortex-A57 (2)

### The 64-bit high performance Cortex-A57 -2 [12]

- 10/2012: Announced along with the low power Cortex-A53 processor, with immediate availability for licensing.
- 2014: First mobile devices with Cortex-A57 models are emerged.
- They are 64-bit successors to the high performance 32-bit Cortex A15.
- The A57 and A53 models can be used either as stand alone processors or as components of a big-LITTLE configuration, similar to the 32-bit Cortex-A15/A7 combination.
- Interoperability with the ARM Mali GPU family is provided.
- Target process technology: 16 or 20 nm.

## 7.2 The 64-bit high performance Cortex-A57 (3)

### Key features of the Cortex-A57

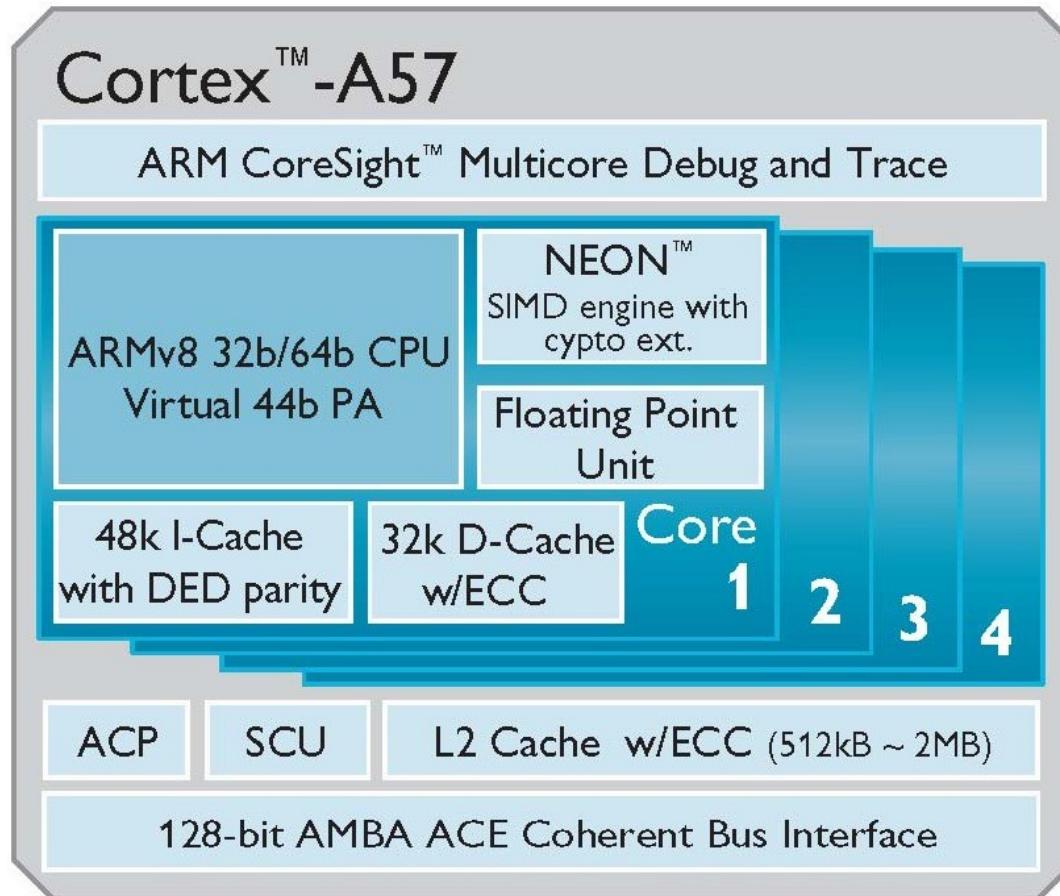
- Fully compatible with the preceding ARMv7 32-bit ISA.
- Integrated L2 cache of 512 kB to 2 MB.
- Up to 4 Cortex-A57 CPUs that execute the ARMv8 64-bit ISA.
- 128-bit AMBA coherent interface for connecting multiple (up to 4) Cortex-A57 processors.
- System wide cache coherence supported by a Snoop Control Unit (SCU).

### Remarks

AMBA: Advanced Microcontroller Bus Architecture  
(On-chip bus standard for SoC) designs

## 7.2 The 64-bit high performance Cortex-A57 (4)

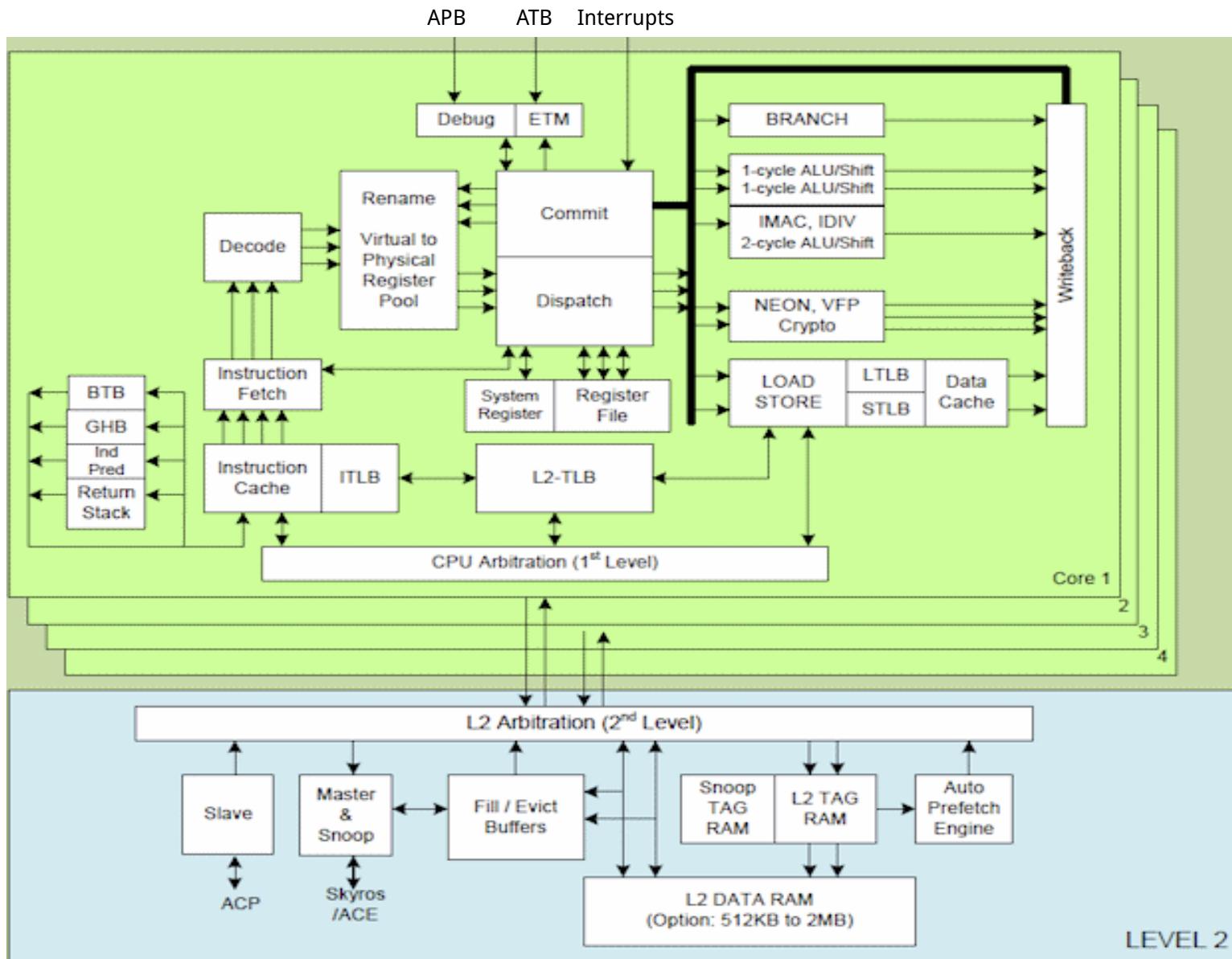
### High level block diagram of the Cortex-A57 [53]



- PA: Physical Address
- DED: Double Error Detection
- ECC: Error Correcting Code
- ACP: Accelerator Coherence Port  
(to connect non-cached coherent data sources)
- SCU: Snoop Control Unit
- AMBA: Advanced Microcontroller Bus Architecture  
(On-chip bus standard for SoC designs)
- ACE: AXI Coherency Extensions  
(Used in big.LITTLE systems for smartphones, tablets, etc.)
- AXI: Advanced eXtensible Interface  
(The most widespread AMBA interface).

## 7.2 The 64-bit high performance Cortex-A57 (5)

### Main functional blocks of the 64-bit high performance Cortex-A57 CPU [74]



## 7.2 The 64-bit high performance Cortex-A57 (6)

Remarks: Non trivial abbreviations in the above Figure

ATB: AMBA Trace Bus

APB: Advanced Peripheral Bus

ACP: Accelerator Coherence Port

(to connect non-cached coherent data sources)

ACE: AXI Coherency Extensions

(Used in big.LITTLE systems for smartphones, tablets, etc.)

AXI: Advanced eXtensible Interface

(The most widespread AMBA interface).

## 7.2 The 64-bit high performance Cortex-A57 (7)

### Key features of the microarchitecture of the Cortex-A57 core -1

- Each core **fetches four instructions** per cycle from the Icache,
- **decodes and renames three microinstructions** per cycle,
- **dispatches three microinstructions** per cycle to the issue queues,
- whereas the issue queues **issue up to eight microinstructions** per cycle to the eight available execution units.

### The available execution units are

- a branch unit
- dual single cycle integer units
- a multi-cycle integer MAC/DIV/CRC unit
- dual Advanced SIMD (NEON)/FP. Crypto units and
- dual load/store units.

## 7.2 The 64-bit high performance Cortex-A57 (8)

### Key features of the microarchitecture of the Cortex-A57 core -2

- Core efficiency: **4.8 DMIPS/MHz**
- Expected core frequency **up to 2.5 GHz** in a **16 nm** process implementation.

## 7.2 The 64-bit high performance Cortex-A57 (9)

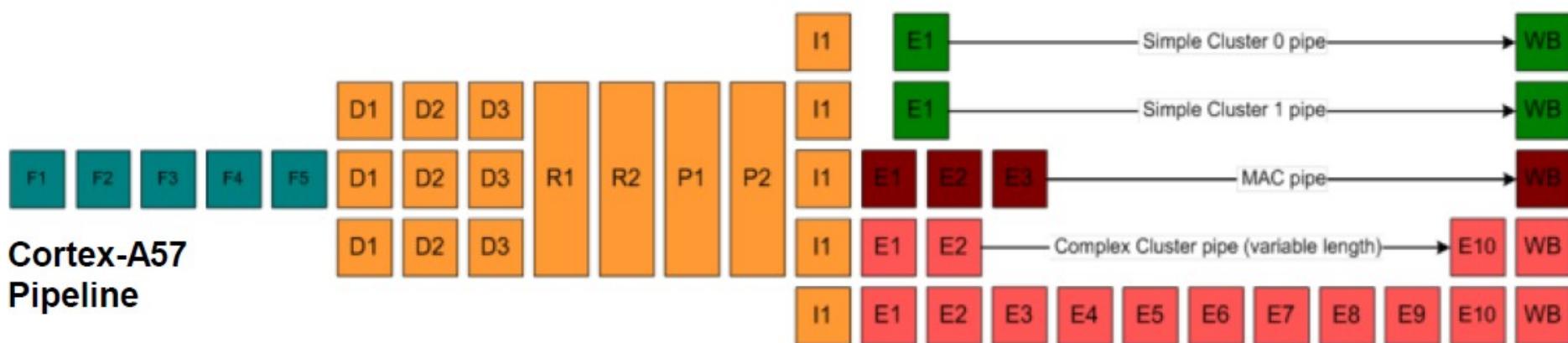
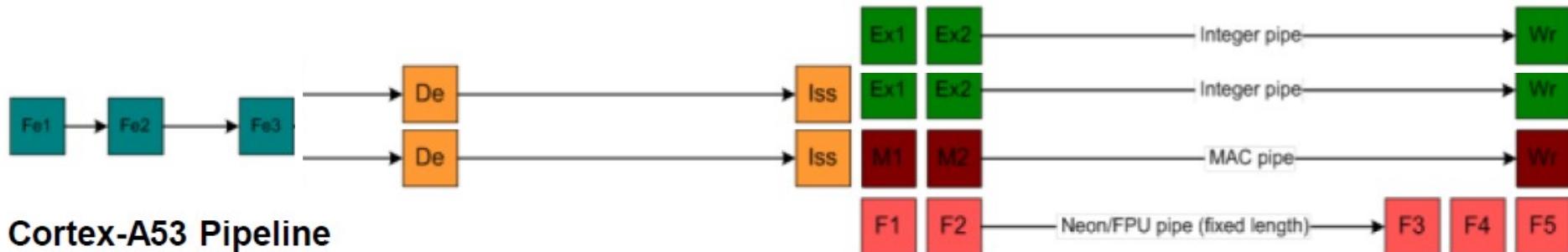
### Pipeline of the Cortex-A57 core -1

- The Cortex-A57 core has a 3-wide in-order front end and an 8 issue-wide out-of-order back end pipeline with 15 stages for integer processing and additional pipeline stages for NEON and FP processing, as indicated in the next two Figures.

## 7.2 The 64-bit high performance Cortex-A57 (10)

Contrasting the Cortex-A53 and Cortex-A57 arithmetic pipelines

[Based on 54]



D: Decode

R: Rename

P: Dispatch

I: Issue

E: Execute

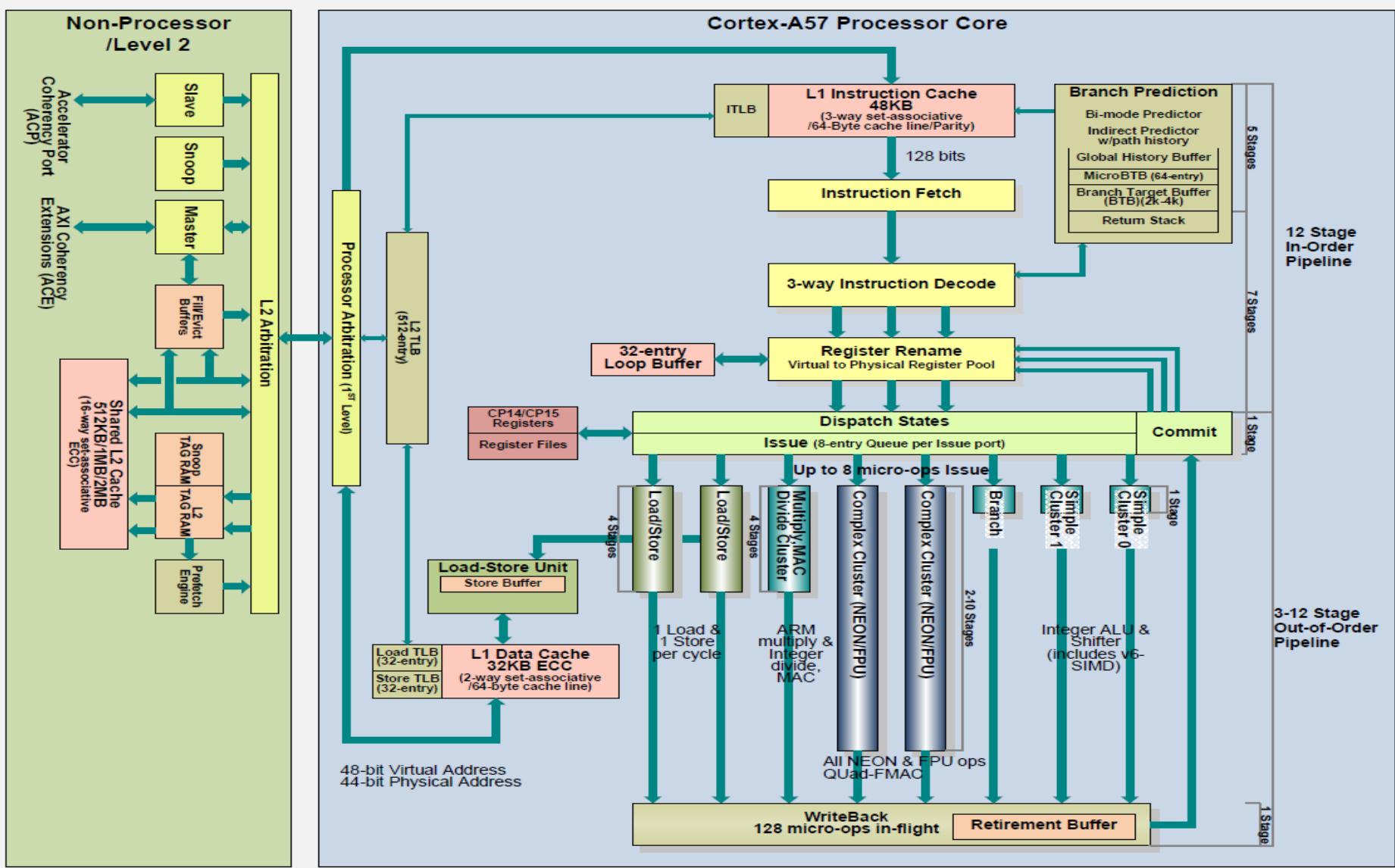
WB: Write Back

Note: Branch and Load/Store pipelines not shown

(1x Load/Store pipeline for the Cortex A-53 and  
2x Load/Store and 1x Branch pipeline for the Cortex-A-57)

## 7.2 The 64-bit high performance Cortex-A57 (11)

### Pipeline structure of the Cortex-A57 core (alternative view) [71]



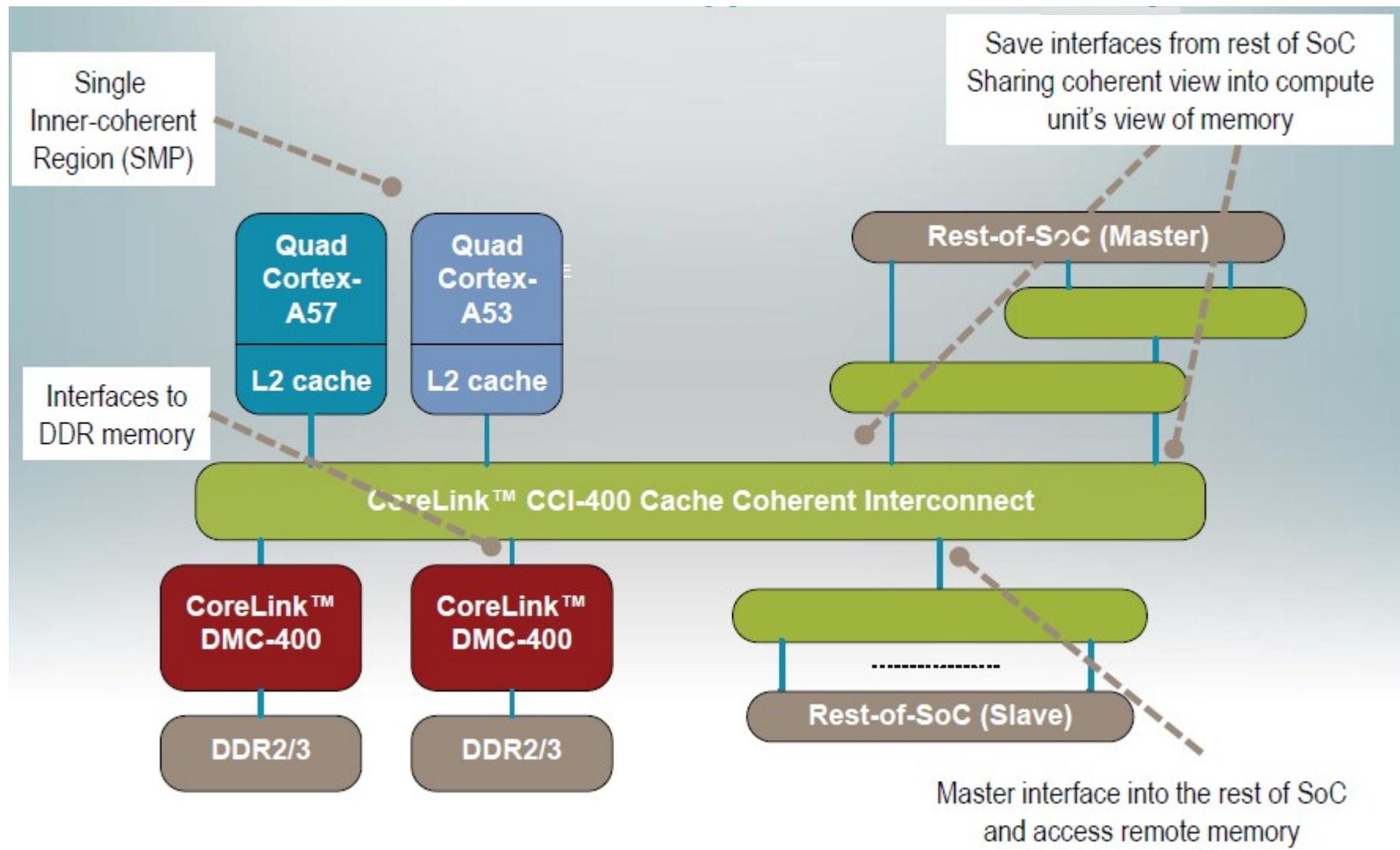
## 7.2 The 64-bit high performance Cortex-A57 (12)

Cortex-A57/A53 performance - compared to the Cortex-A15 [55]



## 7.2 The 64-bit high performance Cortex-A57 (13)

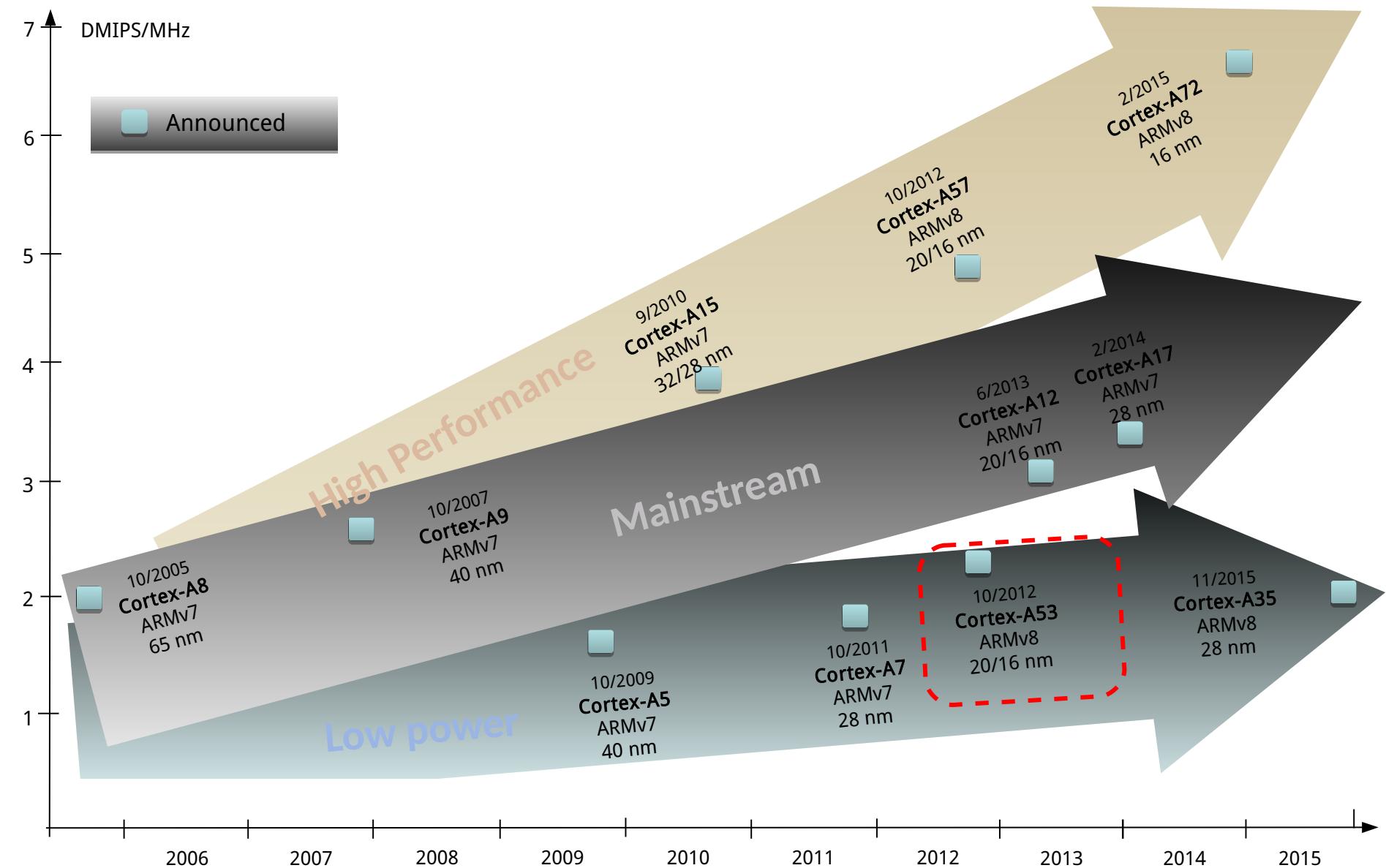
Example: A Cortex-A57/Cortex-A53 big.LITTLE system [52]



## 7.3 The 64-bit low power Cortex-A53

## 5. Overview of ARM's Cortex-A series (6)

### 7.3 The 64-bit low power Cortex-A53 - 1 (based on [12])



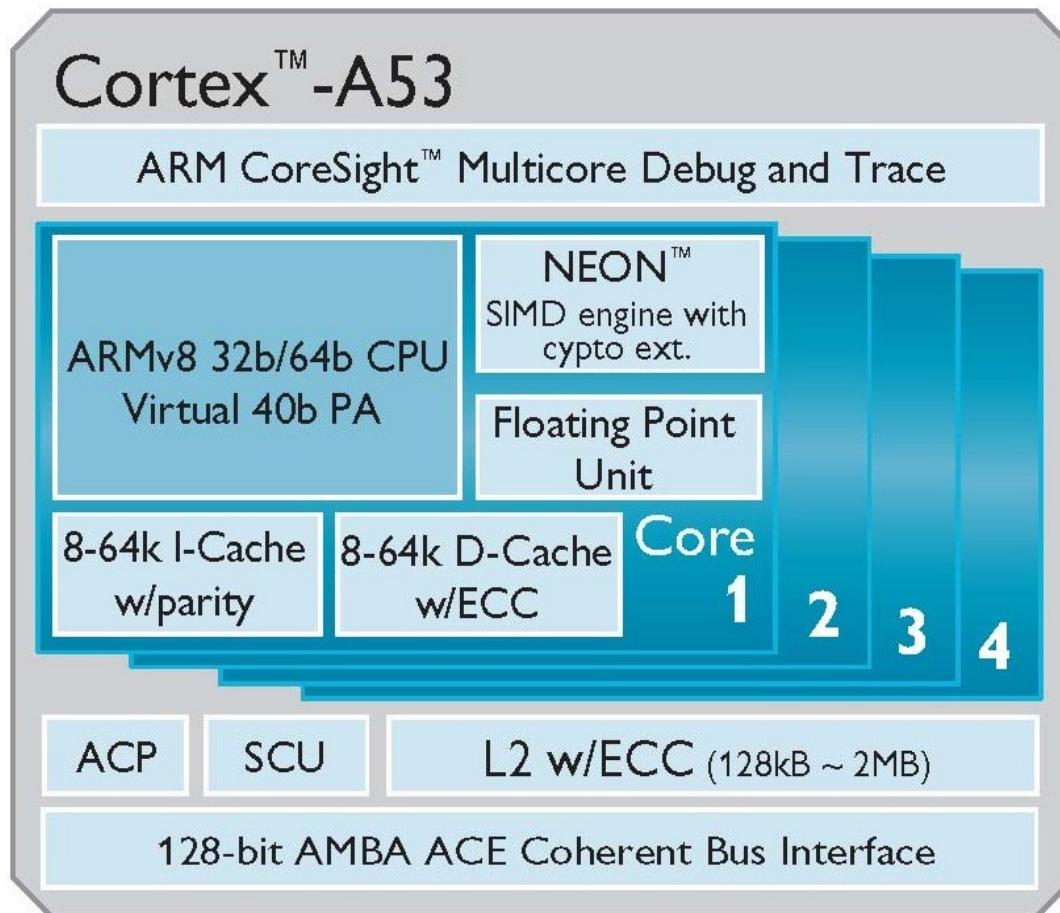
## 7.3 The 64-bit low power Cortex-A53 (2)

### The 64-bit low power Cortex-A53 -2 [12]

- 10/2012: Announced along with the performance oriented Cortex-A57 processor, with immediate availability for licensing.
- 2014: First mobile devices with the Cortex-A53.
- It is the 64-bit successor to the Cortex-A7.
- The A57 and A53 models can be used either as stand alone processors or as components in a big-LITTLE configuration, similar to the 32-bit Cortex-A15 and A7 models.
- Target process technology: 16 or 20 nm.

## 7.3 The 64-bit low power Cortex-A53 (3)

### High level block diagram of the Cortex-A53 [53]



- PA: Physical Address
- DED: Double Error Detection
- ECC: Error Correcting Code
- ACP: Accelerator Coherence Port  
(to connect non-cached coherent data sources)
- SCU: Snoop Control Unit
- AMBA: Advanced Microcontroller Bus Architecture  
(On-chip bus standard for SoC designs)
- ACE: AXI Coherency Extensions  
(Used in big.LITTLE systems for smartphones, tablets, etc.)
- AXI: Advanced eXtensible Interface  
(The most widespread AMBA interface).

## 7.3 The 64-bit low power Cortex-A53 (4)

### Key features of the microarchitecture of the Cortex-A53 core -1

- Fully compatible with the preceding ARMv7 32-bit ISA.
- Integrated L2 cache of 128 kB to 2 MB.
- Up to 4 Cortex-A53 CPU cores that execute the ARMv8 64-bit ISA.
- 128-bit AMBA coherent interface for connecting multiple (up to 4) Cortex-A53 processors.
- System wide cache coherence supported by a Snoop Control Unit (SCU).

### Remarks

AMBA: Advanced Microcontroller Bus Architecture  
(On-chip bus standard for SoC) designs

## 7.3 The 64-bit low power Cortex-A53 (5)

### Key features of the microarchitecture of the Cortex-A53 core -2

- The Cortex-A53 core has a dual-issue in-order front end with 5 pipelines constituting the back end, as indicated in the next Figure.

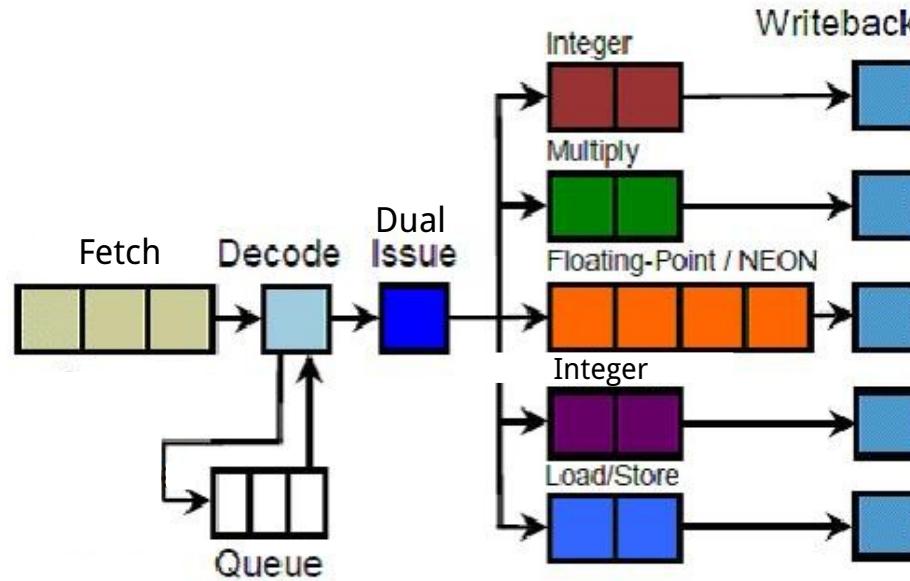


Figure: Pipeline stages of the Cortex-A53 [76]

- The pipeline for integer processing has 8 pipeline stages, NEON and FP processing has two additional pipeline stages, as seen in the Figure above.

## 7.3 The 64-bit low power Cortex-A53 (6)

### Contrasting the Cortex-A7 and Cortex-A53 microarchitectures [75]

• ARM CPU Core Comparison		
• ARM ISA	• Cortex-A7	• Cortex-A53
• Issue Width	• ARMv7 (32-bit)	• ARMv8 (32/64-bit)
• Pipeline Length	• Partially 2 micro-ops	• 2 micro-ops
• Integer Add	• 8	• 8
• Integer Mul	• 2	• 2
• Load/Store Units	• 1	• 1
• Branch Units	• 1	• 1
• FP/NEON ALUs	• 1x64-bit	• 1x64-bit
• L1 Cache	• 8KB-64KB I\$ + 8KB-64KB D\$	• 8KB-64KB I\$ + 8KB-64KB D\$
• L2 Cache	• 128KB - 1MB (Optional)	• 128KB - 2MB (Optional)

## 7.3 The 64-bit low power Cortex-A53 (7)

### Remarks [75]

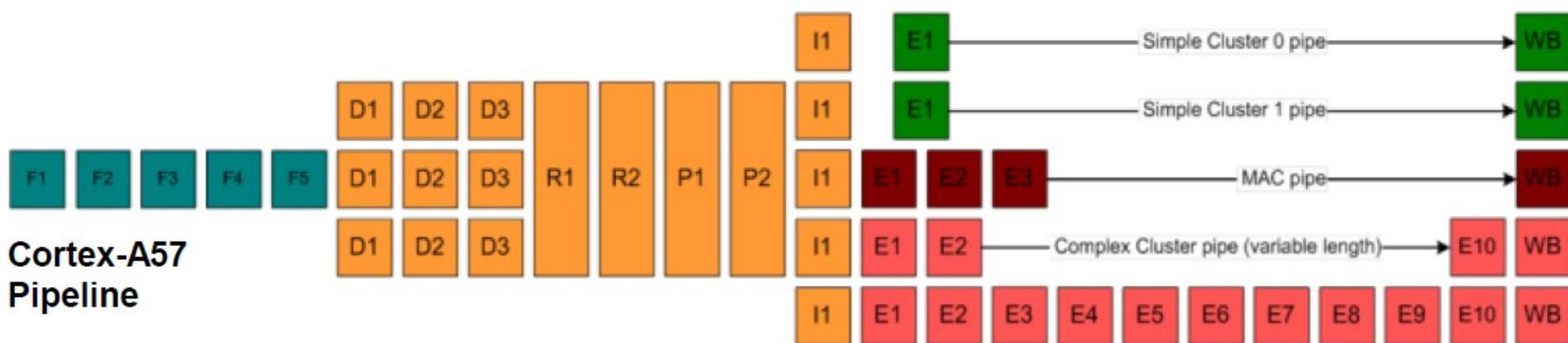
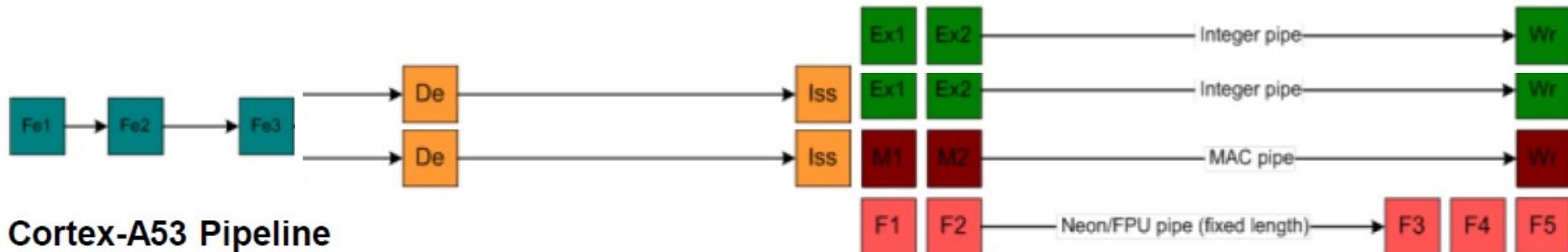
We note that the Cortex-A7 has a partially dual-issue capability, meaning that the second issue slot can only issue branch and integer operations.

In the Cortex-A53 the second issue slot can also issue load-store and FP/NEON operations.

In addition, the branch prediction capabilities of the A53 were also significantly improved by including conditional and indirect jump predictors.

## 7.3 The 64-bit low power Cortex-A53 (8)

Contrasting the Cortex-A53 and Cortex-A57 arithmetic pipelines  
[Based on 54]



D: Decode  
R: Rename  
P: Dispatch  
I: Issue  
E: Execute  
WB: Write Back

Note: Branch and Load/Store pipelines not shown  
(1x Load/Store pipeline for the Cortex A-53 and  
2x Load/Store and 1x Branch pipeline for the Cortex-A-57)

## 7.3 The 64-bit low power Cortex-A53 (9)

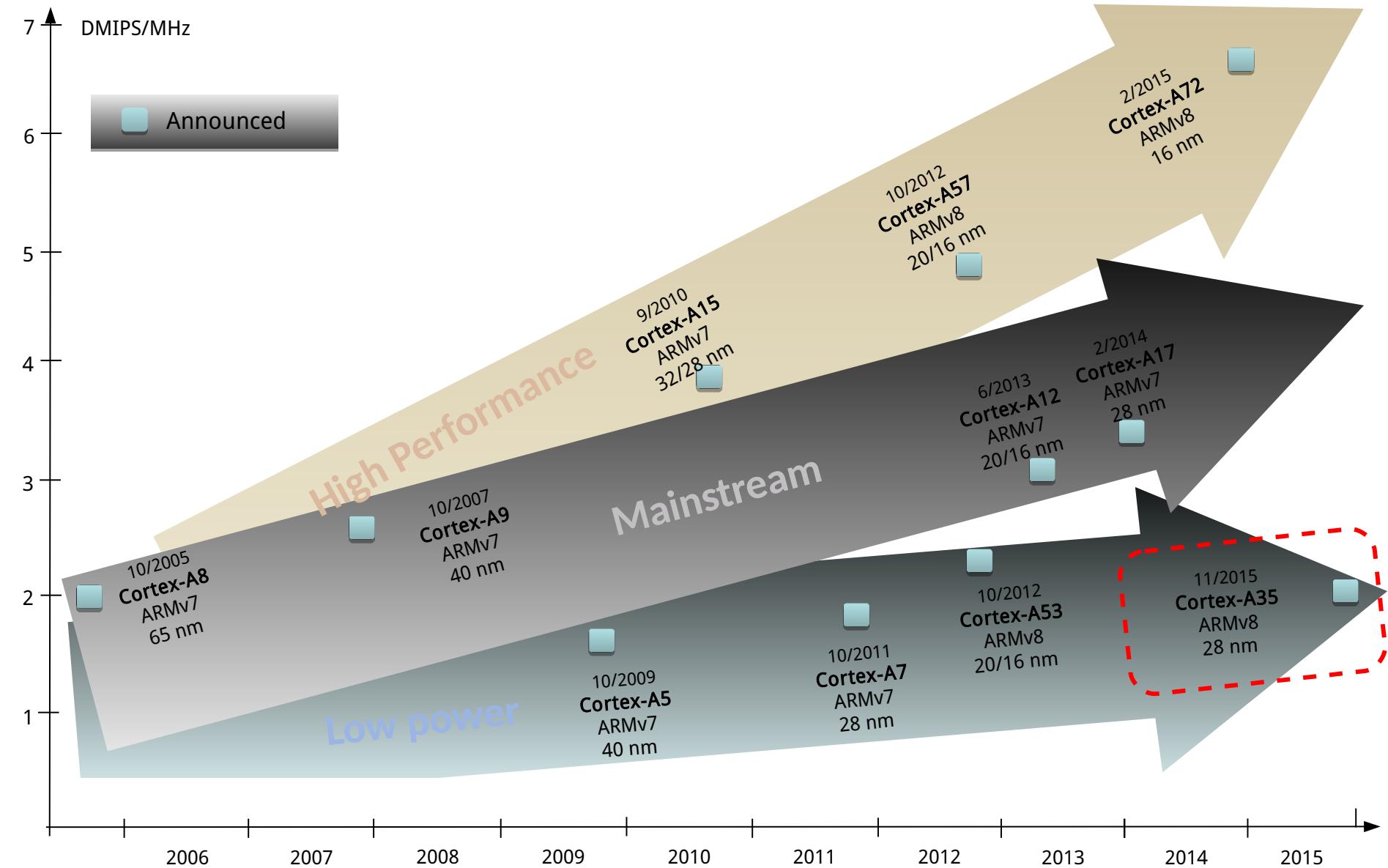
### Key features of the microarchitecture of the Cortex-A53 core -3

- Core efficiency: [2.3 DMIPS/MHz](#)
- Expected core frequency up to 1.5 GHz.

## 7.4 The 64-bit low power Cortex-A35

## 5. Overview of ARM's Cortex-A series (6)

### 7.4 The 64-bit low power Cortex-A35- 1 (Based on [12])

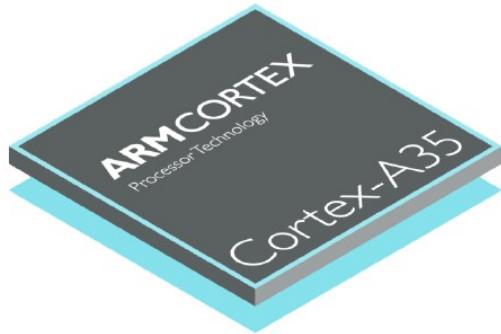


## The 64-bit low power Cortex-A35- 2

- Announced in 11/2015.
- Devices expected by the end of 2016.
- It is targeting a wide range of application processors **from mobile to deeply embedded**.
- It is ARM's **most efficient application processor**, as comparisons with the Cortex-A7 and A53 demonstrate at the same feature size (28 nm), as seen in the next Figure.

## 7.4 The 64-bit low power Cortex-A35 (3)

Efficiency of the 28 nm Cortex-A35 vs. the 28 nm Cortex-A7 [77]



**ARM TRUSTZONE**  
System Security



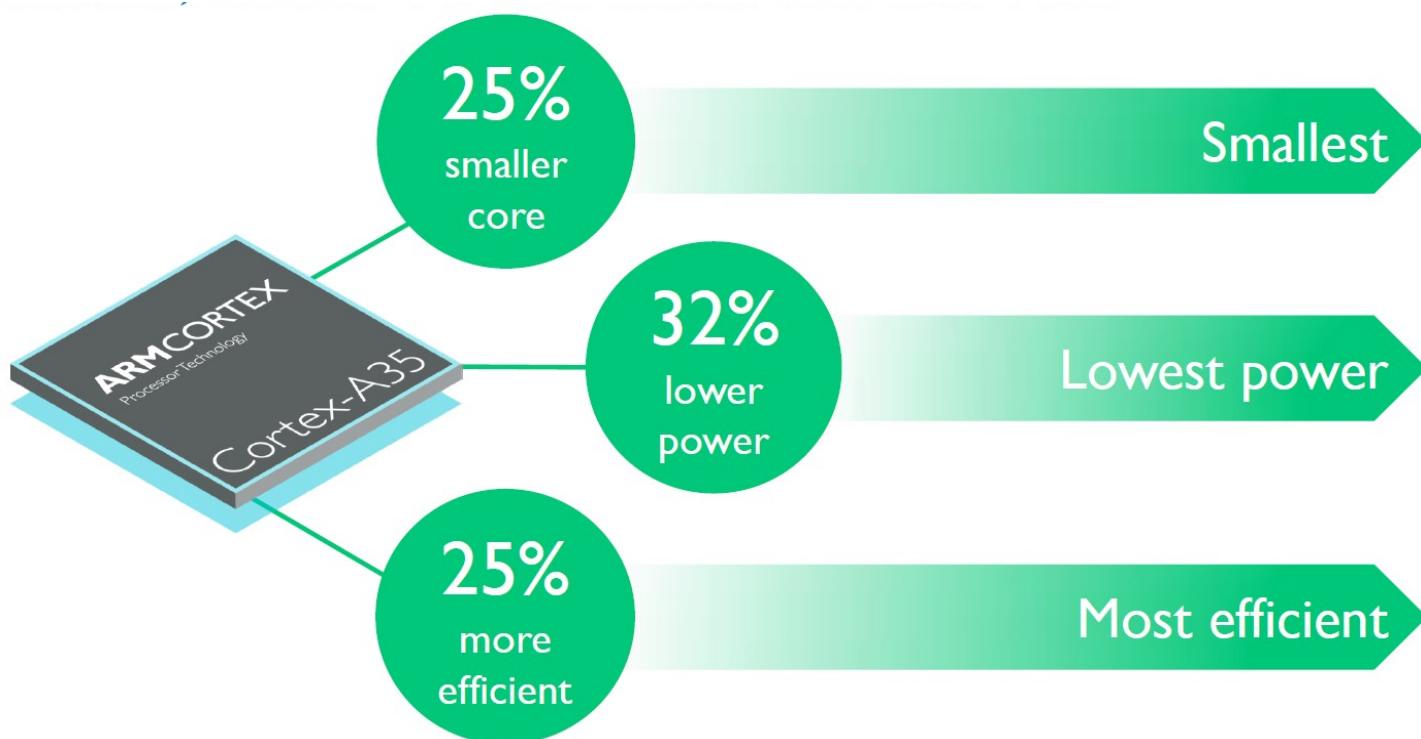
10% Lower power

+ 6% to 40% performance uplift

+ 64b capable with full backwards compatibility

## 7.4 The 64-bit low power Cortex-A35 (4)

Efficiency of the 28 nm Cortex-A35 vs. the 28 nm Cortex-A53 [77]



© ARM 2015

Same frequency implementations on 28nm process technology with identical core configurations

## 7.4 The 64-bit low power Cortex-A35 (5)

### The 64-bit high performance Cortex-A35- 2

- It is a widely configurable application processor, as indicated below.

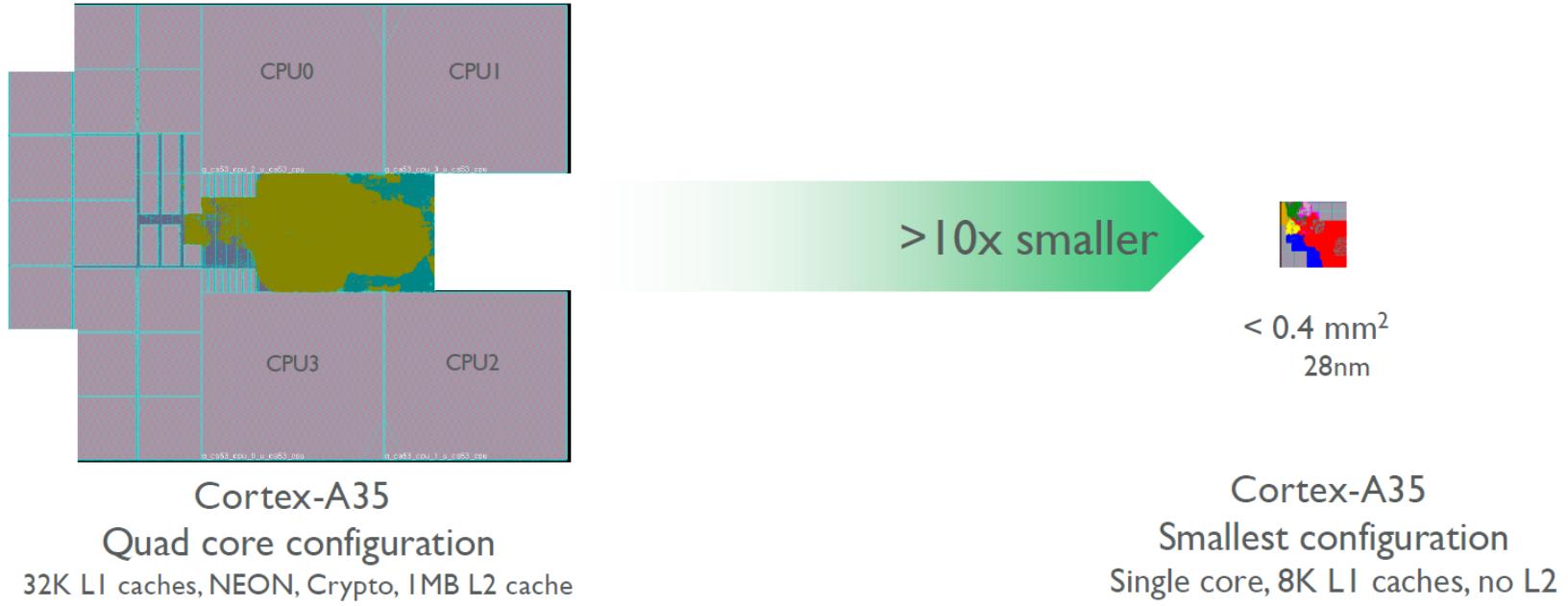


Figure: Configuration options of the Cortex-A35 [77]

- It is configurable for applications ranging from mobiles to deeply embedded.
- Target consumption is below 125 mW.
- On 28 nm technology it achieves 1 GHz by 90 mW, for planned smaller feature size of 14/16 nm ARM expect less consumption.

## 7.4 The 64-bit low power Cortex-A35 (6)

### Microarchitecture of the Cortex-A35

- It can have **one to quad cores**, as discussed before.
- The Cortex-A35 cores have **in-order, 8-stage FX pipelines** with limited dual-issue capability.
- The pipeline layout is shown in the next Figure.

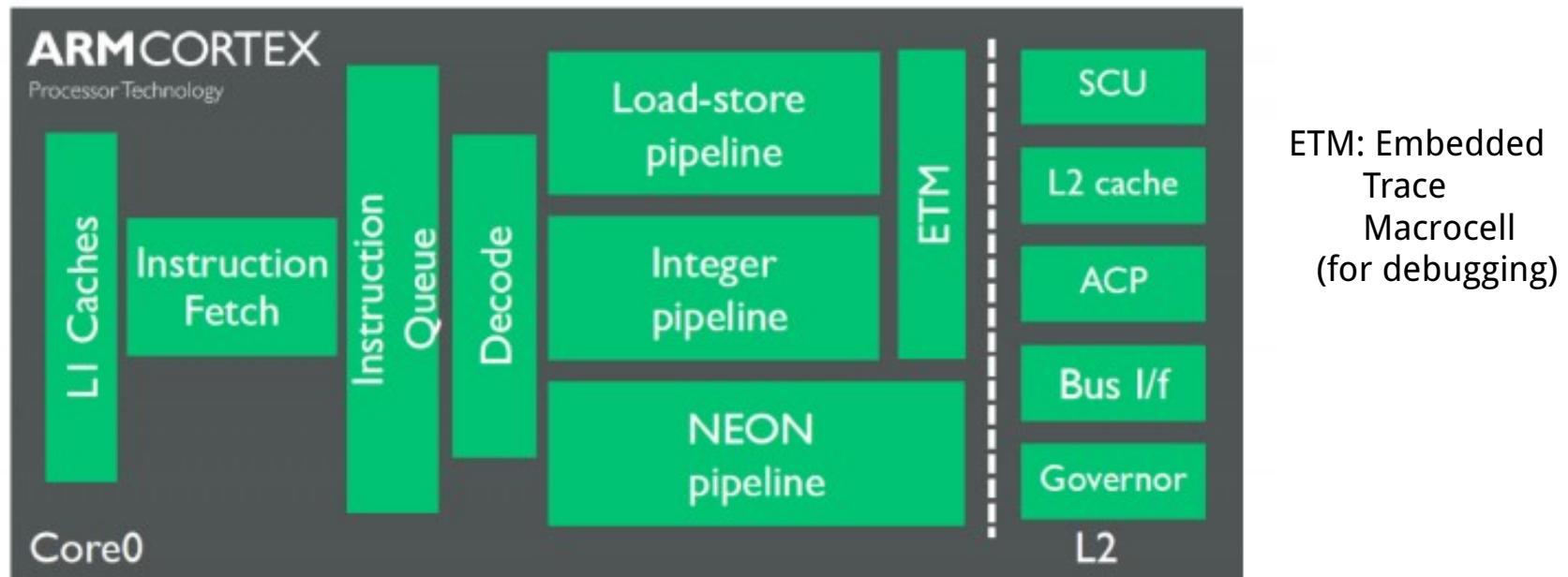


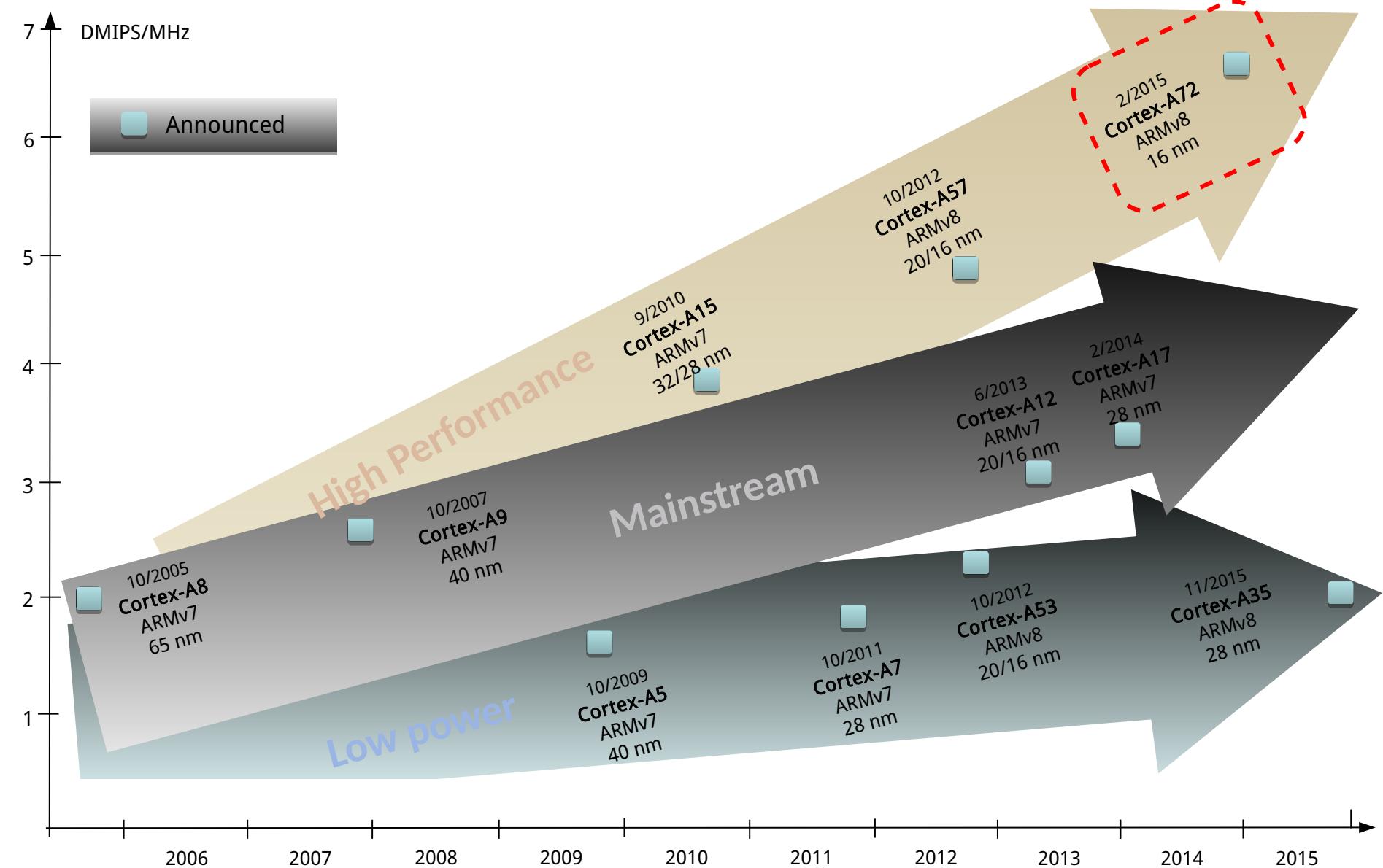
Figure: Pipeline layout of the Cortex-A35 [77]

- Compared to the Cortex-A7 ARM improved many subsystems, like instruction fetch, branch prediction, memory subsystem.

## 7.5 The 64-bit high performance Cortex-A72

## 5. Overview of ARM's Cortex-A series (6)

### 7.5 The 64-bit high performance Cortex-A72 -1(Based on [12])

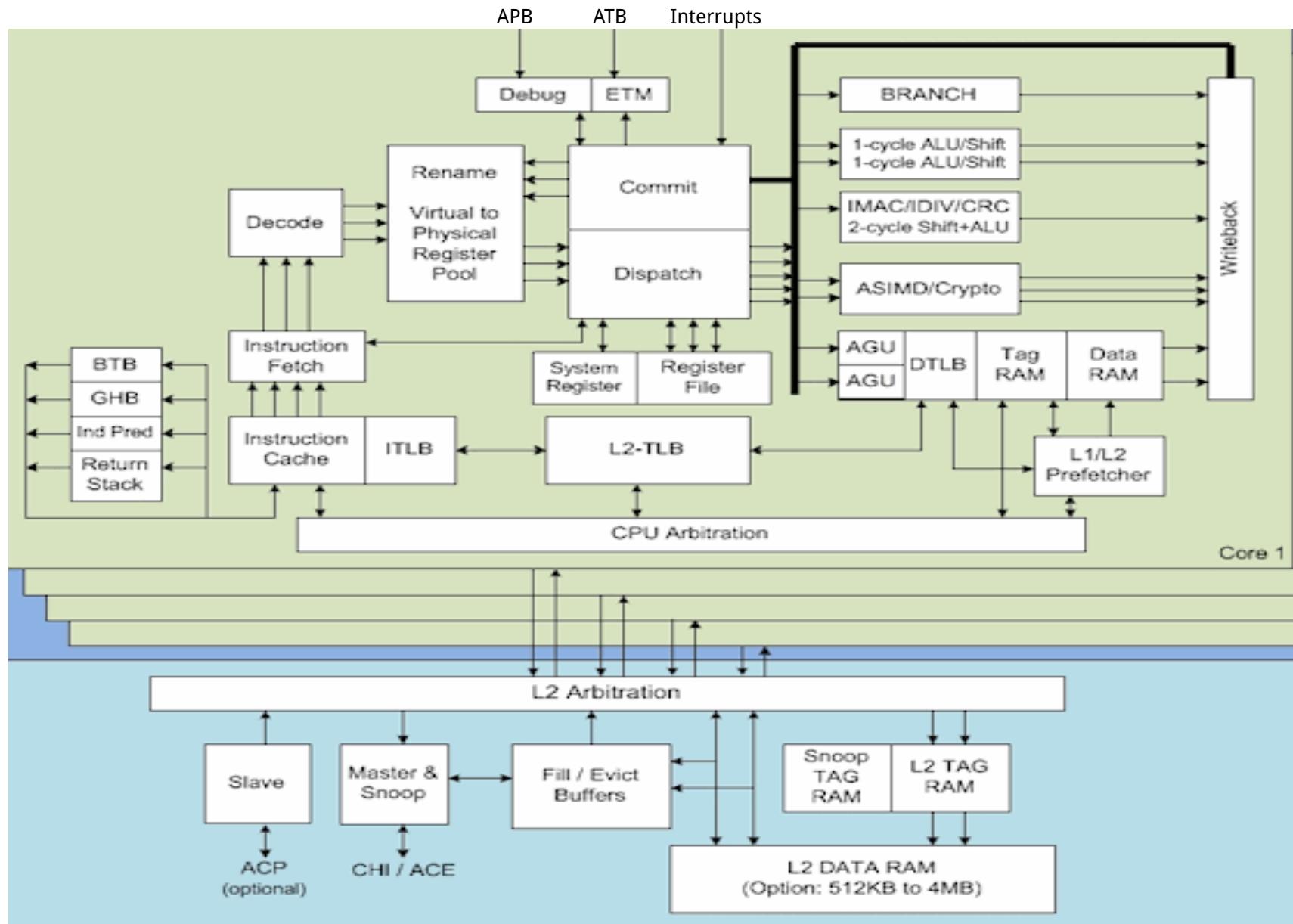


The 64-bit high performance Cortex-A72 -2

Announced in 2/2015

## 7.4 The 64-bit high performance Cortex-A72 (3)

### Main functional blocks of the 64-bit high performance Cortex-A72 [72]



## 7.4 The 64-bit high performance Cortex-A72 (4)

Remarks: Non trivial abbreviations on the above Figure

ATB: AMBA Trace Bus

APB: Advanced Peripheral Bus

ACP: Accelerator Coherence Port

(to connect non-cached coherent data sources)

ACE: AXI Coherency Extensions

(Used in big.LITTLE systems for smartphones, tablets, etc.)

AXI: Advanced eXtensible Interface

(The most widespread AMBA interface).

## 7.4 The 64-bit high performance Cortex-A72 (5)

### Remarks to the operation of the Cortex-A72

- Each core fetches four instructions per cycle from the Icache,
- decodes and renames three microinstructions per cycle,
- dispatches five microinstructions per cycle to the issue queues,
- whereas the issue queues issue up to eight microinstructions per cycle to the eight available execution units.

### The available execution units are

- a branch unit
- dual single cycle integer units
- a multi-cycle integer MAC/DIV/CRC unit
- dual Advanced SIMD (NEON)/FP units and
- dual load/store units.

## 7.4 The 64-bit high performance Cortex-A72 (6)

### Note

It is interesting to recognize that the pipeline structure of ARM's high performance processors (Cortex-A15/Cortex-A-57/Cortex-A72) remained basically the same, as is demonstrated by the pipeline structure of the Cortex-A15 below.

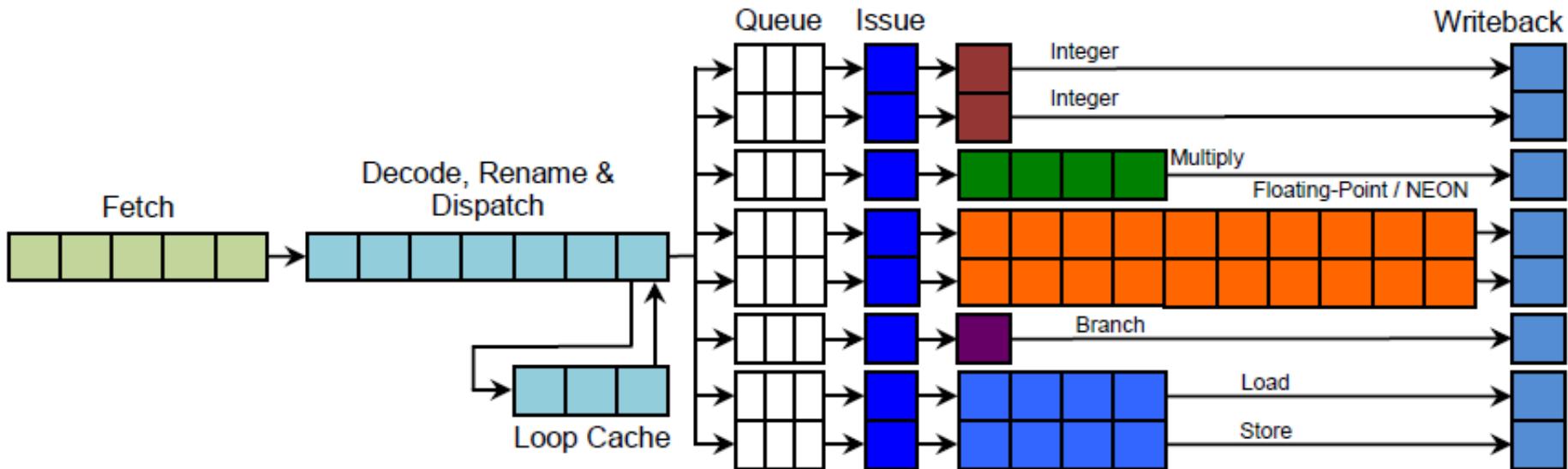
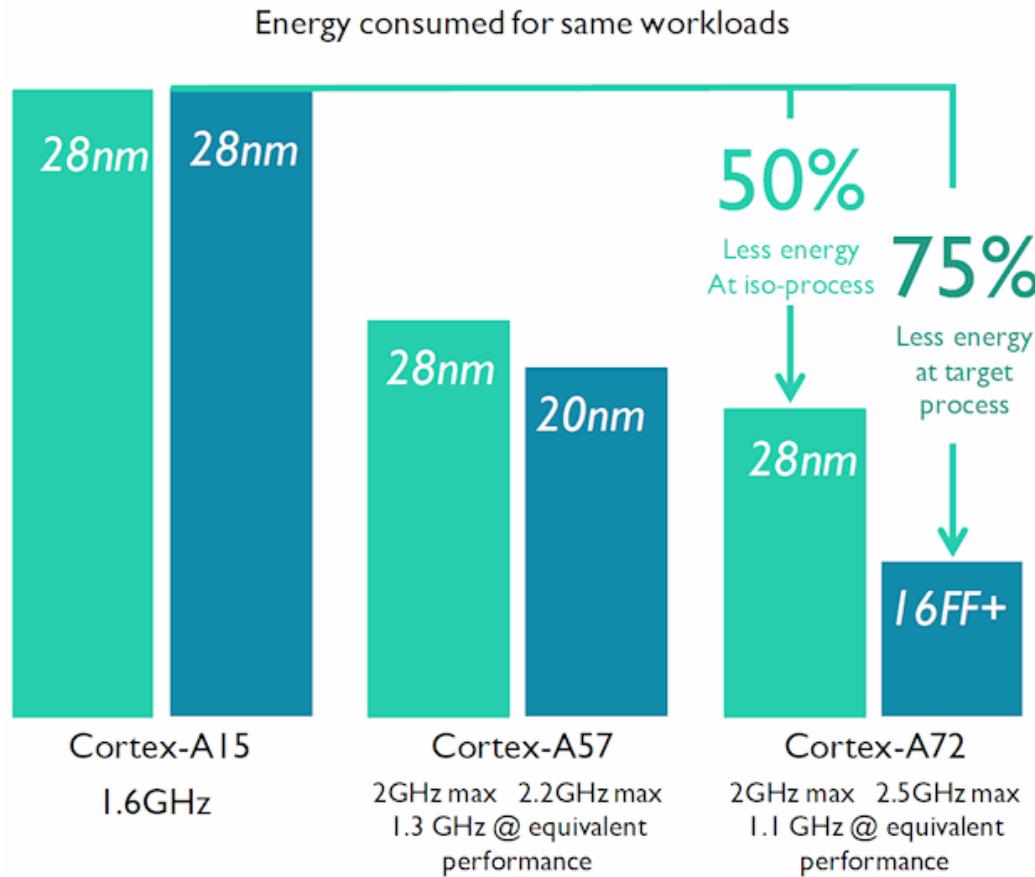


Figure: Implementation of the Cortex-A15 pipelines [37]

As seen in the Figure there are also eight issue queues and basically the same execution pipelines as in both the Cortex-A57 and Cortex-A72.

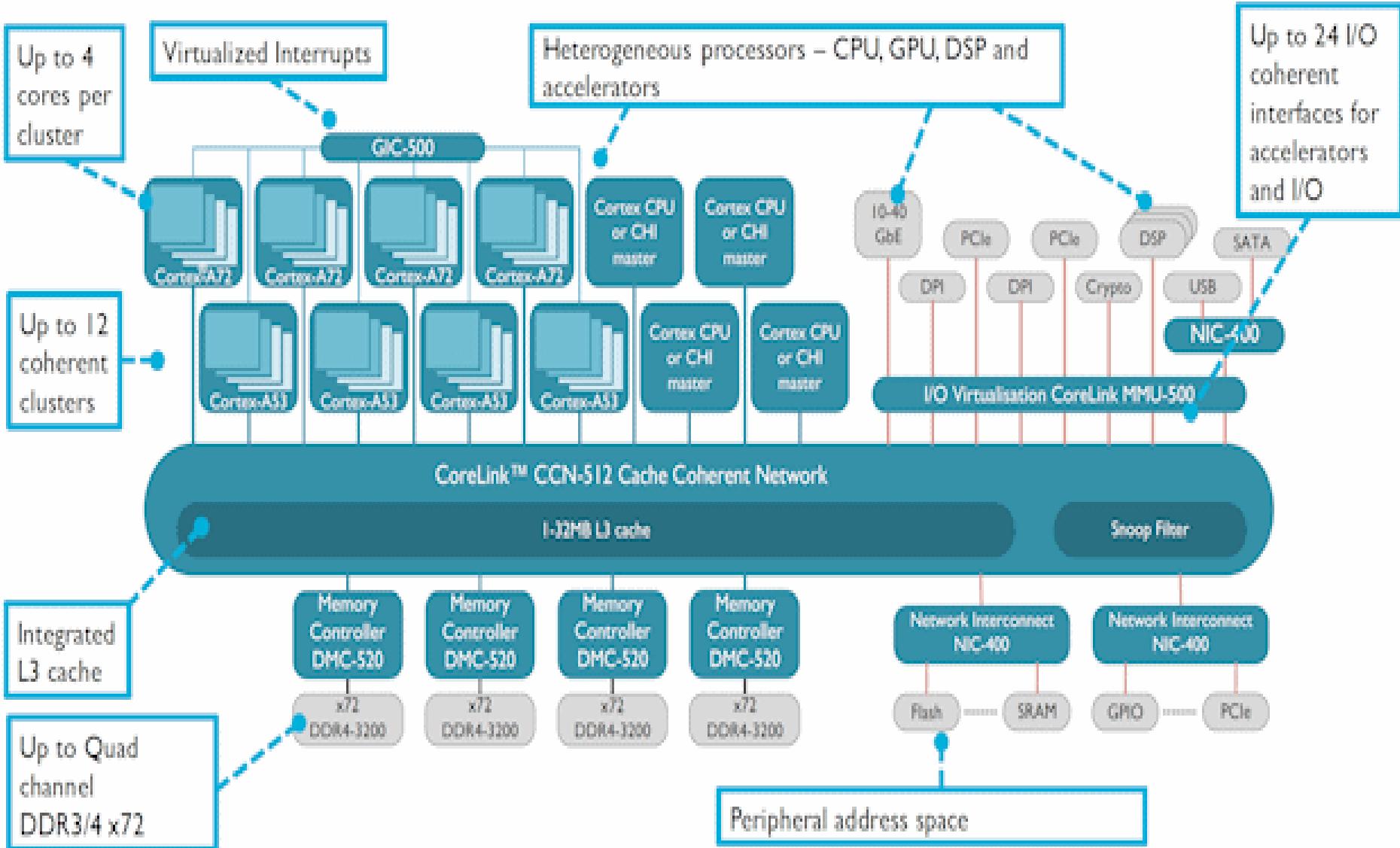
## 7.4 The 64-bit high performance Cortex-A72 (7)

Energy consumption of the Cortex-A72 compared to Cortex-A15/A57 [72]



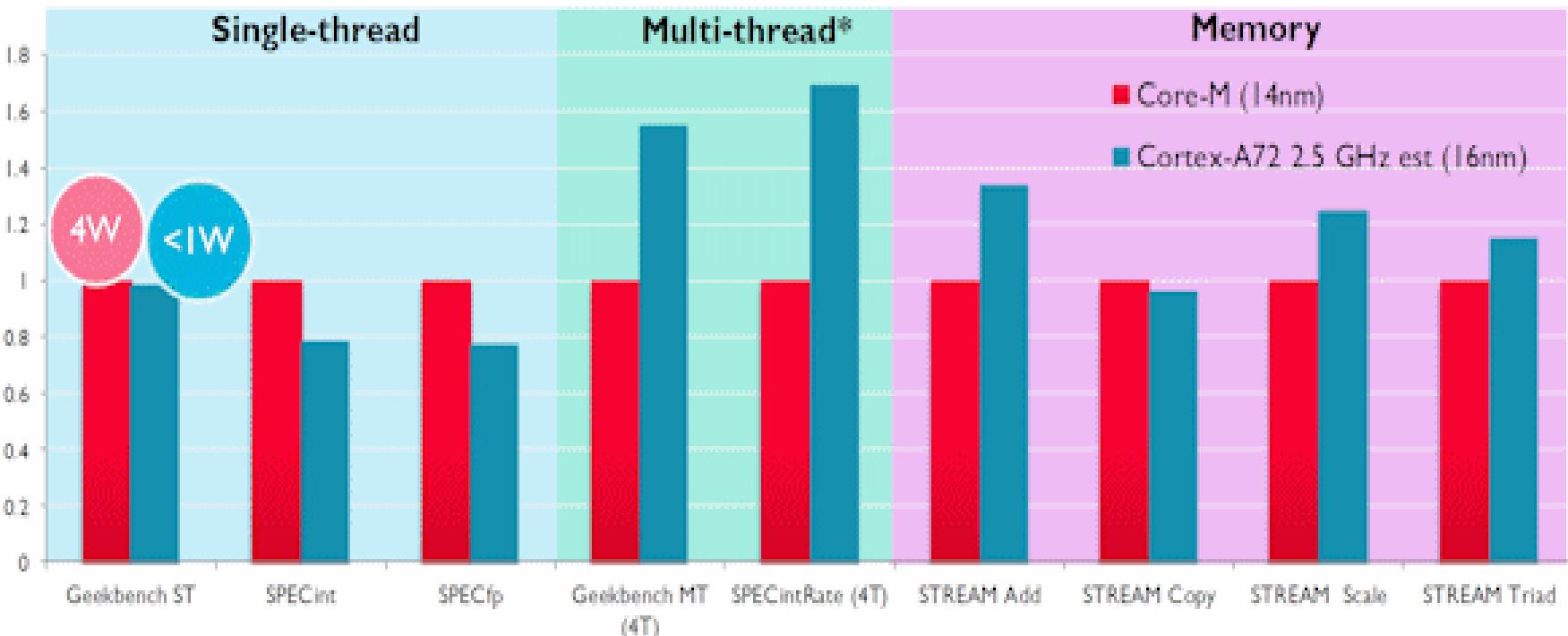
## 7.4 The 64-bit high performance Cortex-A72 (8)

### CoreLink CCN512-based heterogeneous multi-core system [72]



## 7.4 The 64-bit high performance Cortex-A72 (9)

### Performance comparison: ARM's Cortex-A72 vs. Intel's Core-M [72]



- Intel workloads measured on Dell Venue Pro II. SPEC benchmarks measured using gcc compiler v4.9 with -O3 flag.
- Cortex-A72 measured on RTL with realistic memory system with gcc compiler v4.9 - O3 settings.
- Multi-threaded workloads use 2C4T Core-M CPU and estimated on 4C Cortex-A72 configuration w/2MB L2 cache.
- Core-M 5Y10C has maximum rated frequency rating of 2GHz. (Source:ark.intel.com)
- For multi-threaded workloads, the Core-M will be thermally limited and not able to reach maximum target frequency.

ARM

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