
GDDAQ
发行版本 V20250613

Hongyi Wu(吴鸿毅)

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Welcome to GDDAQ's guides.

CHAPTER 1

简介



1.1 版本

- **GUI Qt:** 目前处于版本快速迭代阶段，欢迎大家下载使用

程序下载请访问: [PKUCAENDAQ](#)

网页版说明书请访问: 简体中文/[English](#)

- 对本获取程序有任何的意见及建议 (功能添加及改进)，欢迎给 [吴鸿毅 \(wuhongyi@qq.com\)](mailto:wuhongyi@qq.com) / [发邮件。](mailto:wuhongyi@pku.edu.cn)

1.2 关于

本说明书仅适用于 CAEN 的第二代数字化采集卡 2745/2740/2730 系列采集卡。支持不同模块 PHA/PSD/ZLE/DAW/SCOPE/OPEN 固件混合使用。通用逻辑的实现需要 2495 可编程逻辑模块。

第二代数字化采集卡型号为 x27xx

技术指导:

- Zhihuan Li 李智焕

软件主要开发者:

- 2021 - now

– Hongyi Wu 吴鸿毅 (wuhongyi@qq.com / wuhongyi@pku.edu.cn)

CHAPTER 2

程序安装

本程序安装要求依赖 boost、OpenSSL、Qt5、ROOT6 等第三方库。以下版本经过测试。

- **OS**

- Ubuntu 20.04/22.04/24.04
- Fedora 40
- Rocky 9

- **boost >= 1.67**

- 1.71.0
- 1.74.0
- 1.75.0
- 1.83.0

- **OpenSSL**

- 1.1.1
- 3.0.2
- 3.0.7
- 3.0.13
- 3.2.2

- **Qt 5**

- 5.12.8
- 5.15.3
- 5.15.9
- 5.15.13
- 5.15.17

- **ROOT 6**

- 6.24.08 some bug

- 6.26.16
- 6.30.06 some bug
- 6.32.04 some bug

本程序测试过的系统包含 Ubuntu20.04/22.04/24.04、Fedora40、Rocky9。支持各种 LINUX 操作系统编译。如果您的操作系统编译不通过请联系吴鸿毅。

```
# Ubuntu20.04 依赖安装
sudo apt -y install libboost-dev libboost-all-dev libssl-dev openssl qt5-default_
↳qtcreator libqt5charts5-dev
# Ubuntu22.04 依赖安装
sudo apt -y install libboost-dev libboost-all-dev libssl-dev openssl libqt5charts5-
↳dev
# Ubuntu24.04 依赖安装
sudo apt -y install libboost-dev libboost-all-dev libssl-dev openssl libqt5charts5-
↳dev
# Fedora 40 依赖安装
sudo dnf -y install redhat-lsb-core boost boost-devel openssl openssl-devel qt5-
↳qtcharts qt5-qtcharts-devel qt5-qtbase qt5-qtbase-devel
# Rocky 9 依赖安装
sudo dnf -y install boost boost-devel openssl openssl-devel qt5-qtcharts qt5-
↳qtcharts-devel qt5-qtbase qt5-qtbase-devel
# ROOT 6 推荐 6.26.16
```

2.1 软件安装步骤

- 删除个人目录下的老版本 PKUCAENDAQ 文件夹
- 将本程序包解压缩到个人目录中 (\$HOME)
- 编译安装 driver 文件夹内驱动

```
cd driver
tar -zxvf CAENDGTZ-USB-Drv-1.3.tgz
cd 27xx-digitizer-usb-driver/
sudo ./install.sh

cd ..
tar -zxvf caen_felib-v1.3.2.tar.gz
cd caen_felib-v1.3.2/
./configure --disable-assert
make
sudo make install
sudo ldconfig

cd ..
tar -zxvf caen_dig2-v1.8.1.tar.gz
cd caen_dig2-v1.8.1/
./configure --disable-assert
make
sudo make install
sudo ldconfig
```

- 编译 GUI 软件

```
cd GUI
chmod +x makefile.sh.x
./makefile.sh.x
# 等待编译结束，编译通过之后，文件夹内将生成可执行文件 gddaq
# 检查是否生成可执行文件 gddaq，如有则编译成功。如果没有，请联系吴鸿毅。
```

2.2 LINUX 系统中每个模块使用注册

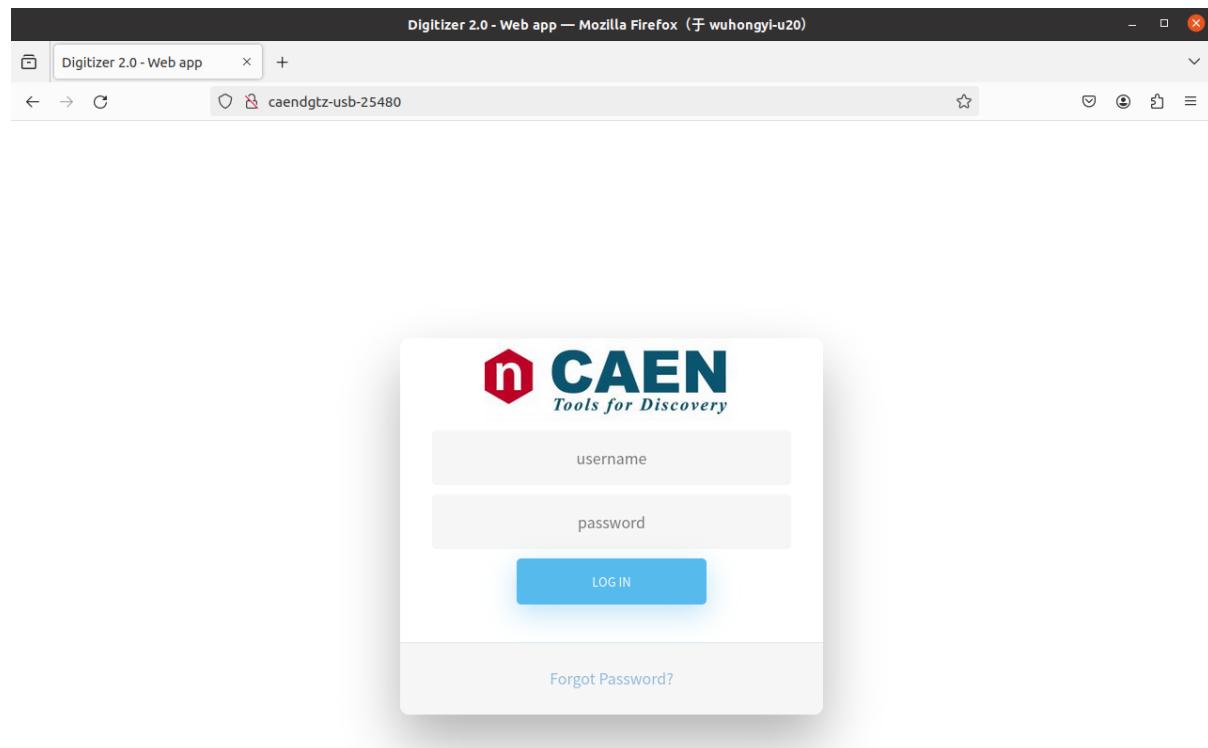
由于某些 Linux 发行版无法自动检索数字化仪 USB 名称，因此第一次使用该模块时，需要先进行注册操作。模块注册需要逐个模块进行。即在进行注册操作时，仅能有一个模块通过 USB 连接到 LINUX 系统。

将 USB3.0 线缆 type-C 端连接到模块，另一端连接到电脑。然后在浏览器中输入 CAENDGTZ-USB-{PIDNUMBER}，这里 {PIDNUMBER} 替换为使用的模块的 PID 码，例如：CAENDGTZ-USB-25480。看是否能访问，如果不能访问，说明还未对该模块进行驱动注册。

在 USB 驱动安装包内，例如 CAENDGTZ-USB-Drv-1.2 里面，有驱动注册脚本文件 regPID.sh，通过以下命令运行。执行之后会看到注册成功的提示。

```
sudo ./regPID.sh
```

之后，再通过网页访问 CAENDGTZ-USB-{PIDNUMBER}，即可看到以下登陆页面，默认用户名、密码均为 admin。



登陆之后界面如下所示，左侧菜单栏中，可以进行网络设置。如果想通过网线进行数据获取，则通过该页面进行 IP 设置。根据实验室网络情况，选择 DHCP 自动分配 IP 或者 Manual 手动配置 IP。进行 IP 设置之后，在浏览器中输入模块的 IP，则也可以访问该设置页面。

The screenshot shows the Digitizer 2.0 Home page in Mozilla Firefox. The title bar reads "Digitizer 2.0 - Home — Mozilla Firefox (于 wuhongyi-u20)". The main content area is divided into three sections: "Errors flags", "Board information", and "Hardware monitor".

Errors flags:

- Power Status (Green)
- Board Init (Green)
- SI5341 PLL Lock (Green)
- SI5395 PLL Lock (Green)
- LMK04832 PLL Lock (Green)
- JESD204B Lock (Green)
- DDR4 PL Bank0 Calibration (Green)
- DDR4 PL Bank1 Calibration (Green)
- DDR4 PS Calibration (Green)
- FPGA Configuration (Green)
- BIC Check (Green)
- ADC Temp (Green)
- Air Outlet Temp (Green)
- FPGA Temp (Green)
- DC/DC Temp (Green)
- Clock In (Green)
- ADC Shutdown (Green)

Board information:

- Model name: DT2745B
- Firmware version: 2022092904
- Firmware type: DPP_PSD
- Bitstream version: 0.1.27
- PID: 25480
- License: Not Licensed
- Trial time left: 02:16
- BIOS: 2.1
- System: 2022090600
- LAN Link up (Green)
- USB Link up (Green)

Hardware monitor:

- Temp Sens Air In: 31.2 °C
- Temp Sens Air Out: 44.4 °C
- Temp Sens Core: 69.2 °C
- Temp Sens First ADC: 40.3 °C
- Temp Sens Last ADC: 54.1 °C
- Temp Sens DC/DC: 43.9 °C
- V In Sens DC/DC: 5.039 V
- V Out Sens DC/DC: 0.725 V
- I Out Sens DC/DC: 7.484 A
- Speed Sens Fan 1: 3330 rpm
- Speed Sens Fan 2: 3300 rpm

Left sidebar (Menu):

- Dashboard (selected)
- Board ID card
- Network settings
- User management
- Firmware
- Clock settings
- License

Bottom left sidebar:

- Mon, 17 Dec 2103
05:21:34 GMT
- Version 1.1.7
©2021-2024 CAEN SpA

CHAPTER 3

固件

3.1 最新固件

- 2745
 - V2745-scope-1G-2024112500.cup
 - V2745-dpp-pha-1G-2025052201.cup
 - V2745-dpp-psd-1G-2025052200.cup
 - V2745-dpp-zle-1G-2025012707.cup
 - V2745-OpenDPP-2025060604.cup
 - V2745-OpenScope-2025051100.cup
- 2740
 - V2740-scope-1G-2024112500.cup
 - V2740-dpp-pha-1G-2025052201.cup
 - V2740-dpp-psd-1G-2025052200.cup
 - V2740-dpp-zle-1G-2025012707.cup
 - V2740-OpenDPP-2025060603.cup
 - V2740-OpenScope-2025051102.cup
- 2730
 - V2730-scope-1G-2025060602.cup
 - V2730-dpp-psd-1G-2025052203.cup
 - V2730-OpenDPP-2025060601.cup
- 2751
 - V2751-scope-1G-2025040700.cup

为了方便实验的诊断和调试，我们建议 CAEN 在 DPP 固件中添加/修改了以下功能：

- 外部信号重置时间戳，可通过 SIN/GPIO 输入信号来重置时间戳（已完成）

- 获取 start 时可选是否重置时间戳（未完成）
- 添加类似 SelfTriggerRate 的监视参数，监视符合/反符合的计数率，监视实际的输出计数率（未完成）
- WaveDigitalProbe 中添加符合、反符合信号（未完成）
- 2730 添加输入信号延迟（未完成）

3.2 固件更新

通过 USB (CAENDGTZ-USB-{PIDNUMBER}) 或者 IP 方式访问模块配置页面，在左侧菜单栏有个 Firmware，点击进入该页面，如下：

The screenshot shows the 'Firmware' configuration page. On the left, there's a sidebar with various menu items like Dashboard, Board ID card, Network settings, User management, Time/Date settings, Parameters (Beta), and Firmware (which is currently selected). The main content area has a heading 'Firmware' and a sub-section 'Storage Space Usage' showing 11% usage. A button 'Upload new firmware...' is visible. Below this, a table lists several firmware versions:

Version	Type	Action Buttons
2023112703	ETH 1G	Current, Default, More
DPP-PHA		
2023091902	ETH 1G	More
DPP-ZLE		
2023091901	ETH 1G	More
DPP-PSD		
2023091900	ETH 1G	More
Scope		
2022052302	ETH 1G	Factory, More
Factory firmware Scope		

At the bottom of the page, there are footer details: 2024/2/6, GMT+1 14:29:01, Version 1.2.0, ©2021-2024 CAEN SpA.

检查该页面的 Scope/PHA/PSD/ZLE 固件版本与获取程序包中，firmware 文件夹内的是否一致，如果不一致，通过“Upload new firmware”上传新固件。网页中每个固件右端均有一个蓝色下三角按钮，通过点击该按钮，可以进行当前使用的固件进行切换，设置开机默认加载的固件等。另外，及时删除老版本的固件。

CHAPTER 4

图形化指南

使用图形化软件前，请先阅读时间同步，GUI 操作等相关内容。

CHAPTER 5

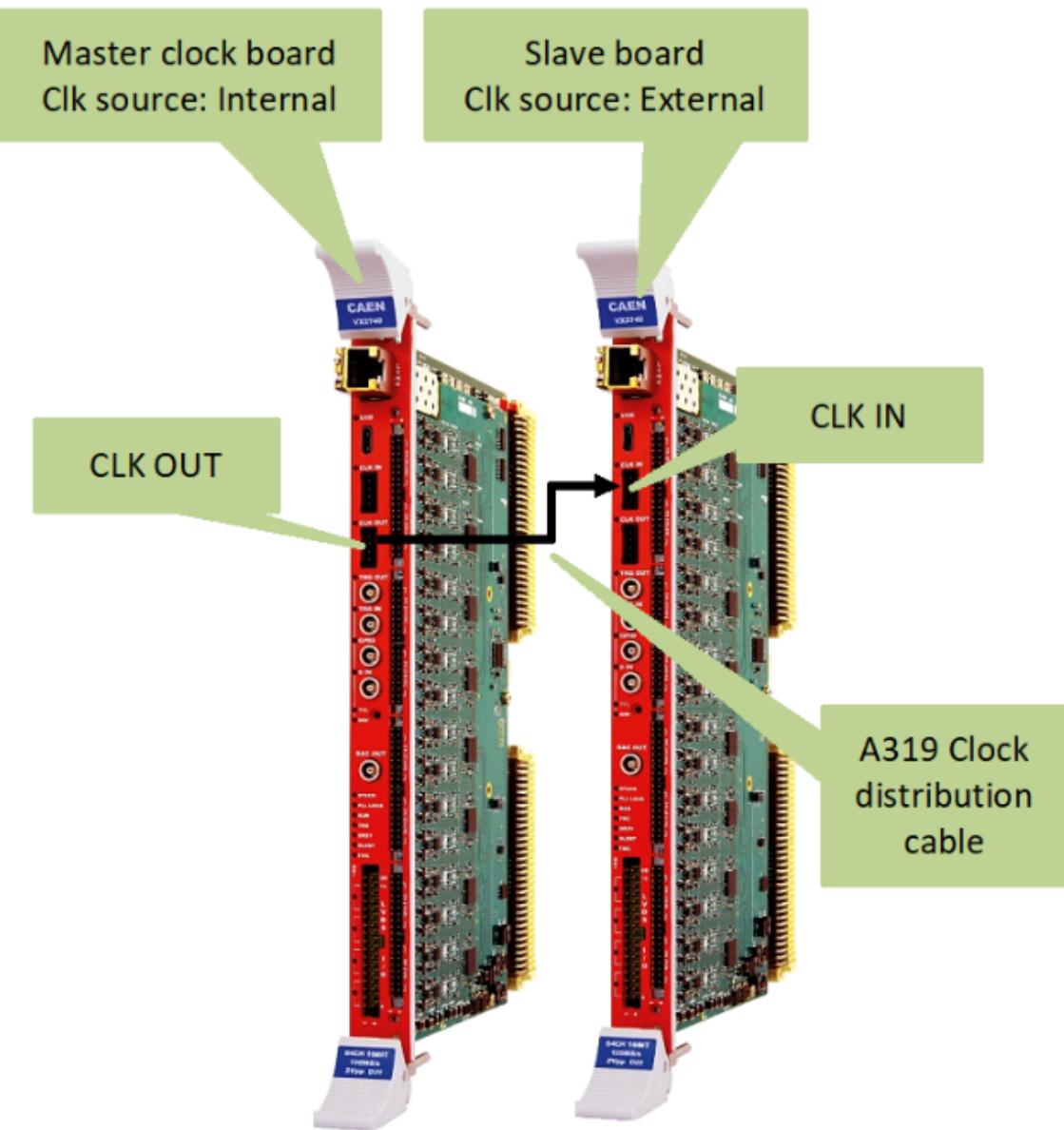
时间同步和采集

在多模块的采集系统中，一个最基本的要求是所有模块同步采集。其要求所有模块共用一个时钟源，然后同时开始和结束数据采集。

5.1 时钟源设置

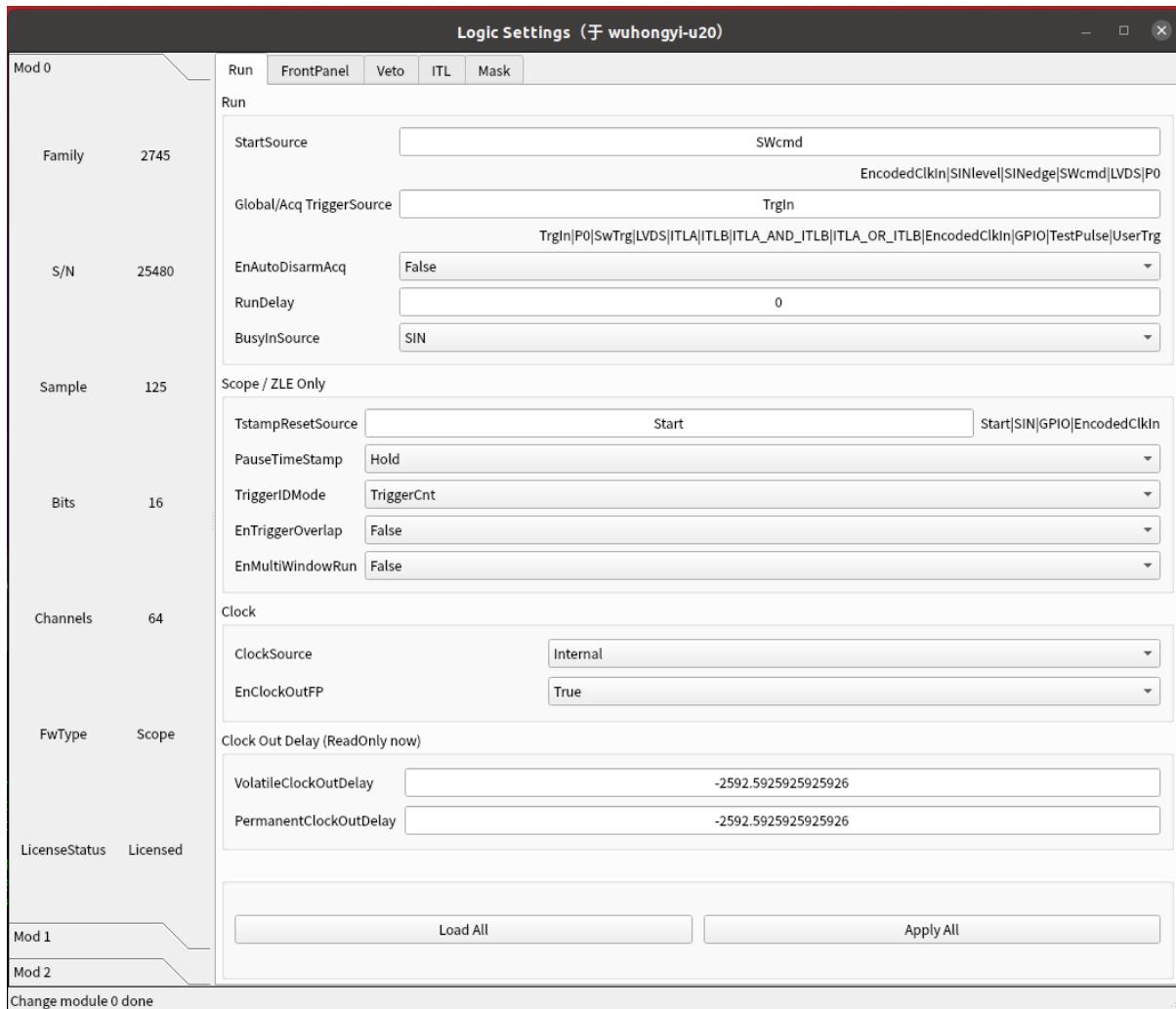
CAEN 的时钟可通过前面板的 A319 线缆串连，也可通过机箱背板来共享时钟（开发中）。

下图为典型的时钟同步配置图，通过 A319，前一个的 CLK OUT 连接到后一个的 CLK IN。

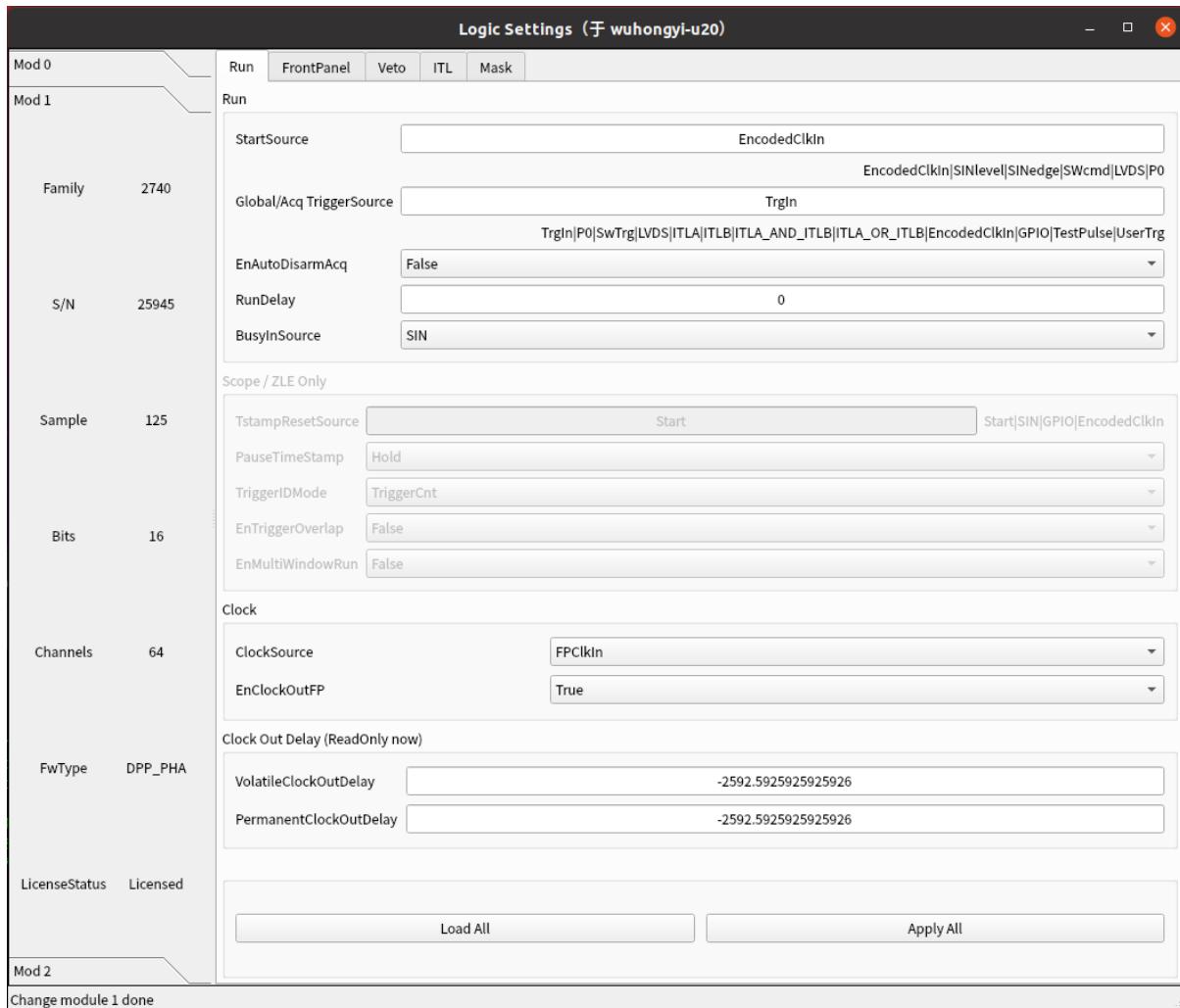


链接时钟同步线缆之后，还需要依次对每个模块设置时钟源：

对于主模块，需要设置 ClockSource 为 Internal，设置 EnClockOutFP 为 True，如下图所示：



对于所有的从模块，需要 ClockSource 为 FPclkIn，设置 EnClockOutFP 为 True，如下图所示：



以上设置为将主模块的内部时钟通过前面板输出，从模块依次接收前一个模块通过前面板传输来的时钟信号。

5.2 同步采集

对于一个同步的系统，通常主模块设置为用来控制获取的开始、结束，其它从模块也需要进行相应的一些设置。通过前面板来控制获取的开始和结束，常用有以下三种方式：SYNC-CLKIN、SIN-GPIO、SIN-TRGOUT。其中 SYNC-CLKIN 是最广泛被使用的，因其包含在前面板的时钟同步线内，而另外两种则需要占用前面板上的 SIN/GPIO/TRGOUT LEMO 端口，常用于与其它获取系统的同步采集。

5.3 SYNC-CLKIN

主模块需要将 StartSource 设置为 SWcmd，将 SyncOutMode 设置为 Run。所有从模块将 StartSource 设置为 EncodedClkIn，将 SyncOutMode 设置为 SyncIn。

5.4 SIN-GPIO

主模块需要将 StartSource 设置为 SWcmd，将 GPIOMode 设置为 Run。所有从模块将 StartSource 设置为 SINlevel，将 GPIOMode 设置为 SIN。

5.5 SIN-TRGOUT

将主模块的 TRGOUT 连接到第一个从模块的 SIN，依次类推。

主模块需要将 StartSource 设置为 SWcmd，将 TrgOutMode 设置为 Run。所有从模块将 StartSource 设置为 SINlevel，将 TrgOutMode 设置为 Run。

5.6 系统外部时钟

x27xx 模块的默认时钟频率是 62.5 MHz。当 DAQ 与其它获取系统要同步时，输入外部系统的时钟不是 62.5 MHz 时，需要进行 PLL 的配置。CAEN 提供部分时钟频率的配置文件，如果所使用时钟频率 CAEN 网页上没有提供，联系 CAEN 获取相应文件。

如下图，点击“Upload new PLL”，上传所需要的 PLL 相关文件。

如下图，选择所需要的配置文件，点击“apply”按钮，然后时钟选项需要选择外部输入。之后重启模块使 PLL 生效。

PLL configuration

The PLL Configuration allows you to upload new configuration files and select which one to apply.

[Upload new PLL](#)

Current configuration (si5395) -> [si5395_default_config.txt](#)

Choose configuration:

si5395_default_config.txt

si5395_V2724_01-Refclk100M.txt
si5395_V2724_01-Refclk10M.txt
si5395_V2724_01-Refclk20M.txt
si5395_V2724_01-Refclk25M.txt
si5395_V2724_01-Refclk50M.txt
si5395_default_config.txt



[✓ Apply](#)

CHAPTER 6

图形交互界面

6.1 配置文件

配置文件放置于 **pars** 文件夹内，
json 格式文件，主要包含模块的 PID 或者 IP 等信息。

```
{  
  "modules": 3,  
  "connecttype": "eth",  
  "pid": [25480, 25945, 24946],  
  "ip": ["162.105.54.162", "162.105.54.187", "162.105.54.90"],  
  
  "par": "setting.json",  
  
  "userpars": "../pars/init.txt"  
}
```

其中，参数 **modules** 为系统使用数据采集卡数量，参数 **connecttype** 为采集卡与获取电脑的连接方式，可填写“usb”或者“eth”。使用 **usb** 读取，单个模块上限为 280 MB/s，使用网络读取，目前使用的 1G 网络，单个模块的上限为 110 MB/s。如果采用 **USB** 方式读取，则参数 **pid** 生效，依次为系统每个模块的 PID。如果采用网络读取，则参数 **ip** 生效，依次为系统每个模块 IPV4 的 IP。

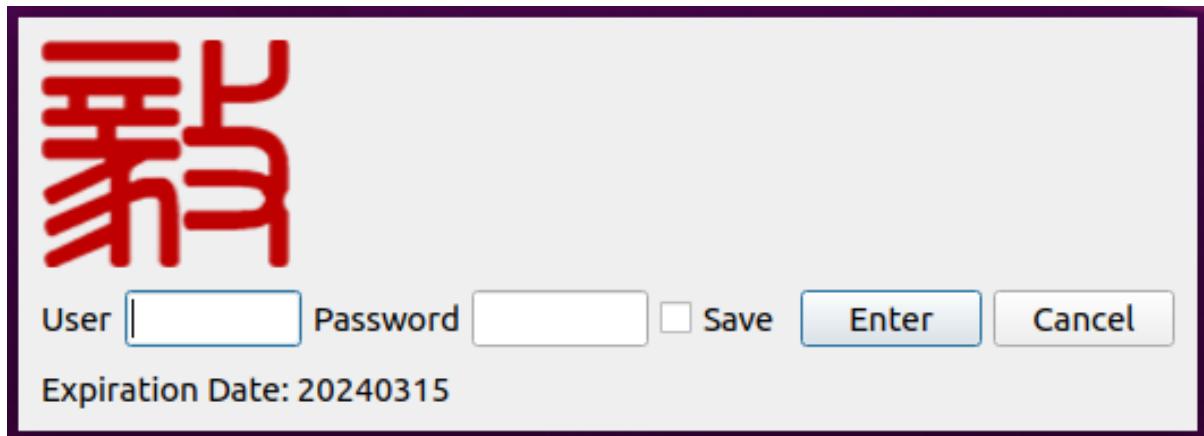
获取参数文件。

进入 GUI 目录，执行以下命令即可弹出主控制界面

```
./gddaq  
# 如果出现以下错误，设置以下环境变量  
# ./gddaq: error while loading shared libraries: libCAEN_FELib.so.0: cannot open  
#       shared object file: No such file or directory  
# export LD_LIBRARY_PATH=/usr/local/lib:$LD_LIBRARY_PATH
```

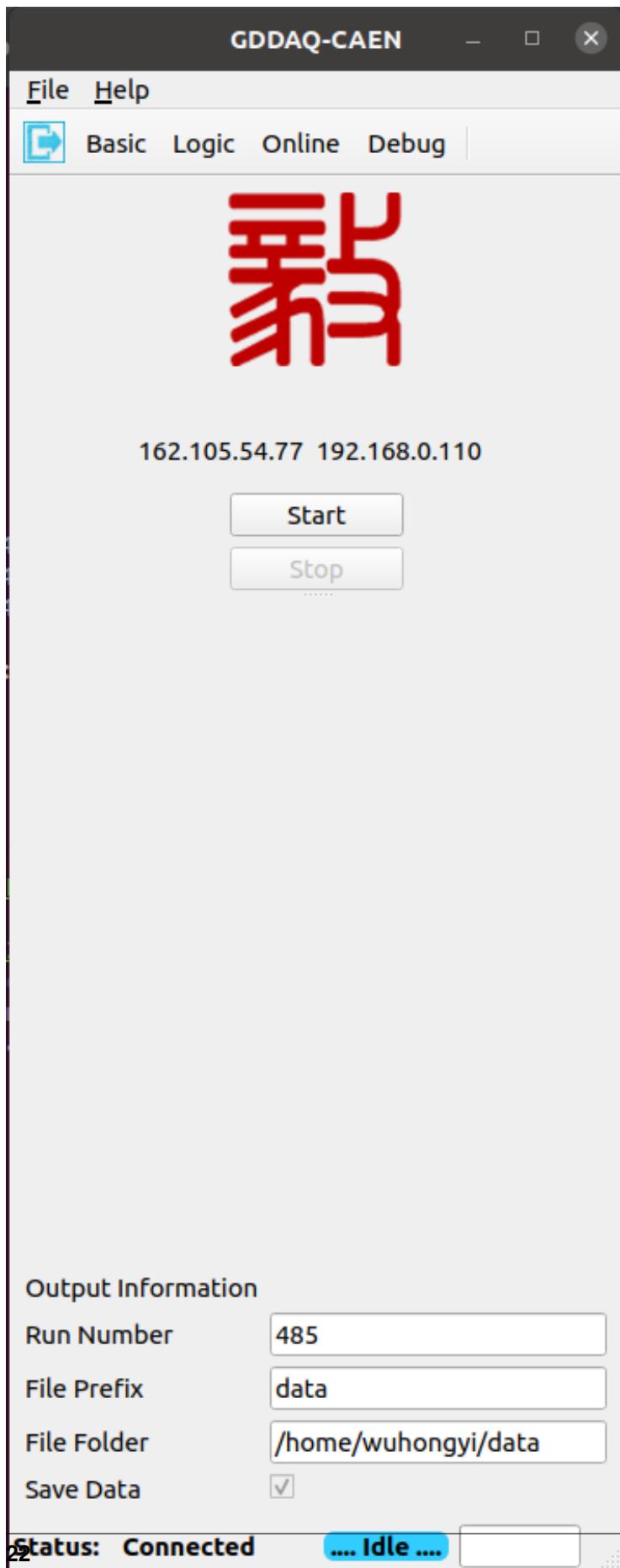
6.2 登陆界面

为了实现不同登陆账号不同操作权限。
降低实验值班人员的操作权限，目前暂未实现。。。

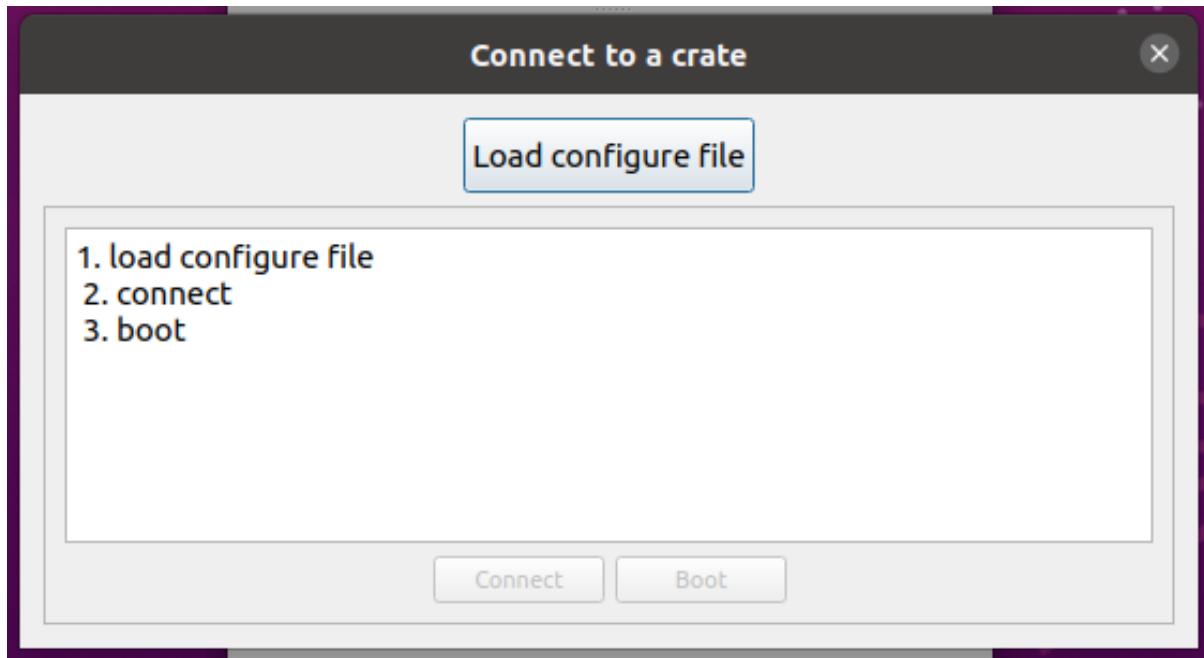


输入用户名 (admin)、密码 (admin) 后，弹出主控制界面。

6.3 主控制界面

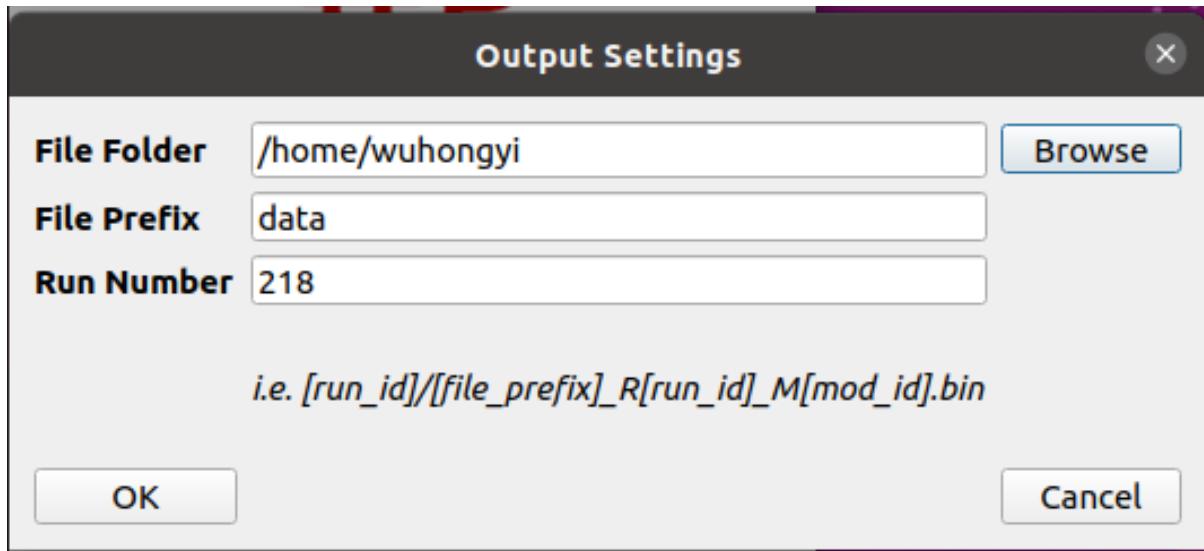


主界面左上角 File 下拉选择 “connect to device”，弹出如下界面中，点击文件选择框，选择提前配置好的参数文件。

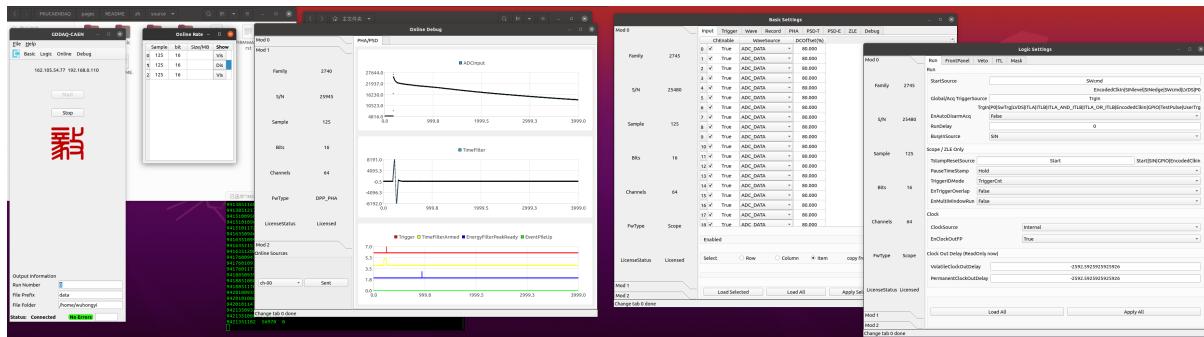


当配置文件加载后，会在对话框中间显示配置主要配置信息，PID 或者 IP 信息。然后点击“connect”，之后再点击“boot”，走完进度条之后，该弹出界面自动关闭。所有配置文件中的模块均完成初始化。

主界面左上角 File 下拉选择 “Output Configure”，弹出如下界面。本界面用于设置输出数据的文件夹，文件名称以及运行编号。按 OK 按钮关闭界面。以上信息只能在本界面进行修改，获取主界面显示该信息。



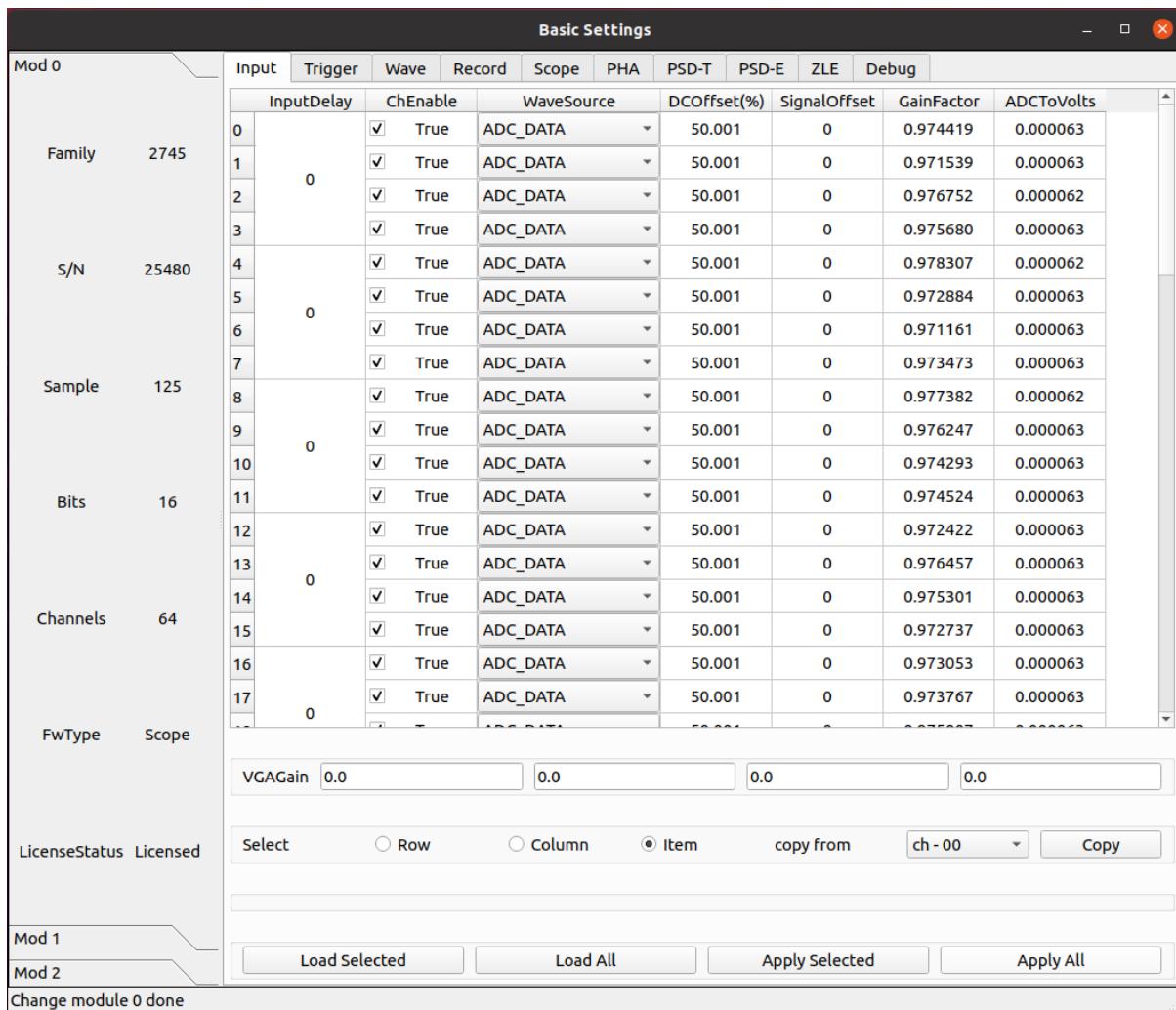
完成系统初始化之后，主控制界面上方的 Basic、Logic、Online、Debug 四个按钮将会浮起，点击即可弹出相应的子界面，再点击即可隐藏。



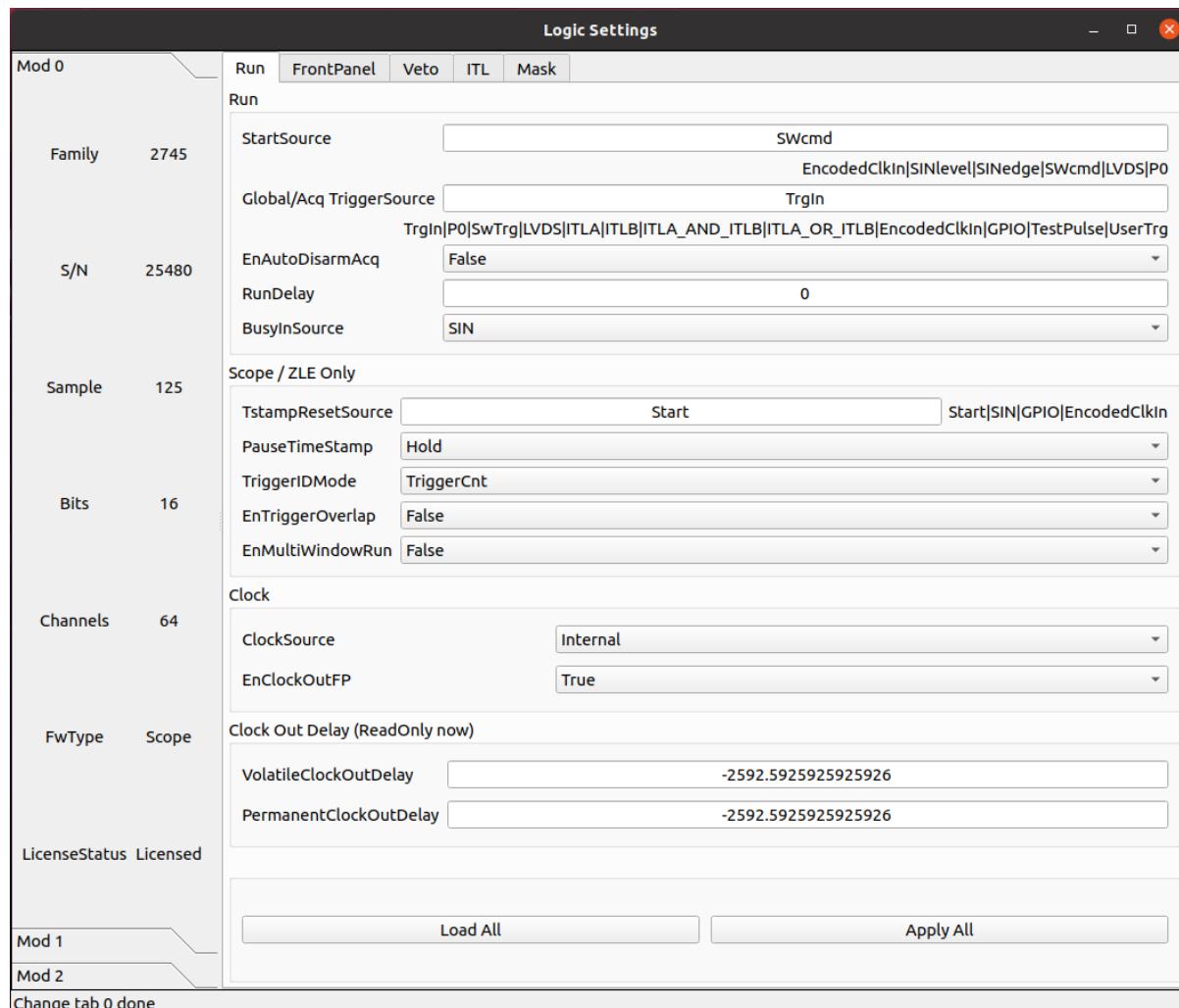
在弹出的 Basic、Logic、Debug 子界面，当系统为多个模块时通过点击左侧的“Mod 0”、“Mod 1”、“Mod 2”等切换标签进行采集模块的切换，切换时会自动读取右边页面中的信息。每个子界面上方有多个标签页，点击该标签即可切换到相应参数配置页面。

由于本程序能够自适应不同的固件，在同一个参数设置标签页，不同的固件中会显示不同的可设置参数。

基础参数设置



逻辑参数设置

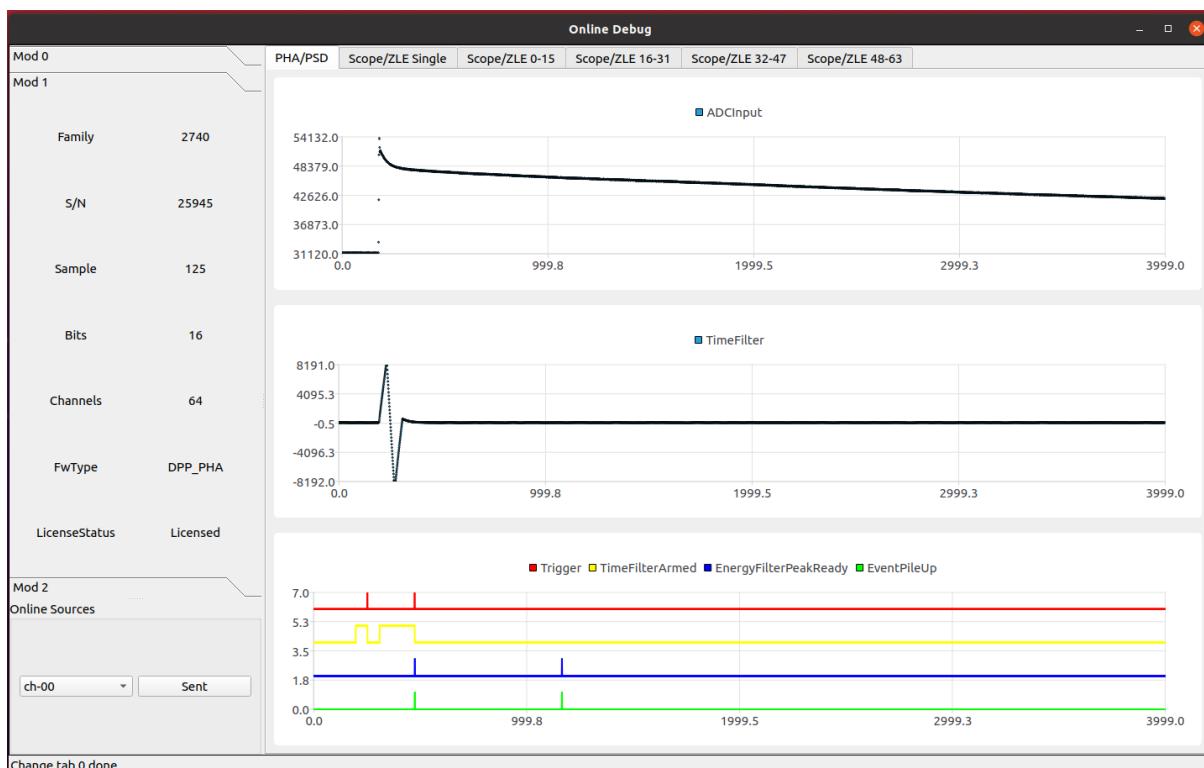
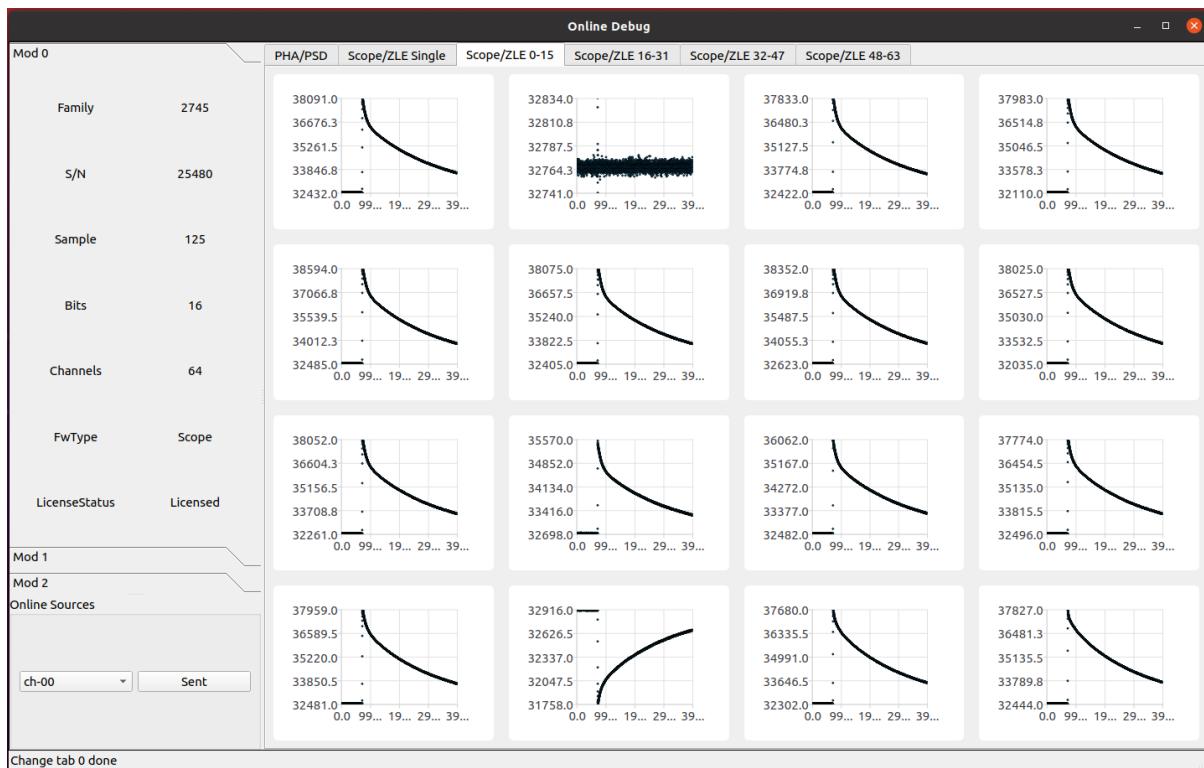


实时计数率监视

The screenshot shows three windows from the GDDAQ software interface:

- Online Rate** window: A table with columns Sample, bit, Size/MB, and Show. It contains three rows of data: 0, 1, and 2. Row 0 has Show set to Dis. Row 1 has Show set to Dis. Row 2 has Show set to Vis.
- Mod 0** window: A table with four columns: SelfTrgRate, SelfTrgRate, SelfTrgRate, and SelfTrgRate. It contains 16 rows of data, indexed 0 to 15. The data shows varying values for the first column, mostly 0 or low values, and the last column has a value of 840952 at index 11.
- Mod 1** window: A table with ten columns: SelfTrgRate, Realtime, Deadtime, TriggerCnt, vedEventC, WaveCnt, SelfTrgRate, Realtime, Deadtime, and TriggerCnt. It contains 16 rows of data, indexed 0 to 15. Most columns show constant values across all rows.

波形监视与调试



6.4 网页在线监视

GUI 程序占用端口 8765 进行在线显示，用户可通过 ip:8765 进行访问，本地可使用 127.0.0.1:8765 访问。访问在线监视需要登陆，共设置 admin 和 guest 两个用户。admin 的密码为 admin，该账号获得所有访问权限，可以随时进行谱的清除等操作。guest 没有密码，只能查看在线监视信息。

CHAPTER 7

SCOPE 固件

7.1 基本参数配置

7.1.1 输入信号

参数 ChGain

仅限 x2730.

设置可变增益放大器（VGA）的增益。

Unit of Measure: dB

参数 InputDelay

设置输入延迟，单位为采样点。

该值设置每 4 个通道共用一个相同配置。

参数 ChEnable

独立设定每个通道是否开启使用。如果通道不启用，它不提供任何数据，同时它的自触发也关闭。

参数 WaveSource

在正常模式下，采集的波形来源于模拟输入的 A/D 转换产生的 ADC 采样序列。出于测试目的，可以用内部数据生成器替换 ADC 数据。

- **ADC_DATA**
 - Data from the ADC (normal operating mode)
- **ADC_TEST_TOGGLE**
 - Toggle between 0x5555 and 0xAAAA (test mode)
- **ADC_TEST_RAMP**
 - 16-bit ramp pattern (test mode)
- **ADC_TEST_SIN**
 - 8-point sine wave test pattern
- **ADC_TEST_PRBS**
 - 16-bit PRBS generated by a 23-bit PRBS pattern generator (test mode)
- **Ramp**
 - Data from a ramp generator. It is actually a 16-bit field, where the 6 most significant bits identify the channel and the 10 less significant bits are the samples of a ramp from 0x000 up to 0x3FF (i.e. 0 to 1023). It is so a 10-bit ramp with offset given by “channel*1024”. For channel 0, it is a counter from 0 to 1023; for channel 1, it is a counter from 1024 to 2047, and so on
- **IPE**
 - Not implemented
- **SquareWave**
 - Internally generated programmable square wave

参数 DCOffset

对于每个通道，将恒定的 DC 偏移（由 16 位 DAC 控制）添加到模拟输入，以在 ADC 的动态范围内调整信号基线的位置（即模拟输入的“零伏”）。

由于部件的公差，有必要校准偏移 DAC。校准是通过工厂测试完成的，通常不需要重新校准。然而，可以执行新的校准。校准参数存储在板的闪存中，并在通电时加载。每次写入或读取 DCOffset 参数时，内部逻辑会自动应用这些参数。

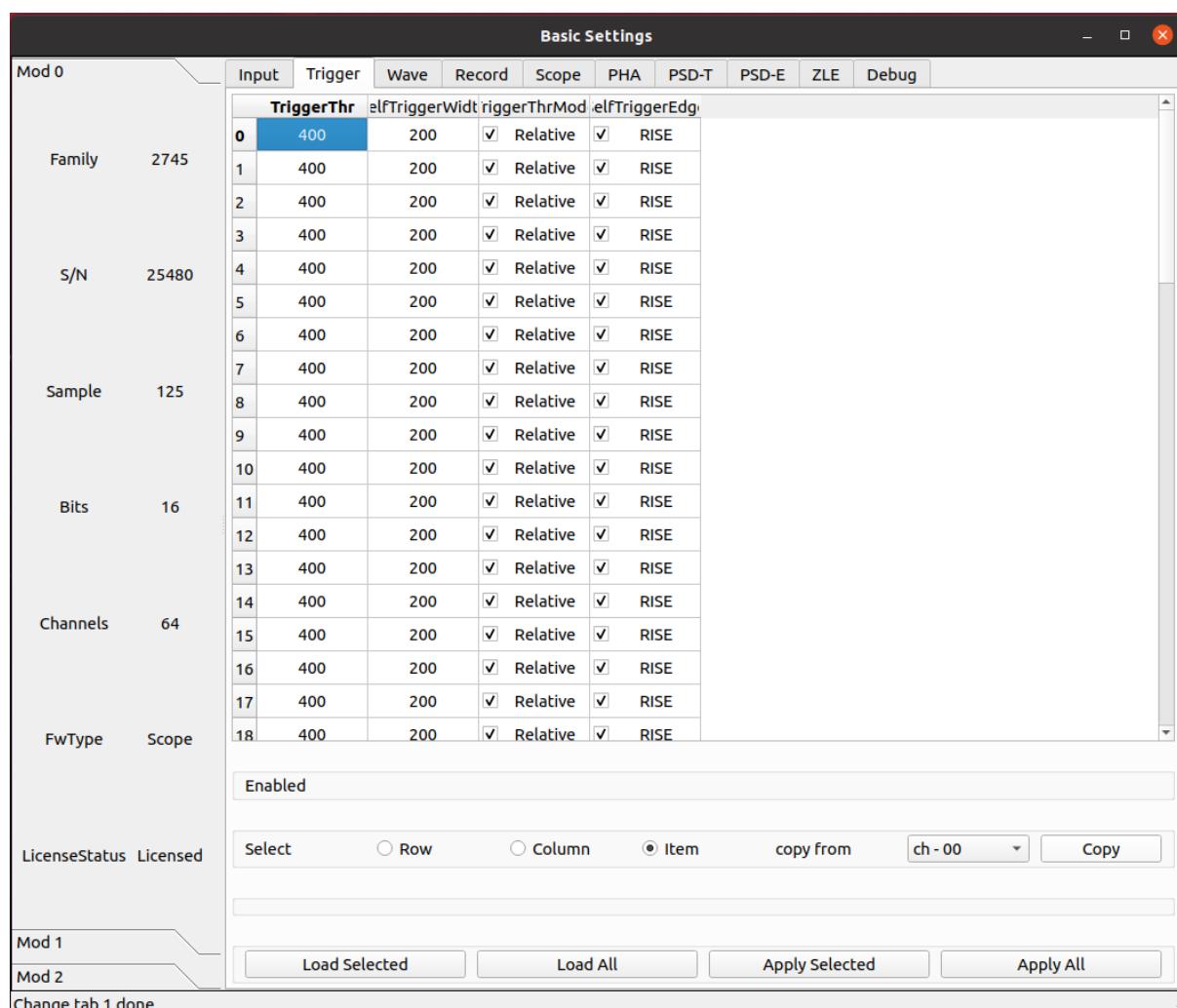
DCOffset 参数为数字，单位为满刻度的百分比。当 DCOffset 为 0 时，输入信号的基线处于 ADC 0。当 DCOffset 为 100 时，输入信号的基线处于 ADC \$2^{NBIT}-1\$。

参数 VGAGain

2745 特有。

以 0.5 dB 为步长设置可变增益放大器（VGA）的增益。参数设置每 16 个通道为一组，64 通道分为 4 组。最小可设置为 0，最大为 40。

7.1.2 触发



参数 TriggerThr

数字化模块的每个通道都有一个数字前沿甄别器，该甄别器具有可编程阈值，能够对输入脉冲进行自触发，并产生一个自触发信号（或过阈值信号），馈送道内部触发逻辑或输出端口。

此参数设置触发阈值。典型地，该值是相对于信号的基线的，并且阈值是 17 位带符号的整数；在这种情况下，当 DCoffset 参数改变时，阈值自动跟随基线。有时，设置阈值的绝对值是更好的策略，该阈值相对于 ADC 道址的范围；在这种情况下，阈值是无符号的整数。

参数 SelfTriggerWidth

产生自触发信号的数字前沿甄别器的输出可以在“线性”模式下使用，这意味着它会持续信号保持在阈值以上（或以下）的时间，从而充当“过阈值”信号，或者可以通过可编程门产生器，使其成为固定宽度的脉冲。门产生器是不可再触发的单稳态，当超过阈值时变高，在编程时间后变低。该参数定义了过阈值的固定宽度脉冲。

参数 TriggerThrMode

定义触发阈值是相对于基线还是绝对阈值。

- **Relative**

- The threshold is relative to the baseline and automatically follows it when the DCOffset parameter is changed.

- **Absolute**

- The threshold is absolute, referred to the ADC input range. It does not follow the DCOffset setting.

参数 SelfTriggerEdge

定义自触发必须在阈值上升或下降时产生。同样地，当信号高于或低于阈值时，过阈值信号将为 TRUE。

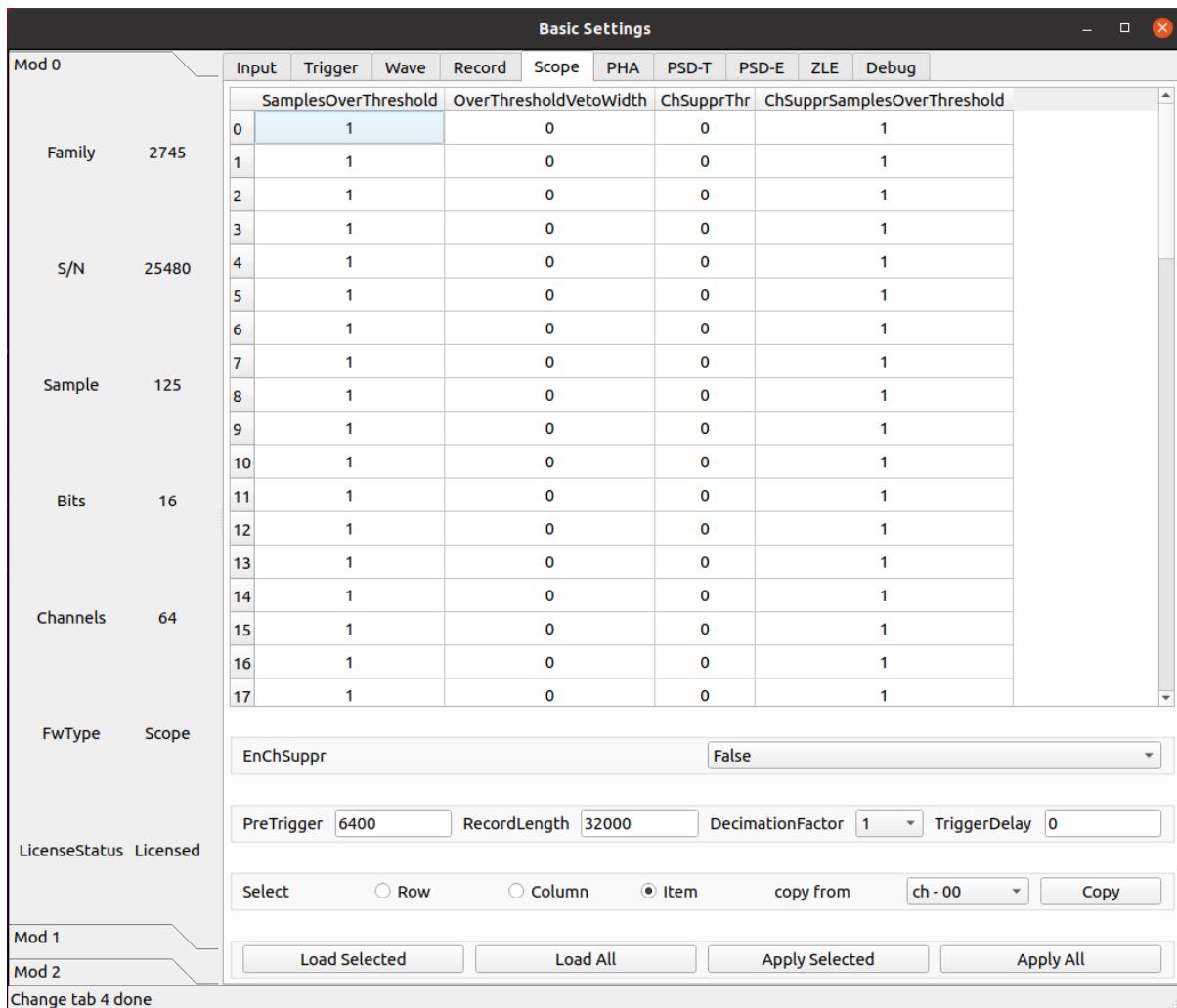
- **RISE**

- The trigger occurs on the rising crossing of the threshold and the OverThr is true when the signal is above the threshold

- **FALL**

- The trigger occurs on the falling crossing of the threshold and the OverThr is true when the signal is below the threshold

7.1.3 scope



参数 SamplesOverThreshold

超过阈值的样点数。

参数 OverThresholdVetoWidth

Veto width to discard triggers when crossing the threshold in the opposite direction to the trigger one

参数 ChSupperThr

通道零抑制阈值。与 TriggerThr 共享的配置参数 TriggerThrMode 和 SelfTriggerEdge。

单位为整数，ADC 道址。

参数 ChUpperSamplesOverThreshold

通道零抑制超过阈值的采样点数。

参数 EnChSupper

启用通道零抑制。

- **True**
 - Channel zero-suppression is enabled
- **False**
 - Channel zero-suppression is disabled

参数 PreTrigger

触发在波形中的位置之前的时间（即预触发窗口的大小）。波形的实际大小将自动四舍五入到最接近的允许值。通过读回参数可以得到确切的数值。

单位为时间， ns

参数 RecordLength

波形大小（即采集窗口的大小）。波形的实际大小将自动四舍五入到最接近的允许值。通过读回参数可以得到确切的数值。记录时间长度取决于降频设置。

单位为时间， ns

参数 DecimationFactor

设置应用于模块标称采样频率的抽取因子。如果启用，则参数 RecordLength、PreTrigger 和 TriggerDelay 按照标称采样计算采样点数，实际两个采样点的间隔为抽取因子设置的时间间隔。

- **1**
 - Decimation disabled (default)
- **2**
 - Sampling Frequency / 2
- **4**
 - Sampling Frequency / 4
- **8**
 - Sampling Frequency / 8
- **16**
 - Sampling Frequency / 16
- **32**
 - Sampling Frequency / 32
- **64**
 - Sampling Frequency / 64
- **128**
 - Sampling Frequency / 128

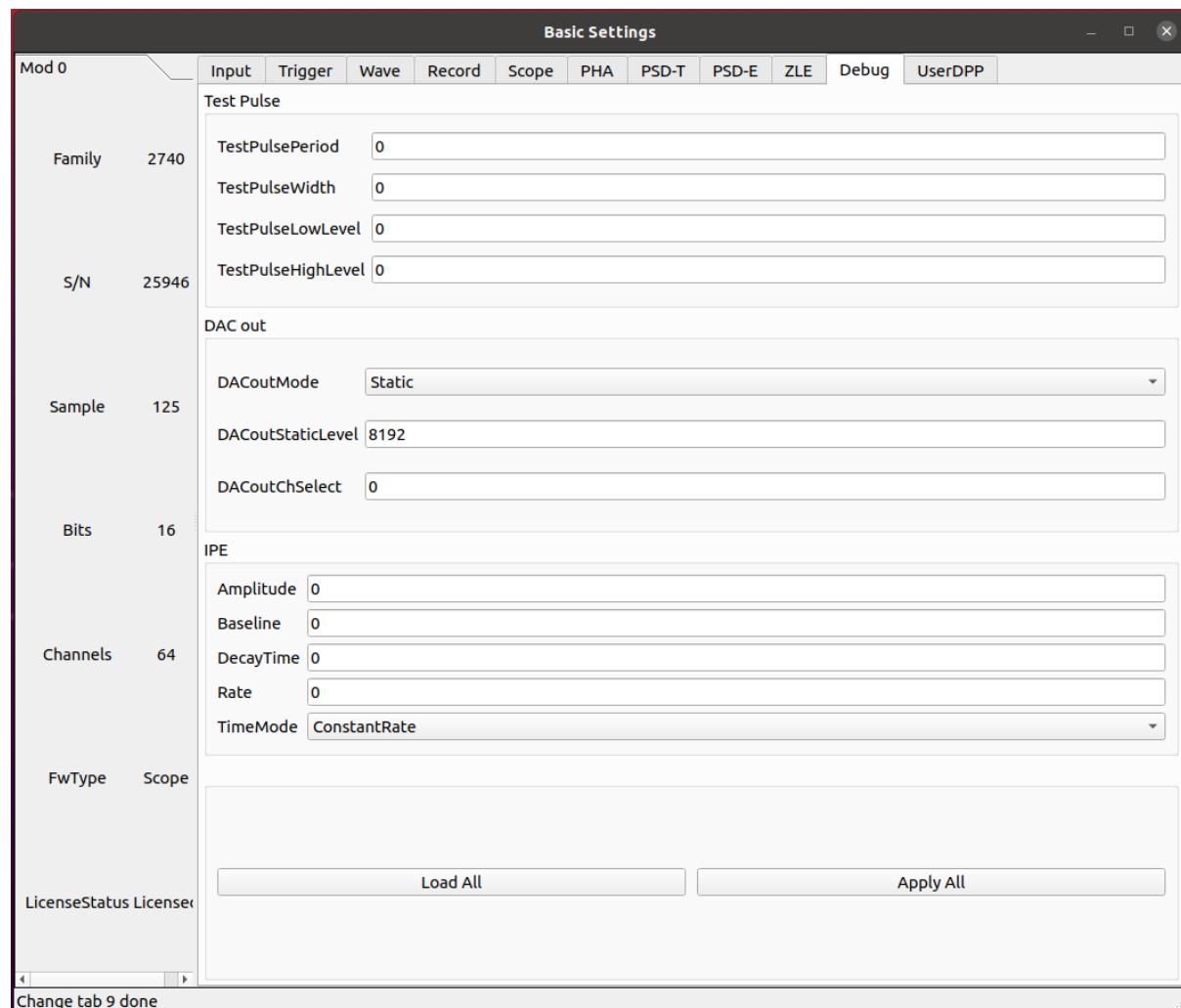
- 256
 - Sampling Frequency / 256
- 512
 - Sampling Frequency / 512
- 1024
 - Sampling Frequency / 1024

参数 TriggerDelay

表示添加到采集触发器延迟的时间。此参数可用于获取在触发位置之后开始的窗口。

单位为时间, ns

7.1.4 诊断



参数 TestPulsePeriod

测试脉冲是一种可编程方波，可用作内部周期性触发器（主要用于测试目的）或在 TRGOUT 和 GPIO 输出上生成逻辑测试脉冲（TTL 或 NIM）。此参数设置测试脉冲的周期。

单位为时间， ns

参数 TestPulseWidth

测试脉冲的宽度（信号保持高电平的时间）。

单位为时间， ns

参数 TestPulseLowLevel

以 ADC 道址表示的测试脉冲低电平

参数 TestPulseHighLevel

以 ADC 道址表示的测试脉冲高电平

参数 DACoutMode

选择要在前面板 DAC LEMO 口输出发送的信号类型。

- **Static**
 - DAC output stays at a fixed level, given by the DACoutStaticLevel parameter
- **Ramp**
 - The DAC output is driven by a 14-bit counter
- **Sin5MHz**
 - The DAC output is a sine wave at 5 MHz with fixed amplitude
- **Square**
 - Square wave with period and width set by TestPulsePeriod and TestPulseWidth and amplitude between TestPulseLowLevel and TestPulseHighLevel.
- **IPE**
 - Not implemented
- **ChInput**
 - The DAC reproduces the input signal received by one input channel, selected by the DACoutChSelect parameter
- **MemOccupancy**
 - Level of the memory occupancy (not yet implemented)
- **ChSum**
 - The DAC reproduces the “analog” sum of all the digitizer inputs (not yet implemented)
- **OverThrSum**
 - The DAC output is proportional to the number of channels that are currently above the threshold

参数 DACoutStaticLevel

当 DACoutMode = Static 时, 此参数设置 DAC 输出的 14 位电平。

参数 DACoutChSelect

当 DACoutMode = ChInput 时, DAC 输出由该参数选择的通道的输入信号。

参数 IPEAmplitude

The new digitizers are equipped with an Internal Pulse Emulator capable of generating exponential pulses. This parameter determines the amplitude of the pulse.

Unit of Measure: ADC counts

参数 IPEBaseline

Sets the offset of the exponential pulses generated by the Internal Pulse Emulator.

Unit of Measure: ADC counts

参数 IPEDecayTime

Sets the decay time of the exponential pulses generated by the Internal Pulse Emulator.

Unit of Measure: ns

参数 IPERate

Sets the rate of the exponential pulses generated by the Internal Pulse Emulator.

Unit of Measure: Hz

参数 IPETimeMode

Selectes the time distribution of the Internal Pulse Emulator.

- ConstantRate

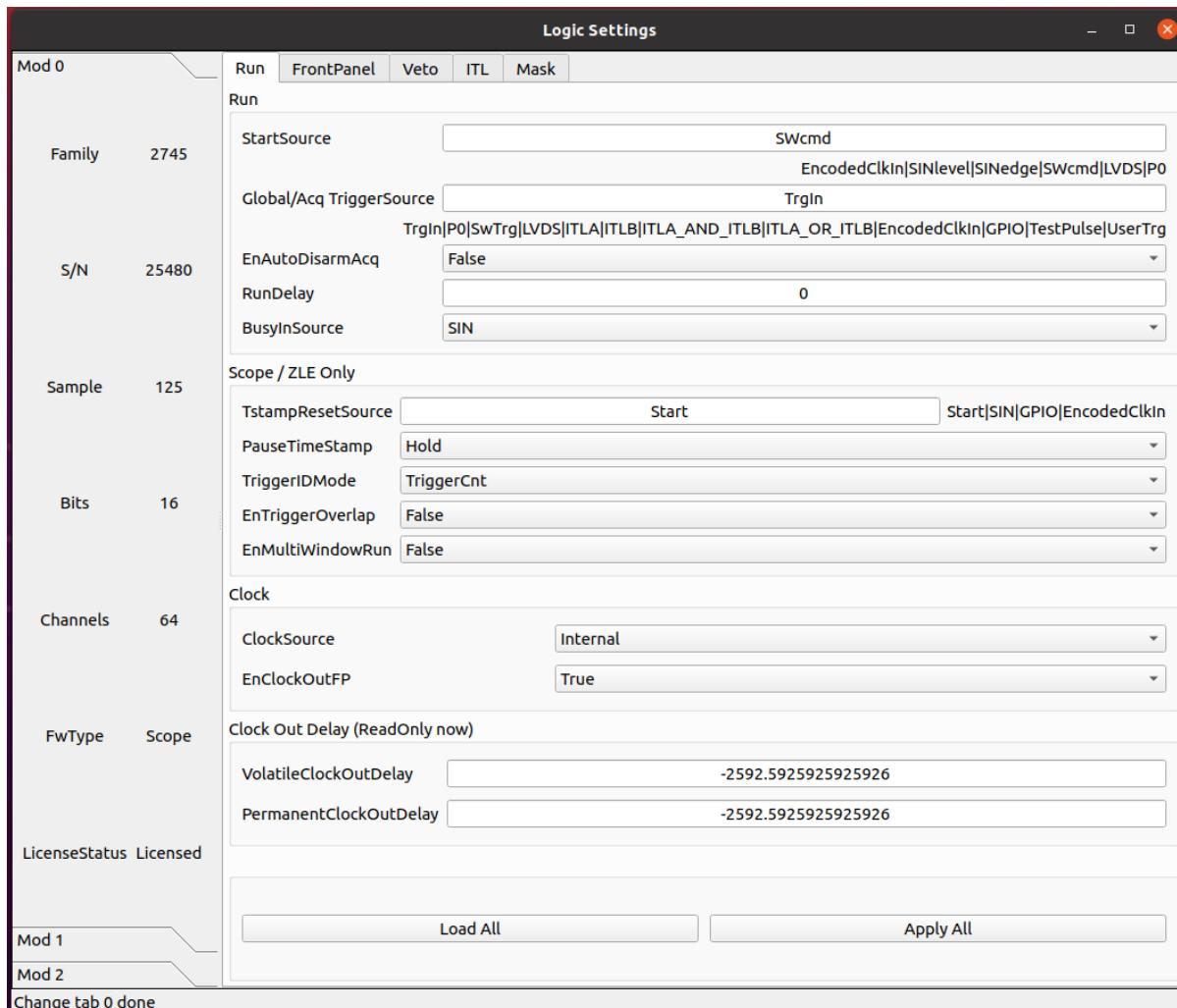
- Pulse shapes are constant over time. It is possible to set the frequency using the IPERate parameter

- Poissonian

- The pulse rate follows a Poisson distribution. The average frequency value can be configured using the IPERate parameter

7.2 逻辑参数配置

7.2.1 运行



参数 StartSource

Defines the source for the start of run. Multiple options are allowed, separated by “|” .

- **EncodedClkIn**

- Start from CLK-IN/SYNC connector on the front panel. This is a 4-pin connector (LVDS signals) used to propagate the reference clock (typ. 62.5 MHz) and a Sync signal. The rising edge of the Sync starts the acquisition, that lasts until the Sync returns low (falling edge).

- **SINlevel**

- Start from SIN (1=run, 0=stop)

- **SINedge**

- Start from SIN (rising edge = run; stop from SW)

- **SWcmd**

- Start from SW

- **LVDS**

- Start from LVDS
- **FirstTrigger**
 - Start on 1st trigger (stop from SW)
- **P0**
 - Start from P0 (backplane)

参数 AcqTriggerSource

Defines the source for the Acquisition Trigger, which is the signal that opens the acquisition window and saves the waveforms in the memory buffers. Multiple options are allowed, separated by “|” .

- **TrgIn**
 - Front Panel TRGIN
- **P0**
 - Trigger from P0 (backplane)
- **SwTrg**
 - Software trigger
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers
- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (encoded CLK-IN trigger)
- **GPIO**
 - Front Panel GPIO
- **TestPulse**
 - Internal Test Pulse
- **UserTrg**
 - User custom trigger source

参数 EnAutoDisarmAcq

When enabled, the Auto Disarm option disarms the acquisition at the stop of run. When the start of run is controlled by an external signal, this option prevents the digitizer to restart without the intervention of the software.

- **True**
 - The acquisition is automatically disarmed after the stop. It is therefore necessary to rearm the digitizer (with the relevant command sent by the software) before starting a new run.
- **False**
 - The acquisition is not disarmed after the stop. Multiple transition of the start signal will produce multiple runs.

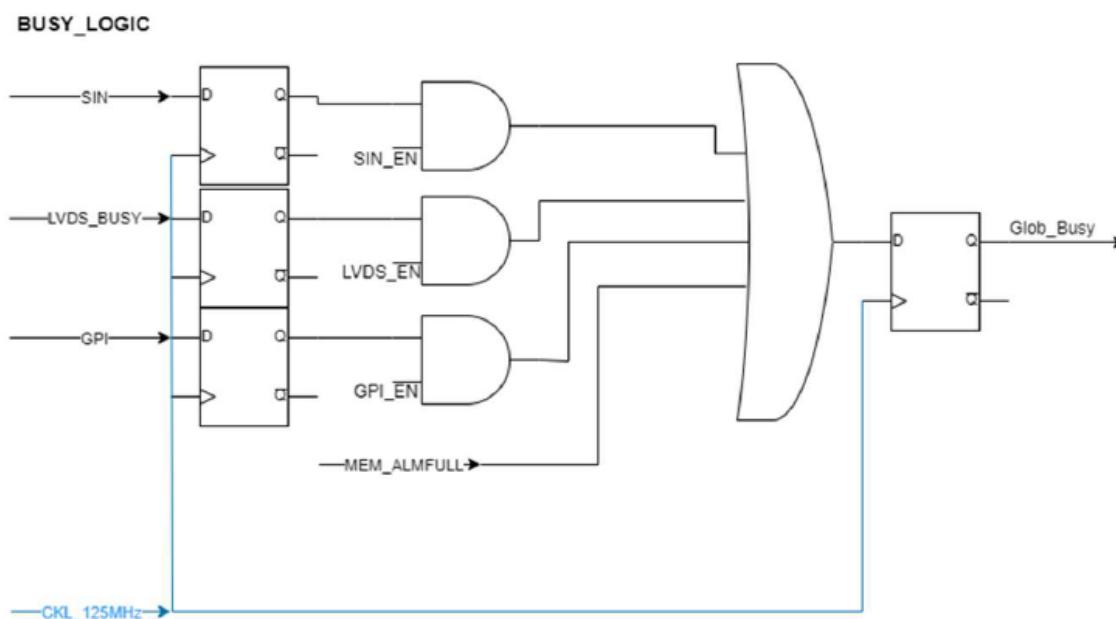
参数 RunDelay

When the start of run is controlled by a RUN signal that is propagated in daisy chain between the boards (for instance through the ClkIn- ClkOut or SIN-GPIO sync chain), it is necessary to compensate for the propagation delay and let the boards start exactly at the same time. The RunDelay parameter allows the start of the acquisition to be delayed by a given number of clock cycles with respect to the rising edge of the RUN signal. Assuming that the propagation delay is 2 cycles, the RunDelay setting will be 0 for the last board in the chain, 2 for the previous one, and so on up 2x(NB-1) for the first one.

Unit of Measure: ns

参数 BusyInSource

In a multi-board system, it might be necessary to prevent one board to accept a new trigger while another board is full and thus unable to accept the same trigger. For this reason, each board can generate a Busy signal to notify that it is unable to get a new trigger. If the busy/veto mechanism has some latency, it is advisable to generate the busy slightly before the digitizer become full. For this purpose, it is possible to assert the busy output when the acquisition memory reaches a certain level of occupancy (internally managed). The OR of the busy signals is typically used to stop the global trigger. It is possible to get the individual busy signals from each board and make an external OR logic or connect the boards with cables to propagate the Busy along the chain. Each board makes an OR between its internal busy and the busy input signal coming from the previous board, thus having a global Busy at the end of the line. This parameter defines the source of the Busy Input (schematized in the figure below)



- **Disabled**
 - The Busy is given by the Internal Busy only (Memory full or almost full)
- **SIN**
 - Busy input from SIN on front panel
- **GPIO**
 - Busy input coming from GPIO on front panel, used as a simple input. It is also possible to use GPIO as a wired OR (bidirectional). In this mode, the Busy line goes high as soon as one board drives it high. All the boards can read the Busy line and use it as a veto for the trigger
- **LVDS**
 - LVDS trgin

参数 TstampResetSource

Defines the source of the timestamp reset. Multiple options are allowed, separated by “|” . The timestamp of the board (internal counter running at 125 MHz) is typically reset at the start of each run, which corresponds to the “zero” of the timestamps. In Multi-board systems, the synchronization of the clock and RUN signals allows event data coming from different boards to be merged and correlated by the time stamp. However, it is possible to configure different ways to control the reset of the time stamp in the cases where it is necessary to synchronize it with an external global time stamping system.

- **Start**
 - Time stamp reset at the start of run
- **SIN**
 - SIN input
- **GPIO**
 - GPIO used as input
- **EncodedClkIn**
 - Not implemented (encoded in CLK-IN/SYNC)

参数 PauseTimeStamp

Allows the time stamp to either stop or run during the pauses of the acquisition

- **Hold**
 - The timestamp stops while pausing the acquisition
- **Run**
 - The timestamp runs while pausing the acquisition

参数 TriggerIDMode

The event data packet contains a 24-bit identifier called TriggerID. This can be the total trigger counter, the saved event counter or a pattern coming from the LVDS I/Os.

- **TriggerCnt**

- The Event triggerID is associated to the total trigger counter. This is a 24-bit counter that is reset at the start of run and increased with every received trigger, including those ones that are not accepted. In this mode, events coming from multiple boards can be correlated by the triggerID that is supposed to be synchronized. There might be gaps due to lost triggers.

- **EventCnt**

- The Event triggerID is a sequential number of the saved event. In this case, there are no gaps in the sequence, but it is not guaranteed that the trigger ID of multiple boards are aligned, thus it is not possible to use it for data correlation.

- **LVDSpattern**

- The triggerID is taken from the 16 LVDS inputs at the time of the trigger arrival. The user can provide an external trigger pattern to correlate the event data between boards or even with other readout electronics

参数 EnTriggerOverlap

Allows a trigger occurring within the acquisition window of a previous trigger to be either accepted or rejected. When accepted, the previous window is prematurely closed and the new window immediately opened, without any dead time between the two.

- **True**

- Triggers with overlapped acquisition windows are accepted.

- **False**

- Triggers with overlapped acquisition windows are not accepted. The rejected triggers are counted by the total trigger counter, so that the trigger-ID in the event header allows for tracing the rejected triggers.

参数 EnMultiWindowRun

When the acquisition start and stop are controlled by an external “RUN” signal (e.g. feeding SIN), it is possible to configure the digitizer to work in two different modes:

The RUN signal acts as a start (rising edge) and stop (falling edge). Therefore, multiple transitions of the RUN signal cause multiple runs (provided that the Auto Disarm option is disabled). At every start of run, the timestamp is reset, and all the statistics and counters are cleared. Typically, the software produces different output files.

The RUN signal acts as “enable” of the acquisition: once the digitizer has been armed, the first rising edge of RUN starts the acquisition. When RUN goes down, the acquisition is “paused” rather than stopped. This means that all data and statistics are frozen, and the timestamp can be either stopped or left running, depending on the PauseTimeStamp parameter. The RUN signal can toggle multiple times within the same acquisition. The stop of the acquisition will be done by a software command. It is necessary to disarm and rearm the acquisition before starting a new run with the rising edge of the RUN signal.

- **True**

- MultiWindow run is enabled. The RUN signal acts as start (first rising edge) and pause (subsequent falling edges) for the acquisition. The stop of the acquisition is always given by a software command

- **False**

- The RUN signal acts as start and stop for the acquisition

参数 ClockSource

This is the source of the system clock. Multiple options are not allowed

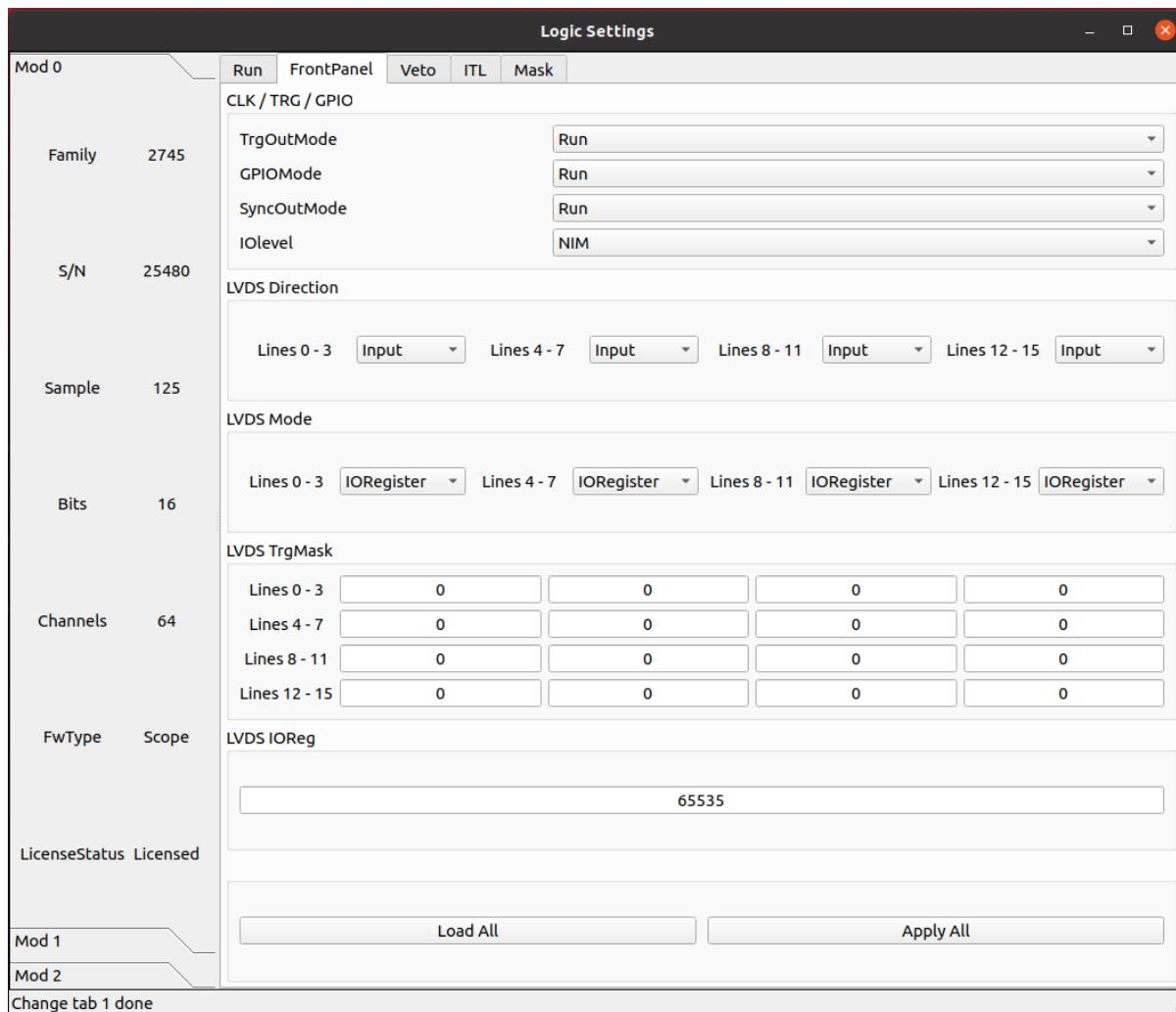
- **Internal**
 - Local oscillator, 62.5 MHz
- **FPClkIn**
 - Front Panel Clock input

参数 EnClockOutFP

Enables clock output on Front Panel for the daisy chain propagation of the clock between multiple boards.

- **True**
 - Enabled
- **False**
 - Disabled

7.2.2 模块前面板



参数 TrgOutMode

Selects the signal that is routed to the TRGOOUT output. Multiple options are not allowed.

- **Disabled**
 - TRGOOUT output disabled
- **TrgIn**
 - Propagation of Front Panel TRGIN (TRGOOUT is a replica, with some delay, of the TRGIN signal)
- **P0**
 - Propagation of P0 trigger
- **SwTrg**
 - Software trigger
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (propagation of the Encoded CLK-IN trigger)
- **Run**
 - Propagation of the RUN signal (acquisition start/stop), before applying the delay given by the Run-Delay parameter
- **RefClk**
 - Monitor of the 62.5 MHz clock (used for phase alignment)
- **TestPulse**
 - Internal Test Pulse
- **Busy**
 - Busy of the board
- **UserTrgout**
 - Trgout coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal
- **SyncIn**
 - SyncIn signal
- **SIN**
 - SIN connector signal
- **GPIO**
 - GPIO connector signal
- **LBinClk**
 - Internal Logic B clock signal
- **AcceptTrg**
 - Accepted triggers signal
- **TrgClk**
 - Trigger clock signal

参数 GPIOMode

Selects the signal that is routed to the GPIO, when this is used as output. Multiple options are not allowed. The GPIO on the front panel is a bidirectional signal that can be used in three different ways:

As independent board output (each board drives its own GPIO)

As a shared input for the boards: the signal is driven high (= 1) or low (= 0) by an external source and connected in “short circuit” among multiple boards using “T” connectors at the inputs. The GPIO is not internally terminated, thus it is necessary to put a 50 Ohm terminator at the end of the line (last “T” of the chain)

As a shared bidirectional line, making a “wired OR”. One or more boards can simultaneously drive the signal high (= 1). If no board drives the GPIO, it remains low (= 0). All boards can read back the signal. It is necessary to put a 50 Ohm terminator at both ends of the line (first and last “T” of the chain). This mode can be used to generate, for instance, the global Busy and Veto logic for multiple boards.

- **Disabled**

- GPIO disabled

- **TrgIn**

- Propagation of Front Panel TRGIN (GPIO is a replica, with some delay, of the TRGIN signal)

- **P0**

- Propagation of P0 trigger

- **SIN**

- Propagation of SIN

- **LVDS**

- LVDS trgin

- **ITLA**

- Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**

- Internal Trigger Logic B: combination of channel self-triggers

- **ITLA_AND_ITLB**

- Second level Trigger logic making the AND of ITL A and B

- **ITLA_OR_ITLB**

- Second level Trigger logic making the OR of ITL A and B

- **EncodedClkIn**

- Not implemented (propagation of the Encoded CLK-IN trigger)

- **SwTrg**

- Software trigger

- **Run**

- Propagation of RUN

- **RefClk**

- Monitor of the 62.5 MHz clock (used for phase alignment)

- **TestPulse**

- Internal Test Pulse

- **Busy**
 - Busy of the board
- **UserGPO**
 - GPO coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal

参数 SyncOutMode

In a multi-board system, it can be useful to propagate a synchronous signal together with the clock (to synchronize the start of the run, for example) on CLK OUT front panel connector. This parameter defines which signal must be sent out. Multiple options are not allowed.

- **Disabled**
 - SyncoutMode is disabled
- **SyncIn**
 - SyncIn signal (if provided with clkIn on CLK IN connector)
- **TestPulse**
 - Internal Test Pulse
- **IntClk**
 - Internal 62.5 MHz clock (for test purposes)
- **Run**
 - Propagation of RUN signal
- **User**
 - User custom SyncoutMode

参数 IOlevel

Sets the electrical logic level of the LEMO I/Os (TRGIN, SIN, TRGOUT, GPIO).

Note that TRGIN and SIN are internally terminated to 50 Ohm, while GPIO and TRGOUT require the termination to 50 Ohms at the receiver

- **NIM**
 - NIM logic (0 = 0V, 1 = -0.8V, that is -16mA)
- **TTL**
 - Low Voltage TTL logic (0 = 0V, 1 = 3.3V)

参数 LVDSDirection

Assigns the direction to a quartet of LVDS I/Os.

- **Input**

- The LVDS lines of the relevant quartet are used as input. The relevant LED on the front panel is OFF.

- **Output**

- The LVDS lines of the relevant quartet are used as output. The relevant LED on the front panel lights-up.

参数 LVDSMode

The digitizer is equipped with 16 LVDS I/Os that can be programmed to be inputs or outputs by groups of 4 (quartets), depending on the LVDSDirection parameter. Once the direction has been selected, it is possible to select the functionality of the LVDS lines, individually for each quartet.

- **SelfTriggers**

- This option is available only when the LVDS are set as outputs. Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by the LVDSTrgMask parameter(16 independent masks, one per LVDS line)

- **Sync**

- Whatever is the direction of the quartet, the 4 lines are rigidly assigned to specific acquisition signals:
0 = Run 1 = Trigger 2 = Busy 3= Veto It is possible to implement a daisy chain distribution of these signals using one quartet as input and another one as output

- **IORRegister**

- The LVDS lines of the quartet are statically controlled by the LVDSIORReg parameter. Use the SetValue function to set the relevant LVDS lines when programmed as output. Use GetValue to read the status of the LVDS lines when programmed as inputs.

- **User**

- User custom.

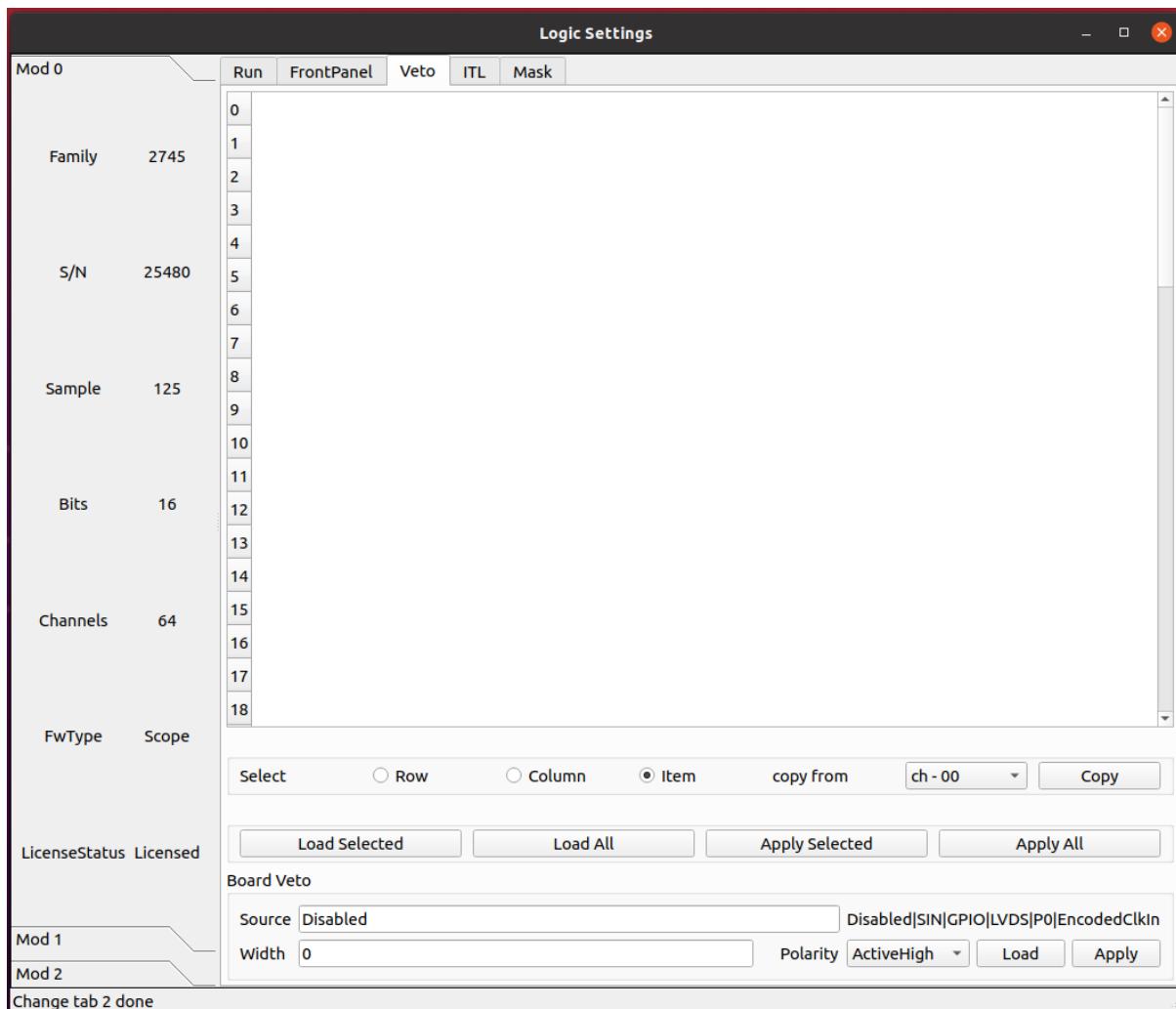
参数 LVDSTrgMask

Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by this parameter. There are 16 independent masks, one per LVDS line. Note that the trigger mask assignment does not imply the LVDS direction and mode settings. It is therefore necessary to set the Direction = Output and Mode = SelfTriggers to use the Self-Trigger propagation to the LVDS I/Os.

参数 LVDSIORReg

Set the status of the LVDS I/O for the quartets when they are programmed to be output and Mode = IORRegister. This parameter reads out the status of the quartets in the case the LVDS I/O are programmed as inputs (possibly externally driven).

7.2.3 反符合



参数 VetoSource

Defines the source for the Veto, which is the signal that inhibits the acquisition trigger. Multiple options are allowed, separated by “|”. The VETO signal can be either active high or low, depending on the VetoPolarity parameter. When active low, it acts as a GATE for the trigger. It is possible to stretch the duration of the VETO by means of the parameter VetoWidth.

- **Disabled**
 - VETO is always OFF
- **SIN**
 - SIN on the front panel
- **GPIO**
 - GPIO on the front panel (used as input)
- **LVDS**
 - LVDS trgin
- **P0**
 - P0 (signal from the backplane)

- **EncodedClkIn**
 - Not implemented (encoded CLK-IN veto)

参数 VetoWidth

Whatever is the source of the VETO signal, it is possible to stretch the duration of the veto up to a given time by means of a re-triggerable monostable. When 0, the monostable is disabled and the veto lasts as long as the selected source is active.

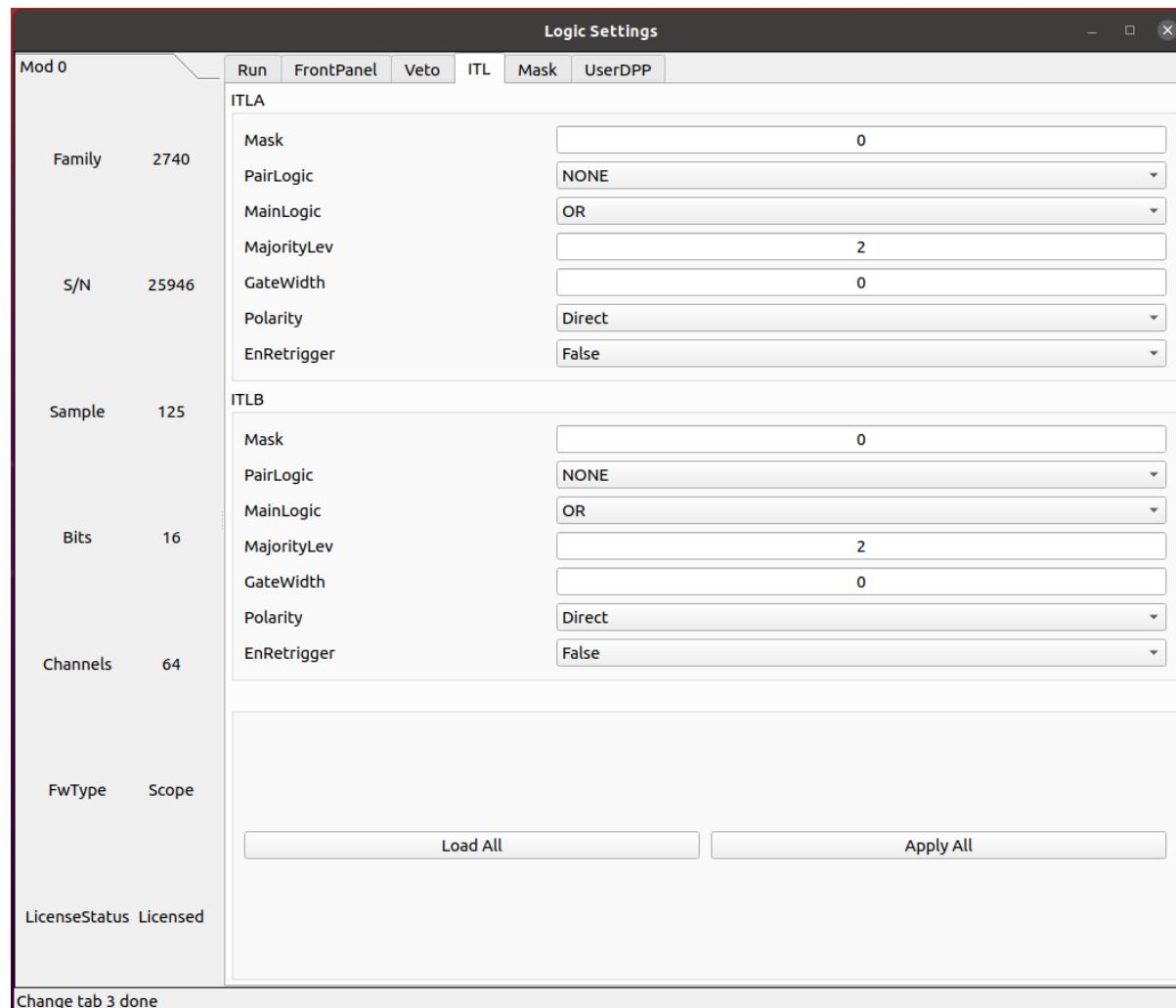
Unit of Measure: ns

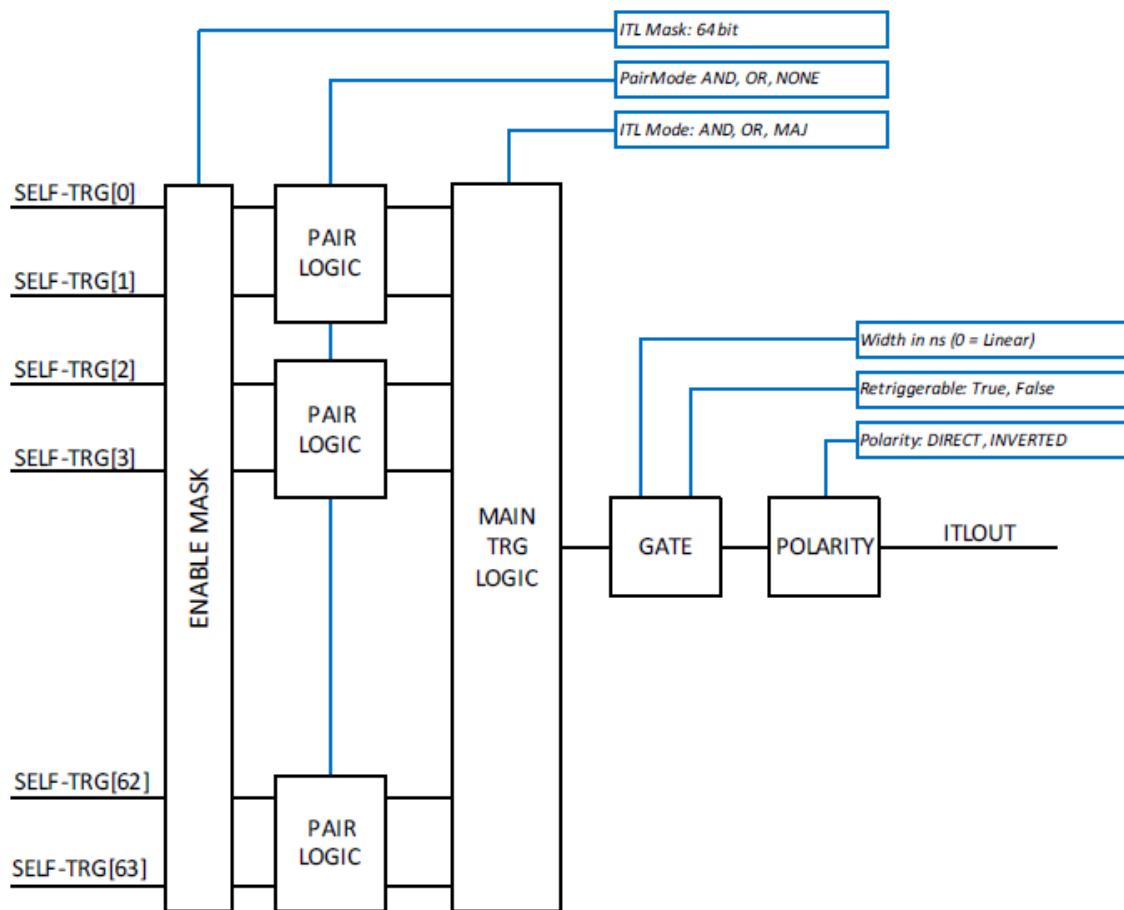
参数 VetoPolarity

Defines the polarity of the Veto

- **ActiveHigh**
 - Veto is active high. The signal acts as an “Inhibit” for the trigger
- **ActiveLow**
 - Veto is active low. The signal acts as a “Gate” the trigger

7.2.4 ITL 逻辑





参数 ITLA/BMask

Enable Mask at the input of the ITLA/B.

参数 ITLA/BPairLogic

Pairs of channels can be combined with an OR or AND before feeding in the Main trigger Logic. This is typically used in the readout of tubes or scintillator bars, where the two ends are read in coincidence, for instance in position sensitive detectors (the coincidence window will be set by the SelfTriggerWidth parameter). When the AND/OR logic is applied, the two outputs of the Pair Logic blocks are identical.

Note that they are counted twice in the following Majority logic. If the Pair Logic is disabled ("NONE" option), the block is transparent, and the two outputs are just a replica of the inputs.

- **OR**
 - Both Pair Logic Outputs = OR of two consecutive self-triggers
- **AND**
 - Both Pair Logic Outputs = AND of two consecutive self-triggers
- **NONE**
 - Outputs = Inputs

参数 ITLA/BMainLogic

Each channel of the digitizer feature a digital bipolar triangular filter discriminator with programmable rise time and threshold able to self-trigger on the input pulses and generate a self-trigger signal. In DPP Mode, the channels acquire independently, so the channel self-trigger is used locally to acquire a waveform. The trigger threshold is then referred to the bipolar triangular filter, and the threshold crossing arms the event selection. The trigger fires at the zero crossing of the time filter signal. The user can see the derivative trace on the signal inspector. It is also possible to combine all the self-triggers of the board, according to a specific trigger logic. There are two independent logic blocks, ITLA and ITLB. Their output can be used separately to feed, for instance, AcqTrigger and TrgOut, or combined in a second level trigger logic to implement more complex trigger schemes. Therefore, the ITLs can either generate the local acquisition trigger, common to all the channels, for the acquisition of the waveform, or propagate the signal outside, through the TRGOUT, thus making it possible to combine triggers of multiple boards in an external trigger logic, that eventually feeds back the TRGIN of the digitizers. Each ITL is made of an input enable mask (64 bits, one per channel), an optional pairing logic that combines the self triggers of two consecutive channels (e.g. paired coincidence) and the main trigger logic that combines the 64 selftriggers with an OR, AND or Majority logic. The output can be linear (no stretching) or reshaped by a programmable gate generator, either re-triggerable or not and finally programmed for polarity (direct or inverted).

- **OR**
 - ITLOUT = masked OR of channel self-triggers
- **AND**
 - ITLOUT = masked AND of channel self-triggers
- **Majority**
 - ITLOUT = masked Majority of channel self-triggers

参数 ITLA/BMajorityLev

Defines the majority level of the Main Logic of the ITL A/B block. The majority output is calculated at every clock cycle, and it becomes TRUE when $Nch \geq MajLev$, where Nch is the number of self-triggers active in that clock cycle and MajLev is the programmed majority level.

Note that when the Pair Logic is used to combine the self triggers two by two (AND/OR), each pair produces two identical signals that will be counted twice in the majority level.

参数 ITLA/BGateWidth

Width of the gate generator at the output of the ITLA/B block.

Unit of Measure: ns

参数 ITLA/BPolarity

Polarity of the gate generator output.

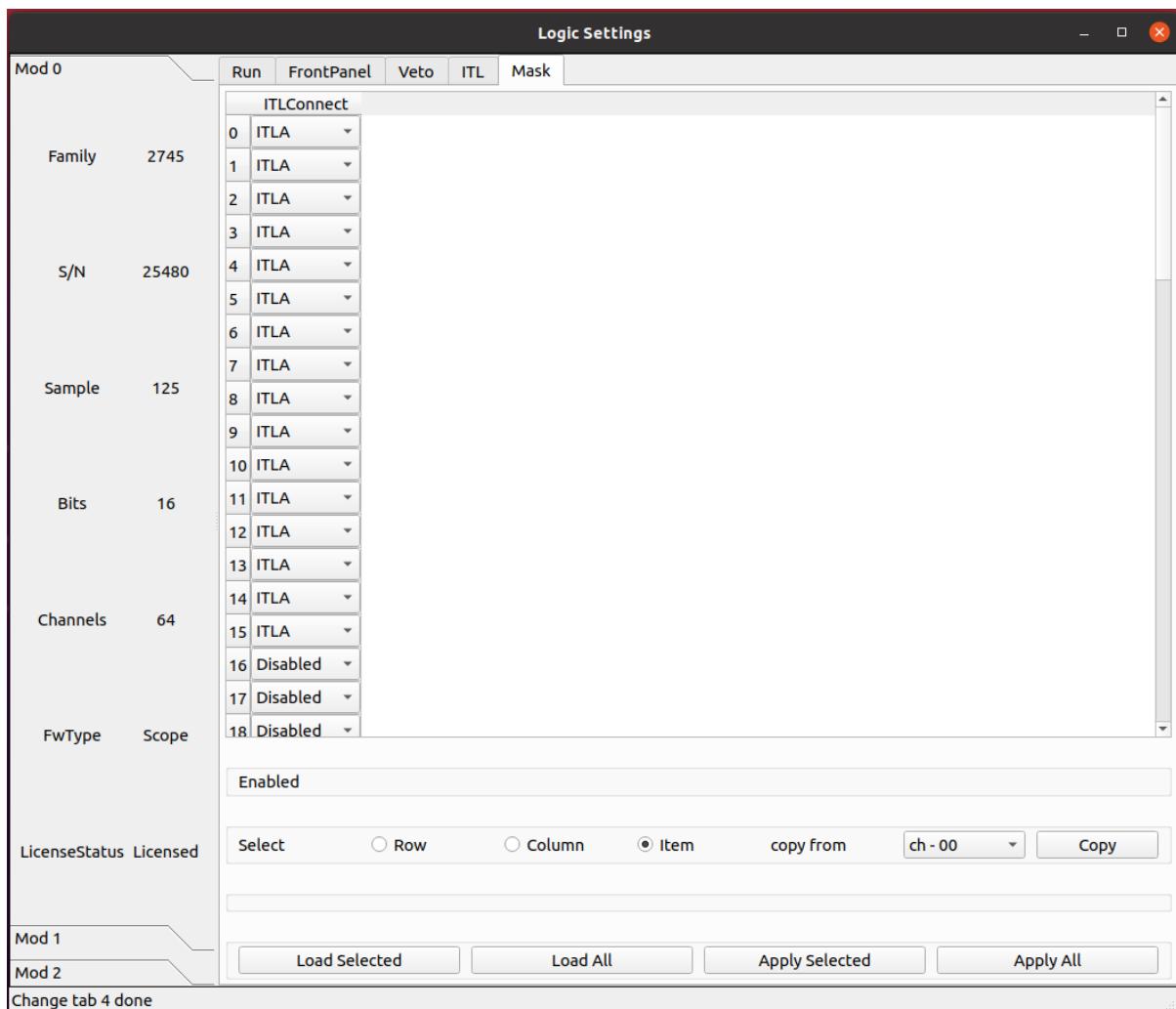
- **Direct**
 - Direct polarity
- **Inverted**
 - Inverted polarity

参数 ITLA/BEnRetrigger

Set the ITLA/B to be retriggerable.

- **True**
 - The ITLA/B is retriggerable
- **False**
 - The ITLA/B is not retriggerable

7.2.5 延迟展宽



parameter ITLConnect

Alternative to ITLAMask, ITLBMask. Determines if the channel partecipate in ITLA or ITLB

- **Disabled**
 - The channel is disabled
- **ITLA**
 - The channel participates in ITLA logic block
- **ITLB**

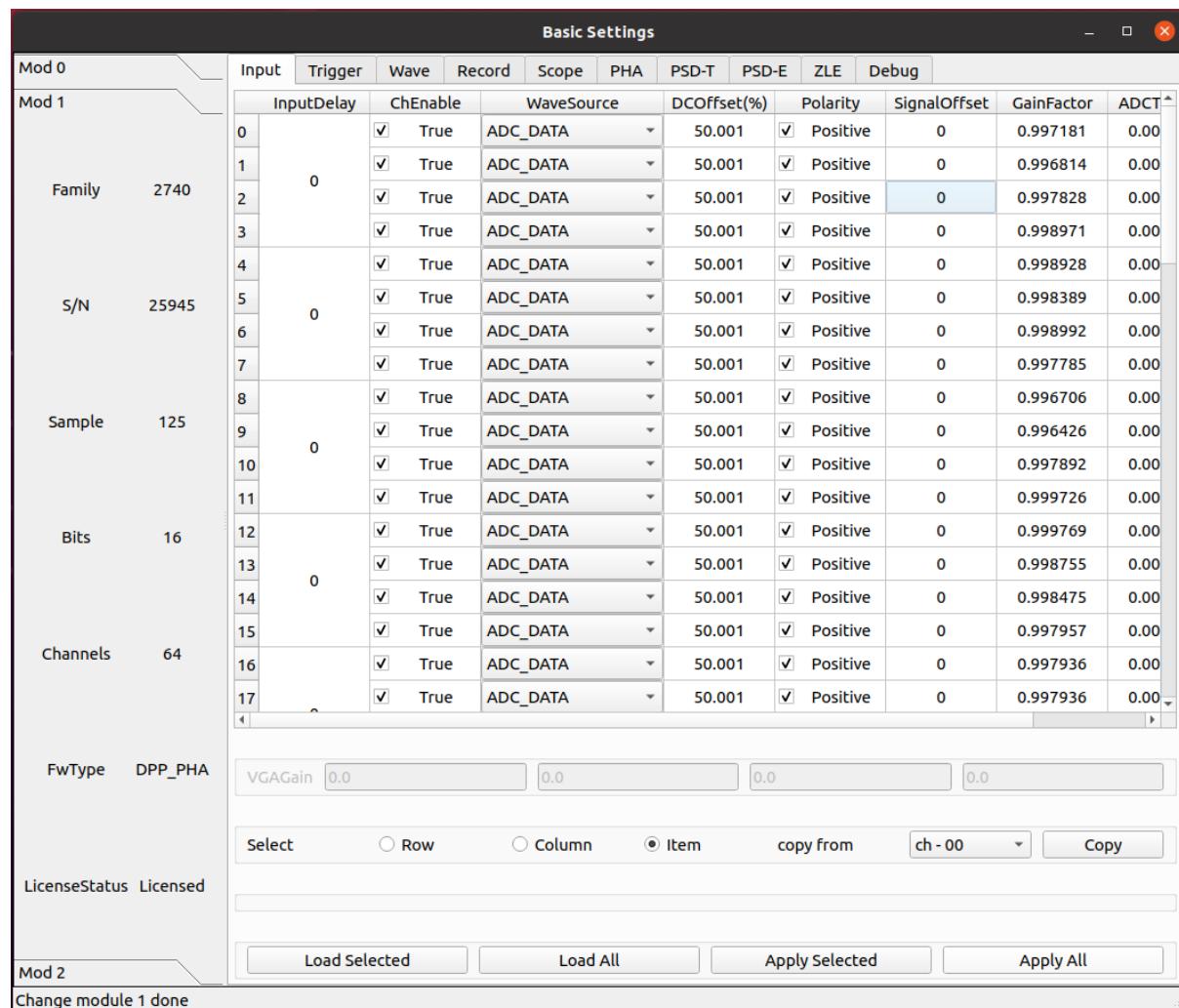
- The channel participates in ITLB logic block

CHAPTER 8

PHA 固件

8.1 基本参数配置

8.1.1 输入信号



参数 ChGain

仅限 x2730.

设置可变增益放大器 (VGA) 的增益。

Unit of Measure: dB

参数 InputDelay

设置输入延迟，单位为采样点。

x2745/x2740 该值设置每 4 个通道共用一个相同配置。

参数 ChEnable

独立设定每个通道是否开启使用。如果通道不启用，它不提供任何数据，同时它的自触发也关闭。

参数 WaveSource

在正常模式下，采集的波形来源于模拟输入的 A/D 转换产生的 ADC 采样序列。出于测试目的，可以用内部数据生成器替换 ADC 数据。

- **ADC_DATA**
 - Data from the ADC (normal operating mode)
- **ADC_TEST_TOGGLE**
 - Toggle between 0x5555 and 0xAAAA (test mode)
- **ADC_TEST_RAMP**
 - 16-bit ramp pattern (test mode)
- **ADC_TEST_SIN**
 - 8-point sine wave test pattern
- **ADC_TEST_PRBS**
 - 16-bit PRBS generated by a 23-bit PRBS pattern generator (test mode)
- **Ramp**
 - Data from a ramp generator. It is actually a 16-bit field, where the 6 most significant bits identify the channel and the 10 less significant bits are the samples of a ramp from 0x000 up to 0x3FF (i.e. 0 to 1023). It is so a 10-bit ramp with offset given by “channel*1024”. For channel 0, it is a counter from 0 to 1023; for channel 1, it is a counter from 1024 to 2047, and so on
- **IPE**
 - Not implemented
- **SquareWave**
 - Internally generated programmable square wave

参数 DCOffset

对于每个通道，将恒定的 DC 偏移（由 16 位 DAC 控制）添加到模拟输入，以在 ADC 的动态范围内调整信号基线的位置（即模拟输入的“零伏”）。

由于部件的公差，有必要校准偏移 DAC。校准是通过工厂测试完成的，通常不需要重新校准。然而，可以执行新的校准。校准参数存储在板的闪存中，并在通电时加载。每次写入或读取 DCOffset 参数时，内部逻辑会自动应用这些参数。

DCOffset 参数为数字，单位为满刻度的百分比。当 DCOffset 为 0 时，输入信号的基线处于 ADC 0。当 DCOffset 为 100 时，输入信号的基线处于 ADC $2^{\{NBIT\}} - 1$ 。

参数 Polarity

设置输入脉冲的极性。

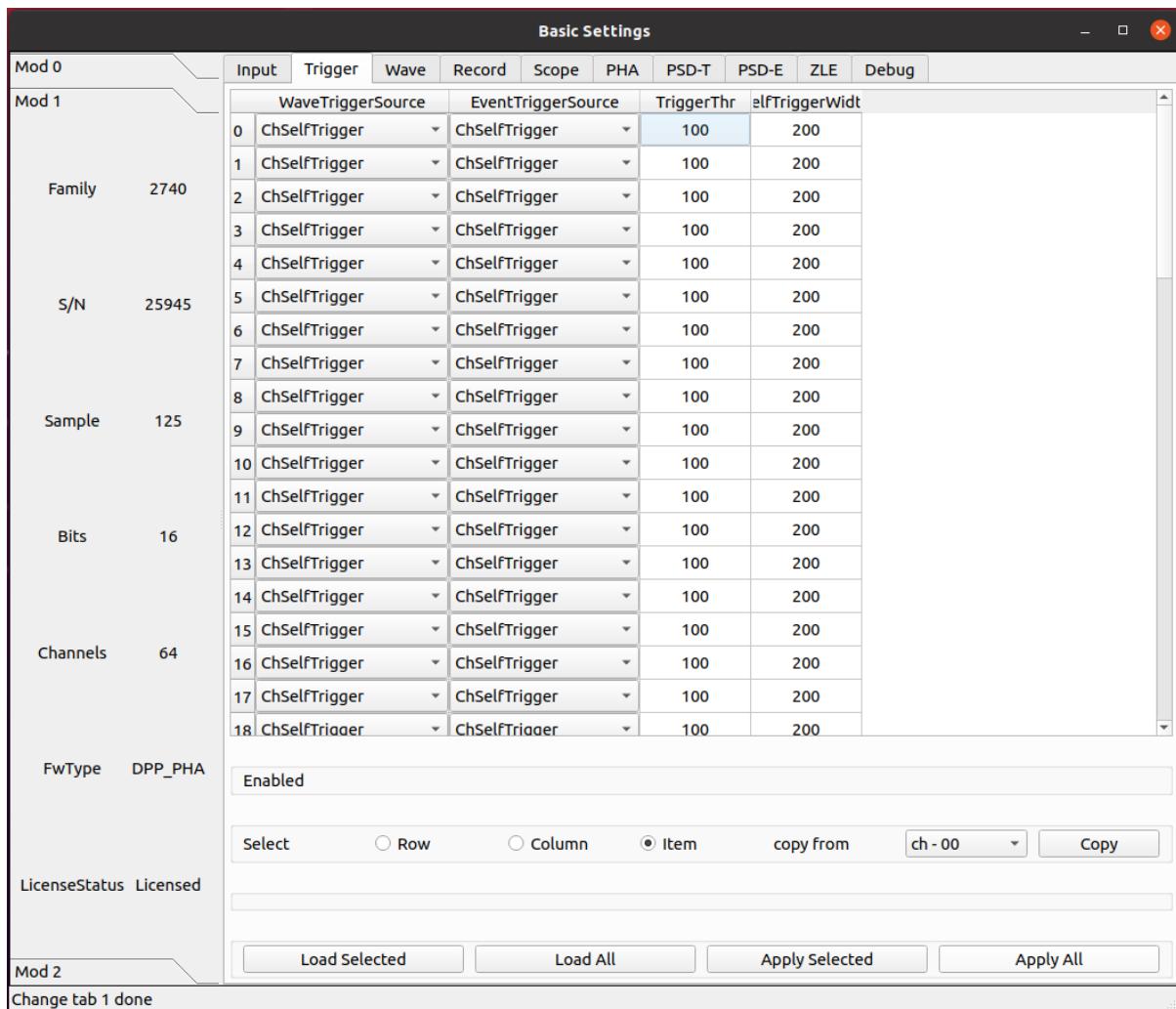
- Positive
 - Positive polarity
- Negative
 - Negative polarity

参数 VGAGain

2745 特有。

以 0.5 dB 为步长设置可变增益放大器（VGA）的增益。参数设置每 16 个通道为一组，64 通道分为 4 组。最小可设置为 0，最大为 40。

8.1.2 触发



参数 WaveTriggerSource

允许设置波形的触发源。

设置此参数意味着获得包括波形和相关时间戳以及能量信息的事件。

- **Disabled**
 - No trigger source enabled for the waveform
- **Ch64Trigger**
 - One (or more) channel self-trigger can generate a trigger for a waveform
- **ChSelfTrigger**
 - Channel self-trigger can generate a trigger for a waveform
- **SwTrg**
 - Software Trigger can generate a trigger for a waveform
- **ADCOverSaturation**
 - ADC Oversaturation can generate a trigger for a waveform
- **ADCUnderSaturation**
 - ADC Undersaturation can generate a trigger for a waveform

- ADC Undersaturation can generate a trigger for a waveform
- **ExternalInhibit**
 - Inhibit can generate a trigger for a waveform
- **TRGIN**
 - External TRGIN can generate a trigger for a waveform
- **GlobalTriggerSource**
 - Acquisition Trigger Source (the same of the Scope mode) can generate a trigger for a waveform
- **LVDS**
 - A signal on the LVDS connectors can generate a trigger for a waveform
- **ITLA**
 - Internal Trigger Logic A can generate a trigger for a waveform
- **ITLB**
 - Internal Trigger Logic B can generate a trigger for a waveform

参数 EventTriggerSource

允许设置时间、能量 (T-E) 事件的触发源。设置此参数意味着获取包括时间戳和能量信息的事件。

- **Disabled**
 - No trigger source enabled for the T-E event
- **Ch64Trigger**
 - One (or more) channel self-trigger can generate a trigger for a T-E event
- **ChSelfTrigger**
 - Channel self-trigger can generate a trigger for a T-E event
- **SwTrg**
 - Software Trigger can generate a trigger for a T-E event
- **TRGIN**
 - External TRGIN can generate a trigger for a T-E event
- **GlobalTriggerSource**
 - Acquisition Trigger Source (the same of the Scope mode) can generate a trigger for a T-E event
- **LVDS**
 - A signal on the LVDS connectors can generate a trigger for a T-E event
- **ITLA**
 - Internal Trigger Logic A can generate a trigger for a T-E event
- **ITLB**
 - Internal Trigger Logic B can generate a trigger for a T-E event

参数 TriggerThr

相对于三角滤波之后的波形的设置阈值。

参数 SelfTriggerWidth

产生自触发信号的数字前沿甄别器的输出可以在“线性”模式下使用，这意味着它会持续信号保持在阈值以上（或以下）的时间，从而充当“过阈值”信号，或者可以通过可编程门产生器，使其成为固定宽度的脉冲。门产生器是不可再触发的单稳态，当超过阈值时变高，在编程时间后变低。该参数定义了过阈值的固定宽度脉冲。

8.1.3 波形

Basic Settings																
Mod 0		Input		Trigger		Wave		Record		Scope						
Mod 1		PreTrigger		RecordLength		Downsampling		Analog0		Analog1						
Family	2740	0	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		1	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		2	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		3	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		4	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
S/N	25945	5	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		6	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		7	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		8	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		9	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
Sample	125	10	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		11	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		12	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		13	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		14	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
Bits	16	15	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		16	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		17	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		18	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
		19	2000	32000	1	▼	ADCInput	▼	TimeFilter	▼	Trigger					
FwType	DPP_PHA															
LicenseStatus		Licensed														
Mod 2																
Change tab 2 done																
Load Selected				Load All				Apply Selected		Apply All						

参数 PreTrigger

波形中触发器位置之前的时间（即预触发窗口的大小）。

单位为时间， ns

参数 RecordLength

波形大小（即采集窗口的大小）。波形的实际大小将自动四舍五入到最接近的允许值。通过读回参数可以得到确切的数值。记录时间长度取决于下采样设置。

单位为时间， ns

参数 DownsamplingFactor

波形的下采样因子。

- 1
 - x1
- 2
 - x2
- 4
 - x4
- 8
 - x8

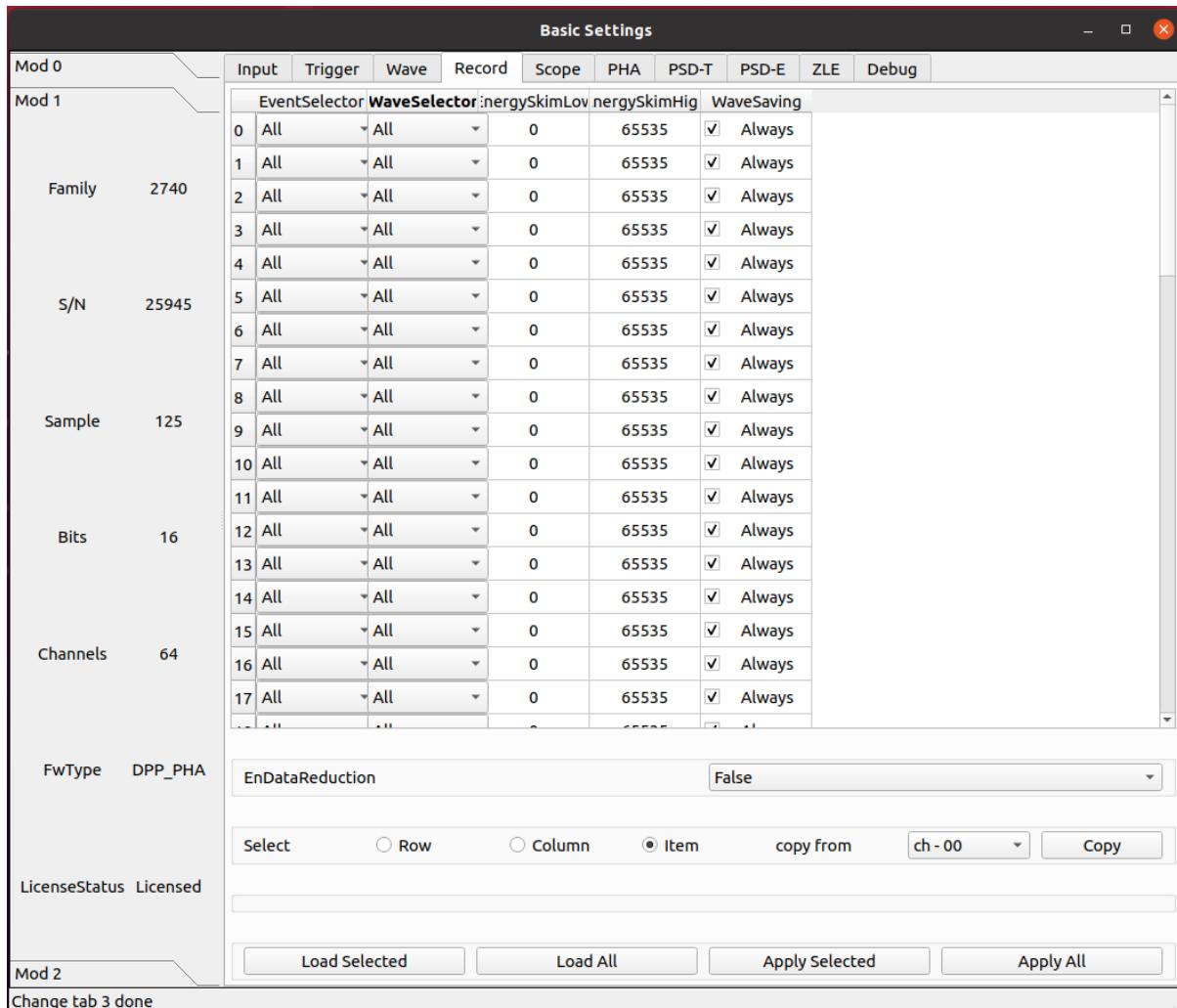
参数 Analog0/1

- ADCInput
 - ADC input probe
- TimeFilter
 - Time Filter probe
- EnergyFilter
 - Energy Filter probe
- EnergyFilterBaseline
 - Energy Filter Baseline
- EnergyFilterMinusBaseline
 - [Energy Filter – Baseline] probe

参数 Digital0/1/2/3

- **Trigger**
 - Trigger probe
- **TimeFilterArmed**
 - Time Filter Armed probe
- **ReTriggerGuard**
 - ReTrigger Guard probe
- **EnergyFilterBaselineFreeze**
 - Energy Filter Baseline Freeze probe
- **EnergyFilterPeaking**
 - Energy Filter Peaking probe
- **EnergyFilterPeakReady**
 - Energy Filter Peak Ready probe
- **EnergyFilterPileupGuard**
 - Energy Filter Pile Up Guard probe
- **EventPileUp**
 - Event Pile Up probe
- **ADCSaturation**
 - ADC Saturation probe
- **ADCSaturationProtection**
 - ADC Saturation Protection probe
- **PostSaturationEvent**
 - Post Saturation Event probe
- **EnergyFilterSaturation**
 - Energy Filter Saturation probe
- **AcquisitionInhibit**
 - Acquisition Inhibit probe

8.1.4 数据记录



参数 EventSelector

设置必须保存的事件。

- All
 - All events are saved
- PileUp
 - Only pileup events are saved
- EnergySkim
 - Save only the events in the Energy Skim range

参数 WaveSelector

设置必须保存的波形。

- **All**
 - All waves are saved
- **PileUp**
 - Only pileup waves are saved
- **EnergySkim**
 - Save only waves in the Energy Skim range

参数 EnergySkimLowDiscriminator

允许标记能量高于低舍弃阈值的事件。16 位。

参数 EnergySkimHighDiscriminator

允许标记能量低于高舍弃阈值的事件。16 位。

参数 WaveSaving

允许始终保存波形或仅根据请求保存波形。

- **Always**
 - Waveforms are always saved
- **OnRequest**
 - Waveforms are saved on request

参数 EnDataReduction

如果启用，2 个 words 压缩为一个 word 事件。

- **True**
 - Option enabled
- **False**
 - Option disabled

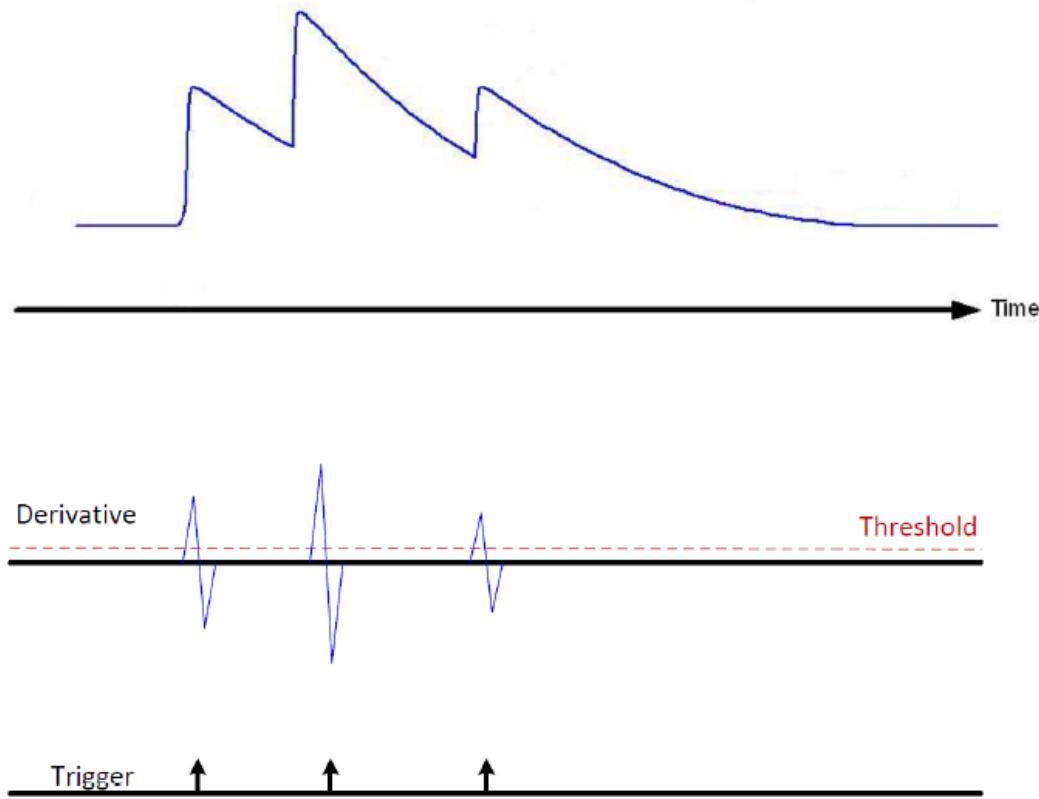
8.1.5 PHA 参数

Basic Settings											
Mod 0		Input	Trigger	Wave	Record	Scope	PHA	PSD-T	PSD-E	ZLE	Debug
Mod 1		TriggerTriangular	RetriggerGuard	PileupGuard	BaselineAvg	BaselineGuard	EnergyRiseTime	EnergyFlatTop	PoleZero	al	al
		0	296	504	960	Medium	0	5000	1000	50000	
		1	296	504	960	Medium	0	5000	1000	50000	
Family	2740	2	296	504	960	Medium	0	5000	1000	50000	
		3	296	504	960	Medium	0	5000	1000	50000	
		4	296	504	960	Medium	0	5000	1000	50000	
S/N	25945	5	296	504	960	Medium	0	5000	1000	50000	
		6	296	504	960	Medium	0	5000	1000	50000	
		7	296	504	960	Medium	0	5000	1000	50000	
Sample	125	8	296	504	960	Medium	0	5000	1000	50000	
		9	296	504	960	Medium	0	5000	1000	50000	
		10	296	504	960	Medium	0	5000	1000	50000	
		11	296	504	960	Medium	0	5000	1000	50000	
Bits	16	12	296	504	960	Medium	0	5000	1000	50000	
		13	296	504	960	Medium	0	5000	1000	50000	
		14	296	504	960	Medium	0	5000	1000	50000	
Channels	64	15	296	504	960	Medium	0	5000	1000	50000	
		16	296	504	960	Medium	0	5000	1000	50000	
		17	296	504	960	Medium	0	5000	1000	50000	
FwType	DPP_PHA										
LicenseStatus	Licensed										
Mod 2											
Change tab 5 done											
<input type="checkbox"/> Enabled											
Select <input type="radio"/> Row <input type="radio"/> Column <input checked="" type="radio"/> Item copy from ch - 00 <input type="button" value="Copy"/>											
<input type="button" value="Load Selected"/> <input type="button" value="Load All"/> <input type="button" value="Apply Selected"/> <input type="button" value="Apply All"/>											

参数 TriggerTriangular

基于三角形滤波信号来区分事件，三角形滤波信号的上升时间可以由用户定义。然后设置的触发阈值是相对于三角滤波信号的，过阈值点为事件选择提供判据。触发点定义为微分信号本身的过零点。此参数设置三角形滤波器的上升时间。

单位为时间， ns



参数 RetriggerGuard

在诸如来自 PMT 的快速信号的情况下，可能发生快速甄别信号中的可能过冲，从而导致再触发，从而可能出现伪堆积。此参数设置禁止再触发保护时间（单位为 ns）。

参数 PileupGuard

如果两个事件的间隔小于梯形持续时间，则相关梯形重叠。梯形持续时间定义为 RT+FT+PileUpGuard，其中 RT 是梯形上升时间，FT 是梯形平顶，PileUpGuard 在峰值时间结束时开始（请参见 PeakingPosition）。此参数允许设置梯形滤波堆积保护（单位：ns）。

参数 BaselineAvg

允许为能量滤波启用低频滤波器

- **Fixed**
 - Baseline fixed at 0
- **VeryLow**
 - Baseline samples for average = 16
- **Low**
 - Baseline samples for average = 64
- **MediumLow**
 - Baseline samples for average = 256
- **Medium**

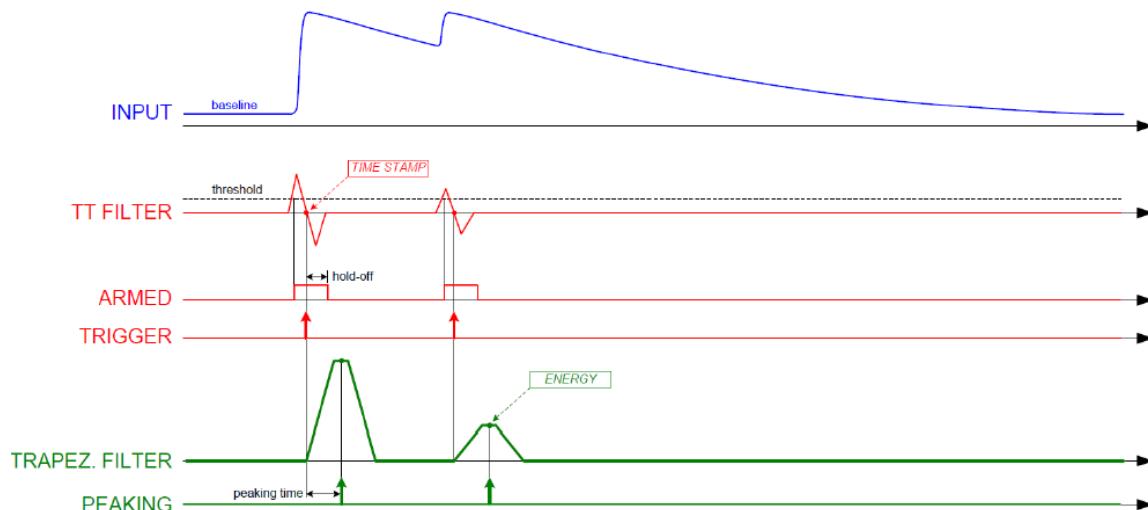
- Baseline samples for average = 1024
- **MediumHigh**
 - Baseline samples for average = 4096
- **High**
 - Baseline samples for average = 16384

参数 BaselineGuard

除了“基线平均值”，用户还可以设置“基线保持”或“基线保护”值，以冻结梯形末端以外的基线计算，从而减少基线计算中的噪声。此参数允许设置峰值后的梯形滤波基线保护（单位：ns）。

参数 EnergyRiseTime

使用梯形滤波评估能量值。与传统的模拟电路中一样，整形放大器能够将电荷敏感前置放大器的指数形状转换为高度与脉冲能量成比例的高斯形状，就像梯形滤波能够将其转换为幅度与输入脉冲能量成比例的梯形信号一样。在这种类比中，能量滤波上升时间对应于成型时间乘以因子 2/2.5。

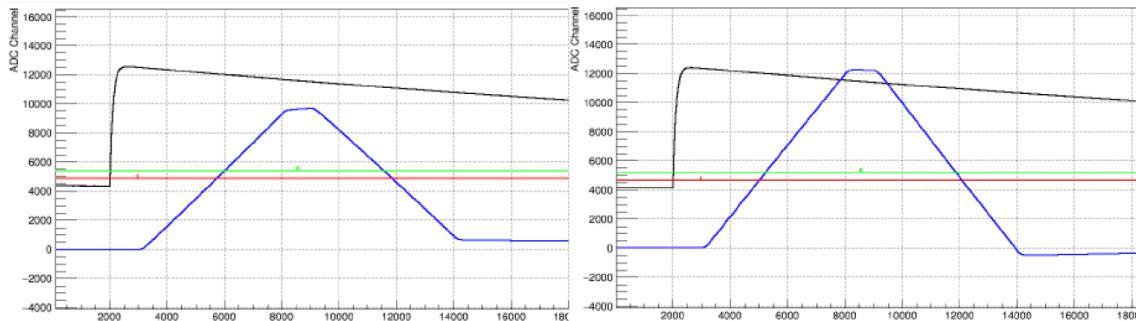


参数 EnergyFlatTop

输入脉冲的能量值被评估为梯形在其平顶区域中的高度。用户必须注意平顶确实是平的，并且峰值（即用于能量计算的样本）在平的区域中。此外，平顶和峰值的正确设置有助于正确评估能量，尤其是当涉及大体积探测器时，并且弹道亏损可能导致能量计算中的显著误差。在这种情况下，增加平顶持续时间并延迟峰值时间以等待完全电荷收集可能是实用的。此参数允许设置梯形平顶（以 ns 单位）。

参数 PoleZero

与整形放大器的高斯脉冲一样，梯形也需要精确的零点调整，以确保在下降沿结束时正确返回到基线。要正确设置零点，用户必须注意设置正确的梯形衰减时间值（也对应于输入衰减时间），以避免下冲或过冲效应。与脉冲衰减相比，当计数率高时，零点调整可以减少由于脉冲堆积而产生的信号伪影。



参数 PeakingPosition

以平顶的百分比 (%) 表示的梯形峰值位置。

步长为 1

参数 PeakingAvg

用于评估峰值的样本数。

- **OneShot**
 - 1 sample
- **LowAVG**
 - 4 samples
- **MediumAVG**
 - 16 samples
- **HighAVG**
 - 64 samples

参数 FineGain

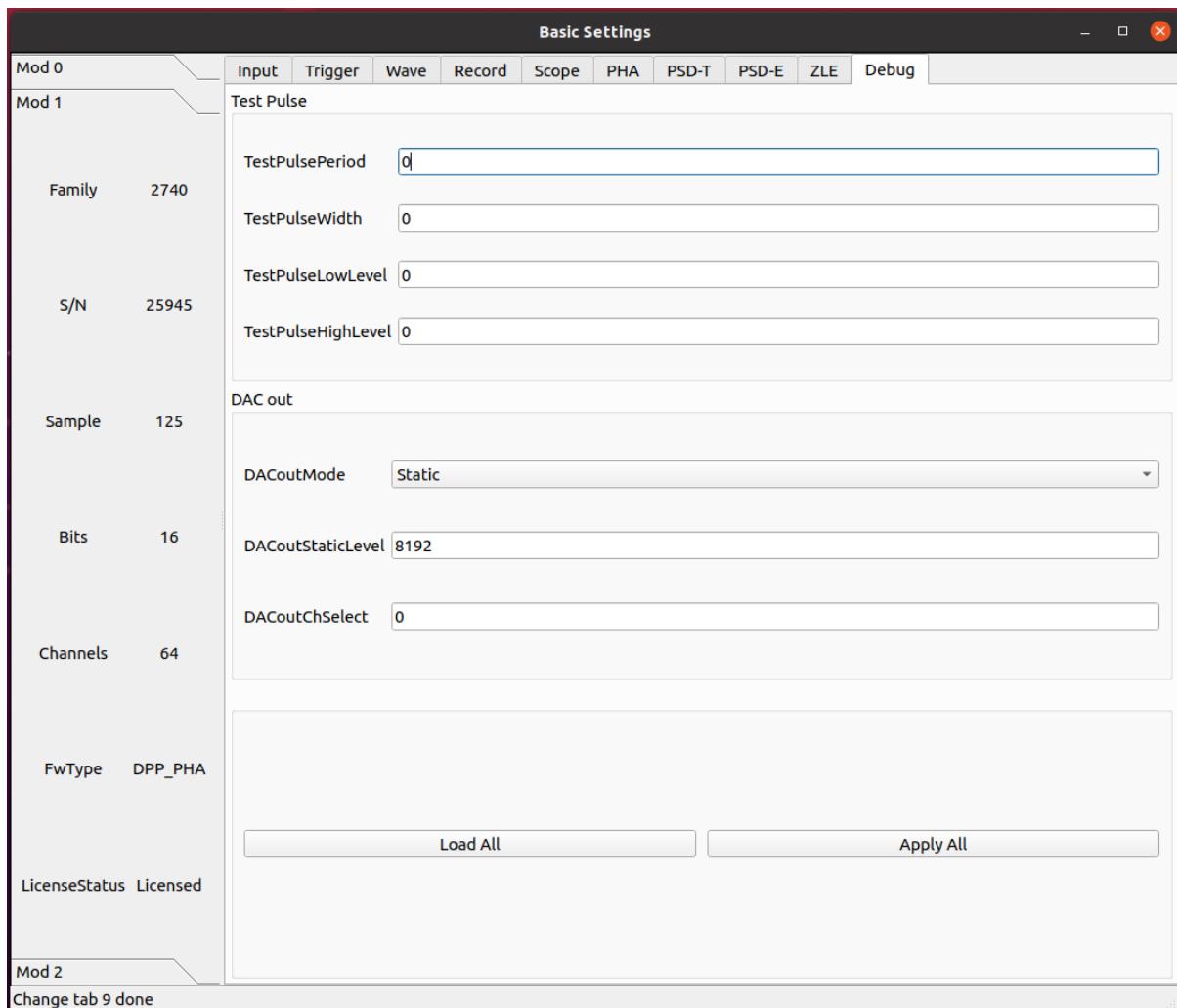
允许设置能量精细增益。能量精细增益是一个数字乘法因子，不会改变满量程范围。

参数 LFLimitation

为能量滤波启用低频滤波器

- **On**
 - Enabled
- **Off**
 - Disabled

8.1.6 诊断



参数 TestPulsePeriod

测试脉冲是一种可编程方波，可用作内部周期性触发器（主要用于测试目的）或在 TRGOUT 和 GPIO 输出上生成逻辑测试脉冲（TTL 或 NIM）。此参数设置测试脉冲的周期。

单位为时间，ns

参数 TestPulseWidth

测试脉冲的宽度（信号保持高电平的时间）。

单位为时间， ns

参数 TestPulseLowLevel

以 ADC 道址表示的测试脉冲低电平

参数 TestPulseHighLevel

以 ADC 道址表示的测试脉冲高电平

参数 DACoutMode

选择要在前面板 DAC LEMO 口输出发送的信号类型。

- **Static**
 - DAC output stays at a fixed level, given by the DACoutStaticLevel parameter
- **Ramp**
 - The DAC output is driven by a 14-bit counter
- **Sin5MHz**
 - The DAC output is a sine wave at 5 MHz with fixed amplitude
- **Square**
 - Square wave with period and width set by TestPulsePeriod and TestPulseWidth and amplitude between TestPulseLowLevel and TestPulseHighLevel.
- **IPE**
 - Not implemented
- **ChInput**
 - The DAC reproduces the input signal received by one input channel, selected by the DACoutChSelect parameter
- **MemOccupancy**
 - Level of the memory occupancy (not yet implemented)
- **ChSum**
 - The DAC reproduces the “analog” sum of all the digitizer inputs (not yet implemented)
- **OverThrSum**
 - The DAC output is proportional to the number of channels that are currently above the threshold

参数 DACoutStaticLevel

当 DACoutMode = Static 时, 此参数设置 DAC 输出的 14 位电平。

参数 DACoutChSelect

当 DACoutMode = ChInput 时, DAC 输出由该参数选择的通道的输入信号。

参数 IPEAmplitude

The new digitizers are equipped with an Internal Pulse Emulator capable of generating exponential pulses. This parameter determines the amplitude of the pulse.

Unit of Measure: ADC counts

参数 IPEBaseline

Sets the offset of the exponential pulses generated by the Internal Pulse Emulator.

Unit of Measure: ADC counts

参数 IPEDecayTime

Sets the decay time of the exponential pulses generated by the Internal Pulse Emulator.

Unit of Measure: ns

参数 IPERate

Sets the rate of the exponential pulses generated by the Internal Pulse Emulator.

Unit of Measure: Hz

参数 IPETimeMode

Selectes the time distribution of the Internal Pulse Emulator.

- ConstantRate

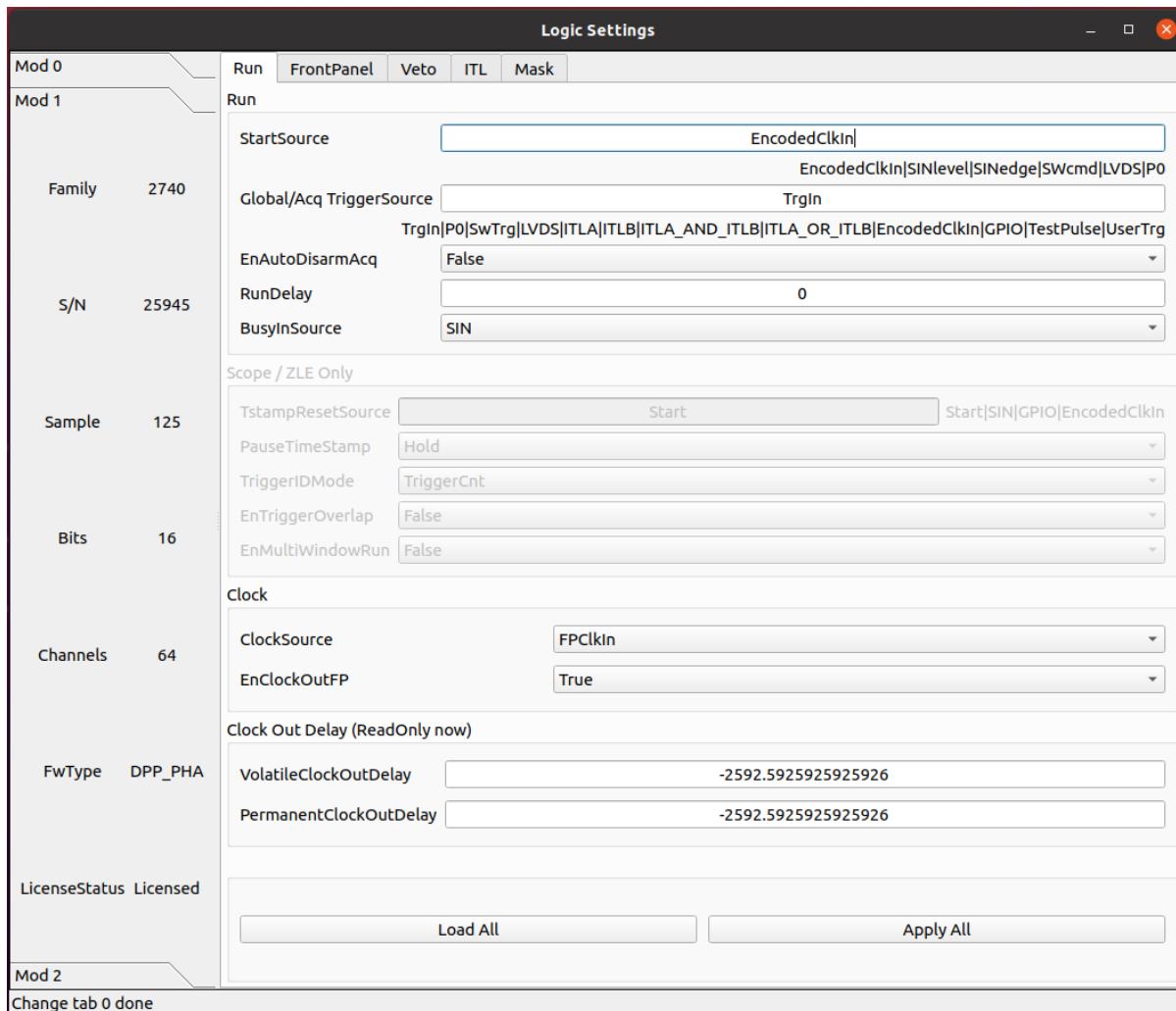
- Pulse shapes are constant over time. It is possible to set the frequency using the IPERate parameter

- Poissonian

- The pulse rate follows a Poisson distribution. The average frequency value can be configured using the IPERate parameter

8.2 逻辑参数配置

8.2.1 运行



参数 StartSource

Defines the source for the start of run. Multiple options are allowed, separated by “|” .

- **EncodedClkIn**
 - Start from CLK-IN/SYNC connector on the front panel. This is a 4-pin connector (LVDS signals) used to propagate the reference clock (typ. 62.5 MHz) and a Sync signal. The rising edge of the Sync starts the acquisition, that lasts until the Sync returns low (falling edge).
- **SINlevel**
 - Start from SIN (1=run, 0=stop)
- **SINedge**
 - Start from SIN (rising edge = run; stop from SW)
- **SWcmd**
 - Start from SW
- **LVDS**

- Start from LVDS
- **P0**
 - Start from P0 (backplane)

参数 GlobalTriggerSource

Defines the source for the Acquisition Trigger, which is the signal that opens the acquisition window and saves the waveforms in the memory buffers. Multiple options are allowed, separated by “|” .

- **TrgIn**
 - Front Panel TRGIN
- **P0**
 - Trigger from P0 (backplane)
- **SwTrg**
 - Software trigger
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers
- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (encoded CLK-IN trigger)
- **GPIO**
 - Front Panel GPIO
- **TestPulse**
 - Internal Test Pulse
- **UserTrg**
 - User custom trigger source

参数 EnAutoDisarmAcq

When enabled, the Auto Disarm option disarms the acquisition at the stop of run. When the start of run is controlled by an external signal, this option prevents the digitizer to restart without the intervention of the software.

- **True**
 - The acquisition is automatically disarmed after the stop. It is therefore necessary to rearm the digitizer (with the relevant command sent by the software) before starting a new run.
- **False**
 - The acquisition is not disarmed after the stop. Multiple transition of the start signal will produce multiple runs.

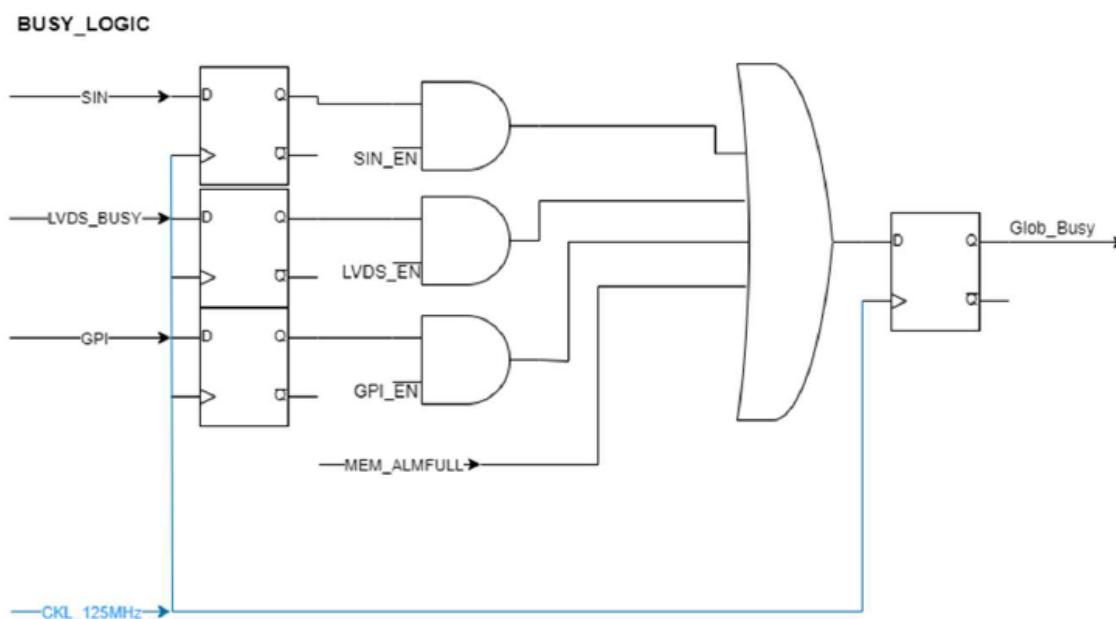
参数 RunDelay

When the start of run is controlled by a RUN signal that is propagated in daisy chain between the boards (for instance through the ClkIn- ClkOut or SIN-GPIO sync chain), it is necessary to compensate for the propagation delay and let the boards start exactly at the same time. The RunDelay parameter allows the start of the acquisition to be delayed by a given number of clock cycles with respect to the rising edge of the RUN signal. Assuming that the propagation delay is 2 cycles, the RunDelay setting will be 0 for the last board in the chain, 2 for the previous one, and so on up 2x(NB-1) for the first one.

Unit of Measure: ns

参数 BusyInSource

In a multi-board system, it might be necessary to prevent one board to accept a new trigger while another board is full and thus unable to accept the same trigger. For this reason, each board can generate a Busy signal to notify that it is unable to get a new trigger. If the busy/veto mechanism has some latency, it is advisable to generate the busy slightly before the digitizer become full. For this purpose, it is possible to assert the busy output when the acquisition memory reaches a certain level of occupancy (internally managed). The OR of the busy signals is typically used to stop the global trigger. It is possible to get the individual busy signals from each board and make an external OR logic or connect the boards with cables to propagate the Busy along the chain. Each board makes an OR between its internal busy and the busy input signal coming from the previous board, thus having a global Busy at the end of the line. This parameter defines the source of the Busy Input (schematized in the figure below)



- **Disabled**
 - The Busy is given by the Internal Busy only (Memory full or almost full)
- **SIN**
 - Busy input from SIN on front panel
- **GPIO**
 - Busy input coming from GPIO on front panel, used as a simple input. It is also possible to use GPIO as a wired OR (bidirectional). In this mode, the Busy line goes high as soon as one board drives it high. All the boards can read the Busy line and use it as a veto for the trigger
- **LVDS**
 - LVDS trgin

参数 ClockSource

This is the source of the system clock. Multiple options are not allowed

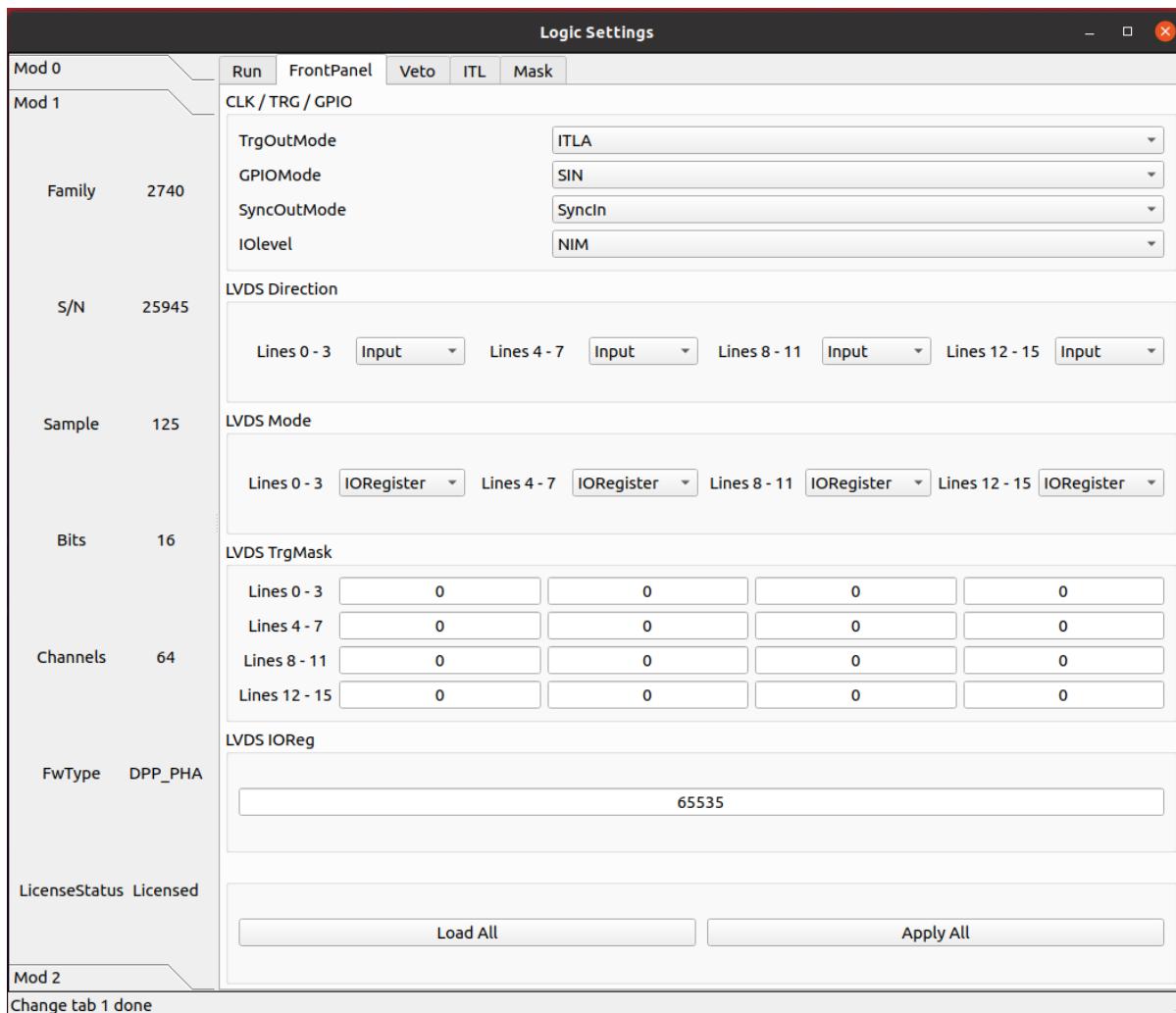
- **Internal**
 - Local oscillator, 62.5 MHz
- **FPClkIn**
 - Front Panel Clock input

参数 EnClockOutFP

Enables clock output on Front Panel for the daisy chain propagation of the clock between multiple boards.

- **True**
 - Enabled
- **False**
 - Disabled

8.2.2 模块前面板



参数 TrgOutMode

Selects the signal that is routed to the TRGOOUT output. Multiple options are not allowed.

- **Disabled**
 - TRGOOUT output disabled
- **TrgIn**
 - Propagation of Front Panel TRGIN (TRGOOUT is a replica, with some delay, of the TRGIN signal)
- **P0**
 - Propagation of P0 trigger
- **SwTrg**
 - Software trigger
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (propagation of the Encoded CLK-IN trigger)
- **Run**
 - Propagation of the RUN signal (acquisition start/stop), before applying the delay given by the Run-Delay parameter
- **RefClk**
 - Monitor of the 62.5 MHz clock (used for phase alignment)
- **TestPulse**
 - Internal Test Pulse
- **Busy**
 - Busy of the board
- **UserTrgout**
 - Trgout coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal
- **SyncIn**
 - SyncIn signal
- **SIN**
 - SIN connector signal
- **GPIO**
 - GPIO connector signal
- **LBinClk**
 - Internal Logic B clock signal
- **AcceptTrg**
 - Accepted triggers signal
- **TrgClk**
 - Trigger clock signal

参数 GPIOMode

Selects the signal that is routed to the GPIO, when this is used as output. Multiple options are not allowed. The GPIO on the front panel is a bidirectional signal that can be used in three different ways:

As independent board output (each board drives its own GPIO)

As a shared input for the boards: the signal is driven high (= 1) or low (= 0) by an external source and connected in “short circuit” among multiple boards using “T” connectors at the inputs. The GPIO is not internally terminated, thus it is necessary to put a 50 Ohm terminator at the end of the line (last “T” of the chain)

As a shared bidirectional line, making a “wired OR”. One or more boards can simultaneously drive the signal high (= 1). If no board drives the GPIO, it remains low (= 0). All boards can read back the signal. It is necessary to put a 50 Ohm terminator at both ends of the line (first and last “T” of the chain). This mode can be used to generate, for instance, the global Busy and Veto logic for multiple boards.

- **Disabled**

- GPIO disabled

- **TrgIn**

- Propagation of Front Panel TRGIN (GPIO is a replica, with some delay, of the TRGIN signal)

- **P0**

- Propagation of P0 trigger

- **SIN**

- Propagation of SIN

- **LVDS**

- LVDS trgin

- **ITLA**

- Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**

- Internal Trigger Logic B: combination of channel self-triggers

- **ITLA_AND_ITLB**

- Second level Trigger logic making the AND of ITL A and B

- **ITLA_OR_ITLB**

- Second level Trigger logic making the OR of ITL A and B

- **EncodedClkIn**

- Not implemented (propagation of the Encoded CLK-IN trigger)

- **SwTrg**

- Software trigger

- **Run**

- Propagation of RUN

- **RefClk**

- Monitor of the 62.5 MHz clock (used for phase alignment)

- **TestPulse**

- Internal Test Pulse

- **Busy**
 - Busy of the board
- **UserGPO**
 - GPO coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal

参数 SyncOutMode

In a multi-board system, it can be useful to propagate a synchronous signal together with the clock (to synchronize the start of the run, for example) on CLK OUT front panel connector. This parameter defines which signal must be sent out. Multiple options are not allowed.

- **Disabled**
 - SyncoutMode is disabled
- **SyncIn**
 - SyncIn signal (if provided with clkIn on CLK IN connector)
- **TestPulse**
 - Internal Test Pulse
- **IntClk**
 - Internal 62.5 MHz clock (for test purposes)
- **Run**
 - Propagation of RUN signal
- **User**
 - User customSyncoutMode

参数 IOlevel

Sets the electrical logic level of the LEMO I/Os (TRGIN, SIN, TRGOUT, GPIO).

Note that TRGIN and SIN are internally terminated to 50 Ohm, while GPIO and TRGOUT require the termination to 50 Ohms at the receiver

- **NIM**
 - NIM logic (0 = 0V, 1 = -0.8V, that is -16mA)
- **TTL**
 - Low Voltage TTL logic (0 = 0V, 1 = 3.3V)

参数 LVDSDirection

Assigns the direction to a quartet of LVDS I/Os.

- **Input**

- The LVDS lines of the relevant quartet are used as input. The relevant LED on the front panel is OFF.

- **Output**

- The LVDS lines of the relevant quartet are used as output. The relevant LED on the front panel lights-up.

参数 LVDSMode

The digitizer is equipped with 16 LVDS I/Os that can be programmed to be inputs or outputs by groups of 4 (quartets), depending on the LVDSDirection parameter. Once the direction has been selected, it is possible to select the functionality of the LVDS lines, individually for each quartet.

- **SelfTriggers**

- This option is available only when the LVDS are set as outputs. Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by the LVDSTrgMask parameter(16 independent masks, one per LVDS line)

- **Sync**

- Whatever is the direction of the quartet, the 4 lines are rigidly assigned to specific acquisition signals:
0 = Run 1 = Trigger 2 = Busy 3= Veto It is possible to implement a daisy chain distribution of these signals using one quartet as input and another one as output

- **IORRegister**

- The LVDS lines of the quartet are statically controlled by the LVDSIORReg parameter. Use the SetValue function to set the relevant LVDS lines when programmed as output. Use GetValue to read the status of the LVDS lines when programmed as inputs.

- **User**

- User custom.

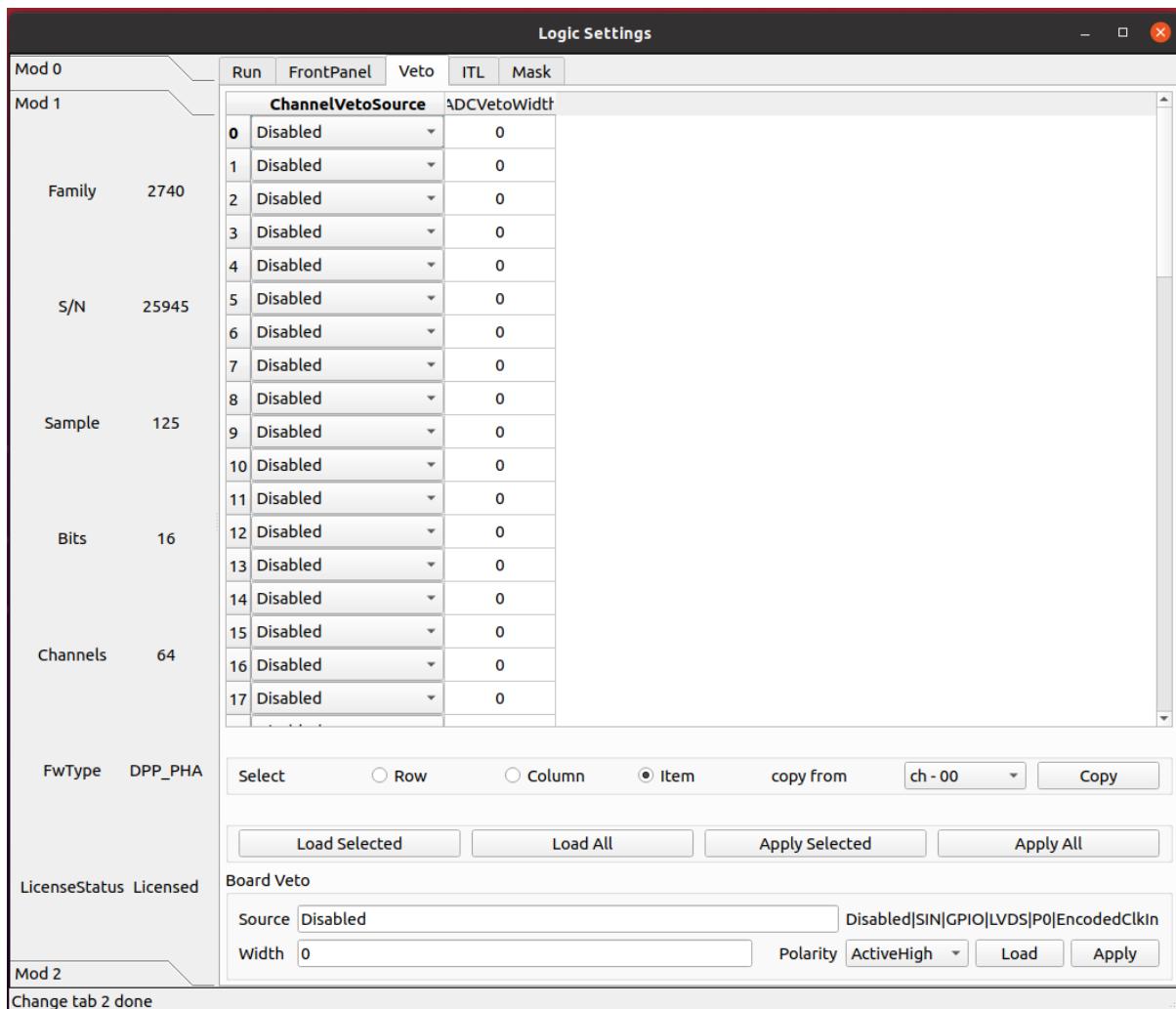
参数 LVDSTrgMask

Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by this parameter. There are 16 independent masks, one per LVDS line. Note that the trigger mask assignment does not imply the LVDS direction and mode settings. It is therefore necessary to set the Direction = Output and Mode = SelfTriggers to use the Self-Trigger propagation to the LVDS I/Os.

参数 LVDSIORReg

Set the status of the LVDS I/O for the quartets when they are programmed to be output and Mode = IORRegister. This parameter reads out the status of the quartets in the case the LVDS I/O are programmed as inputs (possibly externally driven).

8.2.3 反符合



参数 ChannelVetoSource

Allows to set the veto for each channel; it can be external (which means one of the veto options in the previous table), or it can be on a channel base.

- **Disabled**
 - Any channel veto source is disabled
- **BoardVeto**
 - Enables board veto
- **ADCOversaturation**: Enables veto due to ADC oversaturation
- **ADCundersaturation**: Enables veto due to ADC undersaturation

参数 ADCVetoWidth

It is the width of the ADC veto (undersaturation and oversaturation width) expressed in ns.

Unit of Measure: ns

参数 VetoSource

Defines the source for the Veto, which is the signal that inhibits the acquisition trigger. Multiple options are allowed, separated by “|” . The VETO signal can be either active high or low, depending on the VetoPolarity parameter. When active low, it acts as a GATE for the trigger. It is possible to stretch the duration of the VETO by means of the parameter VetoWidth.

- **Disabled**
 - VETO is always OFF
- **SIN**
 - SIN on the front panel
- **GPIO**
 - GPIO on the front panel (used as input)
- **LVDS**
 - LVDS trgin
- **P0**
 - P0 (signal from the backplane)
- **EncodedClkIn**
 - Not implemented (encoded CLK-IN veto)

参数 VetoWidth

Whatever is the source of the VETO signal, it is possible to stretch the duration of the veto up to a given time by means of a re-triggerable monostable. When 0, the monostable is disabled and the veto lasts as long as the selected source is active.

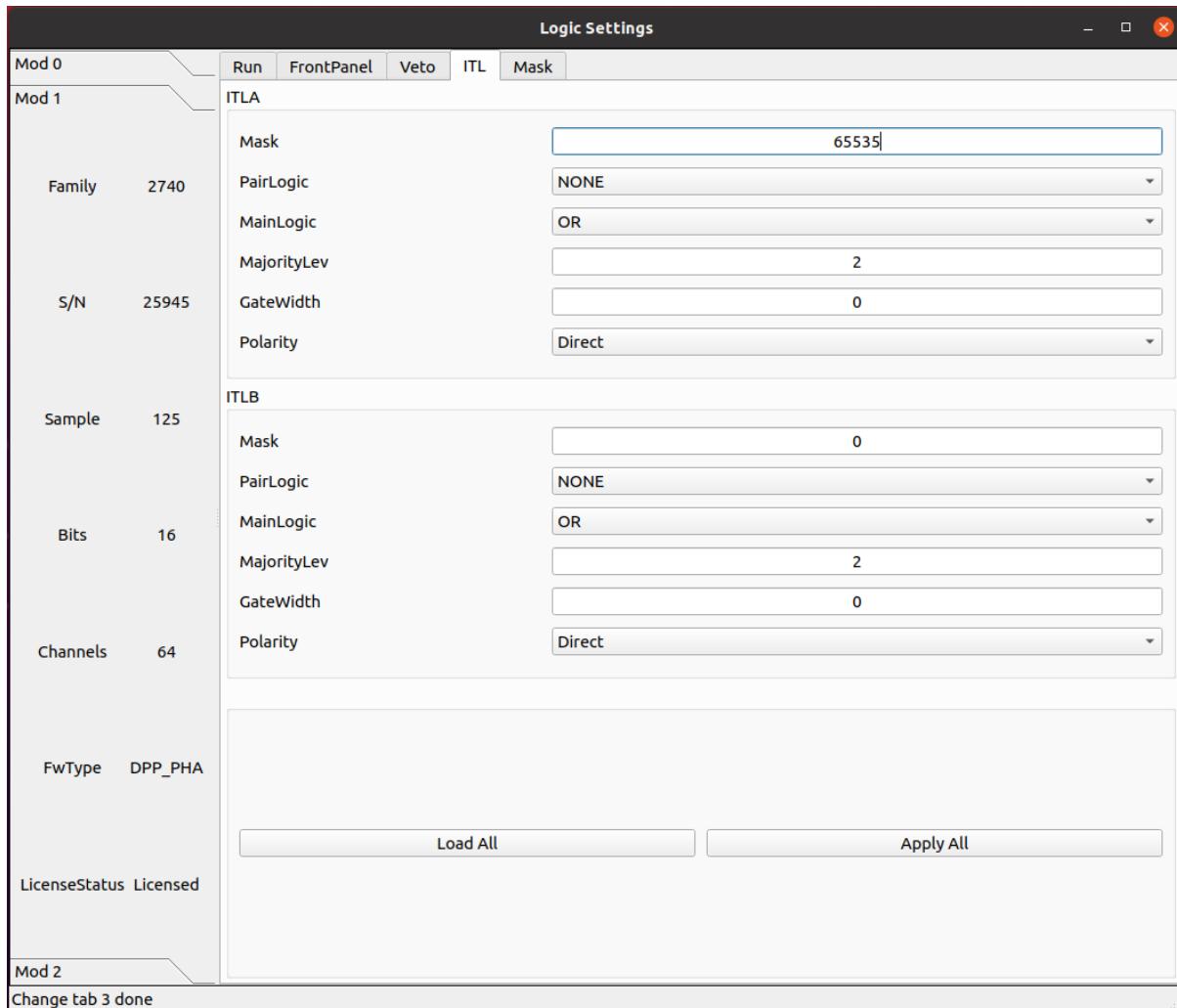
Unit of Measure: ns

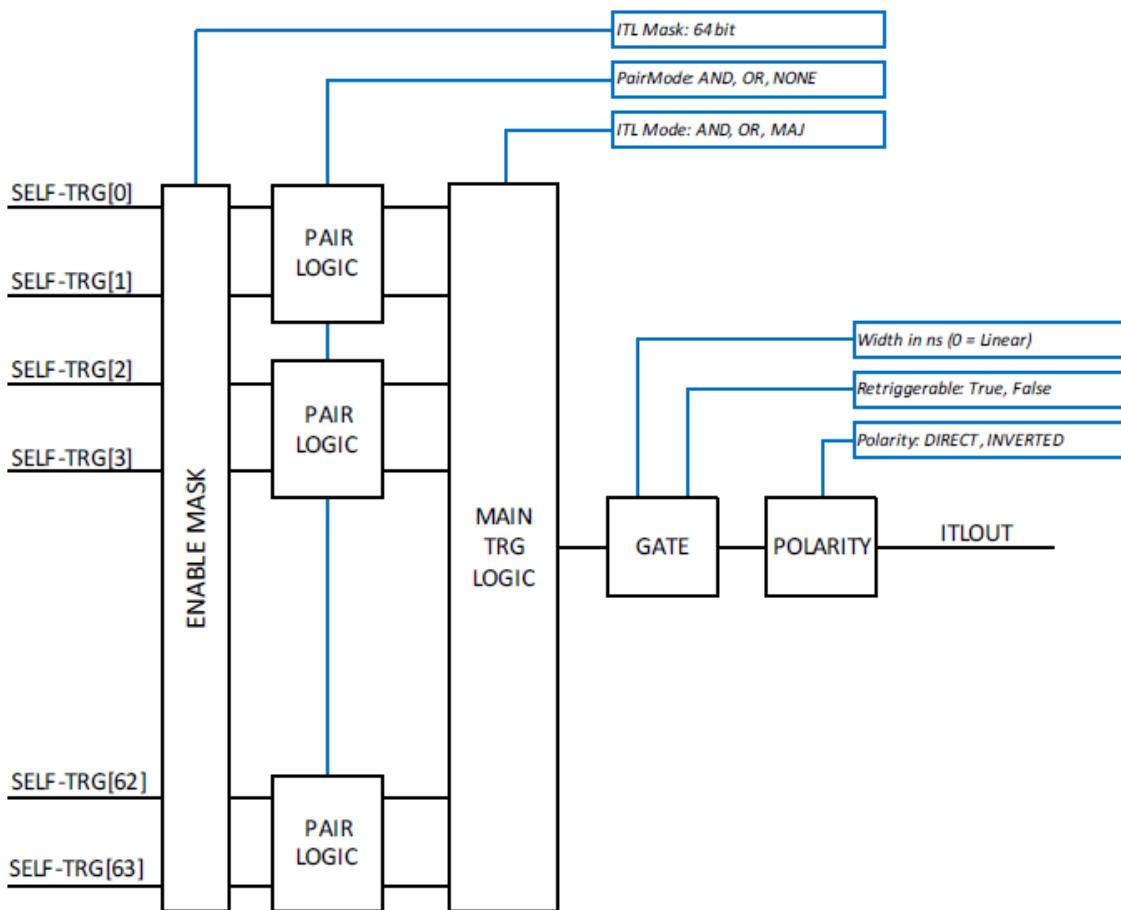
参数 VetoPolarity

Defines the polarity of the Veto

- **ActiveHigh**
 - Veto is active high. The signal acts as an “Inhibit” for the trigger
- **ActiveLow**
 - Veto is active low. The signal acts as a “Gate” the trigger

8.2.4 ITL 逻辑





参数 ITLA/BMask

Enable Mask at the input of the ITLA/B.

参数 ITLA/BPairLogic

Pairs of channels can be combined with an OR or AND before feeding in the Main trigger Logic. This is typically used in the readout of tubes or scintillator bars, where the two ends are read in coincidence, for instance in position sensitive detectors (the coincidence window will be set by the SelfTriggerWidth parameter). When the AND/OR logic is applied, the two outputs of the Pair Logic blocks are identical.

Note that they are counted twice in the following Majority logic. If the Pair Logic is disabled (“NONE” option), the block is transparent, and the two outputs are just a replica of the inputs.

- **OR**
 - Both Pair Logic Outputs = OR of two consecutive self-triggers
- **AND**
 - Both Pair Logic Outputs = AND of two consecutive self-triggers
- **NONE**
 - Outputs = Inputs

参数 ITLA/BMainLogic

Each channel of the digitizer feature a digital bipolar triangular filter discriminator with programmable rise time and threshold able to self-trigger on the input pulses and generate a self-trigger signal. In DPP Mode, the channels acquire independently, so the channel self-trigger is used locally to acquire a waveform. The trigger threshold is then referred to the bipolar triangular filter, and the threshold crossing arms the event selection. The trigger fires at the zero crossing of the time filter signal. The user can see the derivative trace on the signal inspector. It is also possible to combine all the self-triggers of the board, according to a specific trigger logic. There are two independent logic blocks, ITLA and ITLB. Their output can be used separately to feed, for instance, AcqTrigger and TrgOut, or combined in a second level trigger logic to implement more complex trigger schemes. Therefore, the ITLs can either generate the local acquisition trigger, common to all the channels, for the acquisition of the waveform, or propagate the signal outside, through the TRGOUT, thus making it possible to combine triggers of multiple boards in an external trigger logic, that eventually feeds back the TRGIN of the digitizers. Each ITL is made of an input enable mask (64 bits, one per channel), an optional pairing logic that combines the self triggers of two consecutive channels (e.g. paired coincidence) and the main trigger logic that combines the 64 selftriggers with an OR, AND or Majority logic. The output can be linear (no stretching) or reshaped by a programmable gate generator, either re-triggerable or not and finally programmed for polarity (direct or inverted).

- **OR**
 - ITLOUT = masked OR of channel self-triggers
- **AND**
 - ITLOUT = masked AND of channel self-triggers
- **Majority**
 - ITLOUT = masked Majority of channel self-triggers

参数 ITLA/BMajorityLev

Defines the majority level of the Main Logic of the ITL A/B block. The majority output is calculated at every clock cycle, and it becomes TRUE when $Nch \geq MajLev$, where Nch is the number of self-triggers active in that clock cycle and MajLev is the programmed majority level.

Note that when the Pair Logic is used to combine the self triggers two by two (AND/OR), each pair produces two identical signals that will be counted twice in the majority level.

参数 ITLA/BGateWidth

Width of the gate generator at the output of the ITLA/B block.

Unit of Measure: ns

参数 ITLA/BPolarity

Polarity of the gate generator output.

- **Direct**
 - Direct polarity
- **Inverted**
 - Inverted polarity

参数 ITLA/BEnRetigger

Set the ITLA/B to be retriggerable.

- **True**
 - The ITLA/B is retriggerable
- **False**
 - The ITLA/B is not retriggerable

8.2.5 延迟展宽

Logic Settings						
Mod 0		Run	FrontPanel	Veto	ITL	Mask
Mod 1						
			ITLConnect	ChannelsTriggerMask	CoincidenceMask	AnTCoincidenceMask
			0 ITLA	0	Disabled	Disabled
			1 ITLA	0	Disabled	Disabled
			2 ITLA	0	Disabled	Disabled
			3 ITLA	0	Disabled	Disabled
			4 ITLA	0	Disabled	Disabled
			5 ITLA	0	Disabled	Disabled
			6 ITLA	0	Disabled	Disabled
			7 ITLA	0	Disabled	Disabled
			8 ITLA	0	Disabled	Disabled
			9 ITLA	0	Disabled	Disabled
			10 ITLA	0	Disabled	Disabled
			11 ITLA	0	Disabled	Disabled
			12 ITLA	0	Disabled	Disabled
			13 ITLA	0	Disabled	Disabled
			14 ITLA	0	Disabled	Disabled
			15 ITLA	0	Disabled	Disabled
			16 Disabled	0	Disabled	Disabled
			17 Disabled	0	Disabled	Disabled
FwType	DPP_PHA	Enabled				
LicenseStatus	Licensed	Select	<input type="radio"/> Row	<input type="radio"/> Column	<input checked="" type="radio"/> Item	copy from ch - 00 Copy
Mod 2		Load Selected	Load All	Apply Selected	Apply All	
Change tab 4 done						

参数 ITLConnect

Alternative to ITLAMask, ITLBMask. Determines if the channel partecipate in ITLA or ITLB

- **Disabled**
 - The channel is disabled
- **ITLA**
 - The channel participates in ITLA logic block
- **ITLB**

- The channel participates in ITLB logic block

参数 ChannelsTriggerMask

Allows to set the mask over 64 bits to generate a channel trigger. It can be used to trigger a channel using a trigger coming from another channel. It also allows to set the mask over 64 bits to enable the channel to participate in the coincidence logic defined in CoincidenceMask and AntiCoincidenceMask (option Channel64Trg). 64-bit enable mask, each bit representing a channel.

参数 CoincidenceMask

Allows to set the coincidence mask that generates a trigger on the specified channel.

- **Disabled**

- All the coincidence sources are disabled

- **Ch64Trigger**

- One of the 64 channels can generate a coincidence signal

- **TRGIN**

- TRGIN can generate a coincidence signal

- **GlobalTriggerSource**

- Acquisition Trigger can generate a coincidence signal

- **ITLA**

- ITLA can generate a coincidence signal

- **ITLB**

- ITLB can generate a coincidence signal

参数 AntiCoincidenceMask

Allows to set the anticoincidence mask that generates a trigger on the specified channel.

- **Disabled**

- All the coincidence sources are disabled

- **Ch64Trigger**

- One of the 64 channels can generate a coincidence signal

- **TRGIN**

- TRGIN can generate a coincidence signal

- **GlobalTriggerSource**

- Acquisition Trigger can generate a coincidence signal

- **ITLA**

- ITLA can generate a coincidence signal

- **ITLB**

- ITLB can generate a coincidence signal

参数 CoincidenceLength

Coincidence window length in nanoseconds (ns). 16-bit value.

Unit of Measure: ns

CHAPTER 9

PSD 固件

9.1 基本参数配置

9.1.1 输入信号

Basic Settings																				
		Input		Trigger		Wave		Record		Scope										
		InputDelay		ChEnable		WaveSource		DCOffset(%)		Polarity										
		0	1	2	3	4	5	6	7	8	9									
Mod 0		0	0	0	0	0	0	0	0	0	0									
		1	1	1	1	1	1	1	1	1	1									
		2	2	2	2	2	2	2	2	2	2									
		3	3	3	3	3	3	3	3	3	3									
Mod 1		4	4	4	4	4	4	4	4	4	4									
		5	5	5	5	5	5	5	5	5	5									
		6	6	6	6	6	6	6	6	6	6									
		7	7	7	7	7	7	7	7	7	7									
Mod 2		8	8	8	8	8	8	8	8	8	8									
		9	9	9	9	9	9	9	9	9	9									
		10	10	10	10	10	10	10	10	10	10									
		11	11	11	11	11	11	11	11	11	11									
Family	2740	12	12	12	12	12	12	12	12	12	12									
		13	13	13	13	13	13	13	13	13	13									
		14	14	14	14	14	14	14	14	14	14									
		15	15	15	15	15	15	15	15	15	15									
S/N	25946	16	16	16	16	16	16	16	16	16	16									
		17	17	17	17	17	17	17	17	17	17									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
Sample	125	0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
Bits	16	0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
Channels	64	0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
FwType	DPP_PSD	0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
		0	0	0	0	0	0	0	0	0	0									
LicenseStatus		Licensed																		
<input type="button" value="Load Selected"/> <input type="button" value="Load All"/> <input type="button" value="Apply Selected"/> <input type="button" value="Apply All"/>																				
Change tab 0 done																				

参数 ChGain

仅限 x2730.

设置可变增益放大器（VGA）的增益。

Unit of Measure: dB

参数 InputDelay

设置输入延迟，单位为采样点。

该值设置每 4 个通道共用一个相同配置。

参数 ChEnable

独立设定每个通道是否开启使用。如果通道不启用，它不提供任何数据，同时它的自触发也关闭。

参数 WaveSource

在正常模式下，采集的波形来源于模拟输入的 A/D 转换产生的 ADC 采样序列。出于测试目的，可以用内部数据生成器替换 ADC 数据。

- **ADC_DATA**
 - Data from the ADC (normal operating mode)
- **ADC_TEST_TOGGLE**
 - Toggle between 0x5555 and 0xAAAA (test mode)
- **ADC_TEST_RAMP**
 - 16-bit ramp pattern (test mode)
- **ADC_TEST_SIN**
 - 8-point sine wave test pattern
- **ADC_TEST_PRBS**
 - 16-bit PRBS generated by a 23-bit PRBS pattern generator (test mode)
- **Ramp**
 - Data from a ramp generator. It is actually a 16-bit field, where the 6 most significant bits identify the channel and the 10 less significant bits are the samples of a ramp from 0x000 up to 0x3FF (i.e. 0 to 1023). It is so a 10-bit ramp with offset given by “channel*1024”. For channel 0, it is a counter from 0 to 1023; for channel 1, it is a counter from 1024 to 2047, and so on
- **IPE**
 - Not implemented
- **SquareWave**
 - Internally generated programmable square wave

参数 DCOffset

对于每个通道，将恒定的 DC 偏移（由 16 位 DAC 控制）添加到模拟输入，以在 ADC 的动态范围内调整信号基线的位置（即模拟输入的“零伏”）。

由于部件的公差，有必要校准偏移 DAC。校准是通过工厂测试完成的，通常不需要重新校准。然而，可以执行新的校准。校准参数存储在板的闪存中，并在通电时加载。每次写入或读取 DCOffset 参数时，内部逻辑会自动应用这些参数。

DCOffset 参数为数字，单位为满刻度的百分比。当 DCOffset 为 0 时，输入信号的基线处于 ADC 0。当 DCOffset 为 100 时，输入信号的基线处于 ADC $2^{\{NBIT\}} - 1$ 。

参数 Polarity

设置输入脉冲的极性。

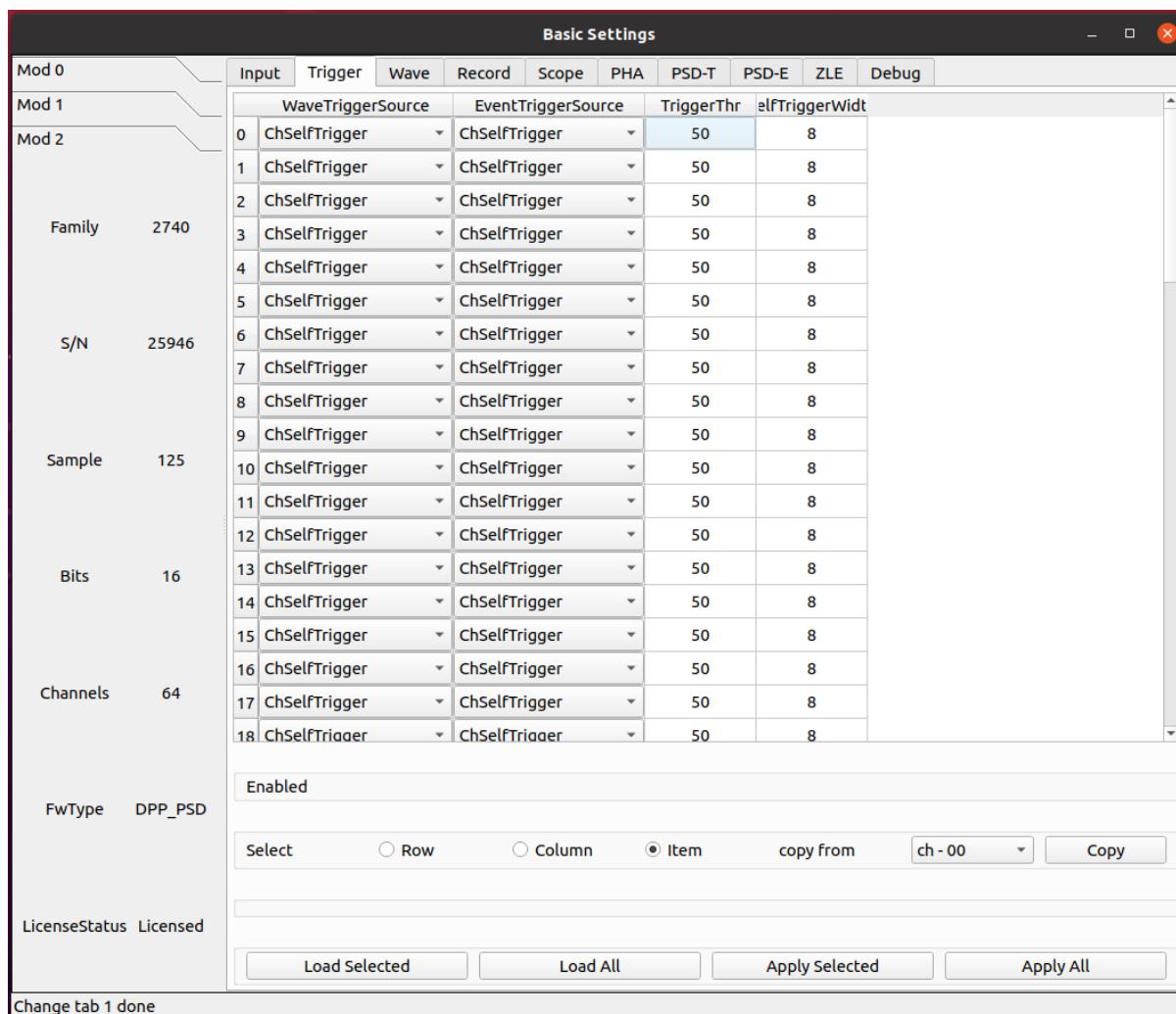
- Positive
 - Positive polarity
- Negative
 - Negative polarity

参数 VGAGain

2745 特有。

以 0.5 dB 为步长设置可变增益放大器（VGA）的增益。参数设置每 16 个通道为一组，64 通道分为 4 组。最小可设置为 0，最大为 40。

9.1.2 触发



参数 WaveTriggerSource

允许设置波形的触发源。

设置此参数意味着获得包括波形和相关时间戳以及能量信息的事件。

- **Disabled**
 - No trigger source enabled for the waveform
- **Ch64Trigger**
 - One (or more) channel self-trigger can generate a trigger for a waveform
- **ChSelfTrigger**
 - Channel self-trigger can generate a trigger for a waveform
- **SwTrg**
 - Software Trigger can generate a trigger for a waveform
- **ADCOverSaturation**
 - ADC Oversaturation can generate a trigger for a waveform
- **ADCUnderSaturation**

- ADC Undersaturation can generate a trigger for a waveform
- **ExternalInhibit**
 - Inhibit can generate a trigger for a waveform
- **TRGIN**
 - External TRGIN can generate a trigger for a waveform
- **GlobalTriggerSource**
 - Acquisition Trigger Source (the same of the Scope mode) can generate a trigger for a waveform
- **LVDS**
 - A signal on the LVDS connectors can generate a trigger for a waveform
- **ITLA**
 - Internal Trigger Logic A can generate a trigger for a waveform
- **ITLB**
 - Internal Trigger Logic B can generate a trigger for a waveform

参数 EventTriggerSource

允许设置时间、能量 (T-E) 事件的触发源。设置此参数意味着获取包括时间戳和能量信息的事件。

- **Disabled**
 - No trigger source enabled for the T-E event
- **Ch64Trigger**
 - One (or more) channel self-trigger can generate a trigger for a T-E event
- **ChSelfTrigger**
 - Channel self-trigger can generate a trigger for a T-E event
- **SwTrg**
 - Software Trigger can generate a trigger for a T-E event
- **TRGIN**
 - External TRGIN can generate a trigger for a T-E event
- **GlobalTriggerSource**
 - Acquisition Trigger Source (the same of the Scope mode) can generate a trigger for a T-E event
- **LVDS**
 - A signal on the LVDS connectors can generate a trigger for a T-E event
- **ITLA**
 - Internal Trigger Logic A can generate a trigger for a T-E event
- **ITLB**
 - Internal Trigger Logic B can generate a trigger for a T-E event

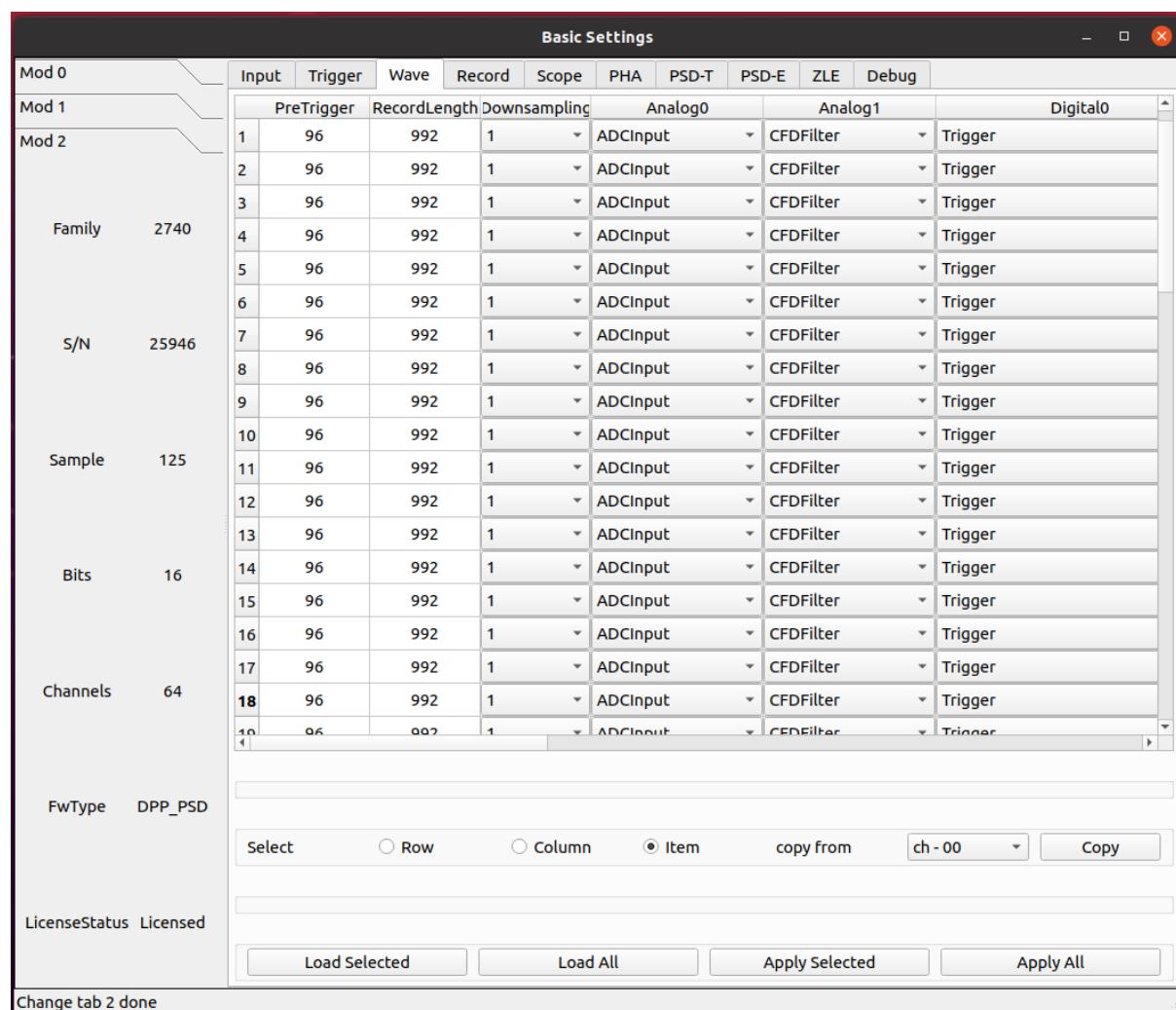
参数 TriggerThr

相对于滤波之后的波形的设置阈值。

参数 SelfTriggerWidth

产生自触发信号的数字前沿甄别器的输出可以在“线性”模式下使用，这意味着它会持续信号保持在阈值以上（或以下）的时间，从而充当“过阈值”信号，或者可以通过可编程门产生器，使其成为固定宽度的脉冲。门产生器是不可再触发的单稳态，当超过阈值时变高，在编程时间后变低。该参数定义了过阈值的固定宽度脉冲。

9.1.3 波形



参数 PreTrigger

波形中触发器位置之前的时间（即预触发窗口的大小）。

单位为时间， ns

参数 RecordLength

波形大小（即采集窗口的大小）。波形的实际大小将自动四舍五入到最接近的允许值。通过读回参数可以得到确切的数值。记录时间长度取决于下采样设置。

单位为时间， ns

参数 DownsamplingFactor

波形的下采样因子。

- 1
 - x1
- 2
 - x2
- 4
 - x4
- 8
 - x8

参数 Analog0/1

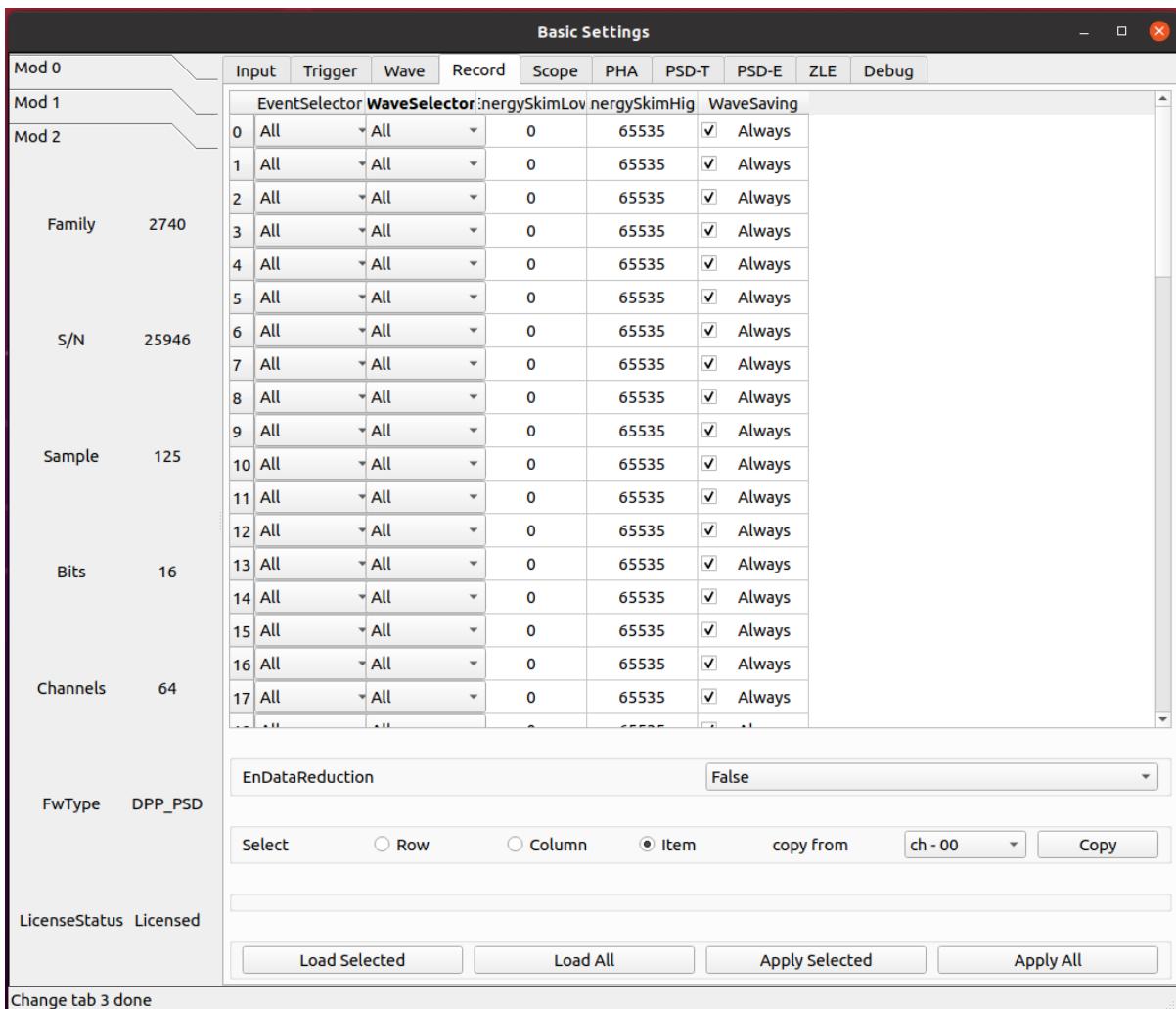
- ADCInput
 - ADC input probe
- ADCInputBaseline
 - ADC input baseline probe
- CFDFilter
 - Constant Fraction Discriminator filter probe

参数 Digital0/1/2/3

- Trigger
 - Trigger probe
- CFDFilterArmed
 - Constant Fraction Discriminator Filter Armed probe
- ReTriggerGuard
 - ReTrigger Guard probe
- ADCInputBaselineFreeze
 - ADC Input Baseline Freeze probe
- ADCInputOverthreshold

- ADCInputOverthreshold
- **ChargeReady**
 - Charge Ready probe
- **LongGate**
 - Long Gate probe
- **PileUpTrigger**
 - Pile Up Trigger probe
- **ShortGate**
 - Short Gate probe
- **ChargeOverRange**
 - Integrated Charge Over Range probe
- **ADCSaturation**
 - ADC Saturation probe
- **ADCInputNegativeOverthreshold**
 - ADC Input Negative Overthreshold probe

9.1.4 数据记录



参数 EventSelector

设置必须保存的事件。

- All
 - All events are saved
 - PileUp
 - Only pileup events are saved
 - EnergySkim
 - Save only the events in the Energy Skim range

参数 WaveSelector

设置必须保存的波形。

- **All**
 - All waves are saved
- **PileUp**
 - Only pileup waves are saved
- **EnergySkim**
 - Save only waves in the Energy Skim range

参数 EnergySkimLowDiscriminator

允许标记能量高于低舍弃阈值的事件。16 位。

参数 EnergySkimHighDiscriminator

允许标记能量低于高舍弃阈值的事件。16 位。

参数 WaveSaving

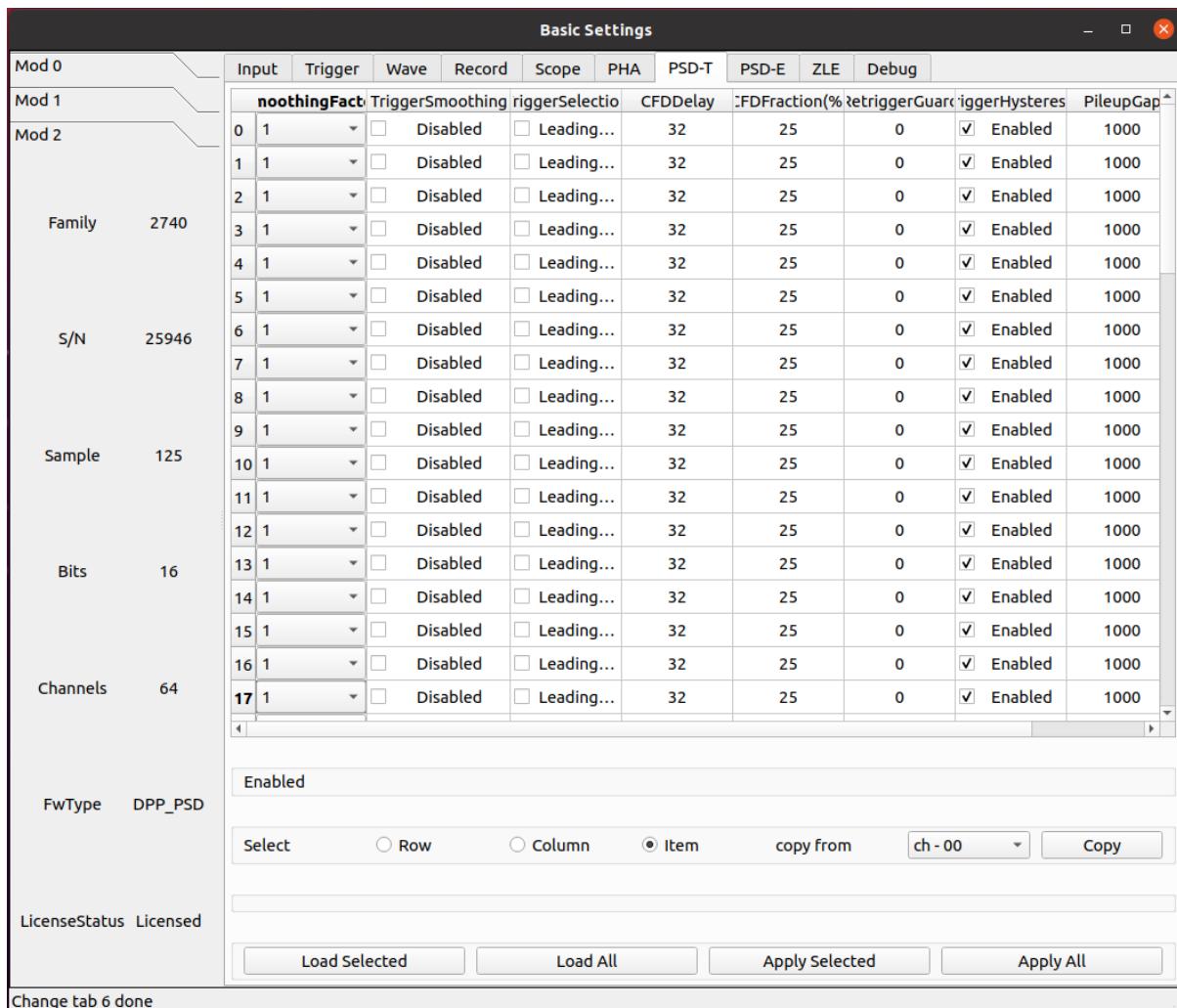
允许始终保存波形或仅根据请求保存波形。

- **Always**
 - Waveforms are always saved
- **OnRequest**
 - Waveforms are saved on request

参数 EnDataReduction

如果启用，2 个 words 压缩为一个 word 事件。

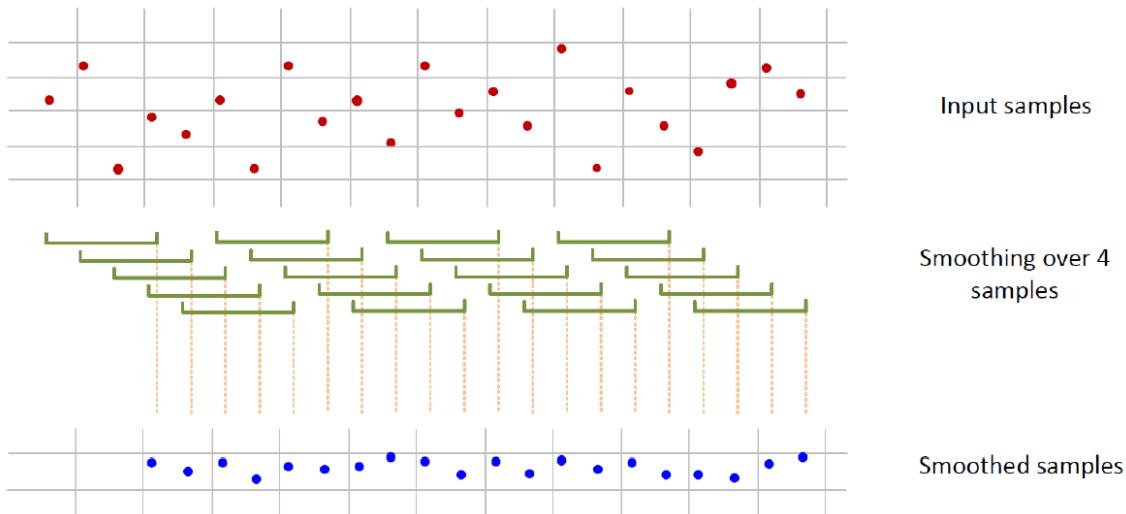
9.1.5 PSD 时间参数



参数 SmoothingFactor

平滑是一个移动平均滤波，其中输入样本被前 n 个样本的平均值代替，其中 n 是：2、4、8 和 16 个样本。启用时（请参见 TriggerSmoothing），触发器将应用于平滑的采样，从而减少对噪声的触发。CFD 和 LED 触发模式均可用于平滑输入。根据 ChargeSmoothing 参数，在输入样本和/或平滑样本上执行电荷积分。

- 1
 - Smoothing is disabled.
- 2
 - Smoothing is done averaging 2 samples.
- 4
 - Smoothing is done averaging 4 samples.
- 8
 - Smoothing is done averaging 8 samples.
- 16
 - Smoothing is done averaging 16 samples.



参数 TriggerSmoothing

启用/禁用触发滤波的平滑因子。

- Enabled
 - Smoothing factor is enabled for the time filter.
- Disabled
 - Smoothing factor is disabled for the time filter.

参数 TriggerSelection

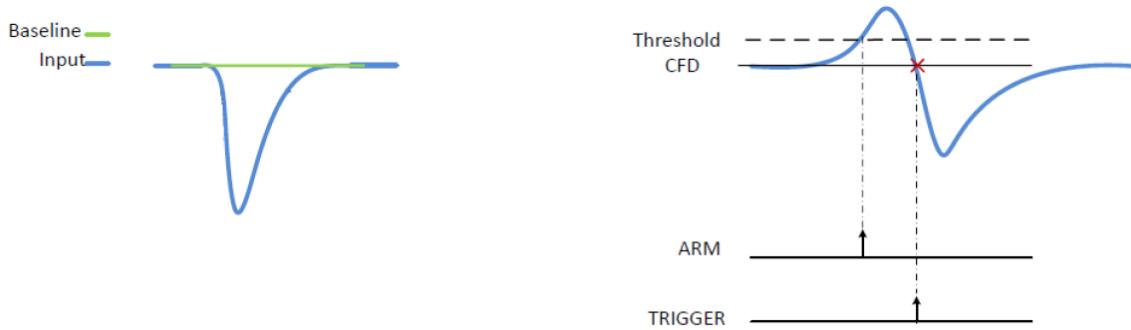
允许用户根据两种算法选择脉冲：前沿，即当脉冲样本超过可编程阈值时识别脉冲，或者通过数字恒比甄别来获得更好的定时信息。在这两种情况下，一旦选择了事件，信号就会延迟可编程数量的样本（对应于以 ns 为单位的“预触发”值），以便能够在触发之前对脉冲进行积分（“预门”）。用于电荷积分的门然后在信号之前由电荷累加器产生和接收。当门有效时，基线保持冻结，采用之前最后的平均值，其值用作电荷积分参考。在可编程“再触发保护”（请参阅 RetriggerGuard）值的整个持续时间内，其他触发信号被禁止。建议设置与信号宽度兼容的触发保持值。基线在整个触发暂停持续时间内保持冻结状态。

- LeadingEdge
 - Set the Leading Edge discriminator
- CFD
 - Set the Constant Fraction discriminator

参数 CFDDelay

discriminates events based on a CFD signal. The digital CFD signal has been implemented in the classical way except for the input signal inversion. The input waveform is first inverted, then attenuated by a factor f equal to the desired timing fraction (see CFDFraction) of full amplitude, then the signal is inverted again and delayed by a time d equal to the time it takes the pulse to rise from the constant fraction level to the pulse peak; the latest two signals are summed to produce a bipolar pulse, the CFD, and its zero crossing –corresponding to the fraction f of the input pulse –is taken as the trigger time.

The delay of the CFD signal can be defined by the user. The TriggerThreshold is then referred to the CFD itself, and the threshold crossing arms the event selection. The trigger fires at the zero crossing of the derivative signal itself.



参数 CDFFraction

- **25**
 - 25%
- **50**
 - 50%
- **75**
 - 75%
- **100**
 - 100%

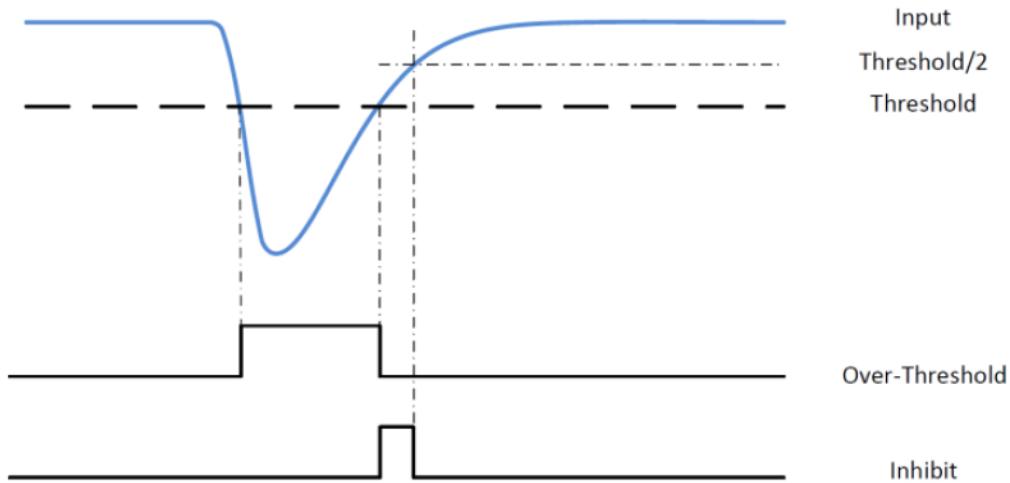
参数 RetriggerGuard

在诸如来自 PMT 的快速信号的情况下，可能发生快甄别信号中的可能过冲，从而导致再触发，从而可能出现伪堆积。此参数允许设置再触发禁止保护（单位为 ns）。

参数 TriggerHysteresis

当输入信号不再超过阈值时，可能会在脉冲尾部再次触发，尤其是在尾部包含尖峰或噪声的情况下。“触发滞后”功能禁止任何触发，直到输入脉冲达到阈值本身的一半。此参数允许启用/禁用触发滞后机制。

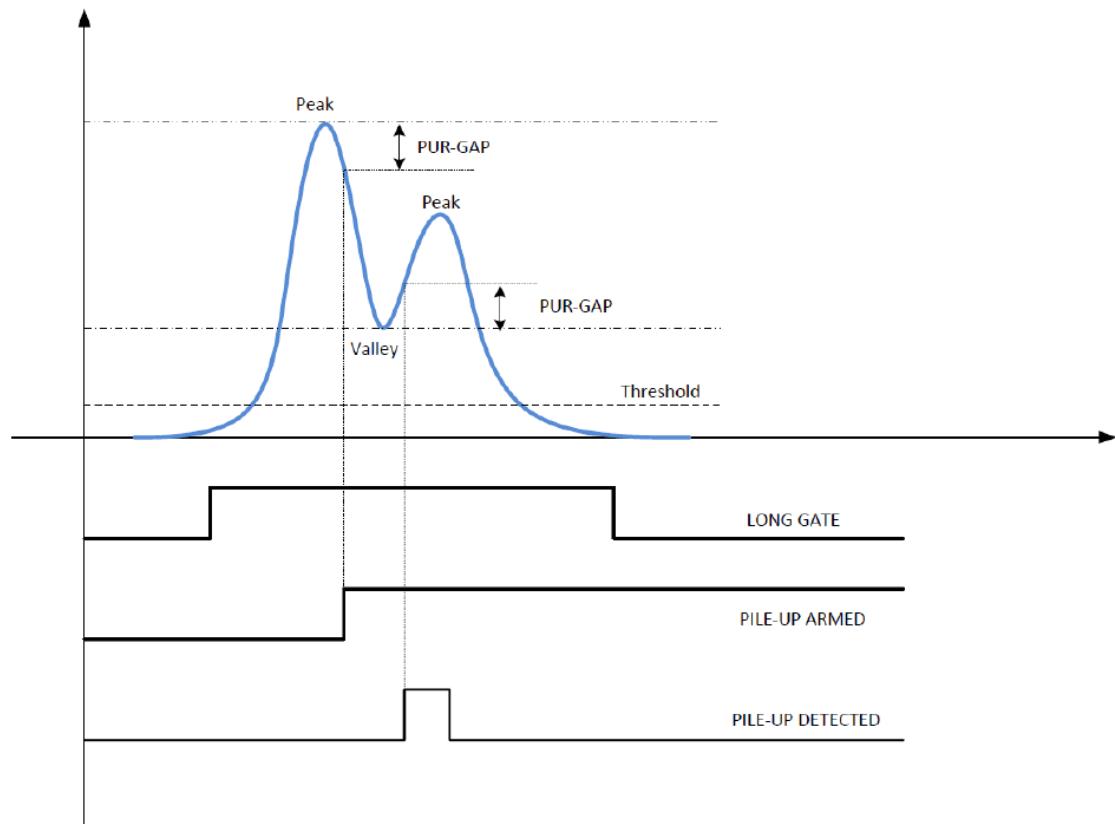
- **Disabled**
 - Trigger hysteresis mechanism is disabled.
- **Enabled**
 - Trigger hysteresis mechanism is enabled.



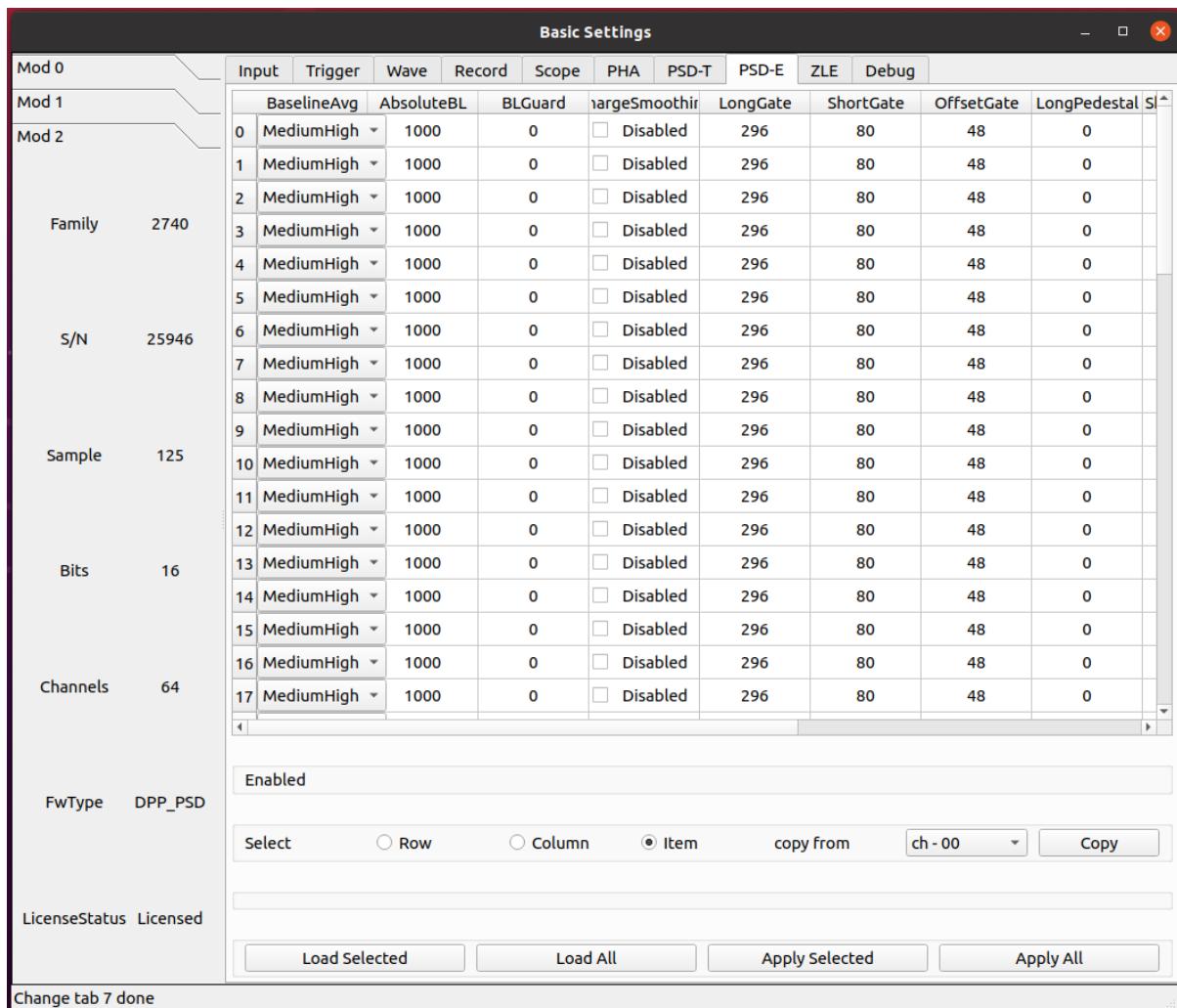
参数 PileupGap

PSD 固件主要用于处理快信号，如来自与光电倍增管耦合的闪烁探测器的信号。相关输出信号不像电荷敏感前置放大器那样显示出长的衰减尾，并且两个脉冲之间堆积的概率非常低。特别是，第二个脉冲位于前一个脉冲的指数尾部的情况相当罕见。然而，使用 PSD 算法，分离闪烁探测器发射的光的快分量和慢分量是很重要的。通常，快成分是快速脉冲（几十 ns），而慢成分是相当长的尾部（通常为几 μs ），其幅度远小于快成分。为了在脉冲形状甄别中获得最佳结果，有必要将“长门”设置为慢成分的整个持续时间。在这些条件下，堆积事件很可能发生在长门期间，并导致慢成分电荷计算错误。因此，发现这些事件很重要。在 PSD 固件中，当同一门内出现峰-谷-峰的情况时，两个事件被视为堆积事件，其中谷和峰之间的间隙是可编程值。当达到峰值时，算法评估与 PileupGap (PUR-GAP) 值相对应的点，并准备检测堆积事件 (pile-up ARMED)。如果存在“谷”条件，并且输入信号超过 PUR-GAP 阈值，则该事件被标记为堆积。在默认配置中，固件不采取任何操作，事件的总电荷在门内进行评估并保存到内存中。

此参数允许设置峰值间隙以识别堆积。



9.1.6 PSD 能量参数



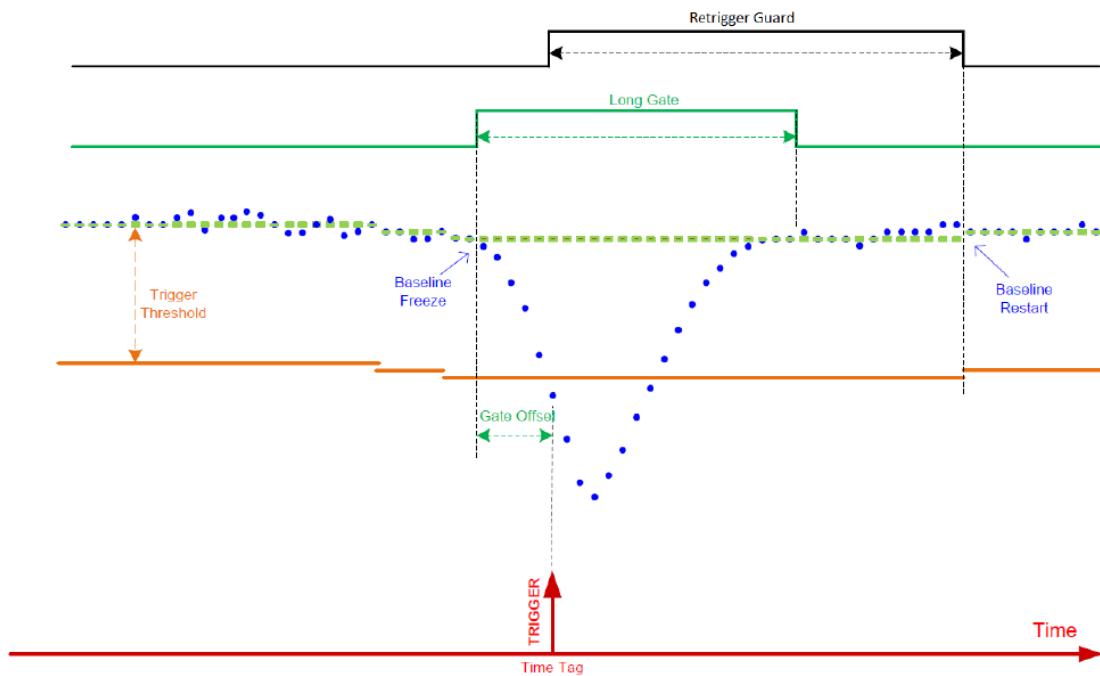
参数 BaselineAvg

数字化模块连续接收输入信号并将其数字化。可以在 ADC 尺度中调整信号基线的位置，使用 DCOffset 参数来利用模块的全部动态范围。基线值是 PSD 固件的一个重要参数，因为其值用作输入脉冲电荷积分的参考值。此外，大多数 DPP 参数与基线值有关，如触发阈值。用户可以设置基线的固定值，也可以让 DPP 固件动态计算。在第一种情况下，用户必须通过选项 Fixed 以 LSB 为单位设置基线值。该值在整个采集运行中保持固定。在后一种情况下，固件动态地将基线评估为移动时间窗口内的 N 个点的平均值。用户可以选择下面列出的选项之一，每个选项对应于预定义数量的样本。然后，从门启动前的几个时钟开始冻结基线，直到长门和触发保持 (trigger hold-off) 之间的最大值结束（请参阅 GateLongLength 和 RetriggerGuard）。此参数允许设置用于平均能量滤波基线的样本数。

- **Fixed**
 - Baseline fixed at AbsoluteBaseline value
- **Low**
 - Baseline samples for average = 16
- **MediumLow**
 - Baseline samples for average = 64
- **MediumHigh**
 - Baseline samples for average = 256

- **High**

- Baseline samples for average = 1024



参数 AbsoluteBL

ADCInput 信号基线的绝对值。

单位为 ADC 道址。

参数 BLGuard

积分门前的能量滤波基线评估保护 (ns)。

参数 ChargeSmoothing

启用/禁用电荷评估的平滑因子。

- **Enabled**

- Smoothing factor is enabled in the charge evaluation

- **Disabled**

- Smoothing factor is disabled in the charge evaluation

参数 ShortGate

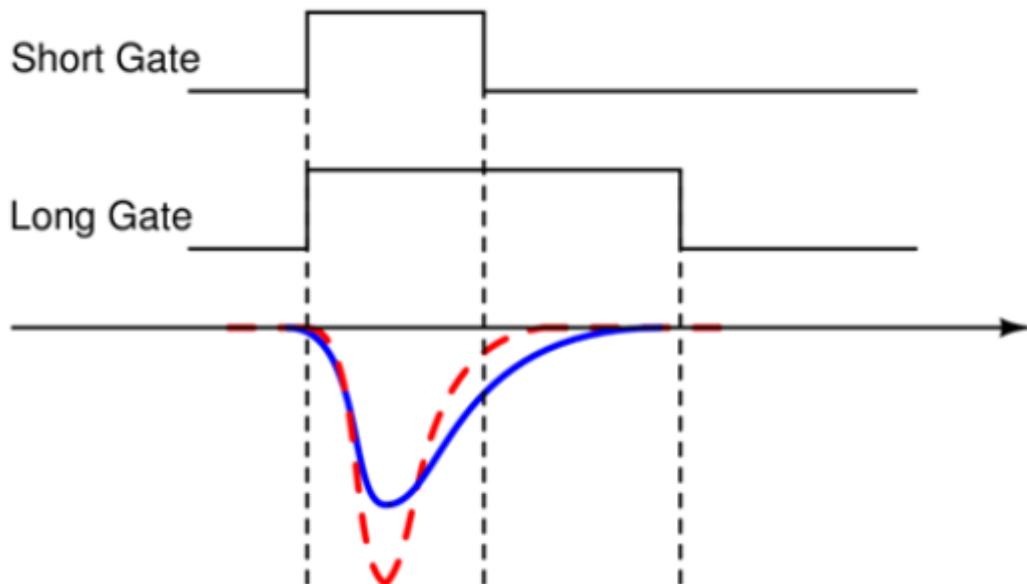
此参数允许设置短门长度。

单位 ns。

参数 LongGate

PSD 固件的目的是对输入信号进行电荷积分，并计算对输入（Qshort 和 Qlong）进行双门积分的 PSD 因子。下图显示了两个不同形状信号的短门和长门位置。

单位 ns。



参数 OffsetGate

此参数允许设置相对于触发信号的门偏置。

单位 ns。

参数 LongPedestal

此参数允许设置长电荷积分 pedestal。这一特性在能量接近零的情况下非常有用。

参数 ShortPedestal

此参数允许设置短电荷积分 pedestal。这一特性在能量接近零的情况下非常有用。

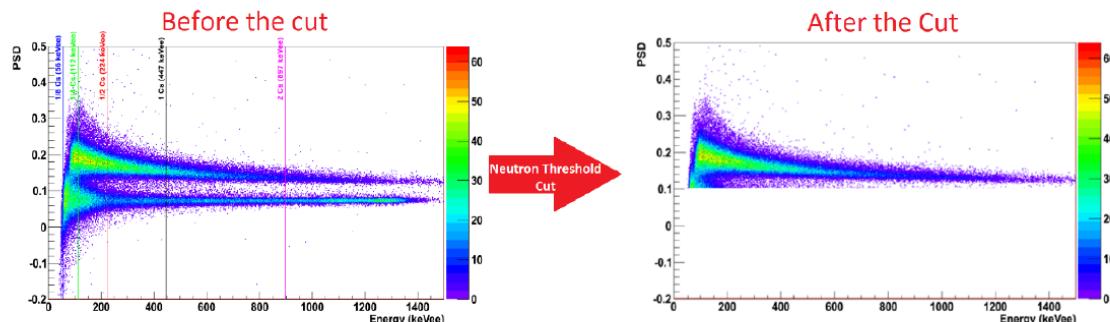
参数 EnergyGain

此参数允许设置能量增益，即重新缩放信号电荷。

- **x1**
 - Charge value is multiplied x1.
- **x4**
 - Charge value is multiplied x4.
- **x16**
 - Charge value is multiplied x16.
- **x64**
 - Charge value is multiplied x64.
- **x256**
 - Charge value is multiplied x256.

参数 NeutronThr

此参数允许设置中子甄别的中子能量阈值。固件将“长能量” - “短能量”之差（即长门和短门中的电荷积分之间的差）与该参数设置的阈值进行比较，以决定是否拒绝该事件。参考下图所示的中子/伽马甄别示例，PSD 上的切口允许用户拒绝大多数伽马事件，从而只记录中子和与中子重叠的少量伽马。



参数 EventReject

启用事件的中子抑制。参见 NeutronThreshold 参数

- **Disabled**
 - Neutron rejection for events is disabled.
- **Enabled**
 - Neutron rejection for events is enabled.

参数 WaveReject

启用波形的中子抑制。参见 NeutronThreshold 参数

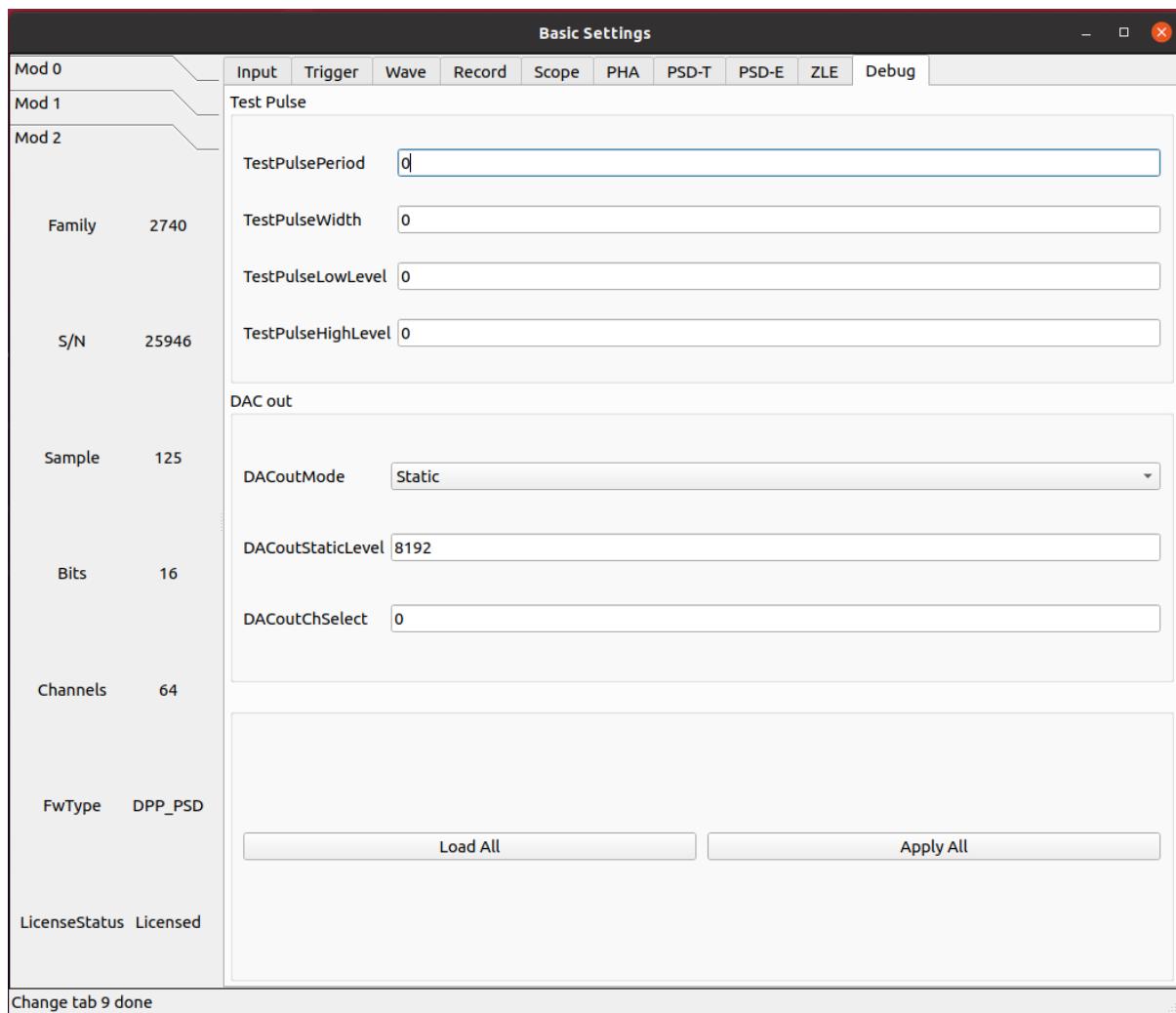
- **Disabled**

- Neutron rejection for waves is disabled.

- **Enabled**

- Neutron rejection for waves is enabled.

9.1.7 诊断



参数 TestPulsePeriod

测试脉冲是一种可编程方波，可用作内部周期性触发器（主要用于测试目的）或在 TRGOUT 和 GPIO 输出上生成逻辑测试脉冲（TTL 或 NIM）。此参数设置测试脉冲的周期。

单位为时间， ns

参数 TestPulseWidth

测试脉冲的宽度（信号保持高电平的时间）。

单位为时间， ns

参数 TestPulseLowLevel

以 ADC 道址表示的测试脉冲低电平

参数 TestPulseHighLevel

以 ADC 道址表示的测试脉冲高电平

参数 DACoutMode

选择要在前面板 DAC LEMO 口输出发送的信号类型。

- **Static**
 - DAC output stays at a fixed level, given by the DACoutStaticLevel parameter
- **Ramp**
 - The DAC output is driven by a 14-bit counter
- **Sin5MHz**
 - The DAC output is a sine wave at 5 MHz with fixed amplitude
- **Square**
 - Square wave with period and width set by TestPulsePeriod and TestPulseWidth and amplitude between TestPulseLowLevel and TestPulseHighLevel.
- **IPE**
 - Not implemented
- **ChInput**
 - The DAC reproduces the input signal received by one input channel, selected by the DACoutChSelect parameter
- **MemOccupancy**
 - Level of the memory occupancy (not yet implemented)
- **ChSum**
 - The DAC reproduces the “analog” sum of all the digitizer inputs (not yet implemented)
- **OverThrSum**
 - The DAC output is proportional to the number of channels that are currently above the threshold

参数 DACoutStaticLevel

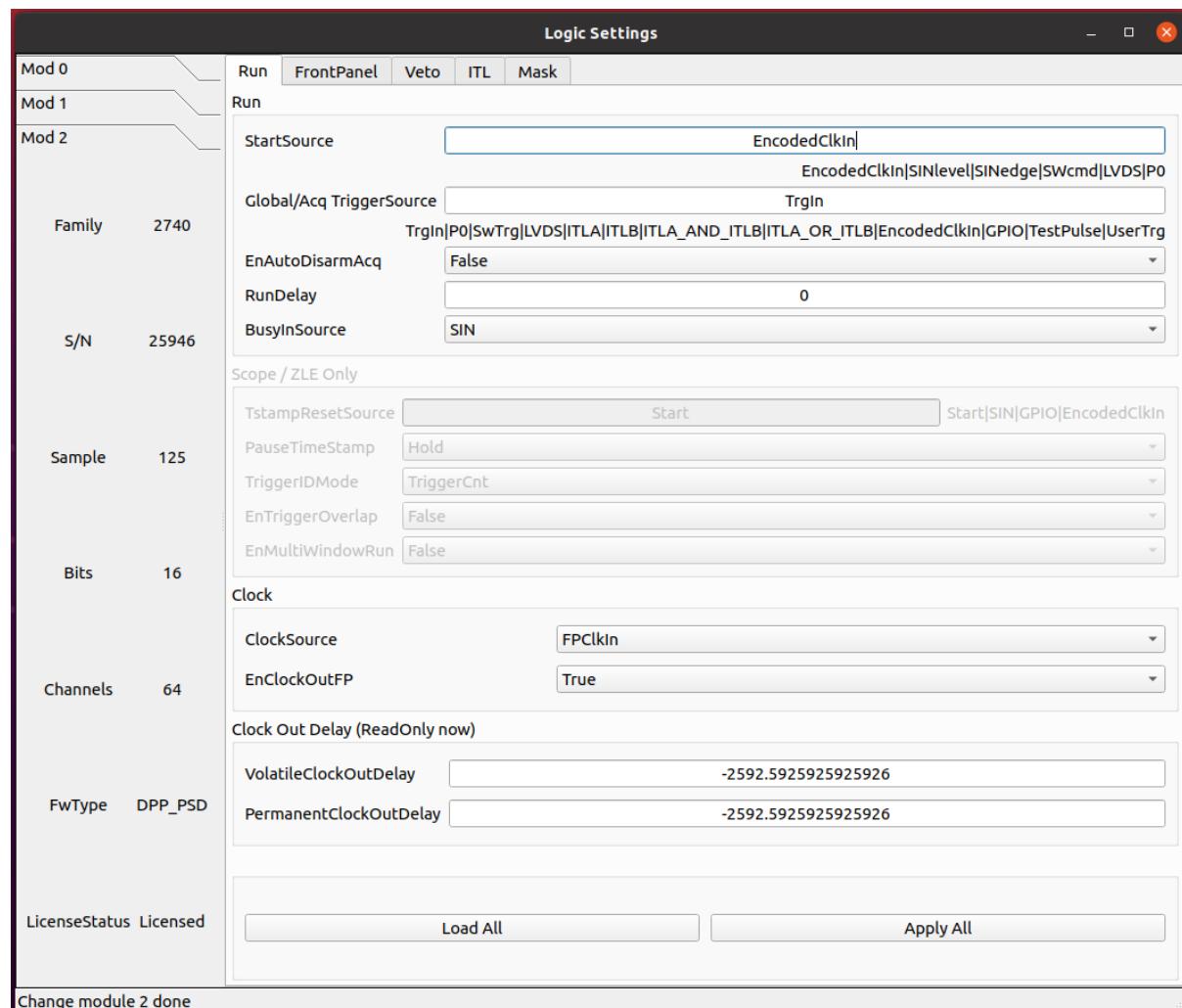
当 DACoutMode = Static 时，此参数设置 DAC 输出的 14 位电平。

参数 DACoutChSelect

当 DACoutMode = ChInput 时，DAC 输出由该参数选择的通道的输入信号。

9.2 逻辑参数配置

9.2.1 运行



参数 StartSource

Defines the source for the start of run. Multiple options are allowed, separated by “|” .

- **EncodedClkIn**

- Start from CLK-IN/SYNC connector on the front panel. This is a 4-pin connector (LVDS signals) used to propagate the reference clock (typ. 62.5 MHz) and a Sync signal. The rising edge of the Sync starts the acquisition, that lasts until the Sync returns low (falling edge).

- **SINlevel**

- Start from SIN (1=run, 0=stop)

- **SINedge**

- Start from SIN (rising edge = run; stop from SW)

- **SWcmd**

- Start from SW

- **LVDS**

- Start from LVDS

- **P0**

- Start from P0 (backplane)

参数 GlobalTriggerSource

Defines the source for the Acquisition Trigger, which is the signal that opens the acquisition window and saves the waveforms in the memory buffers. Multiple options are allowed, separated by “|” .

- **TrgIn**

- Front Panel TRGIN

- **P0**

- Trigger from P0 (backplane)

- **SwTrg**

- Software trigger

- **LVDS**

- LVDS trgin

- **ITLA**

- Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**

- Internal Trigger Logic B: combination of channel self-triggers

- **ITLA_AND_ITLB**

- Second level Trigger logic making the AND of ITL A and B

- **ITLA_OR_ITLB**

- Second level Trigger logic making the OR of ITL A and B

- **EncodedClkIn**

- Not implemented (encoded CLK-IN trigger)

- **GPIO**

- Front Panel GPIO
- **TestPulse**
 - Internal Test Pulse
- **UserTrg**
 - User custom trigger source

参数 EnAutoDisarmAcq

When enabled, the Auto Disarm option disarms the acquisition at the stop of run. When the start of run is controlled by an external signal, this option prevents the digitizer to restart without the intervention of the software.

- **True**
 - The acquisition is automatically disarmed after the stop. It is therefore necessary to rearm the digitizer (with the relevant command sent by the software) before starting a new run.
- **False**
 - The acquisition is not disarmed after the stop. Multiple transition of the start signal will produce multiple runs.

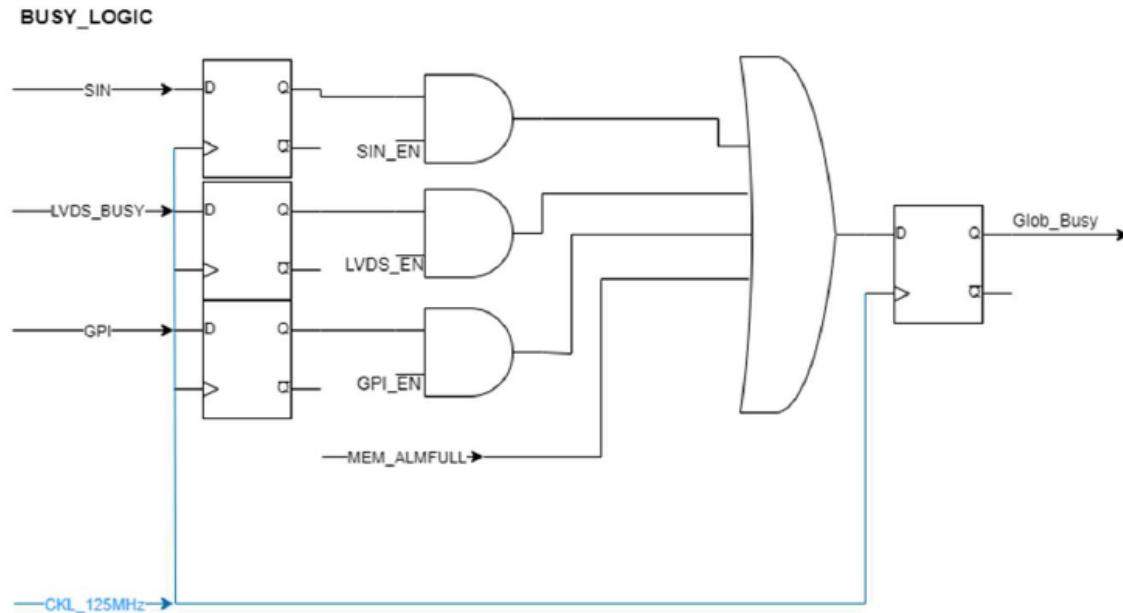
参数 RunDelay

When the start of run is controlled by a RUN signal that is propagated in daisy chain between the boards (for instance through the ClkIn- ClkOut or SIN-GPIO sync chain), it is necessary to compensate for the propagation delay and let the boards start exactly at the same time. The RunDelay parameter allows the start of the acquisition to be delayed by a given number of clock cycles with respect to the rising edge of the RUN signal. Assuming that the propagation delay is 2 cycles, the RunDelay setting will be 0 for the last board in the chain, 2 for the previous one, and so on up 2x(NB-1) for the first one.

Unit of Measure: ns

参数 BusyInSource

In a multi-board system, it might be necessary to prevent one board to accept a new trigger while another board is full and thus unable to accept the same trigger. For this reason, each board can generate a Busy signal to notify that it is unable to get a new trigger. If the busy/veto mechanism has some latency, it is advisable to generate the busy slightly before the digitizer become full. For this purpose, it is possible to assert the busy output when the acquisition memory reaches a certain level of occupancy (internally managed). The OR of the busy signals is typically used to stop the global trigger. It is possible to get the individual busy signals from each board and make an external OR logic or connect the boards with cables to propagate the Busy along the chain. Each board makes an OR between its internal busy and the busy input signal coming from the previous board, thus having a global Busy at the end of the line. This parameter defines the source of the Busy Input (schematized in the figure below)



- **Disabled**
 - The Busy is given by the Internal Busy only (Memory full or almost full)
- **SIN**
 - Busy input from SIN on front panel
- **GPIO**
 - Busy input coming from GPIO on front panel, used as a simple input. It is also possible to use GPIO as a wired OR (bidirectional). In this mode, the Busy line goes high as soon as one board drives it high. All the boards can read the Busy line and use it as a veto for the trigger
- **LVDS**
 - LVDS trgin

参数 ClockSource

This is the source of the system clock. Multiple options are not allowed

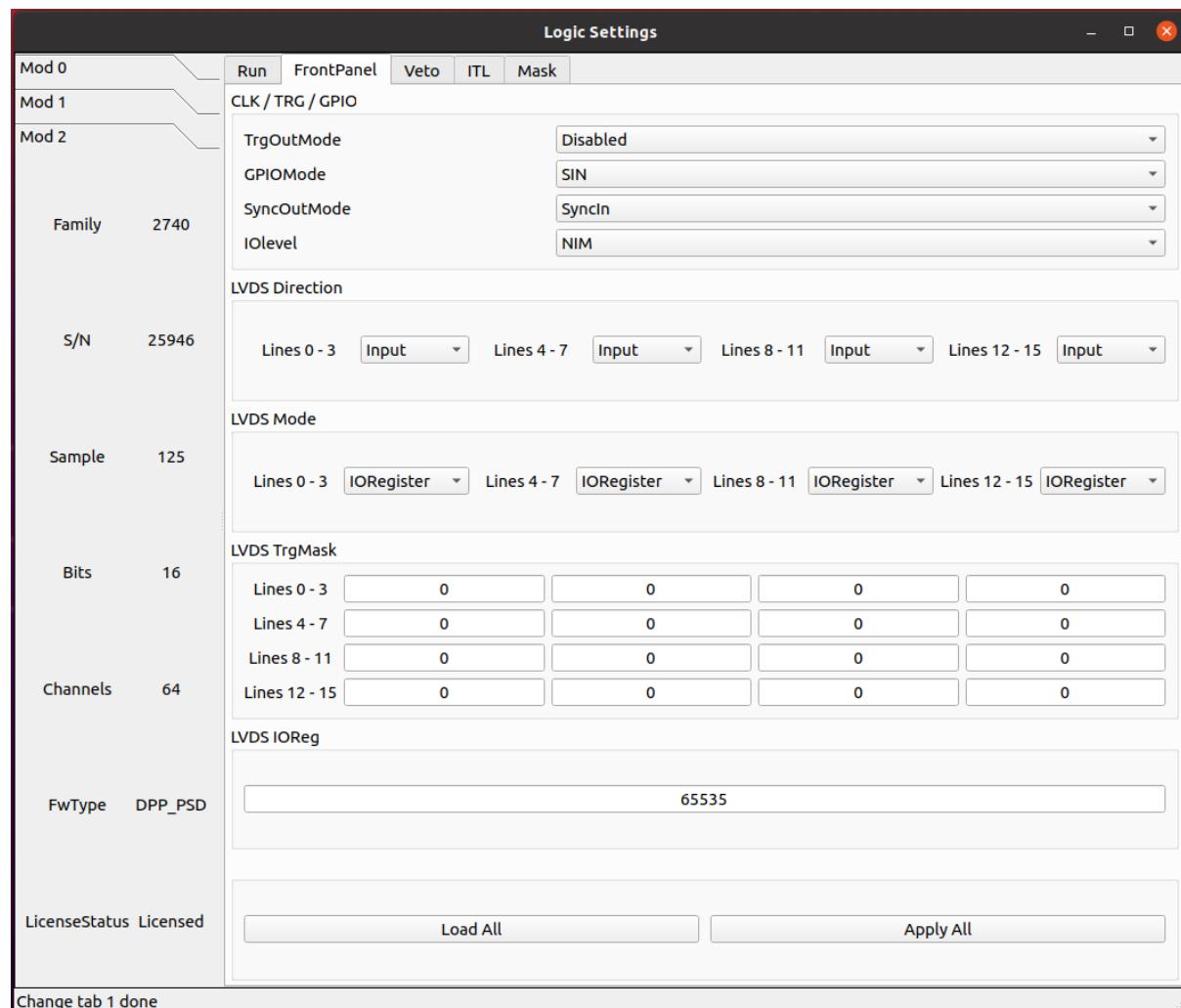
- **Internal**
 - Local oscillator, 62.5 MHz
- **FPClkIn**
 - Front Panel Clock input

参数 EnClockOutFP

Enables clock output on Front Panel for the daisy chain propagation of the clock between multiple boards.

- True
 - Enabled
- False
 - Disabled

9.2.2 模块前面板



参数 TrgOutMode

Selects the signal that is routed to the TRGOOUT output. Multiple options are not allowed.

- Disabled
 - TRGOOUT output disabled
- TrgIn
 - Propagation of Front Panel TRGIN (TRGOOUT is a replica, with some delay, of the TRGIN signal)
- P0

- Propagation of P0 trigger
- **SwTrg**
 - Software trigger
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers
- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (propagation of the Encoded CLK-IN trigger)
- **Run**
 - Propagation of the RUN signal (acquisition start/stop), before applying the delay given by the Run-Delay parameter
- **RefClk**
 - Monitor of the 62.5 MHz clock (used for phase alignment)
- **TestPulse**
 - Internal Test Pulse
- **Busy**
 - Busy of the board
- **UserTrgout**
 - Trgout coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal
- **SyncIn**
 - SyncIn signal
- **SIN**
 - SIN connector signal
- **GPIO**
 - GPIO connector signal
- **LBinClk**
 - Internal Logic B clock signal
- **AcceptTrg**

- Accepted triggers signal
- **TrgClk**
 - Trigger clock signal

参数 GPIOMode

Selects the signal that is routed to the GPIO, when this is used as output. Multiple options are not allowed. The GPIO on the front panel is a bidirectional signal that can be used in three different ways:

As independent board output (each board drives its own GPIO)

As a shared input for the boards: the signal is driven high (= 1) or low (= 0) by an external source and connected in “short circuit” among multiple boards using “T” connectors at the inputs. The GPIO is not internally terminated, thus it is necessary to put a 50 Ohm terminator at the end of the line (last “T” of the chain)

As a shared bidirectional line, making a “wired OR”. One or more boards can simultaneously drive the signal high (= 1). If no board drives the GPIO, it remains low (= 0). All boards can read back the signal. It is necessary to put a 50 Ohm terminator at both ends of the line (first and last “T” of the chain). This mode can be used to generate, for instance, the global Busy and Veto logic for multiple boards.

- **Disabled**
 - GPIO disabled
- **TrgIn**
 - Propagation of Front Panel TRGIN (GPIO is a replica, with some delay, of the TRGIN signal)
- **P0**
 - Propagation of P0 trigger
- **SIN**
 - Propagation of SIN
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers
- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (propagation of the Encoded CLK-IN trigger)
- **SwTrg**
 - Software trigger
- **Run**
 - Propagation of RUN

- **RefClk**
 - Monitor of the 62.5 MHz clock (used for phase alignment)
- **TestPulse**
 - Internal Test Pulse
- **Busy**
 - Busy of the board
- **UserGPO**
 - GPO coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal

参数 SyncOutMode

In a multi-board system, it can be useful to propagate a synchronous signal together with the clock (to synchronize the start of the run, for example) on CLK OUT front panel connector. This parameter defines which signal must be sent out. Multiple options are not allowed.

- **Disabled**
 - SyncoutMode is disabled
- **SyncIn**
 - SyncIn signal (if provided with clkIn on CLK IN connector)
- **TestPulse**
 - Internal Test Pulse
- **IntClk**
 - Internal 62.5 MHz clock (for test purposes)
- **Run**
 - Propagation of RUN signal
- **User**
 - User customSyncoutMode

参数 IOlevel

Sets the electrical logic level of the LEMO I/Os (TRGIN, SIN, TRGOUT, GPIO).

Note that TRGIN and SIN are internally terminated to 50 Ohm, while GPIO and TRGOUT require the termination to 50 Ohms at the receiver

- **NIM**
 - NIM logic (0 = 0V, 1 = -0.8V, that is -16mA)
- **TTL**
 - Low Voltage TLL logic (0 = 0V, 1 = 3.3V)

参数 LVDSDirection

Assigns the direction to a quartet of LVDS I/Os.

- **Input**

- The LVDS lines of the relevant quartet are used as input. The relevant LED on the front panel is OFF.

- **Output**

- The LVDS lines of the relevant quartet are used as output. The relevant LED on the front panel lights-up.

参数 LVDSMode

The digitizer is equipped with 16 LVDS I/Os that can be programmed to be inputs or outputs by groups of 4 (quartets), depending on the LVDSDirection parameter. Once the direction has been selected, it is possible to select the functionality of the LVDS lines, individually for each quartet.

- **SelfTriggers**

- This option is available only when the LVDS are set as outputs. Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by the LVDSTrgMask parameter(16 independent masks, one per LVDS line)

- **Sync**

- Whatever is the direction of the quartet, the 4 lines are rigidly assigned to specific acquisition signals:
0 = Run 1 = Trigger 2 = Busy 3= Veto It is possible to implement a daisy chain distribution of these signals using one quartet as input and another one as output

- **IORRegister**

- The LVDS lines of the quartet are statically controlled by the LVDSIORReg parameter. Use the SetValue function to set the relevant LVDS lines when programmed as output. Use GetValue to read the status of the LVDS lines when programmed as inputs.

- **User**

- User custom.

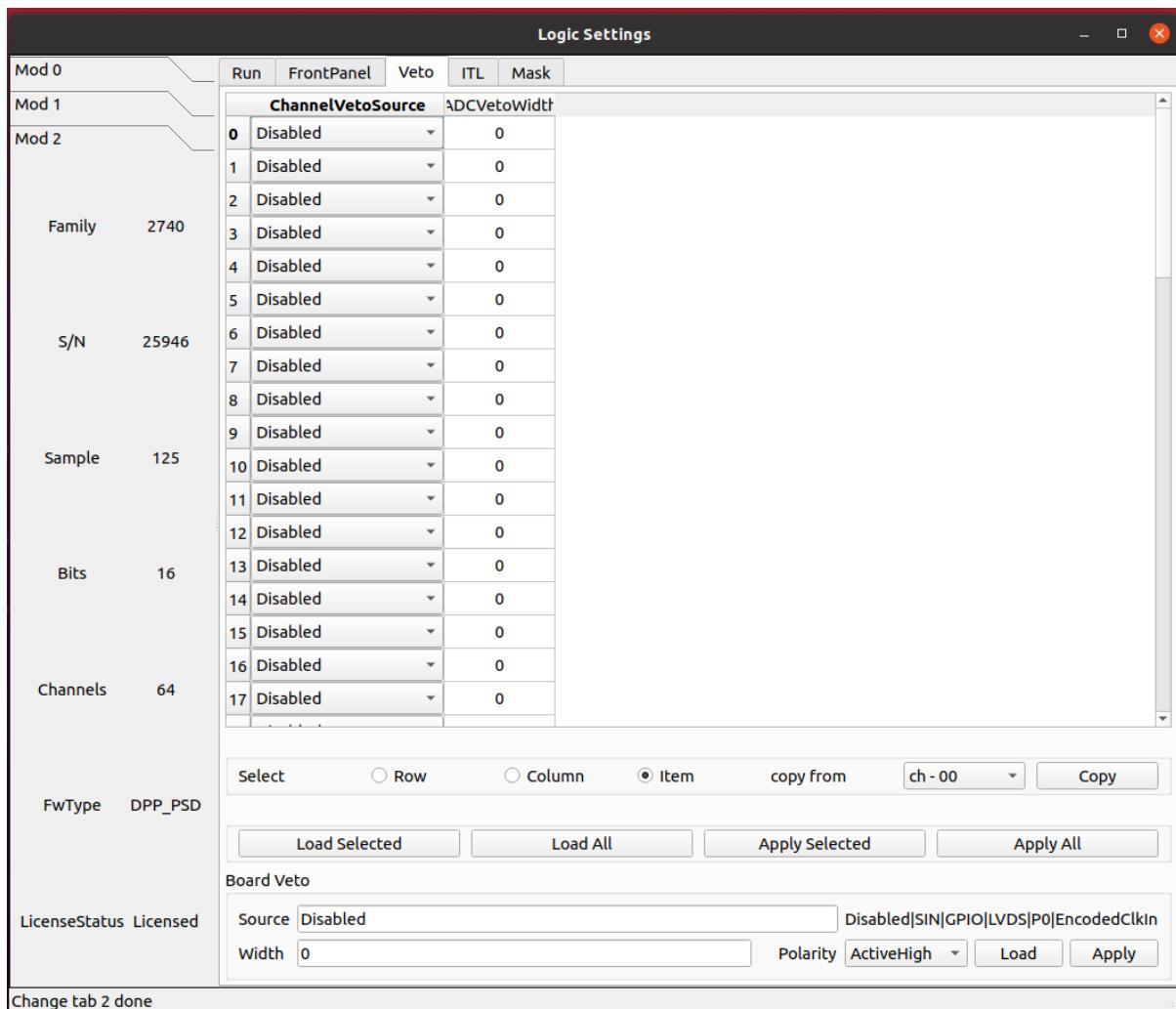
参数 LVDSTrgMask

Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by this parameter. There are 16 independent masks, one per LVDS line. Note that the trigger mask assignment does not imply the LVDS direction and mode settings. It is therefore necessary to set the Direction = Output and Mode = SelfTriggers to use the Self-Trigger propagation to the LVDS I/Os.

参数 LVDSIORReg

Set the status of the LVDS I/O for the quartets when they are programmed to be output and Mode = IORRegister. This parameter reads out the status of the quartets in the case the LVDS I/O are programmed as inputs (possibly externally driven).

9.2.3 反符合



参数 ChannelVetoSource

Allows to set the veto for each channel; it can be external (which means one of the veto options in the previous table), or it can be on a channel base.

- **Disabled**
 - Any channel veto source is disabled
- **BoardVeto**
 - Enables board veto
- ADCOverSaturation: Enables veto due to ADC oversaturation
- ADCUnderSaturation: Enables veto due to ADC undersaturation

参数 ADCVetoWidth

It is the width of the ADC veto (undersaturation and oversaturation width) expressed in ns.

Unit of Measure: ns

参数 VetoSource

Defines the source for the Veto, which is the signal that inhibits the acquisition trigger. Multiple options are allowed, separated by “|” . The VETO signal can be either active high or low, depending on the VetoPolarity parameter. When active low, it acts as a GATE for the trigger. It is possible to stretch the duration of the VETO by means of the parameter VetoWidth.

- **Disabled**
 - VETO is always OFF
- **SIN**
 - SIN on the front panel
- **GPIO**
 - GPIO on the front panel (used as input)
- **LVDS**
 - LVDS trgin
- **P0**
 - P0 (signal from the backplane)
- **EncodedClkIn**
 - Not implemented (encoded CLK-IN veto)

参数 VetoWidth

Whatever is the source of the VETO signal, it is possible to stretch the duration of the veto up to a given time by means of a re-triggerable monostable. When 0, the monostable is disabled and the veto lasts as long as the selected source is active.

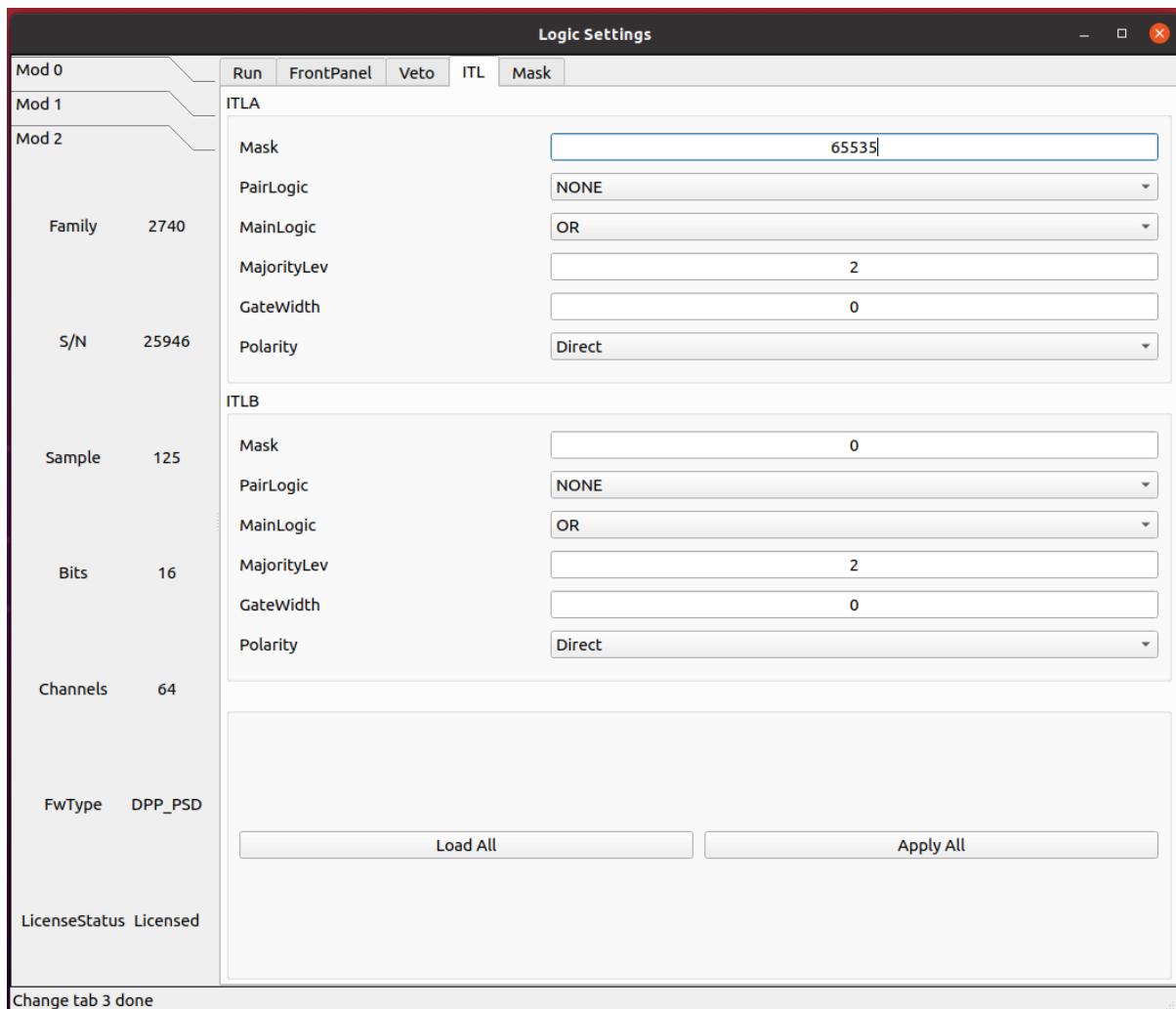
Unit of Measure: ns

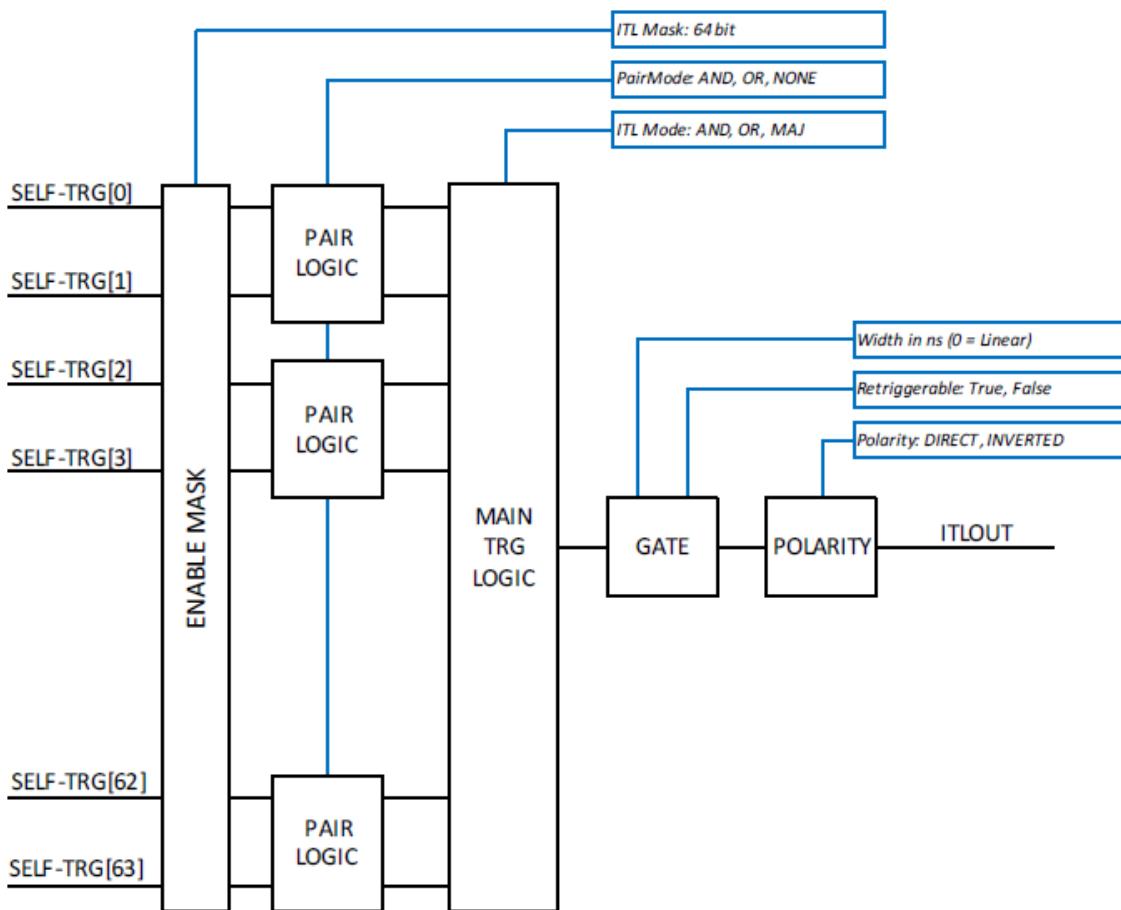
参数 VetoPolarity

Defines the polarity of the Veto

- **ActiveHigh**
 - Veto is active high. The signal acts as an “Inhibit” for the trigger
- **ActiveLow**
 - Veto is active low. The signal acts as a “Gate” the trigger

9.2.4 ITL 逻辑





参数 ITLA/BMask

Enable Mask at the input of the ITLA/B.

参数 ITLA/BPairLogic

Pairs of channels can be combined with an OR or AND before feeding in the Main trigger Logic. This is typically used in the readout of tubes or scintillator bars, where the two ends are read in coincidence, for instance in position sensitive detectors (the coincidence window will be set by the SelfTriggerWidth parameter). When the AND/OR logic is applied, the two outputs of the Pair Logic blocks are identical.

Note that they are counted twice in the following Majority logic. If the Pair Logic is disabled ("NONE" option), the block is transparent, and the two outputs are just a replica of the inputs.

- **OR**
 - Both Pair Logic Outputs = OR of two consecutive self-triggers
- **AND**
 - Both Pair Logic Outputs = AND of two consecutive self-triggers
- **NONE**
 - Outputs = Inputs

参数 ITLA/BMainLogic

Each channel of the digitizer feature a digital bipolar triangular filter discriminator with programmable rise time and threshold able to self-trigger on the input pulses and generate a self-trigger signal. In DPP Mode, the channels acquire independently, so the channel self-trigger is used locally to acquire a waveform. The trigger threshold is then referred to the bipolar triangular filter, and the threshold crossing arms the event selection. The trigger fires at the zero crossing of the time filter signal. The user can see the derivative trace on the signal inspector. It is also possible to combine all the self-triggers of the board, according to a specific trigger logic. There are two independent logic blocks, ITLA and ITLB. Their output can be used separately to feed, for instance, AcqTrigger and TrgOut, or combined in a second level trigger logic to implement more complex trigger schemes. Therefore, the ITLs can either generate the local acquisition trigger, common to all the channels, for the acquisition of the waveform, or propagate the signal outside, through the TRGOUT, thus making it possible to combine triggers of multiple boards in an external trigger logic, that eventually feeds back the TRGIN of the digitizers. Each ITL is made of an input enable mask (64 bits, one per channel), an optional pairing logic that combines the self triggers of two consecutive channels (e.g. paired coincidence) and the main trigger logic that combines the 64 selftriggers with an OR, AND or Majority logic. The output can be linear (no stretching) or reshaped by a programmable gate generator, either re-triggerable or not and finally programmed for polarity (direct or inverted).

- **OR**
 - ITLOUT = masked OR of channel self-triggers
- **AND**
 - ITLOUT = masked AND of channel self-triggers
- **Majority**
 - ITLOUT = masked Majority of channel self-triggers

参数 ITLA/BMajorityLev

Defines the majority level of the Main Logic of the ITL A/B block. The majority output is calculated at every clock cycle, and it becomes TRUE when $Nch \geq MajLev$, where Nch is the number of self-triggers active in that clock cycle and MajLev is the programmed majority level.

Note that when the Pair Logic is used to combine the self triggers two by two (AND/OR), each pair produces two identical signals that will be counted twice in the majority level.

参数 ITLA/BGateWidth

Width of the gate generator at the output of the ITLA/B block.

Unit of Measure: ns

参数 ITLA/BPolarity

Polarity of the gate generator output.

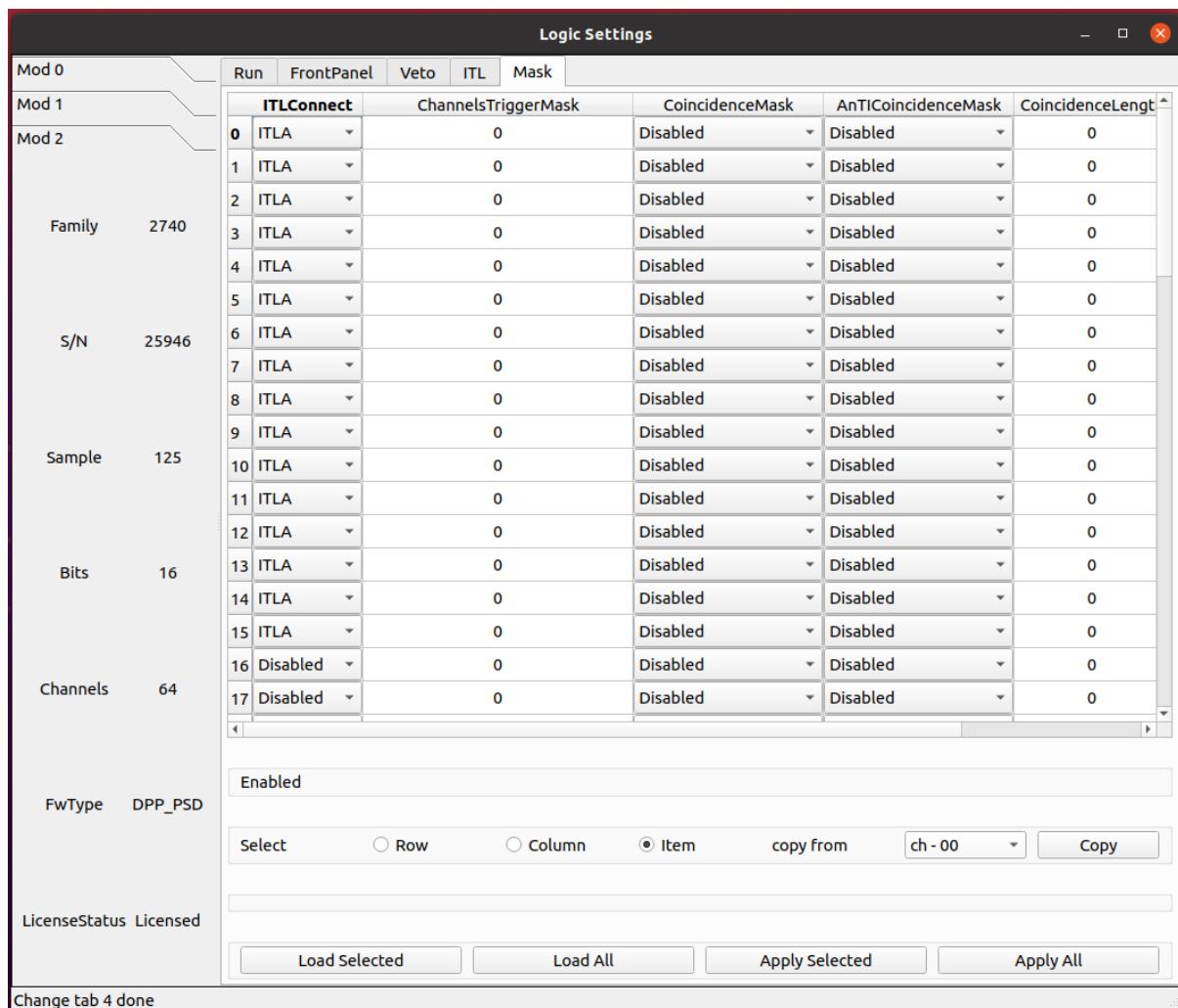
- **Direct**
 - Direct polarity
- **Inverted**
 - Inverted polarity

参数 ITLA/BEnRetigger

Set the ITLA/B to be retriggerable.

- **True**
 - The ITLA/B is retriggerable
- **False**
 - The ITLA/B is not retriggerable

9.2.5 延迟展宽



参数 ITLConnect

Alternative to ITLAMask, ITLBMask. Determines if the channel partecipate in ITLA or ITLB

- **Disabled**
 - The channel is disabled
- **ITLA**
 - The channel participates in ITLA logic block
- **ITLB**

- The channel participates in ITLB logic block

参数 ChannelsTriggerMask

Allows to set the mask over 64 bits to generate a channel trigger. It can be used to trigger a channel using a trigger coming from another channel. It also allows to set the mask over 64 bits to enable the channel to participate in the coincidence logic defined in CoincidenceMask and AntiCoincidenceMask (option Channel64Trg). 64-bit enable mask, each bit representing a channel.

参数 CoincidenceMask

Allows to set the coincidence mask that generates a trigger on the specified channel.

- **Disabled**

- All the coincidence sources are disabled

- **Ch64Trigger**

- One of the 64 channels can generate a coincidence signal

- **TRGIN**

- TRGIN can generate a coincidence signal

- **GlobalTriggerSource**

- Acquisition Trigger can generate a coincidence signal

- **ITLA**

- ITLA can generate a coincidence signal

- **ITLB**

- ITLB can generate a coincidence signal

参数 AntiCoincidenceMask

Allows to set the anticoincidence mask that generates a trigger on the specified channel.

- **Disabled**

- All the coincidence sources are disabled

- **Ch64Trigger**

- One of the 64 channels can generate a coincidence signal

- **TRGIN**

- TRGIN can generate a coincidence signal

- **GlobalTriggerSource**

- Acquisition Trigger can generate a coincidence signal

- **ITLA**

- ITLA can generate a coincidence signal

- **ITLB**

- ITLB can generate a coincidence signal

参数 CoincidenceLength

Coincidence window length in nanoseconds (ns). 16-bit value.

Unit of Measure: ns

CHAPTER 10

ZLE 固件

10.1 基本参数配置

10.1.1 输入信号

参数 ChGain

仅限 x2730.

设置可变增益放大器 (VGA) 的增益。

Unit of Measure: dB

参数 InputDelay

设置输入延迟，单位为采样点。

该值设置每 4 个通道共用一个相同配置。

参数 ChEnable

独立设定每个通道是否开启使用。如果通道不启用，它不提供任何数据，同时它的自触发也关闭。

参数 WaveSource

在正常模式下，采集的波形来源于模拟输入的 A/D 转换产生的 ADC 采样序列。出于测试目的，可以用内部数据生成器替换 ADC 数据。

- **ADC_DATA**
 - Data from the ADC (normal operating mode)
- **ADC_TEST_TOGGLE**
 - Toggle between 0x5555 and 0xAAAA (test mode)
- **ADC_TEST_RAMP**
 - 16-bit ramp pattern (test mode)
- **ADC_TEST_SIN**
 - 8-point sine wave test pattern
- **ADC_TEST_PRBS**
 - 16-bit PRBS generated by a 23-bit PRBS pattern generator (test mode)
- **Ramp**
 - Data from a ramp generator. It is actually a 16-bit field, where the 6 most significant bits identify the channel and the 10 less significant bits are the samples of a ramp from 0x000 up to 0x3FF (i.e. 0 to 1023). It is so a 10-bit ramp with offset given by “channel*1024”. For channel 0, it is a counter from 0 to 1023; for channel 1, it is a counter from 1024 to 2047, and so on
- **IPE**
 - Not implemented
- **SquareWave**
 - Internally generated programmable square wave

参数 DCOffset

对于每个通道，将恒定的 DC 偏移（由 16 位 DAC 控制）添加到模拟输入，以在 ADC 的动态范围内调整信号基线的位置（即模拟输入的“零伏”）。

由于部件的公差，有必要校准偏移 DAC。校准是通过工厂测试完成的，通常不需要重新校准。然而，可以执行新的校准。校准参数存储在板的闪存中，并在通电时加载。每次写入或读取 DCOffset 参数时，内部逻辑会自动应用这些参数。

DCOffset 参数为数字，单位为满刻度的百分比。当 DCOffset 为 0 时，输入信号的基线处于 ADC 0。当 DCOffset 为 100 时，输入信号的基线处于 ADC $2^{\{NBIT\}}-1$ 。

参数 Polarity

设置输入脉冲的极性。

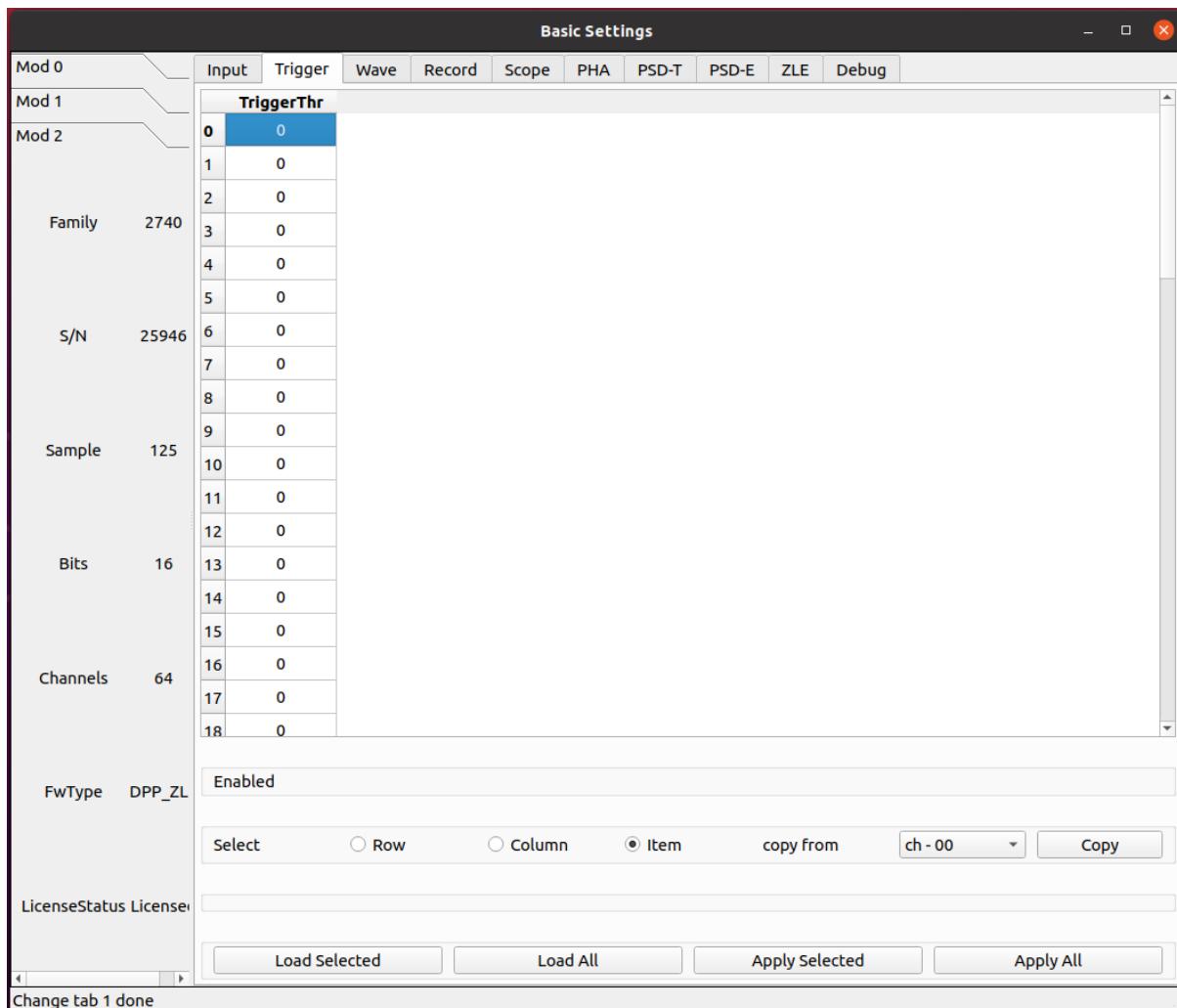
- Positive
 - Positive polarity
- Negative
 - Negative polarity

参数 VGAGain

2745 特有。

以 0.5 dB 为步长设置可变增益放大器（VGA）的增益。参数设置每 16 个通道为一组，64 通道分为 4 组。最小可设置为 0，最大为 40。

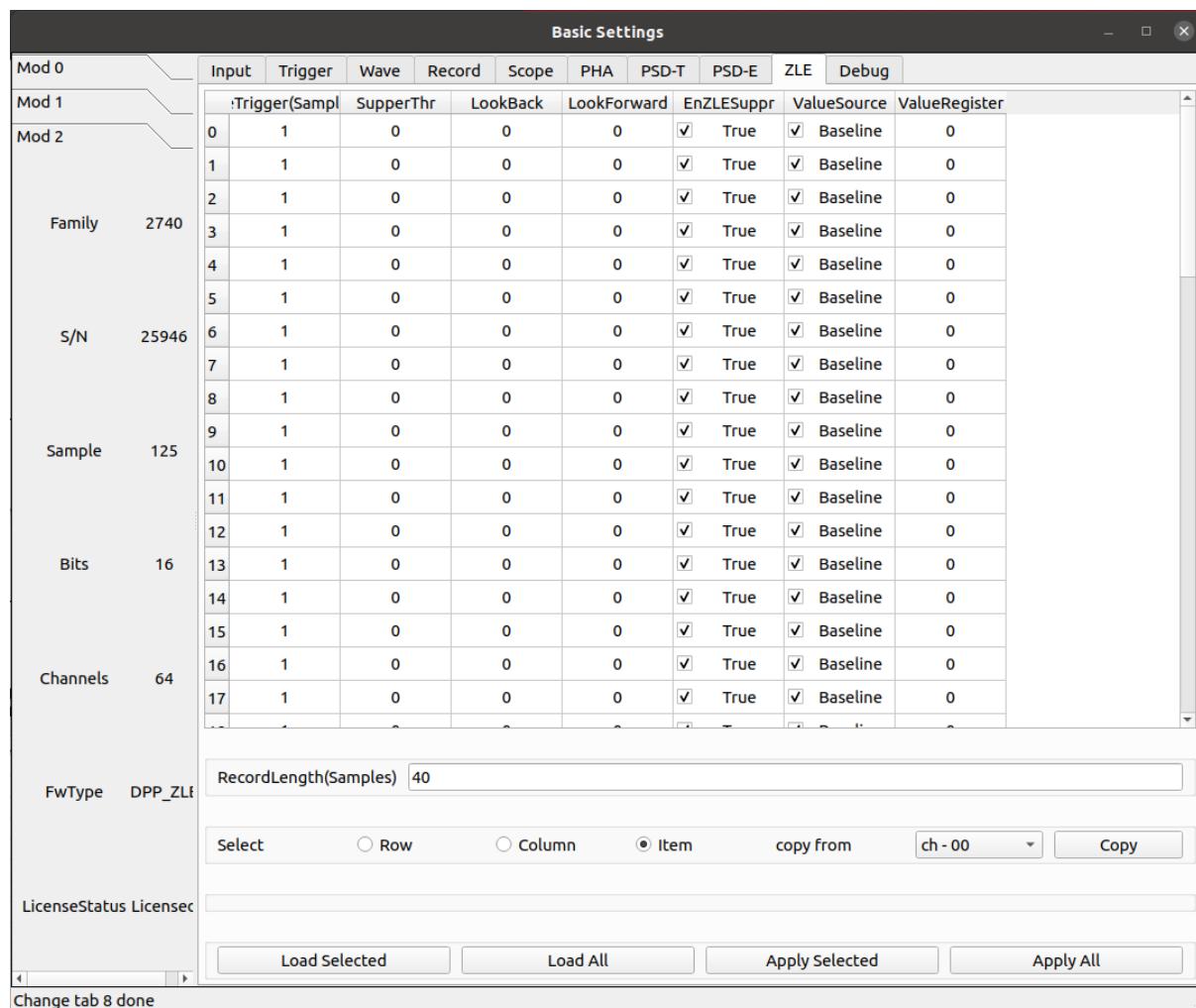
10.1.2 触发



参数 TriggerThr

Each channel of the digitizer has a digital leading-edge discriminator with programmable threshold able to self-trigger on the input pulses and generate a self-trigger signal (or an overthreshold signal) feeding the internal trigger logics or digitizer outputs. This parameter sets the trigger threshold. Typically, the value is relative to the baseline of the signal and the threshold is a 17-bit signed NUMBER number; in this case, the threshold automatically follows the baseline when the DCoffset parameter changes. Sometimes, it is preferable to set an absolute value for the threshold, referred to the ADC range. In this case, the threshold is unsigned NUMBER number.

10.1.3 ZLE 参数



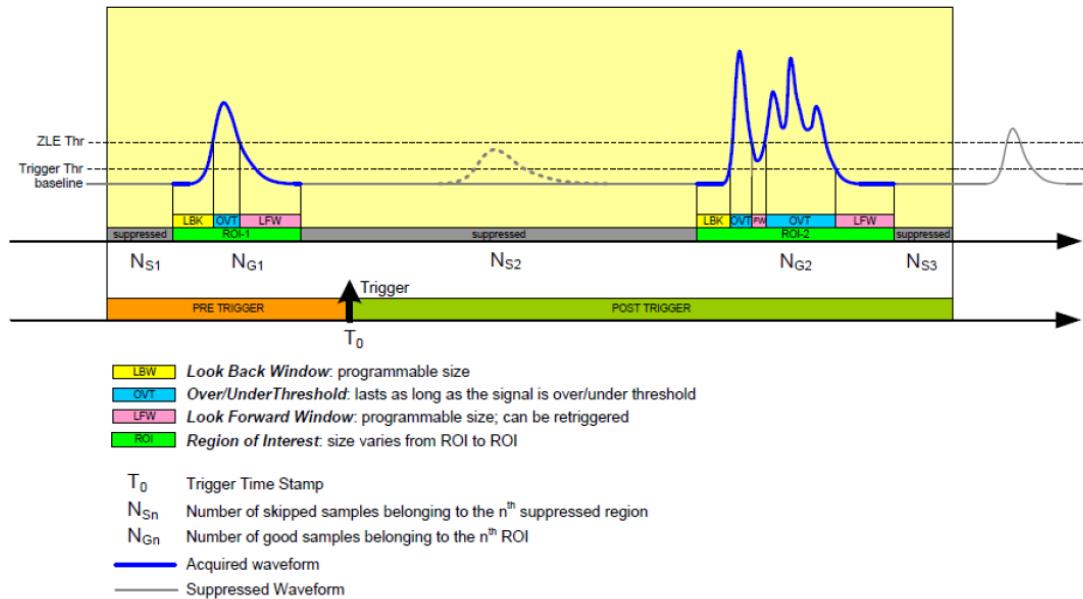
参数 PreTrigger

波形中触发位置之前的样本数（即预触发窗口的大小）。

参数 SupperThr

ZLE 算法进一步检查是否超过了 ZLE 抑制阈值 (SupprThreshold)，并保存过阈值样本（在负极性的情况下低于阈值），这些样本被称为“好”样本。此外，还可以在过/低于阈值之前和之后采集可编程数量的样本（分别为 LookBack 和 LookForward）。丢弃“跳过”的样本；在最终数据中仅记录舍弃的样本数。此参数允许设置 ZLE 数据抑制阈值。

下图显示了 ZLE 算法的参数。信号记录在 ZLE 过阈值之前开始 LookBack 采样（图片中的 LBW），并在相反方向的下阈值之后 LookForward 停止采样。所记录的区域定义了算法的 ROI (感兴趣区域)。在 ROI 之外，算法记录跳过的样本数。



参数 LookBack

This parameter allows to set the ZLE look-back samples.

参数 LookForward

This parameter allows to set the ZLE look-forward samples.

参数 EnZLESuppr

设置是否启用 ZLE 数据压缩。

- **True**
 - ZLE Data reduction is enabled.
- **False**
 - ZLE Data reduction is disabled.

参数 ValueSource

Selection of the default sample value in the payload (baseline or register).

- **Baseline**
 - Default sample value is Baseline.
- **Register**
 - Default sample value is the value.

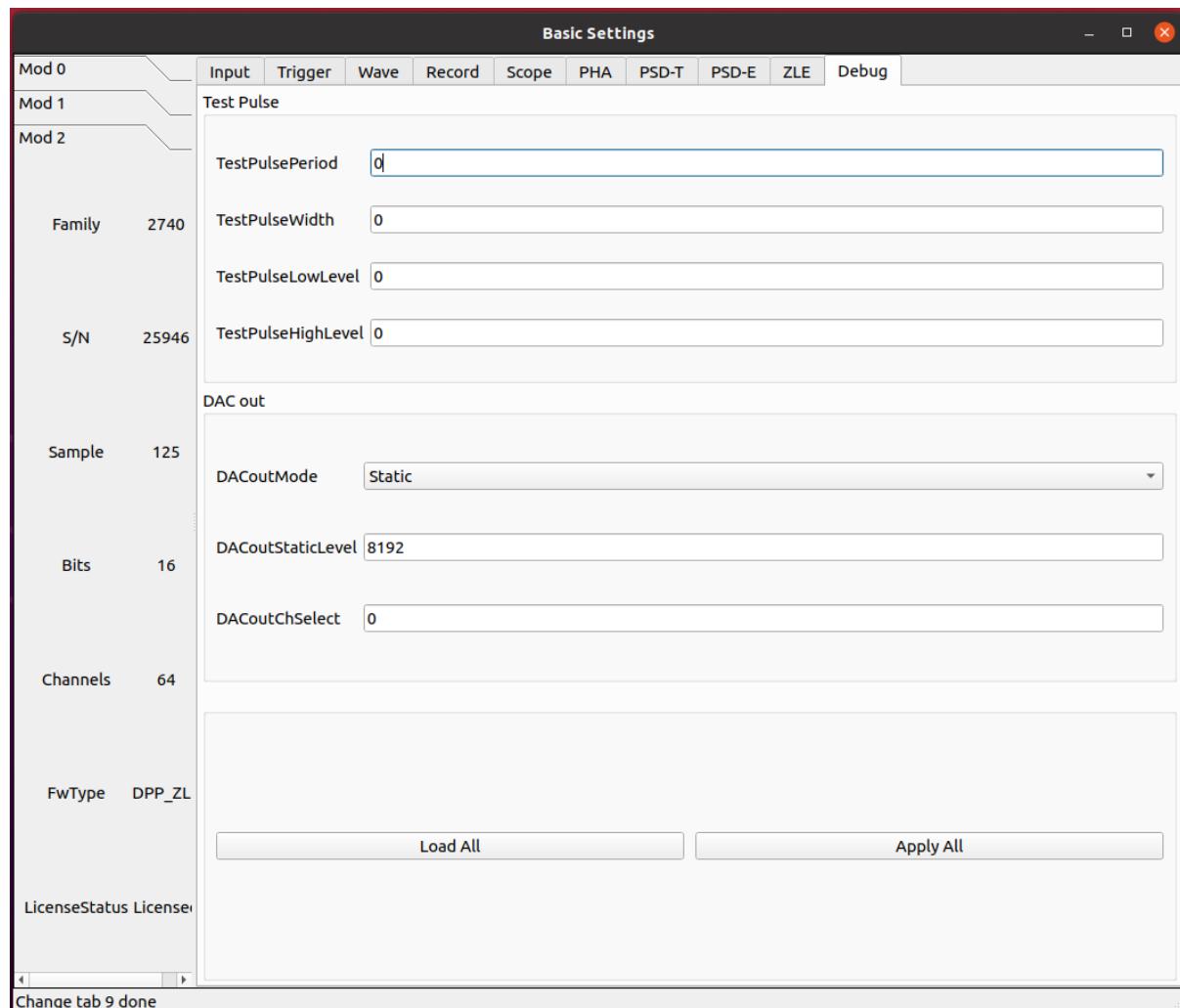
参数 ValueRegister

ZLE 默认采样值寄存器。

参数 RecordLength

波形大小（即采集窗口的大小）。波形的实际大小将自动四舍五入到最接近的允许值。

10.1.4 诊断



参数 TestPulsePeriod

测试脉冲是一种可编程方波，可用作内部周期性触发器（主要用于测试目的）或在 TRGOUT 和 GPIO 输出上生成逻辑测试脉冲（TTL 或 NIM）。此参数设置测试脉冲的周期。

单位为时间, ns

参数 TestPulseWidth

测试脉冲的宽度（信号保持高电平的时间）。

单位为时间， ns

参数 TestPulseLowLevel

以 ADC 道址表示的测试脉冲低电平

参数 TestPulseHighLevel

以 ADC 道址表示的测试脉冲高电平

参数 DACoutMode

选择要在前面板 DAC LEMO 口输出发送的信号类型。

- **Static**
 - DAC output stays at a fixed level, given by the DACoutStaticLevel parameter
- **Ramp**
 - The DAC output is driven by a 14-bit counter
- **Sin5MHz**
 - The DAC output is a sine wave at 5 MHz with fixed amplitude
- **Square**
 - Square wave with period and width set by TestPulsePeriod and TestPulseWidth and amplitude between TestPulseLowLevel and TestPulseHighLevel.
- **IPE**
 - Not implemented
- **ChInput**
 - The DAC reproduces the input signal received by one input channel, selected by the DACoutChSelect parameter
- **MemOccupancy**
 - Level of the memory occupancy (not yet implemented)
- **ChSum**
 - The DAC reproduces the “analog” sum of all the digitizer inputs (not yet implemented)
- **OverThrSum**
 - The DAC output is proportional to the number of channels that are currently above the threshold

参数 DACoutStaticLevel

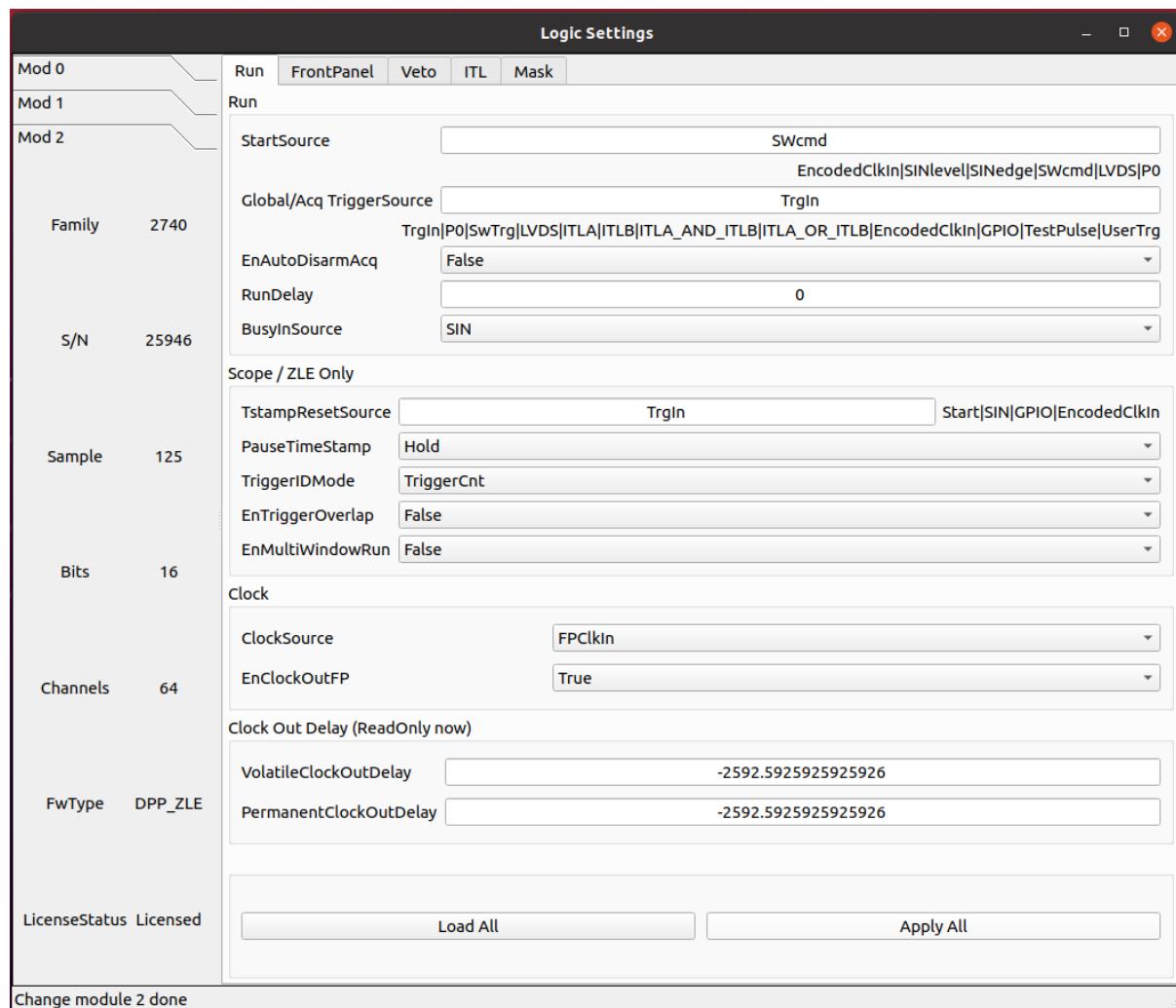
当 DACoutMode = Static 时, 此参数设置 DAC 输出的 14 位电平。

参数 DACoutChSelect

当 DACoutMode = ChInput 时, DAC 输出由该参数选择的通道的输入信号。

10.2 逻辑参数配置

10.2.1 运行



参数 StartSource

Defines the source for the start of run. Multiple options are allowed, separated by “|” .

- **EncodedClkIn**

- Start from CLK-IN/SYNC connector on the front panel. This is a 4-pin connector (LVDS signals) used to propagate the reference clock (typ. 62.5 MHz) and a Sync signal. The rising edge of the Sync starts the acquisition, that lasts until the Sync returns low (falling edge).

- **SINlevel**

- Start from SIN (1=run, 0=stop)

- **SINedge**

- Start from SIN (rising edge = run; stop from SW)

- **SWcmd**

- Start from SW

- **LVDS**

- Start from LVDS

- **FirstTrigger**

- Start on 1st trigger (stop from SW)

- **P0**

- Start from P0 (backplane)

参数 AcqTriggerSource

Defines the source for the Acquisition Trigger, which is the signal that opens the acquisition window and saves the waveforms in the memory buffers. Multiple options are allowed, separated by “|” .

- **TrgIn**

- Front Panel TRGIN

- **P0**

- Trigger from P0 (backplane)

- **SwTrg**

- Software trigger

- **LVDS**

- LVDS trgin

- **ITLA**

- Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**

- Internal Trigger Logic B: combination of channel self-triggers

- **ITLA_AND_ITLB**

- Second level Trigger logic making the AND of ITL A and B

- **ITLA_OR_ITLB**

- Second level Trigger logic making the OR of ITL A and B

- **EncodedClkIn**

- Not implemented (encoded CLK-IN trigger)

- **GPIO**

- Front Panel GPIO

- **TestPulse**

- Internal Test Pulse

- **UserTrg**

- User custom trigger source

参数 EnAutoDisarmAcq

When enabled, the Auto Disarm option disarms the acquisition at the stop of run. When the start of run is controlled by an external signal, this option prevents the digitizer to restart without the intervention of the software.

- **True**

- The acquisition is automatically disarmed after the stop. It is therefore necessary to rearm the digitizer (with the relevant command sent by the software) before starting a new run.

- **False**

- The acquisition is not disarmed after the stop. Multiple transition of the start signal will produce multiple runs.

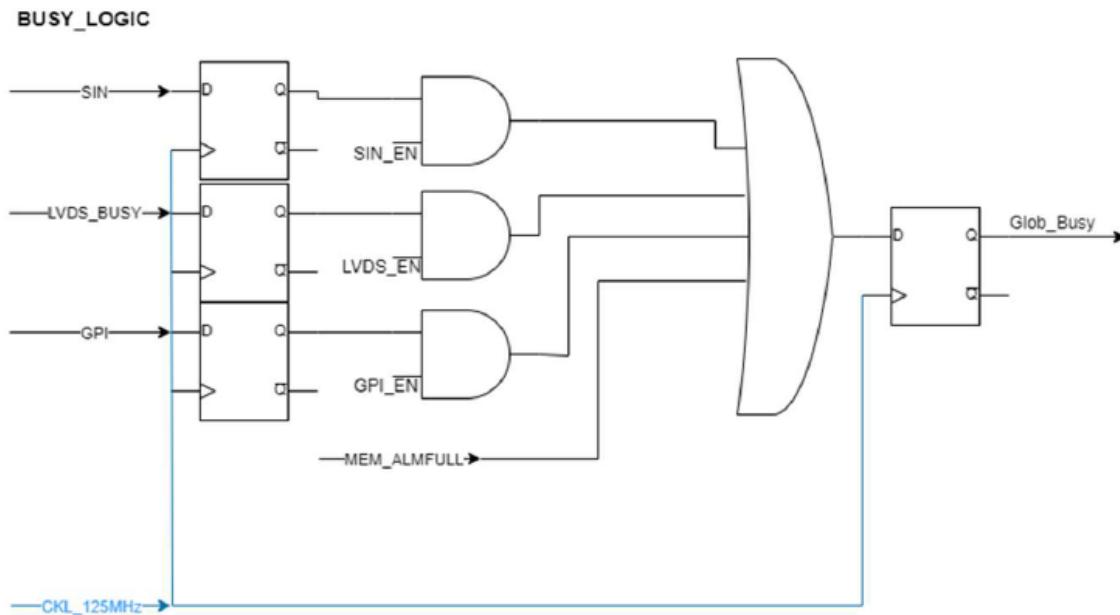
参数 RunDelay

When the start of run is controlled by a RUN signal that is propagated in daisy chain between the boards (for instance through the ClkIn- ClkOut or SIN-GPIO sync chain), it is necessary to compensate for the propagation delay and let the boards start exactly at the same time. The RunDelay parameter allows the start of the acquisition to be delayed by a given number of clock cycles with respect to the rising edge of the RUN signal. Assuming that the propagation delay is 2 cycles, the RunDelay setting will be 0 for the last board in the chain, 2 for the previous one, and so on up 2x(NB-1) for the first one.

Unit of Measure: ns

参数 BusyInSource

In a multi-board system, it might be necessary to prevent one board to accept a new trigger while another board is full and thus unable to accept the same trigger. For this reason, each board can generate a Busy signal to notify that it is unable to get a new trigger. If the busy/veto mechanism has some latency, it is advisable to generate the busy slightly before the digitizer become full. For this purpose, it is possible to assert the busy output when the acquisition memory reaches a certain level of occupancy (internally managed). The OR of the busy signals is typically used to stop the global trigger. It is possible to get the individual busy signals from each board and make an external OR logic or connect the boards with cables to propagate the Busy along the chain. Each board makes an OR between its internal busy and the busy input signal coming from the previous board, thus having a global Busy at the end of the line. This parameter defines the source of the Busy Input (schematized in the figure below)



- **Disabled**
 - The Busy is given by the Internal Busy only (Memory full or almost full)
- **SIN**
 - Busy input from SIN on front panel
- **GPIO**
 - Busy input coming from GPIO on front panel, used as a simple input. It is also possible to use GPIO as a wired OR (bidirectional). In this mode, the Busy line goes high as soon as one board drives it high. All the boards can read the Busy line and use it as a veto for the trigger
- **LVDS**
 - LVDS trigin

参数 TstampResetSource

Defines the source of the timestamp reset. Multiple options are allowed, separated by “|” . The timestamp of the board (internal counter running at 125 MHz) is typically reset at the start of each run, which corresponds to the “zero” of the timestamps. In Multi-board systems, the synchronization of the clock and RUN signals allows event data coming from different boards to be merged and correlated by the time stamp. However, it is possible to configure different ways to control the reset of the time stamp in the cases where it is necessary to synchronize it with an external global time stamping system.

- **Start**
 - Time stamp reset at the start of run
- **SIN**
 - SIN input
- **GPIO**
 - GPIO used as input
- **EncodedClkIn**
 - Not implemented (encoded in CLK-IN/SYNC)

参数 PauseTimeStamp

Allows the time stamp to either stop or run during the pauses of the acquisition

- **Hold**
 - The timestamp stops while pausing the acquisition
- **Run**
 - The timestamp runs while pausing the acquisition

参数 TriggerIDMode

The event data packet contains a 24-bit identifier called TriggerID. This can be the total trigger counter, the saved event counter or a pattern coming from the LVDS I/Os.

- **TriggerCnt**
 - The Event triggerID is associated to the total trigger counter. This is a 24-bit counter that is reset at the start of run and increased with every received trigger, including those ones that are not accepted. In this mode, events coming from multiple boards can be correlated by the triggerID that is supposed to be synchronized. There might be gaps due to lost triggers.
- **EventCnt**
 - The Event triggerID is a sequential number of the saved event. In this case, there are no gaps in the sequence, but it is not guaranteed that the trigger ID of multiple boards are aligned, thus it is not possible to use it for data correlation.
- **LVDSpattern**
 - The triggerID is taken from the 16 LVDS inputs at the time of the trigger arrival. The user can provide an external trigger pattern to correlate the event data between boards or even with other readout electronics

参数 EnTriggerOverlap

Allows a trigger occurring within the acquisition window of a previous trigger to be either accepted or rejected. When accepted, the previous window is prematurely closed and the new window immediately opened, without any dead time between the two.

- **True**
 - Triggers with overlapped acquisition windows are accepted.
- **False**
 - Triggers with overlapped acquisition windows are not accepted. The rejected triggers are counted by the total trigger counter, so that the trigger-ID in the event header allows for tracing the rejected triggers.

参数 EnMultiWindowRun

When the acquisition start and stop are controlled by an external “RUN” signal (e.g. feeding SIN), it is possible to configure the digitizer to work in two different modes:

The RUN signal acts as a start (rising edge) and stop (falling edge). Therefore, multiple transitions of the RUN signal cause multiple runs (provided that the Auto Disarm option is disabled). At every start of run, the timestamp is reset, and all the statistics and counters are cleared. Typically, the software produces different output files.

The RUN signal acts as “enable” of the acquisition: once the digitizer has been armed, the first rising edge of RUN starts the acquisition. When RUN goes down, the acquisition is “paused” rather than

stopped. This means that all data and statistics are frozen, and the timestamp can be either stopped or left running, depending on the PauseTimeStamp parameter. The RUN signal can toggle multiple times within the same acquisition. The stop of the acquisition will be done by a software command. It is necessary to disarm and rearm the acquisition before starting a new run with the rising edge of the RUN signal.

- **True**
 - MultiWindow run is enabled. The RUN signal acts as start (first rising edge) and pause (subsequent falling edges) for the acquisition. The stop of the acquisition is always given by a software command
- **False**
 - The RUN signal acts as start and stop for the acquisition

参数 ClockSource

This is the source of the system clock. Multiple options are not allowed

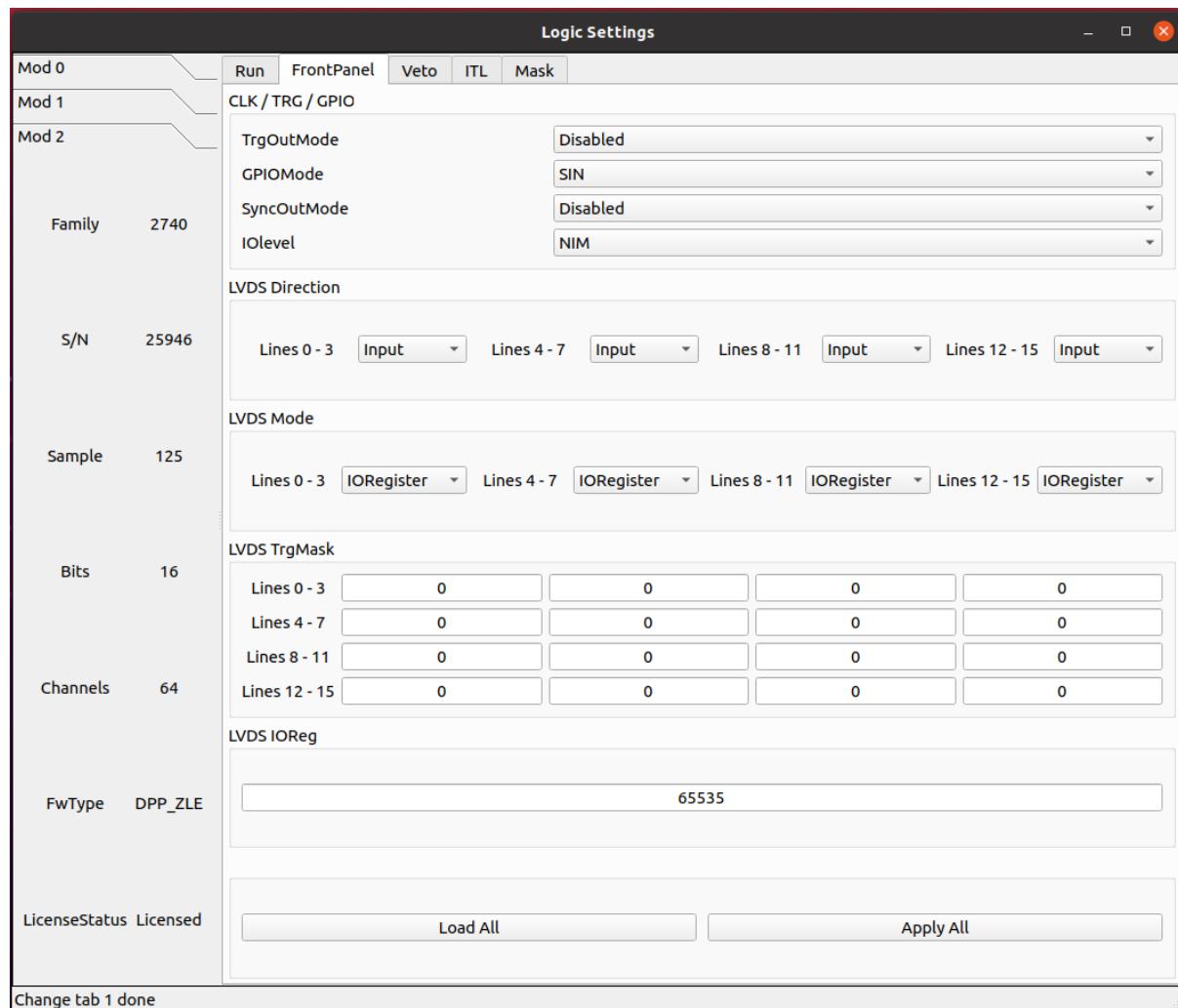
- **Internal**
 - Local oscillator, 62.5 MHz
- **FPClkIn**
 - Front Panel Clock input

参数 EnClockOutFP

Enables clock output on Front Panel for the daisy chain propagation of the clock between multiple boards.

- **True**
 - Enabled
- **False**
 - Disabled

10.2.2 模块前面板



参数 TrgOutMode

Selects the signal that is routed to the TRGOOUT output. Multiple options are not allowed.

- **Disabled**
 - TRGOOUT output disabled
- **TrgIn**
 - Propagation of Front Panel TRGIN (TRGOOUT is a replica, with some delay, of the TRGIN signal)
- **P0**
 - Propagation of P0 trigger
- **SwTrg**
 - Software trigger
- **LVDS**
 - LVDS trgin
- **ITLA**
 - Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**
 - Internal Trigger Logic B: combination of channel self-triggers
- **ITLA_AND_ITLB**
 - Second level Trigger logic making the AND of ITL A and B
- **ITLA_OR_ITLB**
 - Second level Trigger logic making the OR of ITL A and B
- **EncodedClkIn**
 - Not implemented (propagation of the Encoded CLK-IN trigger)
- **Run**
 - Propagation of the RUN signal (acquisition start/stop), before applying the delay given by the Run-Delay parameter
- **RefClk**
 - Monitor of the 62.5 MHz clock (used for phase alignment)
- **TestPulse**
 - Internal Test Pulse
- **Busy**
 - Busy of the board
- **UserTrgout**
 - Trgout coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal
- **SyncIn**
 - SyncIn signal
- **SIN**
 - SIN connector signal
- **GPIO**
 - GPIO connector signal
- **LBinClk**
 - Internal Logic B clock signal
- **AcceptTrg**
 - Accepted triggers signal
- **TrgClk**
 - Trigger clock signal

参数 GPIOMode

Selects the signal that is routed to the GPIO, when this is used as output. Multiple options are not allowed. The GPIO on the front panel is a bidirectional signal that can be used in three different ways:

As independent board output (each board drives its own GPIO)

As a shared input for the boards: the signal is driven high (= 1) or low (= 0) by an external source and connected in “short circuit” among multiple boards using “T” connectors at the inputs. The GPIO is not internally terminated, thus it is necessary to put a 50 Ohm terminator at the end of the line (last “T” of the chain)

As a shared bidirectional line, making a “wired OR”. One or more boards can simultaneously drive the signal high (= 1). If no board drives the GPIO, it remains low (= 0). All boards can read back the signal. It is necessary to put a 50 Ohm terminator at both ends of the line (first and last “T” of the chain). This mode can be used to generate, for instance, the global Busy and Veto logic for multiple boards.

- **Disabled**

- GPIO disabled

- **TrgIn**

- Propagation of Front Panel TRGIN (GPIO is a replica, with some delay, of the TRGIN signal)

- **P0**

- Propagation of P0 trigger

- **SIN**

- Propagation of SIN

- **LVDS**

- LVDS trgin

- **ITLA**

- Internal Trigger Logic A: combination of channel self-triggers

- **ITLB**

- Internal Trigger Logic B: combination of channel self-triggers

- **ITLA_AND_ITLB**

- Second level Trigger logic making the AND of ITL A and B

- **ITLA_OR_ITLB**

- Second level Trigger logic making the OR of ITL A and B

- **EncodedClkIn**

- Not implemented (propagation of the Encoded CLK-IN trigger)

- **SwTrg**

- Software trigger

- **Run**

- Propagation of RUN

- **RefClk**

- Monitor of the 62.5 MHz clock (used for phase alignment)

- **TestPulse**

- Internal Test Pulse

- **Busy**
 - Busy of the board
- **UserGPO**
 - GPO coming from the User Logic (open FPGA)
- **Fixed0**
 - 0 level signal
- **Fixed1**
 - 1 level signal

参数 SyncOutMode

In a multi-board system, it can be useful to propagate a synchronous signal together with the clock (to synchronize the start of the run, for example) on CLK OUT front panel connector. This parameter defines which signal must be sent out. Multiple options are not allowed.

- **Disabled**
 - SyncoutMode is disabled
- **SyncIn**
 - SyncIn signal (if provided with clkIn on CLK IN connector)
- **TestPulse**
 - Internal Test Pulse
- **IntClk**
 - Internal 62.5 MHz clock (for test purposes)
- **Run**
 - Propagation of RUN signal
- **User**
 - User customSyncoutMode

参数 IOlevel

Sets the electrical logic level of the LEMO I/Os (TRGIN, SIN, TRGOUT, GPIO).

Note that TRGIN and SIN are internally terminated to 50 Ohm, while GPIO and TRGOUT require the termination to 50 Ohms at the receiver

- **NIM**
 - NIM logic (0 = 0V, 1 = -0.8V, that is -16mA)
- **TTL**
 - Low Voltage TTL logic (0 = 0V, 1 = 3.3V)

参数 LVDSDirection

Assigns the direction to a quartet of LVDS I/Os.

- **Input**

- The LVDS lines of the relevant quartet are used as input. The relevant LED on the front panel is OFF.

- **Output**

- The LVDS lines of the relevant quartet are used as output. The relevant LED on the front panel lights-up.

参数 LVDSMode

The digitizer is equipped with 16 LVDS I/Os that can be programmed to be inputs or outputs by groups of 4 (quartets), depending on the LVDSDirection parameter. Once the direction has been selected, it is possible to select the functionality of the LVDS lines, individually for each quartet.

- **SelfTriggers**

- This option is available only when the LVDS are set as outputs. Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by the LVDSTrgMask parameter(16 independent masks, one per LVDS line)

- **Sync**

- Whatever is the direction of the quartet, the 4 lines are rigidly assigned to specific acquisition signals:
0 = Run 1 = Trigger 2 = Busy 3= Veto It is possible to implement a daisy chain distribution of these signals using one quartet as input and another one as output

- **IORRegister**

- The LVDS lines of the quartet are statically controlled by the LVDSIORReg parameter. Use the SetValue function to set the relevant LVDS lines when programmed as output. Use GetValue to read the status of the LVDS lines when programmed as inputs.

- **User**

- User custom.

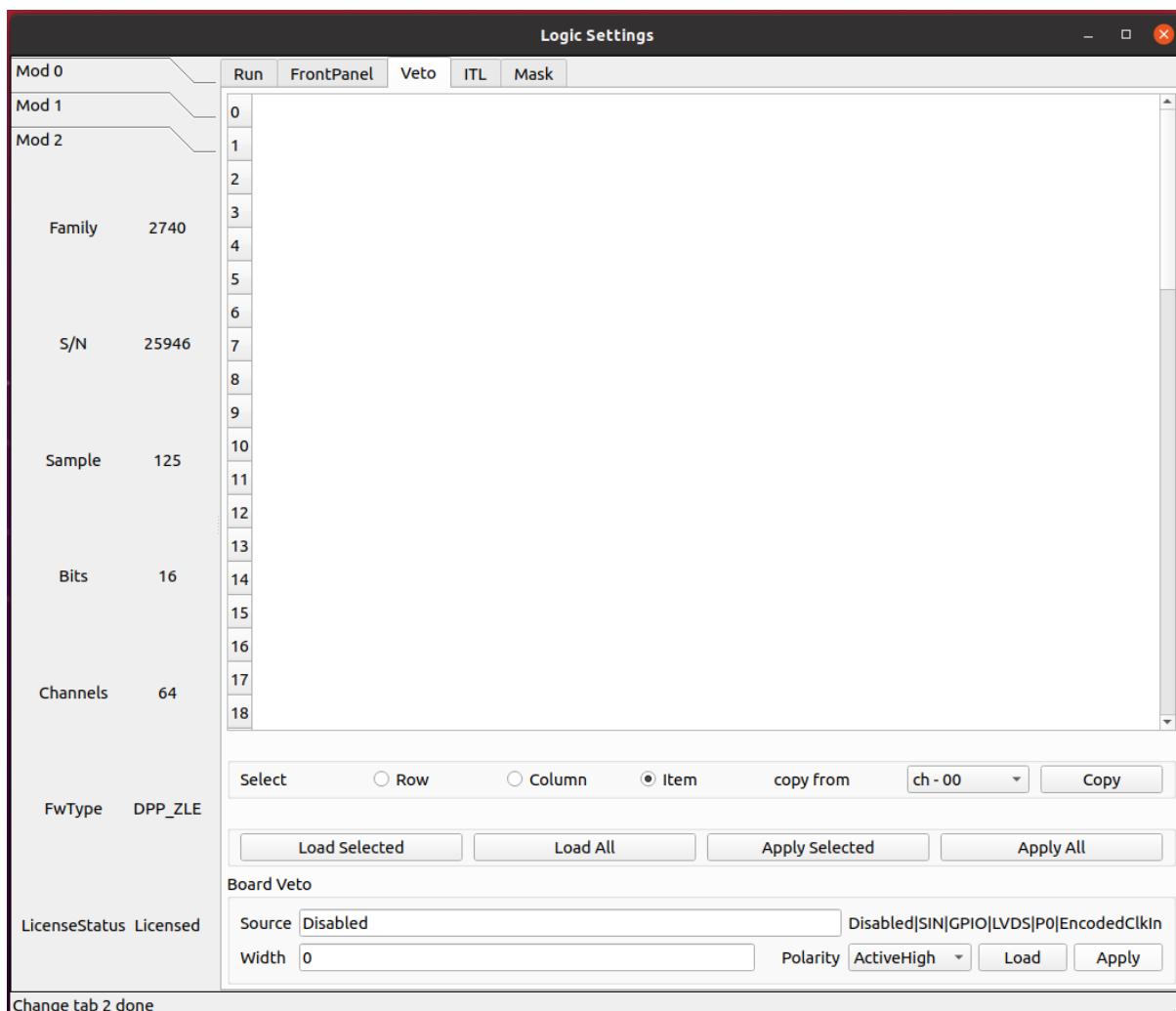
参数 LVDSTrgMask

Each LVDS line can be assigned to a combination of the 64 self-triggers, implemented as a masked OR, where the mask is set by this parameter. There are 16 independent masks, one per LVDS line. Note that the trigger mask assignment does not imply the LVDS direction and mode settings. It is therefore necessary to set the Direction = Output and Mode = SelfTriggers to use the Self-Trigger propagation to the LVDS I/Os.

参数 LVDSIORReg

Set the status of the LVDS I/O for the quartets when they are programmed to be output and Mode = IORRegister. This parameter reads out the status of the quartets in the case the LVDS I/O are programmed as inputs (possibly externally driven).

10.2.3 反符合



参数 VetoSource

Defines the source for the Veto, which is the signal that inhibits the acquisition trigger. Multiple options are allowed, separated by “|”. The VETO signal can be either active high or low, depending on the VetoPolarity parameter. When active low, it acts as a GATE for the trigger. It is possible to stretch the duration of the VETO by means of the parameter VetoWidth.

- **Disabled**
 - VETO is always OFF
- **SIN**
 - SIN on the front panel
- **GPIO**
 - GPIO on the front panel (used as input)
- **LVDS**
 - LVDS trgin
- **P0**
 - P0 (signal from the backplane)

- **EncodedClkIn**
 - Not implemented (encoded CLK-IN veto)

参数 VetoWidth

Whatever is the source of the VETO signal, it is possible to stretch the duration of the veto up to a given time by means of a re-triggerable monostable. When 0, the monostable is disabled and the veto lasts as long as the selected source is active.

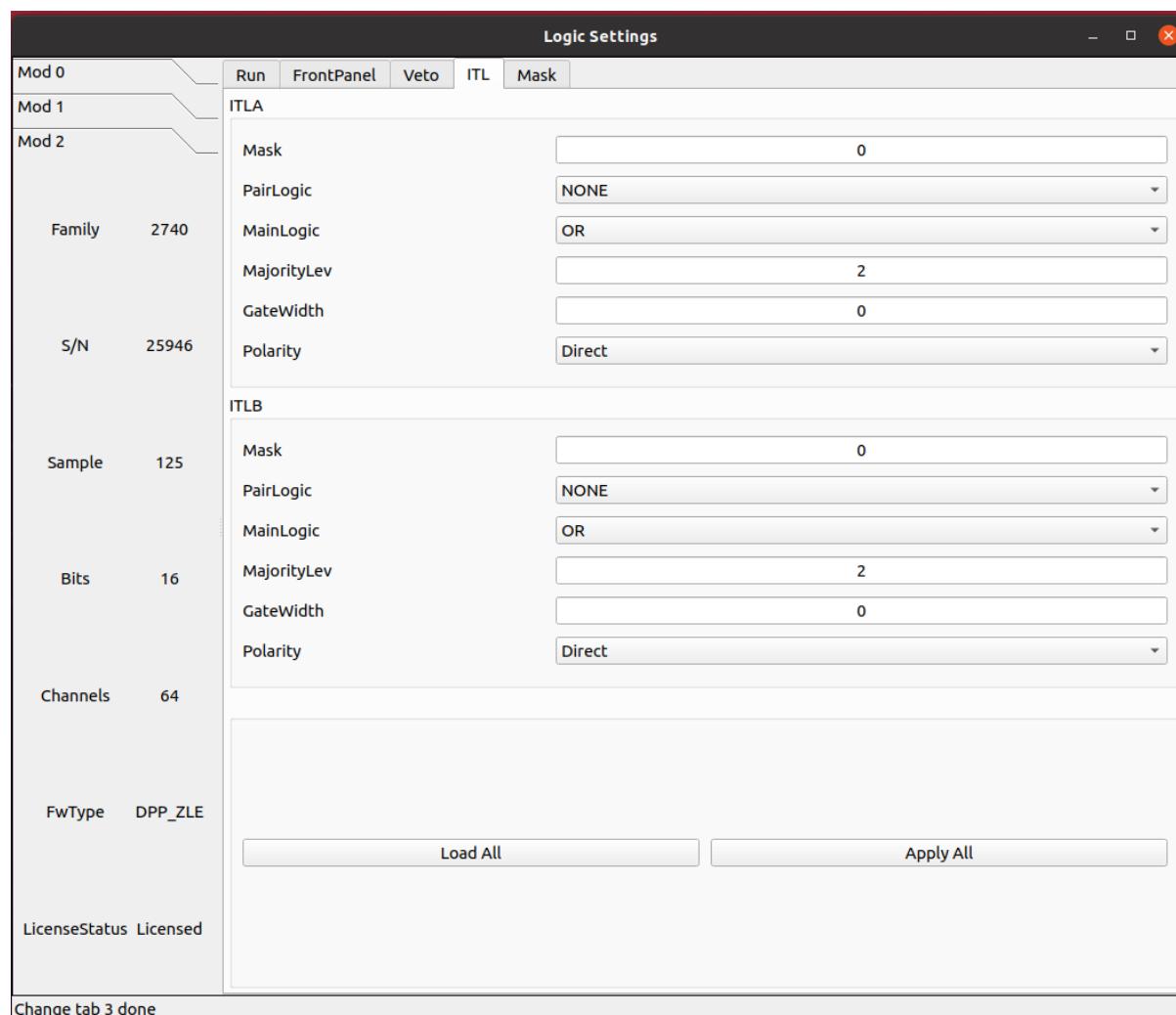
Unit of Measure: ns

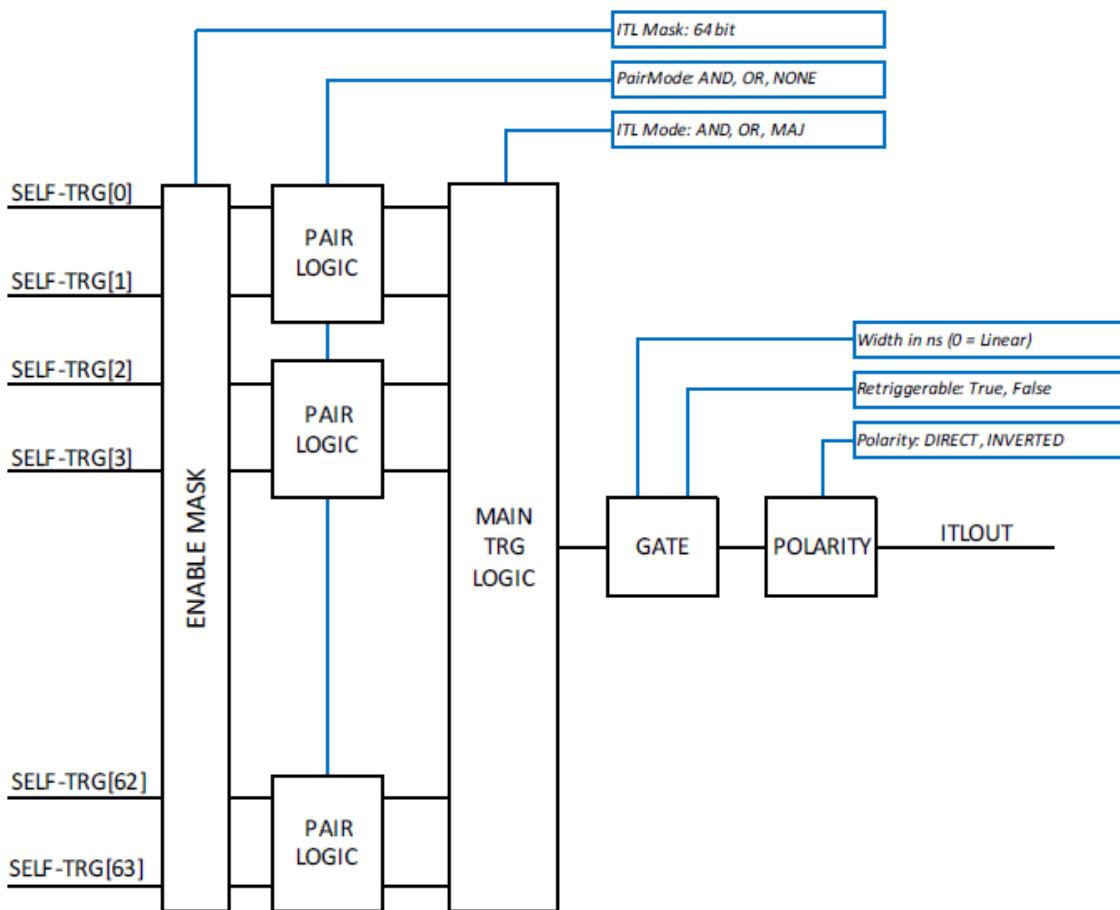
参数 VetoPolarity

Defines the polarity of the Veto

- **ActiveHigh**
 - Veto is active high. The signal acts as an “Inhibit” for the trigger
- **ActiveLow**
 - Veto is active low. The signal acts as a “Gate” the trigger

10.2.4 ITL 逻辑





参数 ITLA/BMask

Enable Mask at the input of the ITLA/B.

参数 ITLA/BPairLogic

Pairs of channels can be combined with an OR or AND before feeding in the Main trigger Logic. This is typically used in the readout of tubes or scintillator bars, where the two ends are read in coincidence, for instance in position sensitive detectors (the coincidence window will be set by the SelfTriggerWidth parameter). When the AND/OR logic is applied, the two outputs of the Pair Logic blocks are identical.

Note that they are counted twice in the following Majority logic. If the Pair Logic is disabled (“NONE” option), the block is transparent, and the two outputs are just a replica of the inputs.

- **OR**
 - Both Pair Logic Outputs = OR of two consecutive self-triggers
- **AND**
 - Both Pair Logic Outputs = AND of two consecutive self-triggers
- **NONE**
 - Outputs = Inputs

参数 ITLA/BMainLogic

Each channel of the digitizer feature a digital bipolar triangular filter discriminator with programmable rise time and threshold able to self-trigger on the input pulses and generate a self-trigger signal. In DPP Mode, the channels acquire independently, so the channel self-trigger is used locally to acquire a waveform. The trigger threshold is then referred to the bipolar triangular filter, and the threshold crossing arms the event selection. The trigger fires at the zero crossing of the time filter signal. The user can see the derivative trace on the signal inspector. It is also possible to combine all the self-triggers of the board, according to a specific trigger logic. There are two independent logic blocks, ITLA and ITLB. Their output can be used separately to feed, for instance, AcqTrigger and TrgOut, or combined in a second level trigger logic to implement more complex trigger schemes. Therefore, the ITLs can either generate the local acquisition trigger, common to all the channels, for the acquisition of the waveform, or propagate the signal outside, through the TRGOUT, thus making it possible to combine triggers of multiple boards in an external trigger logic, that eventually feeds back the TRGIN of the digitizers. Each ITL is made of an input enable mask (64 bits, one per channel), an optional pairing logic that combines the self triggers of two consecutive channels (e.g. paired coincidence) and the main trigger logic that combines the 64 selftriggers with an OR, AND or Majority logic. The output can be linear (no stretching) or reshaped by a programmable gate generator, either re-triggerable or not and finally programmed for polarity (direct or inverted).

- **OR**
 - ITLOUT = masked OR of channel self-triggers
- **AND**
 - ITLOUT = masked AND of channel self-triggers
- **Majority**
 - ITLOUT = masked Majority of channel self-triggers

参数 ITLA/BMajorityLev

Defines the majority level of the Main Logic of the ITL A/B block. The majority output is calculated at every clock cycle, and it becomes TRUE when $Nch \geq MajLev$, where Nch is the number of self-triggers active in that clock cycle and MajLev is the programmed majority level.

Note that when the Pair Logic is used to combine the self triggers two by two (AND/OR), each pair produces two identical signals that will be counted twice in the majority level.

参数 ITLA/BGateWidth

Width of the gate generator at the output of the ITLA/B block.

Unit of Measure: ns

参数 ITLA/BPolarity

Polarity of the gate generator output.

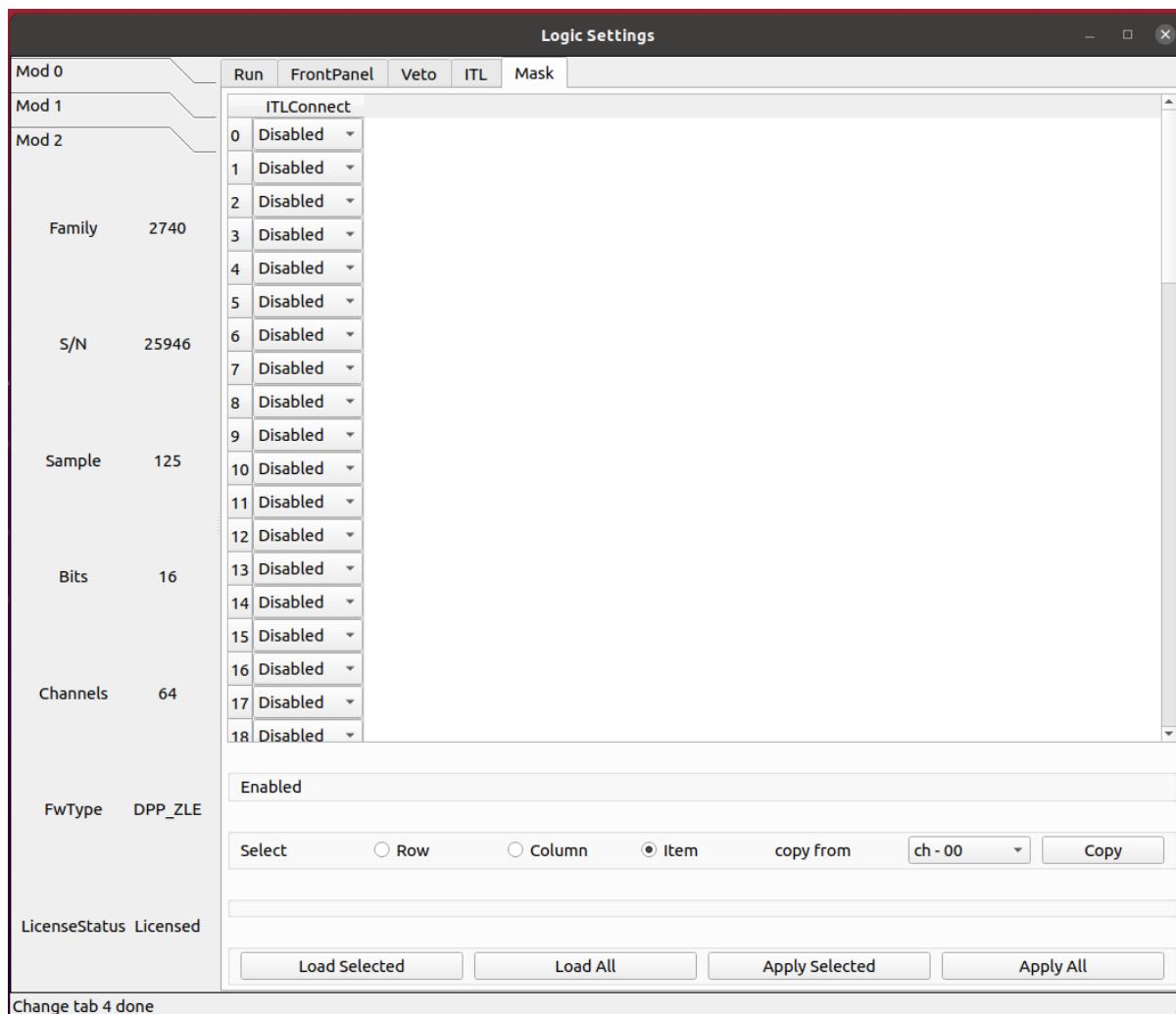
- **Direct**
 - Direct polarity
- **Inverted**
 - Inverted polarity

参数 ITLA/BEnRetrigger

Set the ITLA/B to be retriggerable.

- **True**
 - The ITLA/B is retriggerable
- **False**
 - The ITLA/B is not retriggerable

10.2.5 延迟展宽



参数 ITLConnect

Alternative to ITLAMask, ITLBMask. Determines if the channel partecipate in ITLA or ITLB

- **Disabled**
 - The channel is disabled
- **ITLA**
 - The channel participates in ITLA logic block
- **ITLB**

- The channel participates in ITLB logic block

CHAPTER 11

开放 FPGA

CAEN 开放 FPGA 包括两个开发模式，一个是图形化的软件 SCI-Compiler，适合于没有 FPGA 编程基础的人开发固件；另一个是非公开的 Open FDK，适合于专业的 FPGA 开发人员。这两个模式开发的固件，可以通过固件的信息来区分。我们发布的固件为 Open FDK 开发。

Firmware

This page allows you to upload a new CUP file (firmware image) to your digitizer and select which firmware to run as the default or current version. The 'current' firmware is the one currently running on the digitizer, while the 'default' firmware is the one loaded at startup. You can switch between the loaded firmware on-the-fly, except in cases where changing the communication link is required.

Storage Space Usage:

16%

[Upload new firmware...](#)

2024040906	ETH 1G	Current	⋮
V2740 Open DPP 2024040906 generated by CAEN Open FDK			
2024031601	ETH 1G	⋮	⋮
V2740 OpenDPP firmware generated by SCI-Compiler			
2023112703	ETH 1G	Default	⋮
DPP-PHA			
2023091902	ETH 1G	⋮	⋮
DPP-ZLE			
2023091901	ETH 1G	⋮	⋮
DPP-PSD			
2023091900	ETH 1G	⋮	⋮
Scope			
2022052302	ETH 1G	Factory	⋮
Factory firmware Scope			

SCI-Compiler 开发的固件，运行的采集模块需要有 SCI-Compiler Runtime license，否则只能运行 30 分钟，可通过重启来重新获得 30 分钟的测试时间。

Firmware

This page allows you to upload a new CUP file (firmware image) to your digitizer and select which firmware to run as the default or current version. The 'current' firmware is the one currently running on the digitizer, while the 'default' firmware is the one loaded at startup. You can switch between the loaded firmware on-the-fly, except in cases where changing the communication link is required.

Storage Space Usage:

<div style="width: 100px; height: 10px; background-color: #2e6b2e; margin-bottom: 5px;"></div> <div style="width: 900px; height: 10px; background-color: #cccccc; margin-bottom: 5px;"></div>	16%	Upload new firmware...
2024040906	<small>ETH 1G</small>	<small>Current</small> <small>⋮</small>
V2740 Open DPP 2024040906 generated by CAEN Open FDK		<small>⋮</small>
2024031601	<small>ETH 1G</small>	<small>⋮</small>
V2740 OpenDPP firmware generated by SCI-Compiler		<small>⋮</small>
2023112703	<small>ETH 1G</small>	<small>Default</small> <small>⋮</small>
DPP-PHA		<small>⋮</small>
2023091902	<small>ETH 1G</small>	<small>⋮</small>
DPP-ZLE		<small>⋮</small>
2023091901	<small>ETH 1G</small>	<small>⋮</small>
DPP-PSD		<small>⋮</small>
2023091900	<small>ETH 1G</small>	<small>⋮</small>
Scope		<small>⋮</small>
2022052302	<small>ETH 1G</small>	<small>Factory</small> <small>⋮</small>
Factory firmware Scope		<small>⋮</small>

Open FDK 开发的固件，对采集卡没有任何 license 要求。

CHAPTER 12

UserDPP 固件

吴鸿毅开发固件，本固件侧重于特殊算法的实现。

目前支持 2740/2745/2730 固件定制，欢迎有特殊固件需求的老师联系我们。

2730 的固件，FPGA 运行时钟为 125 MHz。每个时钟的四个采样点相加作为一个采样点处理。

12.1 基本参数配置

12.1.1 输入信号

Basic Settings												
Mod 0		Input	Trigger	Wave	Record	Scope	PHA	PSD-T	PSD-E	ZLE	Debug	UserDPP
		ChGain	ChEnable	WaveSource		DCOffset(%)	SignalOffset	GainFactor	ADCToVolts			
Family	2730	0	0	<input checked="" type="checkbox"/>	True	ADC_DATA	90.002	0	0.988227	0.000247064		
		1	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.989006	0.000246870		
		2	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.982689	0.000248457		
		3	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.983987	0.000248129		
		4	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.985718	0.000247693		
		5	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.981823	0.000248676		
S/N	51413	6	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.986064	0.000247606		
		7	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.984419	0.000248020		
		8	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.998698	0.000244474		
		9	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.994977	0.000245388		
		10	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.992986	0.000245880		
		11	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.992294	0.000246052		
Sample	500	12	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.980612	0.000248983		
		13	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.985025	0.000247867		
		14	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.980352	0.000249049		
		15	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.983641	0.000248216		
		16	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.998352	0.000244559		
		17	0	<input type="checkbox"/>	False	ADC_DATA	50.003	0	0.997919	0.000244665		
Channels	32											
FwType	DPP_OPE	VGAGain	0.0		0.0		0.0		0.0			
		Select	<input type="radio"/>	Row	<input type="radio"/>	Column	<input checked="" type="radio"/>	Item	copy from	ch - 00	Copy	
LicenseStatus	Licensed											
		<input type="button" value="Load Selected"/>			<input type="button" value="Load All"/>			<input type="button" value="Apply Selected"/>		<input type="button" value="Apply All"/>		

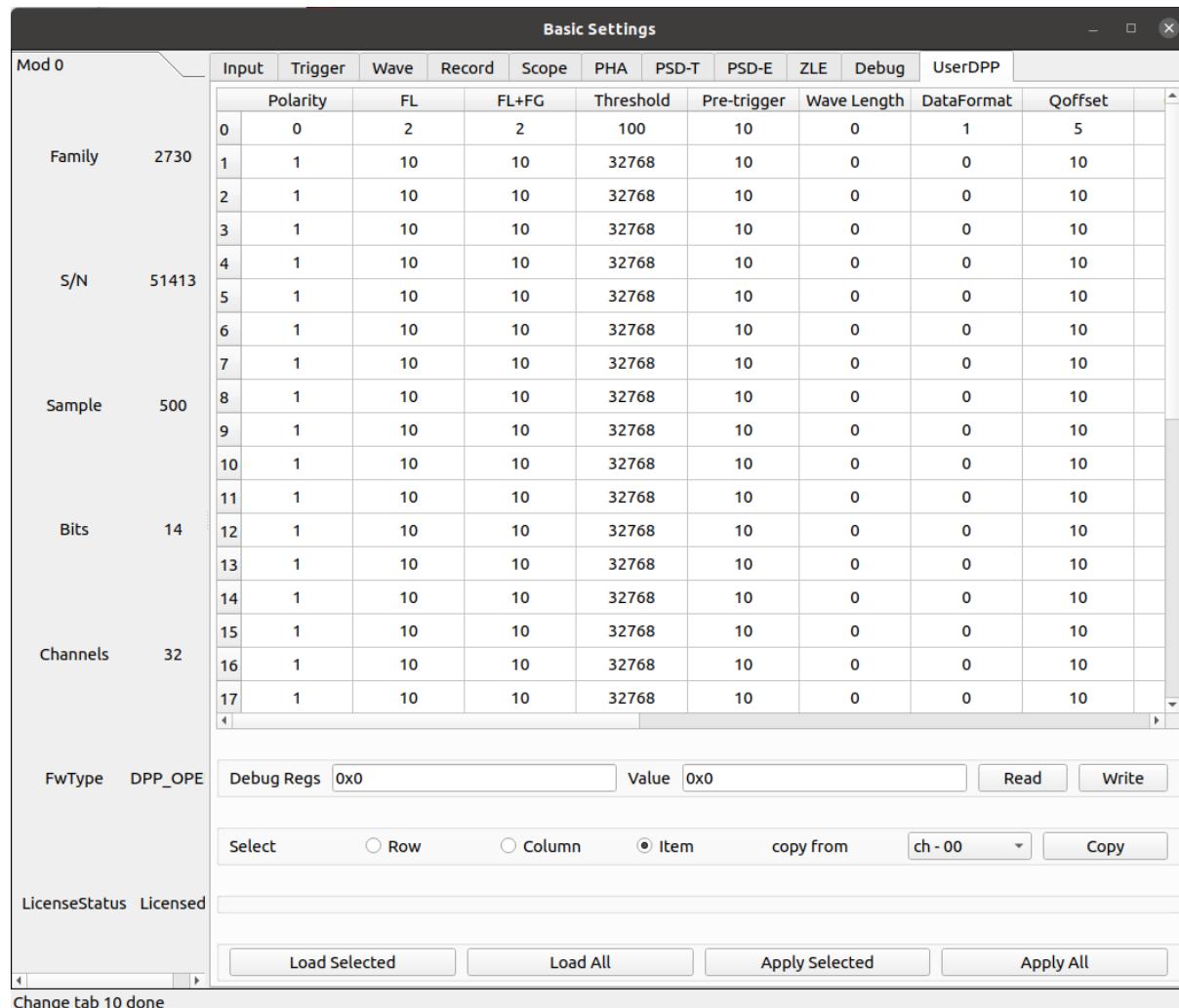
参数 ChEnable

独立设定每个通道是否开启使用。如果通道不启用，它不提供任何数据，同时它的自触发也关闭。

参数 DCOffset

当输入信号为正极性时，DCOffset 0% 为道址 0；当输入信号为负极性时，DCOffset 100% 时为道址 0。

12.1.2 UserDPP



参数 Polarity

当输入信号为正极性时设置为 1，负极性时设置为 0。

参数 FL

XIA fast filter 的参数，快梯形滤波参数

FL 单位为 8 ns。可设置参数为 1-127

参数 FL+FG

快梯形滤波参数

FL+FG 单位为 8 ns, 参数需大于等于 FL。可设置参数为 1-127

参数 Threshold

快梯形滤波的触发阈值

参数 Pre-trigger

当记录波形时候，触发前的长度

参数 Wave Length

当参数值大于 0 时，则记录波形

单位为 4 个采样点。

参数 DataFormat

当参数为 0 时，只输出时间，QDC 等信息。

当参数为 1 时，额外输出 RT 参数，梯形三段积分等信息。

参数 Qoffset

QDC 积分的触发延迟。单位为 8 ns

参数 Qshort

QDC 积分短门。单位为 8 ns

参数 Qlong

QDC 积分长门。单位为 8 ns

参数 QGainShift

QDC 积分短门、长门积分数值，输出前向右移位。用来调节能谱增益。

可设置参数为 0-7

参数 2^n BL

移动平均计算基线，参与平均点的个数为 2^n

可设置参数 1-10

参数 BL Hold

基线计算抑制。当当前触发与上一个触发间隔大于设置参数时，更新基线数值。

单位为 8 ns

参数 RT offset

RT 鉴别算法积分起点偏置。单位为 8 ns

参数 RT gate

RT 鉴别算法积分门。单位为 8 ns

参数 XIAoffset

此参数为 SL+SG 减去触发前保留的采样点

单位为 8 ns

参数 SL

梯形参数的上升沿长度。

单位为 8 ns

参数 SG

梯形参数的平台长度。

单位为 8 ns

12.2 逻辑参数配置

CHAPTER 13

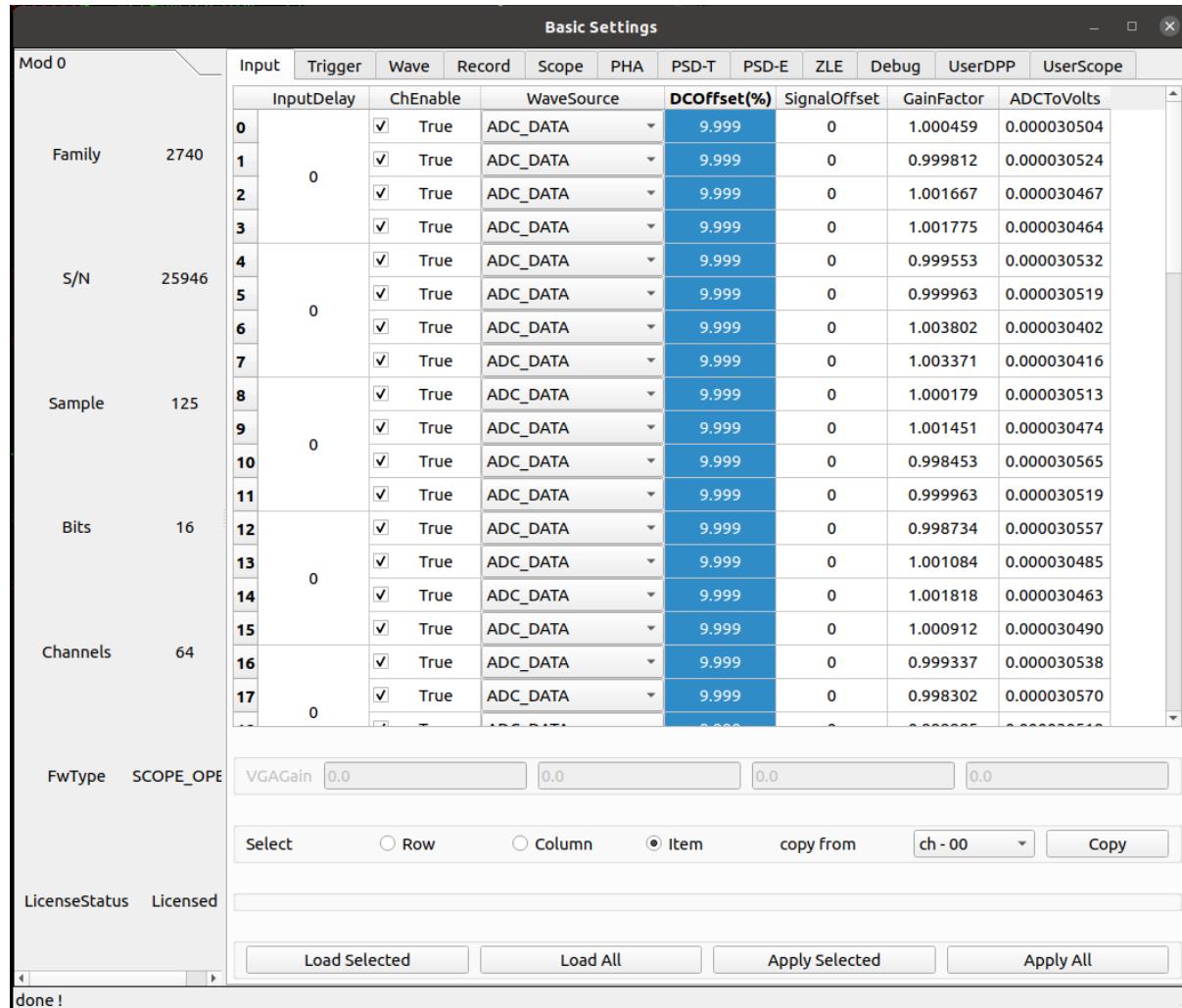
UserScope 固件

吴鸿毅开发固件，本固件侧重于记录超长波形。

目前支持 2740/2745 固件定制，欢迎有特殊固件需求的老师联系我们。

13.1 基本参数配置

13.1.1 输入信号



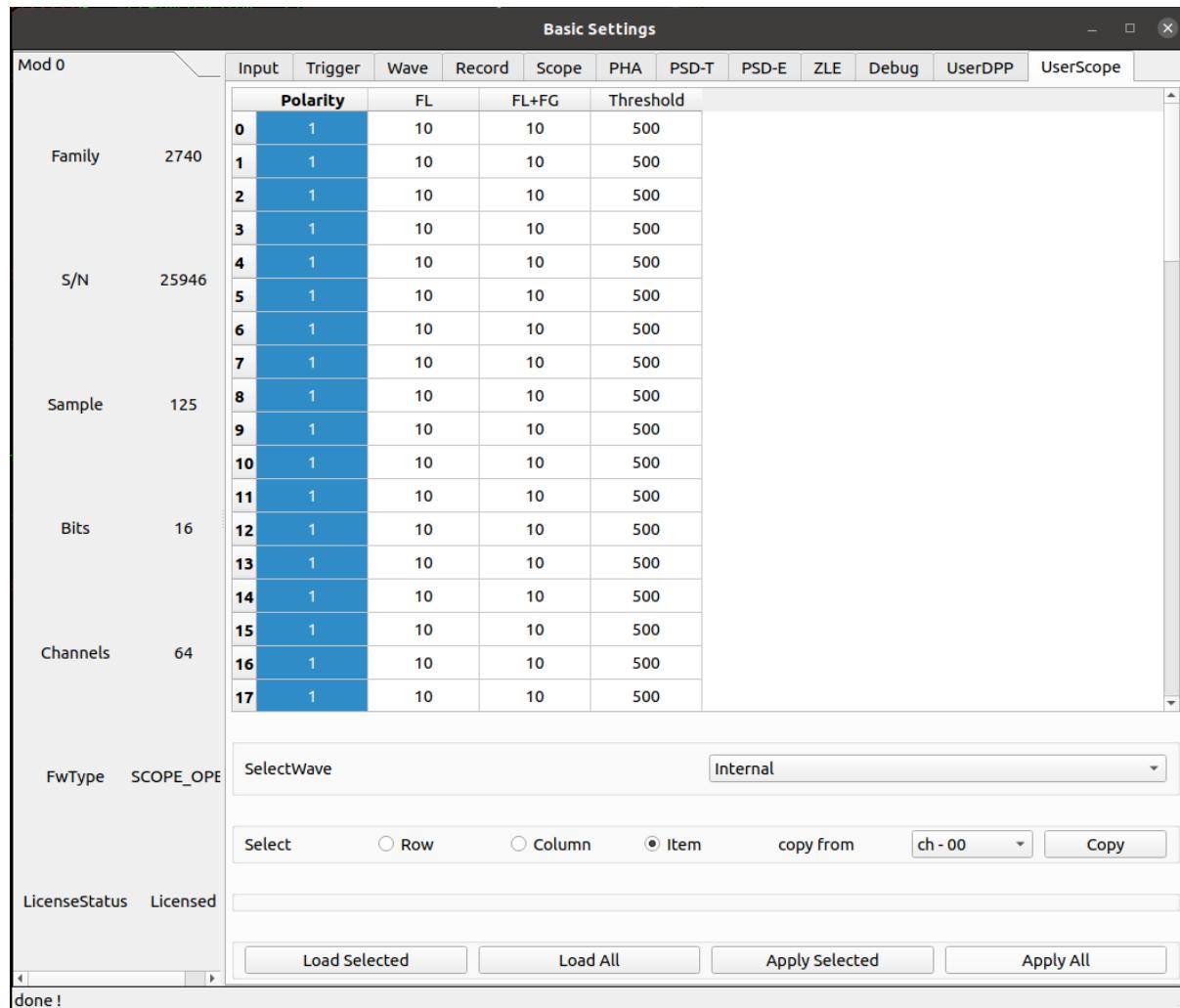
参数 ChEnable

独立设定每个通道是否开启使用。如果通道不启用，它不提供任何数据，同时它的自触发也关闭。

参数 DCOffset

当输入信号为正极性时，DCOffset 0% 为道址 0；当输入信号为负极性时，DCOffset 100% 时为道址 0。

13.1.2 UserScope



参数 Polarity

当输入信号为正极性时设置为 1，负极性时设置为 0。

参数 FL

XIA fast filter 的参数，快梯形滤波参数

FL 单位为 8 ns。可设置参数为 1-127

参数 FL+FG

快梯形滤波参数

FL+FG 单位为 8 ns, 参数需大于等于 FL。可设置参数为 1-127

参数 Threshold

快梯形滤波的触发阈值

CHAPTER 14

UDP

```
#  
sudo apt -y install ethtool
```

```
# sudo ./10Gb_settings.sh <>  
sudo ./10Gb_settings.sh enp1s0
```

CHAPTER 15

应用案例

本章节介绍一些实验应用案例、测试结果等。

$$dB = 20\lg(A/B)$$

- **0 dB**
 - x1

- **6 dB**
 - x2

- **9.5 dB**
 - x3

- **12 dB**
 - x4

- **14 dB**
 - x5

- **15.6 dB**
 - x6

- **16.9 dB**
 - x7

- **18 dB**
 - x8

- **19 dB**
 - x9

- **20 dB**
 - x10

- **21.6 dB**
 - x12

- **22.3 dB**
 - x13
- **22.9 dB**
 - x14
- **24.1 dB**
 - x15
- **25.1 dB**
 - x18
- **26 dB**
 - x20
- **29.5 dB**
 - x30
- **32 dB**
 - x40
- **34 dB**
 - x50
- **35.6 dB**
 - x60
- **36.9 dB**
 - x70
- **38 dB**
 - x80
- **39 dB**
 - x90
- **40 dB**
 - x100

CHAPTER 16

HPGe

- **VGAGain**

- Adjust the gain to achieve a measurement range of 6 MeV

- **Thre**

- based on the noise situation
 - about 50

- **PoleZero**

- based on pre amp parameter
 - about 50us

- **TriggerTriangular**

- 104 ns

- **BaselineAvg**

- MediumHigt

- **EnergyRiseTIme**

- 5104 ns

- **EnergyFlatTop**

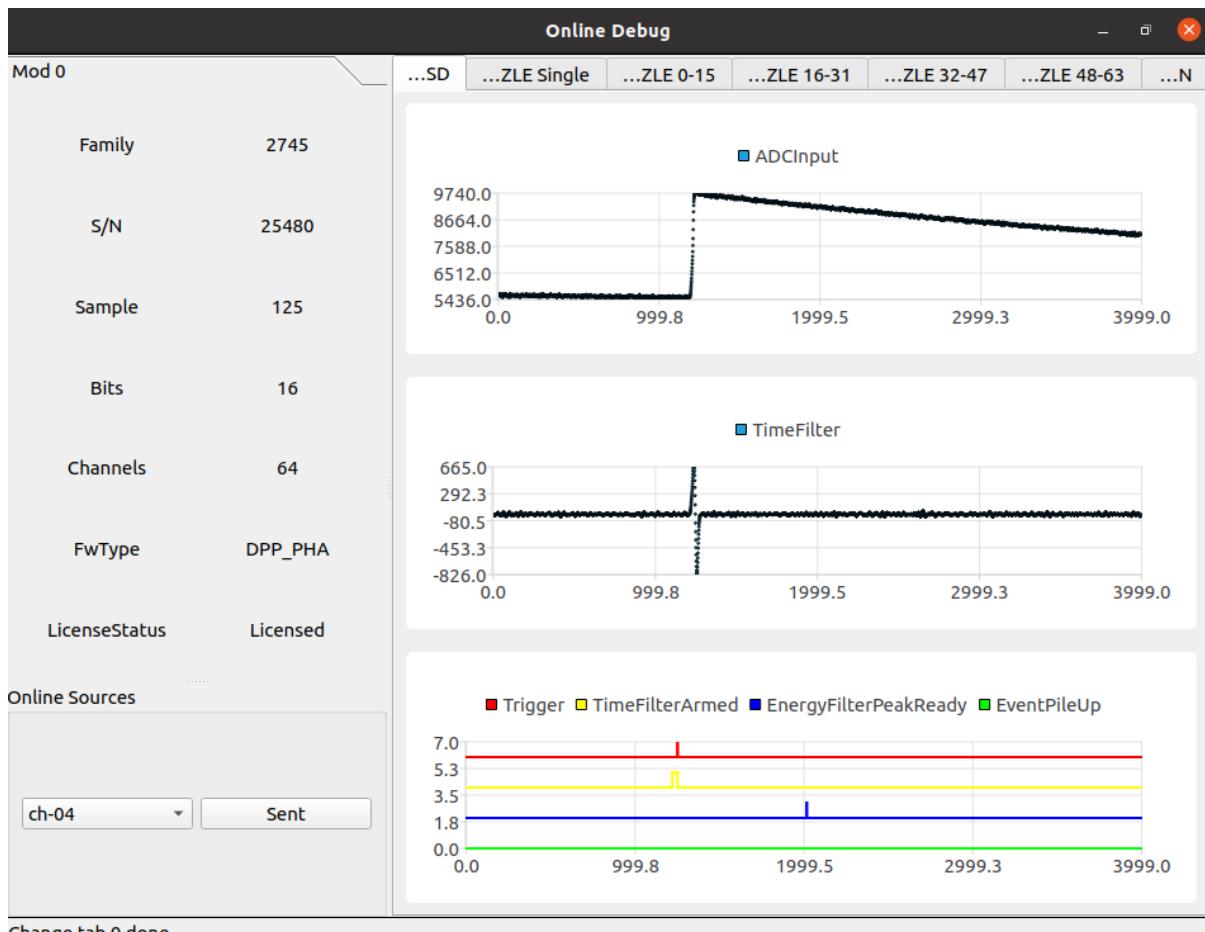
- 1200 ns

- **PeakingPosition**

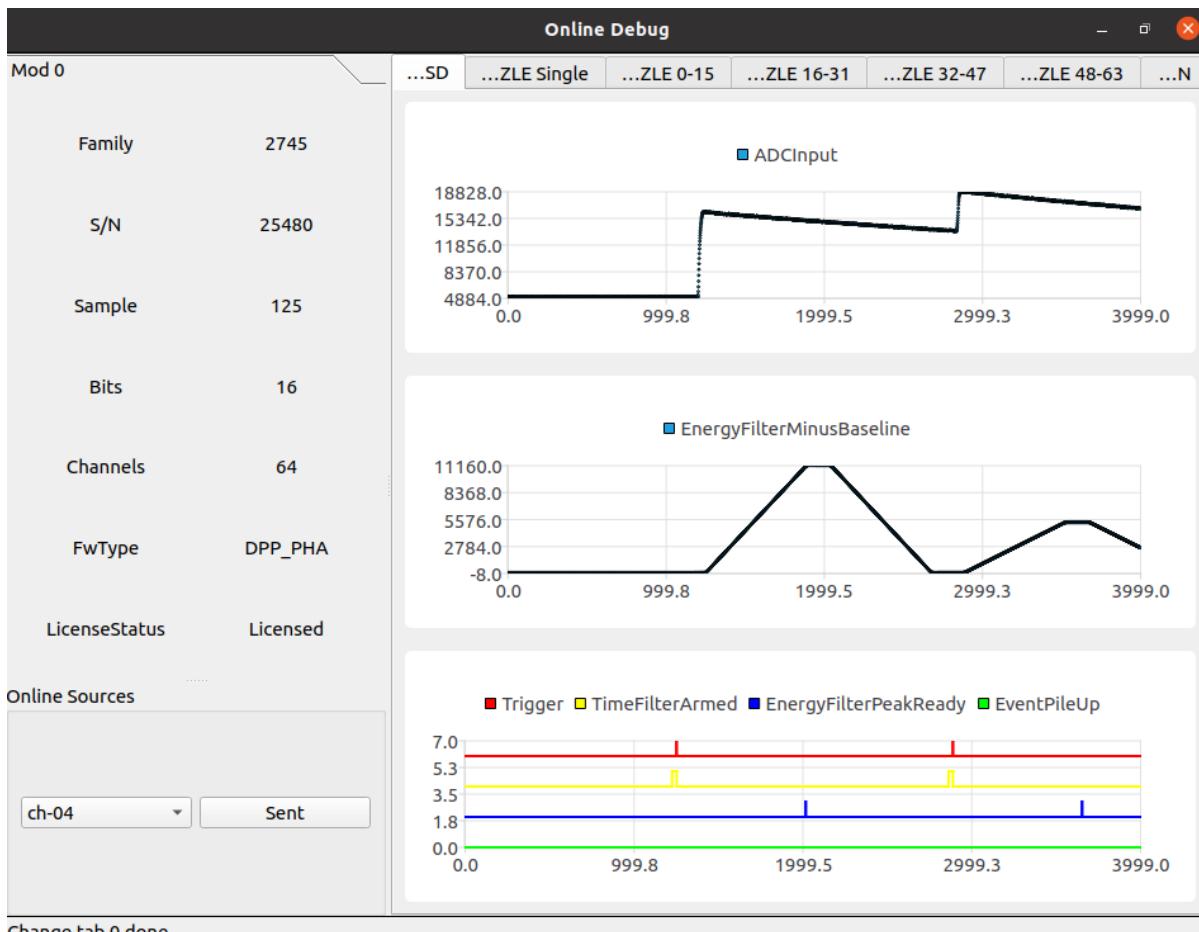
- 91%

- **PeakingAvg**

- OneShot



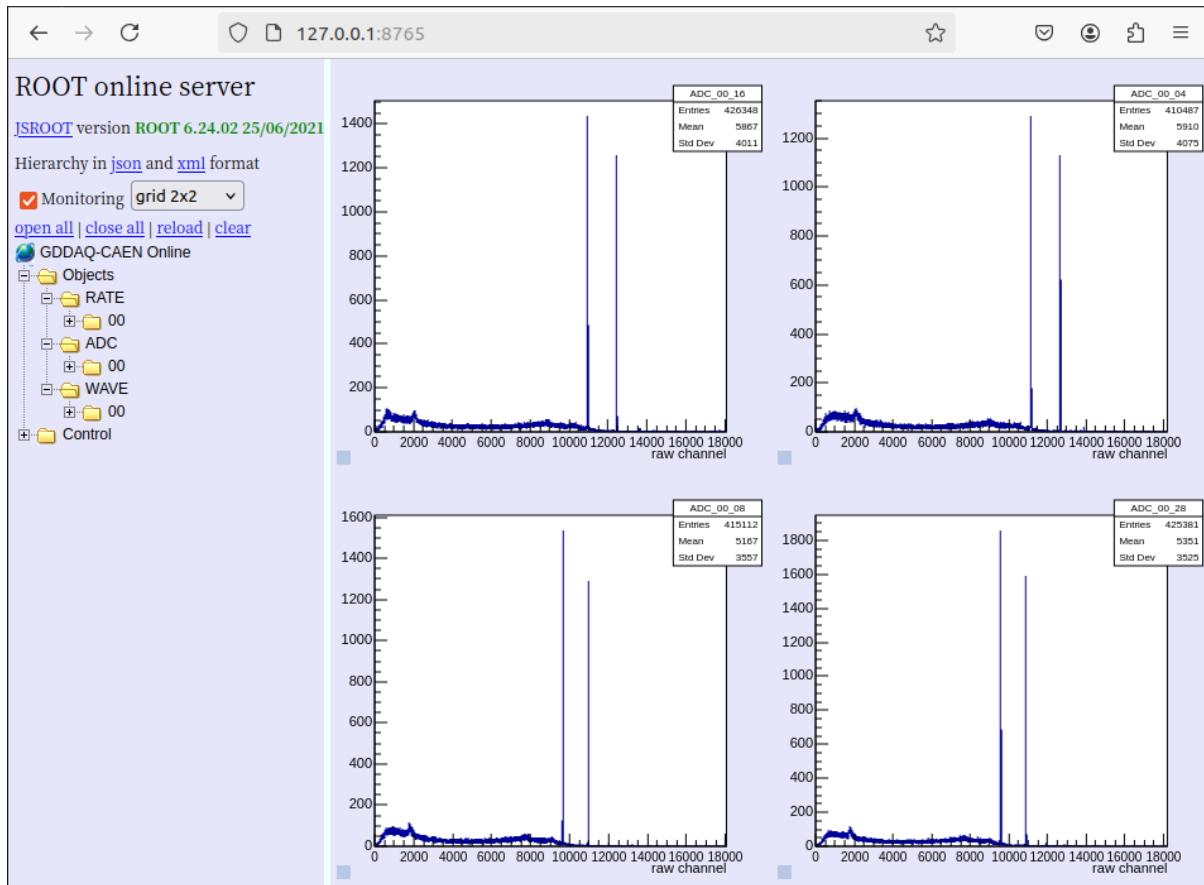
Change tab 0 done



Change tab 0 done

x2745 测量结果:

- **dynamic range**
[0-2MeV]
 - FWHM: 0.15% @ 1332 keV TriggerRate ~ 1000/s
- **dynamic range**
[0-6MeV]
 - FWHM: 0.16% @ 1332 keV TriggerRate ~ 1000/s
 - FWHM: 0.175% @ 1332 keV TriggerRate ~ 4000/s
 - FWHM: 0.190% @ 1332 keV TriggerRate ~ 10000/s



CHAPTER 17

Si

Coming soon.

CHAPTER 18

UserDPP 应用

18.1 2745 HPGe

18.2 2740 He-3

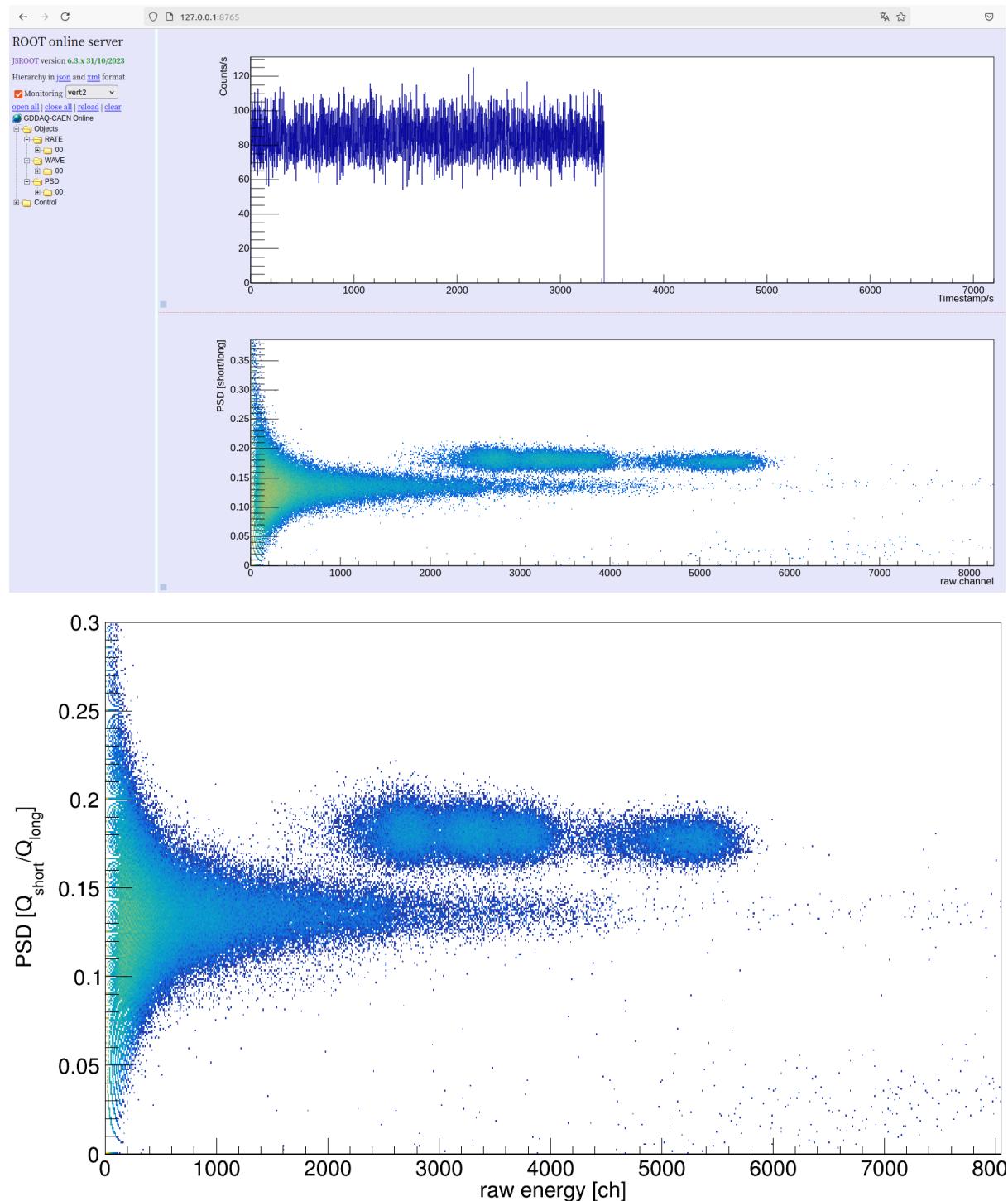
18.3 2740 Si

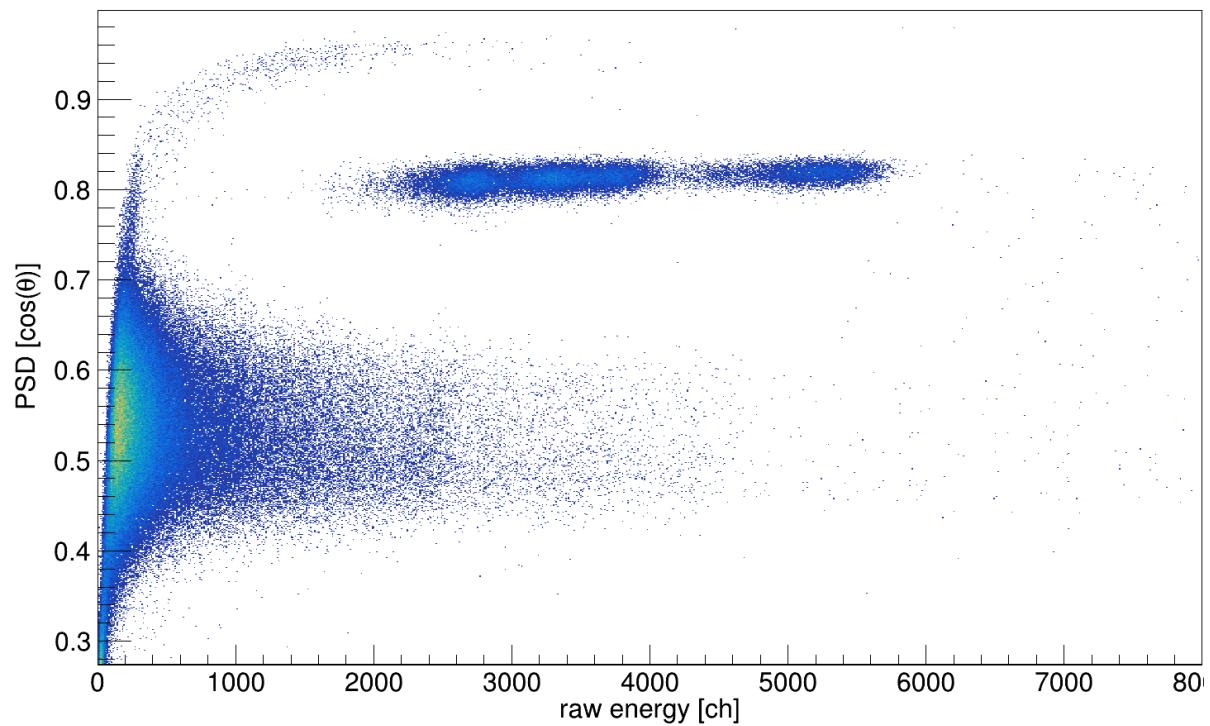
18.4 2730 BaF2

1 英寸 BaF2 探测器

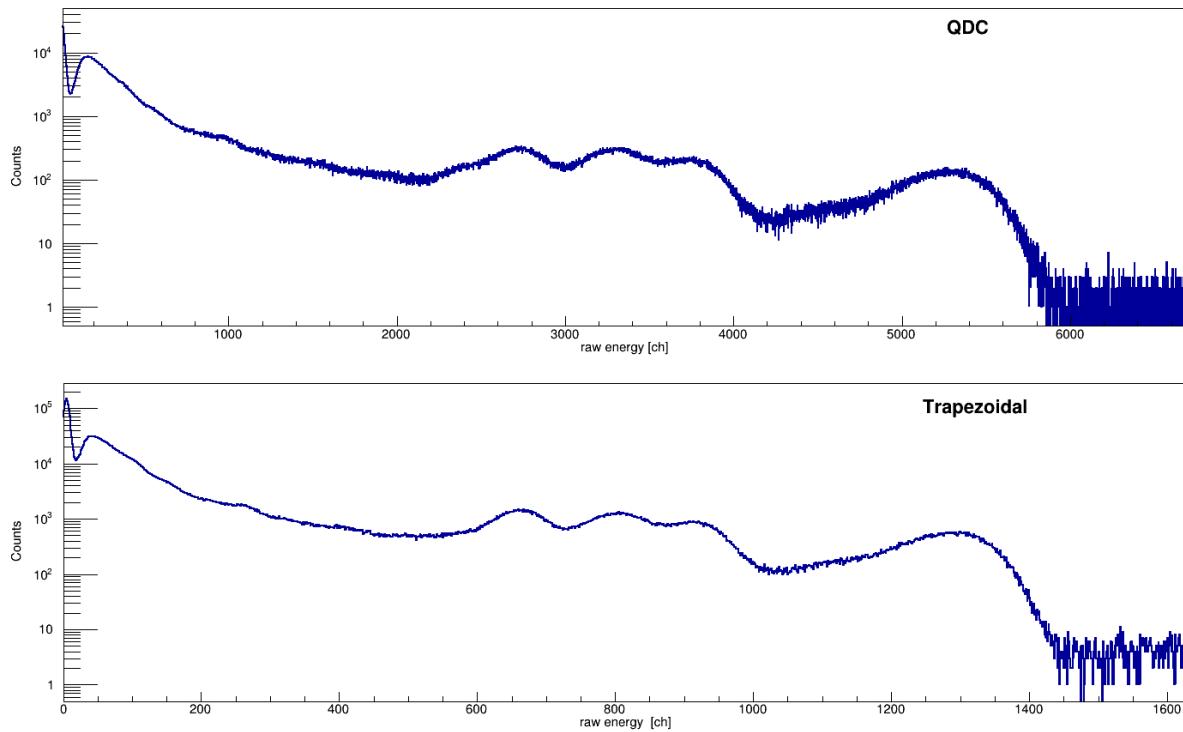
参数

- polarity: 0
- FL: 2
- FL+FG: 2
- Threshold: 100
- Qoffset: 5
- Qshort: 10
- Qlong: 150
- QGainShift: 4
- 2^n BL: 5
- BL Hold: 2000
- RT offset: 10
- RT gate: 80
- XIAOffset: 145
- SL: 140
- SG: 10

BaF₂ 探测器，本底测量。alpha 和 gamma 鉴别



BaF₂ 探测器，本底测量。alpha 和 gamma 鉴别。采用余弦相似度



BaF₂ 探测器，本底测量。QDC 和梯形算法能谱对比

超长波形采集

在聚变研究装置上，一些相关诊断探测器由于其瞬时计数率太高，脉冲堆积严重，需要连续记录 1 s 以上时长的波形。scope 固件能够帮你完成这个目标。

19.1 采集模式

当你要使用超长波形采集模式时，只能使用通道 0，此时需要将其余所有的通道均设置为不启用，系统会将所有的内存全部分配给通道 0。

这里以记录 2 s 连续波形为例，设置单个脉冲记录 10 ms，使用外部触发，间隔 10 ms 连续发送 200 个触发。

在实际操作中，需要考虑外部时钟和采集模块时钟的差异带来的问题，因此记录波形长度需要设置略高于设置的触发时间间隔，然后开启允许波形重叠来保证波形的连续采集没有丢失。

采用千兆网读取数据时，2730 测试最长能够连续采集 5.7 s。采用 10G 的 UDP 模式，可以记录更长的波形。

为了避免采集过程中数据写入磁盘数据传输时间，获取程序专门开发了配套的数据写入模式，用户可以修改开启内存的大小，当读取的数据达到指定大小时，才会进行一次写入。

19.2 计算机缓存清理

在 Linux 系统中，buff/cache 通常指的是缓冲区和缓存。用于加速对磁盘和文件的访问。清理这部分内存通常是为了释放内存空间供其他用途使用，但这并不是一个常见的操作，因为内核会自动管理这部分内存。但是我们记录超长波形时，程序占用内存需要几个 GiB，多次开启程序之后，buff/cache 不会及时释放，

如果你确实需要清理 buff/cache，可以通过执行 sync 命令来确保所有数据已经从缓冲区和缓存中写入磁盘，然后可以通过 echo 命令写入 /proc/sys/vm/drop_caches 来清理缓冲区和缓存。

```
# 同步磁盘数据
sudo sync
# 清除页缓存
sudo bash -c "echo 1 > /proc/sys/vm/drop_caches"
# 清除 dentries 和 inodes
```

(续下页)

(接上页)

```
sudo bash -c "echo 2 > /proc/sys/vm/drop_caches"
# 清除页缓存，dentries和inodes
sudo bash -c "echo 3 > /proc/sys/vm/drop_caches"
```

CHAPTER 20

数据分析

数据转换程序输出数据时间戳单位为 ns

CHAPTER 21

数据解码

DecodeAndSortAll 程序用来将同一轮数据不同采集卡采集的数据转为一个 ROOT 文件。用户的物理分析以本程序产生的 ROOT 文件为基准。本程序生成的数据已经按照时间戳从小到大排列。

用户首先需要修改 **UesrDefine.hh** 文件中的定义

```
// #define ONLYPHA  
// #define ONLYPSD  
// #define ONLYZLE  
// #define ONLYSCOPE
```

如果获取中所有的模块只使用一个类型的固件，则开启对应的定义。如果没有单一固件的定义，则输出的数据文件将默认支持所有的类型固件。

```
#define ROOTFILEPATH "./"          //要生成ROOT文件的路径  
#define ROOTFILENAME "data"        //要生成ROOT文件的名字  
// 生成 ROOT 文件的路径和文件名
```

```
#define RAWFILEPATH "/home/wuhongyi/"      //原始数据的路径  
#define RAWFILENAME "data"                //原始数据的文件名  
#define MODNUMBER 2                      //机箱中使用的模块数  
const unsigned short SamplingRate[MODNUMBER] = {500, 125}; //Specify the sampling  
rate of each modules separately; 125/500/1000 sampling rates; 0 to skip the  
module  
const unsigned short Firmware[MODNUMBER] = {2, 0}; //DPP_PHA=0 DPP_ZLE=1 DPP_PSD=2  
//DPP_DAW=3 OPEN=4 Scope=5  
// 指定每个模块的固件类型，如果类型指定错误，解码数据将存在问题
```

修改之后执行以下命令编译程序：

```
make clean  
make
```

编译成功之后将生成一个可执行文件 **decodeandsort**，程序运行方式：

```
./decodeandsort [RunNnumber]
```

其中 **[RunNnumber]** 为想要转换的文件运行编号。

CHAPTER 22

事件组装

TODO

CHAPTER 23

数据分析框架

TODO

CHAPTER 24

采购推荐

PKUCAENDAQ 长期进行版本更新, 请大家及时下载最新版本。如有任何问题, 请与吴鸿毅联系 (wuhongyi@qq.com / wuhongyi@pku.edu.cn)

CAEN 公司正在推出的数字化 2.0 系列采集卡, 涵盖 125M/250M/500M 以及 1G 采样率。

Model	# Channels	MS/s	# bit	Applications
x2740	64	125	16	64 MCAs for high channel density spectroscopy Good fit for Neutrino and Dark Matter exp. (candidate for Dark Side)
x2751 (*)	16	1000	14	Ultra-fast detectors with ps timing applications
x2725/x2730 (*)	16	250/500	14	Medium-fast detectors Sub-ns timing combined with high energy resolution
x2724 (*)	32	125	16	Spectroscopy & MCA Advanced Front-End (gain, shaping, ...) Semiconductor detector (HPGe, Clover, SDD, ...) Typically connected to charge Sensitive Preamplifier

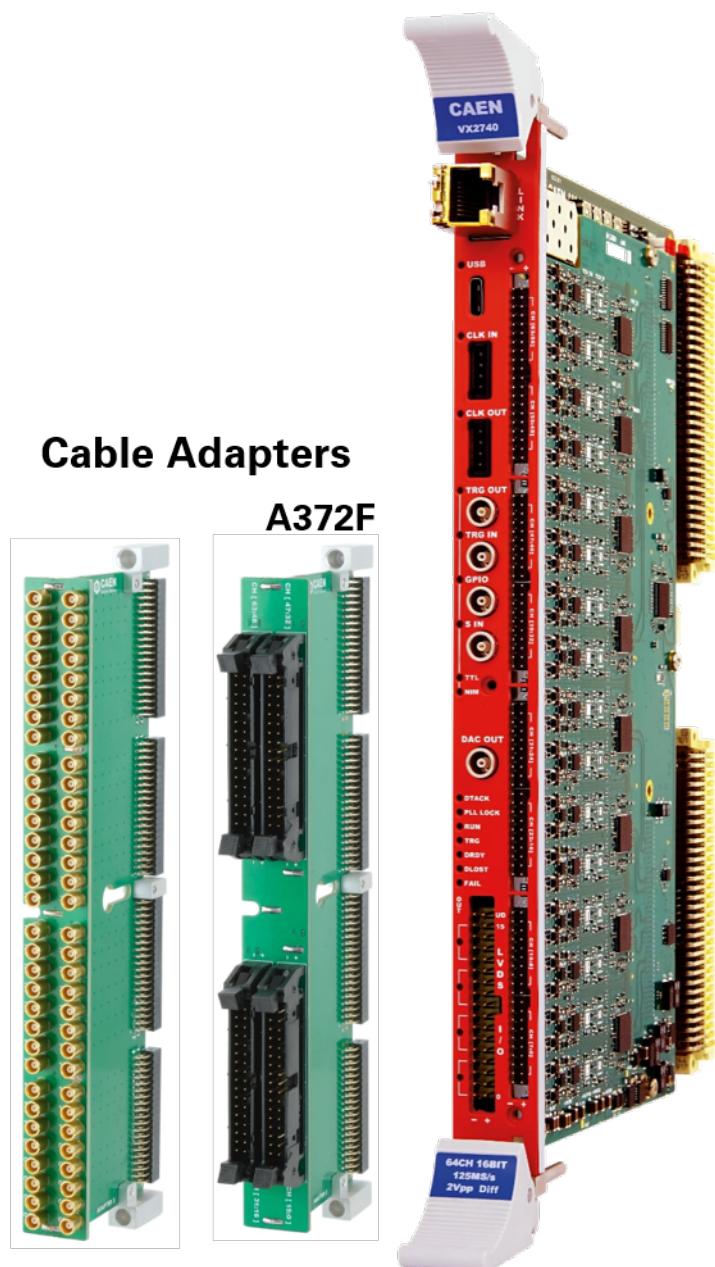
(*) Coming soon. Product specifications are subject to change without notice.

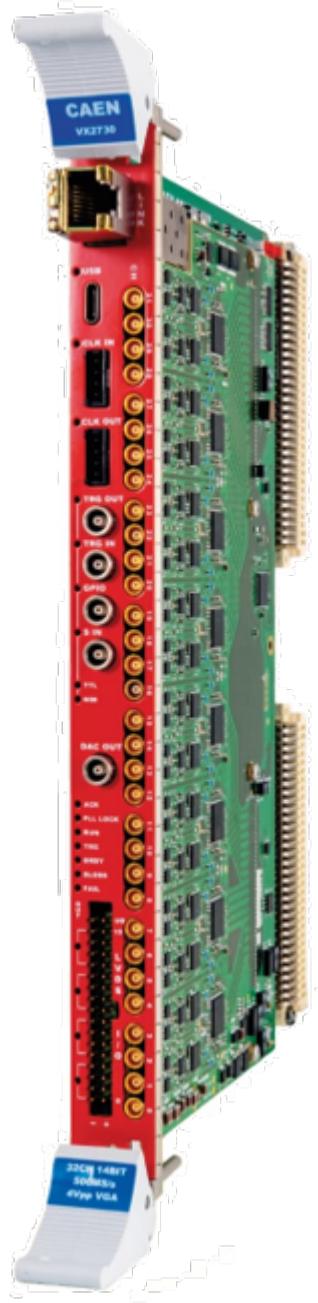
本程序支持数字化 2.0 系列中所有所有型号以及所有固件类型混合运行, 不支持上一代 x724/x725/x730 等产品。目前已经上市的产品包括 2740/2745 系列, 每个模块 64 通道, 125M 采样率, 垂直精度 16 位; 2730 系列, 每个模块 32 通道, 500 M 采样率, 垂直精度 14 位; 2751 系列, 每个模块 16 通道, 1 G 采样

率，垂直精度 14 位。

即将上市的产品有 DTL2745，8 通道，125 M 采样率，16 位；DTL2730，8 通道，500M 采样率，14 位；DTL2751，4 通道，1G 采样率，14 位。

从大规模实验的使用角度来考虑，我们推荐大家尽可能采购 VME 版本而不是桌面版本。VME 版本搭配单槽机箱（μ-crate）同样便携使用，且能够保留它搭建大阵列使用的能力。





24.1 逻辑模块

V2495 需要复杂实验触发逻辑的用户需要采购该配套模块。我们建议每个机箱配一个该模块。对于每个 V2495，我们建议添加三个 A395D 子板。

CHAPTER 25

实验调试

鉴于我们的时间限制，如果您的实验或者调试需要我们的协助，请至少提前提一个月与我们联系，确保我们有充足的时间与您沟通实验的采集需求并设计合理的实验获取方案。（简单调试/实验提前提一个月以上，中等规模或者采集逻辑有特殊需求的提前三个月以上，高通道密度或者实验中存在特殊考虑需要定制固件的需要提前三六个月以上。）**临近实验才与我们联系的，我们一律无法提供任何实验协助。**

在数字化获取系统中每种探测器的能量、时间参数优化都需要经过一定的测试和算法改进（可能需要研究适合该类型探测器的算法并升级固件），对于一种型号的探测器（例如：圣戈班标准 1 英寸 LaBr₃ 探测器）我们优化之后的参数能够适用于所有该型号探测器，但是并不适用于其它型号探测器（包括但不限于更改晶体尺寸、更改 PMT 型号等）。我们的参数优化只针对进口的标准探测器，对于自行封装、自研的探测器不在我们的参数优化范围中（测试并优化好一个型号探测器的能量、时间参数通常需要几个月的时间）。

如果您有标准的探测器需要在本系统中使用，需要我们提前提测并优化采集参数的，请至少提前提半年或一年以上将探测器邮寄到我们实验室进行测试（我们无法保证完成算法优化的时间）。对于我们没有充分测试过的探测器型号，我们将不予提供任何临时的协助和获取参数建议。

25.1 获取方案设计

物理目标的测量：实验设置和数据分析方法。

实验设置通常需要考虑以下几部分：

- 实验的弹靶组合，束流信息：能量、连续束或者周期性束流，等。
- 实验中探测器的型号、数量、摆放位置、以及实验中的计数率范围等。
- 探测器信号输出的前放、PMT 型号。
- 探测器在放射源下的输出信号幅度。实验需要测量的动态范围、阈值等。
- 探测器是否需要记录波形；是否需要使用 QDC 进行粒子鉴别、或者其它方式的粒子鉴别；采用前沿甄别或者恒比定时甄别；等。
- 探测器之间的可能的采集逻辑：符合、反符合、多重性，等。

25.2 软件异常诊断

```
export SPDLOG_LEVEL=info  
./gddaq
```

log 文件保存在 ~/.CAEN/caendig2.log

CHAPTER 26

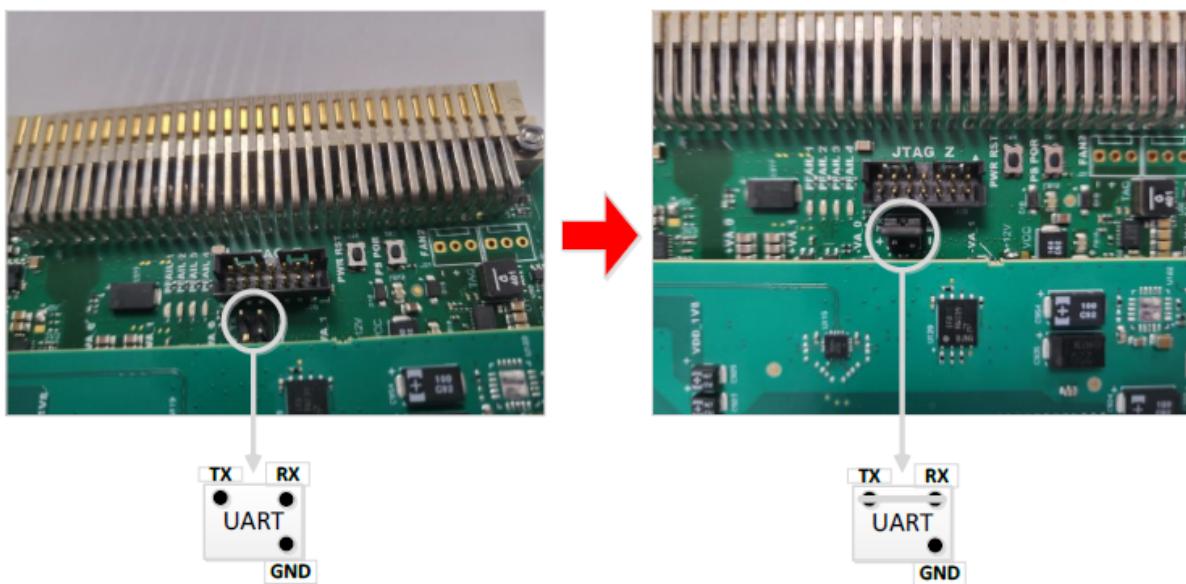
恢复出厂设置

当模块无法通过 USB 和网络方式访问时，可以通过以下方式重置到出厂设置。它会清除所有用户的固件、并且清除 licences PUC。重置之后用户需要重新上传固件以及 PUC 码。

首先将机箱关机，取下采集模块，

Set the Recovery mode:

- In the case of VME models, ensure the VME crate is powered off, extract the digitizer and short-circuit the RX and TX pins on the serial port that is near the JTAG connector on the motherboard. Then, insert the digitizer into the VME crate and power it on

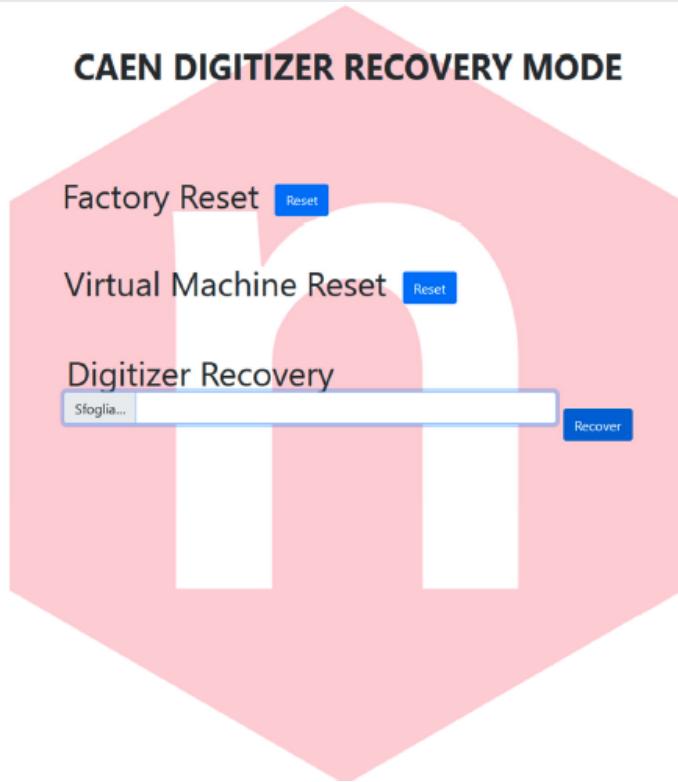


通过跳针短接 RX 和 TX，如上图所示。

将模块插入机箱，开启电源，直到前面板上只有 TTL 和 NIM 两个 LED 常亮。

通过 USB 或者网络访问重置页面。

- USB 方式：<http://caendgtz-usb-recovery> （经测试这个方式无法访问!!!）
- 网络方式：<http://192.168.0.254> （采集模块和电脑通过网线直连，其中 192.168.0.254 是模块的默认 IP）



如上图所示，点击网页上的重置按钮。等待前面板上的只有 TTL 和 NIM 两个 LED 常亮。

关闭机箱，去除短接跳针。重启机箱电源。等待初始化成功，前面板只有 NIM 和 PLL-LOCK 两个 LED 常亮。