CAEN
Tools for Discovery

Electronic Instrumentation

User Manual UM3148

DT5730/DT5725

8-Channel 14-bit 500/250 MS/s **Digitizer**

Rev. 7 – September 20th, 2021

Purpose of this Manual

This document contains the full hardware description of the DT5730 and DT5725 digitizers and the principle of operating as Waveform Digitizer (based on the hereafter called *"waveform recording firmware"*).
For any reference to registers in this document, please refer to [RD2].
For any reference to DPP firmware in this document, please refer to [RD9] [RD10][RD11].

Change Document Record

Date	Revision	Changes
Feb 14th, 2014	00	Initial release
Dec 15th, 2014	01	Added new Chap. **6** on cooling management and Chap. **7** on temperature protection. Updated Sec. **Waveform Recording** Trigger Management**.** General revision.
Jun 10th, 2016	02	Fully reviewed for the new DT5725 digitizer (250 MS/s). Updated Chap. **1**, **3**, **5**, **8**, **13**, Sec. **Clock Distribution**, **PLL Mode**, **Trigger Clock**, **Channel Calibration**, **Custom-sized Events**, **Waveform Recording Event Structure**, **Trigger Distribution**, DPP-PSD Control Software. Added Sec. Changing the ADC Frequency, **CAENScope**, MC^2 Analyzer**.**
Sep 24th, 2019	03	Global review. Added support to the new 730S/725S modules. Added Sections: **DC Offset Individual Setting**, **TRG-IN as Gate**, **Multi-board Synchronization**, **Test Pattern Generator**, **CoMPASS, DPP-ZLEplus and DPP-DAW Control Software, Troubleshooting**.
May 6th, 2020	04	Updated **Tab. 1.1**, Chap. **7**, Sec. **Acquisition Run/Stop**, **CAENScope**. Added Sec. **Channel Self-Trigger Rate Meter (725S and 730S only)**.
Sep 2nd, 2020	05	Updated Sec. **DPP-ZLEplus and DPP-DAW Control Software**, and power consumption specifications in Chap. **3**, **5**.
May 4th, 2021	06	Updated digitizer pictures and Sec. **Troubleshooting**. Reviewed Sec. **External Trigger**. Added more information on the time stamp reset via the GPI connector in Sec. **Timer Reset**.
Sep 20th, 2021	07	Updated **Tab. 1.1**, **Tab. 3.1**, Chap **5**, Sec. **Acquisition Triggering: Samples and Events**, Sec. **Optical Link and USB Access**, Chap. **10**, Sec. **CAENScope**, Sec. **Waveform Recording Event Structure**, Sec. **Trigger Clock**. Removed section about MC^2 Analyzer dismissed software from Chap. **11**.

Symbols, abbreviated terms, and notation

GUI	Graphical User Interface
DPP	Digital Pulse Processing
ETTT	Extended Trigger Time Tag
OS	Operating System
PSD	Pulse Shape Discrimination
TTT	Trigger Time Tag

Reference Documents

[RD1] GD2512 – CAENUpgrader QuickStart Guide
[RD2] UM5118 – 725-730 Raw Waveform Registers Description
[RD3] GD2783 – First Installation Guide to Desktop Digitizers & MCA
[RD4] UM1934 - CAENComm User & Reference Manual
[RD5] UM1935 - CAENDigitizer User & Reference Manual
[RD6] UM2091 - CAEN WaveDump User Manual
[RD7] GD2483 - WaveDump QuickStart Guide
[RD8] UM2092 - CAENSCOPE User Manual
[RD9] UM5960 - CoMPASS User Manual
[RD10] UM5954 – DPP-DAW User Manual
[RD11] UM6064 – DPP-ZLEPlus User Manual
[RD12] GD2728 – How to make Coincidences with CAEN Digitizers
[RD13] UM4413 - A2818 Technical Information Manual
[RD14] UM3121 - A3818 Technical Information Manual
[RD15] AN2472 - CONET1 to CONET2 migration
[RD16] DS7799 – A4818 Data Sheet

https://www.caen.it/support-services/documentation-area/

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MADE IN ITALY: We remark that all our boards have been designed and assembled in Italy. In a challenging environment where a competitive edge is often obtained at the cost of lower wages and declining working conditions, we proudly acknowledge that all those who participated in the production and distribution process of our devices were reasonably paid and worked in a safe environment (while this is true for the boards marked ”MADE IN ITALY”, we cannot guarantee for third-party manufactures).

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1 Introduction

The DT5730 is a Desktop module housing an 8-channel 14-bit 500 MS/s FLASH ADC Waveform Digitizer with software selectable 2 V_{pp} or 0.5 V_{pp} input dynamic range on single-ended MCX coaxial connectors. The DC offset is adjustable in the ±1 V (@ 2 V_{pp}) or ±0.25 (@ 0.5 V_{pp}) range via a 16-bit DAC on each channel (see Sec. **Analog Input Stage**).

Operationally, the mod. DT5725 differs from the DT5730 for working at 250 MS/s sampling frequency.

The ADC resolution and the sampling frequency make these digitizers well suited for mid-fast signal detection systems (e.g. liquid or inorganic scintillators coupled to PMTs or Silicon Photomultipliers).

Each channel has an SRAM Multi-Event Buffer divisible into 1 ÷ 1024 buffers of programmable size. Two sizes of the channel digital memory are available by ordering option (see **Tab. 1.1**).

DT5730 and DT5725 digitizers are provided with FPGAs that can run special DPP firmware for Physics Applications (see Chap. **13**).

A common acquisition trigger signal can be fed externally via the front panel TRG-IN input connector or via software. Alternatively, each channel can generate a self-trigger when the input signal goes under/over a programmable threshold. For each couple of adjacent channels, the relevant self-triggers are then processed to provide a single trigger request. In the DPP firmware, the trigger requests can be used at the channel level for the event acquisition (independent triggering), while in the waveform recording firmware they can be processed by the board to generate a common trigger causing all the channels to acquire an event simultaneously. The trigger from one board can be propagated to the other boards through the front panel GPO output connector.

During the acquisition, the data stream is continuously written in a circular memory buffer. When the trigger occurs, the digitizer writes further samples for the post-trigger and freezes the buffer that can be read by one of the provided readout links. The acquisition can continue without any dead time in a new buffer.

DT5730 and DT5725 feature front panel CLK-IN connector as well as an internal PLL for clock synthesis from internal/external references. Multi-board synchronization is supported, so all DT5730 or all DT5725 can be synchronized to a common clock source and ensuring Trigger time stamps alignment. The fan-in of an external clock signal to each CLK-IN is required. Once synchronized, all data will be aligned and coherent across the multi-board system.

Each module houses USB 2.0 and Optical Link interfaces. USB 2.0 allows data transfers up to 30 MB/s. The Optical Link (CAEN proprietary CONET protocol) supports a transfer rate of 80 MB/s and offers Daisy chain capability. Therefore, it is possible to connect up to 8 ADC modules to a single A2818 Optical Link Controller or A4818 adapter, and up to 32 using an A3818 (4-link version). Optical Link and USB accesses are internally arbitrated. The A4818 adapter from USB-3.0 to Optical Link is also supported.

In addition to the waveform recording firmware, CAEN provides for this digitizer four types of Digital Pulse Processing firmware (DPP):

- Pulse Shape Discrimination (DPP-PSD) combines the functions of a digital QDC (charge integration) and discriminator of different shapes for particle identification.
- Pulse Height Analysis (DPP-PHA) is the digital solution equivalent to Shaping Amplifier and Peak Sensing ADC for nuclear physics or other applications requiring radiation detectors.
- Zero-Length Encoding (DPP-ZLEplus) for zero suppression and data reduction.
- Dynamic Acquisition Windows (DPP-DAW) automatically adjusts the acquisition window length to match the actual input pulse duration.

All these DPP firmware make the digitizer an enhanced system for Physics Applications.

To interface the digitizers, CAEN provides the drivers for the supported communication links, a set of C libraries, LabVIEW VIs and example codes, configuration tools for firmware management (e.g. upgrade, board information, etc.) and direct register access, readout software for the waveform recording firmware (WaveDump, CAENScope) and the DPP firmware (CoMPASS, DPP-ZLE and DPP-DAW Control Software).

Board Models	Description
DT5730	8 ch. 14bit 500 MS/s Digitizer:640kS/ch,CE30,SE
DT5730B	8 ch. 14bit 500 MS/s Digitizer:5.12MS/ch,CE30,SE
DT5730S	8 Ch. 14 bit 500 MS/s Digitizer:640kS/ch,Arria V GX,SE
DT5730SB	8 Ch. 14 bit 500 MS/s Digitizer:5.12MS/ch,Arria V GX,SE
DT5725	8 ch. 14bit 250 MS/s Digitizer:640kS/ch,CE30,SE
DT5725B	8 ch. 14bit 250 MS/s Digitizer:5.12MS/ch,CE30,SE
DT5725S	8 ch. 14bit 250 MS/s Digitizer:640kS/ch,Arria V GX,SE
DT5725SB	8 ch. 14bit 250 MS/s Digitizer:5.12MS /ch,Arria V GX,SE
DPP Firmware	**Description**
DPP-PSD 8ch 730	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x730)
DPP-PSD 8ch 725	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x725)
DPP-PHA 8ch 730	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x730)
DPP-PHA 8ch 725	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x725)
DPP-ZLE 8ch 730	DPP-ZLE – Digital Pulse Processing with Zero Length Encoding (8ch x730)
DPP-ZLE 8ch 725	DPP-ZLE – Digital Pulse Processing with Zero Length Encoding (8ch x725)
DPP-DAW 8ch 730	DPP-DAW – Digital Pulse Processing with Dynamic Acquisition Window (8ch x730)
DPP-DAW 8ch 725	DPP-DAW – Digital Pulse Processing with Dynamic Acquisition Window (8ch x725)
Related Products	**Description**
A2818	A2818 – PCI Optical Link (Rhos compliant)
A3818A	A3818A – PCIe 1 Optical Link
A3818B	A3818B – PCIe 2 Optical Link
A3818C	A3818C – PCIe 4 Optical Link
A4818	A4818 – USB-3.0 to Optical Link
Accessories	**Description**
DT4700	Clock Generator and Fan Out Unit
A318	Adapter for Clock signal FISCHER S101A004 male to 3-pin AMPMODU IV female - 10 cm
A654	Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT4	4 Cable assembly LEMO 00 male to MCX male - 1 m
A654 KIT8	8 Cable assembly LEMO 00 male to MCX male - 1 m
A659	Cable assembly BNC male to MCX male - 1 m
A659 KIT4	4 MCX to BNC Cable Adapter
A659 KIT8	8 MCX to BNC Cable Adapter
AI2730	Optical Fibre 30 m simplex
AI2720	Optical Fibre 20 m simplex
AI2705	Optical Fibre 5 m simplex
AI2703	Optical Fibre 30 cm simplex
AY2730	Optical Fibre 30 m duplex
AY2720	Optical Fibre 20 m duplex
AY2705	Optical Fibre 5 m duplex

Tab. 1.1: Table of models and related items

2 Block Diagram

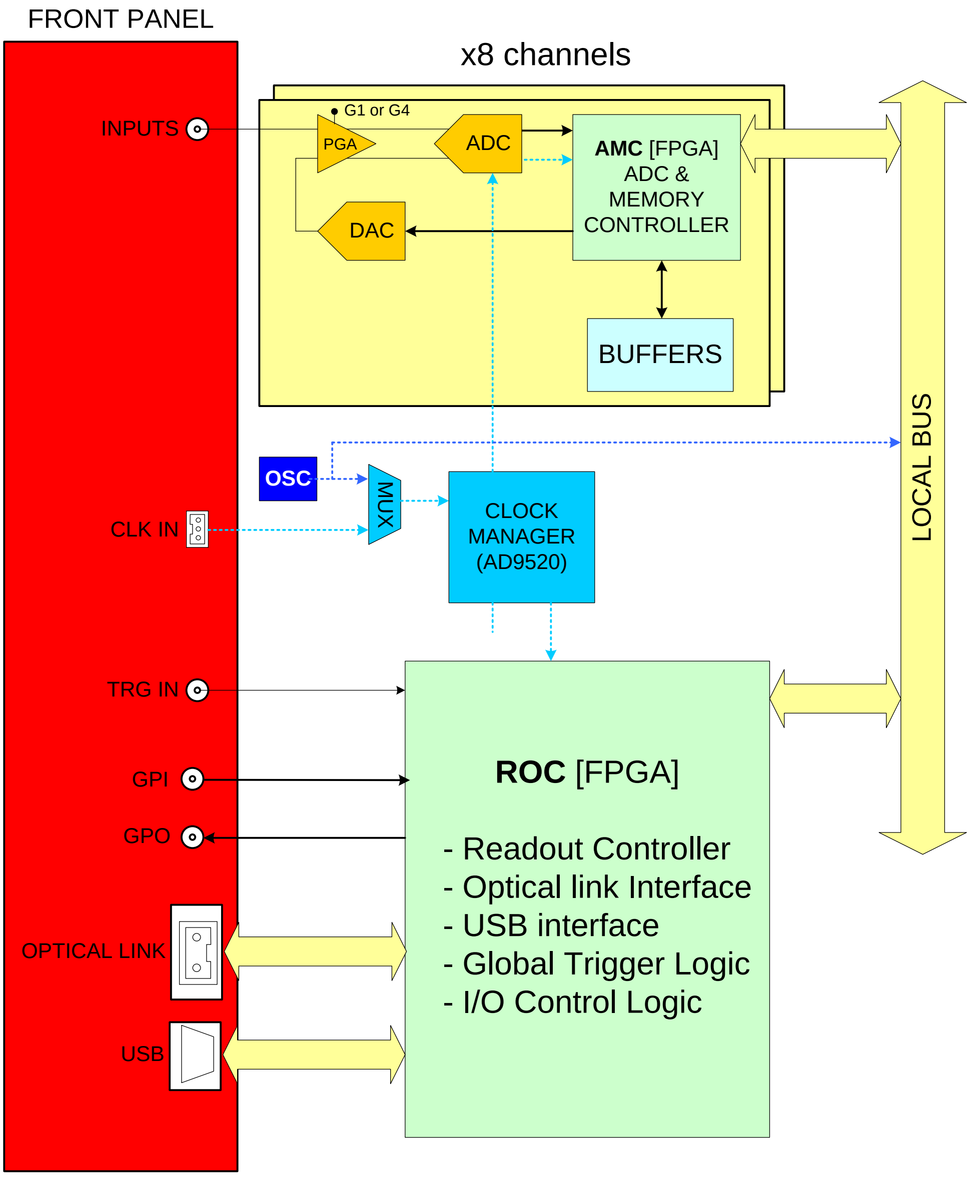


Fig. 2.1: Block Diagram

3 Technical Specifications

GENERAL	**Form Factor** 154x50x164 mm^3 (WxHxD) Desktop		**Weight** 670 g
ANALOG INPUT	**Channels** 8 channels Single-ended	**Connector** MCX	**Bandwidth** 250 MHz (DT5730) 125 MHz (DT5725)
	Impedance (Z_{in}) 50 Ω	**Full Scale Range (FSR)** 0.5 V_{pp} / 2 V_{pp} (default) SW selectable	**Offset** Programmable DAC for DC offset adj. in the full-scale range
DIGITAL CONVERSION	**Resolution** 14 bits	**Sampling Rate (Simultaneous on each channel)** 500 MS/s (DT5730) 250 MS/s (DT5725)	
ADC CLOCK GENERATION	Clock source: internal/external On-board programmable PLL provides generation of the main board clocks from an internal (50 MHz local Oscillator) or external (front panel CLK-IN connector) reference		
DIGITAL I/O	**CLK-IN (AMP Modu II)** AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single-ended NIM/TTL available by A318 adapter) Jitter<100ppm requested	**GPO (LEMO)** General-purpose digital output NIM/TTL, Rt = 50 Ω	
	TRG-IN (LEMO) External trigger digital input NIM/TTL, Z_{in} = 50 Ω	**GPI (LEMO)** General-purpose digital input NIM/TTL, Zin = 50 Ω	
MEMORY	640 kS/ch or 5.12 MS/s Multi-event Buffer divisible into 1 ÷ 1024 buffers Independent read and write access; programmable event size and pre/post-trigger		
TRIGGER	**Trigger Source** <u>Self-trigger</u>: channel over/under threshold for either Common or Individual (DPP only) trigger generation <u>External-trigger</u>: Common by TRG-IN connector <u>Software-trigger</u>: Common by software command	**Trigger Time Stamp DT5730** <u>Waveform Recording</u>: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension by firmware <u>DPP-PSD</u>: 47-bit counter, 2 ns resolution, 78 h range; 10-bit and 2 ps fine time stamp with digital CFD <u>DPP-PHA</u>: 47-bit counter, 2 ns resolution, 78 h range <u>DPP-DAW</u>: 48-bit counter, 2 ns resolution, 156 h range <u>DPP-ZLEplus</u>: 48-bit counter, 16 ns resolution, 625 h range	
	Trigger Propagation GPO programmable digital output	**Trigger Time Stamp DT5725** <u>Waveform Recording</u>: 31-bit counter, 16 ns resolution, 34 s range; 48-bit extension by firmware <u>DPP-PSD</u>: 47-bit counter, 4 ns resolution, 156 h range; 10-bit and 4 ps fine time stamp with digital CFD <u>DPP-PHA</u>: 47-bit counter, 4 ns resolution, 156 h range <u>DPP-DAW</u>: 48-bit counter, 4 ns resolution, 312 h range <u>DPP-ZLEplus</u>: 48-bit counter, 16 ns resolution, 1250 h range	
SYNCHRONIZATION	**Clock Propagation** <u>One-to-many</u>: fan-out by DT4700 to CLK-IN	**Acquisition Synchronization** Sync Start/Stop by digital I/O (TRG-IN/GPI, GPO) **Trigger Time Stamp Alignment** By GPI input connector	
ADC & MEMORY CONTROLLER	**DT5725/DT5725B/DT5730/DT5730B** Altera Cyclone EP4CE30 (one FPGA serves 4 channels)	**DT5725S/DT5725SB/DT5730S/DT5730SB** Intel/Altera Arria V GX (one FPGA serves 4 channels)	
COMMUNICATION INTERFACE	**USB** USB 2.0 compliant Transfer rate: up to 30 MB/s	**Optical Link** CONET proprietary protocol (compliant to A2818/A3818/A4818) Transfer rate: up to 80 MB/s Daisy chain capability	
FIRMWARE	**Waveform Recording Firmware (free)** Firmware for waveform recording	**DPP Firmware (trial)** Firmware for Digital Pulse Processing: DPP-PSD, DPP-PHA, DPP-ZLEplus, DPP-DAW	**Upgrades** Via Optical Link or USB

SOFTWARE	**Libraries** General-purpose C libraries LabVIEW VIs		**Configuration Tools** Firmware upgrade Direct Register R/W Example codes	**Readout Software** Control Software for waveform recording firmware and DPP firmware	
DT5730x POWER REQUIREMENTS (TYP. @+12 VDC)	**FW**	**DT5730**	**DT5730B**	**DT5730S**	**DT5730SB**
	Wav. Rev.	2.8 A	3.0 A	2.9 A	3.5 A
	DPP-PHA	N.A.		2.9 A	3.4 A
	DPP-PSD			2.9 A	3.2 A
	DPP-DAW			2.9 A	3.4 A
	DPP-ZLE			2.3 A	3.2 A
DT5725x POWER REQUIREMENTS (TYP. @+12 VDC)	**FW**	**DT5725**	**DT5725B**	**DT5725S**	**DT5725SB**
	Wav. Rev.	2.0 A	N.A.	2.1 A	2.8 A
	DPP-PHA	N.A.			
	DPP-PSD				
	DPP-DAW				
	DPP-ZLE				

Tab. 3.1: Specifications table

4 Packaging and Compliancy

The unit is a Desktop module housed in an alloy box (weight: 670 g) with the following dimensions:

154 W x 50 H x 164 L mm³ (connectors not included)

154 W x 50 H x 171 L mm³ (including connectors).

Fig. 4.1: Front view

CAUTION: to manage the product, consult the operating instructions provided.

A POTENTIAL RISK EXISTS IF THE OPERATING INSTRUCTIONS ARE NOT FOLLOWED!

CAEN provides the specific document "Precautions for Handling, Storage and Installation" available in the documentation tab of the product web page that the user is mandatory to read before operating with CAEN equipment.

5 Power Requirements

The modules are powered by the external AC-DC 12V-60W stabilized power supply unit included in the delivered kit.

The tables below resume the typical power consumptions at the nominal power supply voltage.

<table>
<tr><th colspan="5">Typical Power Consumptions @+12 VDC</th></tr>
<tr><th>FW</th><th>D5730</th><th>DT5730B</th><th>DT5730S</th><th>DT5730SB</th></tr>
<tr><td>Waveform Recording</td><td>2.8 A</td><td>3.0 A</td><td>2.9 A</td><td>3.5 A</td></tr>
<tr><td>DPP-PHA</td><td colspan="2" rowspan="4">N.A.*</td><td>2.9 A</td><td>3.4 A</td></tr>
<tr><td>DPP-PSD</td><td>2.9 A</td><td>3.2 A</td></tr>
<tr><td>DPP-DAW</td><td>2.9 A</td><td>3.4 A</td></tr>
<tr><td>DPP-ZLE</td><td>2.3 A</td><td>3.2 A</td></tr>
</table>

Tab. 5.1: Power requirements table for DT5730x models

*Not measured values can be assumed to respect the same proportions as the relevant "S" model ones

<table>
<tr><th colspan="5">Typical Power Consumptions @+12 VDC</th></tr>
<tr><th>FW</th><th>D5725</th><th>DT5725B</th><th>DT5725S</th><th>DT5725SB</th></tr>
<tr><td>Waveform Recording</td><td>2.0 A</td><td>N.A.</td><td>2.1 A</td><td>2.8 A</td></tr>
<tr><td>DPP-PHA</td><td colspan="4" rowspan="4">N.A.</td></tr>
<tr><td>DPP-PSD</td></tr>
<tr><td>DPP-DAW</td></tr>
<tr><td>DPP-ZLE</td></tr>
</table>

Tab. 5.2: Power requirements table for DT5725x models

Note.: The declared values are measured in standard operating conditions. In general, they could be subject to slight changes due to the firmware type, the firmware version, and the operating mode.

Note.: Using a different power supply source, like a battery or linear type, it is recommended the source to provide +12 V and, at least the typical current + 20%; the power jack is a 2.1 mm type, a suitable cable is the RS 656-3816 type (or similar)

P R
B X

POWERBOX Switchbox
FRA060/065/072 Series
60-72W
Single Output
AC/DC Switch Mode Adapter, Desktop Style

Features
Universal input single output
OVP, OPP, auto recovery
No load power consumption (@no load) <0.075W
Comply with EISA 2007 / DoE 6 & EU ErP and CoC 5

Input voltage	90VAC~264VAC.
Input current	1.8A max.
Efficiency	87% for CEC requirement.
Hold up time	10mS at nominal line.
Output voltage	12 ~ 48VDC.
Load regulation	±5% max.
Ripple & noise	2% p-p max.
Withstand voltage	I/P-O/P: 3000 VAC (Class II).
	I/P-O/P(V+): 4242 VDC.
	I/P-FG: 2121 VDC (Class I).
Operating temperature	-10°C ~ +60°C derated linearly from 100% load
	@ 40°C to 50% load @ 60°C.
Storage temperature	-20°C to +85°C.
Protections	OCP , OVP , over power & short circuit.
Safety standard	IEC/UL/EN60950-1,CE, CB.
EMC standard	(EN55022, CISPR22, FCC Part 15) Class B,
	EN61000-3-2, 3, EN61000-4-2, 3, 4, 5, 6, 8,
	11, EN55024.
Std output connector	DC barrel jack.
Std output cable / length	Ul1185 or UL1571 / 1.0M.

Model Number	Output Voltage	Output Current	Output Max Watts	Eff Level
FRA060-S12-x	12~15 VDC	5.0~4.0 A	60W	VI
FRA060-S15-x	15~18 VDC	4.0~3.33 A	60W	VI
FRA060-S24-x	18~24 VDC	3.33~2.5 A	60W	VI
FRA060-S36-x	30~36 VDC	2.0~1.67 A	60W	VI
FRA060-S48-x	40~48 VDC	1.5~1.25 A	60W	VI
FRA065-S24-x	18~24 VDC	3.6~2.7 A	65W	VI
FRA072-S24-x	24 VDC	3 A	72W	VI
FRA072-S36-x	30~36 VDC	2.4~2.0 A	72W	VI
FRA072-S48-x	40-48 VDC	1.8~1.5 A	72W	VI

Ordering information:
x= AC Inlet Type Code
x= 4, IEC320 C14 x = 6, IEC320 C6 x = 8, IEC320 C8

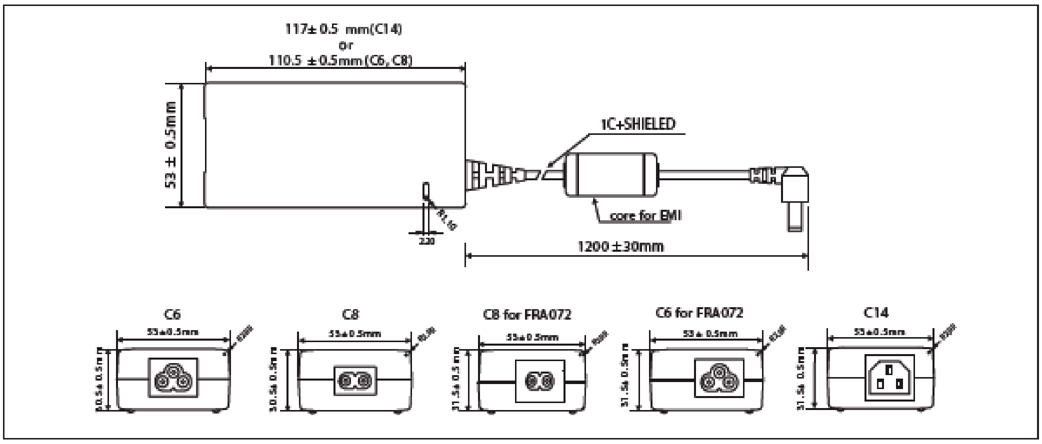


Fig. 5.1: AC/DC power supply provided with the module

6 Cooling Management

Starting from **revision 4** of the motherboard (readable at 0xF04C address of the configuration ROM), DT5730 and DT5725 feature an automatic fan speed control to guarantee an appropriate cooling in consequence of internal temperature variations.

The automatic control is managed by the ROC FPGA firmware from **revision 4.4** on.

CAEN HEARTLY RECOMMENDS MONITORING THE TEMPERATURE OF THE ADC CHIPS DURING THE BOARD OPERATION BY CAEN SOFTWARE (E.G. CoMPASS, WAVEDUMP) OR READING AT REGISTER ADDRESS 0x1nA8.

The user can manually set the fan speed through the bit[3] at register address 0x8168 **[RD2]**:

Hardware revision ≥ 4 and ROC FPGA firmware revision ≥ 4.4

- Bit[3] = 0 (default) sets the automatic fan speed control;
- Bit[3] = 1 sets HIGH the fan speed.

Hardware revision < 4 and ROC FPGA firmware revision < 4.4

- Bit[3] = 0 (default) sets LOW the fan speed;
- Bit[3] = 1 sets HIGH the fan speed.

WARNING: It is recommended not to run ROC FPGA firmware **revision < 4.4** on DT5730 or DT5725 with hardware **revision ≥ 4** as the fans will work always at the maximum speed to prevent hardware damages, but with a high noisiness on the other hand.

7 Temperature Protection

TEMPERATURE PROTECTION IS NOT AVAILABLE FOR WAVEFORM RECORDING FIRMWARE RELEASES < 4.5_0.3 (REFER TO CHAP. 13)

To preserve hardware damages, the digitizer implements an automatic turning off of the board channels in event of internal over-temperature. Internal temperature can be monitored through register address 0x1nA8.

The over-temperature limit is fixed at 85°C for DT5730S/DT5725S digitizers and 70°C for the DT5730/DT5725 ones. As soon as the internal temperature exceeds this limit, the board enters the temperature protection condition and the firmware automatically performs the following actions:

- turns off all the channel ADCs;
- stops the acquisition, if running (data possibly stored at that moment can be read out in any case).

This status does not change as long as the internal temperature remains over 75°C for DT5730S/DT5725S digitizers and 62°C for the DT5730/DT5725 ones. As soon as the temperature decreases under this limit, the user can turn on the channel ADCs again and restart the acquisition, if necessary.

The temperature protection can be controlled through register addresses 0x8104 and 0x81C0.

8 Panels Description

Fig. 8.1: Front panel view

Fig. 8.2: Rear panel view

Front Panel

ANALOG INPUT

FUNCTION

Input connectors from CH0 to CH7 receive the input analog signals.

ELECTRICAL SPECS

Input dynamics:

- 2 V_{pp} (default);
- 0.5 V_{pp} SW selectable.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: MCX connectors.

Type: CS 85MCX-50-0-16 (jack/female).

Manufacturer: SUHNER.

Suggested plug/male: MCX-50-2-16.

Suggested cable: RG174 type.

CLOCK INPUT

FUNCTION

Input connector for the external clock.

ELECTRICAL SPECS

Signal type:

differential LVDS, ECL, PECL, LVPECL, CML. Single-ended to differential A318 cable adapter available (see **Tab. 1.1**).

Coupling: AC.

Z_{diff}: 100 Ω.

Accuracy < 100 ppm.

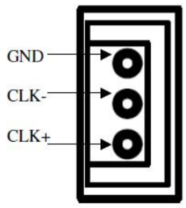
MECHANICAL SPECS

Series: AMPMODU connectors.

Type: 3-102203-4 (3-pin).

Manufacturer: AMP Inc.

PINOUT



CLK IN LED (GREEN): indicates the external clock is enabled.

GENERAL PURPOSE OUTPUT

FUNCTION

General-purpose programmable digital output connector to propagate:

- the internal trigger sources;
- the channel probes (i.e. signals from the mezzanines);
- GPI signal

according to register addresses 0x8110 and 0x811C, or

- the motherboard probes (i.e. signals from the motherboard), like the Run signal, ClkOut signal, ClockPhase signal, PLL_Unlock signal, or Busy signal

according to register address 0x811C.

ELECTRICAL SPECS

Signal level: NIM or TTL software selectable.

Requires 50 Ω termination.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

TRIGGER INPUT

FUNCTION

Digital input connector for the external trigger.

ELECTRICAL SPECS

Signal level: NIM or TTL software selectable.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

GENERAL PURPOSE INPUT

FUNCTION

General-purpose programmable input connector. Can be used to reset the time stamp (Sec. **Timer Reset**) or to start/stop the acquisition.

ELECTRICAL SPECS

Signal level: NIM or TTL software selectable.

Input impedance (Z_{in}): 50 Ω.

MECHANICAL SPECS

Series: 101 A 004 connectors.

Type: DLP 101 A 004-28.

Manufacturer: FISCHER.

Alternatively:

Type: EPL 00 250 NTN.

Manufacturer: LEMO.

OPTICAL LINK PORT

FUNCTION

Optical LINK connector for data readout and flow control. Daisy chainable. Compliant to Multimode 62.5/125 µm cable featuring LC connectors on both sides.

ELECTRICAL SPECS

Transfer rate: up to 80 MB/s.

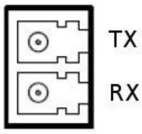
MECHANICAL SPECS

Series: SFF Transceivers.

Type: FTLF8519F-2KNL (LC connectors).

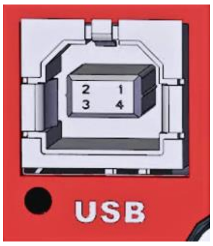
Manufacturer: FINISAR.

PINOUT



LINK LEDs (GREEN/YELLOW): right LED (GREEN) indicates the network presence, while the left LED (YELLOW) signals the data transfer activity.

USB PORT



FUNCTION

USB connector for data readout and flow control.

ELECTRICAL SPECS

Standard: compliant to USB 2.0 and USB 1.0.

Transfer rate: up to 30 MB/s.

MECHANICAL SPECS

Series: USB connectors.

Type: 787780-2 (B-Type).

Manufacturer: AMP Inc.

USB LINK LED (GREEN): indicates the USB communication is active.

DIAGNOSTIC LEDs

DTACK (GREEN): indicates there is a read/write access to the board;

TTL (GREEN): indicates the TTL standard is set for GPO, TRG IN, GPI**;**

NIM (GREEN): indicates the NIM standard is set for GPO, TRG IN, GPI;

PLL LOCK (GREEN): indicates the PLL is locked to the reference clock;

PLL BYPS (GREEN): indicates the PLL drives directly the ADCs. PLL circuit is switched off and PLL LOCK LED is turned off;

RUN (GREEN): indicates the acquisition is running (data taking). See Sec. **Acquisition Run/Stop**;

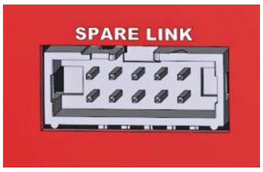
TRG (GREEN): indicates the trigger is accepted;

DRDY (GREEN): indicates the event/data is present in the Output Buffer.;

BUSY (RED): indicates all the buffers are full for at least one channel.

Rear Panel

SPARE LINK



FUNCTION

Auxiliary connector reserved for CAEN usage.

ELECTRICAL SPECS

n.a.

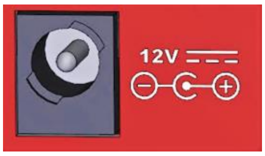
MECHANICAL SPECS

Series: Header connectors.

Type: 7610-5002-5+5.

Manufacturer: 3M.

DC INPUT



FUNCTION

Input connector for the desktop Digitizer main power supply from the external AC/DC adapter.

ELECTRICAL SPECS

Input voltage: +12V DC (typ.).

MECHANICAL SPECS

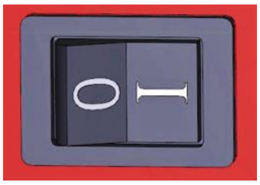
Series: CC power supply connectors

Type: RAPC722X (DC power jack).

Manufacturer: Switchcraft Inc.

PINOUT

ON/OFF SWITCH



FUNCTION

Switch for module power supply ON/OFF:

- **O** → power supply OFF.
- **I** → power supply ON.

ELECTRICAL SPECS

n.a.

MECHANICAL SPECS

Series: A1 switches.

Type: A11331122000 (Single pole two way)

Manufacturer: Molveno.

IDENTIFICATION LABEL

FUNCTION

Reports:

– the model and input range (default);

– the serial number (S/N);

– the CE conformity marking.

9 Functional Description

Analog Input Stage

The internal Programmable Gain Amplifier (**Fig. 9.1**) provides a dual input range of 2 V_{pp} (default) or 0.5 V_{pp} on the single-ended MCX coaxial connectors. To preserve the full dynamic range according to the polarity of the input signal (bipolar, positive unipolar, negative unipolar), it is possible to add a DC offset through a 16-bit DAC, which is up to ±1 V @ 2 V_{pp} and ±0.25 V @ 0.5 V_{pp}. The input bandwidth ranges from DC to 250 MHz (@3dB) for DT5730, to 125 MHz (@3dB) for DT5725 (with 2nd order linear phase anti-aliasing low-pass filter).

The input range is software selectable by directly writing at register address 0x1n28.

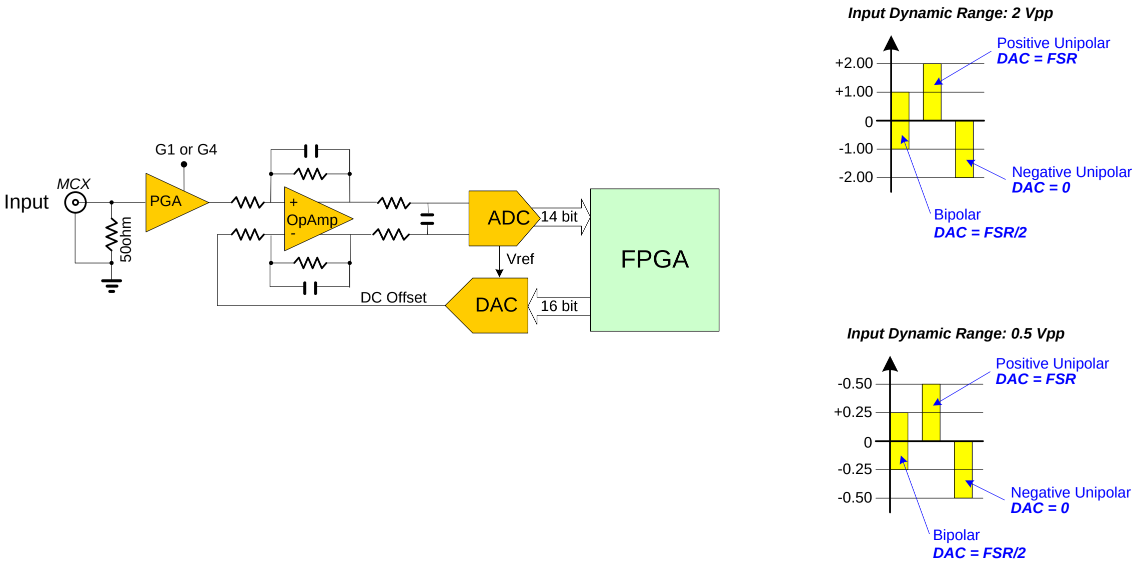


Fig. 9.1: Analog Input Diagram

DC Offset Individual Setting

Setting the DC offset for channel n can be done either by directly writing at register addresses 0x1n98 (or 0x8098 for common setting), or by library function (CAENDigitizerLib -> SetChannelDCOffset), or in the readout software **[RD6][RD8][RD9][RD10][RD11]**.

Clock Distribution

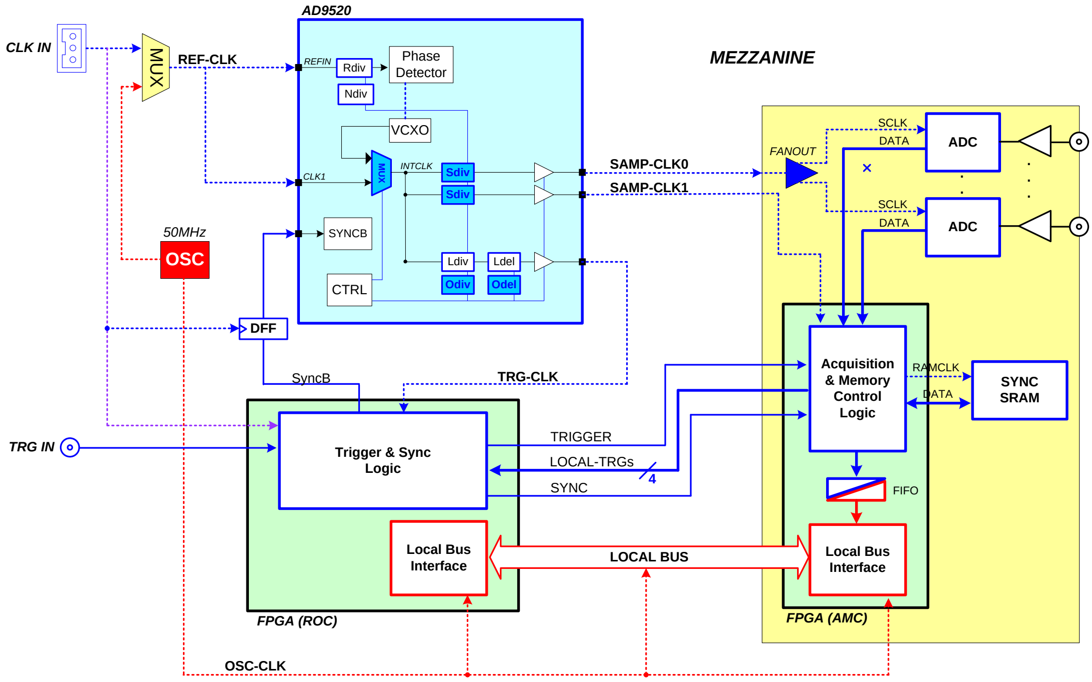


Fig. 9.2: Clock Distribution Diagram

The clock distribution of the module takes place on two domains: OSC-CLK and REF-CLK.

OSC-CLK is a fixed 50-MHz clock coming from a local oscillator that handles USB, Optical Link, and Local Bus, which takes care of the communication between motherboard and mezzanines (see red traces in **Fig. 9.2**).

REF-CLK handles ADC sampling, trigger logic, and acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. REF-CLK can be either an external (via the front panel CLK-IN connector) or an internal (via the 50-MHz local oscillator) source. In the latter mode, OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same).

REF-CLK clock source selection can be done writing bit[6] of 0x8100 register:

- INT mode (default) means REF-CLK is the 50 MHz of the local oscillator (REF-CLK = OSC-CLK);
- EXT mode means REF-CLK source is the external frequency fed on the CLK-IN connector.

CLK-IN signal must be differential (LVDS, ECL, PECL, LVPECL, CML) with a jitter lower than 100 ppm. CAEN provides the A318 cable to adapt single-ended signals coming from an external clock unit into the differential CLK-IN connector.

The DT5725 and DT5730 boards mount a phase-locked-loop (PLL) and clock distribution device, AD9520. It receives the REF-CLK and generates the sampling clock for ADCs and the mezzanine FPGA (SAMP-CLK0 and SAMPCLK1), as well as the trigger logic synchronization clock (TRG-CLK) and the output clock (CLK-OUT).

The AD9520 configuration can be changed and stored in non-volatile memory. Changing the AD9520 configuration is primarily intended to be used for external PLL reference clock frequency change (see Sec. **PLL Mode**). The digitizer locks to an external 50 MHz reference clock in the default AD9520 configuration.

Refer to the AD9520 datasheet for more details:

http://www.analog.com/static/imported-files/data_sheets/AD9520-3.pdf

(in case the active link above does not work, copy and paste it on the internet browser)

PLL Mode

The Phase Detector within the AD9520 device allows to couple REF-CLK with a VCXO (500 MHz frequency) to provide the nominal ADCs frequency (500 MHz for DT5730 and 250 MHz for DT5725).

As introduced in Sec. **Clock Distribution**, the source of the REF-CLK signal can be external on the CLK-IN front panel connector or internal from the 50 MHz local oscillator (see **Fig. 9.2**).

The following options are allowed:

1. <u>50 MHz internal clock source</u> – it is the standard operating mode, where the AD9520 dividers do not require to be reprogrammed (the digitizer works in the AD9520 default configuration). The clock source selection bit (bit[6] of 0x8100) is in default INT mode. REF-CLK = OSC-CLK.
2. <u>50 MHz external clock source</u> – in this case, the clock source is taken from an external device; the AD9520 dividers do not need to be reprogrammed as the external frequency is the same as the default one. The clock source selection bit (bit[6] of 0x8100) must be set in EXT mode. CLK-IN = REF-CLK = OSC-CLK.
3. <u>External clock source different from 50 MHz</u> – the clock signal is externally provided as in point 2, but the AD9520 dividers must be reprogrammed to lock the VCXO to the new REF-CLK and provide the nominal sampling frequency. The clock source selection bit (bit[6] of 0x8100) must be set in EXT mode. CLK-IN = REF-CLK ≠ OSC-CLK.

If the digitizer is locked, the PLL-LOCK front panel LED must be on.

Note: users who need to work as in point 3 must contact CAEN (see Chap. **14**) for feasibility, indicating the required reference clock frequency. In the positive case, CAEN provides the PLL programming file to load on the digitizer by the "Upgrade PLL" function of the CAENUpgrader software tool **[RD1]**.

Trigger Clock

The TRG-CLK logic works at 125 MHz (i.e.1/4 of the SAMP-CLK for DT5730, 1/2 for the DT5725).

Acquisition Modes

Channel Calibration

THE DT725S/DT730S DIGITIZER VERSIONS DO NOT NEED CALIBRATION!

The module performs a self-calibration of the ADCs at its power-on. Anyway, to achieve the best performance, the calibration procedure is recommended to be executed by the user, on command, after the ADCs have stabilized their operating temperature. The calibration will not need to be repeated at each run unless the operating temperature changes significantly, or clock settings are modified (e.g. switching from internal to the external clock).

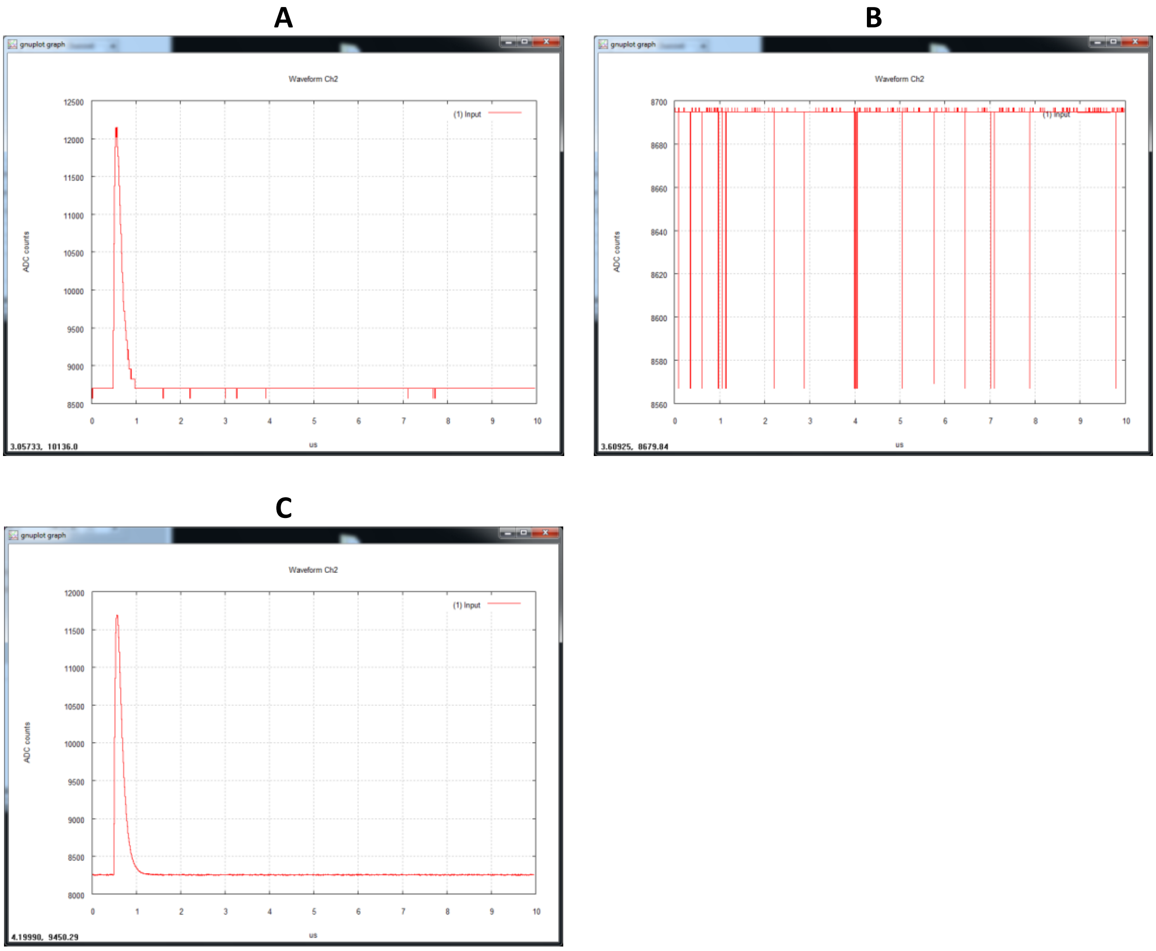
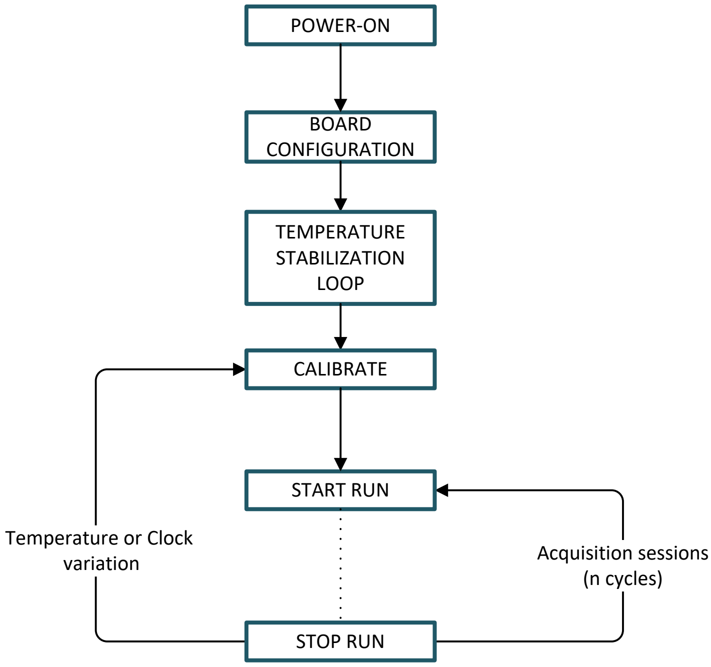


Fig. 9.3: Typical channel before the calibration (A and B) and after the calibration (C)

The diagram below synthesizes the flow for a proper calibration:



– At the low level, the ADCs temperature can be read at the register address 0x1nA8, while the calibration must be performed through register address 0x809C.

  The following steps are required:

  - Write whatever value at register address 0x809C; the self-calibration process will start simultaneously on each channel of the board and the "Calibrating bit" flag of register address 0x1n88 will be set to 0.
  - Poll the "Calibrating bit" flag until it returns to 1.

Note: It is normally not required to calibrate after a board reset but, if a Reset command is intentionally issued to the digitizer (write access at register address 0xEF24) to be directly followed by a calibration procedure, it is recommended to wait for the board to reach stable conditions (100 ms, indicatively) before to start the calibration.

Note: At power-on, a Sync command is also issued by the firmware to the ADCs to synchronize all of them to the board's clock. In the standard operating, this command is not required to be repeated by the user. If a Sync command is intentionally issued (write access at register address 0x813C), the user must consider that a new calibration procedure is needed for a correct board operating.

– At the library level, developers can refer to the routines of the CAENDigitizer library (see Chap. **10**): *ReadTemperature* function for temperature readings, *Set/GetChannelDCOffset* function for DC Offset management, *Reset* function to reset the board, and the *Calibrate* function which executes the channel calibration steps above described.

IMPORTANT NOTE: Starting from CAENDigitizer release 2.6.1, the *Reset* function has been modified so that it no longer includes the channel calibration routine implemented in the code. This calibration must be performed on command by the dedicated *Calibrate* function [RD5].

– At the software level, CAEN manages the on-command channel calibration in the available readout software (see the relevant software documentation).

➢ ***WaveDump***

1. Launch WaveDump: the software performs an automatic ADC calibration and displays a message when it is completed (see **Fig. 9.4**).

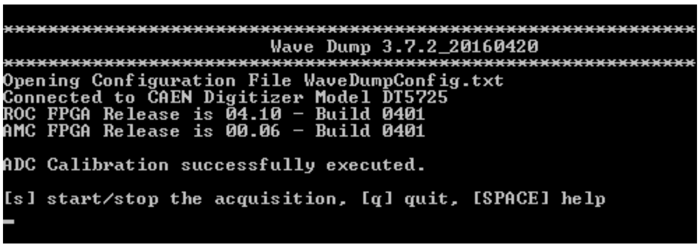


Fig. 9.4: Automatic calibration at WaveDump first run

This allows the user to start an acquisition being sure that the digitizer has been calibrated at least once.

NOTE THAT: If the SKIP_STARTUP_CALIBRATION parameter is set to YES in the WaveDump configuration file, the automatic start-up calibration is not performed, and no message is displayed.

2. At any time, once the acquisition is stopped ("s" command by keyboard), the channel temperature can be read out for monitoring ("m" command).

3. In case of significant variations, a manual channel calibration can be forced ("c" command) as in **Fig. 9.5**.

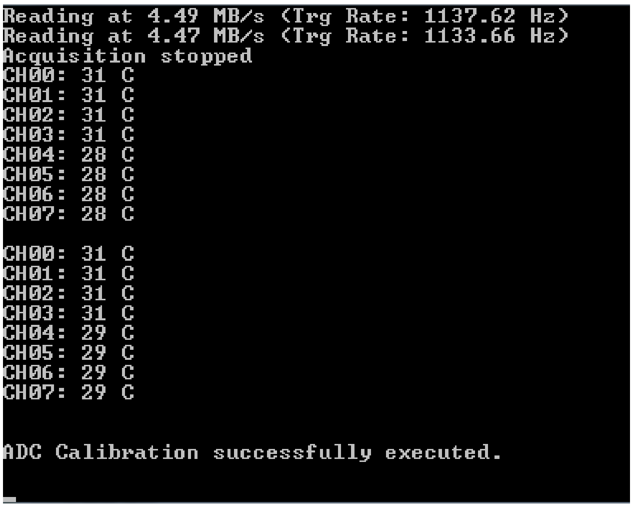


Fig. 9.5: Temperature monitoring with manual calibration in WaveDump software

4. The acquisition can then start again ("s" command).

See the WaveDump User Manual for a complete software description **[RD6]**.

- ***CoMPASS***

1.Launch CoMPASS software.

2.Connect to the digitizer.

3.Before starting the acquisition, go to the “Input” tab and enable the “Calib. ADC” checkcell.

4.Start the acquisition: the calibration of the channel ADCs is performed at every start acquisition.

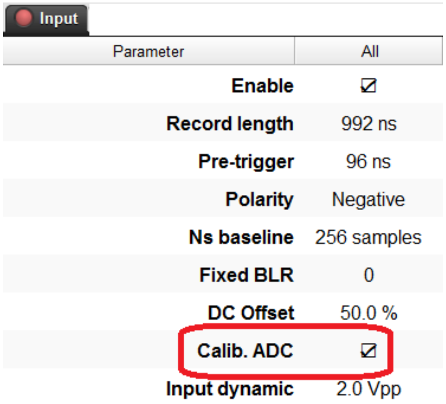


Fig. 9.6: Channel calibration in CoMPASS software

Acquisition Run/Stop

The acquisition can be started and stopped in different ways, according to bit[1:0] setting at register address 0x8100 and bit[2] of the same register:

- SW CONTROLLED (bit[1:0] = 00): Start and Stop take place by software command. Bit[2] = 0 means stopped, while bit[2] = 1 means running.

- GPI CONTROLLED (bit[1:0] = 01): acquisition is armed by setting bit[2] = 1, then two options are selectable through bit [11]:
    - START/STOP ON LEVEL - If bit[11] = 0, then acquisition starts when the GPI signal is high and stops when it is low; if bit[2] = 0 (disarmed), the acquisition is always off.
    - START ON EDGE - If bit[11] = 1, then acquisition starts on the rising edge of the GPI signal and must be stopped by software command (bit[2] = 0).

Note: the START ON EDGE option is implemented from ROC FPGA fw revision 4.22 on.

- FIRST TRIGGER CONTROLLED (bit[1:0] = 10): bit[2] = 1 arms the acquisition and the Start is issued on the first trigger pulse (rising edge) on the TRG-IN connector. This pulse is not used as a trigger; actual triggers start from the second pulse on TRG-IN. The Stop acquisition must be SW controlled (resetting bit[2]).

Acquisition Triggering: Samples and Events

In the waveform recording firmware, the arrival of the trigger signal during the acquisition provokes:

- The storage of the Trigger Time Tag (TTT), that is the time reference related to the start of the run. It is a 31-bit counter plus an overflow bit (see Sec. **Header**). The value of the counter is updated at the same frequency as the Trigger Logic Unit (see **Fig. 9.2**), that is 125 MHz (8 ns) or every 4 ADC clock cycles of the DT5730 and 2 of the DT5725. As the acquired data are written into the board internal memory in 4-sample bunches, the TTT counter value is read at half the Trigger Logic frequency (i.e. 62.5 MHz), fixing the Trigger Time Tag resolution at 16 ns for both DT5730 and DT5725 (i.e. the LSB of the TTT is always "0").
- The increment the EVENT COUNTER.
- The filling of the active buffer with the pre/post-trigger samples, whose number is programmable via register address 0x8114; the acquisition window width (also referred to as record length) is determined via register addresses 0x800C and 0x8020; then, the buffer is frozen for readout purposes, while acquisition goes on in another buffer.

An event is therefore composed of the trigger time tag, pre-, and post-trigger samples, and the event counter.

Overlap between "acquisition windows" may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via register address 0x8000).

If the board is programmed to accept the overlapped triggers, as the "overlapping" trigger arrives, the currently active buffer is filled up, then the samples storage continues in the subsequent one. In this case, not all events will have the same size (see **Fig. 9.7**)

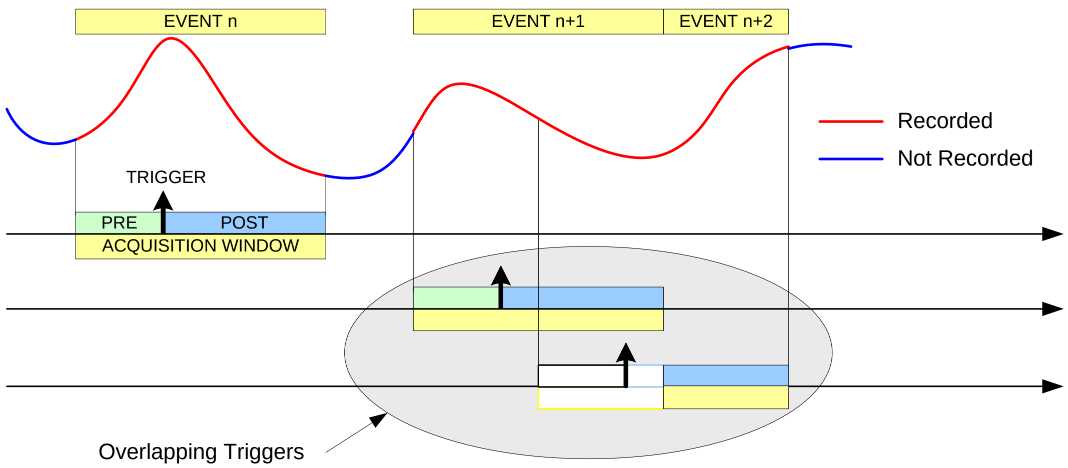


Fig. 9.7: Trigger overlap

A trigger can be refused for the following cases:

- The acquisition is not active.
- Memory is FULL and therefore there are no available buffers.
- The required number of samples for building the pre-trigger of the event is not reached yet; typically, this happens when the trigger occurs too early either with respect to the *RUN Acquisition* command (see Sec. **Acquisition Run/Stop**) or with respect to a buffer emptying after a *Memory FULL* status (see Sec. **Full/Busy Management**).
- The trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers.

As a trigger is refused, the current buffer is not frozen, and the acquisition continues writing on it. The EVENT COUNTER can be programmed to be either incremented or not. If this function is enabled, the EVENT COUNTER value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the EVENT COUNTER value coincides with the sequence of buffers saved and read out.

Multi-Event Memory Organization

Each channel of the DT5730/DT5725 features an SRAM memory to store the acquired events. The memory size for the event storage is 640 kS/ch or 5.12 MS/s, according to the board version (see **Tab. 1.1**). The channel memory can be divided into a programmable number of buffers, N_b (N_b from 1 up to 1024), by the register address 0x800C, as described in **Tab. 9.1**.

Register Value 0x800C	Buffer Number (N_b)	Size of one Buffer/channel(*)	
		SRAM 1.25 MB (640 kS)	SRAM 10.24 MB (5.12 MS)
0x00	1	1.25 MB – 20 B (640 kS – 10 S)	10.24 MB – 20 B (5.12 MS – 10 S)
0x01	2	640 kB – 20 B (320 kS – 10 S)	5.12 MB – 20 B (2.56 MS – 10 S)
0x02	4	320 kB – 20 B (160 kS – 10 S)	2.56 MB -20 B (1.28 MS – 10 S)
0x03	8	160 kB – 20 B (80 kS – 10 S)	1.28 MB – 20 B (0.64 MS – 10 S)
0x04	16	80 kB – 20 B (40 kS – 10 S)	0.64 MB – 20 B (0.32 MS – 10 S)
0x05	32	40 kB -20 B (20 kS – 10 S)	0.32 MB – 20 B (0.16 MS – 10 S)
0x06	64	20 kB – 20 B (10 kS – 10 S)	0.16 MB – 20 B (0.08 MS – 10 S)
0x07	128	10 kB – 20 B (5 kS – 10 S)	0.08 MB – 20 B (0.04 MS – 10 S)
0x08	256	5 kB – 20 B (2.5 kS – 10 S)	0.04 MB – 20 B (0.02 MS – 10 S)
0x09	512	2.5 kB – 20 B (1.25 kS – 10 S)	0.02 MB – 20 B (0.01 MS – 10 S)
0x0A	1024	1.25 kB – 20 B (640 S – 10 S)	0.01 MB – 20 B (5.12 kS – 10 S)

Tab. 9.1: Buffer Organization

Referring to the 640 kS memory size, then each buffer contains 640k/N_b samples (e.g. N_b = 1024 means 640 samples in each buffer).

(*)**IMPORTANT:** For AMC FPGA firmware release < **0.2**, the Size of one Buffer related to each Buffer Number must be intended as the number of the samples in **Tab. 9.1** without decreasing by 10 samples (20 bytes).

Custom-sized Events

In case an event size less than the buffer size is needed, the user can set the N_LOC value at register address 0x8020, where N_LOC is the number of memory locations. The size of the event is so forced to be according to the formula:

$$N_{sample} = 10 * N\_LOC$$

When N_LOC = 0, the custom size is disabled.

Note: The value of N_LOC must be set so that the relevant number of samples does not exceed the buffer size and it must not be modified while the acquisition is running. Even using the custom size setting, the number of buffers and the buffer size are not affected by N_LOC, but they are still determined by N_b.

The concepts of buffer organization and custom size directly affect the width of the acquisition window (i.e. number of the digitized waveform samples per event). The Record Length parameter defined in CAEN software (such as WaveDump and CAENScope introduced in Chap. **11**) and the *Set/GetRecordLength* function of the CAENDigitizer library rely on these concepts **[RD5]**.

Note: In the case of DPP firmware, refer to the specific documentation **[RD9]**.

Waveform Recording Event Structure

The event can be read out via Optical Link or USB; data format is 32-bit long word (see **Fig. 9.10**).

An event is structured as:

- **Header** (four 32-bit words)
- **Data** (variable size and format)

Header

The header consists of four words carrying the following information:

- **EVENT SIZE** (bit[27:0] of 1st header word) is the size of the event, that is the number of 32-bit long words to be read.
- **BOARD FAIL FLAG** (bit[26] of 2nd header word), implemented from ROC FPGA firmware revision **4.5** on (reserved otherwise), is set to "1" as a consequence of a hardware problem (e.g. PLL unlocking or over-temperature condition); the user can collect more information about the cause by reading at register address 0x8178 and contact CAEN if necessary (see Chap. **14**).
- **Bit[24]** (2nd header word) identifies the event format; it is reserved and must be 0.
- **TRG OPTIONS** (bit[23:8] of 2nd header word)**; s**tarting from revision **4.6** of the ROC FPGA firmware (reserved otherwise), these 16 bits can be programmed to provide different trigger information according to the setting of bits[22:21] at register address 0x811C (see **Tab. 9.2**).

0x811C REGISTER Bits[22:21]	FUNCTIONAL DESCRIPTION	Reserved/TRG OPTIONS INFORMATION (bit[23:8] of 2nd header word)
00 (default)	Reserved	Must be 0
01	Event Trigger Source	Indicates the trigger source causing the event acquisition: Bit[23:19] = 0000 Bit[18] = Software Trigger Bit[17] = External Trigger Bit[16:12] = 00000 Bit[11:8] = Channel Trigger requests (refer to Sec. **Self-Trigger**)
10	Extended Trigger Time Tag (ETTT)	A 48-bit Trigger Time Tag (ETTT) information is configured, where bit[23:8] contribute as the 16 most significant bits together with the 32-bit TTT field of the 4th header word
11	Not used	If configured, it acts the same as the "00" setting

Tab. 9.2: Reserved/Trg Options configuration table

- **CHANNEL MASK** (bit[7:0] of 2nd header word) is the mask of the channels participating in the event (e.g. CH0 and CH6 participating → Channel Mask = 0100 0001). This information must be used by the software to acknowledge which channel the samples are coming from (the first event contains the samples from the channel with the lowest number).
- **EVENT COUNTER** (bit[23:0] of 3rd header word) is the trigger counter; it can count either accepted triggers only, or all triggers (according to bit[3] of register address 0x8100).

- **TRIGGER TIME TAG** (bit[31:0] of 4th header word) is the Trigger Time Tag information (TTT), which is the trigger time reference (see Sec. **Acquisition Triggering: Samples and Events**). The word is composed of the value of the 31-bit counter of the Trigger Time Tag (bit[30:0]) plus the overflow bit (bit[31]) indicating that the timestamp counter has overflowed at least once (**Fig. 9.8**). If the ETTT option is enabled, then this field becomes the 32 less significant bits of the 48-bit Extended Trigger Time Tag information in addition to the 16 bits (MSB) of the TRG OPTIONS field (2nd event word). Note that, in the ETTT case, the overflow bit is no more provided (**Fig. 9.9**). The trigger time tag is reset either after each start of acquisition or via front panel signal on GPI connector and increments at the frequency of 125 MHz (8ns). The trigger time tag value is then read at half this frequency (62.5 MHz), so the Trigger Time Tag specifications result in 16 ns resolution and 17 s range (i.e. 8 ns*(2^{31}-1)), which can be extended to 625 h (i.e. 8 ns*(2^{48}-1)) by the Extended Trigger Time Tag option.

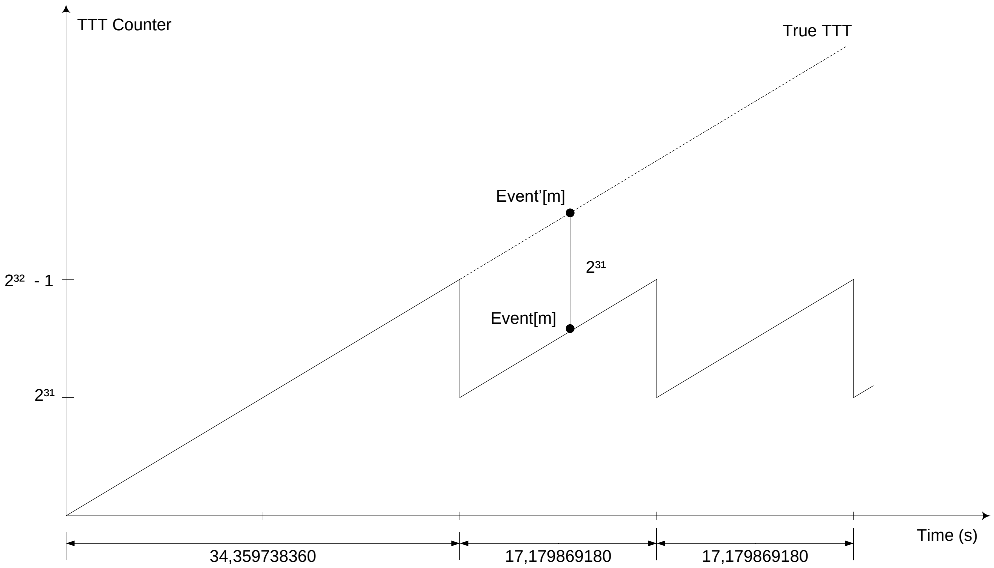


Fig. 9.8: TTT description

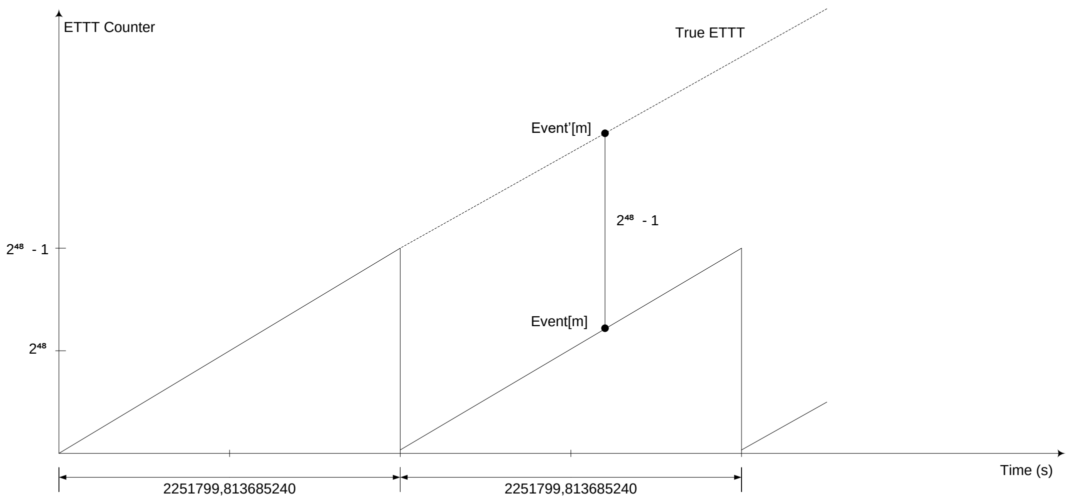


Fig. 9.9: ETTT description

Data

Data corresponds to the samples from the enabled channels. Data from masked channels are not read. Bit[31:30] of the data words identifies how many samples are stored in the corresponding word.

Event Format Example

The event format is shown in the following figure (case of 8 channels enabled).

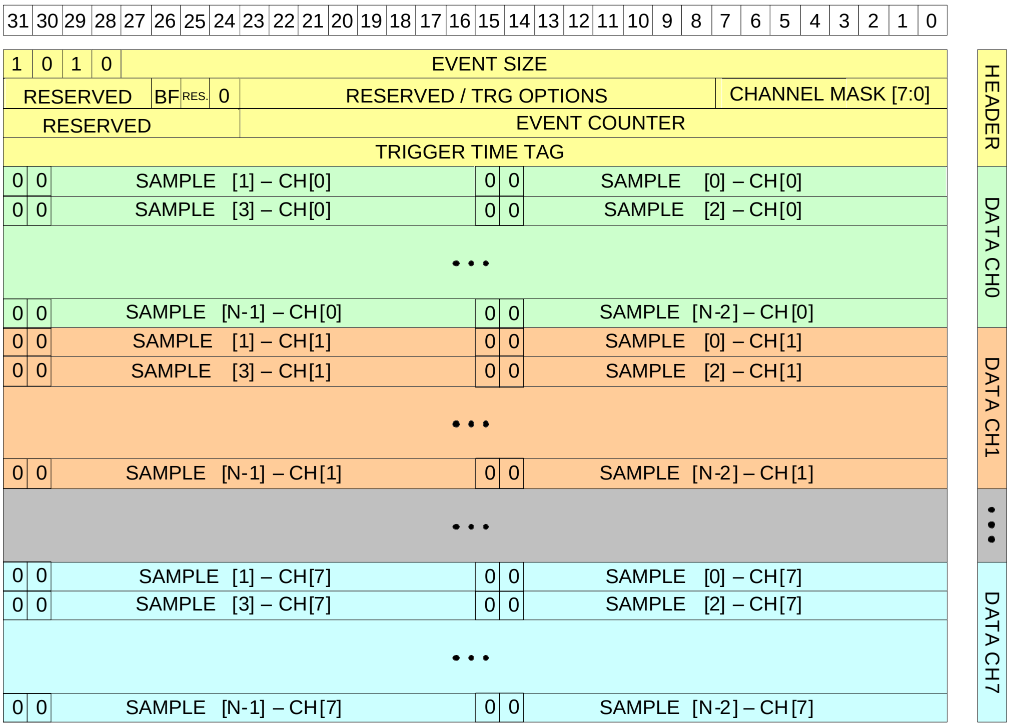


Fig. 9.10: Event format example

Full/Busy Management

Each channel of the digitizer is provided with an SRAM memory that can be organized in a programmable number N_b of circular buffers (see Sec. **Multi-Event Memory Organization**). When the trigger occurs, the FPGA writes further a programmable number of samples for the post-trigger and freezes the buffer, so that the stored data can be read via USB or Optical Link, while the acquisition can continue in a new buffer.

When all buffers are filled, the board is considered FULL: no trigger is accepted and the acquisition stops (the samples coming from the ADC are not written into the memory, so they are lost). As soon as at least one buffer is read out, the board exits the FULL condition and acquisition restarts.

IMPORTANT: *When the acquisition restarts, no trigger is accepted until at least the entire buffer is written. This means that the dead time is extended for a certain time (depending on the size of the acquisition window) after the board exits the FULL condition.*

A way to eliminate this extra dead time is by setting bit[5] = 1 at register address 0x8100. The board is so programmed to enter the FULL condition when N_b-1 buffers are written: no trigger is then accepted, but samples writing continues in the last available buffer. As soon as one buffer is read out and becomes free, the boards exit the FULL condition and can immediately accept a new trigger. This way, the FULL reflects the BUSY condition of the board (i.e. inability to accept triggers).

Note: when bit[5] = 1, the minimum number of circular buffers to be programmed is $N_b = 2$.

In some cases, the BUSY propagation from the digitizer to other parts of the system has some latency and one or more triggers may occur while the digitizer is already FULL and unable to accept those triggers. This condition causes event loss and it is particularly unsuitable when multiple digitizers are running synchronously because the triggers accepted by one board and not by other boards cause event misalignment.

In these cases, it is possible to program the BUSY signal to be asserted when the digitizer is close to the FULL condition, but it has still some free buffers (Almost FULL condition). In this mode, the digitizer remains able to accept some more triggers even after the BUSY assertion, and the system can tolerate a delay in the inhibit of the trigger generation. When the Almost FULL condition is enabled by setting the Almost FULL level to “X” (register address 0x816C), the BUSY signal is asserted as soon as X buffers are filled, although the board still goes FULL (and rejects triggers) when the number of filled buffers is N_b or $N_b - 1$, depending on the bit[5] at register address 0x8100 as above described.

It is possible to provide the BUSY signal on the digitizer front panel GPO output by bit[20], bit[19:18], and bit[17:16] at register address 0x811C.

Channel Self-Trigger Rate Meter (725S and 730S only)

Each channel of the digitizer is equipped with a digital discriminator with a programmable threshold (see Sec. **Self-Trigger**). The discriminator activity can be monitored through a special counter. The 32-bit value of this counter (register address 0x1nEC) indicates how many times per second the input pulse crossed the discriminator threshold on channel n.

Note: the counter is available for 725S and 730S models only and implemented from ROC FPGA fw revision 4.22 on.

Waveform Recording Trigger Management

When operating the waveform recording firmware, all board channels share the same trigger (board common trigger), so they acquire an event simultaneously and in the same way (determined number of samples according to the buffer organization and custom size settings, as well as the position with respect to the trigger defined by the post-trigger).

Note: For the trigger management in the DPP firmware operating, please refer to The DPP documentation **[RD9][RD10][RD11]**.

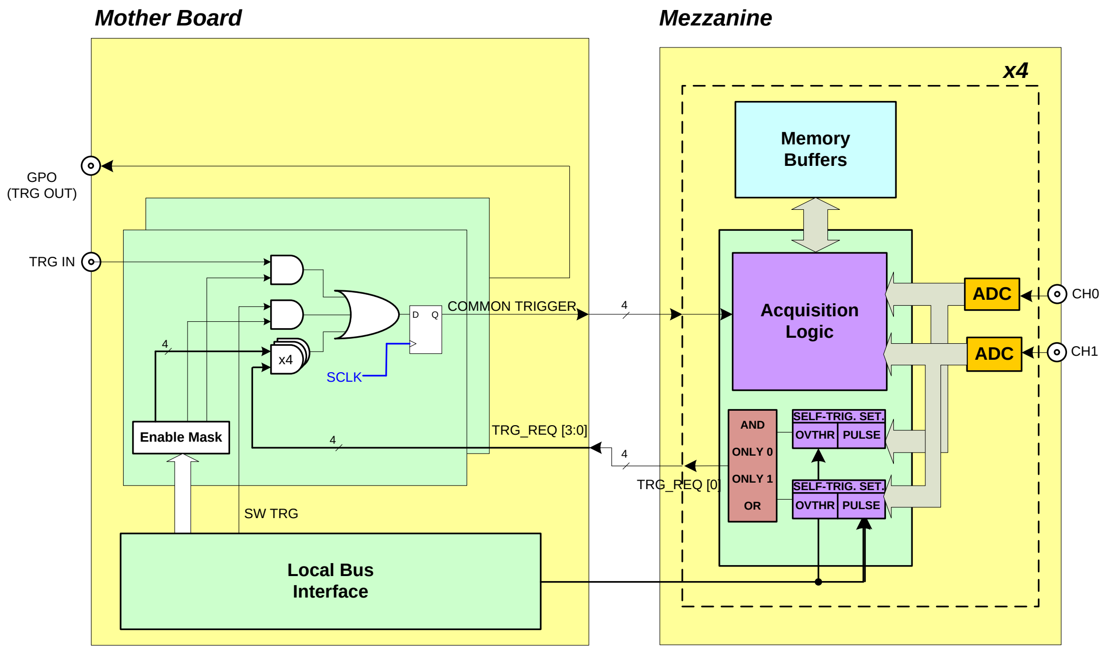


Fig. 9.11: Block Diagram of the trigger management

The digitizer supports different sources for the generation of the board common trigger (configurable at register address 0x810C):

- Software trigger
- External trigger
- Self-trigger
- Coincidence
- TRG-IN as Gate

Software Trigger

Software triggers are internally produced via a software command (write access at register address 0x8108) through USB or Optical Link.

External Trigger

A TTL or NIM external signal can be provided in the front panel TRG-IN connector (configurable at register address 0x811C). When setting up a system of multiple digitizers (see Sec. **Multi-board Synchronization**), there could be a random jitter of 1 TRG-CLK hit (see Sec. **Trigger Clock**) if the external signal is provided asynchronously with the internal clock of the boards (e.g. external trigger FAN-IN on TRG-IN). One board could then sense the trigger at clock_hit[N], while another board at clock_hit[N+1] and the same jitter is then present between the pulse acquired by one board and that acquired by the other board.

Self-Trigger

Each channel can generate a self-trigger signal when the digitized input pulse crosses a configurable threshold (register address 0x1n80). The self-triggers of each couple of adjacent channels are then processed to output a single trigger request. The trigger requests are propagated to the central trigger logic where they are ORed to produce the board common trigger, which is finally distributed back to all channels causing the event acquisition (see **Fig. 9.11**). An example of self-trigger and trigger request logic for channel 0 and channel 1 couple is schematized in **Fig. 9.12**.

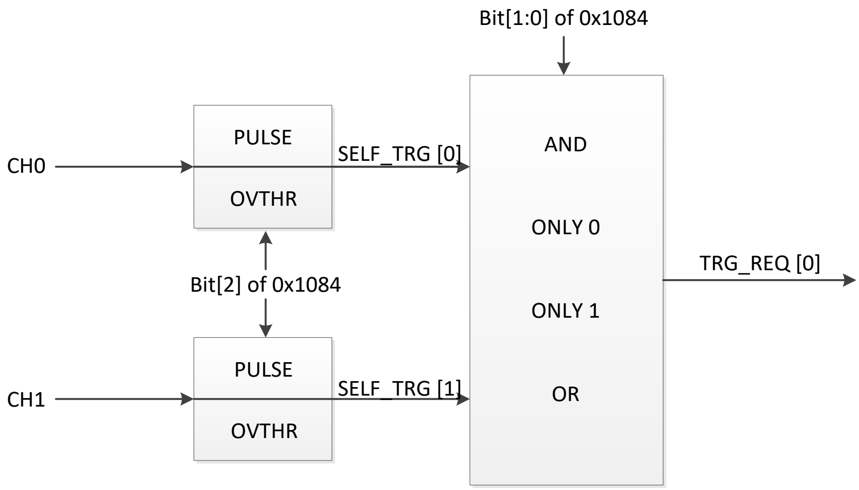


Fig. 9.12: Self Trigger and Trigger Request logic for Ch0 and Ch1 couple; a single trigger request signal is generated.

The FPGA, by register address 0x1n84, can be programmed for the self-trigger to be:

- an *over/under-threshold signal* (see **Fig. 9.13**). This signal can be programmed to be active (i.e. “1”) as long as the input pulse stays over the threshold or under the threshold (depending on the trigger polarity bit at register address 0x8000).

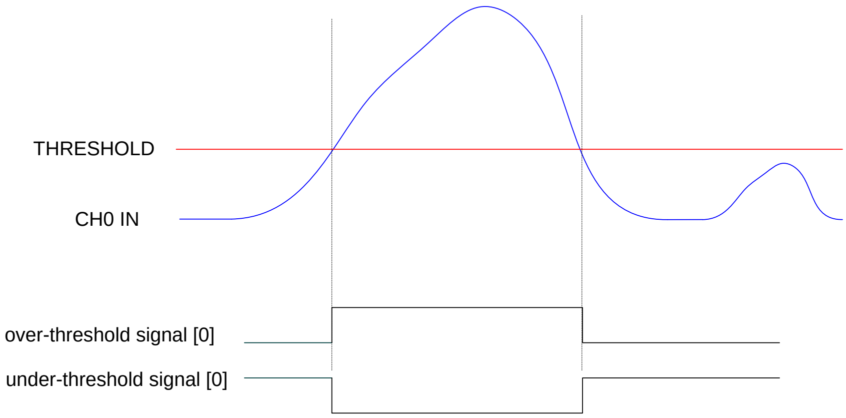


Fig. 9.13: Channel over/under threshold signal

- a *pulse of configurable width* (see **Fig. 9.14**); the width parameter can be set at register address 0x1n70.

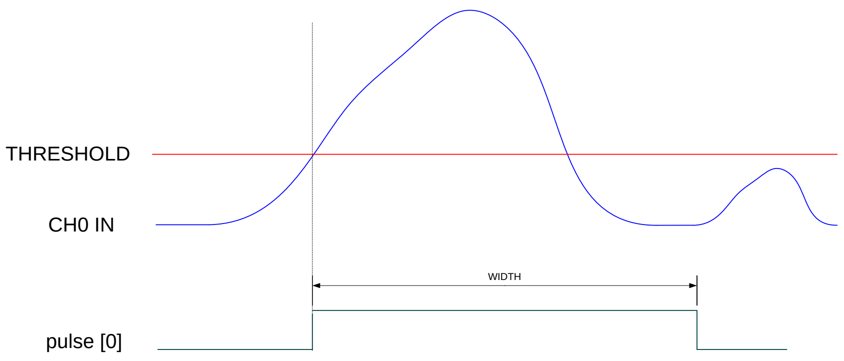


Fig. 9.14: Channel pulse signal

The FPGA, by register address 0x1n84, can be programmed for the trigger request for a couple of adjacent channels to be the

AND,

ONLY CH(n),

ONLY CH(n+1),

OR

of the relevant self-trigger signals (see **Fig. 9.12**).

Default Conditions: by default, the FPGA is programmed so that the trigger request is the OR of two pulses of 4ns-width.

Note: the above-described configurability of both the self-trigger logic and the trigger request logic are supported only by AMC FPGA firmware releases > **0.1**.
Previous revisions of the firmware do not implement the register address 0x1n84 as well as the 0x1n70; the self-trigger is intended only as the over/under threshold signal and a trigger request is intended only as the OR of the self-triggers couple.

Trigger Coincidence Level

Operating with the waveform recording firmware, the acquisition trigger is common to the whole board. This common trigger allows the coincidence acquisition mode to be performed through the Majority operation.

Note: From AMC FPGA firmware release > **0.1**, it is possible to program the self-trigger logic as described in Sec. **Self-Trigger**.

Enabling the coincidences is possible by writing at register address 0x810C:

- Bit[3:0] enable the trigger request signals to participate in the coincidence;
- Bit[23:20] set the coincidence window (T_{TVAW}) linearly in steps of the Trigger clock;
- Bit[26:24] set the Majority level (i.e. Coincidence level).

The coincidence takes place when:

Number of enabled trigger requests > Majority level

Supposing that bit[3:0] = 0xF (i.e. all the 4 trigger requests are enabled) and bit[26:24] = 01 (i.e. Majority level = 1), a common trigger is issued whenever at least two of the enabled trigger requests are in coincidence within the programmed T_{TVAW}.

The Majority level must be smaller than the number of trigger requests enabled via bit[3:0] mask. The default setting is bit[26:24] = 00 (i.e. Majority level = 0), which means the coincidence acquisition mode is disabled and the T_{TVAW} is meaningless. In this case, the board common trigger is simple OR of the signals from the enabled channels pairs.

Note: In the following pictures CH4 up to CH7 are considered disabled in order not to overload the plots.

Fig. 9.15 and **Fig. 9.16** show the trigger management when the coincidences are disabled

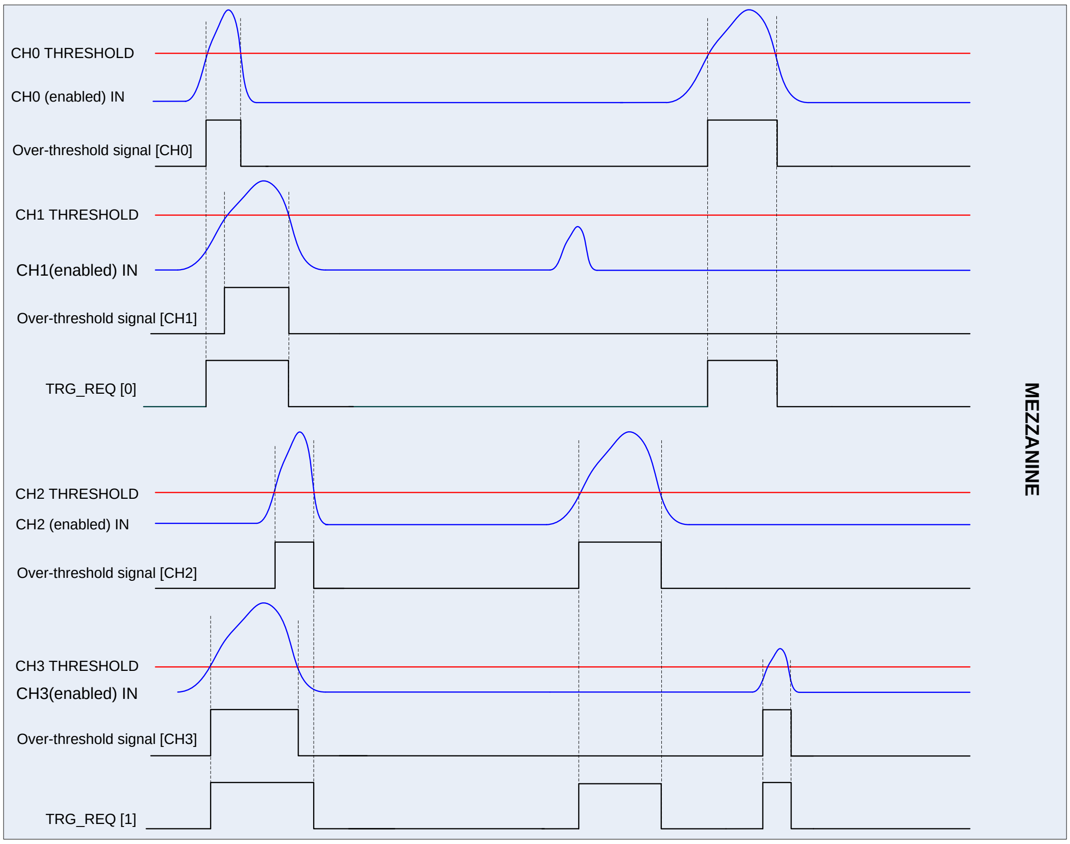


Fig. 9.15: Trigger request management at mezzanine level with Majority level = 0

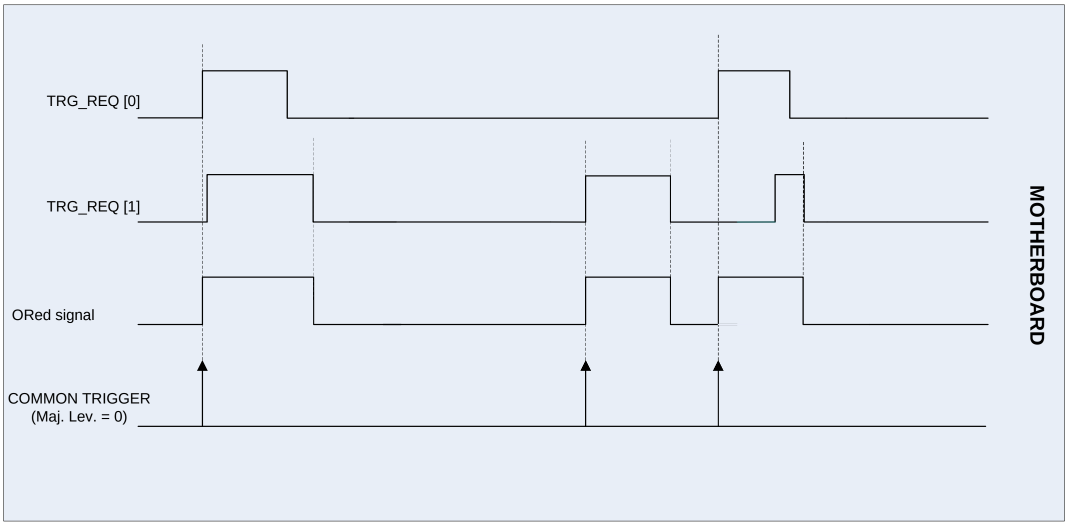


Fig. 9.16: Trigger request management at motherboard level with Majority level = 0

Fig. 9.17 and shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} is a value different from 0. To simplify the description, CH1 and CH3 channels are considered disabled, so that the relevant trigger requests are the over-threshold signals from CH0 and CH1.

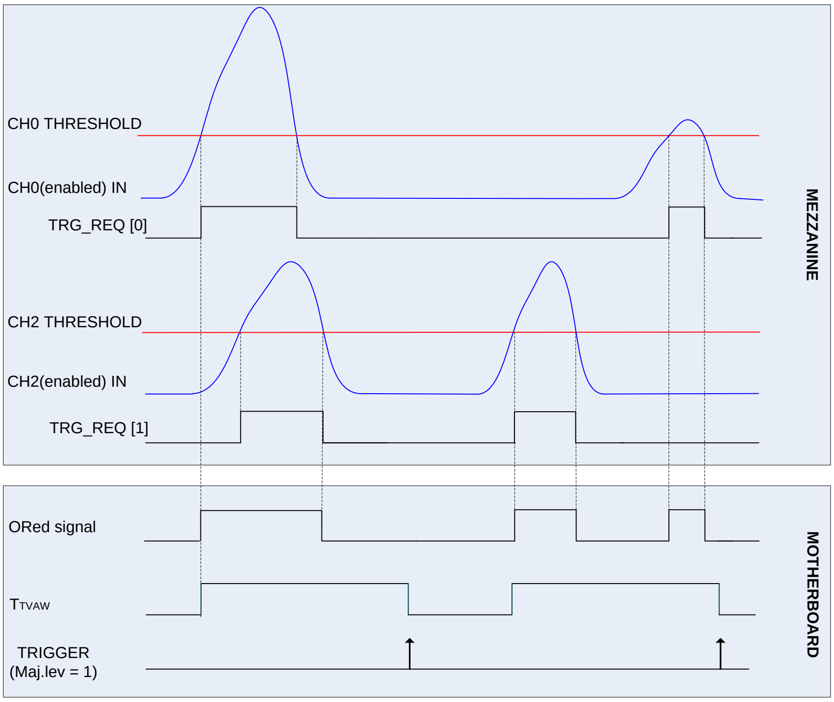


Fig. 9.17: Trigger request relationship with Majority level = 1 and $T_{TVAW} \neq 0$

Note: with respect to the position where the common trigger is generated, the portion of the input signal stored depends on the programmed length of the acquisition window and the post-trigger setting.

Fig. 9.18 shows the trigger management in case the coincidences are enabled with Majority level = 1 and T_{TVAW} = 0 (i.e. 1 clock cycle). To simplify the description, CH1 and CH3 channels are considered disabled, so that the relevant trigger requests are the over-threshold signals from CH0 and CH1.

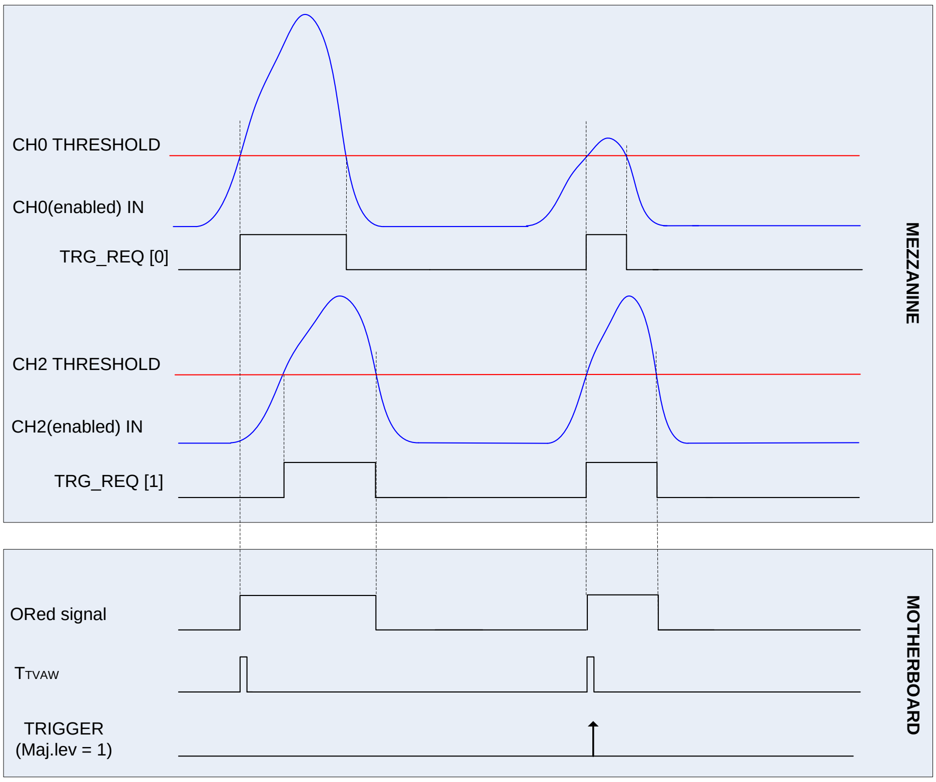


Fig. 9.18: Trigger request relationship with Majority level = 1 and T_{TVAW} = 0

In this case, the common trigger is issued when at least two of the enabled trigger requests are instantaneously in coincidence (T_{TVAW} does not apply).

Note: CAEN provides a guide to coincidences including a practical example of making coincidences with the waveform recording firmware **[RD12]**.

TRG-IN as Gate

It is possible to configure TRG-IN as a gate for trigger anti-veto function. The common acquisition trigger is then issued upon the AND between the external signal on TRG-IN and the other trigger sources but the software trigger (i.e. the software trigger cannot participate in the Trigger as Gate mode).

This mode is enabled by setting bit[27] = 1 of register 0x810C and bit[10] = 1 of register 0x811C. The trigger sources participating in AND with TRG-IN are configurable through register 0x810C as well.

Trigger Distribution

As described in Sec. **Waveform Recording** Trigger Management, the OR of all the enabled trigger sources, synchronized with the internal clock, becomes the common trigger of the board that is fed in parallel to all channels, consequently provoking the capture of an event. By default, only the Software Trigger and the External Trigger participate in the common acquisition trigger (refer to the red path on top of **Fig. 9.19**).

A Trigger Out signal is also generated on the relevant front panel GPO connector (NIM or TTL) allowing the User for extending the trigger signal to other boards.

Thanks to its configurability (see **Fig. 9.19**), GPO can propagate:

- the OR of all the enabled trigger sources (only the Software Trigger is provided by default, as in the red path of **Fig. 9.19**);
- the OR, AND, or MAJORITY exclusively of the channel trigger requests.

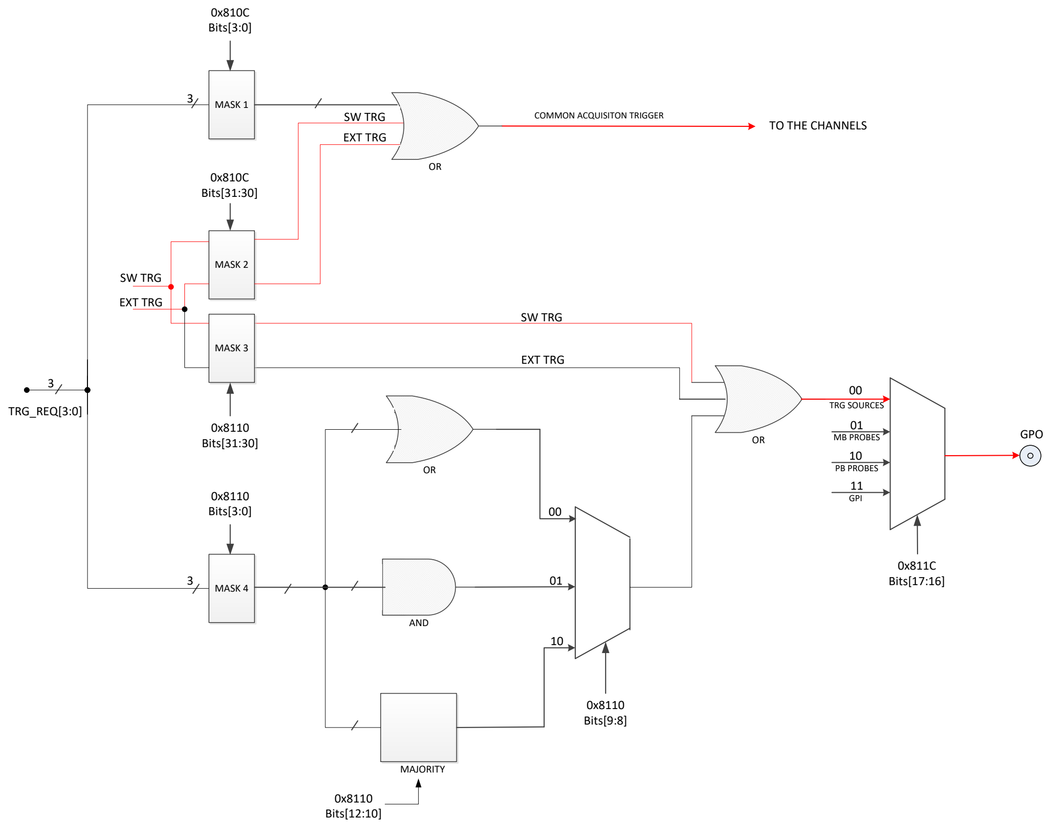


Fig. 9.19: Trigger configuration on GPO front panel output connector

The registers involved in the GPO programming are:

- 0x8110;
- 0x811C.

Example

It could be required to start the acquisition on all the channels of a multi-board system as soon as one of the channels of a board (board “n”) crosses its threshold. Trigger Out signal is then fed to an external Fan-Out logic unit; the obtained signal has then to be provided to the external trigger input TRG-IN of all the boards in the system (including the board which generated the Trigger Out signal). In this case, the programming steps to be performed are following described:

1. Register 0x8110 on board “n”:
   - Enable the desired trigger request as Trigger Out signal on board “n” (by bit[3:0] mask);
   - Disable Software Trigger and External Trigger as Trigger Out signal on board “n” (bit[31:30] = 00);
   - Set Trigger Out signal as the OR of the enabled trigger requests on board “n” (bit[9:8] = 00).
2. Register 0x811C on board “n”:
   - Configure the digitizer to propagates on GPO the internal trigger sources according to the 0x8110 settings (i.e. the enabled trigger request, in the specific case) onboard “n” (bit[17:16] = 00).
3. Register 0x810C on all the boards in the system (including board “n”):
   - Enable External Trigger to participate in the board’s common acquisition trigger, disable Software Trigger and the Trigger Requests from the channels (bit[31:30] = 01; bit[3:0] = 0000).

Multi-board Synchronization

When multi-board systems are involved in an experiment, it is necessary to synchronize different boards. In this way, the user can acquire from N boards each one with Y channels, like if they were just one board with (N * Y) channels.

While all the channels of the same board are simultaneously sampled at the same clock frequency by design, the main issue with a multi-board system is to guarantee the clock synchronization for the channels of all the boards. This is achieved by using an external clock unit, like CAEN DT4700, which generates the needed reference clock and can provide it in fan-out on the CLK-IN connector of up to ten digitizers.

Other issues are the synchronization of the start of the run to let all the boards have the same zero for timestamps, the trigger synchronization to propagate and combine the triggers from all the boards to have the same common acquisition trigger, and the event data synchronization to keep event data aligned across boards (busy/veto management).

Please, contact CAEN for details (see Chap. **14**).

Test Pattern Generator

The FPGA AMC can emulate the ADC and write into memory a sawtooth signal sweeping the entire ADC dynamics for test purposes. It can be enabled via register 0x8000.

Reset, Clear, and Default Configuration

Global Reset

Global Reset is performed at power-on of the module or via software by writing at register address 0xEF24 (whatever 32-bit value can be written). It allows clearing the data off the Output Buffer, the event counter and performs a global reset of the FPGAs restoring them to their default configuration. It initializes all counters to their initial state and clears all detected error conditions.

Memory Reset

The Memory Reset clears the data off the Output Buffer.

The Memory Reset can be forwarded via write access at register address 0xEF28 (whatever 32-bit value can be written).

Timer Reset

The Timer Reset allows initializing the timer which allows tagging an event. Time counters are reset after a SW Clear command (register address 0xEF28); the reset can also be forwarded with a pulse sent to the front panel GPI input. In case the GPI connector needs to be used to reset the trigger time stamps, no configurations or access to registers are necessary. The user only has to transmit a NIM or TTL signal to the input, depending on the software selected logic level for the GPI connector. The time stamps reset occurs at every leading edge of the logic signal sent to the GPI connector.

Data Transfer Capabilities

The board features a Multi-Event digital memory per channel, configurable by the user to be divided into 1 up to 1024 buffers, as detailed in Sec. **Multi-Event Memory Organization**. Once they are written in the memory, the events become available for readout via USB or Optical Link. During the memory readout, the board can store other events (independently from the readout) on the available free buffers.

The events are read out sequentially and completely, starting from the header of the first available event, followed by the samples of the enabled channels (from 0 to 7) as reported in **Fig. 9.10**. Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to read out an event partially.

The size of the event (EVENT SIZE) is configurable and depends on register addresses 0x8020 and 0x800C, as well as on the number of enabled channels.

Block Transfers

The Block Transfer readout mode allows to read N complete events sequentially, where N is set at register address 0xEF1C, or by using the *SetMaxNumEventsBLT* function of the CAENDigitizer library **[RD5]**.

When developing software, the readout process can be implemented on a different basis:

- Using **Interrupts**: as soon as the programmed number of events is available for readout, the board sends an interrupt to the PC over the optical communication link **(not supported by USB)**.
- Using **Polling** (interrupts disabled): by performing periodic read accesses to a specific register of the board it is possible to know the number of events present in the board and perform a BLT read of the specific size to read them out.
- Using **Continuous Read** (interrupts disabled): continuous data read of the maximum allowed size (e.g. total memory size) is performed by the software without polling the board. The actual size of the block read is determined by the board that terminates the BLT access at the end of the data, according to the configuration of register address 0xEF1C, or by the library function *SetMaxNumEventsBLT* above mentioned. If the board is empty, the BLT access is immediately terminated, and the “Read Block” function will return 0 bytes (it is the *ReadData* function in the CAENDigitizer Library **[RD5]**).

Independently from the above methods, it is suggested to ask the board for the maximum of the events per block being set. Furthermore, the greater this maximum, the greater the readout efficiency, despite a larger memory allocation required on the host station side, which is not a real drawback considering nowadays personal computers.

Single Data Transfer

This mode allows to read out one word at a time, starting from the header (4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in Sec. **Waveform Recording Event Structure**.

After the 1st word is transferred, it is suggested to check the EVENT SIZE information and then do as many cycles as necessary (EVENT SIZE -1) to read completely the event.

Optical Link and USB Access

The board houses a USB2.0 compliant port with a maximum theoretical transfer rate of 30 MB/s and a Daisy chainable Optical Link (communication path which uses optical fibre cables as physical transmission line and CONET2 serial protocol) with a maximum theoretical transfer rate of 80 MB/s supported by CAEN A2818 PCI and A3818 PCIe controllers (see **Tab. 1.1**).

A single link can connect up to 8 digitizers in a Daisy chain, so a maximum of 8 boards can be Daisy chained by the single-link A2818 card, while a maximum of 32 boards by the 4-link A3818 card.

Address Modifier, Base Address, Data Width are some of the parameters for read/write accesses via the optical link. Wrong parameter settings cause Bus Error.

Bit[3] at register address 0xEF00 enables the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed. Interrupts can also be managed at the CAENDigitizer library level **[RD5]**.

Note: CONET2 is CAEN proprietary serial protocol developed to allow the optical link communication between the host PC, equipped with A2818 or A3818 controllers, and CAEN CONET slaves. CONET2 is 50% more efficient in the data rate transfer than the previous CONET1 version. The two protocol versions are not compliant with each other and before migrating from CONET1 to CONET2 it is recommended to read the instructions provided by CAEN in the dedicated Application Note **[RD14]**.

The CONET protocol is also implemented in the A4818 adapter from USB-3.0 to Optical Link (see **Tab. 1.1**), while this device does not support the interrupts.

10 Drivers & Libraries

Drivers

To interface with the board, CAEN provides Windows® and Linux® drivers for the different types of the supported physical communication links:

- **CONET Optical Link,** managed by the A2818 (PCI) and A3818 (PCIe) cards. The driver installation packages are downloadable for free on the CAEN website at the A2818 or A3818 page respectively (**login required**).

Note: For the installation of the Optical Link driver, refer to the User Manual of the specific card **[RD13] [RD14]**.

- **USB-2.0 Link.** The driver installation packages are downloadable for free on the CAEN website at the digitizer page (**login required**).

Note: to install the USB Link driver on Windows OS, refer to the dedicated Guide **[RD3]**. Linux users can follow the installation instructions of the ReadMe file included in the packet.

- **USB-3.0 Link.** The driver installation package is required only for Windows OS and downloadable for free on the CAEN website at the adapter page (**login required**). Find the installation instructions in the adapter data sheet **[RD16]**.

Libraries

CAEN libraries are a set of middleware software required by CAEN software tools for correct functioning. These libraries, including also demo and example programs, represent a powerful base for users who want to develop customized applications for the digitizer control (communication, configuration, readout, etc.):

- **CAENDPP (DPP-PHA firmware only)** is a high-level library of C functions designed to completely control exclusively CAEN digitizers running DPP-PHA firmware and Digital MCAs. The library manages all the relevant board settings, DPP parameters configuration, data acquisition storage. Configuration of synchronized start/stop acquisition is supported in multi-board hardware setup, as well as the single board can be configured for coincidences or anticoincidences among channels. Histograms are built at the library level and managed through specific library functions; other advanced histogram functionalities are provided (e.g. histogram recovery). Lists of data can be automatically saved to output files. HV management is also handled by the library if supported by the target board.

- **CAENDigitizer** is a library of C functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware. The CAENDigitizer library is based on the CAENComm which is based on CAENVMELib, as said above. For this reason, **the CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

- **CAENComm** library manages the communication at a low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm is based in turn on CAENVMElib and it requires the CAENVMELib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why **CAENVMELib must be already installed on your PC before installing the CAENComm**.

Find the libraries' installation packages for free download on the CAEN website (www.caen.it) at the relevant library product page (**login required**).

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM CAENDIGITIZER REL. 2.15.0 ON

WHEN TO INSTALL CAEN LIBRARIES:

WINDOWS® compliant CAEN software = NO. *CAEN software for Windows® is stand-alone, which means the program locally installs the DLL files of the required libraries.*

LINUX® compliant CAEN software = YES. *CAEN software for Linux® is generally not stand-alone. The user must install the required libraries apart to run the software.*

WINDOWS® and LINUX® compliant customized software = YES. *The user must install the required libraries apart in case of custom software development.*

The CAENComm (and so the CAENDigitizer) library supports the following communication channels:

PC → USB-2.0 → DT5730/DT5725

PC → PCI (A2818) → CONET → DT5730/DT5725

PC → PCIe (A3818) → CONET → DT5730/DT5725

PC → USB-3.0 → A4818 → CONET → DT5730/DT5725

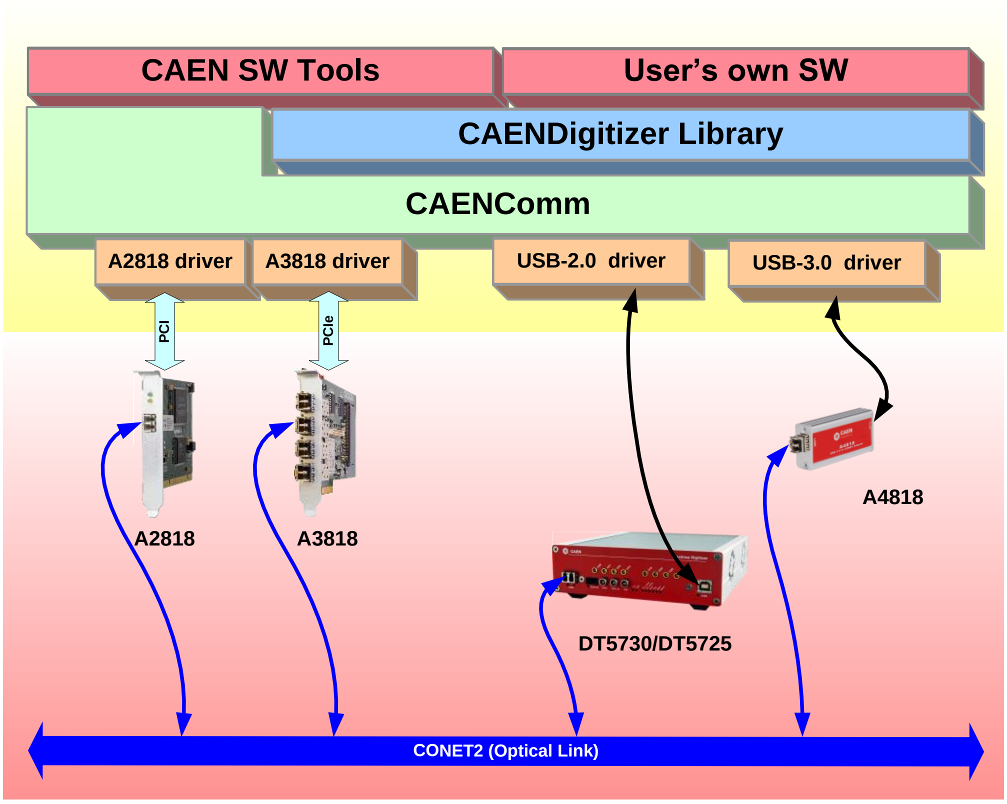


Fig. 10.1: Drivers and software layers

LabVIEW Support

CAEN also provides LabVIEW drivers for Windows OS only. The CAENVMELib and CAENComm C installation packages include LabVIEW VIs, while a dedicated CAENDigitizer LabVIEW library is available with VIs and demos for the waveform recording firmware and the different kinds of DPP firmware.

11 Software Tools

CAEN provides software tools to interface the 730 and 725 digitizer families, which are available for free download on the CAEN website (www.caen.it) in the relevant software and firmware product pages (**login required**).

CAENUpgrader

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM SOFTWARE REL. 1.6.6 ON

CAENUpgrader software is composed of command-line tools together with a Java Graphical User Interface.

With DT5730/DT5725, CAENUpgrader allows in few easy steps to:

- Upload different FPGA firmware versions on the digitizer
- Read the firmware release of the digitizer and the Controller (when included in the communication chain)
- Manage the firmware license, in case of DPP firmware
- Upgrade the internal PLL
- Get the Board Info file, useful in case of Support
- Manage the reboot of the FPGA firmware from the Backup or the Standard FLASH page.

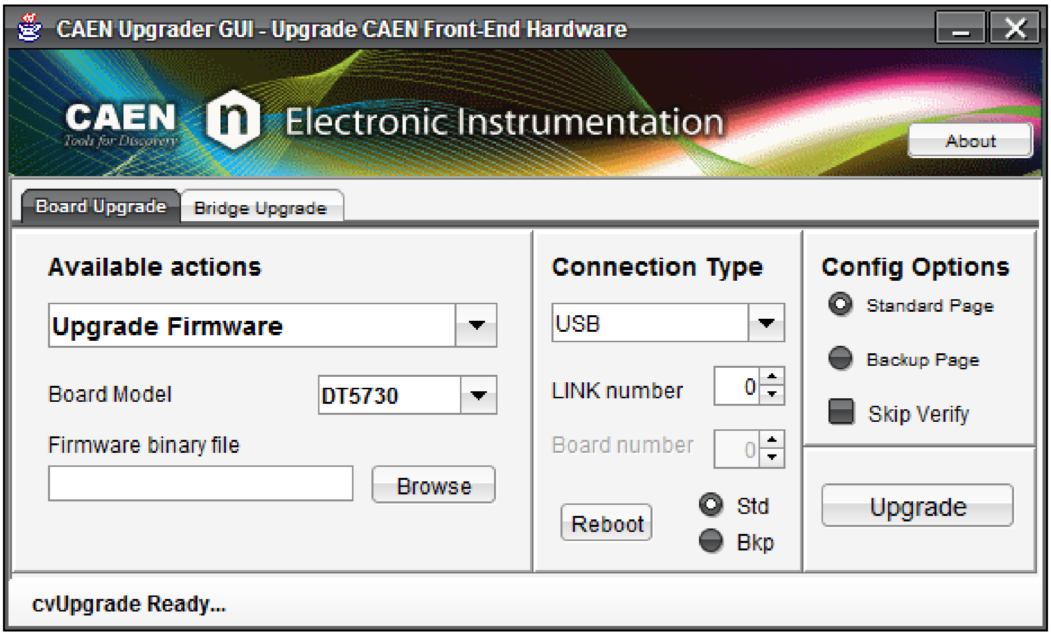


Fig. 11.1: CAENUpgrader Graphical User Interface

CAENUpgrader runs on Windows® and Linux® platforms, 32 and 64-bit operating systems. Users must also install the required third-party Oracle Java RE 8 u40 or higher.

The software relies on the CAENComm library (see Sec. **Libraries**).

CAENUpgrader for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVME and CAENCOMM libraries to be installed apart by the user.

Refer to the CAENUpgrader documentation for installation instructions and a detailed description **[RD1]**.

CAENComm Demo

CAENComm Demo is a simple software developed in C/C++ source code and provided both with Java™ and LabVIEW™ GUI interface. The demo mainly allows for a full board configuration at a low level by direct read/write access to the registers and may be used as a debug instrument.

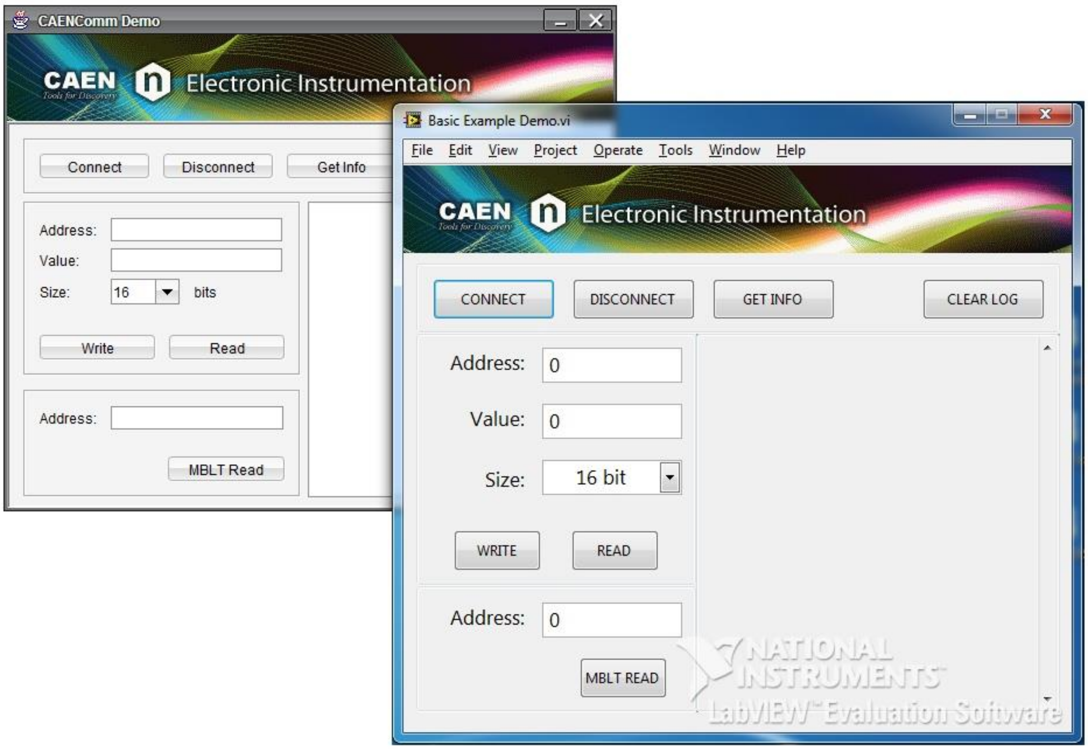


Fig. 11.2: CAENComm Demo Java™ and LabVIEW™ graphical interface

The Demo is currently provided only with the CAENComm library Windows® installation package.

Refer to the CAENComm documentation for installation instructions and a detailed description **[RD4]**.

CAEN WAVEDump

THIS SOFTWARE DOES NOT WORK WITH DPP FIRMWARE

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM SOFTWARE REL. 3.10.0 ON

WaveDump is a basic console application, with no graphics, supporting only CAEN digitizers running the waveform recording firmware. It allows the user to program a single board (according to a text configuration file containing a list of parameters and instructions), to start/stop the acquisition, read the data, display the readout and trigger rate, apply some post-processing (e.g. FFT and amplitude histogram), save data to a file and also plot the waveforms using Gnuplot (third-party graphing utility: www.gnuplot.info).

WaveDump is a very helpful example of C code demonstrating the use of libraries and methods for an efficient readout and data analysis. Thanks to the included source files and the VS project, starting with this demo is strongly recommended to all those users willing to write the software on their own.

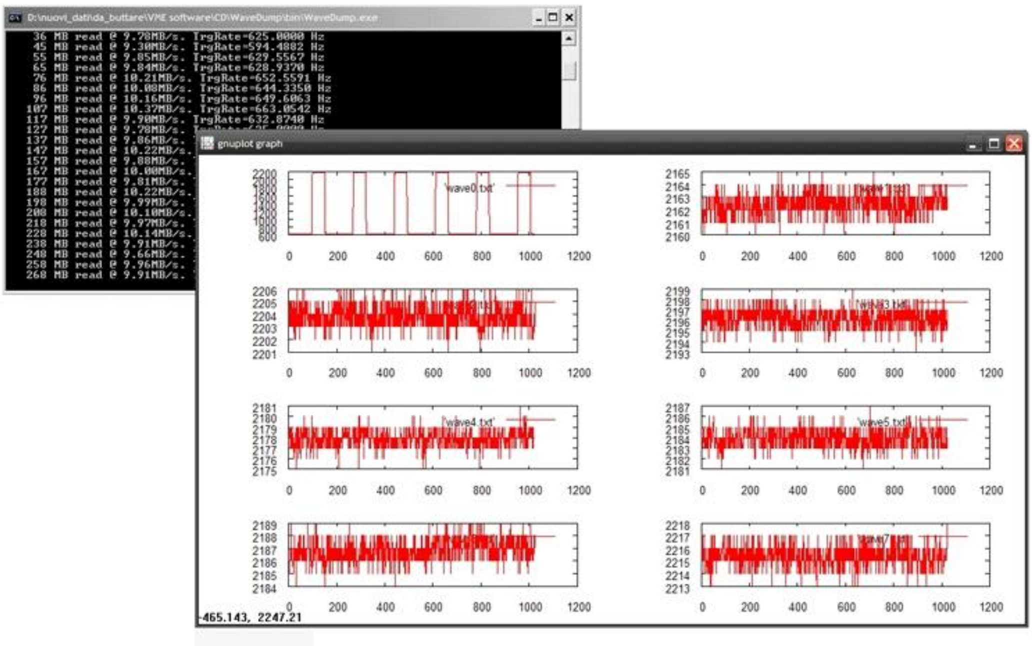


Fig. 11.3: CAEN WaveDump

CAEN WaveDump runs on Windows® and Linux® platforms. Linux users are required to install the third-party Gnuplot.

The software relies on the CAENDigitizer and CAENComm libraries (see **Libraries**).

WaveDump for Windows® is stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.
The Linux® version of the software needs the required CAENVMELib and CAENCOMM libraries to be installed apart by the user.

Refer to the WaveDump documentation for installation instructions and a detailed description **[RD6] [RD7]**.

CAENScope

THIS SOFTWARE DOES NOT WORK WITH DPP FIRMWARE

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM SOFTWARE REL 1.02 ON

In an oscilloscope-like framework, CAENScope software permits managing the waves coming from CAEN digitizers running the waveform recording firmware.

The different sections of the GUI contain all the required instruments to configure the digitizer and plot the waveforms. Once connected, the software retrieves the digitizer information. Different parameters can be set for the channels, the trigger, and the trace visualization (up to 16 traces can be simultaneously plotted). Signals are recordable to files in two different Binary formats (raw and SQLite db) and Text format (XML). It is also possible to save and restore the software settings, to import saved waves for an offline inspection.

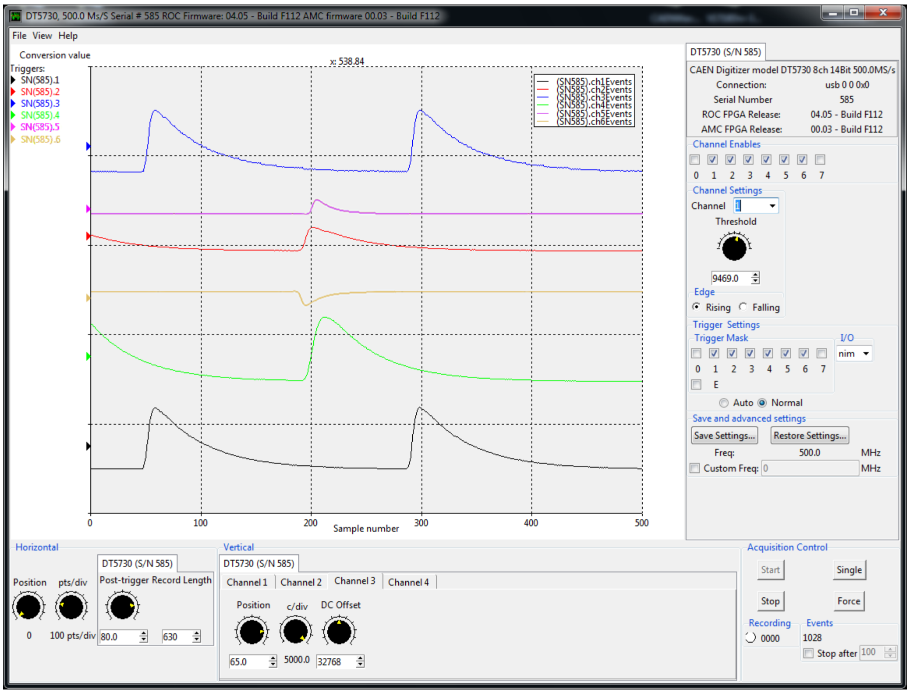


Fig. 11.4: CAENScope mainframe

CAENScope runs on Windows® and Linux® platforms.

Linux users are required to install the following packages:

- sharutils;
- libXft;
- libXss (specifically for Debian derived distributions, e.g. Debian, Ubuntu, etc.);
- libXScrnSaver (specifically for RedHat derived distributions, e.g. RHEL, Fedora, Centos, etc.).

The software relies on the CAENDigitizer and CAENComm libraries (see Sec. **Libraries**).

Note: Windows® and Linux® versions of CAENScope are stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.

Refer to the CAENScope documentation for installation instructions and a detailed description **[RD8]**.

CoMPASS

THIS SOFTWARE DOES NOT WORK WITH WAVEFORM RECORDING FIRMWARE

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM SOFTWARE REL.1.3.0 ON

CoMPASS (CAEN Muti-PArameter Spectroscopy Software) is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizer inputs and the software acquires energy, timing, and PSD spectra.

CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithms. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

CoMPASS Software supports the DPP-PSD, DPP-PHA and DPP-QDC firmware.

Fig. 11.5: CoMPASS software tool

This software is standalone both on Linux® and Windows® OS.

Refer to CoMPASS documentation for installation instructions and a detailed description **[RD9]**.

DPP-ZLEplus and DPP-DAW Control Software

THIS SOFTWARE DOES NOT WORK WITH WAVEFORM RECORDING FIRMWARE

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM DPP-DAW SOFTWARE REL. 1.0.1 ON

THE 725S/730S DIGITIZER VERSIONS ARE SUPPORTED FROM DPP-ZLE SOFTWARE REL. 1.1 WINDOWS AND REL. 1.0 LINUX

These two C software applications are provided for the DPP-ZLEplus and DPP-DAW firmware respectively. Each one allows the User configuring the parameters of the relevant DPP algorithm and control the data acquisition. The User can also take the included C source code as an example to access the underlying library functions and develop customized readout software. The package includes the source files, the Visual Studio project, and a Makefile for Linux users.

The software runs on Windows® and Linux® platforms.

The software relies on the CAENDigitizer and CAENComm libraries (see **Libraries**).

Note: Windows® and Linux® versions of the software are stand-alone, the user needs to install only the driver for the communication link, while the software locally installs the DLLs of the required libraries.

Refer to the software documentation for installation instructions and a detailed description **[RD10][RD11]**.

12 HW Installation

Power-on Sequence

To power on the board, perform the following steps:

1. connect the 12V DC power supply to the digitizer through the DC input rear connector;
2. power on the digitizer through the ON/OFF rear switch.

See Sec. **Rear Panel** to identify the relevant components

Power-on Status

At power-on, the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration.

After the power-on, only the NIM and PLL LOCK LEDs must stay on (see **Fig. 12.1)**.

Fig. 12.1: Front panel LEDs status at power-on

EXCEPT FOR THE 725S/730S VERSIONS, AFTER POWER-ON, CAEN RECOMMENDS PERFORMING THE CHANNEL CALIBRATION AS DESCRIBED ON PAGE 25 TO ACHIEVE THE BEST DEVICE PERFORMANCES

13 Firmware and Upgrades

The board hosts one FPGA on the mainboard and two FPGAs per mezzanine (i.e. one FPGA per 4 channels). The channel FPGAs firmware is identical. A unique file is provided that will update all the FPGAs at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface):

FPGA Altera Cyclone EP1C20.

AMC FPGA MEZZANINE FPGA (ADC readout/Memory Controller):

FPGA Altera Cyclone EP4CE30

or

FPGA INTEL/ALTERA ARRIA V GX

(725S and 730S versions only)

The firmware is stored onto the onboard FLASH memory. Two copies of the firmware are stored in two different pages of the FLASH, referred to as Standard (STD) and Backup (BKP). In the case of waveform recording firmware, the board is factory equipped with the same firmware version on both pages.

At power-on, a microcontroller reads the FLASH memory and programs the module automatically loading the first working firmware copy, that is the STD one in normal operating.

It is possible to upgrade the board firmware via USB or Optical Link by writing the FLASH with the CAENUpgrader software (see Chap. **11**).

IT IS STRONGLY SUGGESTED TO OPERATE THE DIGITIZER UPON THE STD COPY OF THE FIRMWARE. UPGRADES ARE RECOMMENDED ONLY ON THE STD PAGE OF THE FLASH. THE BKP COPY IS TO BE INTENDED ONLY FOR RECOVERY USAGE. IF BOTH PAGES RESULT CORRUPTED, THE USER WILL NO LONGER BE ABLE TO UPLOAD THE FIRMWARE VIA USB OR OPTICAL LINK AGAIN AND THE BOARD NEEDS TO BE SENT TO CAEN IN REPAIR!

Firmware Upgrade

Firmware updates are available for download on the CAEN website (www.caen.it) at the digitizer page **(login required)**.

Different firmware updates are available for the 725/730 digitizer families:

- The waveform recording firmware;
- The DPP firmware implementing different algorithms for Physics Applications:

  DPP-PSD firmware for the Pulse Shape Discrimination

  DPP-PHA firmware for the Pulse Height Analysis

  DPP-ZLEplus firmware with Zero Length Encoding

  DPP-DAW firmware with Dynamic Acquisition Window

The waveform recording is a free firmware and updates are free downloadable.

The DPP firmware is a pay firmware: the trial version can be freely downloaded and is fully functional for a 30-minute per power cycle operation. The user must then purchase a license and store the provided unlock code onto the digitizer to run the firmware and its updates without time limitation. The license is managed by the CAENUpgrader tool **[RD1]**.

Firmware Files Description

The programming file is a CFA file (CAEN Firmware Archive). It is an archiving file format that aggregates all the programming files of the same firmware type which are compatible with the same digitizer family.

The name of the CFA file follows a general convention:

- *<DIGITIZER>*_rev_X.Y_W.Z.CFA for the waveform recording firmware
- *<DIGITIZER>*_*<DPP_ALGORITHM>*_rev_X.Y_W.Z.CFA for the DPP firmware

where:

<DIGITIZER> means all the boards that can be updated by the CFA file:

- x730 (includes x730, x730B, x730C, x730D module versions)
- x730S (includes x730S, x730SB, x730SC, x730SD module versions)
- x725 (includes x725, x725B, x725C, x725D module versions)
- x725S (includes x725S, x725SB, x725SC, x725SD module versions)

Note: The “x” prefix stands for DT5 in the case of desktop format, N6 for NIM format, and V1/VX1 for VME64/VME64x format);

<DPP_ALGORITHM> is the DPP firmware type (options are DPP-PSD, DPP-PHA, DPP-ZLEplus, DPP-DAW)

X.Y is the major/minor revision number of the ROC FPGA

W.Z is the major/minor revision number of the AMC FPGA

To discriminate between the waveform recording firmware and the DPP ones by the firmware version, the reference is the major revision number of the AMC FPGA (W):

W < 128 means a waveform recording firmware

W ≥ 128 means a DPP firmware, and it is a fixed number specific for each DPP and digitizer family.

For the 730 and 725 digitizer families:

W = 136 means DPP-PSD firmware

W = 139 means DPP-PHA firmware

W = 140 means DPP-ZLEplus firmware

W = 141 means DPP-DAW firmware

Troubleshooting

In case of upgrade failure (e.g. STD FLASH page is corrupted), the user can try to reboot the board: after a power cycle, the system programs the board automatically from the alternative FLASH page (e.g. BKP FLASH page), if this is not corrupted as well (see Sec. **Power-on Status**). The user can so perform a further upgrade attempt on the STD page to restore the firmware copy.

The reboot from the FLASH pages is managed by CAENUpgrader only through the USB link (**Fig. 13.1**).

Fig. 13.1: Reboot section of CAENUpgrader

Note: old versions of the digitizer motherboard have slightly different FLASH management. It is always recommended to use the latest release of CAENUpgrader software (see. Chap. **11**) to get the BoardInfoFile (using the "Get Information" function) and check that the FLASH_TYPE = 0. Alternatively, use a software utility like CAENComm Demo to read at register address 0xF050 and check that bit[7] = 0. In this case, at power-on, the micro-controller loads exactly the firmware copy from the STD page of the FLASH.

When a failure occurs during the upgrade of the STD page of the FLASH, which compromises the communication with the DT5730/725, the user can perform the following recovering procedure as the first attempt:

- force the board to reboot loading the copy of the firmware stored on the BKP page of the FLASH. For this purpose, make sure to connect by USB link and use the "Reboot" function in CAENUpgrader software by checking the "Bkp" option;
- use CAENUpgrader to read the firmware revision (in this case the one of the BKP copy). If this succeeds, it is so possible to communicate again with the board;
- use CAENUpgrader to load the proper firmware file on the STD page, then power-cycle in order the board to get operative again.

If neither of the procedures here described succeeds, it is recommended to send the board back to CAEN in repair (see Chap. **14**).

14 Technical Support

CAEN makes available the technical support of its specialists for requests concerning the software and hardware. Use the support form available at the following link:

https://www.caen.it/support-services/support-form/

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