



User Manual UM5960

**CoMPASS**

Multiparametric DAQ Software for Physics Applications

Rev. 3 - February 6<sup>th</sup>, 2018

# Purpose of this Manual

The User Manual contains the full description of the CoMPASS readout software compliant with 720, 725, 730, and 751 digitizer series running DPP-PSD firmware (releases 4.9\_131.11 for x720, 4.11\_136.11 for x725 and x730, 4.11\_132.8 and 4.12\_132.33 for x751), and 724, 725, 730, and 781 digitizer series running DPP-PHA firmware (releases 4.15\_128.36 for x724 and x781 and 4.15\_139.8 for x725 and x730). For future release compatibility check the release notes files.

## Change Document Record

Date	Revision	Changes
September 28 <sup>th</sup> , 2017	00	Initial Release
November 9 <sup>th</sup> , 2017	01	Added support to CoMPASS for Linux OS. Added Tof plot which was missing in the previous version.
December 12 <sup>th</sup> , 2017	02	Modified Statistics tab. Added "Real time playback" in the Offline run.
February 6 <sup>th</sup> , 2018	03	Added "Channel time offset" option in the Sync/Trg tab.

## Symbols, abbreviated terms and notation

ADC	Analog-to-Digital Converter
AMC	ADC & Memory Controller
DAQ	Data Acquisition
DAC	Digital-to-Analog Converter
DC	Direct Current
DPP	Digital Pulse Processing
DPP-QDC	DPP for Charge to Digital Converter
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
LVDS	Low-Voltage Differential Signal
ROC	ReadOut Controller
USB	Universal Serial Bus

## Reference Documents

- [RD1] W. R. Leo. *Techniques for Nuclear and Particle Physics Experiments*. Ed. by Springer. II ed.
- [RD2] L.Stevanato et al., "Pulse shape discrimination with fast digitizers". In: *NIM A* 748 (2014), pp. 33–38.
- [RD3] AN2506 - Digital Gamma Neutron discrimination with Liquid Scintillators.
- [RD4] UM4380 - 725-730 DPP-PSD Registers Description.
- [RD5] UM5110 - 751 DPP-PSD Registers Description.
- [RD6] GD2827 - How to make coincidences with CAEN digitizers.
- [RD7] UM4855 - 720 DPP-PSD Registers Description.
- [RD8] AN2086 - Synchronization of CAEN Digitizers in Multiple Board Acquisition Systems.
- [RD9] V.T. Jordanov and G.F. Knoll, "Digital Synthesis of pulse shapes in real time for high resolution radiation spectroscopy". In: *NIM A* 345 (1994), p. 337.
- [RD10] GD6300 - CoMPASS Quick Start Guide.

All CAEN documents can be downloaded at: <http://www.caen.it/csite/LibrarySearch.jsp>

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CAEN S.pA.

Via Vetraia, 11 55049 Viareggio (LU) - ITALY

Tel. +39.0584.388.398 Fax +39.0584.388.959

[info@caen.it](mailto:info@caen.it)

[www.caen.it](http://www.caen.it)

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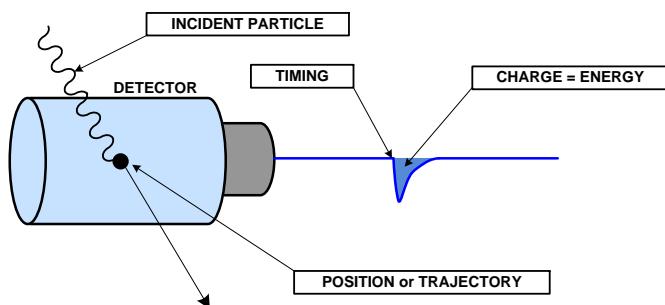
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# 1 Introduction

The function of the Front End electronics in nuclear physics applications is to acquire the electrical charge pulses generated by a detector, to extract the quantities of interest and to convert them into a digital format. These information are then acquired, saved and analyzed by a computer. In most applications, relevant quantities are the particle energy (proportional to the charge released by the particle in the detector) and the time of arrival; in some cases the acquisition is restricted to the pulse counting, actually a “selective” counting, meaning that one or more energy intervals or other criteria are used to select which particles must be counted. In some other cases, it is necessary to discriminate the type of the particle by means of the pulse shape; for example, the  $\gamma$ -n discrimination is based on a detector response variation when stimulated by a gamma or a neutron; this variation leads to a different rise and/or decay time of the pulse. The acquisition system is usually completed by digital logic units whose purpose is to perform (anti)coincidences, generate triggers, vetoes and other signals that take into account the correlation between different channels and may give further information such as the particle position or trajectory.

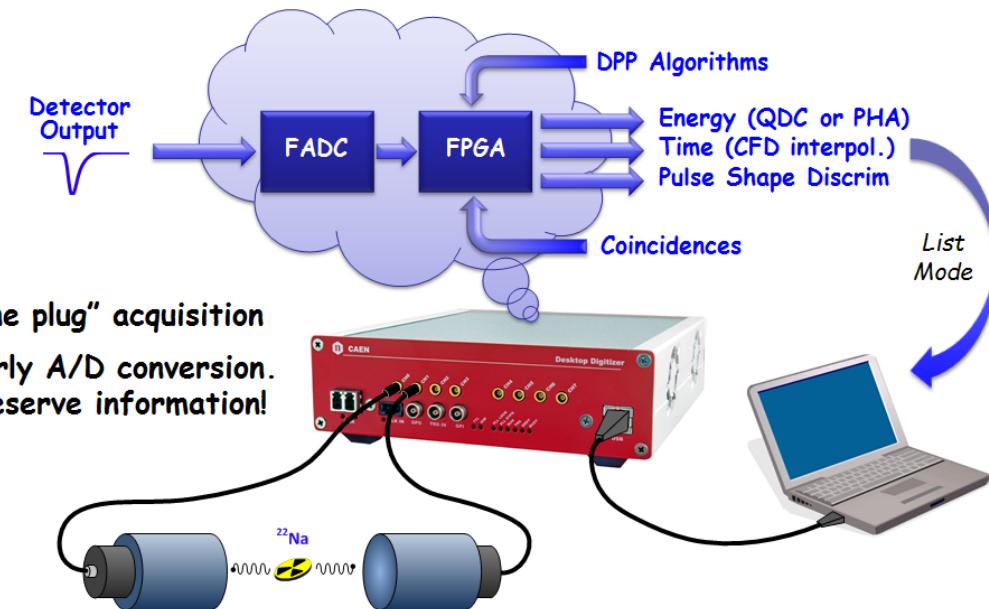


**Fig. 1.1:** Electrical charge pulse generated by a particle interacting with a detector.

Nowadays, the availability of very fast and high precision flash ADCs permits to design acquisition systems in which the Analog to Digital conversion occurs as close as possible to the detector. In principle, this acquisition system allows to minimize the information loss. Actually, the acquisition will be affected by uncertainties due to the quantization noise and to other sources of electronic noise. In general, the applications that require precise timing measurements are more oriented to the use of high sample frequency digitizers (500 MS/s or more), while the 12-14 bit digitizers are well suited for acquisitions where high energy resolution is a pre-requisite.

In recent years, the use of waveform digitizers for readout of radiation detectors has become popular in many different physics applications: the conventional analog electronics is going to be replaced by a full digital approach, where the detector output (with or without preamplifier, depending on the detector type) is directly connected to the digitizer input. This approach is especially beneficial in multi-parametric acquisition systems, where the analysis involves different quantities and parameters, such as energy, pulse shape and timing. In fact, thanks to Digital Pulse Processing (DPP) it is possible to apply dedicated algorithms on-line (typically in the FPGAs), to extract the information of interest from the raw waveform. DPP algorithms allow the digitizer to implement in “one single box” the different functionalities of the old fashion TDC, QDC, Peak Sensing ADC, discriminator and other analog and logic modules [RD1]. Furthermore, the DPP allows the digital readout to be sustainable in terms of data throughput because the full waveform is not necessarily read out but used for debugging purposes only. This results in an “all-in-one, multi-parametric digital DAQ for physics applications”.

CAEN has developed a complete family of waveform digitizers well suited for physics, medical, homeland security and industrial applications. They are available in different form factors (VME, Desktop and NIM)



**Fig. 1.2:** All-in-one Spectroscopy DAQ.

as showed in Tab. 1.1. In addition, CAEN developed also several digital pulse processing algorithms that allows the user to extract a set of significant information like energy, precise timing, PSD and so on [RD1]. Tab. 1.2 shows the functionalities supported by the different models and that will be described in the following sections.

MODEL <sup>(1)</sup>	Form Factor	# channels	Sampling Frequency (MS/s)	# Bits	Input Dynamic Range (Vpp)	Bandwidth (MHz)	Memory (Msample/ch)		DPP firmware
							Record Length small	big	
<b>x724</b>	VME	8	100	14	0.5 - 2.25 - 10	40	0.5	4	PHA
	Desktop/NIM	4					500 $\mu$ s	4ms	
<b>x720</b>	VME	8	250	12	2	125	1.25	10	PSD
	Desktop/NIM	4					5ms	40ms	
<b>x730</b>	VME	16	500	14	0.5 and 2	250	1.25	10	PHA, PSD
	Desktop/NIM	8					250 $\mu$ s	2ms	
<b>x725</b>	VME	16	250	14	0.5 and 2	125	1.25	10	PHA, PSD
	Desktop/NIM	8					500 $\mu$ s	4ms	
<b>x751</b>	VME	8	1000/2000	10	1	500	1.8/3.6	14.4/28.8	PSD
	Desktop/NIM	4					1.8ms	14.4ms	
<b>x781</b>	Desktop/NIM	4	100	14	0.3 - 1 - 3 - 10	5	0.5		PHA
							500 $\mu$ s		

**Tab. 1.1:** CAEN Waveform Digitizers selection table.

Model	Waveform Recording	PHA	PSD	CFD	QDC
x730	✓	✓	✓	✓	✓
x725	✓	✓	✓	✓	✓
x751	✓		✓	✓	✓
x724	✓	✓			
x720	✓		✓		✓
x781	✓	✓			

**Tab. 1.2:** Functionalities implemented in the CAEN digital algorithms and supported by the digitizers.

**CoMPASS** is the new software from CAEN able to implement a Multi-parametric DAQ for Physics Applications, where the detectors can be connected directly to the digitizers inputs and the software acquires energy, timing, and PSD spectra. CoMPASS software has been designed as a user-friendly interface to manage the acquisition with all the CAEN DPP algorithm. CoMPASS can manage multiple boards, even in synchronized mode, and the event correlation between different channels (in hardware and/or software), apply energy and PSD cuts, calculate and show the statistics (trigger rates, data throughput, etc...), save the output data files (raw data, lists, waveforms, spectra) and use the saved files to run off-line with different processing parameters.

CoMPASS Software supports CAEN x720, x724, x725, x730, x751 digitizer families running the DPP-PSD, and DPP-PHA, and the x781 MCA family. More details about the supported boards and firmware are given in the following sections.



**Note:** 725, 730, and 751 series requires the calibration of the ADCs before starting the acquisition. CoMPASS performs the calibration at every start acquisition.

## 2 Charge Integration and $\gamma$ -N discrimination: the DPP-PSD Firmware

A digitizer running the DPP-PSD firmware becomes a multichannel data acquisition system for nuclear physics or other applications requiring radiation detectors. The digitizer accepts signals directly from the detector and implements a digital replacement of *Dual Gate QDC*, *Discriminator* and *Gate Generator*. All these functionalities are performed inside the board FPGA without any use of external cables, nor additional boards or delay lines. The acquisition is therefore performed by a single compact system which replaces the traditional analog boards. It is also possible to operate with multi-board systems: the front panel clock, the trigger and the general purpose LVDS I/Os connectors (VME only) make possible the synchronization of several boards.

Finally both the board configuration and the acquisition can be completely managed by the CAEN CoMPASS Software, which allows the user to set the parameters for the acquisition, to configure the boards, and to perform the data readout. It allows also to collect and plot the time, energy and PSD spectra, to apply filters and to save the data.

The main functionalities of a digitizer running DPP-PSD firmware are listed below, where any parameter can be programmed by the provided software:

- Auto selection of the events with a digital leading edge discrimination or a digital constant fraction discrimination (725, 730, and 751 series only);
- Input signal baseline (pedestal) calculation and pedestal subtraction for energy calculation;
- Single gate integration for the energy spectra calculation;
- Double integration of the prompt and delayed charge for Pulse Shape Discrimination.

Fig. 2.1 shows a typical example of signals from neutrons and gamma, where it is possible to see a difference in the waveform shapes. The slow and fast components are used by the algorithm to compute the PSD, according to the formula:

$$\text{PSD} = \frac{(Q_{\text{Long}} - Q_{\text{Short}})}{Q_{\text{Long}}} \quad (2.1)$$

which corresponds to the ratio between the integral of the tail ( $Q_{\text{long}} - Q_{\text{short}}$ ) and the total charge ( $Q_{\text{long}}$ ).

See [RD2] for an example of DPP-PSD application for gamma-neutron discrimination in liquid scintillators, and [RD3] for an application of the performances of the event selection based on the described algorithm.

 **Note:** The description of the DPP-PSD system of this Manual is compliant with DPP-PSD firmware release 4.9\_131.11 for 720 series, DPP-PSD firmware release 4.11\_136.10 for 725 series and 730 series, DPP-PSD firmware release 4.11\_132.8 and 4.12\_132.33 for 751 series, and CoMPASS Software release 1.0. For future release compatibility check in the firmware and software revision history files.

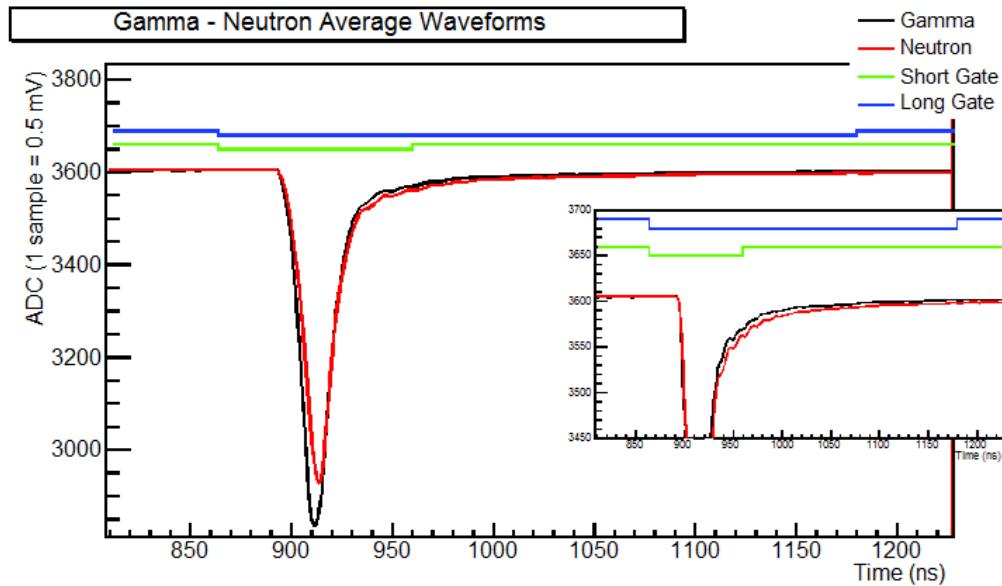


Fig. 2.1: Plot of typical  $\gamma$ -Neutron waveforms.

## Principle of Operation

The figure below shows the functional block diagram of the DPP-PSD firmware:

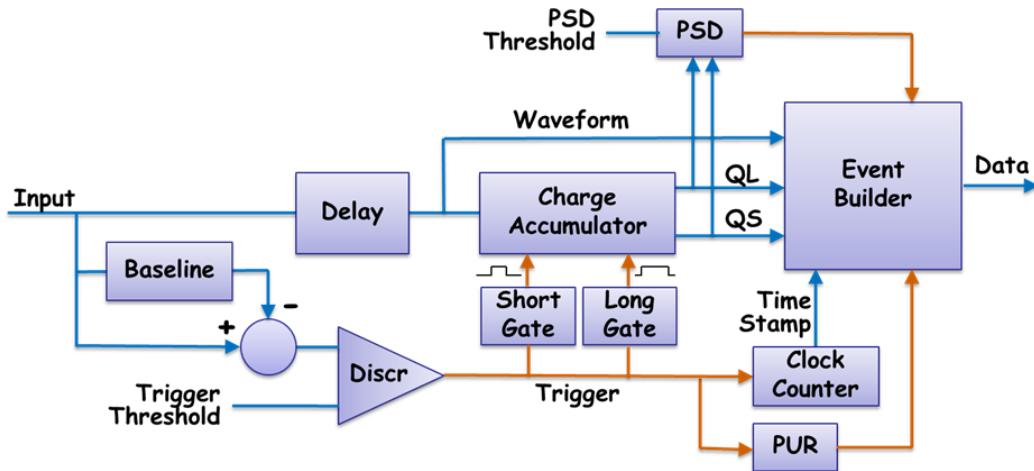
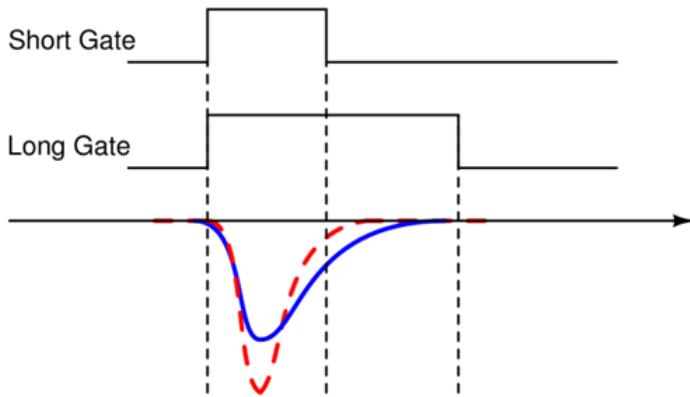


Fig. 2.2: Functional Block Diagram of the DPP-PSD.

The aim of the DPP-PSD firmware is to perform a charge integration of the input signal and to calculate the PSD factor performing a double gate integration of the input ( $Q_{\text{short}}$  and  $Q_{\text{long}}$ ). Fig. 2.3 shows the short and long gates position for two signals of different shapes.

The following sub-sections summarizes the DPP-PSD features.



**Fig. 2.3:** Long and short gate graphic position with respect to a couple of input pulses. The blue pulse has a longer tail than the red one.

## Baseline calculation

The digitizer continuously receives the input signal and digitizes it. The position of the signal baseline can be adjusted in the ADC scale to exploit the full dynamics of the digitizer using the **DC Offset** parameter.

The baseline value is an important parameter of the DPP-PSD firmware, since its value is used as a reference value for the charge integration of the input pulses. Moreover, most of the DPP parameters are related to the baseline value, like the trigger threshold.

The user can set either a fixed value for the baseline, or let the DPP firmware calculate it dynamically. In the first case the user must set the baseline value in LSB units through the command **Fixed BLR**. This value remains fixed for the entire acquisition run. In the latter case the firmware dynamically evaluates the baseline as the mean value of N points inside a moving time window. The user can choose the N value among 8, 32, and 128 for 720 series; 8, 16, 32, 64, 128, 256, and 512 for 751 series, and 16, 64, 256, 1024 for 725 and 730 series. The baseline is then frozen from few clocks before the gates start, up to the end of the maximum value between the long gate and the trigger hold-off<sup>1</sup>. For 751 series the freeze lasts some trigger clocks more than this maximum value. After that the baseline restarts again its calculation considering in the mean value also the points before the freeze. This allows to have almost no dead-time due to the baseline calculation.



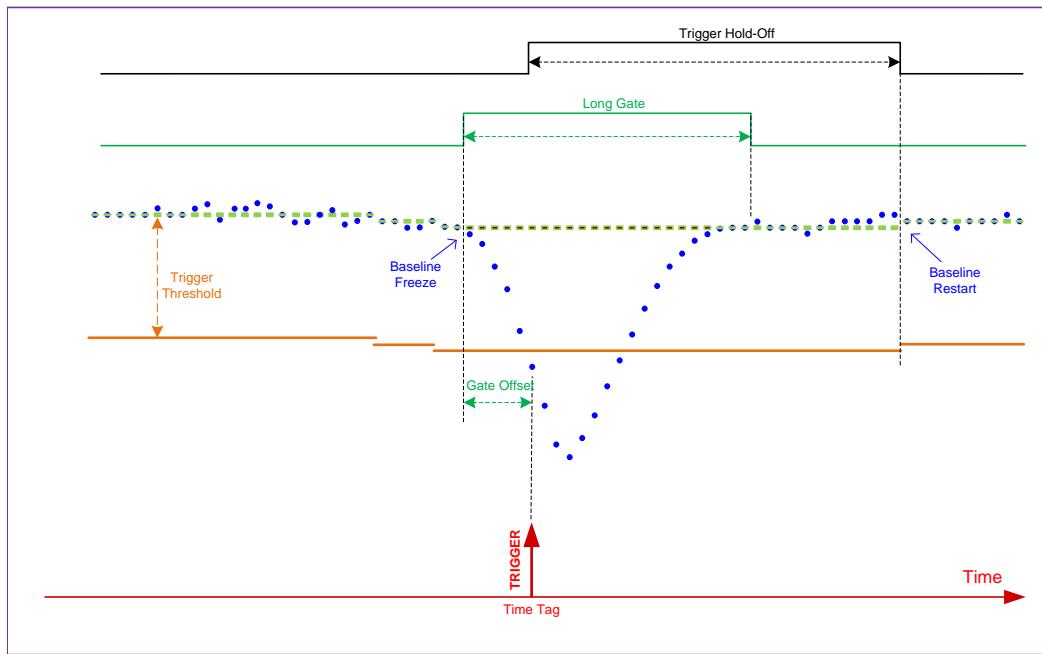
**Note:** In case of 725 and 730 series the user can set the time before the gate for the baseline freeze start, through register 0x1nD8 (default value = 16 ns). This option can be useful when the gate does not cover the beginning of the signal, and the baseline becomes distorted. The baseline freeze lasts for the maximum value among the long gate, the trigger hold-off, and the over-threshold signals.



**Note:** In case of 725 and 730 series the baseline remains frozen also on events clipping in the gate (saturation) and on opposite polarity. Refer to Sect. **Veto (725 and 730 series only)** for additional details.

Fig. 2.4 shows how the baseline calculation and freeze work. The trigger threshold dynamically follows the baseline variations. Note that in case of overshoots before the charge integration the baseline can be distorted and the reference for the trigger threshold might not be accurate. In that case it might be more convenient to use the fixed baseline value.

<sup>1</sup>The trigger hold-off defines the time window after the trigger where other triggers are inhibited



**Fig. 2.4:** Baseline calculation as managed by the DPP-PSD algorithm.

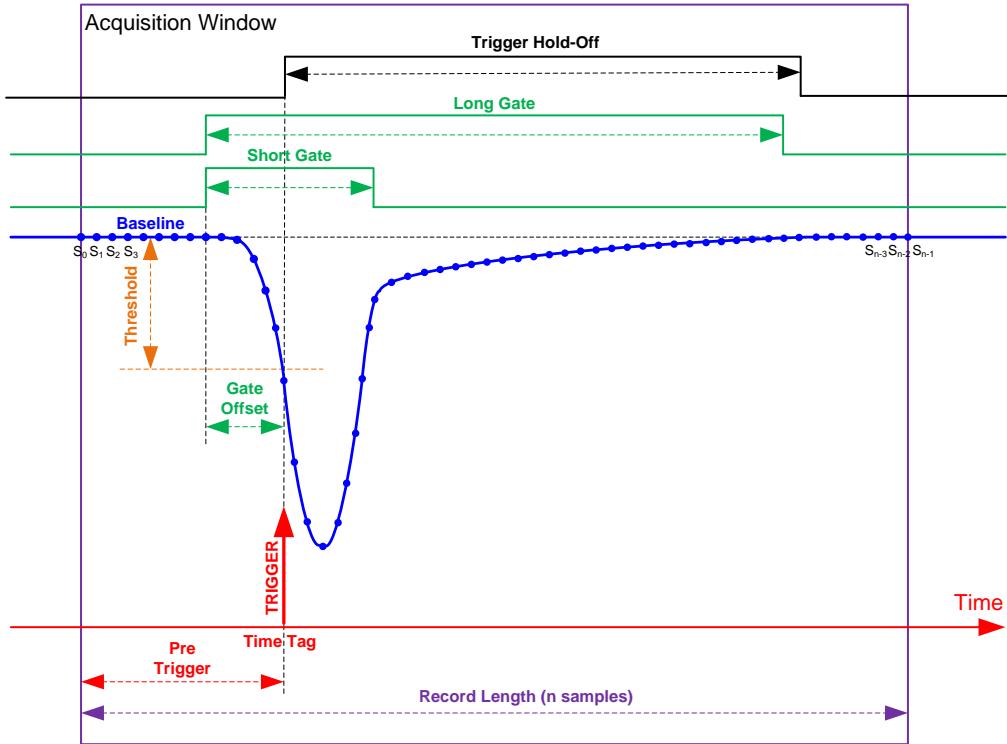
## Trigger Management

The DPP-PSD allows the user to select the pulses according to two methods: leading edge, where a pulse is identified when its samples crosses a programmable threshold value, or through a digital constant fraction discrimination to have a better timing information.

In both cases once the event is selected, the signal is delayed by a programmable number of samples (corresponding to the “pre-trigger” value in ns) to be able to integrate the pulse before the trigger (“Pre-Gate”). The gates for charge integration are then generated and are received by the charge accumulator before the signal. While the gates are active the baseline remains frozen to the last averaged value and its value is used as charge integration reference. For the whole duration of a programmable “trigger hold-off” value, other trigger signals are inhibited. It is recommended to set a trigger hold-off value compatible with the signal width. The baseline remains frozen for the whole trigger hold-off duration. For 751 series the baseline remains frozen for a longer time. Fig. 2.5 summarizes all the DPP-PSD parameters.

### Digital Leading Edge

The baseline value, which can be a fixed value selected by the user, or continuously calculated by the firmware is then subtracted from the input signal, giving  $\text{input\_sub} = \text{input} - \text{baseline}$  (Digital Baseline Restorer). The  $\text{input\_sub}$  value is compared with the value of the trigger threshold and the event is selected as soon as the  $\text{input\_sub}$  signal crosses the threshold (see Fig. 2.5). The time stamp precision in the pulse identification is equal to the ADC sampling (4 ns for 720 and 725 series, 2 ns for 730, and 1 ns for 751).



**Fig. 2.5:** Diagram summarizing the DPP-PSD parameters. The trigger fires as soon as the signal crosses the threshold value. Long Gate, Short Gate, Gate Offset, Pre-Trigger, Trigger Hold-Off, and Record Length are also shown for one acquisition window.

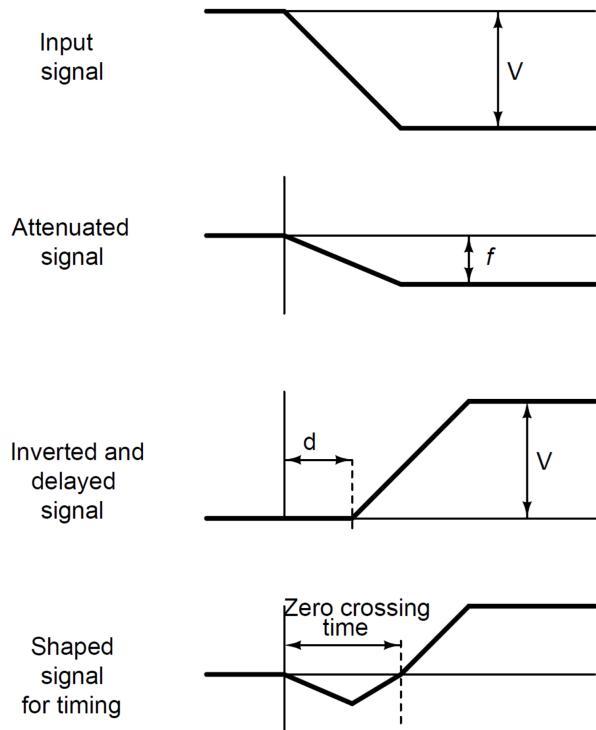
## Digital Constant Fraction Discrimination (725, 730, and 751 series)



**Note:** The CFD for 751 series is supported from DPP-PSD firmware release **greater than 132.32**.

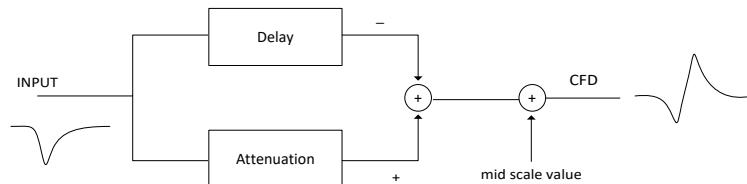
Using analog signals the Time Stamp determination is traditionally done with CFD (Constant Fraction Discriminator) modules. This technique sets the time stamp of a pulse to the time when the amplitude reaches a fixed fraction of the full amplitude. The DPP-PSD firmware for 725, 730, and 751 families intends to exploit the advantages of a CFD technique using a digital sampling device. The standard implementation of the leading edge trigger (refer to Sec. **Digital Leading Edge**), that may suffer from amplitude walk issues. Conversely triggering on a constant fraction of the input may reduce this issue since it is independent from the amplitude pulse. On the other side a simple linear interpolation between two points can solve the problem of the sampling clock granularity, thus improving the timing resolution.

The digital CFD signal has been implemented in the classical way. The input waveform is attenuated by a factor  $f$  equal to the desired timing fraction of full amplitude, then the signal is inverted and delayed by a time  $d$  equal to the time it takes the pulse to rise from the constant fraction level to the pulse peak; the latest two signals are summed to produce a bipolar pulse, the CFD, and its zero crossing – corresponding to the fraction  $f$  of the input pulse – is taken as the trigger time (see Fig. 2.6).



**Fig. 2.6:** Classical implementation of the Constant Fraction Discriminator. The input signal is first attenuated by a factor  $f$ , then inverted and delayed. The resulting signal has its zero crossing corresponding to the set fraction  $f$ .

The digital implementation of the CFD is shown in Fig. 2.7. The input sample is split into two path: the first performs the delay in steps of the sampling clock (4 ns in case of 725, 2 ns in case of 730 series, 1 ns in case of 751 series), the second performs the attenuation. Possible choices of attenuation are: 25%, 50%, 75%, and 100% (i.e. no attenuation) with respect to the input amplitude. The CFD signal is referred to the mid-scale of the dynamics, i.e. channel 8192 in case of 725 and 730 series, channel 512 for 751 series.



**Fig. 2.7:** Implementation of the digital CFD in the DPP-PSD firmware of 725, 730, and 751 series. Mid-scale value corresponds to 8192 in case of 725 and 730 series, 512 for 751 series.

To enable the CFD discrimination the user must set the related option in the Discrimination tab of the Settings (see Sec. **The Discriminator Tab**).

It is also possible to select which samples are used for the zero crossing linear interpolation. The  $n$ -th sample before and after the zero crossing must be chosen according to the CFD signal, in such a way they are in the linear slope of the CFD itself. By default the first samples before and after the zero crossing are used by CoMPASS. To modify this value the user must use a FreeWrites command (refer to Sec. **The Acquisition Tab**) writing at 0x1n3C [RD4], [RD5].



**Note:** The interpolation points are used also in case of Leading Edge Discrimination.

A typical signal from CFD is shown in Fig. 2.8, where the red points are the digital samples. The Sample

Before the Zero Crossing (SBZC) and the Sample After the Zero Crossing (SAZC) are the samples before and after the zero crossing (in case of interpolation they are the n-th samples before and after the ZC).

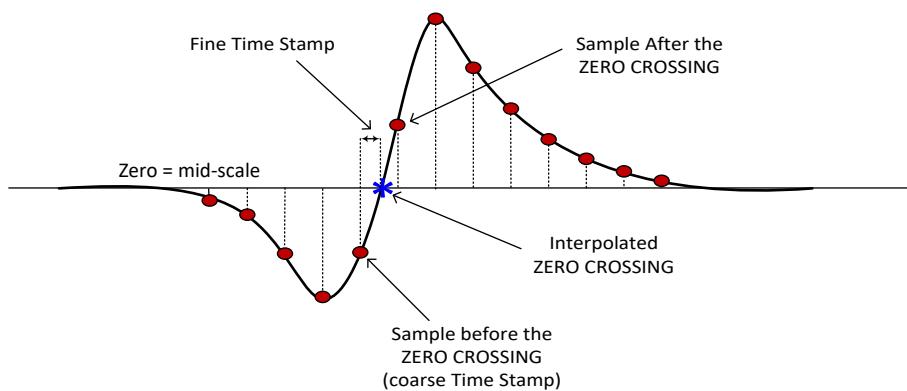
The SBZC corresponds to the Coarse Time Stamp ( $T_{\text{coarse}}$ ), that is the trigger time stamp as evaluated by the standard PSD algorithm (leading edge). The value of the Fine Time Stamp  $T_{\text{fine}}$  (see Fig. 2.8) is calculated as the linear interpolation of the SBZC and the SAZC according to the formula:

$$T_{\text{fine}} = \frac{\text{midScale} - \text{SBZC}}{\text{SAZC} - \text{SBZC}} \cdot T_{\text{sampler}} \quad (2.2)$$

where midScale corresponds to 8192 in case of 725 and 730 series, and 512 for 751 series, and  $T_{\text{sampler}}$  is the sampling period of the specific series (4 ns in case of 725, 2 ns for 730, 1 ns in case of 751).

The “Interpolated Zero Crossing” (ZC) then corresponds to the sum of the Coarse Time Stamp and the Fine Time Stamp.

$$ZC = T_{\text{coarse}} + T_{\text{fine}} \quad (2.3)$$



**Fig. 2.8:** A typical CFD signal. Red points are the digital samples. The Sample Before the Zero Crossing (SBZC) and the Sample After the Zero Crossing (SAZC) are the samples before and after the zero crossing. The SBZC corresponds to the Coarse Time Stamp. The algorithm can also evaluate the Fine Time Stamp, and the corresponding time will be the sum of the SBZC and the Fine Time Stamp.

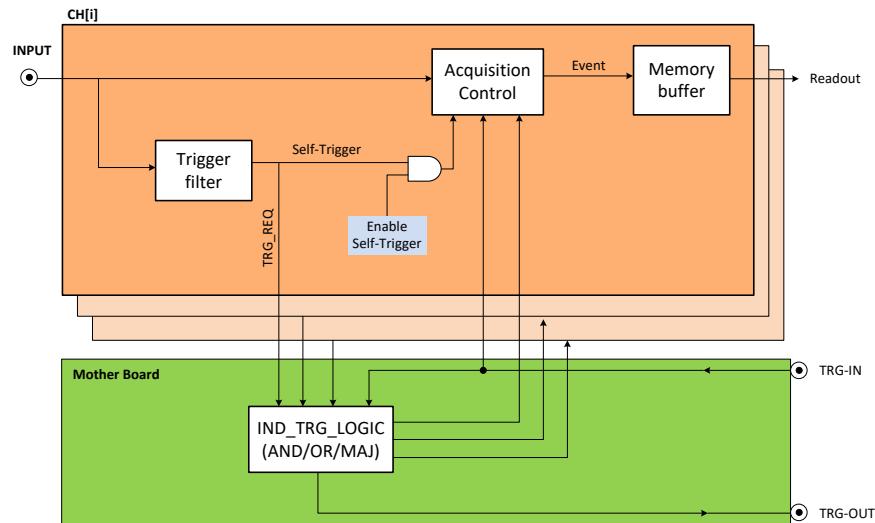
The fine time stamp is reported as a 10 bit number by the FPGA, thus corresponding to a precision of  $T_{\text{samp}}/1024$ , which is about 1 ps for 751 series, 2 ps for 730, and 4 ps for 725.

## Multi Trigger Options

The DPP-PSD firmware allows for several way of trigger generation:

1. each channel can “self-trigger” on its own input signal when the input crosses a programmable threshold, or through the CFD (725, 730, and 751 only). The self-trigger works on each channel independently from the other channels;
2. each channel triggers independently, then only those events satisfying programmable conditions are saved. Referring to Fig. 2.9: the IND\_TRG\_LOGIC (Individual Trigger Logic) can combine (AND/OR/MAJ) the trigger request (TRG\_REQ) from each self-trigger. When the logic condition is met, a trigger validation (TRG\_VAL) is sent back to each channel individually to enable the acquisition of that event. Events not receiving a TRG\_VAL signal are discarded. This technique allows to make coincidence and anti-coincidence requests among different channels (refer to [RD6] for further details);
3. the board can accept an external trigger on the TRG IN connector. The external trigger can be used in OR logic operation with the channel self-trigger, or it can be used as a VETO to inhibit the individual self-trigger. If the self-trigger is disabled, the acquisition is managed by the external trigger only;

4. individual trigger and logic combination of self-trigger of different channels (AND/OR/MAJ) can be propagated through the TRG-OUT connector.



**Fig. 2.9:** Diagram showing the structure of the trigger management of the DPP-PSD firmware.

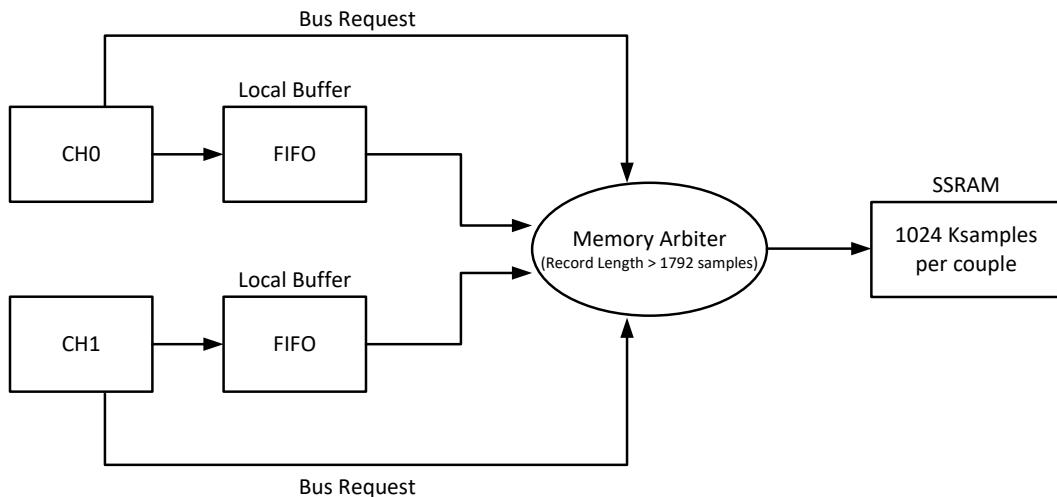
In case of 725 and 730 series, each channel can manage the self-trigger independently but it shares the same memory buffer with the other channel of the couple (0-1, 2-3, etc.) (see Fig. 2.10). The user must take care in case he/she wants to acquire large waveform length. Indeed the DPP-PSD algorithm is meant to acquire small size events, typically time stamps and charges, and possibly small portions of the waveform for post-processing. In case of **record length less than 1792 samples**, each channel has enough memory in its local buffer to acquire events independently from the other channel. For record length greater than 1792 samples, the couple must use an external SRAM memory, and a memory arbiter decides in “fair mode” which event of the two channels is saved.



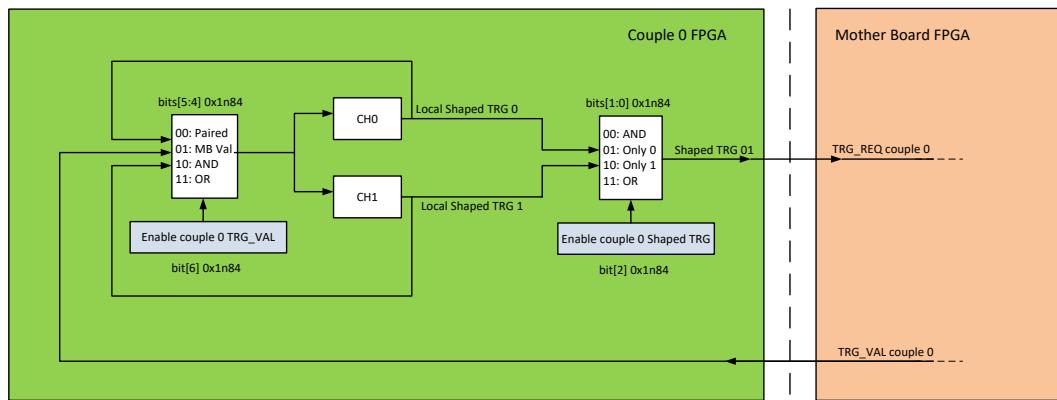
**Note:** In case of List mode, the Record Length is ignored.

Moreover the channels of the couple share the same TRG\_REQ for the coincidence logic. This means that it is not possible to set different coincidence logic among channels of two different couples (refer to [RD6] for further details). Anyway a great advantage comes in case of coincidences between channels of the same couple, which can be managed inside the channel FPGA, with no propagation to the mother board.

The TRG\_REQ from couple and the TRG\_VAL to the couple are managed by bits[6:0] of register 0x1n84, according to the bit scheme reported in Fig. 2.11.



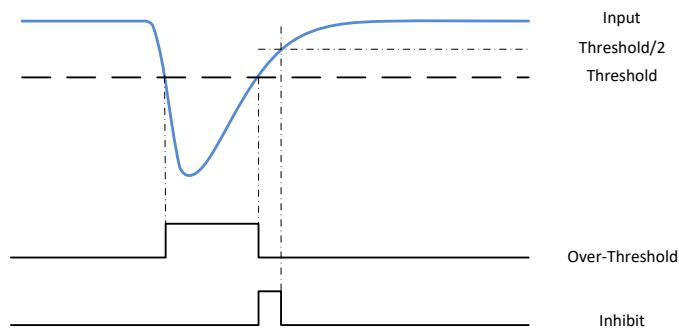
**Fig. 2.10:** Memory management of 725 and 730 series.



**Fig. 2.11:** Local Trigger Management inside couple 0 of 725-730 digitizer series. Couple 0 is made of channel 0 and channel 1. The same applies for the other couples of the 725 and 730.

### Trigger Hysteresis (725 and 730 series only)

When the input signal is no more over-threshold, the trigger could fire again in the tail of the pulse, especially in case the tail contains spikes or noise. The “Trigger Hysteresis” feature inhibits any trigger until the input pulse reaches half of the threshold value itself. See Fig. 2.12 for a diagram of this feature. This option is enabled by default. To modify this value use a FreeWrites command (refer to Sec. **The Acquisition Tab**) writing at 0x1n80 [RD4].

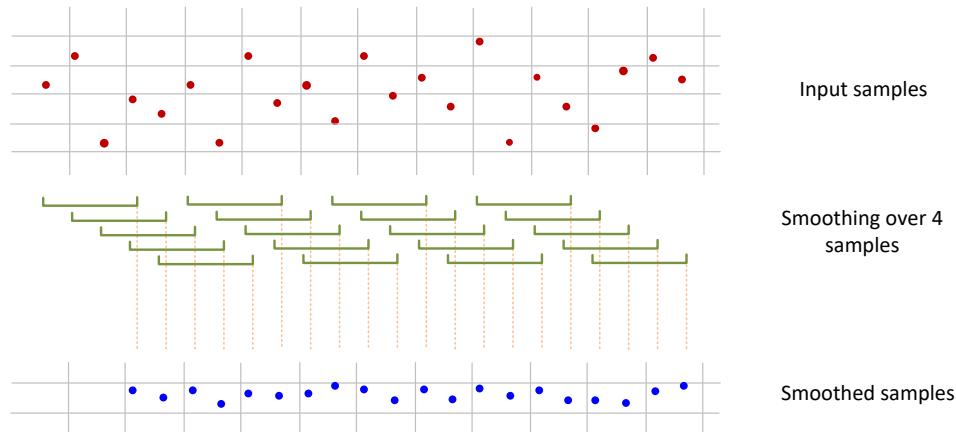


**Fig. 2.12:** Trigger Hysteresis in DPP-PSD firmware. Any other triggers are inhibited after the over-threshold until the input reaches the value of half the threshold.

### Input Smoothing (725 and 730 series only)

The smoothing is a moving average filter, where the input samples are replaced by the mean value of the previous n samples, where n is: 2, 4, 8 and 16 samples.

When enabled, the trigger is applied on the smoothed samples, thus reducing triggering on noise. Both CFD and LED triggering modes can be used on the smoothed input. The charge integration is either performed on the input samples or on the smoothed samples, according to bit [11] of register 0x1n80 [**RD4**].



**Fig. 2.13:** Example of smoothing over four samples. The input samples are averaged over four samples and replaced in the smoothed samples by the mean value.

### Veto (725 and 730 series only)



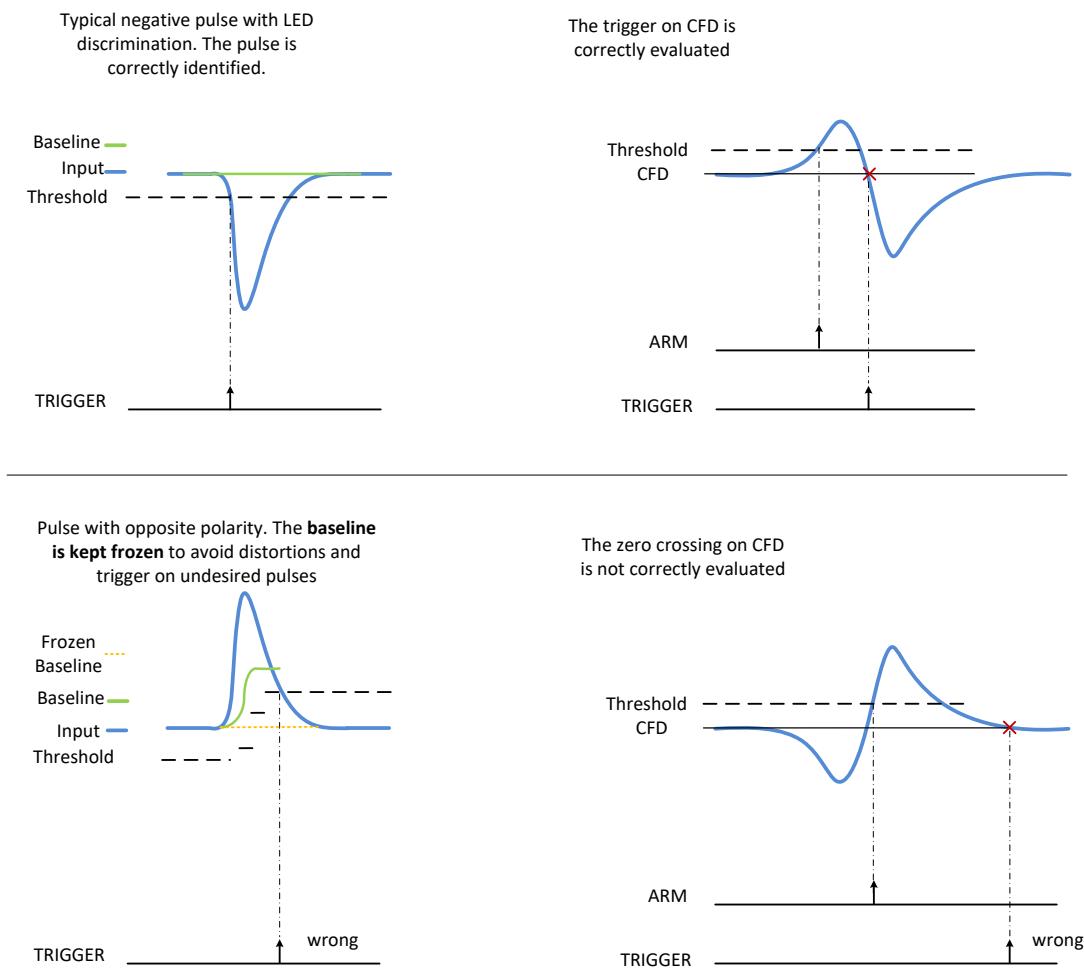
**Note:** Veto options can be enabled via register writes using the FreeWrites options (refer to Sec. **The Acquisition Tab**).



**Note:** In case of 720 and 751 series the veto is managed by the Global Trigger Mask register (0x810C) and Trigger Validation Mask (0x8180 + 4n).

In case of 725 and 730 series the user can set a different coincidence logic between channels inside the couple and extra couples. For example, it is possible to set the AND between the channels inside the couple, and set a veto from external trigger for all couples (see [**RD6**] for additional examples). The other digitizer series can handle just one type of coincidence logic and do not have the veto management of 725 and 730 series.

In particular, while the coincidence inside the couple is managed by bits[6:0] of register 0x1n84 (see Fig. 2.11), bits[19:18] of the same register [RD4] manage the veto source, which can be common among all channels (set it through register 0x810C, and it can be generated by an external trigger or by a combination of the trigger requests from couples), or individually set for the couples of channels (each couple can have a different veto, which can be set through register 0x8180 (+4n), where n is the couple index, and it can be generated by an external trigger or by a combination of the trigger requests from couples). Finally a veto can come from events saturating inside the gate (clipping) or from events with opposite polarity, as for example, in case of undershoot/overshoot, the signal can trigger on noise while it returns to zero. The firmware automatically detects pulses with opposite polarity and in case of LED discrimination freezes the baseline. This avoid distortions in the baseline and triggering of wrong pulses (see bottom left of Fig. 2.14). In case of CFD discrimination, since the CFD is a bipolar signal, there is a zero crossing even for opposite polarity (see bottom right of Fig. 2.14). Triggers on opposite polarity are inhibited by default; set bit[31] = 1 of register 0x1n80 to disable this option



**Fig. 2.14:** Example of input of opposite polarity. Top left and top right pictures shows the case of a negative pulse polarity, where the trigger is correctly evaluated both for LED and CFD discrimination. Bottom left picture shows an opposite pulse polarity (positive) and the corresponding CFD (right). To avoid distortions on the baseline (green line) the baseline is kept frozen (yellow) and the event is not triggered. Also the CFD is not inhibited by default.

The user can set the width of the veto duration through register 0x1nD4. In particular bits[15:0] define the width, and bits[17:16] define the step, that can be chosen among 8 ns, 2 us, 524 us, and 134 ms.



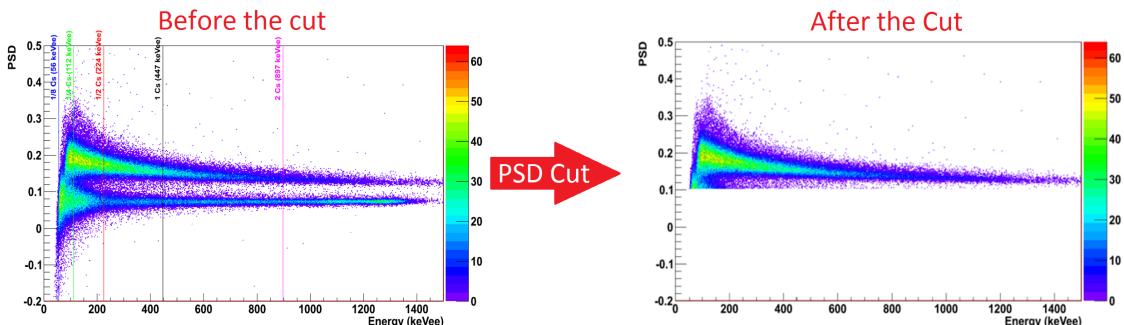
**Note:** A veto width equal to 0 means that the veto lasts for the duration of the signal that generated it. A veto width different from 0 extends the veto duration by the amount of time written in the register.

## Online PSD Selection

The PSD value as defined in Sec. **Principle of Operation** can be used to online select the events. Indeed, it is possible to select events under or below a programmable PSD threshold. Referring to the example of neutron/gamma discrimination shown in Fig. 2.15, the cut on PSD allows the user to reject most of the gamma events, thus recording only neutrons and the small amount of gamma overlapping with the neutrons.

The user has two possible ways to perform the online PSD selection:

1. Setting a PSD Cut on CoMPASS through **The Rejection Tab** or directly in the PSD plot (see Sec. **The Plotter Window**). In this case the cut will be applied at a software level and will not affect the data throughput from the digitizer.
2. Set the FPGA registers 0x1n78 and 0x1n80 (**[RD7]**, **[RD4]**, **[RD5]**) using the FreeWrites commands (refer to Sec. **The Acquisition Tab**). In this case the data throughput after the cut can be significantly reduced.



**Fig. 2.15:** 2D scatter plot of PSD parameter vs Energy in a neutron-gamma application. On the left the 2D plot before the cut, on the right the plot after the cut on PSD.

## Zero Suppression Based on Charge (725 and 730 series)

Input signals of small amplitude can be selected by setting a small threshold level. Unfortunately, this might result in an increase of the noise level. The noise can be distinguished by real signals in the energy spectrum, since it usually appears as a peak close to the 0 energy. Register Charge Zero Suppression Threshold 0x1n44 allows the user to set a threshold in the spectrum ( $Q_{thr}$ ) to cut events with charge  $Q_{long} < Q_{thr}$ . This option can be enabled by setting bit[25] of register 0x1n80.  $Q_{thr}$  is expressed as a 16 bit number, where 1 LSB corresponds to a specific value of charge which depends on the *Energy Coarse Gain* factor (refer to **The Energy Calibration Tab**).

## Pile-Up Management

The DPP-PSD firmware is mainly designed to work with fast signals like those coming from scintillation detectors coupled with Photomultiplier Tubes. The relevant output signals do not show long decay tails as in the case of charge sensitive preamplifiers, and the probability of pile-up between two pulses is quite low. In particular, the case of a second pulse sitting on the exponential tail of the previous one is rather rare. However, with the PSD algorithm, it is important to separate fast and slow components of the light emitted by the scintillation detector. Typically, the fast component is a quick pulse (few tens of ns) while the slow component is a quite long tail (typically a few  $\mu$ s) having amplitude much smaller than the fast component (see **[RD8]**). To get the best results in the pulse shape discrimination, it is necessary to set the “Long Gate” as long as the full duration of the slow component. Under this conditions, most likely the events in pile-up occur during the long gate and cause an error in the calculation of the charge of the slow component. For this reason, it is important to detect these cases, especially high rate PSD acquisitions.

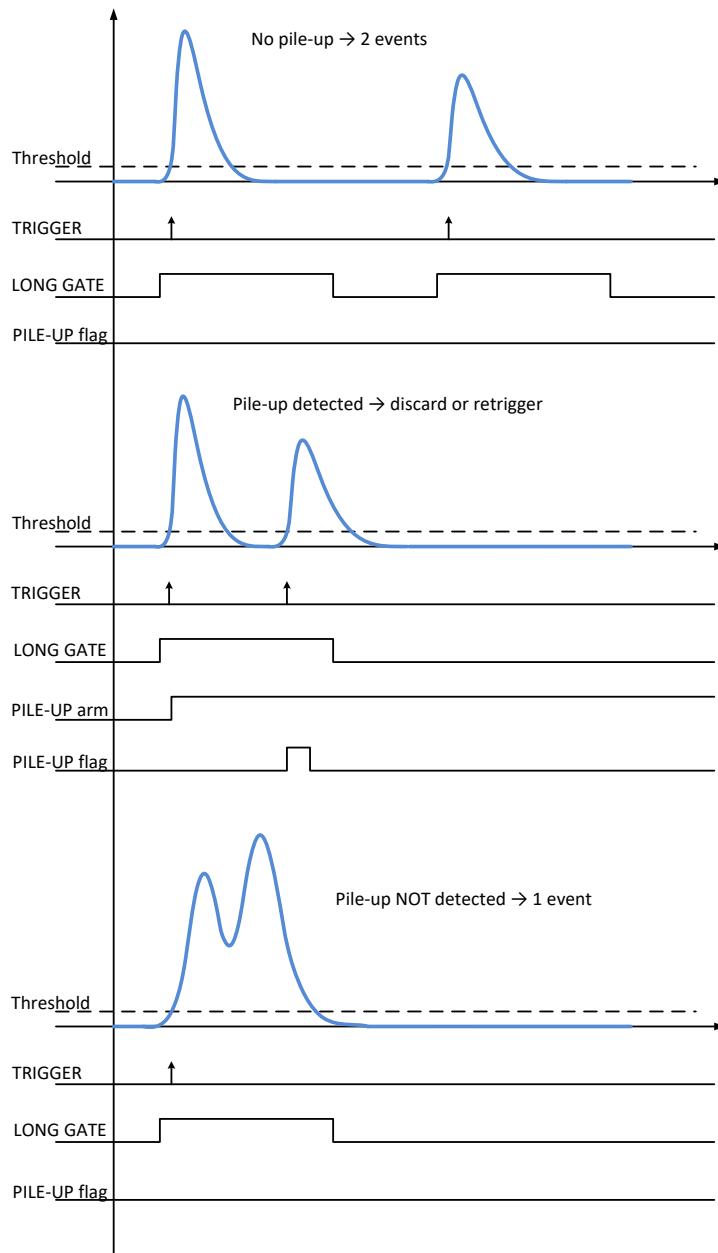
## Pile-up management (751 family)

In the DPP-PSD firmware (751 family only) two events are considered in pile-up only when they both cross the threshold within the same integration gate. When the first signal triggers, the short and long gates are opened for integration. If another event crosses the threshold within the long gate, they are flagged as pile-up. If the second event does not cross the threshold, then the pile-up condition is not detected. Referring to Fig. 2.16, from top to bottom there are three possible cases:

1. two distinct events do not overlap into the same integration gate. This is the case when no pile-up occurred;
2. two events trigger into the same gate. The pile-up flag is high and three possible scenarios are available:
  - no action is taken and the two pulses are integrated into the same integration gate;
  - the event is discarded and no charge is evaluated and saved;
  - a second gate is opened for the second pulse.

See next section for further details;

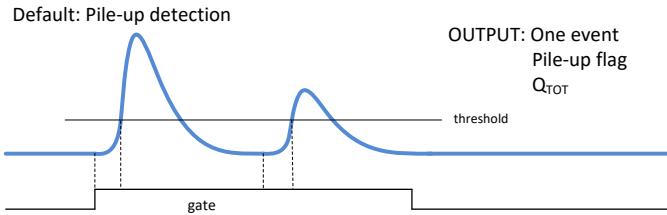
3. two pulses overlap into the same gate, and the second pulse does not overcome the threshold. The event is not recognized as pile-up.



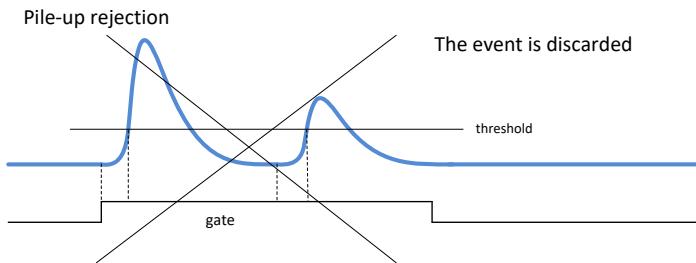
**Fig. 2.16:** From top to bottom: (1) two distinct events do not overlap into the same integration gate. This is the case when no pile-up occurred. (2) Two events trigger into the same gate. The pile-up flag is high and three possible scenarios are available: (a) no action is taken and the two pulses are integrated into the integration gate; (b) the event is discarded and no event is saved; (c) a second gate is opened for the second pulse (see next section for further details). (3) Two pulses overlap into the same gate, but the second pulse does not overcome the threshold. The event is not recognized as pile-up.

In the DPP-PSD firmware there are three options for the pile-up management:

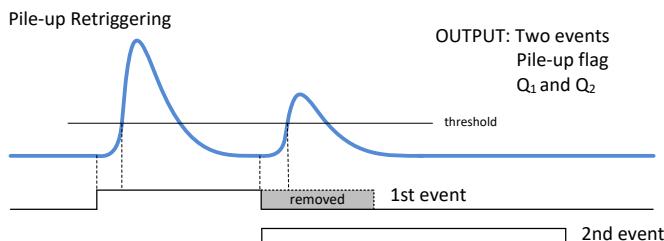
1. **Default:** in the default configuration the algorithm detects pile-up events, evaluates the total charge of the two pulses – which is therefore considered as a single “event”, and flags that event as “pile-up”.



2. **Pile-up rejection:** this configuration is enabled by setting bit [26] = 1 of register 0x1n80 (where n is the channel number) through a FreeWrites command (refer to Sec. bf The Acquisition Tab). In this way the events are rejected at board level, thus reducing the throughput rate. If the user wants to acquire them and discard at software level it is possible to enable the option **PUR** enable of **The Rejection Tab**.



3. **Pile-up Retriggering:** this configuration is enabled by setting bit [25] = 1 of register 0x1n80 (where n is the channel number) through a FreeWrites command (refer to Sec. bf The Acquisition Tab). In this case, when another pulse arrives within the long gate (and after the end of the short gate), the charge integration is stopped prematurely. A new event is created, by opening short and long gate again. The charge in the first event is the result of the integration of the signal up to the start of the new gate; because of the truncation of the gate (see figure below), it is not guaranteed that the full charge (i.e. energy) of the first pulse is completely integrated in the first gate. The second gate will integrate the charge of the second pulse, including the pre-gate region; it is worth noticing that the second gate can integrate also part of the charge belonging to the first gate. The user can apply some corrections to the charge of the two events based on the two time stamps, that give information about the separation between pulses. Both events are tagged as “pile-up”.

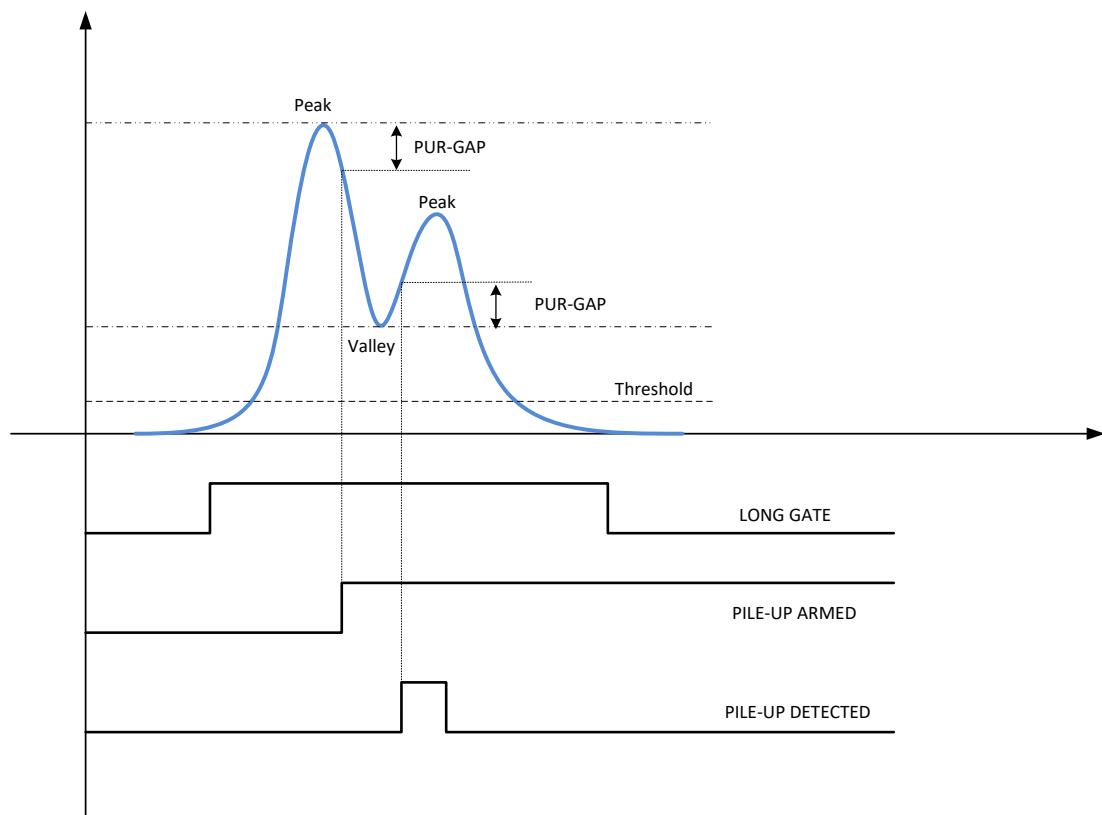


### Pile-up management (720, 725, and 730 series)

In the DPP-PSD firmware of 720, 725 and 730 families, two events are considered in pile-up when there is a situation of peak-valley-peak inside the same gate, where the gap between the valley and the peak is a programmable value. Referring to Fig. 2.17, when the peak value is reached the algorithm evaluates the point corresponding to the PUR-GAP value and gets ready to detect a pile-up event (PILE-UP ARMED). If there is a condition of “valley”, and the input signal overcomes the PUR-GAP threshold, then the event is tagged as pile-up. In the default configuration the firmware does not take any action and the total charge of the event is evaluated within the gate and saved into memory.



**Note:** CoMPASS allows the user to enable the pile-up rejection and to set the PUR gap value. Refer to **The Rejection Tab** section for more details.



**Fig. 2.17:** Pile-up definition for 720, 725, and 730 series.

## Supported Models

The following table lists the digitizer models supported by CoMPASS and able to run the DPP-PSD firmware:

Desktop Digitizer	Description
DT5720B	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
DT5720C	2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
DT5720D	4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
DT5720E	2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
DT5725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725B	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730B	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5751	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
NIM Digitizer	Description
N6720B	4 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
N6720C	2 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
N6720D	4 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
N6720E	2 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
N6725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6751	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
N6751C	2/4 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8 MS/ch, EP3C16, SE
Desktop Digitizer	Description
V1720E	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
V1720F(*)	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, DIFF
V1720G	8 Ch. 12 bit 250 MS/s Digitizer: 10MS/ch, C20, SE
V1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
V1751B(*)	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, DIFF
V1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8MS/ch, EP3C16, SE
VX1720E	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, SE
VX1720F(*)	8 Ch. 12 bit 250 MS/s Digitizer: 1.25MS/ch, C20, DIFF
VX1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
VX1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1751	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, SE
VX1751B(*)	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 1.8/3.6MS/ch, EP3C16, DIFF

VX1751C	4/8 Ch. 10 bit 2/1 GS/s Digitizer: 14.4/28.8MS/ch, EP3C16, SE
<b>DPP-PSD Firmware</b>	<b>Description</b>
DPP-PSD (8ch x720)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x720)
DPP-PSD (4/2ch x720)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (4/2ch x720)
DPP-PSD (16ch x725)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (16ch x725)
DPP-PSD (8ch x725)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x725)
DPP-SUP 16ch x725	DPP-SUP - Super Licence for 16ch x725 Digital Pulse Processing
DPP-SUP 8ch x725	DPP-SUP - Super Licence for 8ch x725 Digital Pulse Processing
DPP-PSD (16ch x730)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (16ch x730)
DPP-PSD (8ch x730)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x730)
DPP-SUP (16ch x730)	DPP-SUP - Super Licence for 16ch x730 Digital Pulse Processing
DPP-SUP (8ch x730)	DPP-SUP - Super Licence for 8ch x730 Digital Pulse Processing
DPP-PSD (8ch x751)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (8ch x751)
DPP-PSD (4ch x751)	DPP-PSD - Digital Pulse Processing for Pulse Shape Discrimination (4ch x751)

(\*) The board is currently obsolete.

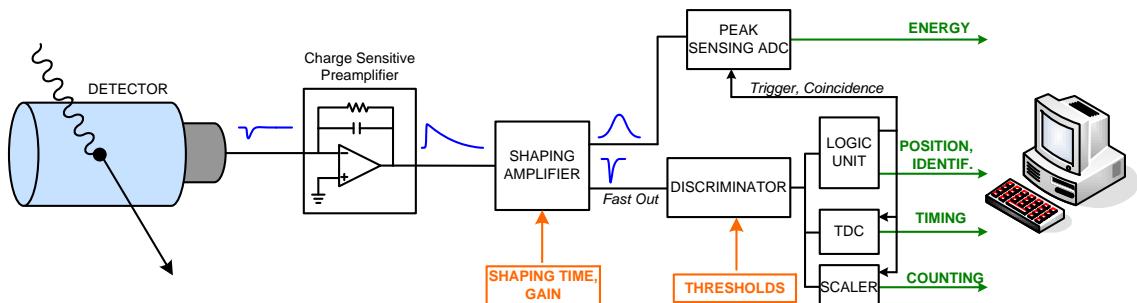
**Tab. 2.1:** CoMPASS supported boards with DPP-PSD firmware.

## 3 Pulse Height Analysis and Digital MCA: the DPP-PHA Firmware

The aim of this DPP-PHA firmware is to implement a digital version of the analog chain made by Shaping Amplifier + Peak Sensing ADC (Multi Channel Analyzer). CoMPASS supports the following digitizers running the DPP-PHA firmware: Mod. **x724** (14 bit, 100MS/s), Mod. **x725** (14 bit, 250 MS/s), Mod. **x730** (14 bit 500 MS/s) and the Digital MCA Mod. **DT5781**. It is mainly used for high resolution spectroscopy (Germanium and Silicon detectors) but it is also well suited for inorganic scintillators like NaI or CsI. The output of the charge sensitive preamplifier or of the photomultiplier is directly connected to the input of the digitizer/MCA with **no use of the Shaping Amplifier**.

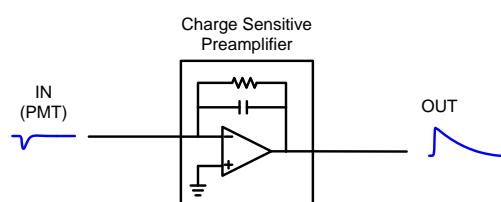
### Traditional Analog Approach

The traditional analog chain for signal readout from nuclear radiation detector usually makes use of almost all-analog chains, where the electronics rely upon three fundamental devices: the Charge Sensitive Preamplifier, the Shaping Amplifier and the Peak Sensing ADC (refer to Fig. 3.1).



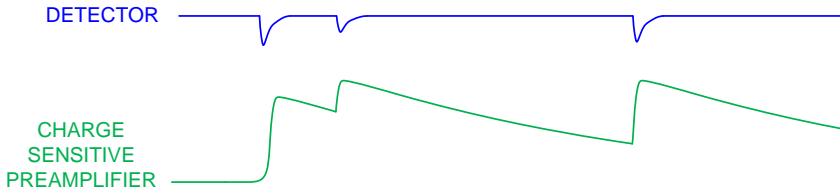
**Fig. 3.1:** Nuclear Radiation Detector (with Charge Sensitive Preamplifier) Analog Chain Block Diagram.

The Charge Sensitive Preamplifier (Fig. 3.2) integrates the signal coming from the detector, as the HPGe, thus converting the collected charge into a voltage step. The integrating capacitor is put in parallel with a discharging resistor, so that the preamplifier output will have pulses with a fast rise time and a long exponential tail with decay time  $\tau$ . The charge information (proportional to the energy released by the particle in the detector) is therefore represented by the pulse height. The charge-amplitude proportionality is set by the capacitor value  $V_{OUT} = \frac{Q}{C}$  and the decay time of the output signal is  $\tau = RC$ .



**Fig. 3.2:** Simplified schematic of a RC-type Charge Sensitive Preamplifier.

To have a good charge-amplitude conversion and to minimize the noise, the decay time  $\tau$  is much larger than the width of the detector signal, typically 50-100  $\mu$ s, and for this reason pile-up of different particle detections can arise (Fig. 3.3).

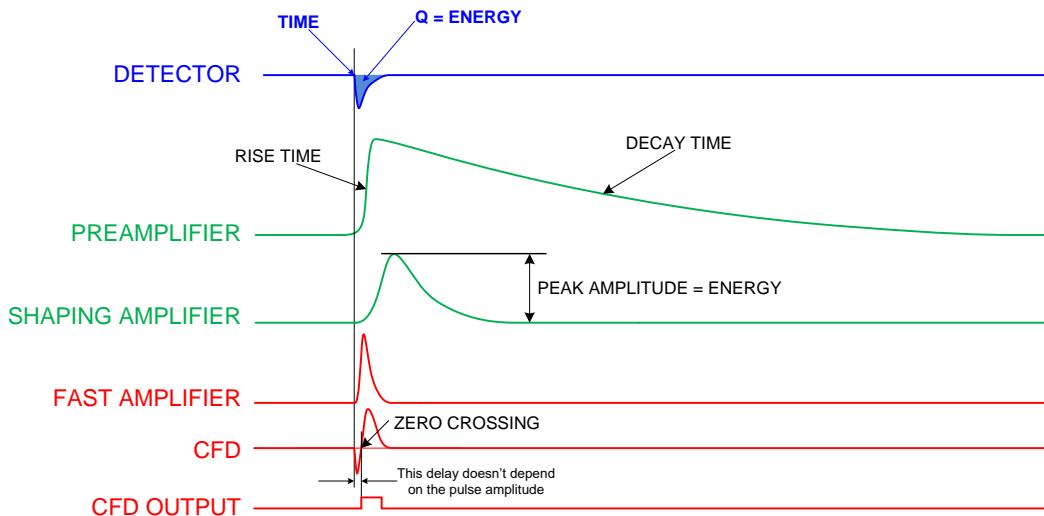


**Fig. 3.3:** Pile-up of detector signals due to the large decay time of the Preamplifier output.

Another drawback when using a Charge Sensitive Preamplifier is when the peak is too sharp for the Peak Sensing ADC to be detected with the required precision.

To avoid these problems the pre-amplified signal is usually feed into a Shaping Amplifier, that provides out a quasi-Gaussian output whose height is still proportional to the energy released by the detected particle. Finally, the signal from the Shaping Amplifier is fed into a Peak Sensing ADC, which is able to evaluate and digitize the height of the pulses, and filling a histogram with these values, which corresponds to the energy spectrum.

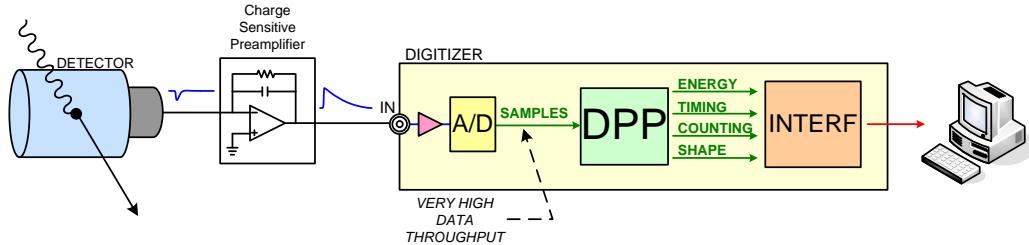
To preserve the timing information, the fast component of the signal (rising edge) is usually treated by a Fast Amplifier (or Timing Amplifier) that derives the signal; the output of the fast amplifier usually feeds a chain made of a Discriminator (CFD), a TDC and/or a Scaler for the timing/counting acquisition. Further modules can be present to implement logic units, to make coincidences (giving the position and the trajectory of the particles), to generate triggers or to give information about the pulse shape (time over threshold, zero crossing, etc.) for the particles identification. Usually the Fast Amplifier is included into the Shaping Amplifier module and the relevant signal is provided as a separate fast output (or timing output). The typical signal shapes from the analog chain is shown in Fig. 3.4.



**Fig. 3.4:** Signals in the traditional analog chain.

## CAEN Digital Approach

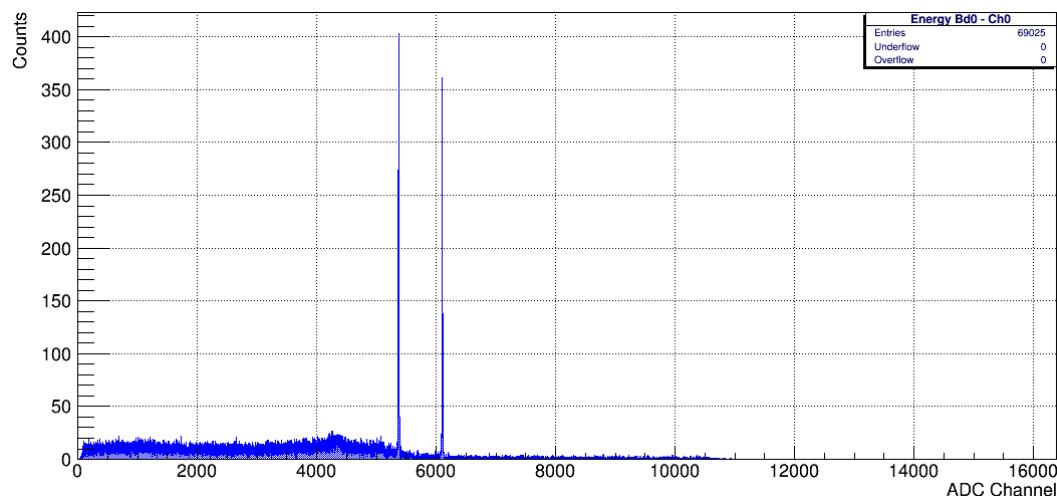
In the CAEN digital approach all blocks from the shaping amplifier to the PC are synthesized into a single device, the digitizer (see Fig. 3.5).



**Fig. 3.5:** Block Diagram of a Digitizer-based Spectroscopy System.

The new FPGA based techniques allow the user to change the readout parameters according to the detector characteristics, thus enabling the measurement of different radiations with different detectors using the same hardware. The digitizer becomes itself a Digital Multi Channel Analyzer (MCA).

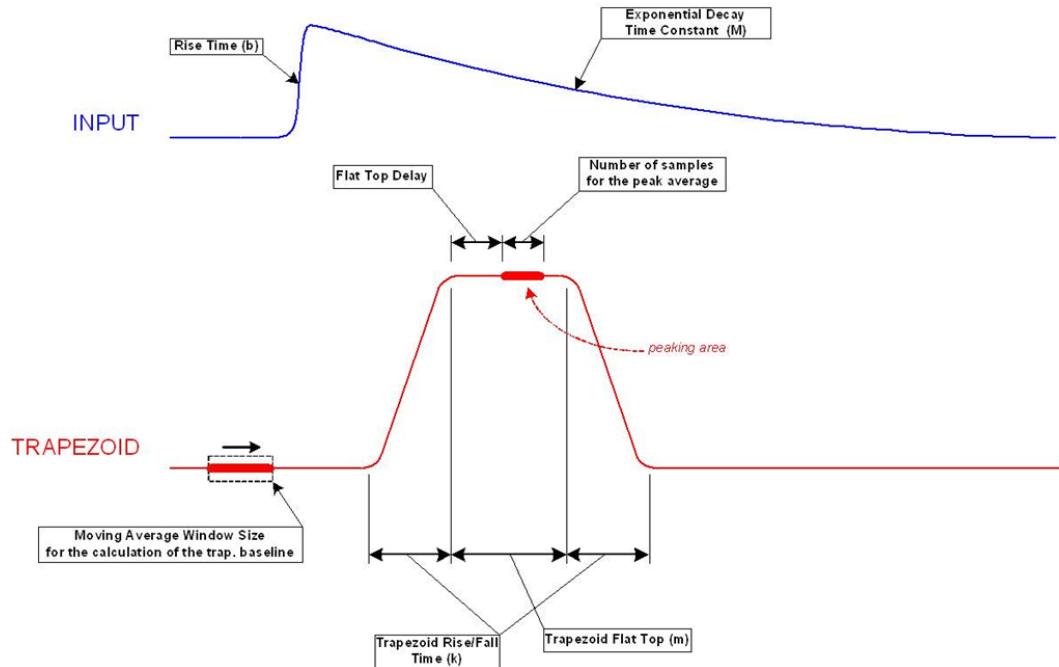
In the technique called Multi Channel Analysis the energy spectrum histogram X-axis can be segmented in “bins” or “Channels”, each one representing a pulse height value, in V (or, if calibrated, the corresponding radiation Energy in keV). The maximum number of available “bins” or “channels” is dictated by the resolution of the ADC. A 14-bit (1:16384) ADC resolution allows a 16 K “Channels” Spectrum to be generated. The spectrum resolution should be matched with the detector Energy resolution for optimal results (i.e. a 1K Channels Spectrum is good enough of basic gamma spectroscopy with NaI detectors while at least an 8K Channels Spectrum is needed to appreciate the intrinsic Energy resolution of HPGe Detectors). The histogram Y-axis values indicate the number of counts accumulated during the measuring time in the corresponding x-axis “bin” or “Channel”.



**Fig. 3.6:**  $^{60}\text{Co}$  energy spectrum from HPGe detector.

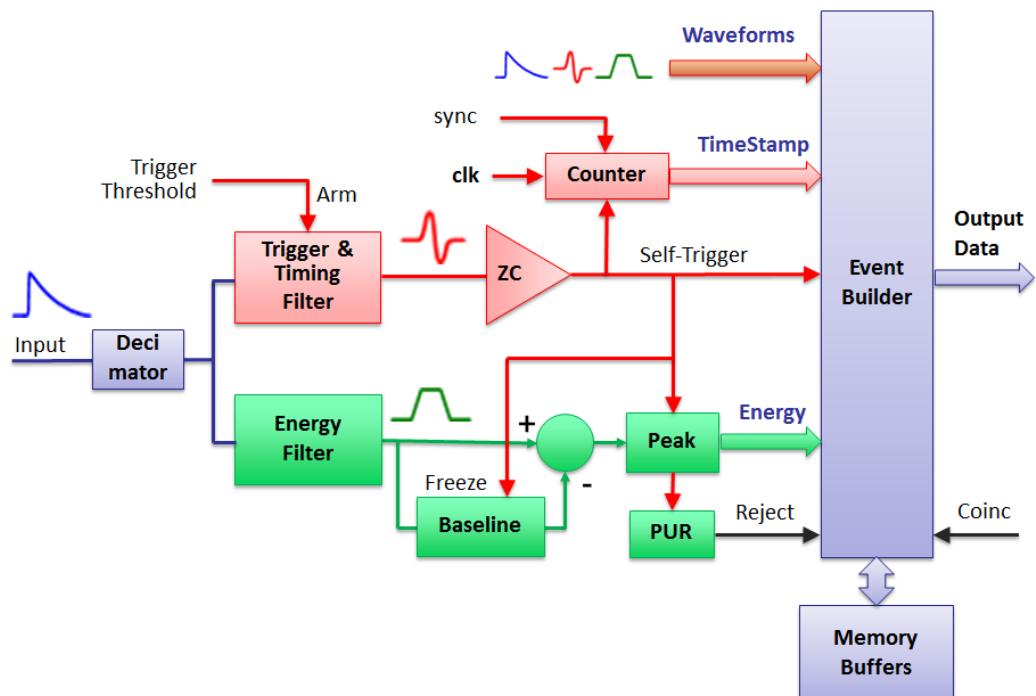
The algorithm implemented in the digitizer FPGA is based on the Jordanov trapezoidal filter [RD9] and it is called **DPP-PHA** (**Digital Pulse Processing for Pulse Height Analysis**). The trapezoidal filter is a filter able to transform the typical exponential decay signal generated by a charge sensitive preamplifier into a trapezoid whose flat top height is proportional to the amplitude of the input pulse (that is to the energy released by the particle in the detector) (see Fig. 3.7). The trapezoid plays almost the same role of the shaping amplifier in a traditional analog acquisition system. There is an analogy between the two systems: both have a “shaping time” constant and must be calibrated for the pole-zero cancellation. For both, a

long shaping time gives a better resolution but has higher probability of pile-up. Both are AC coupled with respect to the output of the preamplifier whose baseline is hence removed, but both have their own output DC offset and this constitutes another baseline for the peak detection.



**Fig. 3.7:** Pulse Height Analysis with Trapezoid Method.

The block diagram of the processing chain inside the digitizer FPGA is shown in Fig. 3.8.



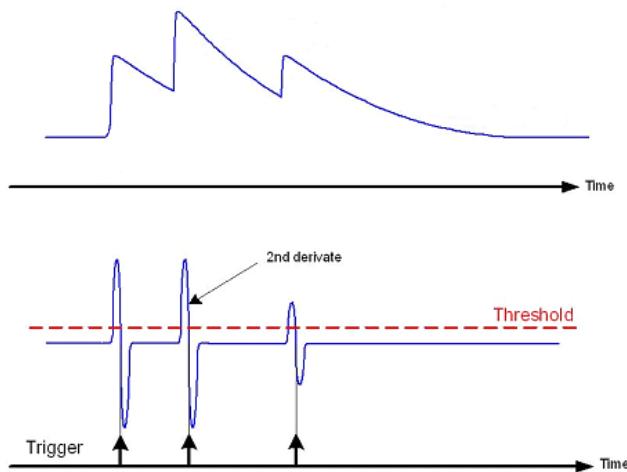
**Fig. 3.8:** Block Diagram of the DPP-PHA firmware.

## Decimator

The first block after the polarity selector is the decimator filter, which can be used in the case the signal is particularly slow, hence it is necessary to set values for the DPP time parameters that are not within the allowed range. The effect of the decimator is to scale down the sampling frequency of a factor 2, 4 or 8; it might have also benefits in terms of noise, since it averages a certain number of samples to make a new sample for the data stream. The decimation applies to the energy filter only (i.e. to Decay Time (Pole-Zero Compensation), Trap. Rise Time, and Trap. Flat Top). Timing filter (RC-CR<sup>2</sup>), Baseline, Trigger Hold-Off, and Record Length are not affected.

## Trigger and Timing Filter

After the decimator, there are two parallel branches: one for timing and triggering, the other one for the energy. The aim of the Trigger and Timing Filter (TTF) is to identify the input pulses, generate a digital signal called trigger that identifies the pulse, and calculate the time of occurrence of the event (trigger time stamp). The TTF performs a digital RC-CR<sup>2</sup> filter, whose zero crossing corresponds to the trigger time stamp. In analogy with a CFD – Constant Fraction Discrimination – the RC-CR<sup>2</sup> signal is bipolar and its zero crossing is independent of the pulse amplitude. The integrative component of the RC-CR<sup>2</sup> is a smoothing filter based on a moving average filter that reduces the high frequency noise and prevents the trigger logic to generate false triggers on spikes or fast fluctuation of the signals. The derivative component allows to subtract the baseline, so that the trigger threshold is not affected by the low frequency fluctuation. Moreover the pile up effect is significantly reduced (see Sec. **Pile-up Rejection**).



**Fig. 3.9:** The Trigger and Timing Filter allows to detect pulses on the zero-crossing of the RC-CR<sup>2</sup> signal, which corresponds to a 2<sup>nd</sup> derivative of the input pulse. The derivative component of the RC-CR<sup>2</sup> subtracts the baseline and makes easier to perform a zero-crossing calculation.

The trigger logic gets armed at the **Threshold** crossing, then it generates the trigger signal at the RC-CR<sup>2</sup> zero crossing. Setting the threshold value corresponds to set the LLD (lower level discrimination) of the energy spectrum. The user can check from the histogram which value corresponds to the set threshold level. Refer to Sect. How to set the Trigger for further details on how to set the threshold. Another important parameter for the trigger logic is the **RC-CR<sup>2</sup>** smoothing, corresponding to the number of samples used for the RC-CR<sup>2</sup> signal formation. Increasing this parameter may help in reducing high frequency noise, but have the drawback to make the signal slower and smaller, due to the smoothing. Finally the **Input Rise Time** is the time the RC-CR<sup>2</sup> reaches its maximum value. This value should correspond to the input rise time, in such a way the RC-CR<sup>2</sup> peak value corresponds to the height of the input signal. Examples on how to proper set the trigger and timing filter can be found in [RD10].

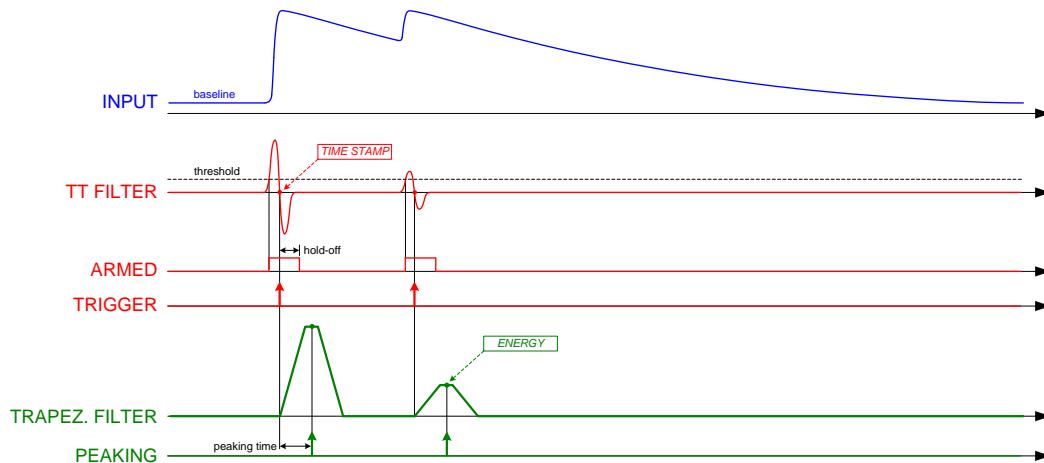
## Trapezoidal Filter (Energy Filter)

As in the traditional analog chain, the Shaping Amplifier is able to convert the exponential shape from the Charge Sensitive Preamplifier into a Gaussian shape whose height is proportional to the pulse energy, in the same way the Trapezoidal filter is able to transform it into a trapezoidal signal whose amplitude is proportional to the input pulse height (energy). In this analogy, the **Trapezoid Rise Time** corresponds to the Shaping Time times a factor of 2/2.5. Therefore for an analog shaping of 3us the user can set a trapezoid rise time of 7-8 us (see also [RD10]).

In case of high rate signal the trapezoid rise time value should be reduced in order to avoid pile-up effects (see Sec. **Pile-up Rejection**), choosing a compromise between high resolution (high value of trapezoid rise time) and pile-up rejection (and corresponding dead time).

The energy value of the input pulse is evaluated as the height of the trapezoid in its **Flat Top** region. The user must take care that the flat top is really flat and that the **Peaking** (i.e. the samples used for the energy calculation) is in the flat region. Moreover the correct setting of flat top and peaking helps in the correct evaluation of the energy especially when large volume detectors are involved and the ballistic deficit may cause a significant error in the energy calculation. In this case it may be convenient to increase the flat top duration and delay the peaking time to wait for the full charge collection.

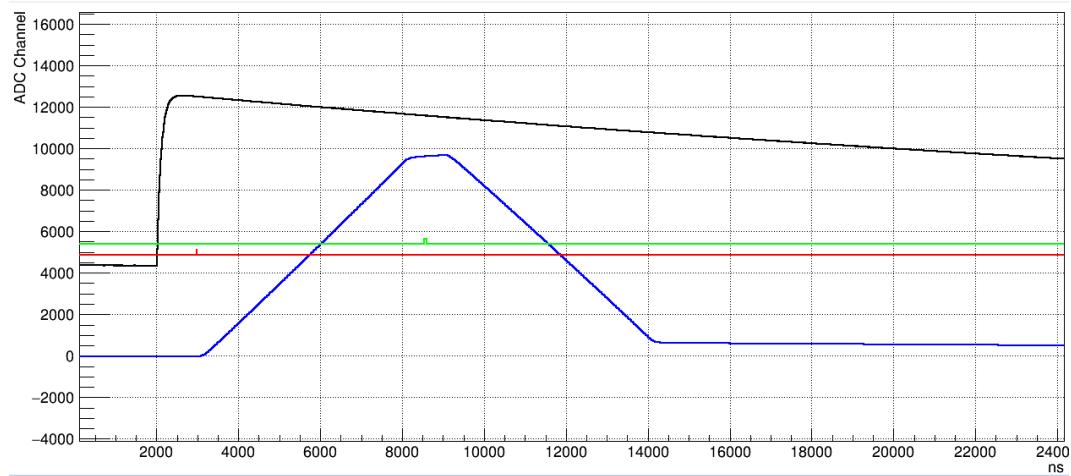
Fig. 3.10 summarizes the settings for both the Trigger and Timing Filter and for the Trapezoid Filter.



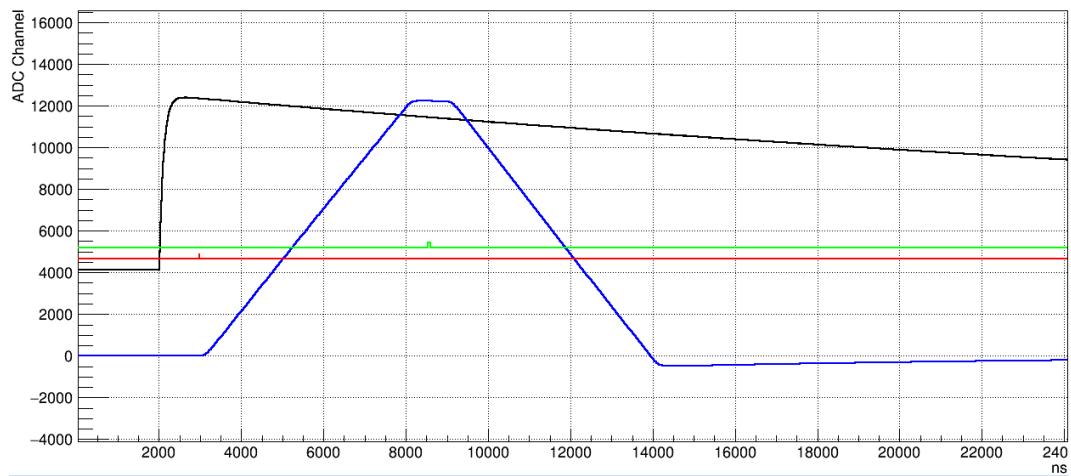
**Fig. 3.10:** Simplified signals scheme of the Trigger and Timing filter (red) and the Trapezoidal Filter (green). In blue the input pulses from Preamplifier.

## Pole-Zero Adjustment

Like the Gaussian pulse of the Shaping Amplifier, also the trapezoid requires an accurate pole-zero adjustment to guarantee the correct return to the baseline at the end of the falling edge. To correctly set the pole-zero the user must take care of setting the proper **Trapezoid Decay Time** value (which corresponds also to the Input Decay Time) to avoid either undershoot or overshoot effects (as can be seen in Fig. 3.11 and 3.12). Pole Zero Adjustment can reduce signal artifacts due to pulses pile up occurring when the counting rate is high compared to the pulse decay.



**Fig. 3.11:** Pole Zero effects of overshoot of the trapezoid (blue curve).



**Fig. 3.12:** Pole Zero effects of undershoot of the trapezoid (blue curve).

## Baseline Restoration

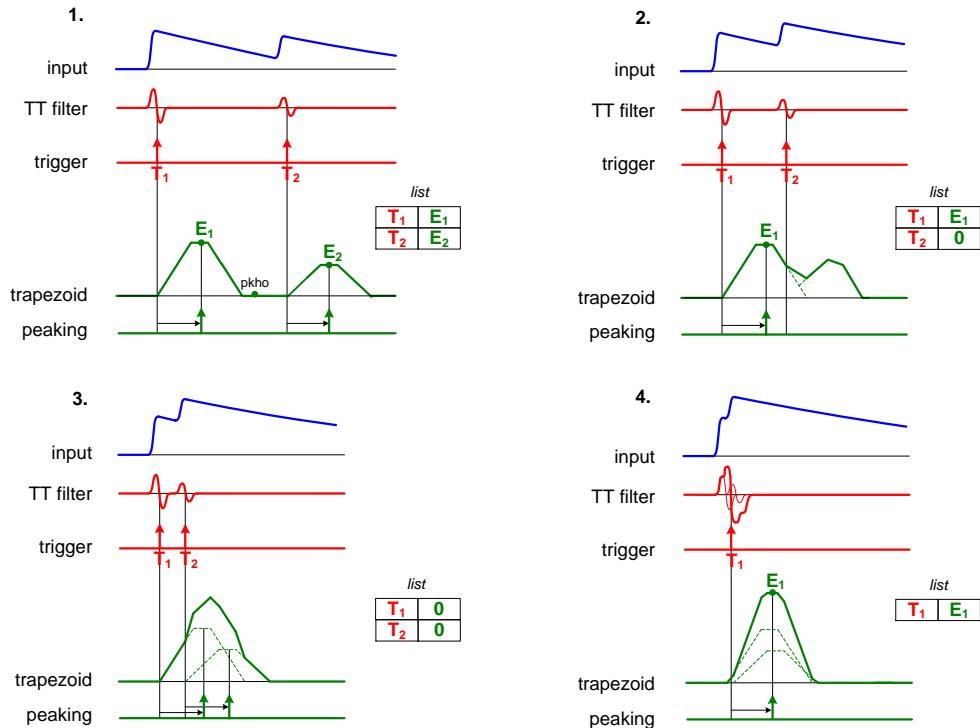
The energy filter includes also a baseline restorer that operates on the trapezoidal filter output and calculates the baseline by averaging a programmable number of points before the start of the trapezoid. The baseline is then frozen for the trapeze duration and used for the height calculation. Once the trapezoid is returned to the baseline, the averaging restarts to run. The pulse height (i.e. the trapezoid amplitude) is given as the distance between the flat top and the baseline taken in the programmed position; to further reduce the fluctuation of this distance due to the noise, it is possible to average a certain number of points in the flat top before subtracting the baseline. In case of high resolution measurements, it is strongly suggested to increase the number of **Baseline Mean** samples at the maximum allowed value. Furthermore the user can also set the **Baseline Hold-Off** value to freeze the baseline calculation beyond the trapezoid end, thus reducing the noise on the baseline calculation. In case of high rate those values must be reduced to avoid pile-up effects.

## Pile-up Rejection

If two events are separated by less than the trapezoid duration, then the relevant trapezoids overlap. The trapezoid duration pkrun is defined as  $pkrun = RT + FT + pkho$ , where RT is the trapezoid Rise Time, FT is the trapezoid Flat Top, and pkho is the Peak Hold-Off, which starts at the end of the Flat Top. There are four different cases (Fig. 3.13):

- $\Delta T > pkrun$ , the two events are well separated and none of them is flagged as pile-up.
- $RT + FT < T < pkho$ , the rising edge of the 2<sup>nd</sup> trapezoid overlaps on the pkho of the 1<sup>st</sup> one. In this case only the first event has a correct value of energy, while the second one is tagged as pile-up.
- $1.5 * IRT < \Delta T < RT + FT$ , where IRT is the Input Rise Time, which corresponds to the time the RC-CR<sup>2</sup> signal reaches its maximum value, and  $1.5 * IRT$  is the time the RC-CR<sup>2</sup> signal crosses the zero. The two events are both flagged as pile-up, since the two trapezoids overlaps.
- $\Delta T < 1.5 * IRT$ , the two pulses are too close and the trigger filter is unable to resolve the double pulse condition. In this case, the pile-up cannot be recognized and the two pulses are treated as a single pulse. The algorithm returns only one time stamp and one energy, whose value corresponds to about the sum of the two energies ('sum peak' in the spectrum).

Except for the case 3, the DPP-PHA algorithm is able to save into the memory buffer all the incoming events, including the piled-up pulses; the energy value is anyhow meaningless. During the readout of the event list, these events won't be accumulated into the histograms (that are calculated in the software), although they participate to the total count, thus giving an accurate estimation of the Input Count Rate. Furthermore, the energy spectrum can be corrected run-time by a statistical redistribution of the missed energies over the spectrum acquired within a specific time slot.



**Fig. 3.13:** The effect of trapezoid overlapping in the four main cases: 1. The two trapezoids are well separated (top left); 2. The second trapezoid starts on the falling edge of the first one (top right). 3. The second trapezoid starts on the rising edge of the first one (bottom left). 4. The two input pulses pile-up in the input rise time (bottom right).

## Dead Time

When a pulse is processed by an analog chain block, the maximum read-out rate is limited by the need to complete the processing of the current pulse before being able to process a successive valid signal. When the processing time of a pulse is larger than the time interval before the arrival of the next pulse, the analog chain is “temporarily blind” and misses one or more successive pulses. The actual live counting time is therefore smaller than the total counting time, and the difference between total time and live counting time is called “Dead time”. The Digital MCA read out capability is rather independent from the ADC sampling time and processing speed than from the signal width, and in general allows for higher counting rates than the analog chain. The digital MCA dead time is also an information on the relationship between total measurement time and live counting time values.

## Supported Models

The following table lists the digitizer models supported by CoMPASS and able to run the DPP-PHA firmware:

Board Model	Description
DT5724(*)	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
DT5724A(*)	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
DT5724B	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
DT5724C	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
DT5724D(*)	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
DT5724E(*)	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
DT5724F	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
DT5724G	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
DT5725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
DT5725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
DT5730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
DT5781	Quad Digital MCA
DT5781A	Dual Digital MCA
NIM Digitizer	Description
N6724(*)	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
N6724A(*)	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
N6724B	4 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
N6724C	2 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
N6724F	4 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
N6724G	2 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
N6725	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
N6725B	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6730	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
N6730B	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
N6781	Quad Digital MCA
N6781A	Dual Digital MCA
Desktop Digitizer	Description
V1724(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
V1724B(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
V1724C(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, DIFF
V1724D(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, DIFF
V1724E	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
V1724F(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, DIFF
V1724G	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C20, SE
V1725	16 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725B	16 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1725C	8 Ch. 14 bit 250 MS/s Digitizer: 640kS/ch, CE30, SE
V1725D	8 Ch. 14 bit 250 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
V1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
V1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1724(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, SE
VX1724B(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, SE
VX1724C(*)	8 Ch. 14 bit 100 MS/s Digitizer: 512kS/ch, C4, DIFF
VX1724D(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C4, DIFF

VX1724E	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, SE
VX1724F(*)	8 Ch. 14 bit 100 MS/s Digitizer: 4MS/ch, C20, DIFF
VX1730	16 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730B	16 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
VX1730C	8 Ch. 14 bit 500 MS/s Digitizer: 640kS/ch, CE30, SE
VX1730D	8 Ch. 14 bit 500 MS/s Digitizer: 5.12MS/ch, CE30, SE
DPP-PHA Firmware	Description
DPP-PHA (8ch x724)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x724)
DPP-PHA (4/2ch x724)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (4/2ch x724)
DPP-PHA (16ch x725)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis for (16ch x725)
DPP-PHA (8ch x725)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis for (8ch x725)
DPP-SUP 16ch x725	DPP-SUP - Super Licence for 16ch x725 Digital Pulse Processing
DPP-SUP 8ch x725	DPP-SUP - Super Licence for 8ch x725 Digital Pulse Processing
DPP-PHA (16ch x730)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (16ch x730)
DPP-PHA (8ch x730)	DPP-PHA - Digital Pulse Processing for Pulse Height Analysis (8ch x730)
DPP-SUP (16ch x730)	DPP-SUP - Super Licence for 16ch x730 Digital Pulse Processing
DPP-SUP (8ch x730)	DPP-SUP - Super Licence for 8ch x730 Digital Pulse Processing

(\*) The board is currently obsolete.

**Tab. 3.1:** CoMPASS supported CAEN boards for DPP-PHA firmware.

# 4 Software Interface

## Introduction

The CoMPASS software is an application that manages the communication and the data acquisition from digitizers where a DPP firmware is installed. The software automatically detects the connected boards despite the communication interface, allows the user to set the DPP settings, displays the waveforms and histograms, and saves the data as will be described in Sec. **GUI Description**.

## System Requirements

In order to be able to install CoMPASS, the host station needs Windows or Linux OS, and the third-party software **Java Runtime Environment 8 or later** (trademark of Oracle Inc., which can be downloaded from <http://www.java.com>).

In case of Linux OS please also check the following:

- `getconf LONG_BIT = 64`
- `ldd --version ≥ 2.17`
- `gcc -v ≥ 4.8.2`
- `java -version ≥ 8`

For additional details about the requirements and software installation refer to **[RD10]**

## Block Diagram

The CoMPASS software block diagram is depicted in Fig. 4.1. CoMPASS is composed by three main parts: the Graphic User Interface (GUI), the Server and the Plotter.

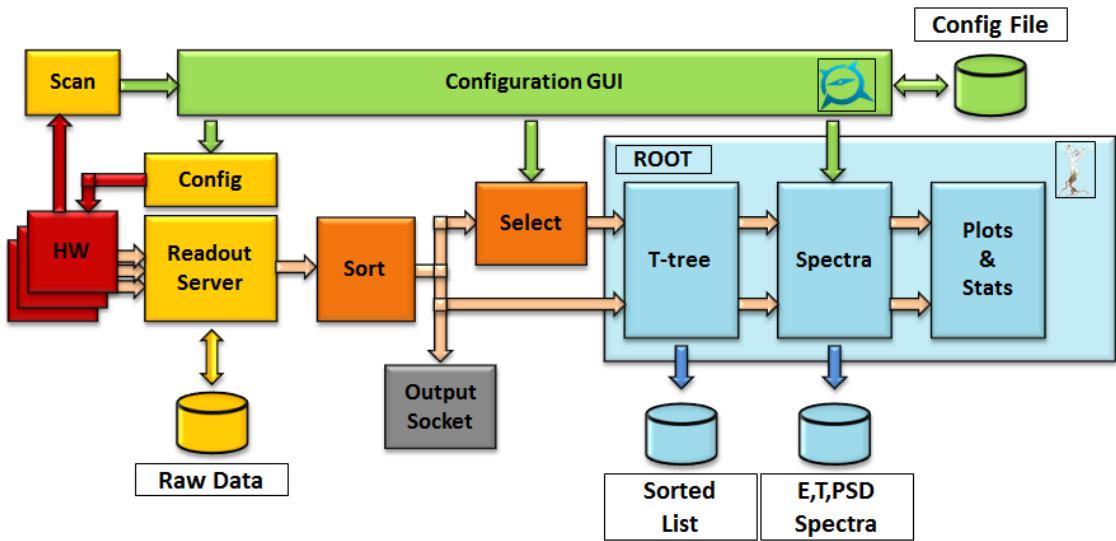
The GUI allows the user to easily scan and connect to the present hardware, set and optimize all acquisition parameters, to start/stop the acquisition, to set the spectra, to monitor the acquisition statistics and to save the data on the disk in several formats.

The server has the following mains functions:

- configures the digitizers according to the settings stored in a configuration file that the user modifies via the GUI
- manages the acquisition from the digitizers
- redirects the data streaming to the online processing and visualization algorithms
- saves the data in a raw format that can be used for a further offline run

The Plotter provides:

- the visualization of Waveforms, time, energy, PSD and scatterplot spectra;
- Energy calibration, zoom/pan, ROIs and filters definitions;
- saves the histograms
- saves the list. There is one list file per channel which includes: Channel Number and Board ID in the file name, TimeStamp, Energy, Flags and optionally waveforms samples for each event.



**Fig. 4.1:** CoMPASS block diagram.

The acquisition software can also perform offline runs in which the data are coming from the raw files saved during the standard online run, and apply different filters to produce new spectra.

## GUI Description



**Note:** Refer to [RD10] for a detailed description of the installation procedure both for Windows and Linux and for an example of application.

When the CoMPASS software is launched, the following Initial Main Screen is displayed:

From the main panel of the CoMPASS software GUI (Fig. 4.2) select

**FILE -> New Project**, or press the button

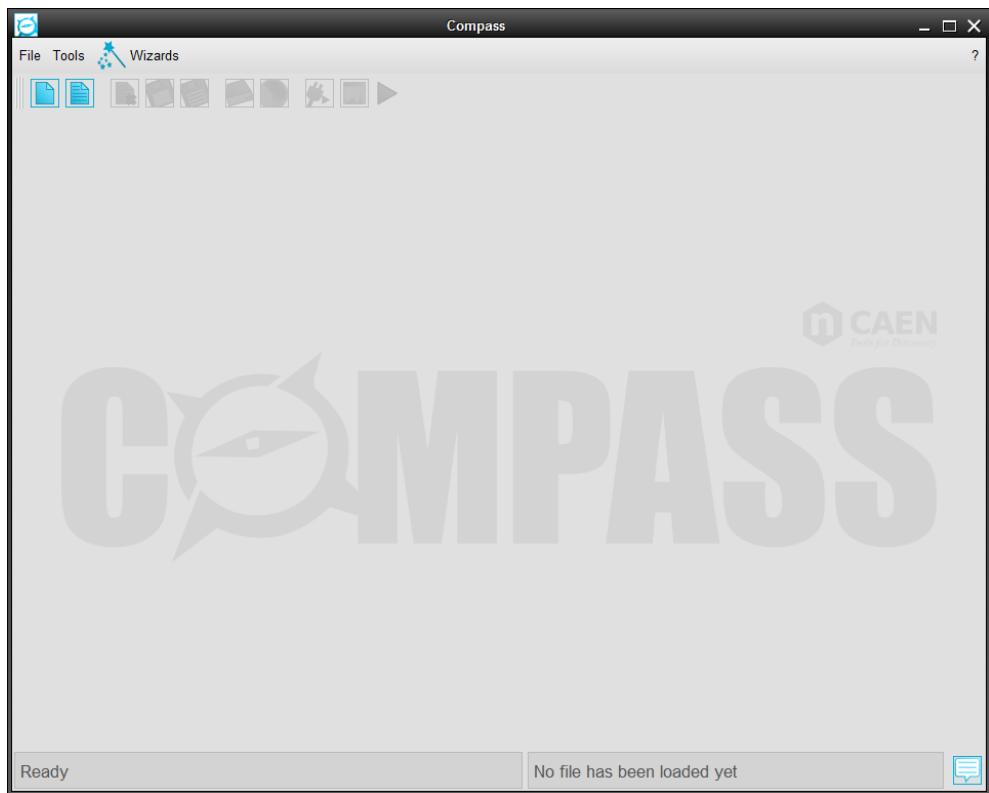


A pop-up windows will appear asking the user to select the folder in which the project will be saved. Each project will include all the details about the involved boards and respective firmware and settings.

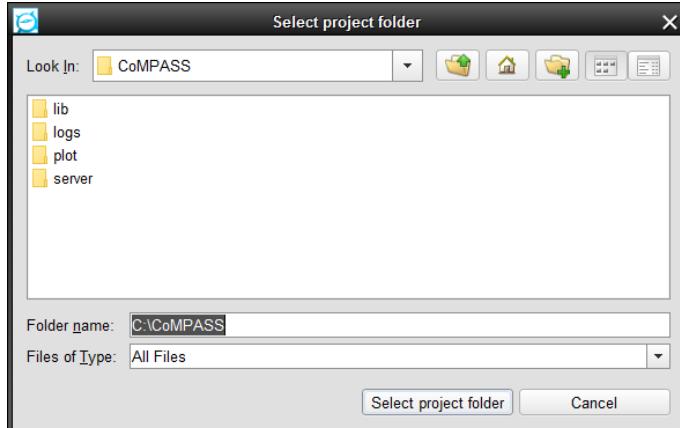
Select an already existing folder or create a new one by pressing the button



The CoMPASS Software will then scan all the active connection interfaces searching for the connected boards. After the scan has completed CoMPASS will show the detected board as different sub-tabs in the Acquisition and Settings tab (Fig. 4.4 and 4.5).



**Fig. 4.2:** CoMPASS Start window.



**Fig. 4.3:** CoMPASS New Project window.

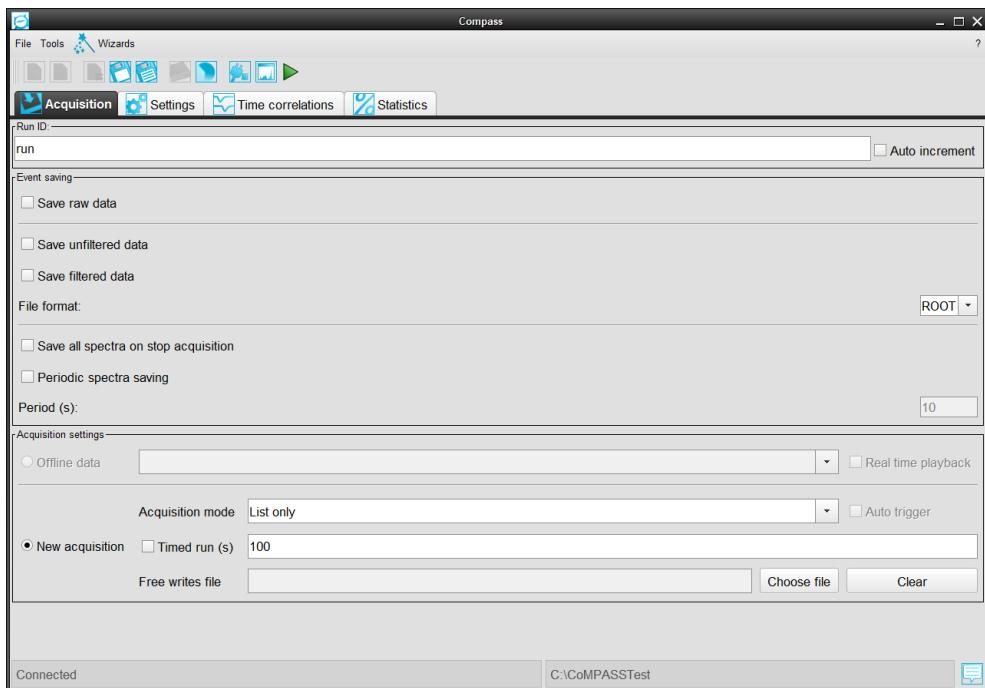
## Menu Bar Items

The menu bar is constituted by the following items: File, Tools, Wizards.

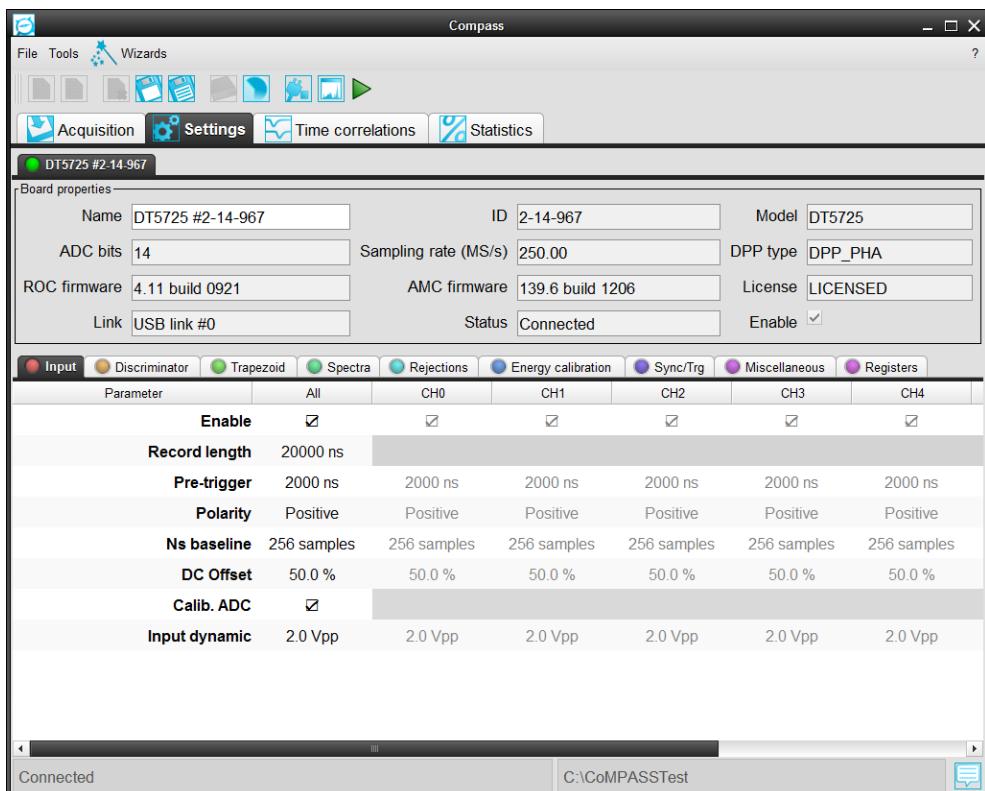
### File

The pull-down Menu shows the following items: New Project/Open Project/Save Project/Save Project As/Close Project/Exit

- **New Project:** this function allows the user to start a new project (Fig. 4.3). The user have to select the folder in which the project will be created and then press on the button "Select Project Folder". If



**Fig. 4.4:** CoMPASS Acquistion Tab.



**Fig. 4.5:** CoMPASS Settings Tab.

the folder already contains a CoMPASS project a pop-up appears informing the user that can decide to overwrite the selected folder content or change it.

Clicking Yes, CoMPASS will try to connect to the boards while clicking No, CoMPASS will return to the starting window.



- **Open Project**
- **Save Project**
- **Save Project As**
- **Close Project:** close the current project.

In order to close the project the user must first disconnect from the boards by pressing the button



If the configuration has not been saved ComPASS notifies the user asking for the action to do.



- **Exit:** completely close CoMPASS

## Tools

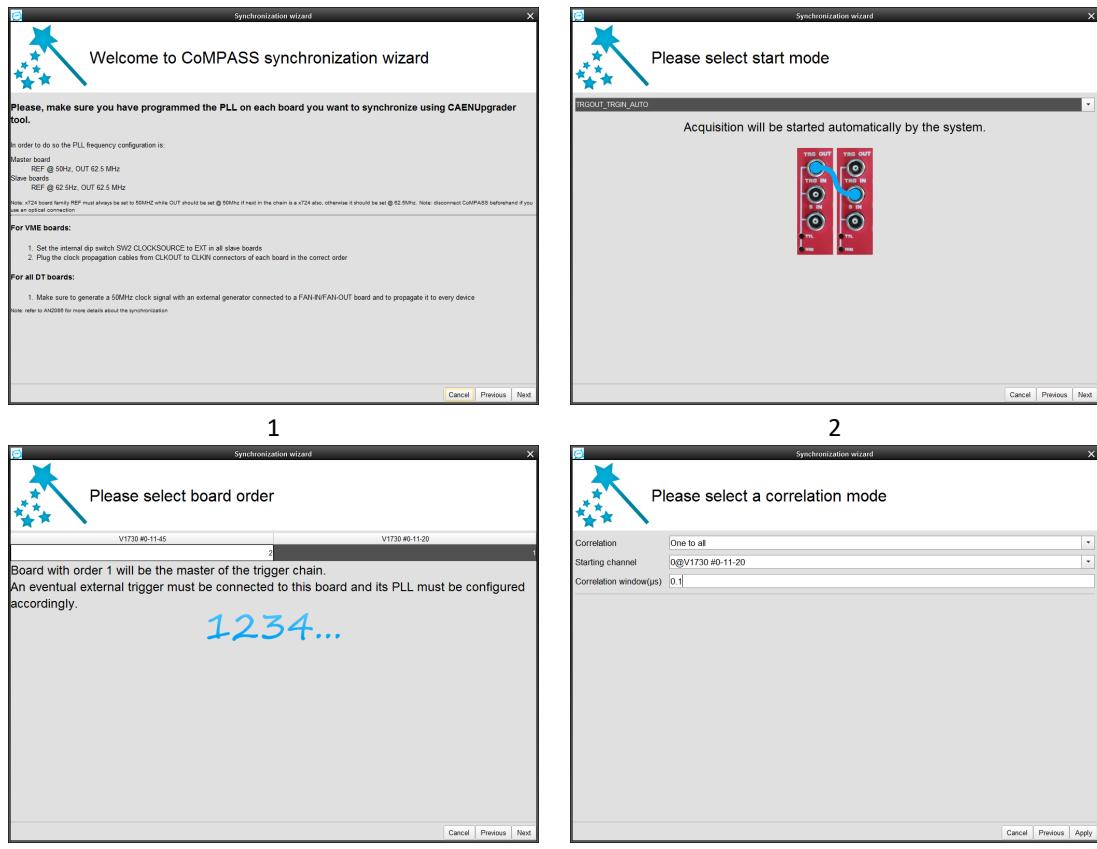
The pull-down Menu shows the following items:

- **Scan:** this function allows the user to scan for the connected boards through all the interfaces supported by CAEN digitizer
- **Connect/Disconnect:** this function allows the user to connect/disconnect to the connected digitizer(s)
- **Show Plot/Hide Plot:** this function allows the user to open/close the CoMPASS plotter
- **Start Acquisition/Stop Acquisition:** this function allows the user to Start/Stop the acquisition
- **System log:** this function allows the user to open the system log and check for possible error or warning messages
- **Skin:** this function allows the user to change the CoMPASS skin

## Wizards

The pull-down Menu shows the following items:

- **Synchronization wizard:** allows the user to configure the synchronization among multiple boards. Each page of the wizard guides the user throughout the configuration. In particular:

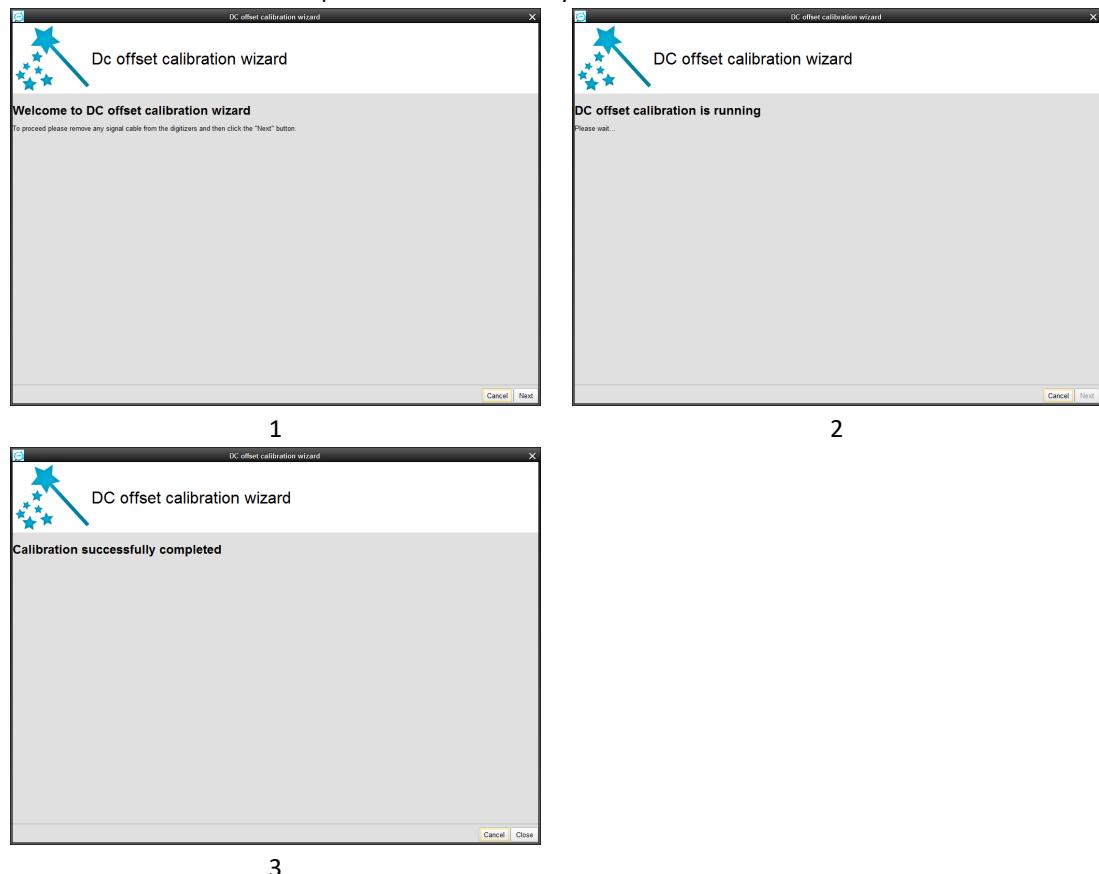


1. defines the steps to be done in advance to properly setup the system: i.e. program the PLL of the boards using the CAENUpgrader tool, connect the clock cables, and set the dip switch "Clock source" to EXT (for VME slave boards).
2. select the desired start/stop acquisition modes:
  - GPO\_TRGIN\_AUTO (Desktop/NIM only), propagates the run through GPO to TRGIN front panel connectors. The start acquisition is automatically sent through the software command (press PLAY).
  - GPO\_TRGIN\_EXTERN (Desktop/NIM only), propagates the run through GPO to TRGIN front panel connectors. The start acquisition is done by the first trigger on the MASTER board and automatically propagated to the SLAVES.
  - TRGOUT\_TRGIN\_AUTO (VME only), propagates the run through TRG-OUT to TRGIN front panel connectors. The start acquisition is automatically sent through the software command (press PLAY).
  - TRGOUT\_TRGIN\_EXTERN (VME only), propagates the run through TRG-OUT to TRGIN front panel connectors. The start acquisition is done by the first trigger on the MASTER board and automatically propagated to the SLAVES.
  - TRGOUT\_SYNCIN (VME only), propagates the run through TRG-OUT to S-IN front panel connectors. The run is synchronized with the level of an external signal on S-IN of the MASTER and propagated to the SLAVES.
  - GPO\_GPI (Desktop/NIM only), propagates the run through GPO to GPI front panel connectors. The run is synchronized with the level of an external signal on GPI of the MASTER and propagated to the SLAVES.

A picture shows the cable connection for the run propagation

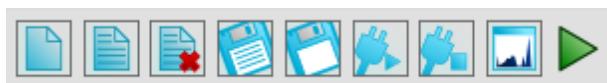
3. select the board order, where 1 is the master.
4. select the correlation mode. Refer to Sec. **The Time Correlation Tab** for more details.

- **DC offset calibration wizard:** allows the user to perform the DC offset calibration and save the calibration into the project. The user must make sure that no input cable is fed into the input connectors. The DC offset calibration then proceeds automatically.



## Icon Bar

The following Icon Bar is present under theMenuBar



**Fig. 4.6:** CoMPASS Icon Bar.

The above icons correspond to the following functions (from left to right):

1. New Project  : this icon has the same function of the Menu Bar/ File / New Project command
2. Open Project  : this icon has the same function of the Menu Bar/ File / Open Project command
3. Close Project  : this icon has the same function of the Menu Bar/ File / Close Project command
4. Save Project  : this icon has the same function of the Menu Bar/ File / Save Project command

5. Save Project as  : this icon has the same function of the Menu Bar/ File / Save Project Project as command
6. Connect/Disconnect Board   : these icons have the same function of the Menu Bar/ Tools / Connect/Disconnect Board command
7. Show/Hide Plot  : these icons have the same function of the Menu Bar/ Tools / Show/Hide Plot command
8. Start/Stop Acquisition   : these icons have the same function of the Menu Bar/ Tools / Start/Stop Acquisition command

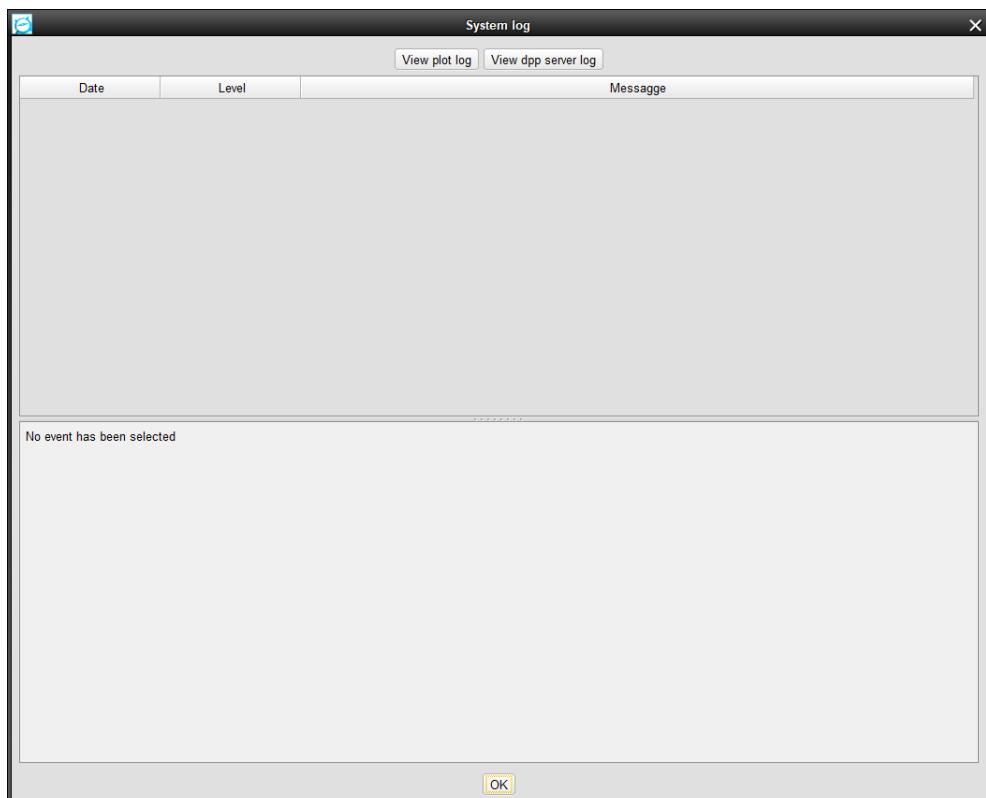
## The System Information Ribbon

The System Information Windows show on the left side the **status** (connected or disconnected) of the boards included in the project and on the right side the **current project folder path**.



**Fig. 4.7:** CoMPASS System Ribbon.

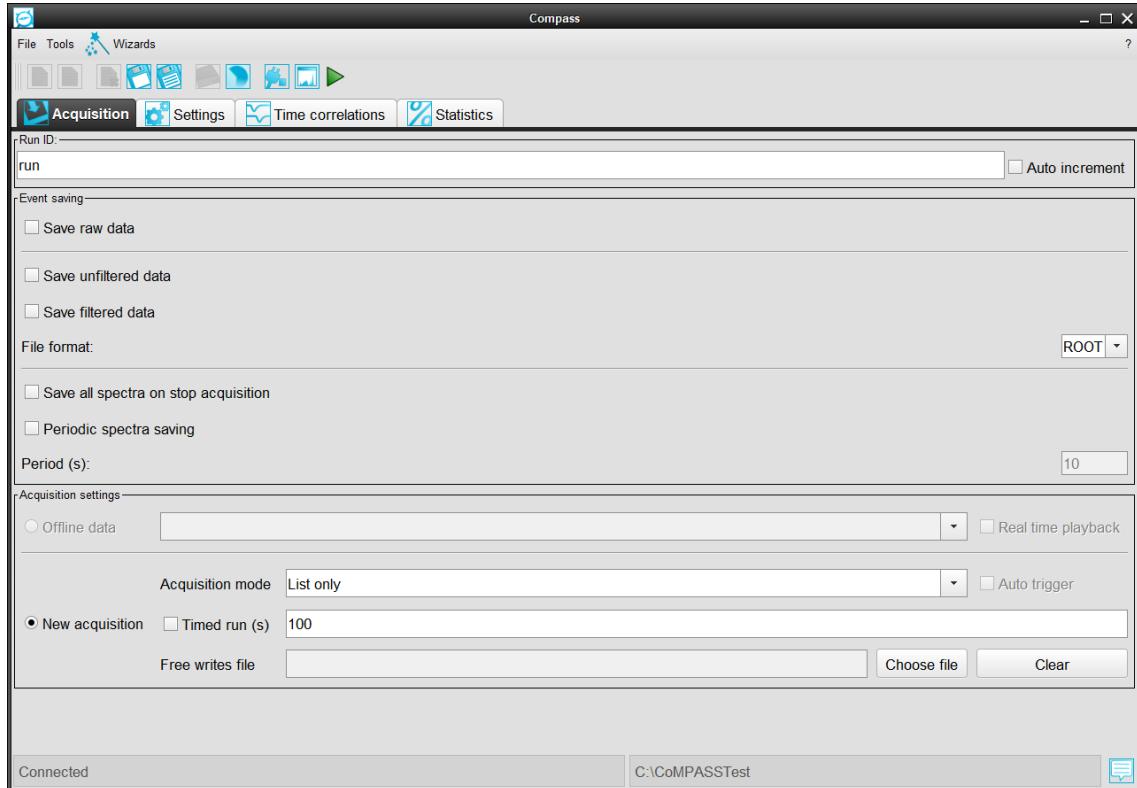
 Pressing on the  the user can open the System Log panel in the diagnostic messages provided by CoMPASS are included.



**Fig. 4.8:** CoMPASS System Log Windows.

## The Acquisition Tab

The Acquisition Tab allows the user to set and view the global acquisition parameters.



**Fig. 4.9:** CoMPASS Acquisition Tab.

The Acquisition Tab is divided into 3 different fields:

1. **Run ID:** in this field the user can write a custom run name and click on the Auto-Increment tick will let the software to add a progressive number that will be incremented at each start of run.
2. **Event Saving:** in this field the user can select if and which kind of events are saved and the desired file format. Filtered and unfiltered data can be saved in more than one format: .root, .csv and .bin, while the raw data are saved in a .cae proprietary format. See the following paragraphs for more details.
3. **Acquisition settings:** in this field the user can select if performing a new acquisition or running an offline run starting from a raw data file recorded in a previous session.

In case of **Offline data** the user can select the .cae file to be reproduced and the speed of reproduction. Default is high speed, otherwise select **Real time playback** for reproducing the run at the real speed.

In case of **New acquisition** the user can:

- select the **Acquisition Mode** (Waves or List)
- enable or disable a **Timed run** and set the run duration
- enable or disable the **Autotigger** functionality clicking on the corresponding tick
- include a **FreeWrites** file to make special board configurations using register writes. It is possible to **Choose a file** or to **Clear** the settings if no longer required.

The **FreeWrites** file must be written according to one of the following format:

- boardID address value
- boardID address value mask
- boardID address value FirstBit LastBit



**Note:** Writes can be done for individual address only, **do not** use the broadcast addresses.

where "mask" corresponds to the bit/bits to be written, "FirstBit" and "LastBit" can be used when there are consecutive bits to be written.

For example:

- (a) (board ID = 2-14-967) to write register 0x810C equal to 0xC0000000 use the notation:  
2-14-967 0x810C 0xC0000000
- (b) (board ID = 2-14-967) to set bit[12] = 1 of register 0x1080 either use the notation:  
2-14-967 0x1080 0x1000 0x1000  
2-14-967 0x1080 0x1 12 12
- (c) (board ID = 2-14-967) to set bit[20:22] = 100 (bin) of register 0x1080 either use the notation:  
2-14-967 0x1080 0x400000 0x700000  
2-14-967 0x1080 0x4 20 22



**Note:** The FreeWrites are loaded every time the acquisition is started and the write commands are executed at the end of the digitizer programming (settings might be overwritten by the FreeWrites commands).

## Data Saving Options

It is possible to save data in different ways:

1. Save the raw data
2. Save the energy, PSD, time and 2D spectrum
3. Save the list of Trigger Time Stamp, Energy, PSD and possibly waveforms for each event
4. Save an image of the energy, PSD, time and 2D spectrum

Select the run name and tick the "Auto increment" box to increase the run index at every start acquisition.

Run ID:	run	<input type="checkbox"/> Auto increment
---------	-----	---

All saved files are available in the project folder, under the "DAQ\run" sub-folder. For each run, **run.info** and **settings.xml** files are saved, reporting general run information and the boards settings respectively.

### Save the raw data

In order to save the raw data the user must select the "**Save raw data option**" tick into the Event Saving section of the Acquisition Tab.

Event saving:	<input type="checkbox"/> Save raw data
---------------	--

The raw data is saved into a proprietary file format and can be processed again performing an offline run where the user can run again the full acquisition possibly setting different data selection.

## Save the list of Trigger Time Stamp, Energy, PSD and waveforms

In order to save a list file in which the Trigger Time Stamp, Energy, PSD and possibly waveform samples information are included the user must select the "**Save filtered data**" and/or the "**Save unfiltered data**" tick into the Event Saving section of the Acquisition Tab if he/she want to save the data in which the possible defined filter are applied or not respectively. One file is generated for filtered and/or unfiltered data under the path: "DAQ\run\FILTERED\UNFILTERED".



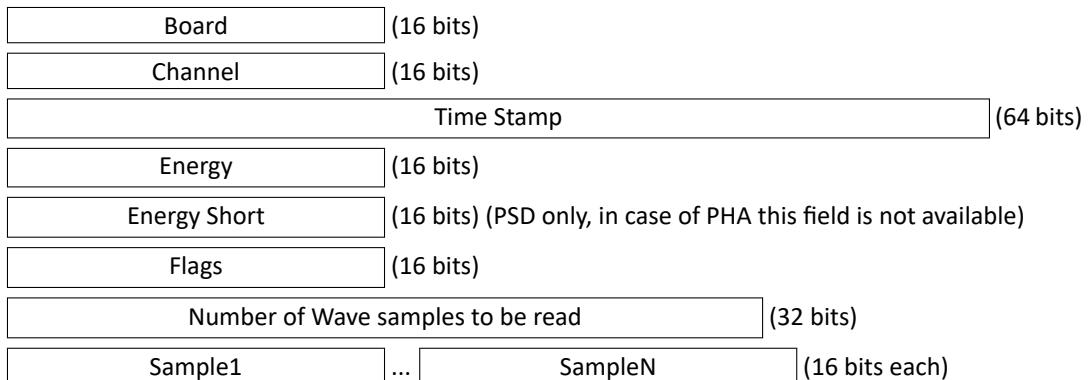
The available file formats are root (.root), *Comma Separated Values* (.csv) and Binary (.bin).

1. In case of **.root** format, a tree is generated with all the information. The tree name is "data" and it contains the following branches: "channel", "time stamp", "board", "energy", "energy short" (PSD only), "flags".
2. In case of **.csv** format, a first raw indicates the meaning of the subsequent values, which are:
  - PSD (+ waveform) = Time stamp, Energy, Energy short, Flags, (samples);
  - PHA (+ waveform) = Time stamp, Energy, Flags, (samples).



**Note:** The time stamp is expressed in ps.

3. In case of **.bin** format, the output file is represented as follows:



**Flags** are listed below:

0x1	A dead-time is occurred before this event
0x2	Time stamp roll-over
0x4	Time stamp reset from external
0x8	Fake event
0x10	A memory full is occurred before this event
0x20	A trigger lost is occurred before this event
0x40	N triggers have been lost (N can be set through bits[17:16] of register 0x1n84 <b>[RD4]</b> )
0x80	The event is saturating inside the gate - clipping
0x100	1024 triggers have been counted
0x400	The input is saturating
0x800	N triggers have been counted (N can be set through bits[17:16] of register 0x1n84 <b>[RD4]</b> )
0x1000	Event not matched in the time correlation filter but visualized in the waveform
0x4000	Event with fine time stamp
0x8000	Piled-up event

## Save the spectra

Energy, PSD, time and 2D spectra can be saved choosing between two options:

- save all spectra at the end of the run;
- save all spectra periodically, with a programmable period.

Both options can be checked together.



## Save an image of the energy, PSD, time and 2D spectrum

In order to save a picture of the energy, PSD, time and 2D spectrum the user must press the button



The picture is saved in the .png format.

## The Settings Tab

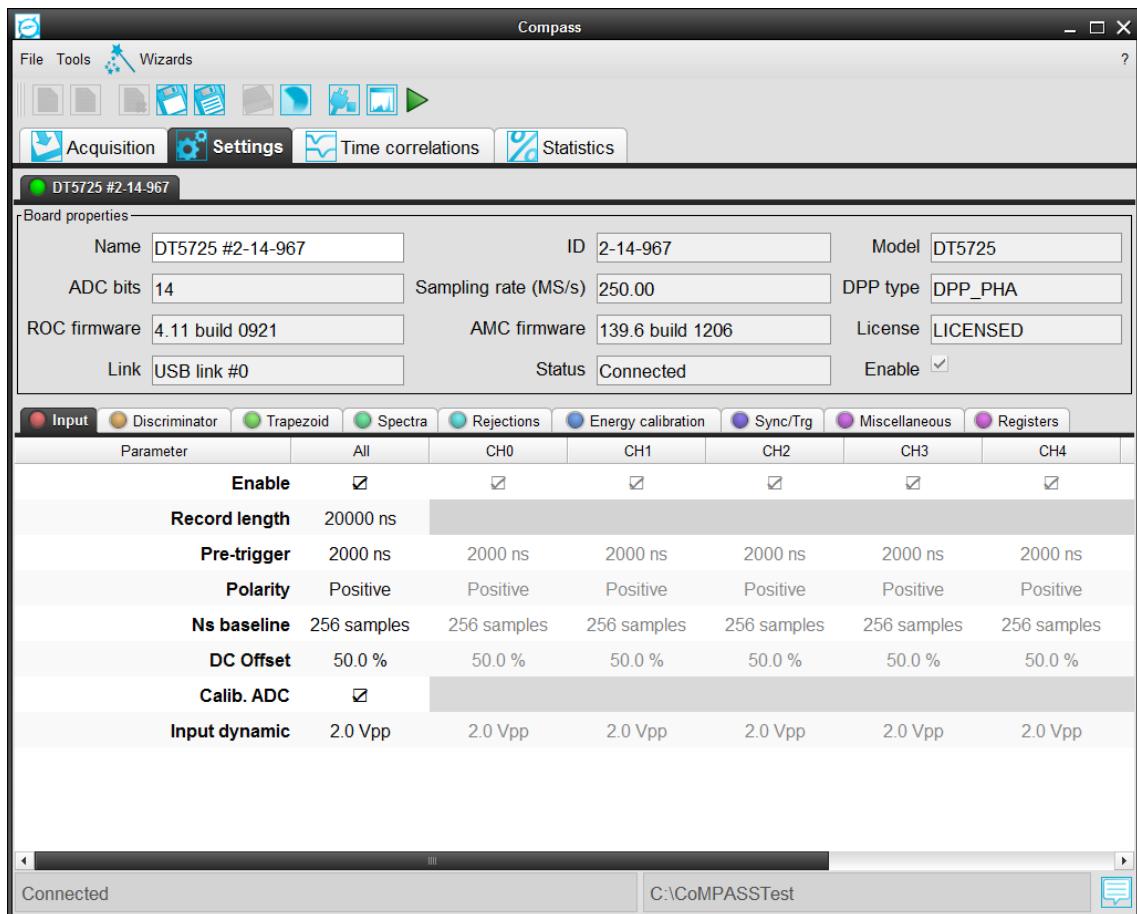
The Settings Tab and the subtabs there included allows the user to set all the acquisition parameters at the board and single channel level. For each parameter, acting on the "All" column, the modified setting will be applied to all the channel of the board while acting on the "Ch n" column the modified setting will be applied only to the selected channel.



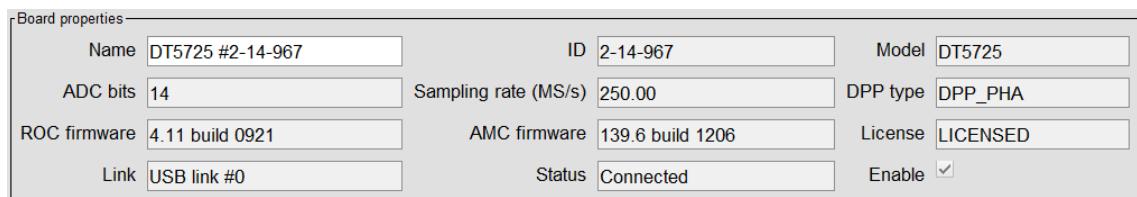
**Note:** The individual setting on "CHn" is not modified by the global setting on the "All" column.

In the following sections a detailed description of all the subtabs is provided.

In the top part of the Settings Tab the **Board Properties** section includes as many tab as the number of connected boards and in each tab several fields in which many information about the active and selected board are shown, like board ID and model, the firmware type and release, the DPP licence information, and the communication link used and the global board status.



**Fig. 4.10:** CoMPASS Settings Tab.



**Fig. 4.11:** Board Properties section in the Settings Tab.

## The Input Tab

The **Input Signal Tab** is shown in Fig. 4.12.

The **Input Signal Tab** allows the user to operate on the following hardware and firmware parameters:

- **Enable:** to enable or disable the channel(s)
- **Record Length:** selects the length of the acquisition window expressed in ns
- **Pre-Trigger:** sets the portion of the waveform acquisition window to be saved before the trigger. Its value is expressed in ns.
- **Polarity:** selects the polarity (Negative/Positive) of the input signal to be processed by the DPP-PSD/PHA algorithm. In case of DPP-PHA firmware, the algorithm works with positive pulses only. By setting “Negative” the algorithm will invert the digital samples of the input and the input will always appear as positive in the waveform inspector.
- **Ns baseline:** sets the number of samples used by the mean filter to calculate the input pulse baseline. Allowed values are:

Input	
Parameter	All
<b>Enable</b>	<input checked="" type="checkbox"/>
<b>Record length</b>	992 ns
<b>Pre-trigger</b>	96 ns
<b>Polarity</b>	Negative
<b>Ns baseline</b>	256 samples
<b>Fixed BLR</b>	0
<b>DC Offset</b>	50.0 %
<b>Calib. ADC</b>	<input type="checkbox"/>
<b>Input dynamic</b>	2.0 Vpp

**Fig. 4.12:** CoMPASS Input Tab.

- for the 720 series: “Fixed”, 8, 32, 128;
- for the 724 series: “Fixed, 16, 64, 256, 1024, 4096, 16384;
- for the 725 and 730 series (DPP-PSD): “Fixed”, 16, 64, 256, 1024;
- for the 725 and 730 series (DPP-PHA): “Fixed”, 16, 64, 256, 1024, 4096, 16384;
- for the 751 series: “Fixed”, 8, 16, 32 64, 128, 256, 512

The “Fixed” option enables the absolute baseline calculation and requires the definition of “Fixed BLR” (the value of fixed baseline) in the GUI. In case of DPP-PHA “Fixed” means that the baseline is not evaluated.

- **DC Offset** sets the value of the DC Offset applied to the channel, expressed as the percentage of the Full Scale Range. Moving the DC Offset corresponds to moving the baseline level of the input signal upward or downward in the dynamic scale to cover the full width of the pulse itself, thus avoiding saturation. It is usually recommended to move the baseline upward for negative pulse, downward for positive signals. Mid-scale are fine for bipolar signals, or for small pulses. In case of saturation (both in the upper or lower limit) the algorithm stops any calculation.

The ADC scale goes (from bottom to top) from 0 to 100% for positive polarity, and from 100% to 0 for negative polarity. 50% sets the signal baseline to mid-scale. It is also possible to calibrate the DC Offset to have the same value among different channels (refer to Sec. **Wizards**).

- **Calib. ADC**: performs the calibration of the channel ADCs at every start acquisition (725, 730 and 751 series only). It is recommended to leave it enabled.
- **Input dynamic**: select the digitizer input dynamic range. Options are:
  - 0.5, 2 V<sub>pp</sub> for 725 and 730 family;
  - 0.3, 1, 3, 10 V<sub>pp</sub> for the 781 family;
  - not available for x720, x724 and x751 digitizer family.

## The Discriminator Tab

The **Discriminator Tab** is shown in Fig. 4.13 (DPP-PSD only) and in Fig. 4.13 (DPP-PHA only).

The **Discriminator Tab** allows the user to operate on the following hardware and firmware parameters:

- **Discriminator mode** (DPP-PSD only): when available, sets the discriminator mode, Leading Edge or CFD;
- **CFD delay** (DPP-PSD only): when available, sets the CFD delay in ns;
- **CFD fraction** (DPP-PSD only): when available, sets the CFD fraction. Option are 25%, 50%, 75% and 100%;

Discriminator	
Parameter	All
<b>Discriminator mode</b>	CFD
<b>Threshold</b>	100 lsb
<b>Trigger holdoff</b>	1024 ns
<b>Cfd delay</b>	4 ns
<b>Cfd fraction</b>	75%
<b>Input Smoothing</b>	Disabled

Fig. 4.13: CoMPASS Discriminator Tab (DPP-PSD with CFD Only (725, 730, and 751 series)).

Discriminator	
Parameter	All
<b>Threshold</b>	100 lsb
<b>Trigger holdoff</b>	480 ns
<b>Fast Discriminator smoothing</b>	4 samples
<b>Input rise time</b>	100 ns

Fig. 4.14: CoMPASS Discriminator Tab (DPP-PHA Only).

- **Input smoothing** (DPP-PSD only): the smoothing is a moving average filter, where the input samples are replaced by the mean value of the previous n samples. When enabled, the trigger is applied on the smoothed samples, thus reducing triggering on noise. Both CFD and LED triggering modes can be used on the smoothed input.
- **Threshold**: The threshold value can be set from 0 to the Max Number of Channels (Bins) in LSB.
- **Trigger holdoff**: during the Trigger Hold-Off Time other trigger signals are not accepted by the digitizer. It can be set in microseconds;
- **Ttf smoothing** (DPP-PHA only): the RC-CR<sup>2</sup> input signal second derivative smoothing value can be selected between 4, 8, 16, 32 and 64 (64 only for the x725 and 730 series);
- **Ttf delay** (DPP-PHA only): this is a value set to optimize the shape the RC-CR<sup>2</sup> signal used to trigger the board channels. Maximum allowed value is 2.55 us;

## The QDC/Trapezoid Tab

The tab corresponding to the energy calculation is called **QDC** for the DPP-PSD firmware (see Fig. 4.15) and **Trapezoid** for DPP-PHA firmware (see Fig. 4.16).

QDC	
Parameter	All
<b>Gate</b>	800 ns
<b>Short gate</b>	400 ns
<b>Pre-gate</b>	48 ns

Fig. 4.15: CoMPASS QDC Tab (DPP-PSD Only).

The two tabs allows the user to evaluate the pulse energy, by means of a charge integration of the pulse inside a gate (DPP-PSD), or by means of a trapezoidal filter (DPP-PHA). The programmable parameters are the following:

Trapezoid	
Parameter	All
<b>Trap. rise time</b>	4.992 $\mu$ s
<b>Trap. flat top</b>	0.992 $\mu$ s
<b>Trap. pole zero</b>	50.000 $\mu$ s
<b>Peaking time</b>	80.6 %
<b>Ns peak</b>	1 samples
<b>Peak holdoff</b>	0.992 $\mu$ s

Fig. 4.16: CoMPASS Trapezoid Tab (DPP-PHA Only).

- **Gate** (DPP-PSD only): sets the gate width for the Energy and  $Q_{long}$  calculation. Values are expressed in ns and can vary in steps of clock units (i.e. 4 ns if 720 series and 725 series, 2 ns for 730 series, and 1 ns if 751 series);
- **Short gate** (DPP-PSD only): sets the short gate width for the  $Q_{short}$  calculation. Values are expressed in ns and can vary in steps of clock units;
- **Pre-gate** (DPP-PSD only): sets the “pre-gate” parameter, i.e. the starting position of the gate and short gate before the trigger signal. Values are expressed in ns and can vary in steps of clock units. Pre-gate and Pre-trigger must follow the relation:

- For 720 series

$$\text{Pre-gate} \leq \text{Pre-trigger} - 32\text{ns} \quad (4.1)$$

- For 725-730 series the firmware automatically adjusts wrong combinations of pre-gate and pre-trigger to the minimum allowed values.
- For 751 series

$$\text{Pre-gate} \leq \text{Pre-trigger} - 8\text{ns} \quad (4.2)$$

- **Trap. rise time** (DPP-PHA only): Allowed values for the Trapezoid Rise time are from 0 to 10.20 us with 10 ns steps for 724 series, 8.184 us with 8 ns steps for 730, and 16.368 us with 16 ns steps for 725;
- **Trap. flat top** (DPP-PHA only): Allowed values for the Trapezoid Rise time are from 0 to 10.20 us with 10 ns steps for 724 series, 8.192 us with 8 ns steps for 730, and 16.384 us with 16 ns steps for 725;



**Note:** the sum of the Trapezoid Rise Time and Flat Top should not exceed 15 us times the Decimation value for 724 and 781 series (DPP-PHA firmware release < 128.64 only), 16 us times the Decimation value for 725 series, and 8 us times the Decimation value for 730 series.

- **Trap. pole zero** (DPP-PHA only): The user can set the Trapezoid pole zero compensation from 0 up to 655.35 us with 10 ns steps for 724 series, 524.280 us with 8 ns steps for 730, and 1048.560 us with 16 ns steps for 725;
- **Peaking time** (DPP-PHA only): The user can set the Peaking time value from 0% to 100% in 0.1% steps, which corresponds to the percentage of the flat top duration;
- **Ns peak** (DPP-PHA only): The user can set how many Flat Top sample have to be used for the energy evaluation. Options are: 1, 4, 16, 64.
- **Peak holdoff** (DPP-PHA only): The user can set the Peak hold off time that defines how close must be two trapezoids to be considered piled-up.

## The Spectra Tab

The **Spectra Tab** summarizes the number of channels and the limits of all the spectra that can be done with CoMPASS (see Fig. 4.17).

Spectra	
Parameter	All
<b>Energy N channels</b>	16384
<b>PSD N channels</b>	16384
<b>Time intervals N channels</b>	16384
<b>Time intervals Tmin</b>	0.000 µs
<b>Time intervals Tmax</b>	1000.000 µs
<b>Start/stop Δt N channels</b>	16384
<b>Start/stop Δt Tmin</b>	-10000 ns
<b>Start/stop Δt Tmax</b>	10000 ns
<b>2D Energy N channels</b>	1024
<b>2D PSD N channels</b>	1024

**Fig. 4.17:** CoMPASS Spectr Tab.

Allowed values are

- **Energy N channels:** 256, 512, 1024, 2048, 4096, 8192, 16384.
- **PSD/Time Intervals/Start-Stop Δt N channels:** 1024, 2048, 4096, 8192, 16384.
- **2D Energy/2D PSD N channels:** 128, 256, 512, 1024.

## The Rejection Tab

The **Rejection Tab** allows the user to apply filters on the histogram and select the corresponding events.

It is also possible to apply the cut directly on the plot by pressing the button 

A cursor will then become available and the user have to click on the histogram points that will be the "Low Cut" and "High Cut".

To apply the cut the user have to press the button 

The allowed cuts are shown in Fig. 4.18:

Rejections	
Parameter	All
Energy low cut	0.000
Energy high cut	0.000
Energy cut enable	<input type="checkbox"/>
PSD low cut	0.000
PSD high cut	0.000
PSD cut enable	<input type="checkbox"/>
Time intervals low cut	0
Time intervals high cut	0
Time intervals cut enable	<input type="checkbox"/>
Saturation rejection enable	<input type="checkbox"/>
PUR enable	<input type="checkbox"/>
PUR gap	1000 lsb

**Fig. 4.18:** CoMPASS Rejection Tab.

- **Energy Low cut:** the value (in LSB or Energy units when the Energy calibration is performed - refer to Sec. **The Energy Histogram Icon Bar**) to use as a lower value for a user defined filter;
- **Energy High cut:** the value (in LSB or Energy units) to use as a higher value for a user defined filter;
- **Energy cut enable:** enable/disable the energy cut;
- **PSD Low cut:** the value (between 0 and 1) to use as a lower value for a user defined filter;
- **PSD High cut:** the value (between 0 and 1) to use as a higher value for a user defined filter;
- **PSD cut enable:** enable/disable the PSD cut;
- **Time intervals low cut:** the value (in ns) to use as a lower value for a user defined filter;
- **Time intervals high cut:** the value (in ns) to use as a higher value for a user defined filter;
- **Time intervals cut enable:** enable/disable the Time intervals cut;
- **Saturation rejection enable:** enable/disable the event rejection in case of saturation;
- **PUR enable:** enable/disable the event rejection in case of pile-up;
- **PUR gap:** the value (in LSB units) of the PUR gap for the pile-up identification. Refer to Sec. **Pile-up management (720, 725, and 730 series)**.

## The Energy Calibration Tab

The **Energy Calibration Tab** is shown in Fig. 4.19 for DPP-PSD and Fig. 4.20 for DPP-PHA.

Energy calibration	
Parameter	All
<b>Energy coarse gain</b>	80 pC/LSB
C0	0.000
C1	1.000
C2	0.000
<b>Calibration units</b>	keV

Fig. 4.19: CoMPASS Energy Calibration Tab (DPP-PSD).

Energy calibration	
Parameter	All
<b>Energy fine gain</b>	1
C0	0.000
C1	1.000
C2	0.000
<b>Calibration units</b>	keV

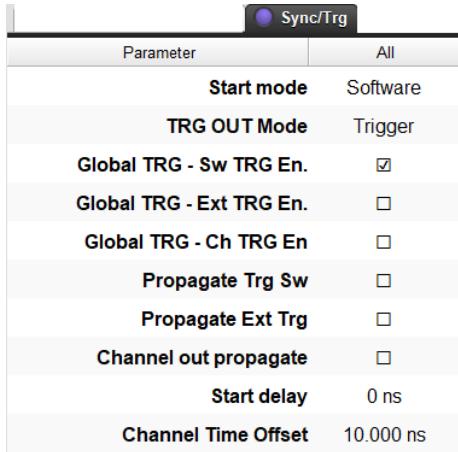
Fig. 4.20: CoMPASS Energy Calibration Tab (DPP-PHA).

The **Energy Calibration Tab** allows the user to operate on the following commands:

- **Energy coarse gain** (DPP-PSD only): the Energy coarse gain allows to rescale the signal charge. This is useful especially when the charge exceeds the full-scale range. The user sets, the weight of the LSB for the charge data. For instance, if Q = 100 counts and Charge Sens. = 40 fC/LSB, the integrated charge is 4 pC. When the charge pulse exceeds the full scale range, it is recommended to reduce the sensitivity in order to avoid saturation. The allowed values (fC/LSB) are:
  - for the 720 series: 40, 160, 640, 2560;
  - for the 725 and 730 series: 5, 20, 80, 320, 1280;
  - for the 751 series: 20, 40, 80, 160, 320, 640
- **Energy fine gain** (DPP-PHA only): The user can set the Energy fine Gain from x1 to x10
- **C0/C1/C2**: the energy spectrum calibration parameters (Read-Only). The calibration panel and procedure will be described in the following paragraphs;
- **Calibration Units**: the energy spectrum calibration units (Read-Only). The calibration panel and procedure will be described in the following paragraphs;

## The Sync/Trg Tab

The **Sync/Trg Tab** is shown in Fig. 4.21.



Parameter	All
<b>Start mode</b>	Software
<b>TRG OUT Mode</b>	Trigger
Global TRG - Sw TRG En.	<input checked="" type="checkbox"/>
Global TRG - Ext TRG En.	<input type="checkbox"/>
Global TRG - Ch TRG En	<input type="checkbox"/>
Propagate Trg Sw	<input type="checkbox"/>
Propagate Ext Trg	<input type="checkbox"/>
Channel out propagate	<input type="checkbox"/>
<b>Start delay</b>	0 ns
<b>Channel Time Offset</b>	10.000 ns

Fig. 4.21: CoMPASS Sync/Trg Tab.

The **Sync/Trg Tab** allows the user to operate on the following commands:

- **Start mode:** decides how the acquisition is started/stopped. Options are:
  - **Software:** start/stop commands are made via software by pressing the relative buttons.
  - **S\_IN Controlled:** the acquisition is synchronized with an external signal level on the S\_IN (GPI in case of Desktop/NIM form factors) front panel connector.
  - **First Trigger:** the acquisition starts on the first trigger received by the board and stops on the software command.
- **TRG OUT mode:** decides which signal is propagated to the TRG-OUT (GPO in case of Desktop/NIM form factors) front panel connector. Options are:
  - **0 level test signal:** propagates a low-level test signal.
  - **1 level test signal:** propagates a high-level test signal.
  - **Trigger:** propagates the internal trigger according to options "Propagate Trg Sw", "Propagate Ext Trg", and "Channel out propagate".
  - **Acq. ON:** propagates a signal which is high when the acquisition is on.
  - **Sampling clock:** propagates a signal which is synchronous with the sampling clock of the ADCs.
  - **PLL clock:** propagates a signal which is synchronous with the PLL clock.
  - **Busy signal:** propagates a signal which is synchronous with the busy.
  - **PLL lock:** propagates a signal which identifies a PLL lock loss.
  - **Channel signal:** propagates signal probes from channels.
  - **Sync in:** propagates the signal from S-IN (GPI) front panel connector.
- **Global TRG - Sw TRG En. / Ext TRG En. / Ch TRG En.:** decides which signal participates to the global trigger generation, choosing among software trigger, external trigger, and the channels trigger.
- **Propagate Trg Sw / Ext Trg:** Propagate on TRG-OUT front panel connector the Software/External trigger respectively.
- **Propagate Trg val to TRG OUT:** This option must be always enabled to propagate the signals from mother-board to mezzanines.
- **Channel out propagate:** propagate the channel trigger to TRG-OUT front panel connector.
- **Start delay:** sets the delay between master and slaves in case of multi-board synchronization.
- **Channel time offset:** sets a time offset for the board channels. This option can be used for fine adjustment of the delay in case of multi-board synchronization.

## The Miscellaneous Tab

The **Miscellaneous Tab** is shown in Fig. 4.22.

Miscellaneous	
Parameter	All
Label	Channel
FPIO type	NIM
<b>Rate optimization</b>	511

**Fig. 4.22:** CoMPASS Miscellaneous Tab.

The **Miscellaneous Tab** allows the user to operate on the following commands:

- **Label:** writing in this field the user can customize the channel label;
  - **FPIO type:** the user can select the signal type of the front panel I/O. Options: NIM, TTL.
  - **Rate optimization:** in case of low input rate (typ. < 100 Hz) it is required to set it to smaller value to optimize the throughput. In Waves mode CoMPASS automatically evaluate the appropriate value.

## The Register Map Tab

The **Register Map Tab** is shown in Fig. 4.23.

**Fig. 4.23:** CoMPASS Register Map Tab.

The **Register Map Tab** allows the user to operate directly on the firmware registers. The user can select the desired register in the top left combo box. The value will then appear in the **Address** field. The channel number (if required) can be selected in the **Ch** field.

If the register is a Read-Only one, only the **Read** button will be selectable and clicking on it the register value will be that reported in the **Value** field.

If the register is a Write-Only one, only the **Write** button will be selectable and the user has to write the desired value in the **Value** field and then press the Write button.

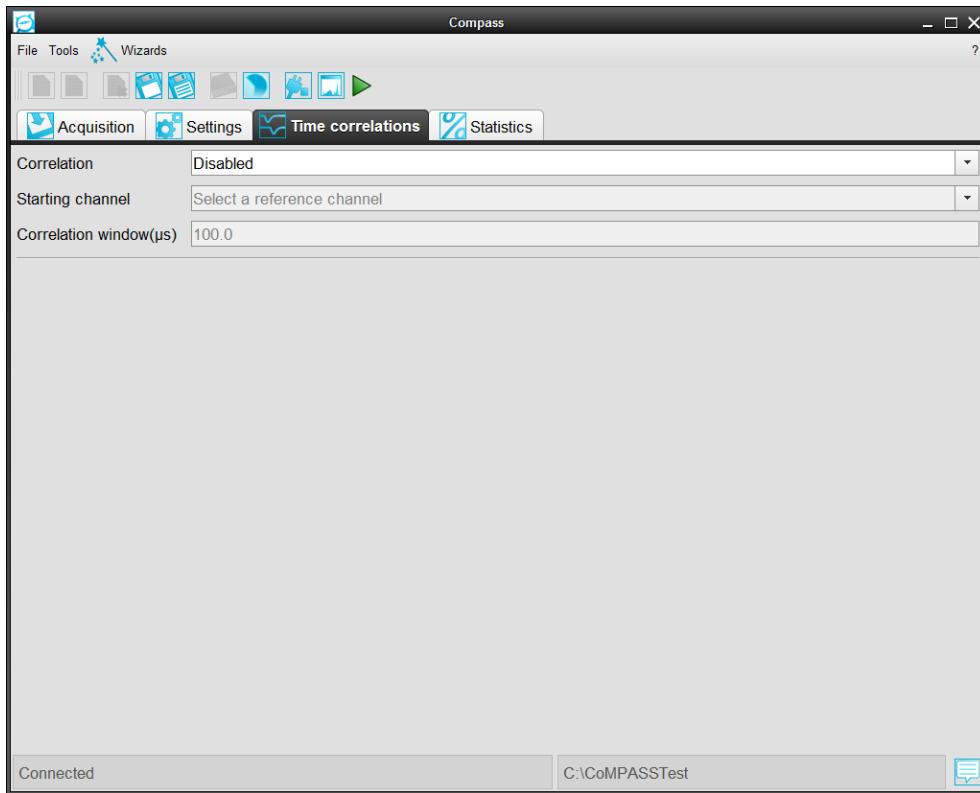
If the register in a Read/Write one both the functionalities described here above become available.

The three lines in the middle of the tab show the map of the selected register displaying the value of each single bit and including together with a quick description of the associated functionality (in the central line).

The user can also save on the local disk the full register map by clicking on the **Save register map to disk** button.

## The Time Correlation Tab

The **Time Correlation Tab** is shown in Fig. 4.24.



**Fig. 4.24:** CoMPASS Time Correlation Tab.

The **Time Correlation Tab** allows the user to operate on channel time correlation settings. The correlation is performed at the software level, i.e. without any modification of the boards firmware registers.

Using the **Correlation** combo box the user can select the following options:

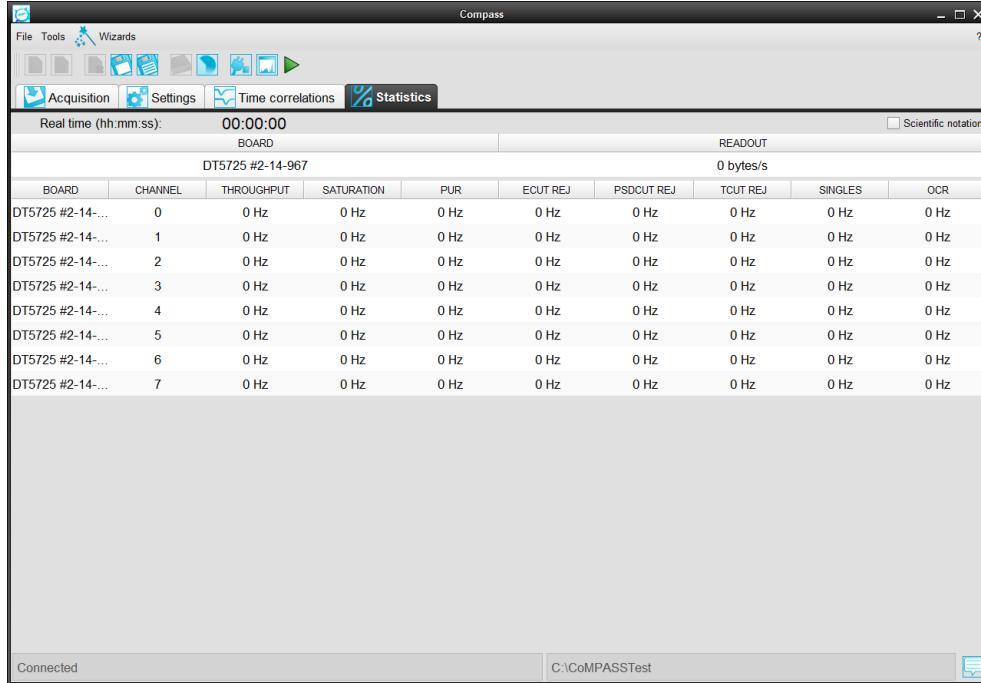
- **Disabled:** no correlation between the digitizer channels;
- **Couple:** the software will correlate the digitizer channels  $n$  and  $n+1$ , i.e. CH0 with CH1, CH2 with CH3 and so on and evaluates the time difference  $T_{\text{Ch}n+1} - T_{\text{Ch}n}$ ;
- **One to all:** it corresponds to the option **Common Start** in the traditional analog electronics with TDCs. One channel is meant to provide the reference time ( $T_{\text{start}}$ ) while all the others will be evaluated with respect to it ( $T_{\text{stop}}$ ).

Both in case of "Couple" and "One to all" options, the time differences are shown in the Tof plot (see Sec. **The Plotter Window**).

When selecting the "One to all" option the user must specify the reference channel in the **Starting channel** field. The width of the correlation window (in us) has to be specified in the **Correlation window** field.

## The Statistics Tab

The **Statistics Tab** is shown in Fig. 4.25.



**Fig. 4.25:** CoMPASS Statistics Tab.

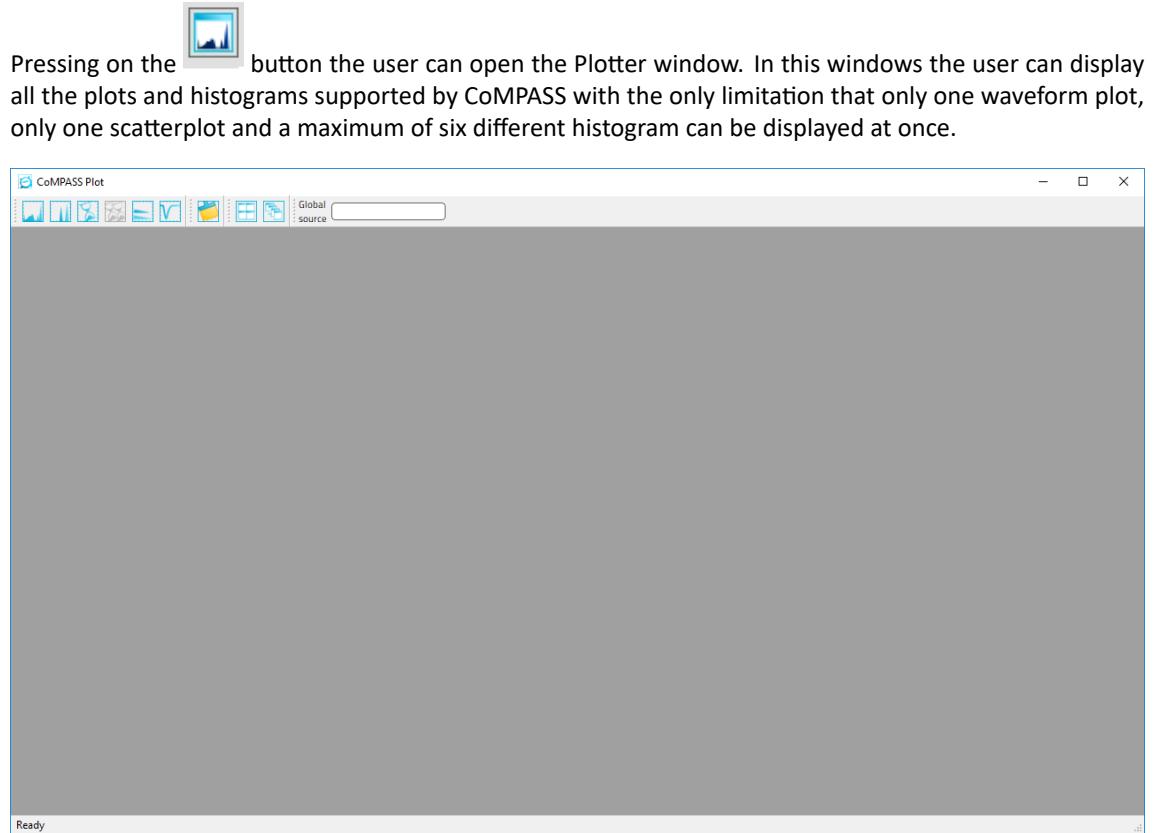
The **Statistics Tab** allows the user to monitor the acquisition statistics of the current run such as:

- **Real Time** of the acquisition;
- **Throughput**, the data rate from the board;
- **Saturation**, the rate of events saturating both the input dynamics and the gate or the trapezoid. In case of gate saturation, both the short and long gate are considered, both negative and positive saturation. Saturation cut must be enabled in the "Rejections" tab;
- **PUR** (Pile-Up Rejection), the rate of events identified as piled-up. Pile-up rejection must be enabled in the "Rejections" tab;
- **ECUT/PSDCUT/TCUT REJ**, the rate of events that have NOT passed the energy/PSD/time cuts. Cuts must be enabled in the "Rejections" tab or through the plot;
- **SINGLES**, the rate of events that have NOT passed the software time correlations (that can be set through the "Time Correlation" tab);
- **OCR**, the rate of events passing the cuts and filling the histograms.

NOTE: the sum of the columns from "Saturation" to "OCR" should give the "Throughput".

In addition the user can choose to display the information using the scientific notation in place of the standard one just clicking on the dedicated tick.

## The Plotter Window



**Fig. 4.26:** CoMPASS Plotter Window.

## The Plotter Window Icon Bar



**Fig. 4.27:** CoMPASS Plotter Window Icon Bar.

The above icons correspond to the following functions (from left to right):

1. **New Energy Histogram**  : this icon opens a new Energy Histogram;
2. **New PSD Histogram**  : this icon opens a new PSD Histogram;
3. **New Time Histogram**  : this icon opens a new Time Histogram;
4. **New Tof Histogram**  : this icon opens a new Tof (time difference between two channels) Histogram. This icon is active only when "Time Correlations" are enabled;
5. **New Scatterplot Histogram**  : this icon opens a new Scatterplot (Energy/PSD) Histogram;
6. **New Waveform**  : this icon opens the Waveform inspector. This icon is active only if "Acquisition mode = Waves";

7. **Clear All Histograms**  : this icon resets all the histograms;
8. **Tile**  : this icon allows to display the plots in tile mode;
9. **Cascader**  : this icon allows to display the plots in cascade mode;
10. **Global source**  : this combo box allows the user to select the global source to which all the plot will be referred.

Fig. 4.28 shows an example of the CoMPASS plotter in which a waveform plot, an energy histogram, a PSD histogram, a time histogram and a energy/PSD scatterplot are shown all together.

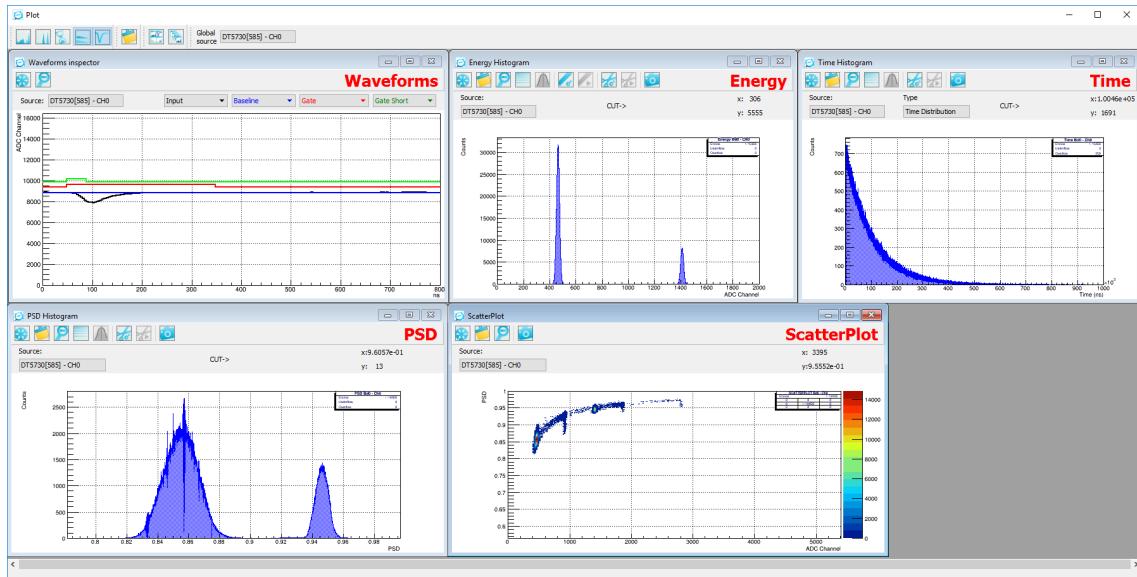


Fig. 4.28: CoMPASS Plotter Window with several plot displayed.

## The Waveform Plot Icon Bar



Fig. 4.29: CoMPASS Waveform Plot Icon Bar.

The above icons correspond to the following functions (from left to right):

1. **Freeze Plot**  : disable/enable the automatic refresh of the plot.
2. **Unzoom**  : unzoom the plot. **Note:** to zoom the plot select an interval in the x-axis or in the y-axis.

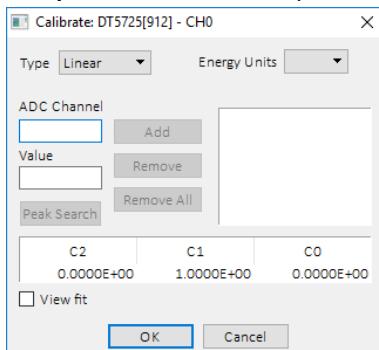
## The Energy Histogram Icon Bar

The above icons correspond to the following functions (from left to right):

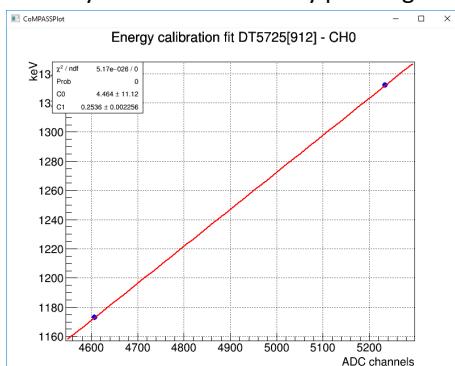


**Fig. 4.30:** CoMPASS Energy Histogram Icon Bar.

1. **Freeze Plot**  : disable/enable the automatic refresh of the plot.
2. **Clean Histogram**  : reset the histogram.
3. **Unzoom**  : unzoom the plot. **Note:** to zoom the plot select an interval in the x-axis or in the y-axis.
4. **LogY**  : Set the logarithmic y-scale.
5. **Fit:**  Fit the selected area. **Note:** to enable this button first freeze the plot.
6. **Setup Calibration:**  Opens the calibration window.



The user can select the calibration curve, choosing between "Linear" and "Quadratic", the Energy Units between keV and MeV, and add the peaks value in ADC channel and energy. It is also possible to verify the calibration fit by pressing "View fit"



7. **Apply Calibration:**  Apply the set calibration.
8. **Define Cut:**  After pressing this button it is possible to select the low and high cuts directly in the plot by clicking the two positions in the spectrum. The values of cuts will appear below the icon bar.

**CUT->**  
Low:6207.640  
High:9885.860

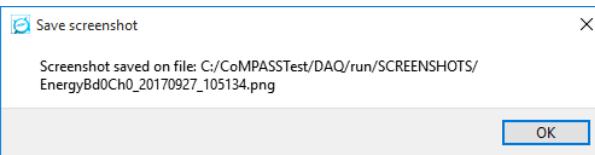
**Note:** it is also possible to select the cuts from the "Rejection" tab (see Sec. **The Rejection Tab**).

9. **Cut Apply:**  This button apply the selected cut. The dataset will be marked as "Filtered".

Dataset

Filtered

10. **Snapshot:**  This button takes a screenshot of the current plot.



11. **Save spectrum:**  This button save the spectrum in a txt file with one-column of energy values.



The histogram range can be defined in **The Spectra Tab** under "Settings" (*Energy*).

## The Time Histogram Icon Bar



**Fig. 4.31:** CoMPASS Time Histogram Icon Bar.

The icons for the time histogram plot are the same as for **The Energy Histogram Icon Bar**, with the exception of the calibration icons which are not available.

In case of Time histogram it is possible to select the x-axis scale choosing among nano, micro and milli seconds.

The histogram range can be defined in **The Spectra Tab** under "Settings" (*Time intervals*).

## The Tof Histogram Icon Bar



**Fig. 4.32:** CoMPASS Tof Histogram Icon Bar.

The icons for the Tof histogram plot are the same as for **The Time Histogram Icon Bar**, with the exception of the cuts, which correspond to the "Correlation Window" under the "Time Correlations" tab.

In case of Tof histogram it is possible to select the x-axis scale choosing among nano, micro and milli seconds.

The histogram range can be defined in **The Spectra Tab** under "Settings" (*Start/stop Δt*).

## The PSD Histogram Icon Bar

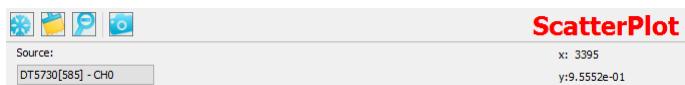


**Fig. 4.33:** CoMPASS PSD Histogram Icon Bar.

The icons for the PSD histogram plot are the same as for **The Energy Histogram Icon Bar**, with the exception of the calibration icons which are not available.

The histogram range can be defined in **The Spectra Tab** under "Settings" (*PSD*).

## The Scatterplot Histogram Icon Bar



**Fig. 4.34:** CoMPASS ScatterPlot Histogram Icon Bar.

Refer to Sec. **The Energy Histogram Icon Bar** for a description of the Scatterplot histogram icons.

The 2D histogram ranges can be defined in **The Spectra Tab** under "Settings" (*2D Energy/2D PSD*).

## 5 Technical Support

CAEN makes available the technical support of its specialists at the e-mail addresses below:

**support.nuclear@caen.it**  
(for questions about the hardware)

**support.computing@caen.it**  
(for questions about software and libraries)



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**CAEN S.p.A.**  
Via Vetraia, 11  
55049 Viareggio  
Italy  
Tel. +39.0584.388.398  
Fax +39.0584.388.959  
[info@caen.it](mailto:info@caen.it)  
[www.caen.it](http://www.caen.it)

**CAEN GmbH**  
Eckehardweg 10  
42653 Solingen  
Germany  
Tel. +49.212.2544077  
Mobile +49(0)15116548484  
Fax +49.212.2544079  
[info@caen-de.com](mailto:info@caen-de.com)  
[www.caen-de.com](http://www.caen-de.com)

**CAEN Technologies, Inc.**  
1140 Bay Street - Suite 2 C  
Staten Island, NY 10305  
USA  
Tel. +1.718.981.0401  
Fax +1.718.556.9185  
[info@caentechnologies.com](mailto:info@caentechnologies.com)  
[www.caentechnologies.com](http://www.caentechnologies.com)

