

TFE4188 - Lecture 3

# Reference and bias

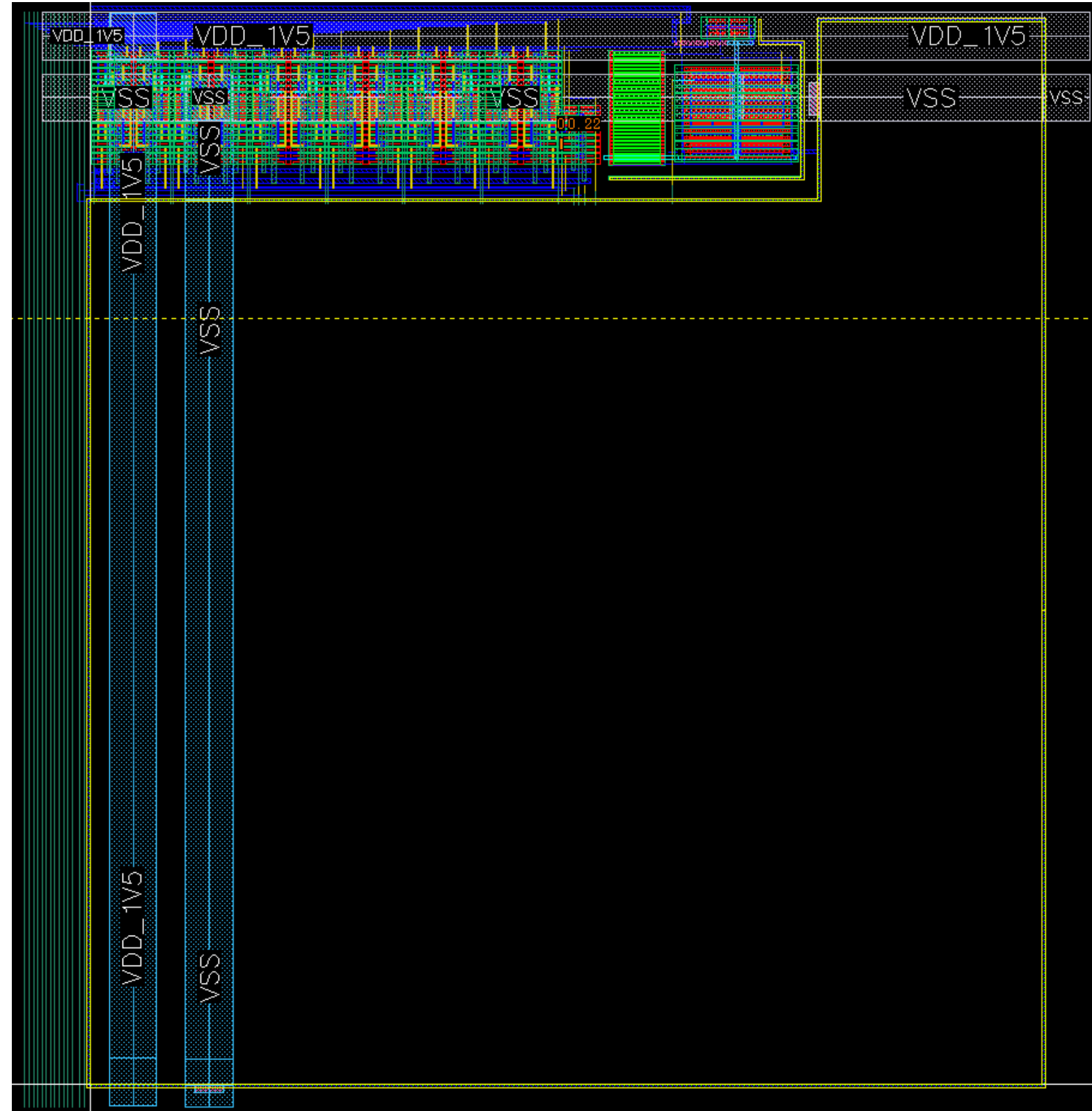
# Housekeeping

Syllabus on <https://github.com/wulffern/aic2022/blob/main/syllabus.md>

Area of your design is constrained by SUN\_AS\_WRAP. You must all use that cell!

Specification review next week, you must follow the [Spec checklist](#)

Grading of the project includes the specification review



# Grading of the project

Created by Carsten Wulff, last modified on 17.01.2022

The project counts for 45 % of the grade

Milestones	What does it mean	Checklist	Output	Points
M1 Specification	<ul style="list-style-type: none"><li>Plan of what the circuit is going to do, and roughly how it's going to be implemented</li><li>Plan of how you're going to verify functionality</li></ul>	Specifcation Review	Confluence	10
M2 Design review	<ul style="list-style-type: none"><li>Prove functionality and performance with schematic simulation</li></ul>	Design Review	Confluence Schematic	10
M3 Layout review	<ul style="list-style-type: none"><li>Placement, most blocks layed out</li></ul>	Layout Review	Confluence Schematic Layout	10
M4 Tapeout review	<ul style="list-style-type: none"><li>LVS/DRC clean. Prove functionality and performance with parasitic extracted simulation</li></ul>	Tapeout Review	Confluence	20
Paper  Design complexity / Good design descisions	<ul style="list-style-type: none"><li>Write a paper describing your circuit.</li><li>Your paper should look like <a href="https://ieeexplore.ieee.org/document/7906479">https://ieeexplore.ieee.org/document/7906479</a> The source code is available <a href="https://github.com/wulffern/jssc2017">https://github.com/wulffern/jssc2017</a></li><li>You must use the IEEEtran.cls</li><li>Submitted manuscripts, describing both the theoretical and implementation aspects of an advance solid-state circuit design, are allowed to have up to 8 pages in the two-column format. This page limit is valid for the whole manuscript, but excluding references and bios. All figures must be sized such that they are properly readable. No modifications to the IEEE templates are allowed.</li></ul>		PDF submission on blackboard	50
Coolness factor	These are extra points.			10
Max points				100

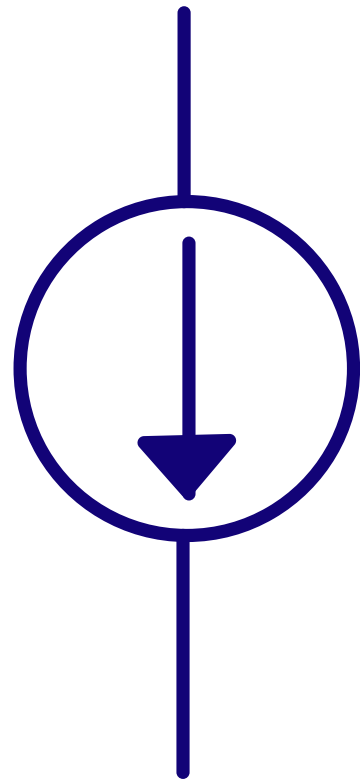
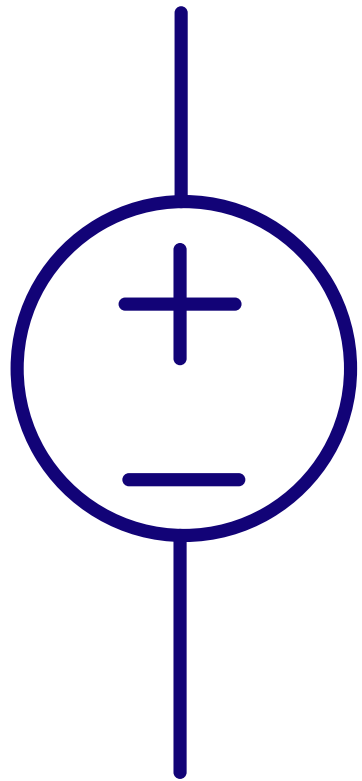
Week	Book	Monday	Project plan	Exercise
2	CJM 1-6	Course intro, what I expect you to know, project, analog design fundamentals	Specification	
3	Slides	ESD and IC Input/Output	Specification	x
4	CJM 7,8	<b>Reference and bias</b>	Specification	
5	CJM 12	Analog Front-end	M1. Specification review	x
6	CJM 11-14	Switched capacitor circuits	Design	
7	JSSC, CJM 18	State-of-the-art ADCs	Design	x
8	Slides	Low power radio receivers	Design	
9	Slides	Communication standards from circuit perspective	M2. Design review	x
10	CJM 7.4, CFAS,+DC/DC	Voltage regulation	Layout	
11	CJM 19, CFAS	Clock generation	M3. Layout review	x
12	Paper	Energy sources	Layout/LPE simulation	
13	Slides	Chip infrastructure	Layout/LPE simulation	x
14		Tapeout review	M4. Tapeout review	
15		Easter		
16		Easter		
17		Exam repetition		

# Goal for today

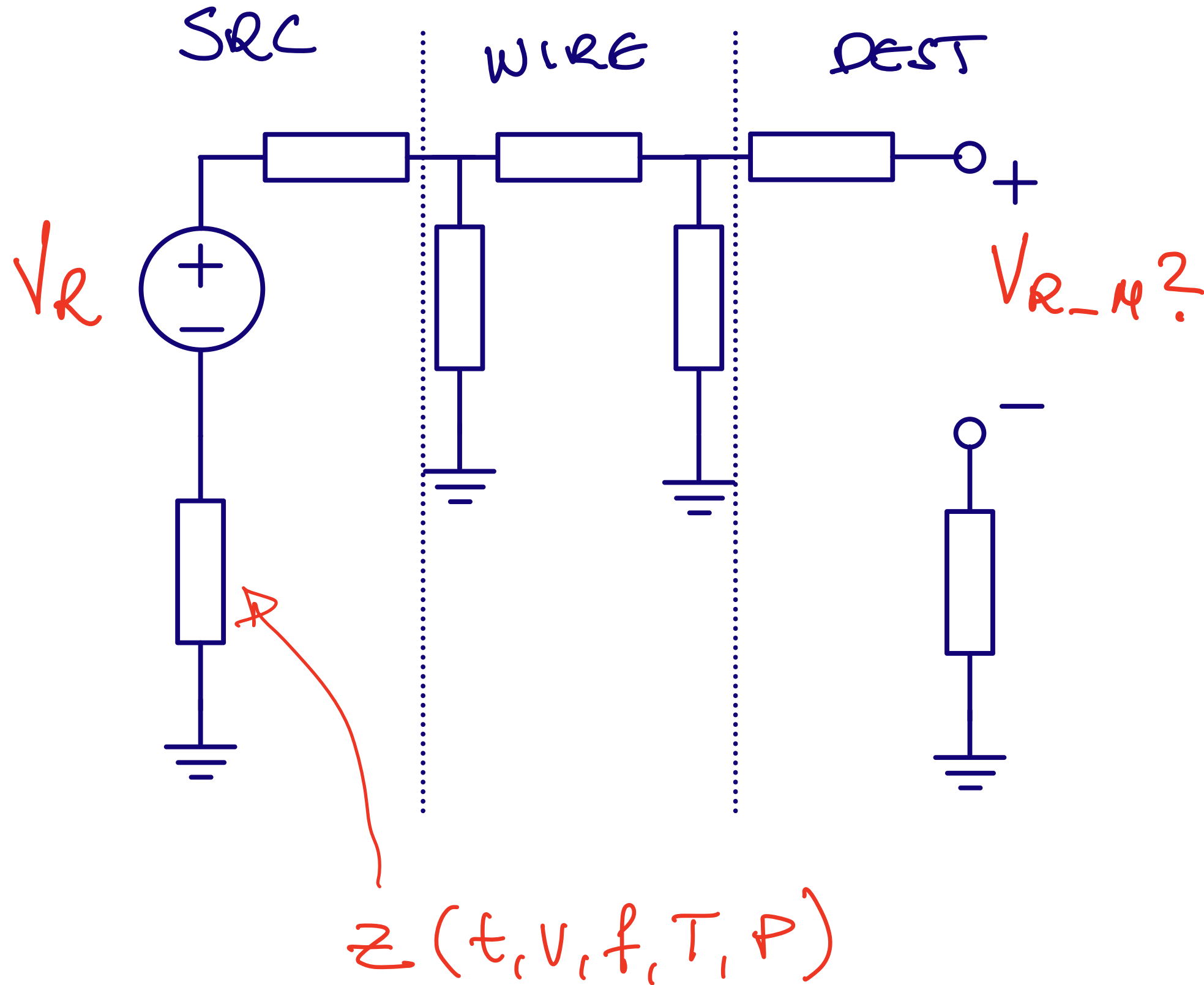
Understand **why** we need reference and bias circuits

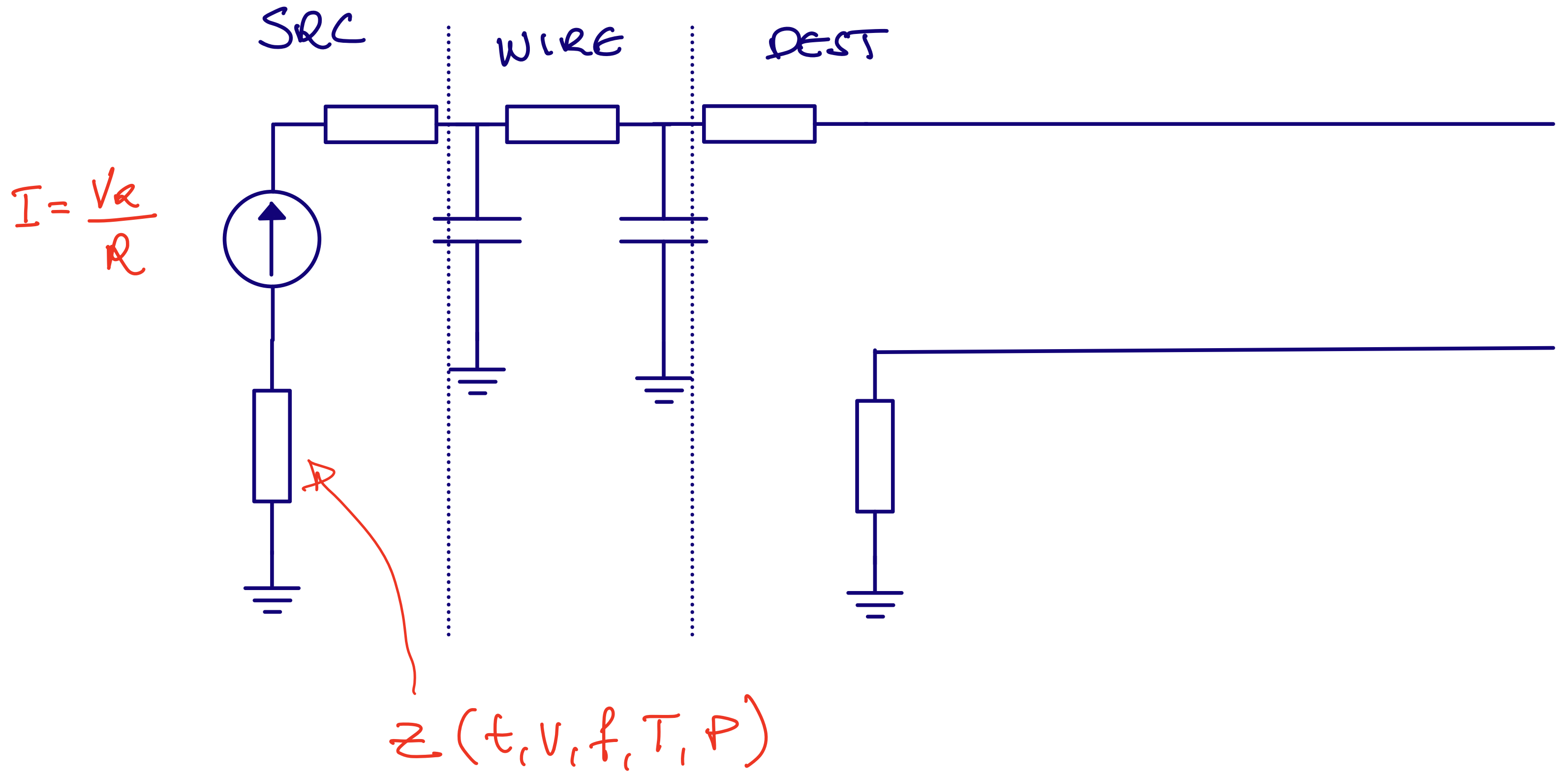
Introduction to **circuit architectures**

**Why**







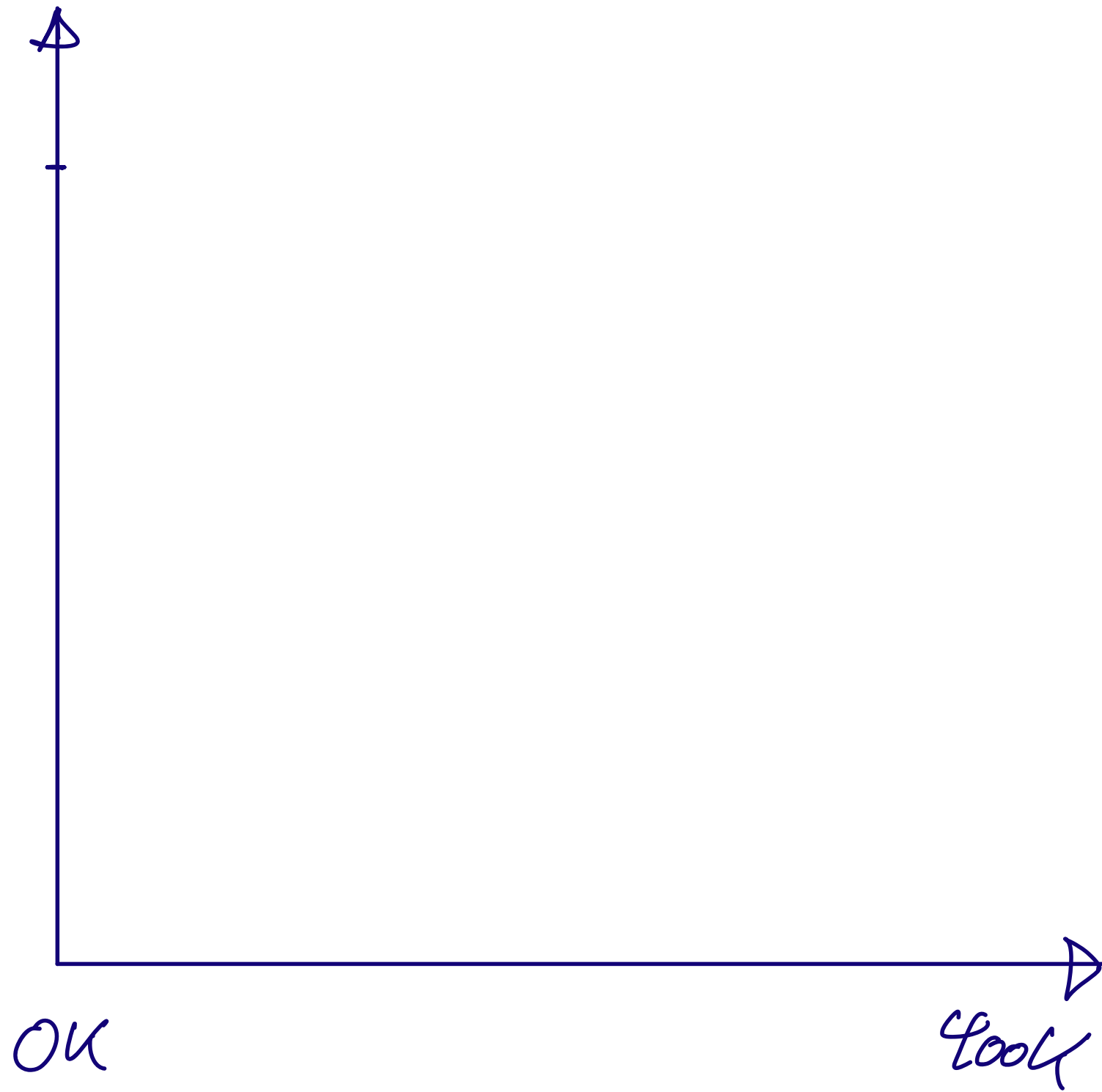
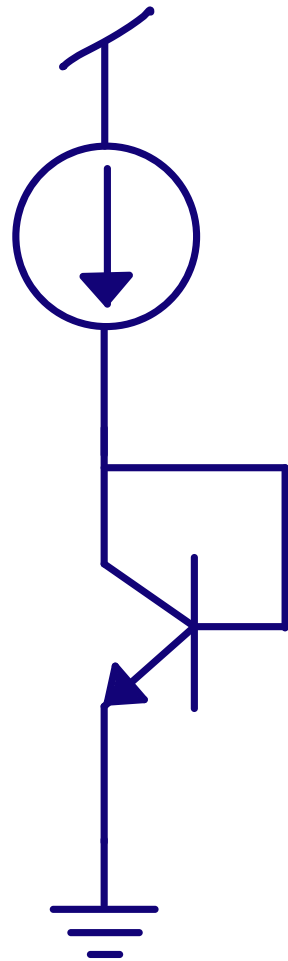


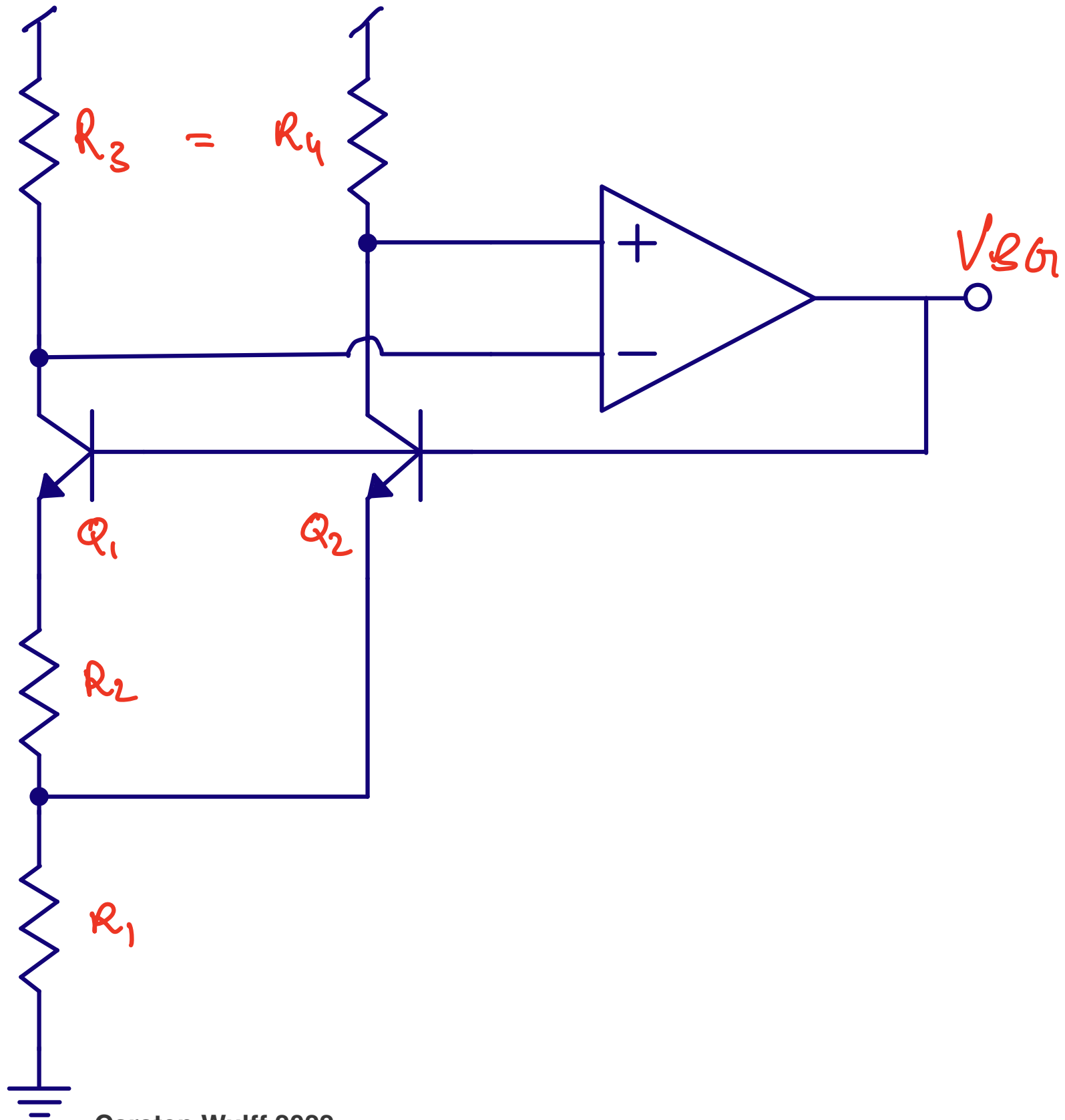


What quantity do we have  
access to on an IC that is  
independent of PVT?

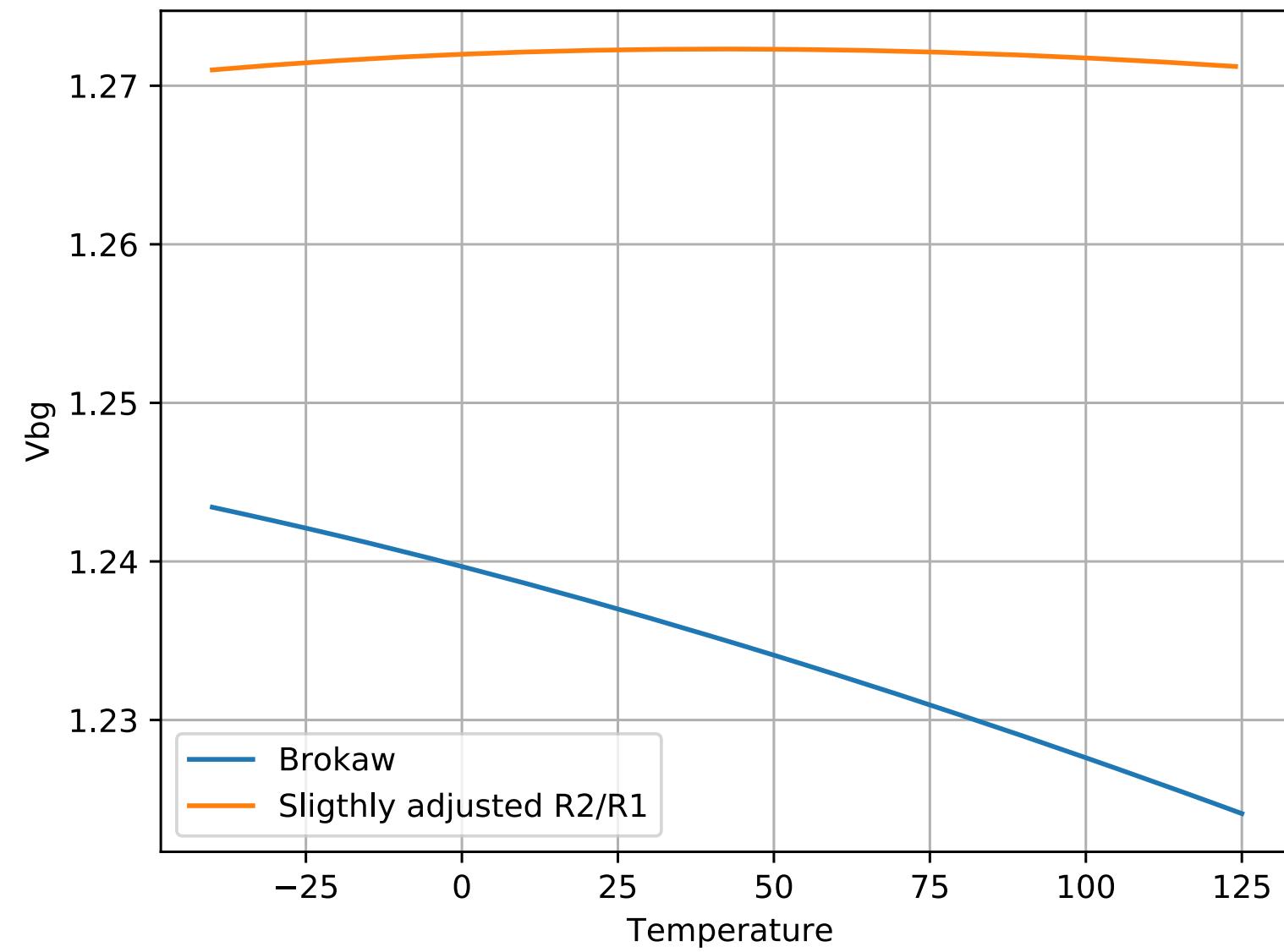
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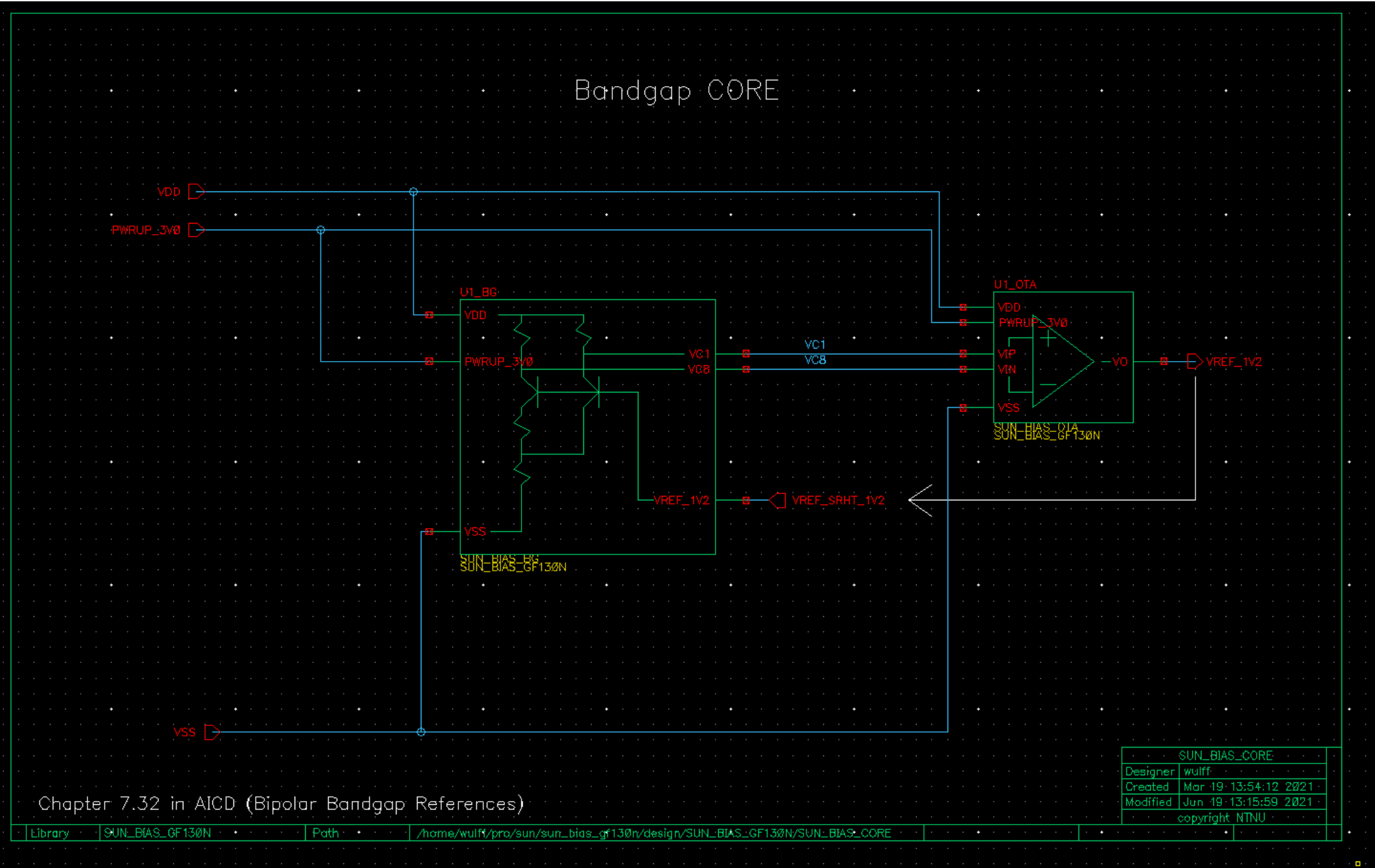
# Bandgap voltage reference



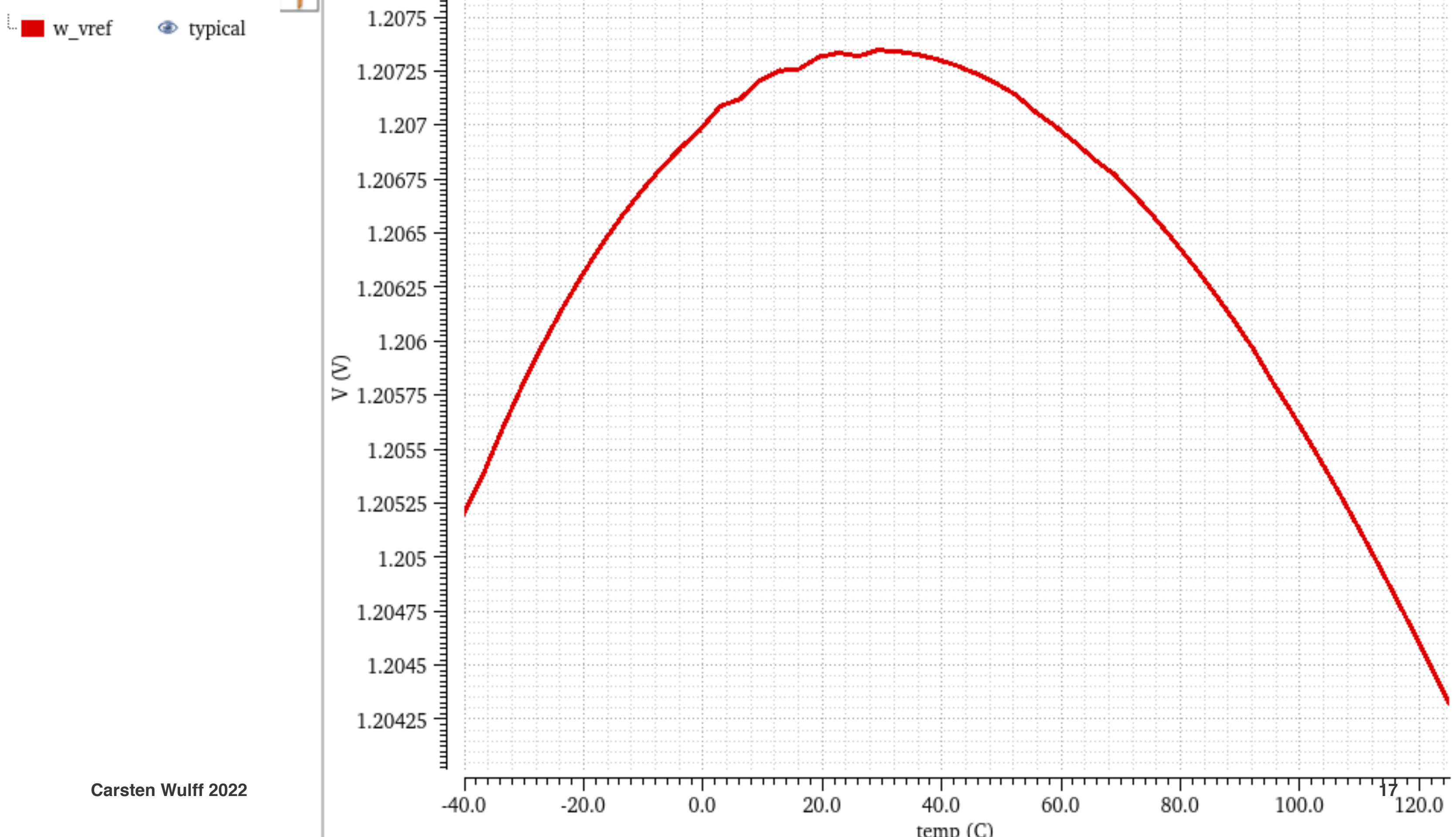


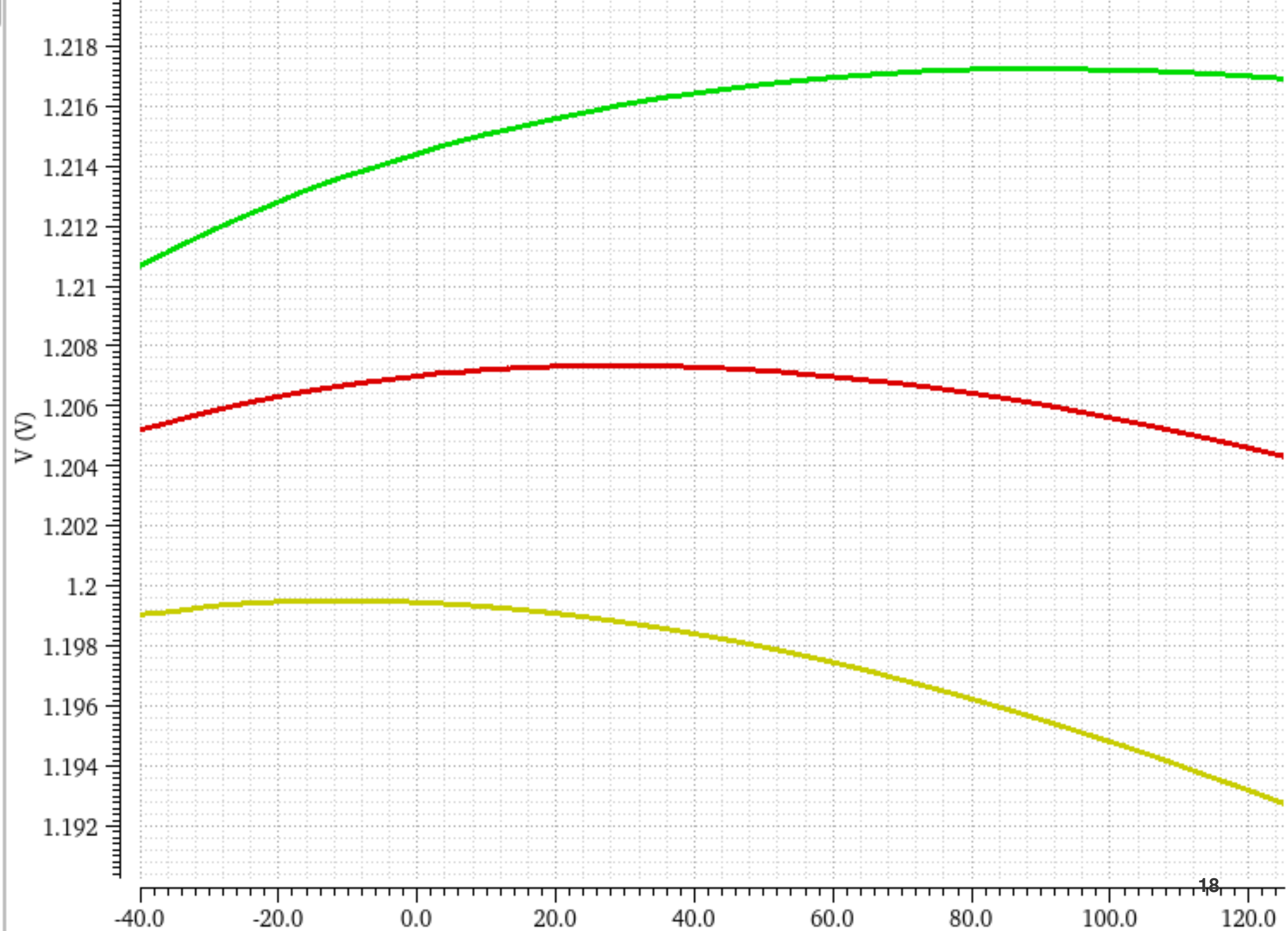
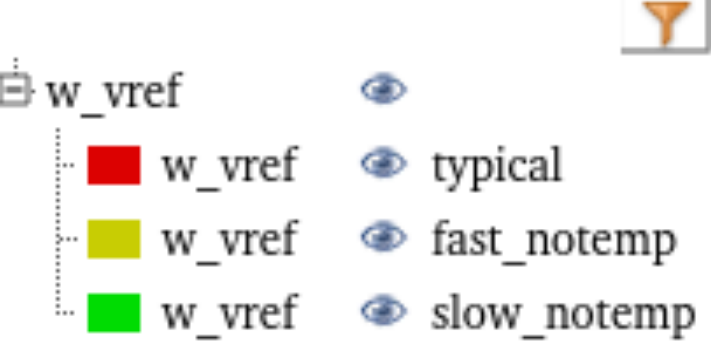
sun/sun\_bias\_gf130n/go/

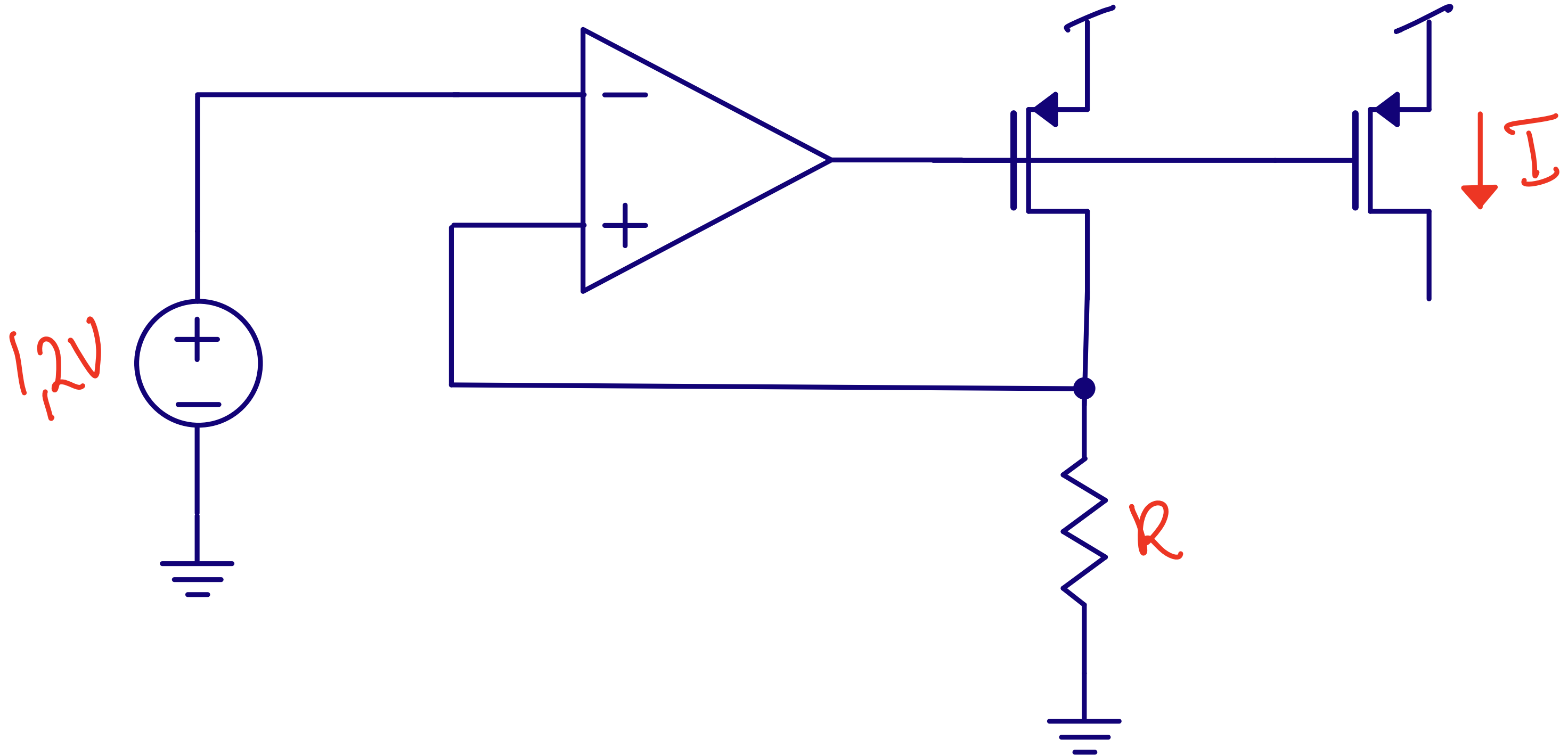




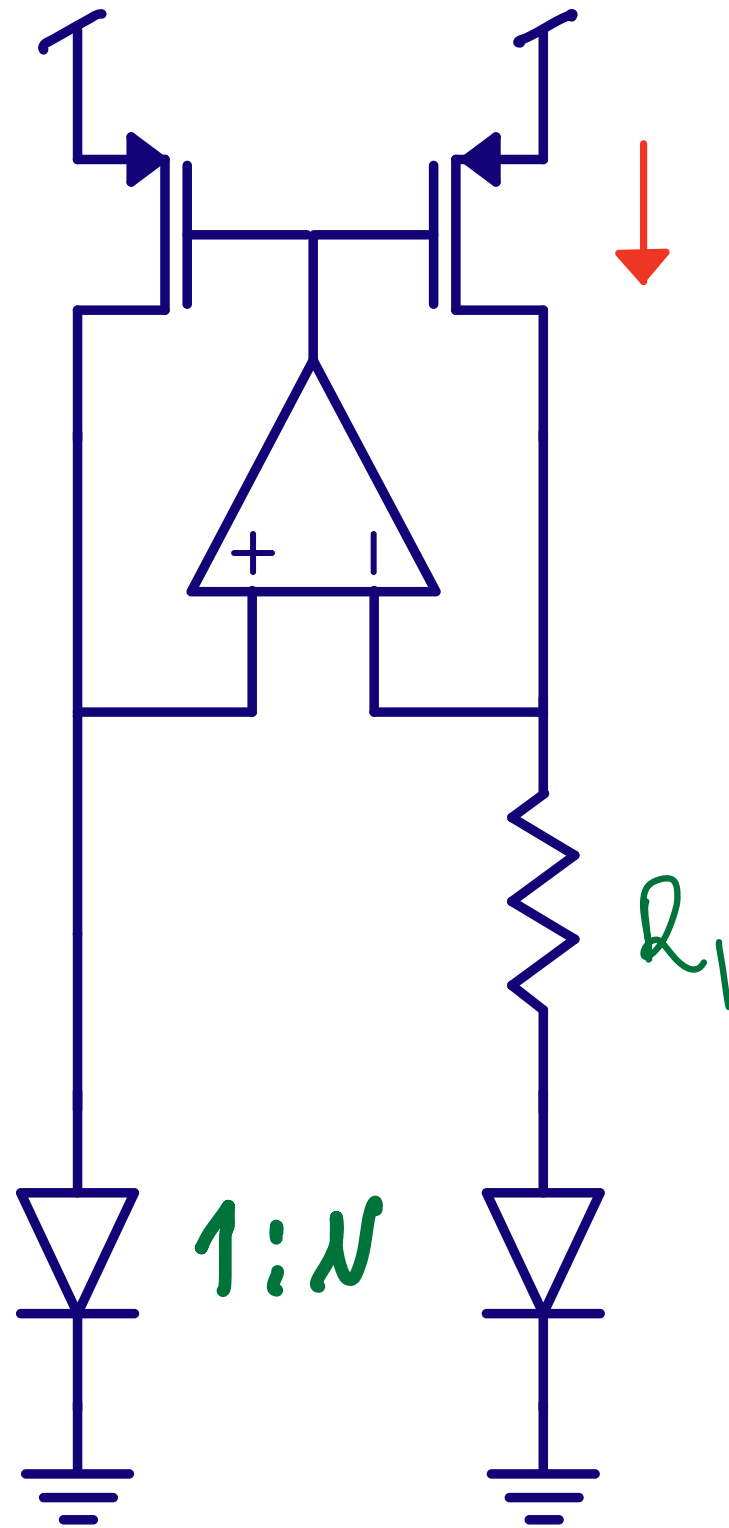


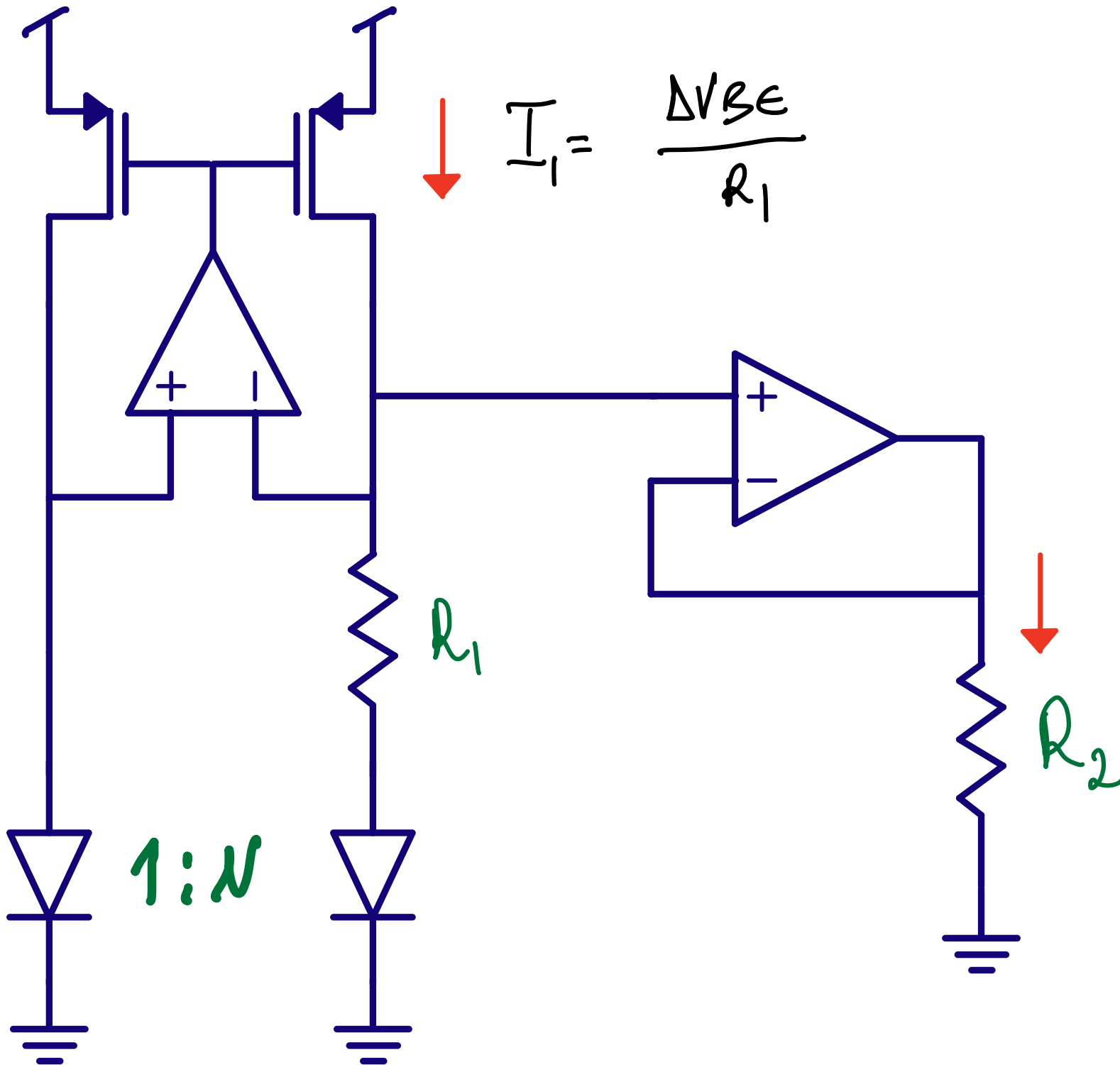


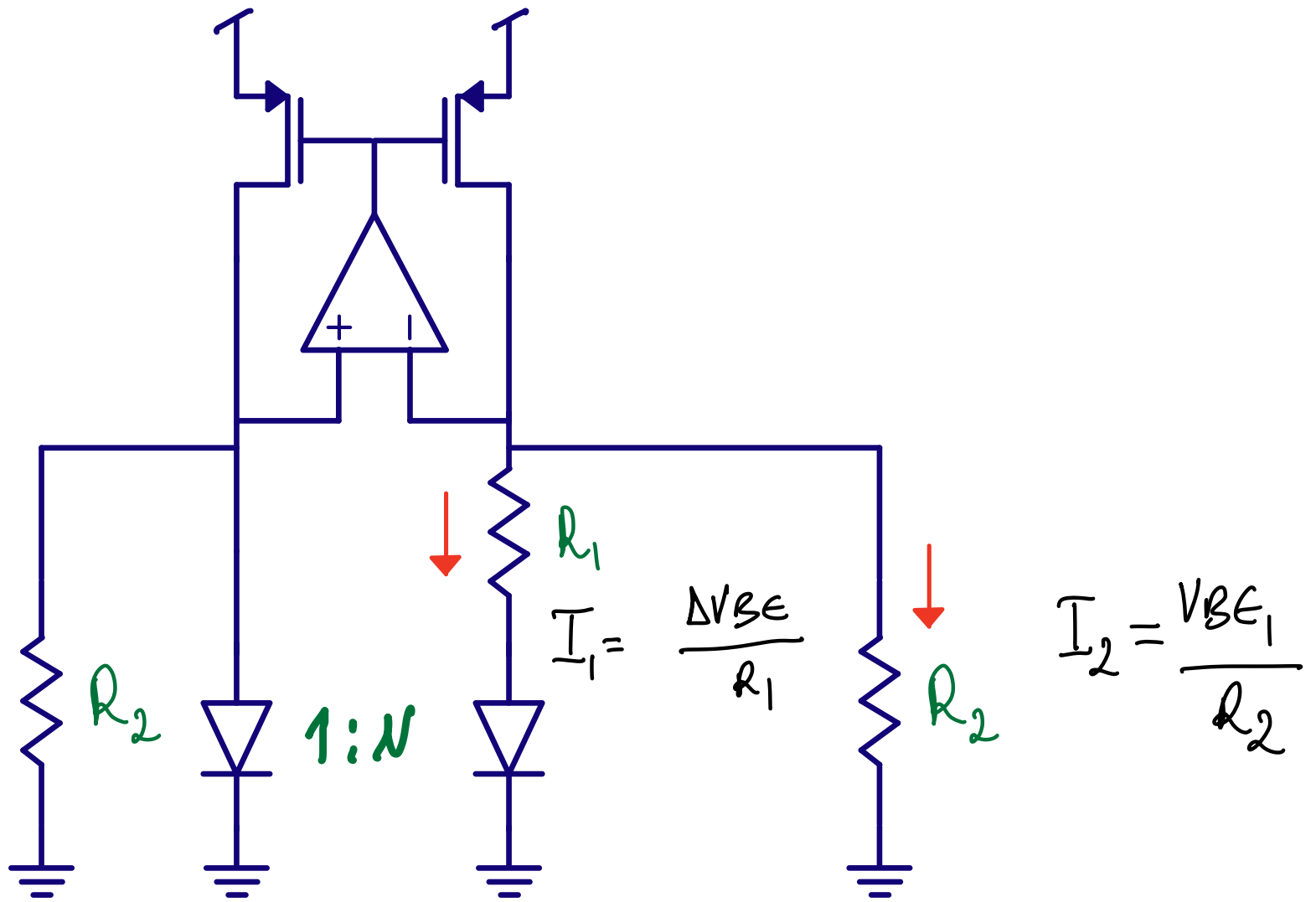


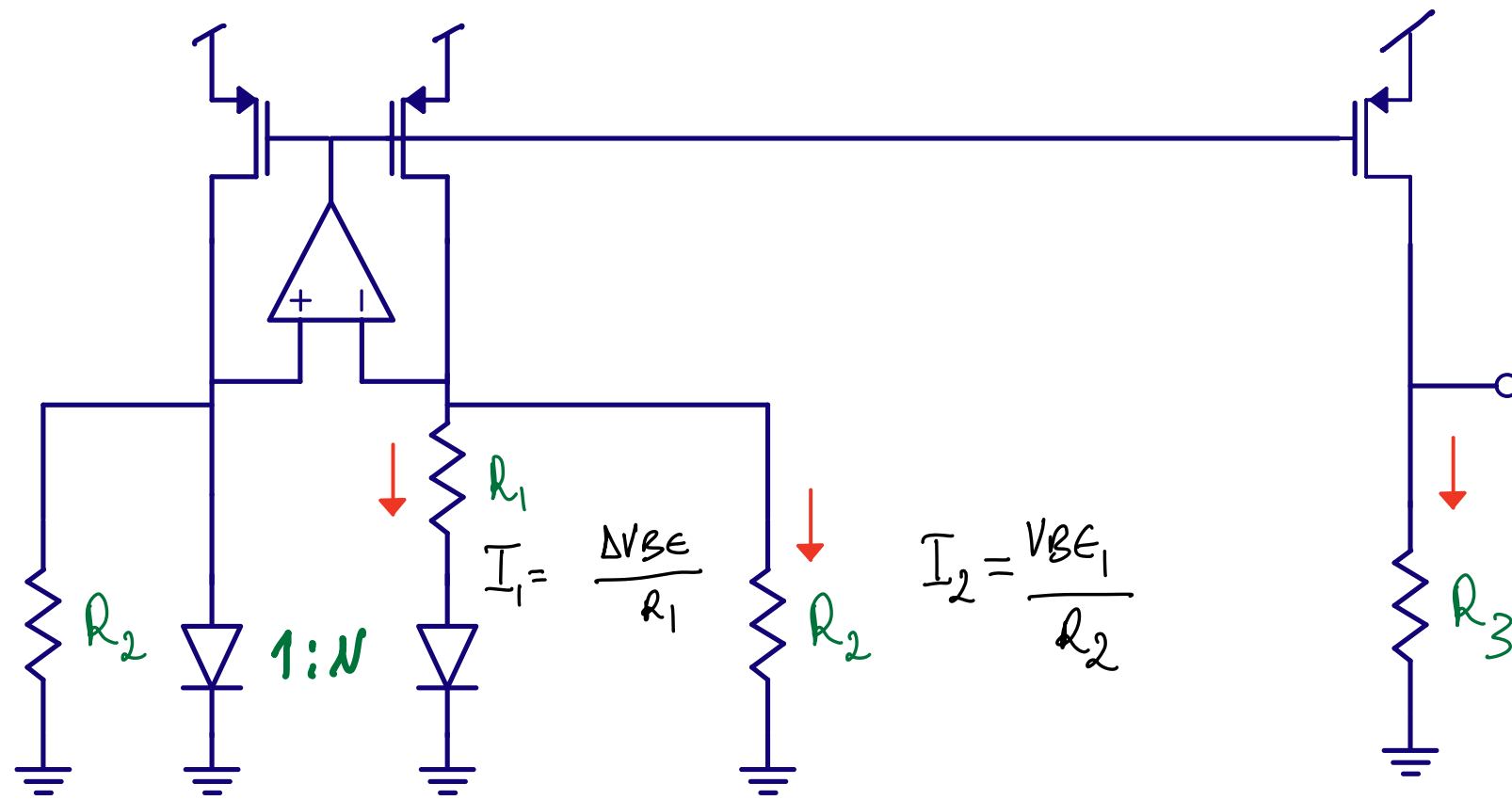


# Low voltage bandgap





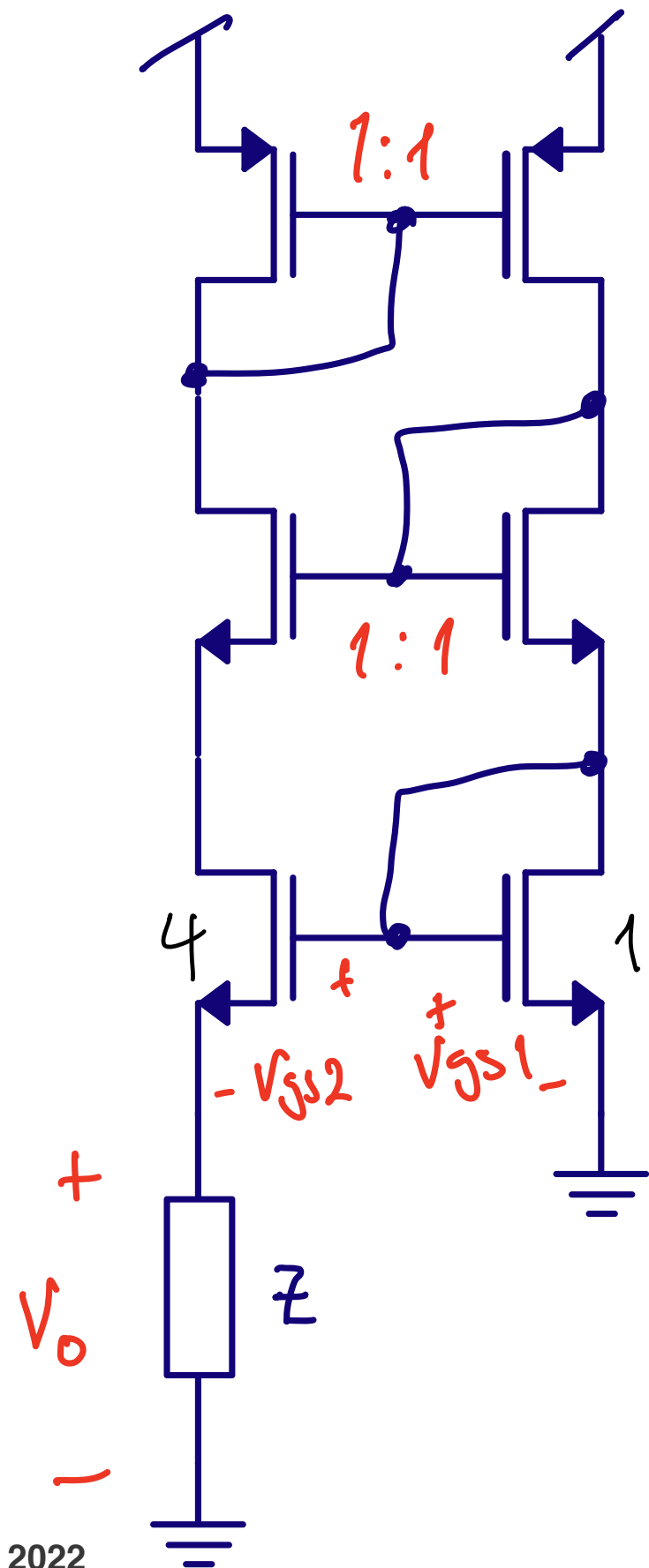


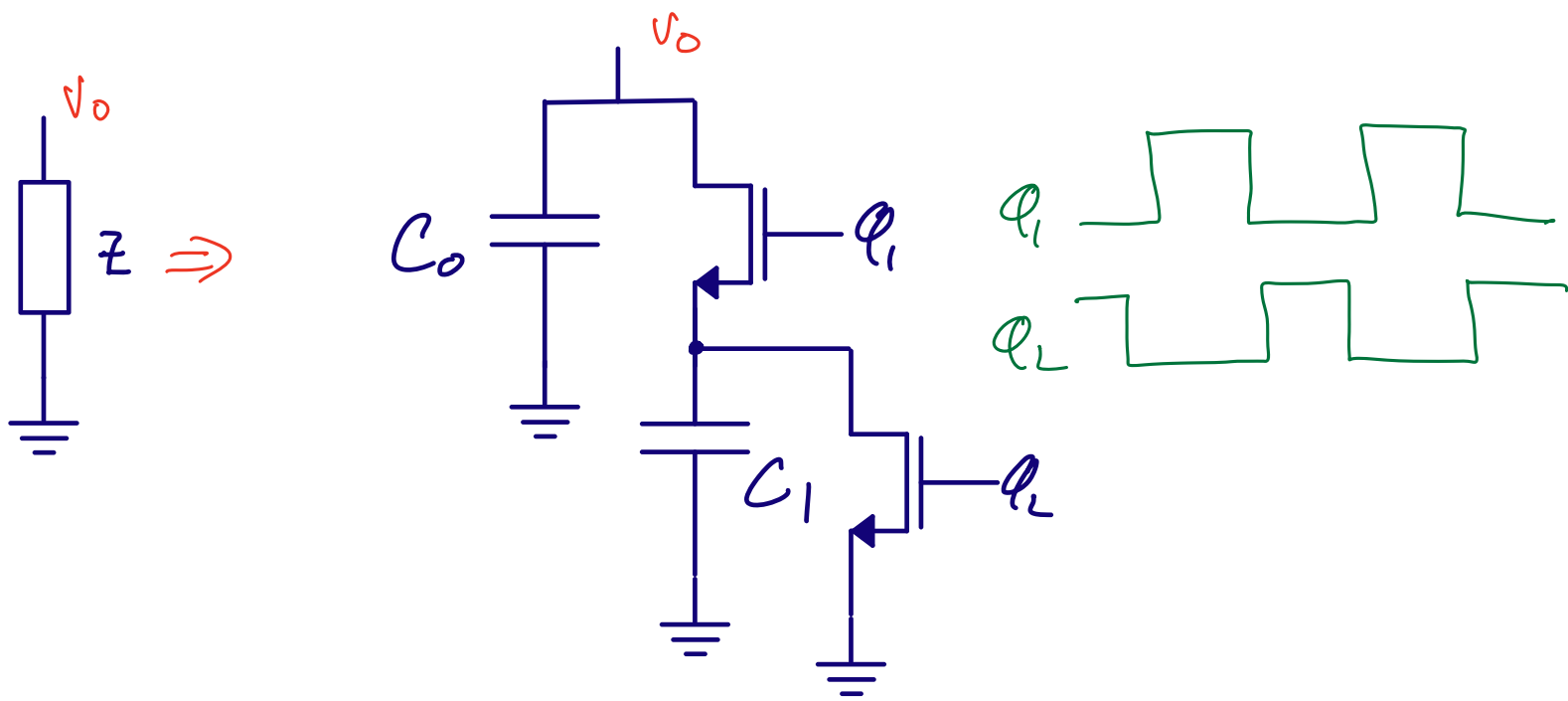




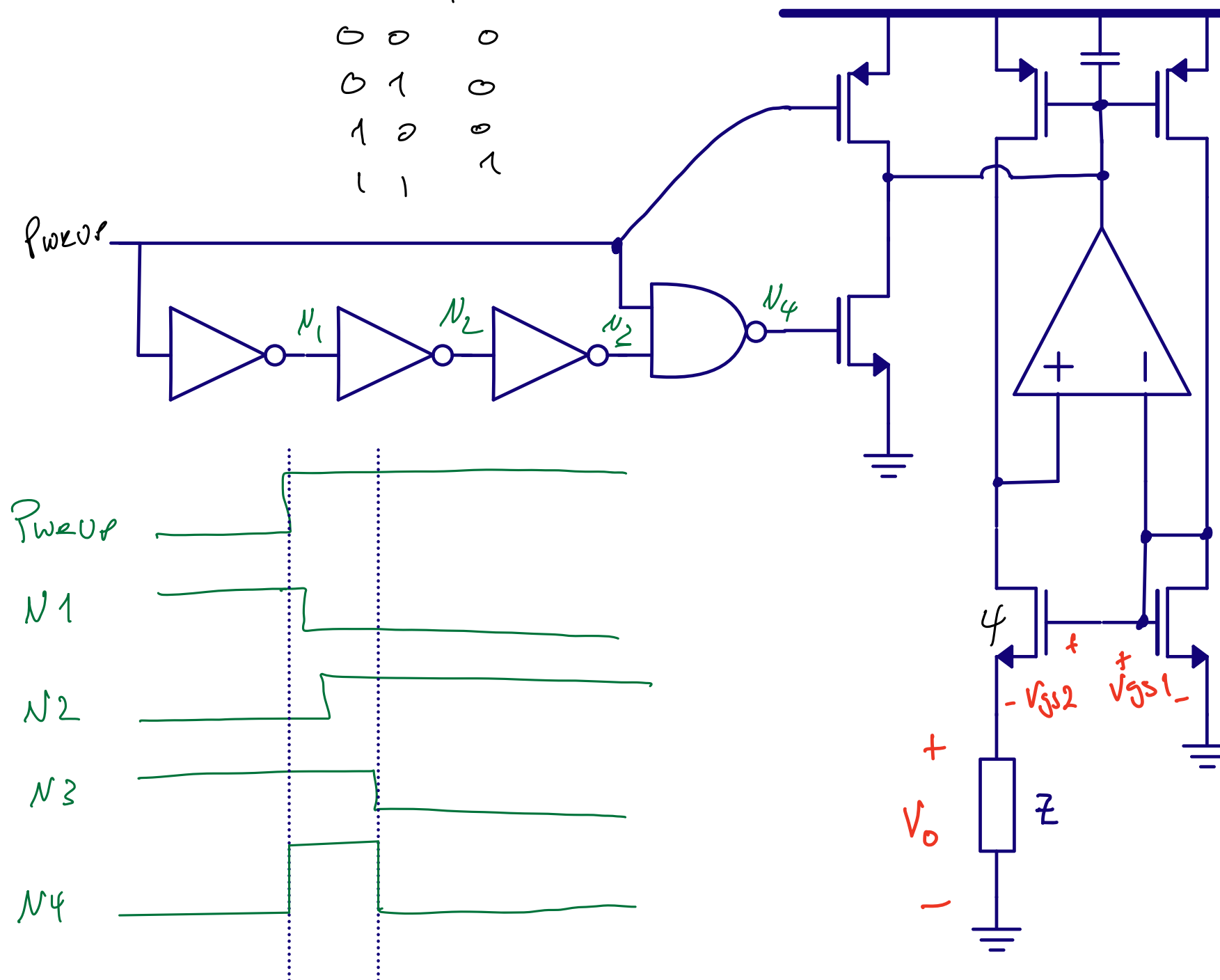
# Bias

Sometimes we just need a current





A	B	NOZ
0	0	0
0	1	0
1	0	0
1	1	1



# Thanks!

