TFE4188 - Lecture 5

Switched-Capacitor Circuits

Housekeeping

Added "Continuous-time analog filters in nano-scale CMOS, challenges and opportunities" video to Lecture 4

Added Lecture 6 papers. Read them until next time.

Lecture in week 8 will be digital

No-one is showing up to the physical exercise hours, so we go digital

Week	Book	Monday	Project plan	Exercise
2	CJM 1-6	Course intro, what I expect you to know, project, analog design fundamentals	Specification	
3	Slides	ESD and IC Input/Output	Specification	x
4	CJM 7,8	Reference and bias	Specification	
5	CJM 12	Analog Front-end	M1. Specification review	x
6	CJM 11-14	**Switched capacitor circuits**	Design	
7	JSSC, CJM 18	State-of-the-art ADCs	Design	x
8	Slides	Low power radio recievers	Design	
9	Slides	Communication standards from circuit perspective	M2. Design review	x
10	CJM 7.4, CFAS,+DC/DC	Voltage regulation	Layout	
11	CJM 19, CFAS	Clock generation	M3. Layout review	x
12	Paper	Energy sources	Layout/LPE simulation	
13	Slides	Chip infrastructure	Layout/LPE simulation	x
14		Tapeout review	M4. Tapeout review	
15		Easter		
16		Easter		
17		Exam repetition		

Goal for today

Understand **why** would use switched capacitor circuits

Introduction to **discrete-time**, and **switched capacitor**

Why

Active-RC

$$\omega_{p|z} \propto \frac{1}{RC}$$

Gm-C

$$\omega_{p|z} \propto \frac{G_m}{C}$$

$$\omega_{p|z} \propto \frac{C_1}{C_2}$$

A pipelined 5-Msample/s 9-bit analog-to-digital converter

Good common-mode rejection

Precise gain

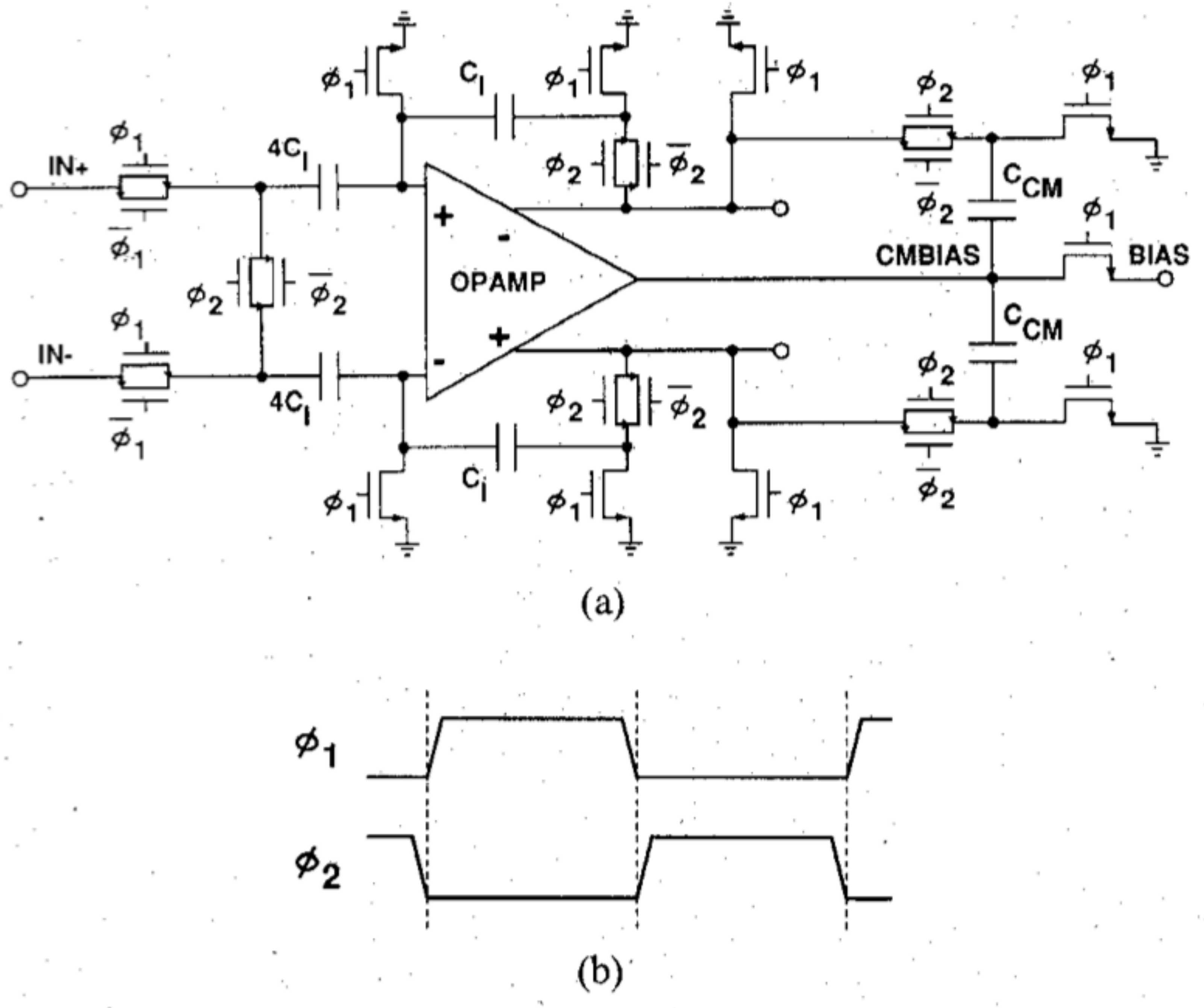


Fig. 6. (a) Schematic of S/H amplifier. (b) Timing diagram of a two-phase nonoverlapping clock.

Nano-scale CMOS

Advantage

Switches become smaller (less charge injection)

Capacitors become more dense

Challenge

High-gain OTA's (tricky to get 100 dB open loop gain)

Discrete-Time Signals

Define x_c as a continuous time signal, continuous value signal

Define $\ell(t) = \begin{cases} 1 & \text{if } t \geq 0 \\ 0 & \text{if } t < 0 \end{cases}$

Define

$$x_{sn}(t) = \frac{x_c(nT)}{\tau}\left[\ell(t - nT) - \ell(t - nT - \tau)\right]$$

Define $x_s(t) = \sum_{n=-\infty}^{\infty} x_{sn}(t)$

A sampled signal of an analog signal you can think of it as an infinite sum of pulse trains where the area under the pulse train is equal to the analog signal.

Why do this?

If $x_s(t) = \sum_{n=-\infty}^{\infty} x_{sn}(t)$

Then $X_{sn}(s) = \frac{1}{\tau}\frac{1 - e^{-s\tau}}{s}x_c(nT)e^{-snT}$

And $X_s(s) = \frac{1}{\tau}\frac{1 - e^{-s\tau}}{s} \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT}$

Thus $\lim_{\tau \to 0} \to X_s(s) = \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT}$

Or $X_s(j\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X_c\left(j\omega - \frac{jk2\pi}{T}\right)$

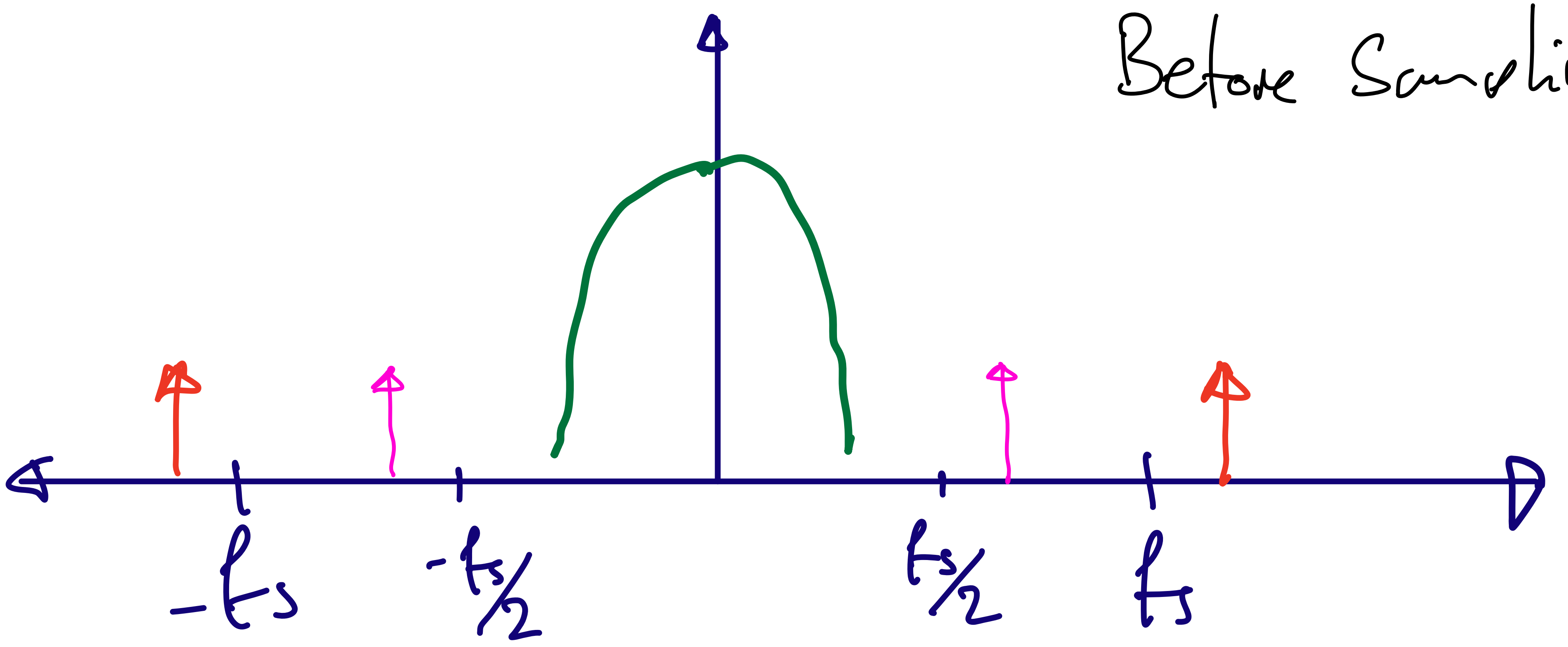
The spectrum of a sampled signal is an infinite sum of frequency shifted spectra

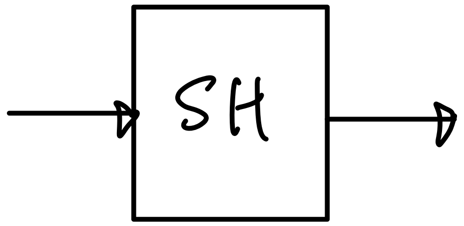
or equivalenty

When you sample a signal, then there will be copies of the input spectrum at every nf_s

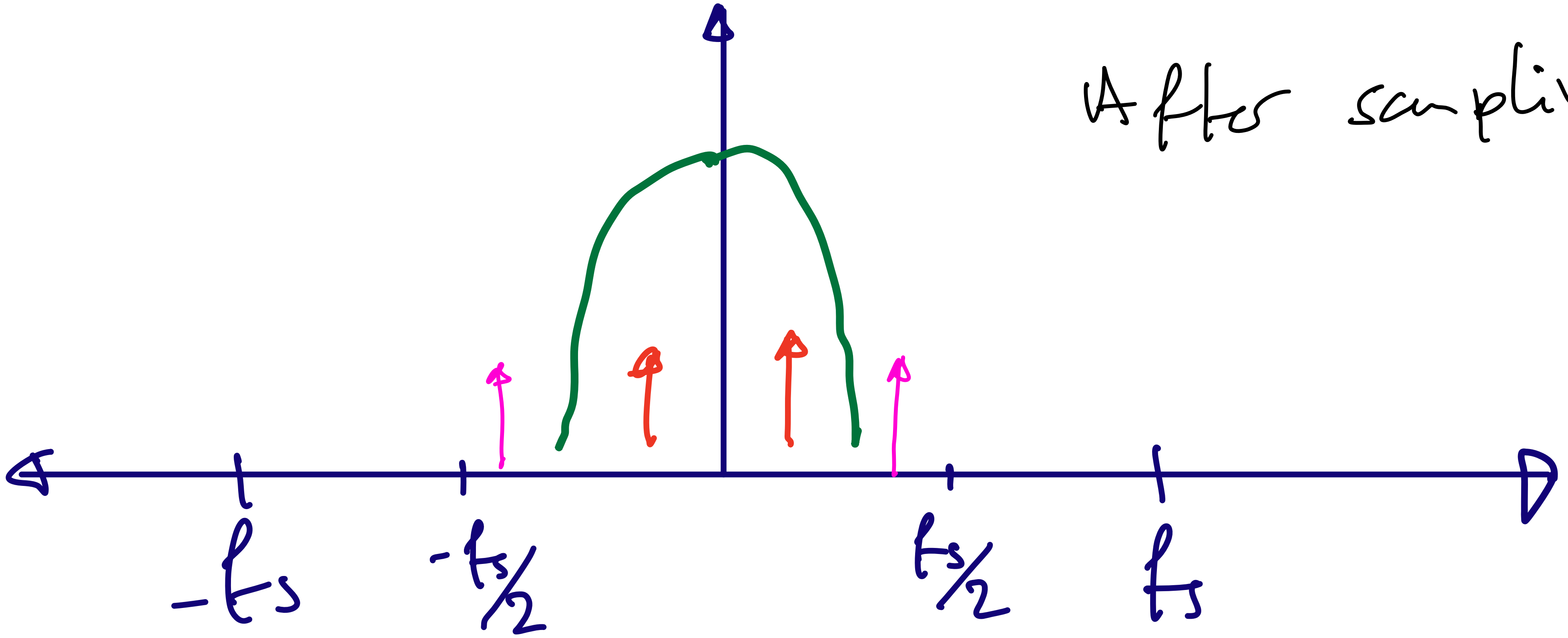
However, if you do an FFT of a sampled signal, then all those infinite spectra will fold down between $0 \to f_s/2$ or $-f_s/2 \to f_s/2$ for a complex FFT

Before Sampling

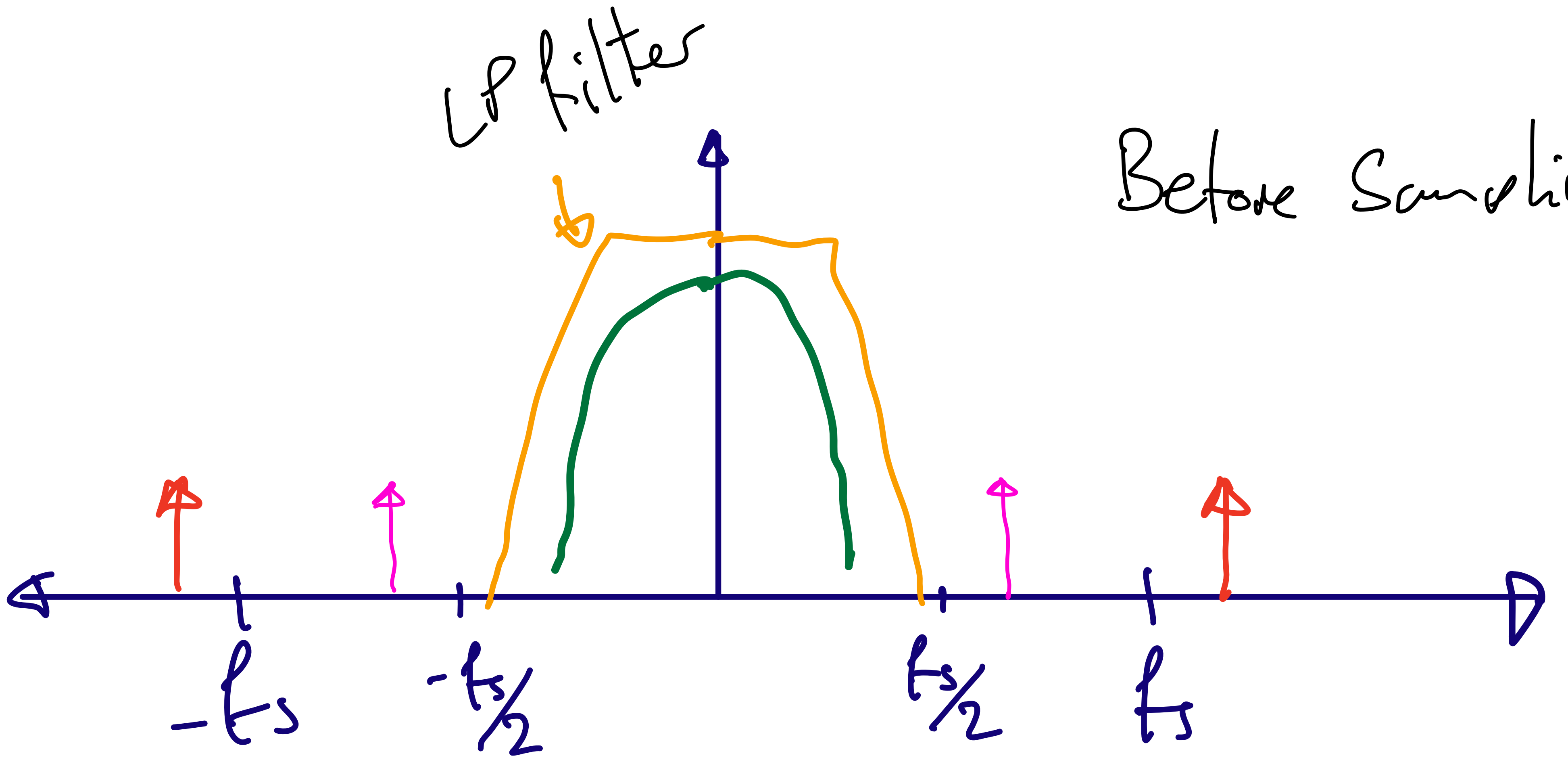




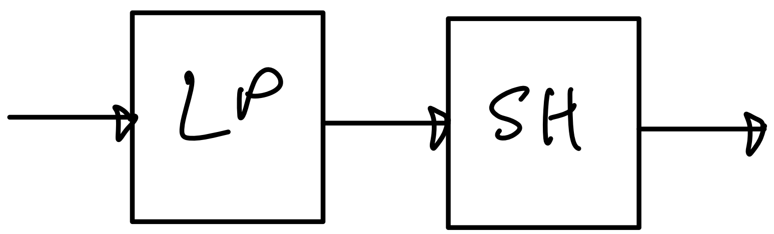
After sampling



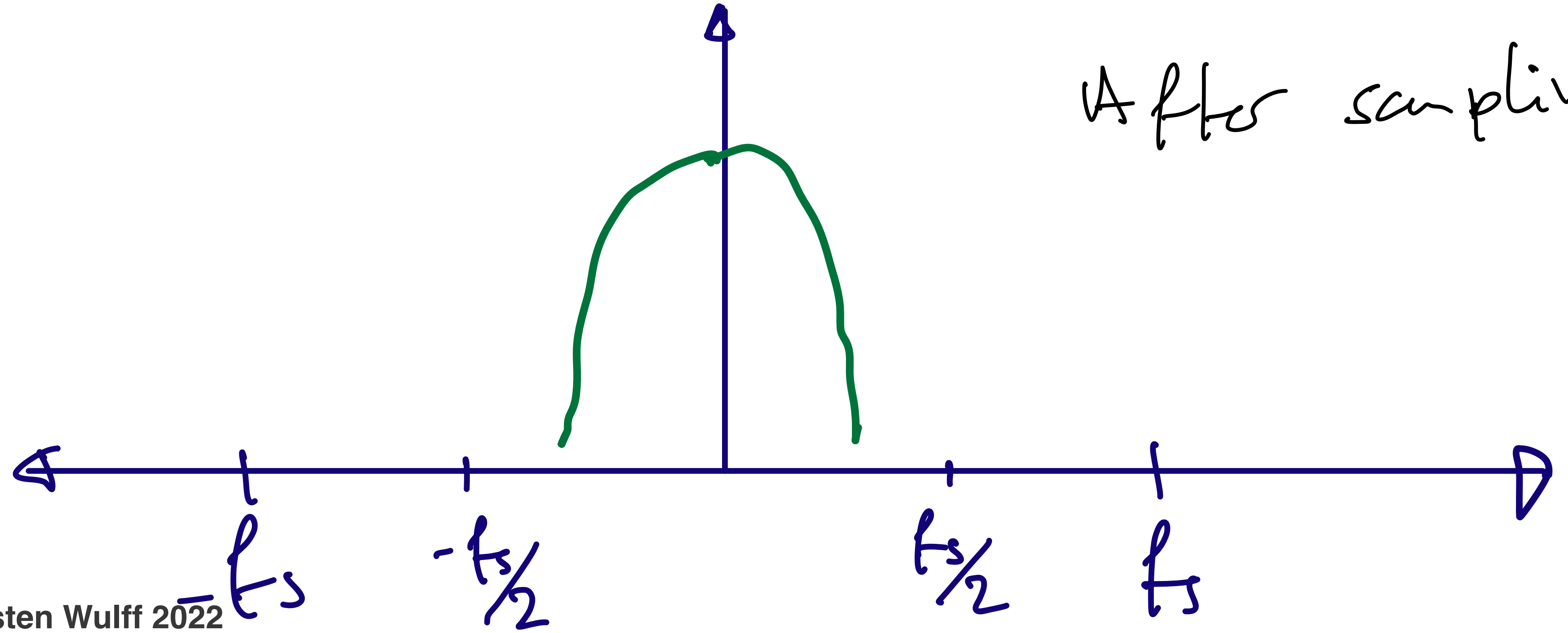
Before Sampling



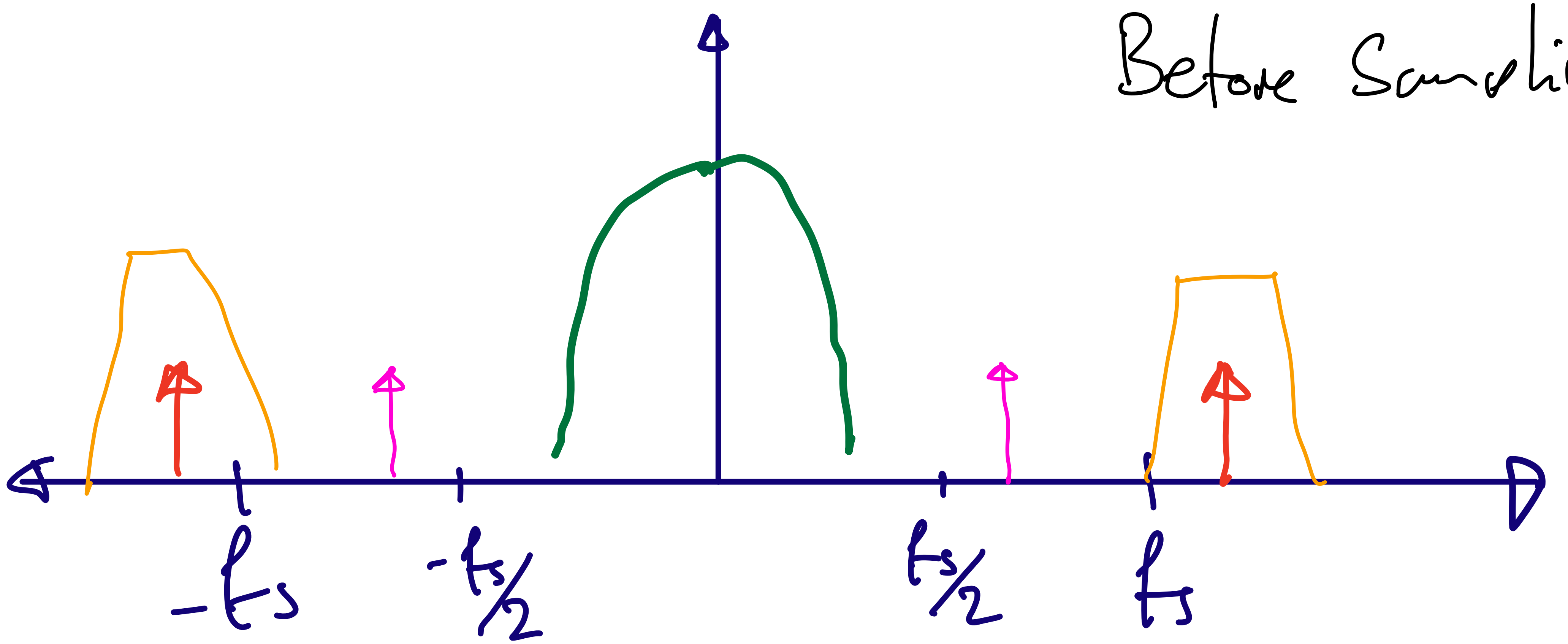
Anti-Alias

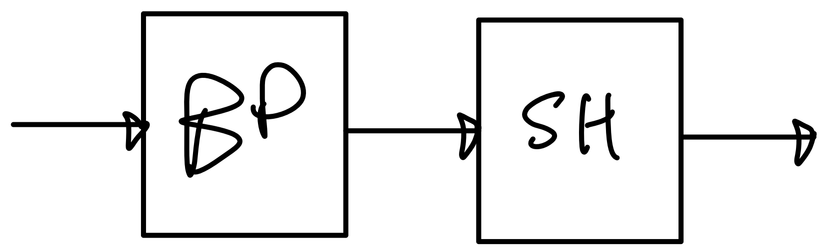


After sampling

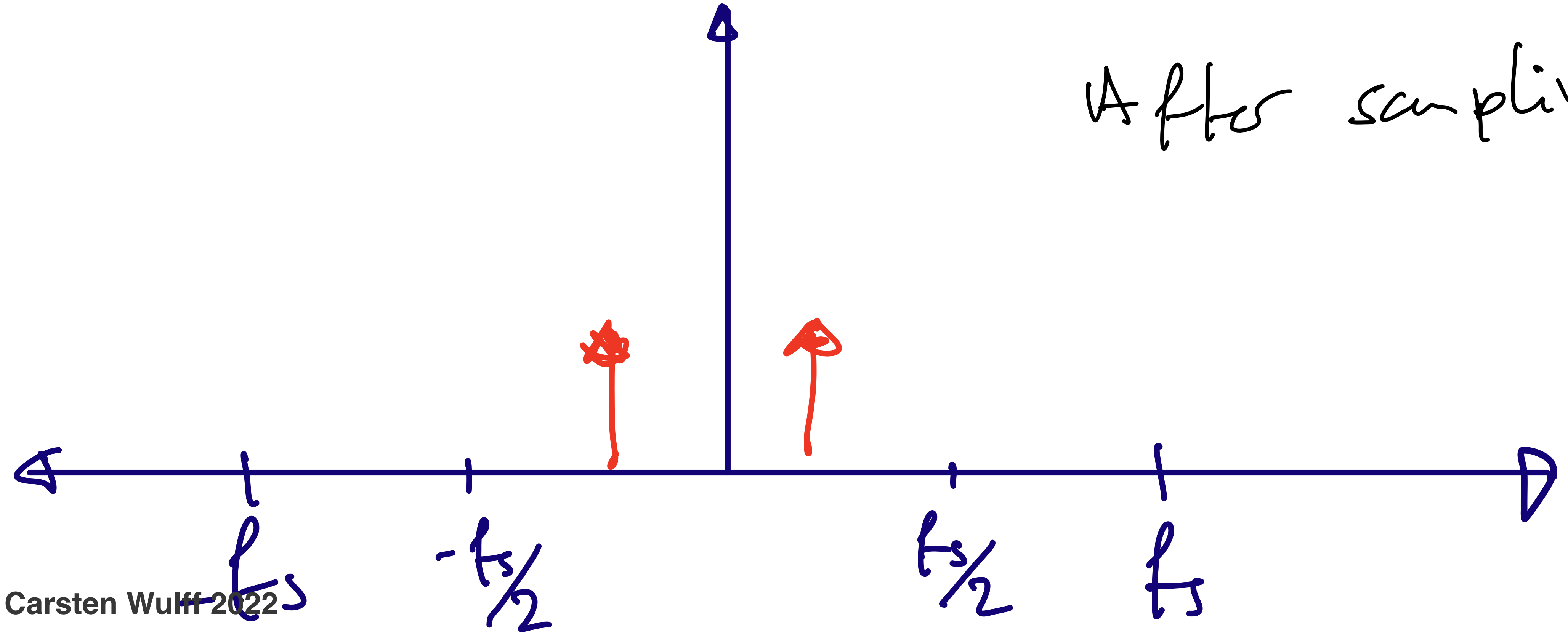


Before Sampling





After sampling

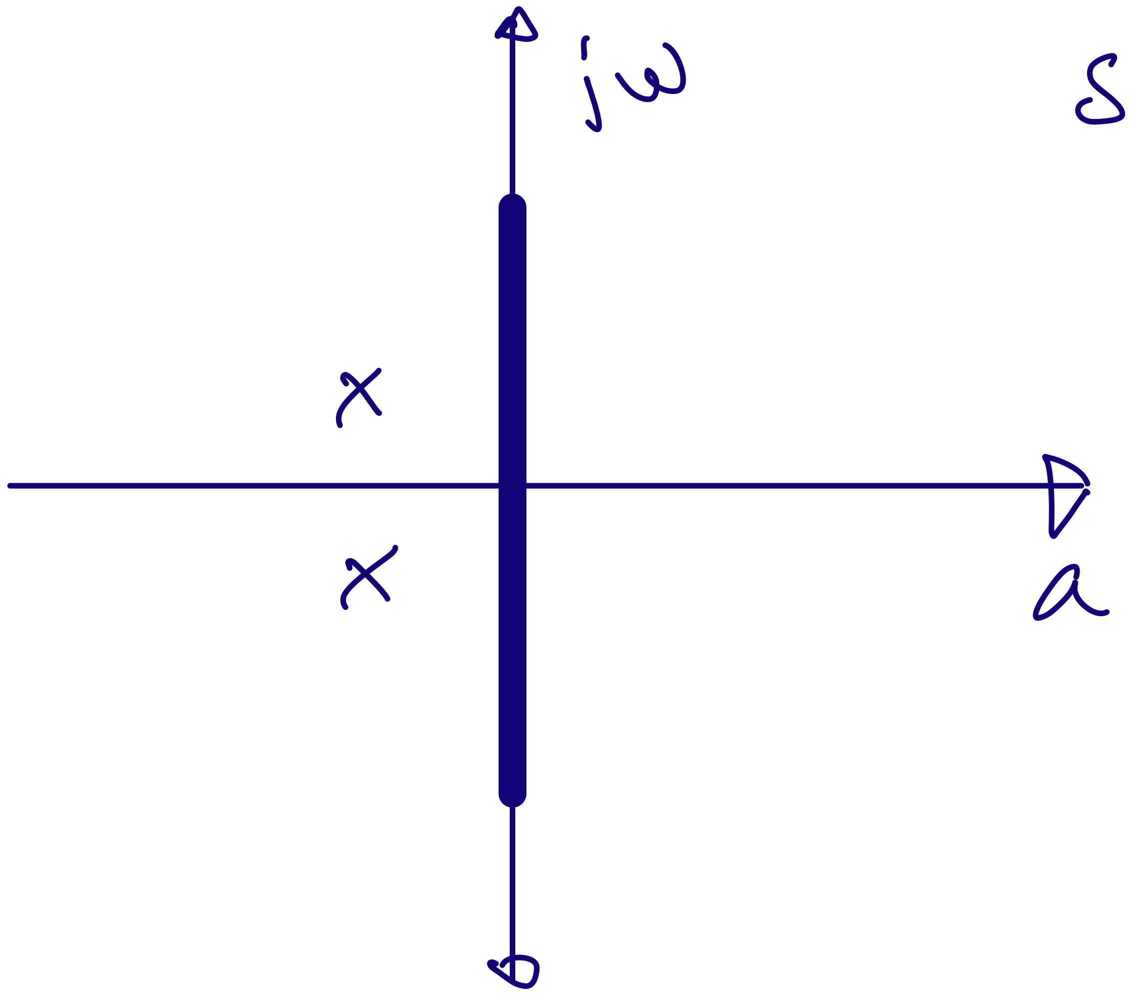


$$X_s(s) = \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT}$$

$$X_s(z) = \sum_{n=-\infty}^{\infty} x_c[n]z^{-n}$$

For discrete time signal processing we use Z-transform

If you're unfamiliar with the Z-transform, read the book or search https://en.wikipedia.org/wiki/Z-transform



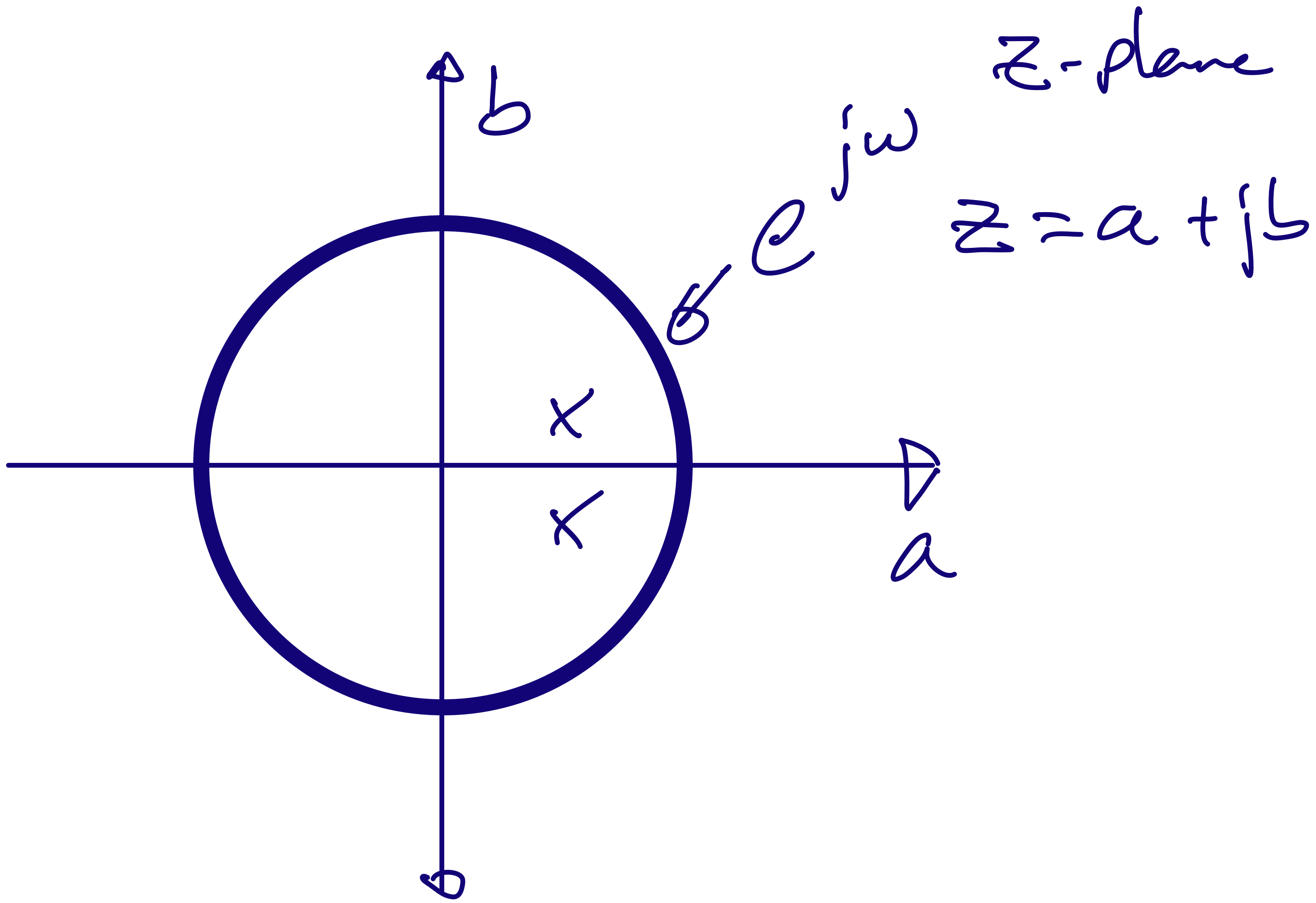
$s = a + jw$

Pole-Zero plots

If you're not comfortable with pole/zero plots, have a look at

What does the Laplace Transform really tell us

Z-domain

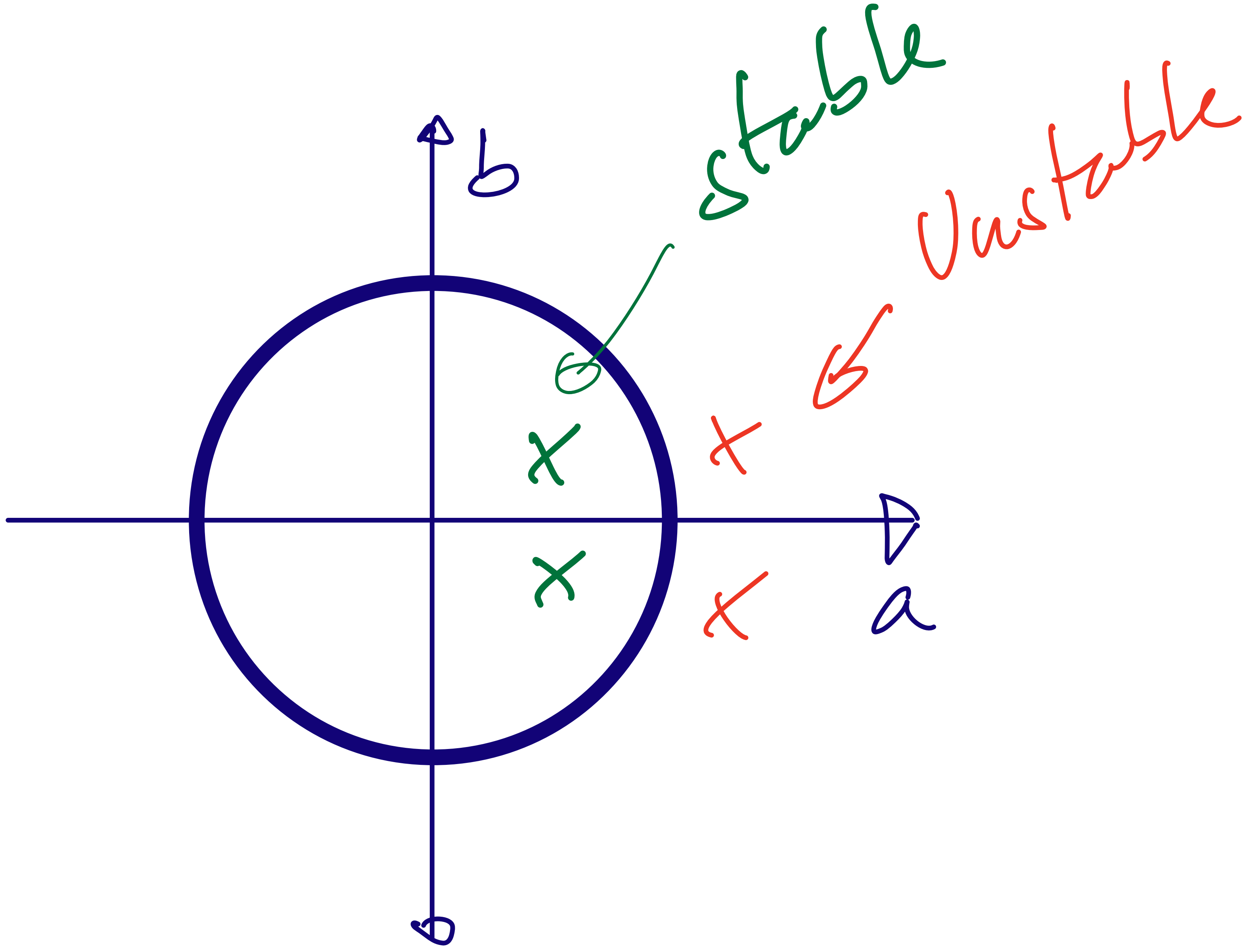


Spectra repeat every 2π (every f_s)

Bi-linear transform

$$s = \frac{z-1}{z+1}$$

Warning: First-order approximation https://en.wikipedia.org/wiki/Bilinear_transform



First order filter

$$y[n+1] = bx[n] + ay[n] \Rightarrow yz = bx + ay$$

$$y[n] = bx[n-1] + ay[n-1] \Rightarrow y = bxz^{-1} + ayz^{-1}$$

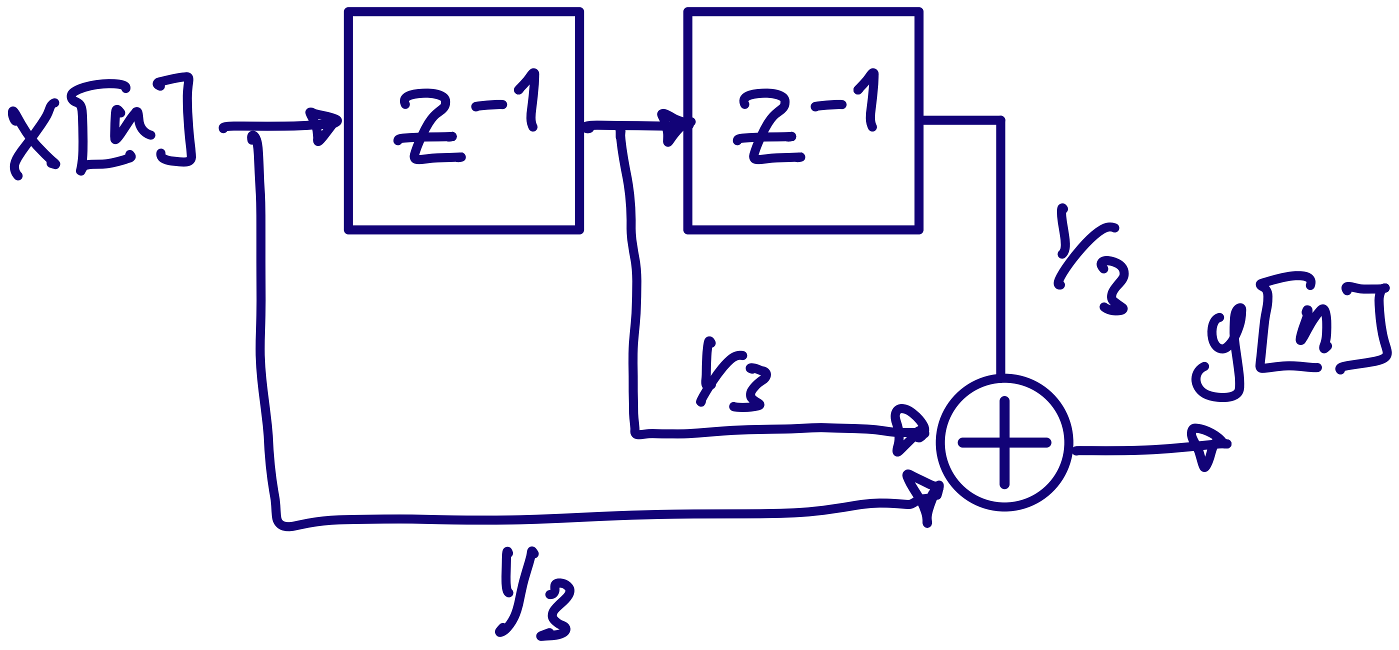
$$H(z) = \frac{b}{z-a}$$

Infinite-impulse response (IIR)

$$h[n] = \begin{cases} k & \text{if } n < 1 \\ a^{n-1}b + a^n k & \text{if } n \geq 1 \end{cases}$$

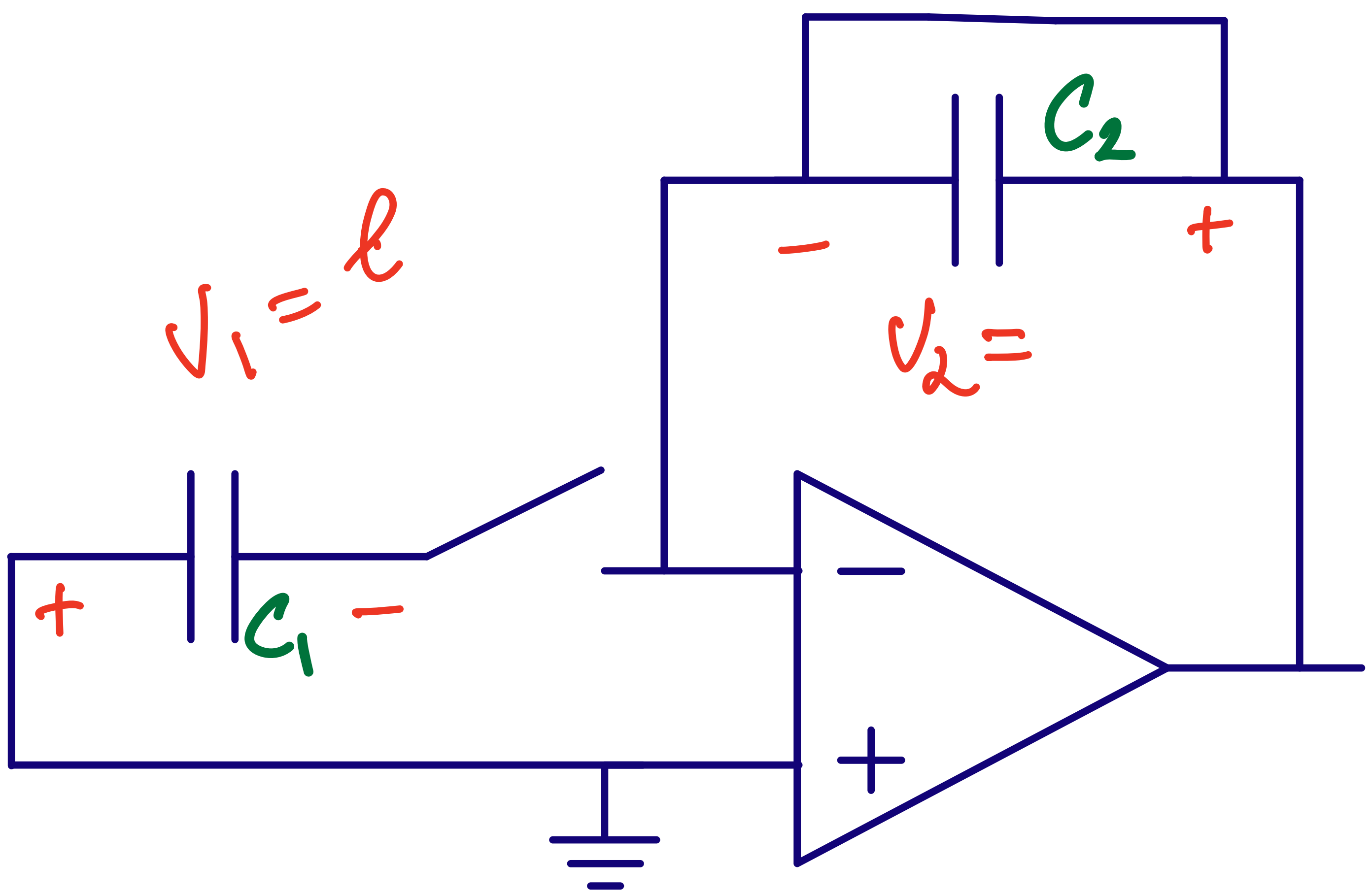
Head's up: Fig 13.12 in AIC is wrong

Finite-impulse response(FIR)



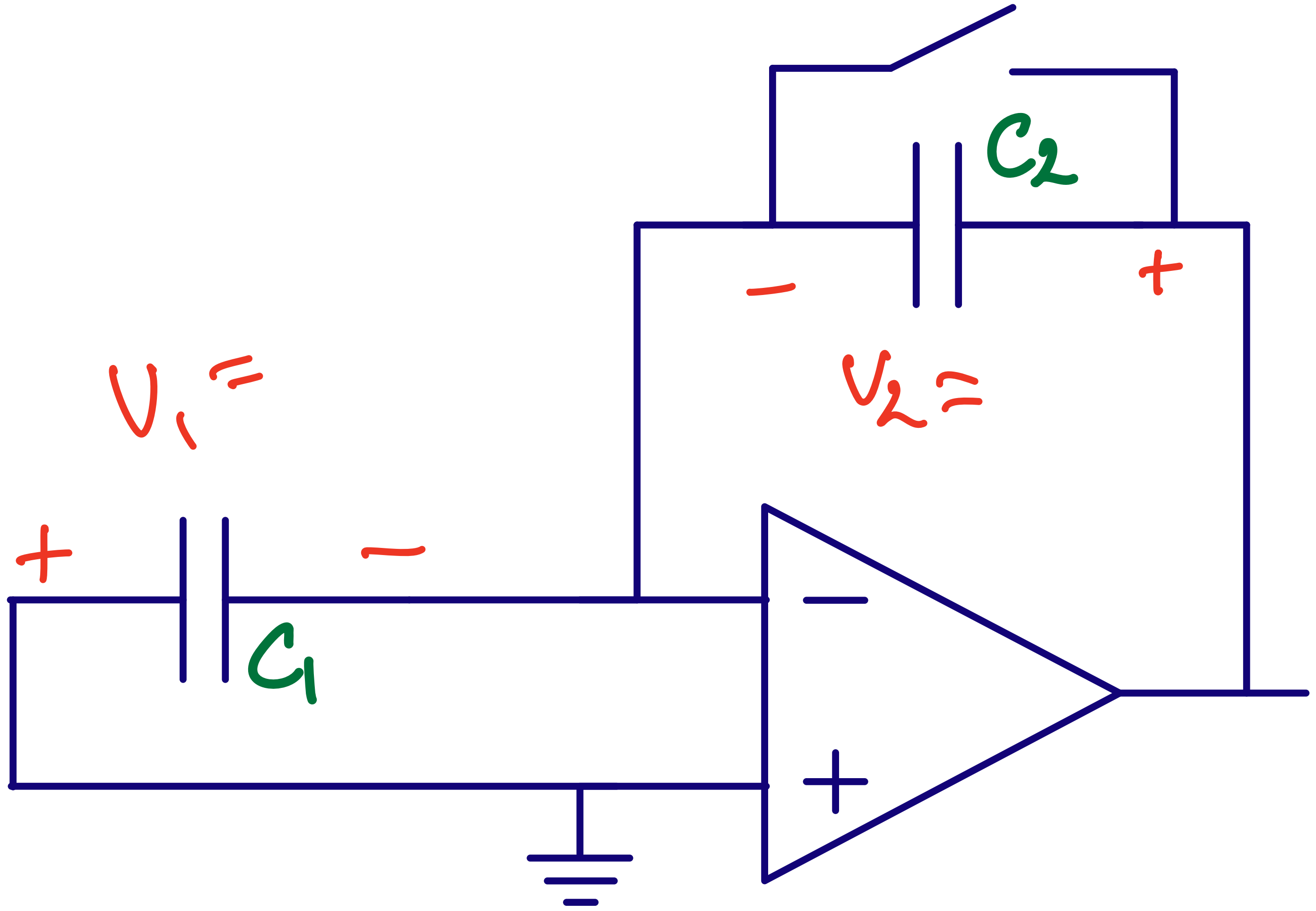
$$H(z) = \frac{1}{3}\sum_{i=0}^{2} z^{-1}$$

Switched-Capacitor



$Q_1 =$

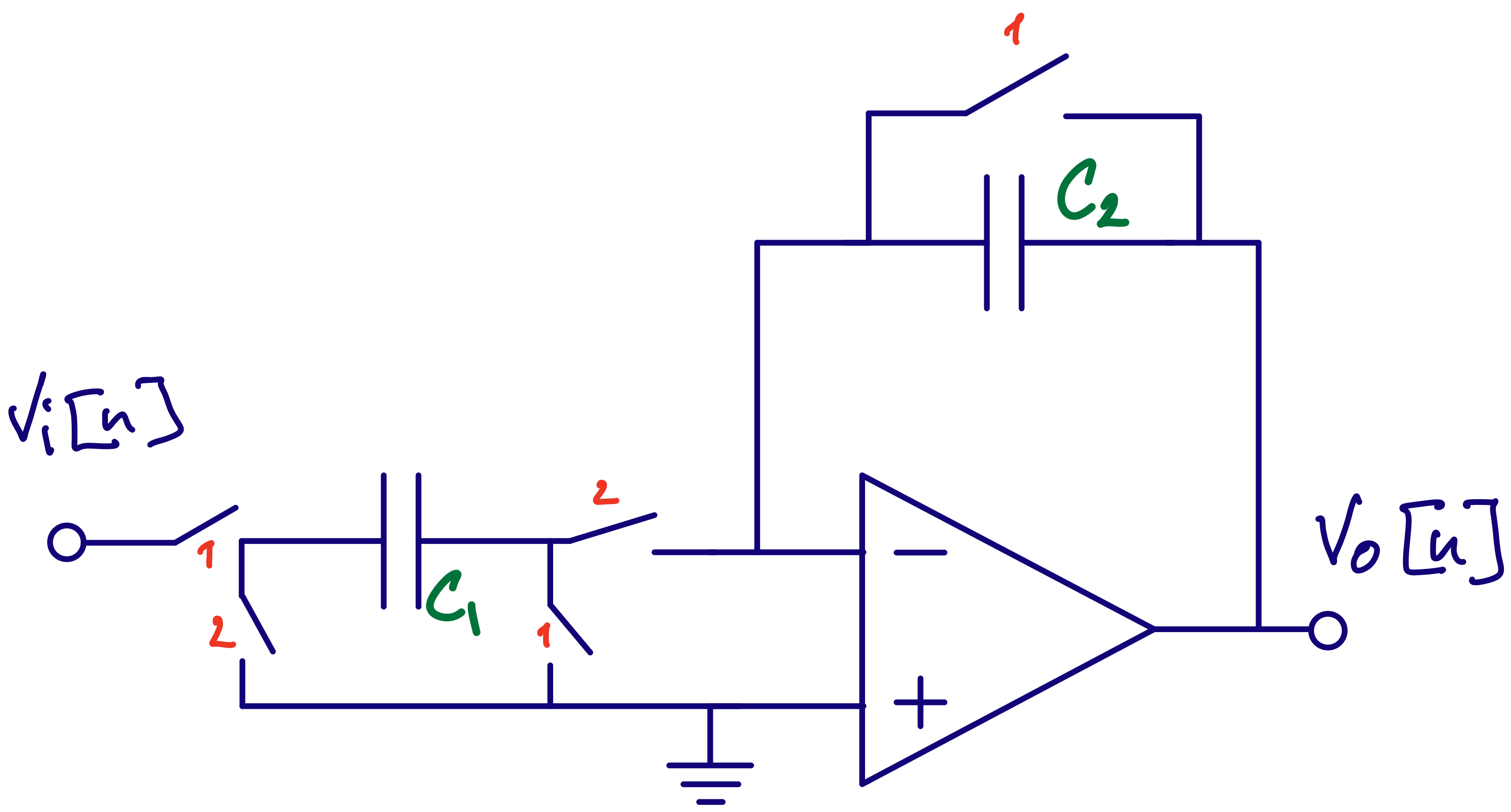
$Q_2 =$



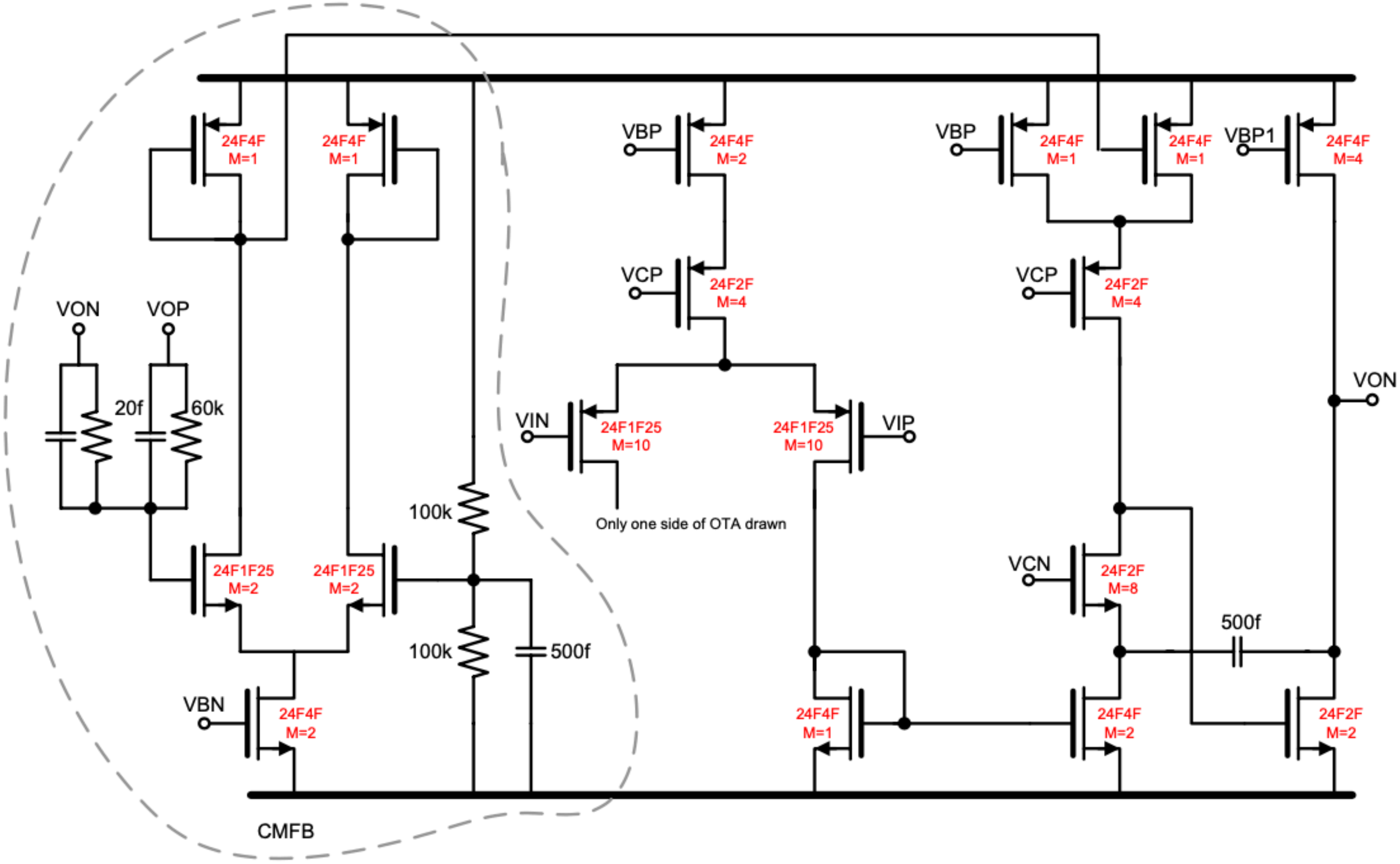
$Q_1 =$

$Q_2 =$

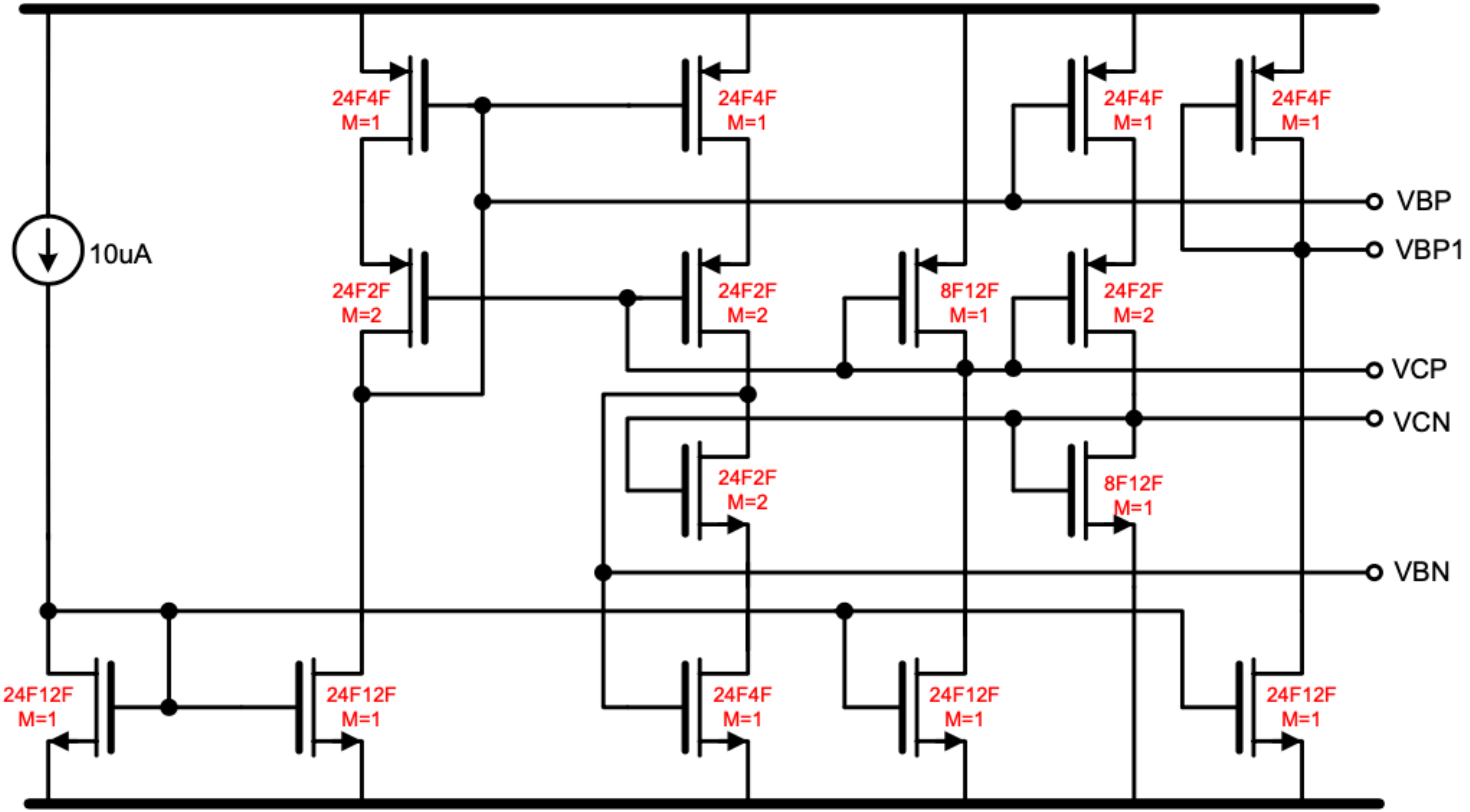
What do we need?



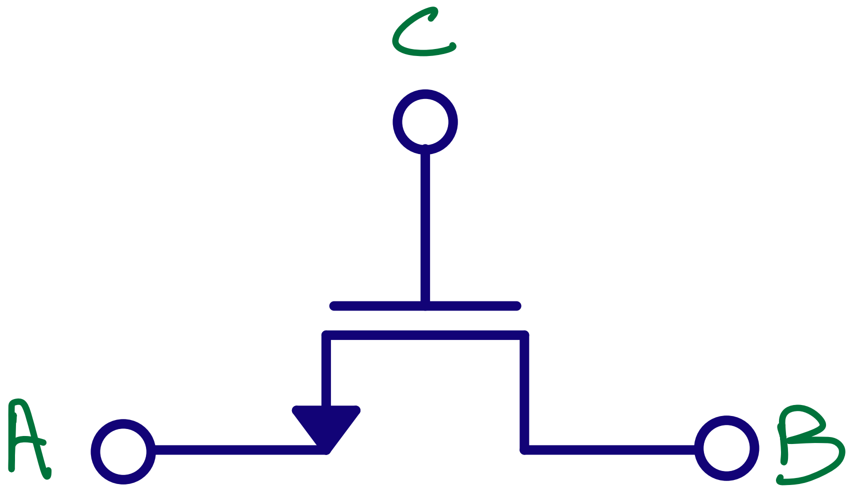
OTA

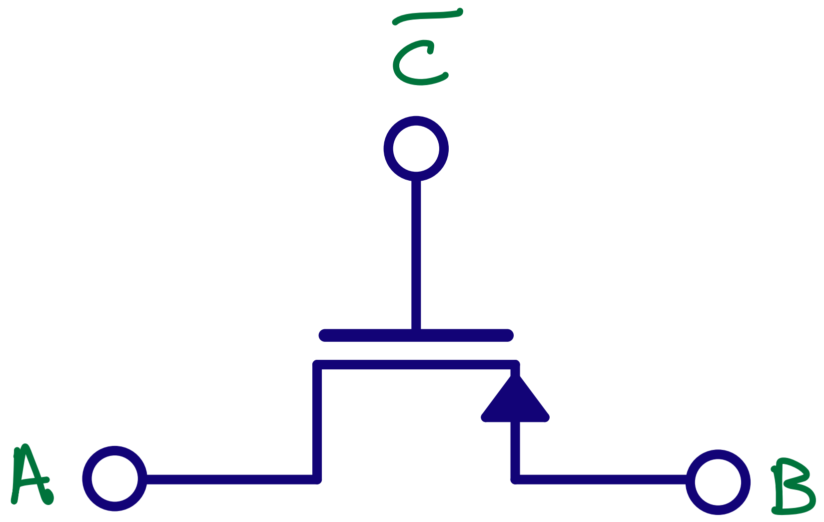


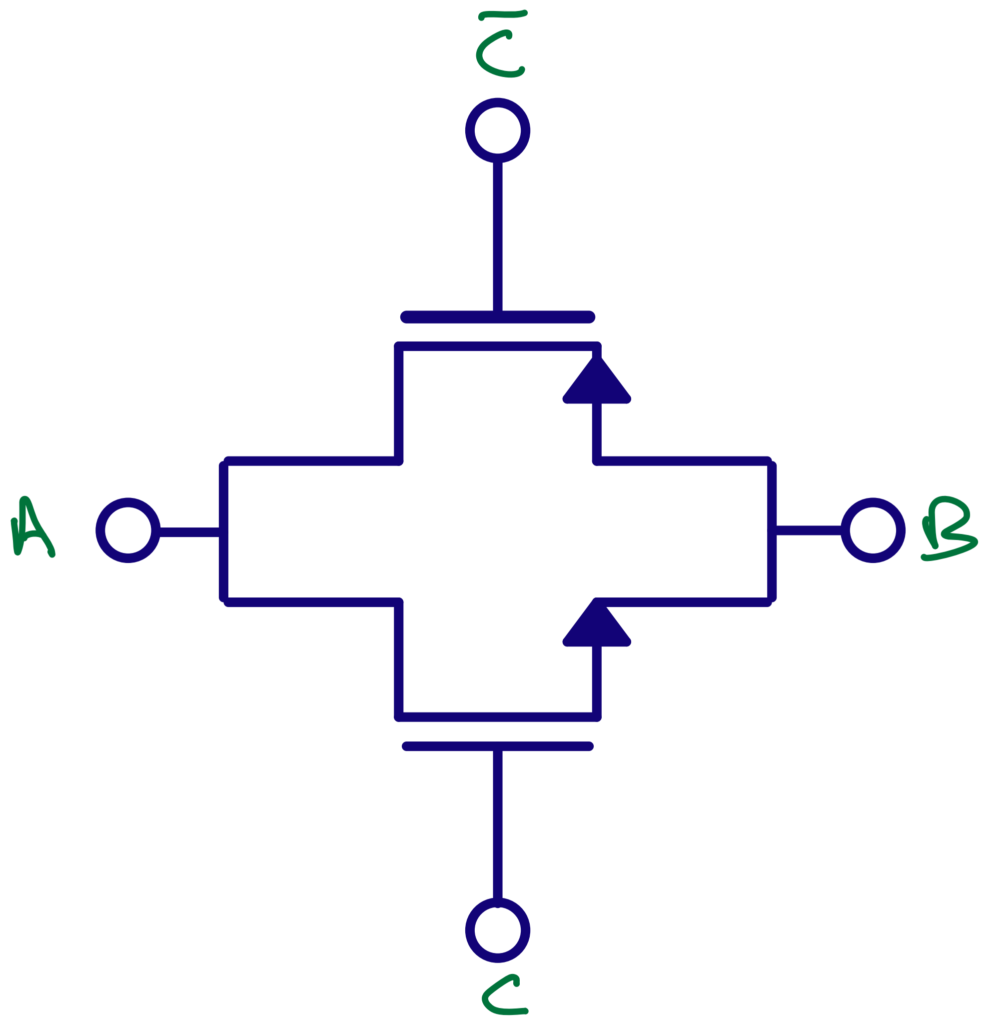
F = minimum transistor gate length. For example 24F4F => W = 24 x min gate, L= 4 x min gate

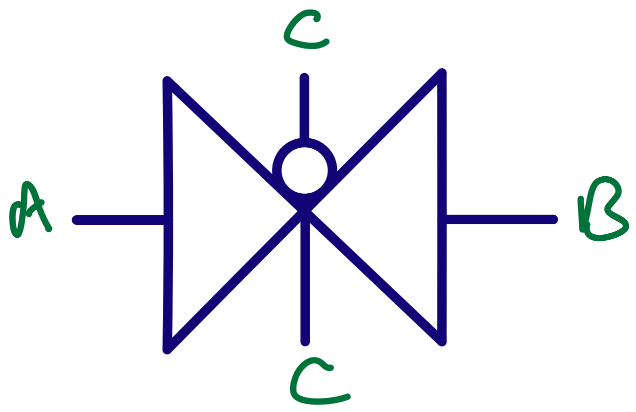

24F4F
M=1
24F4F
M=1
24F4F
M=1
24F4F
M=1
VBP
VBP1
10uA
24F2F
M=2
24F2F
M=2
8F12F
M=1
24F2F
M=2
VCP
VCN
24F2F
M=2
8F12F
M=1
VBN
24F12F
M=1
24F12F
M=1
24F4F
M=1
24F12F
M=1
24F12F
M=1

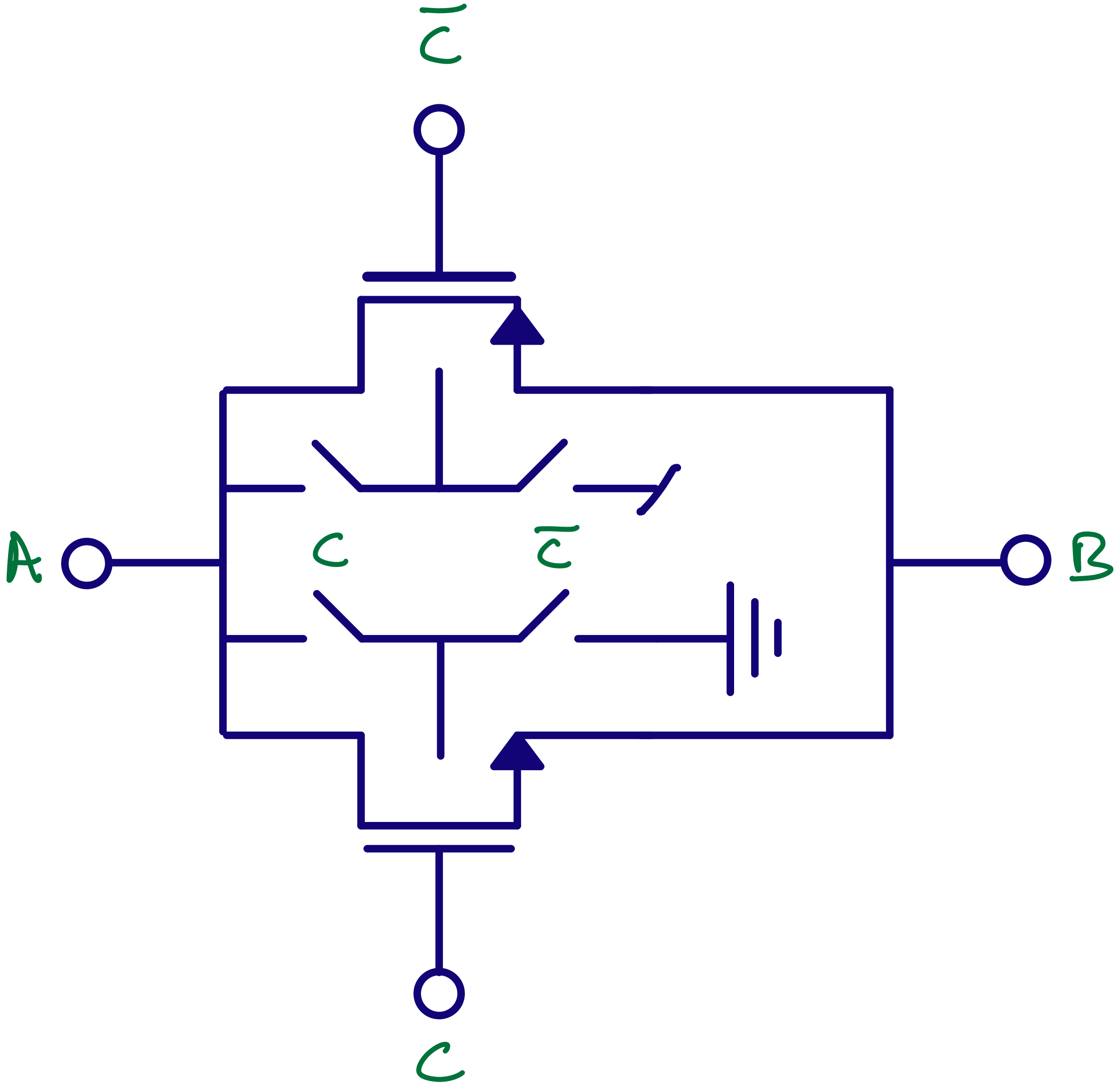
Switches


C
A
B

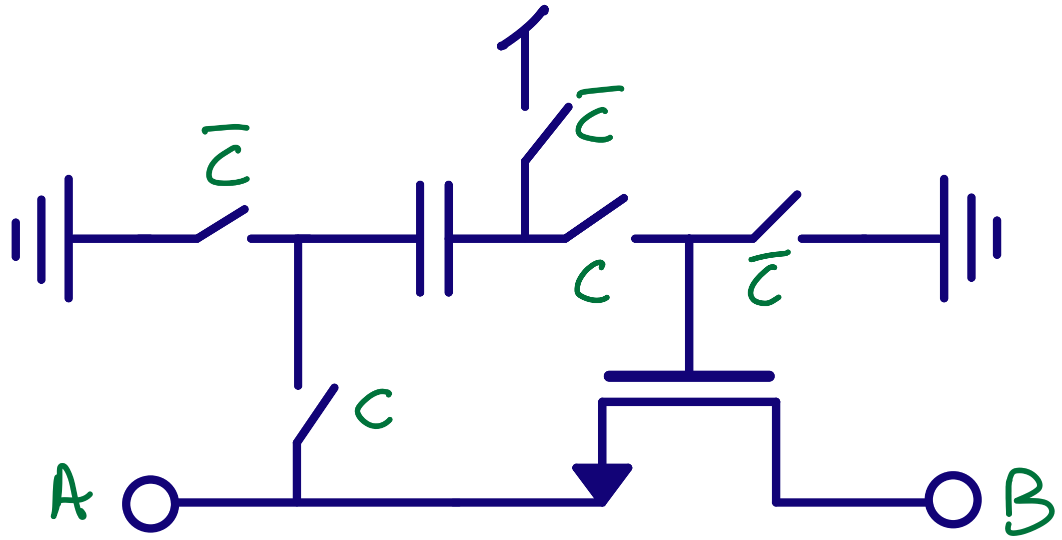

$\bar{C}$
A
B


$\bar{C}$
A
B
C

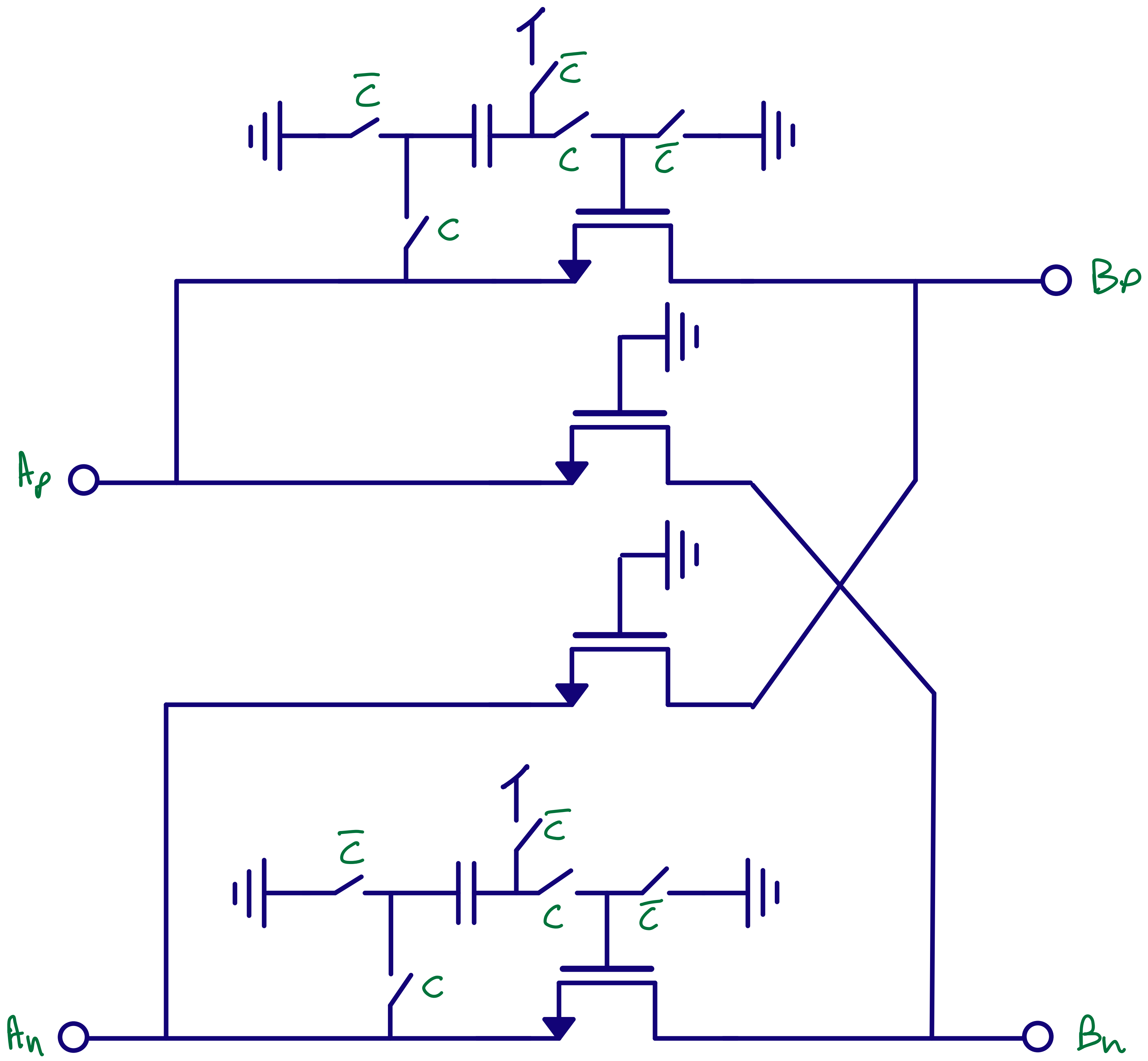

C
A
B
C



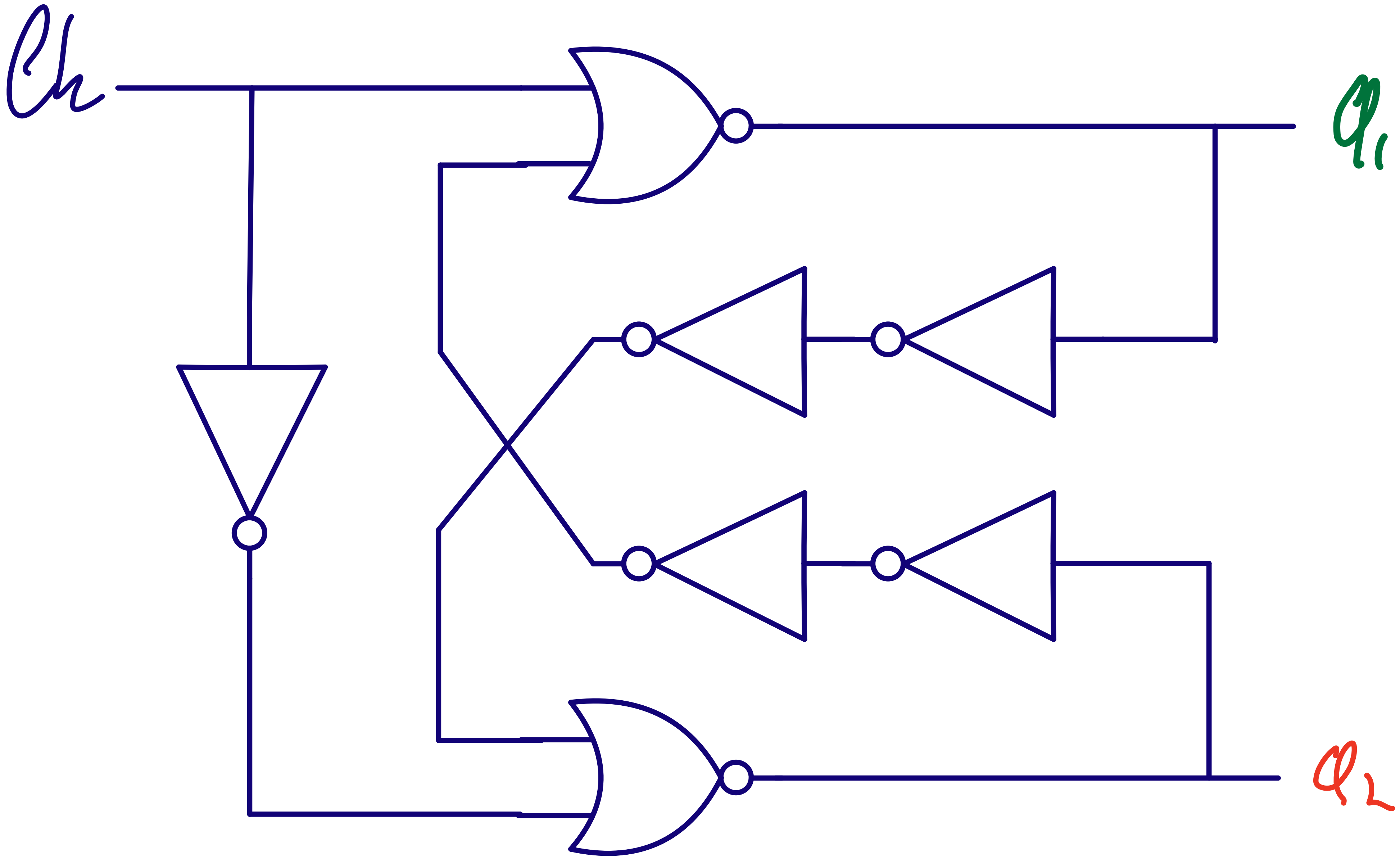
C̄
A
C
C̄
B
C



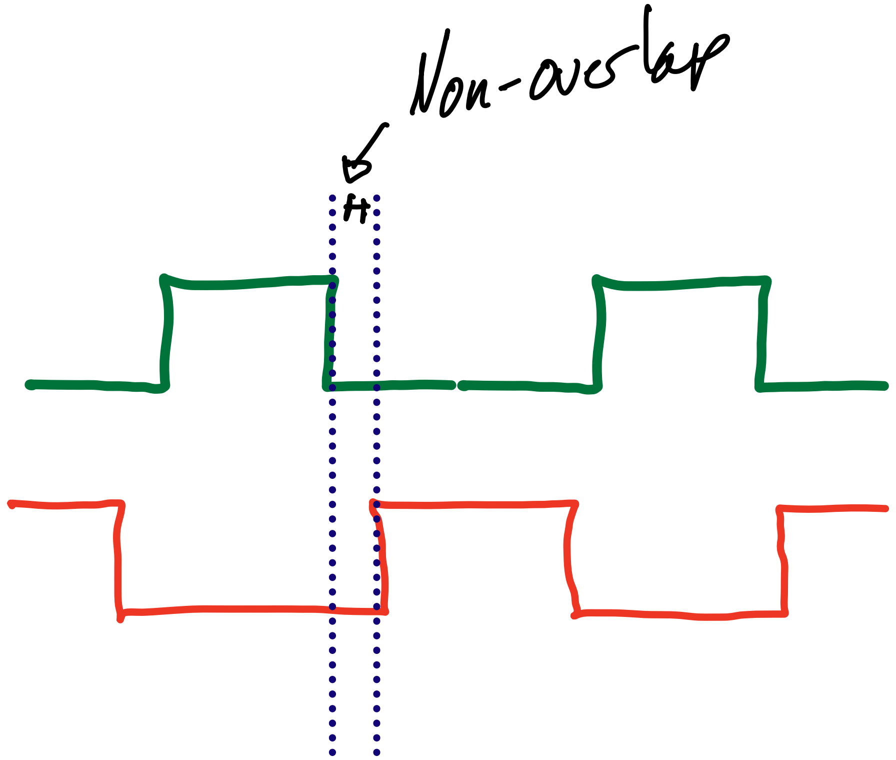
C̄
C̄
C
C̄
C
A
B


$\bar{c}$
$\bar{c}$
c
$\bar{c}$
c
B_p
A_p
$\bar{c}$
$\bar{c}$
c
$\bar{c}$
c
A_n
B_n

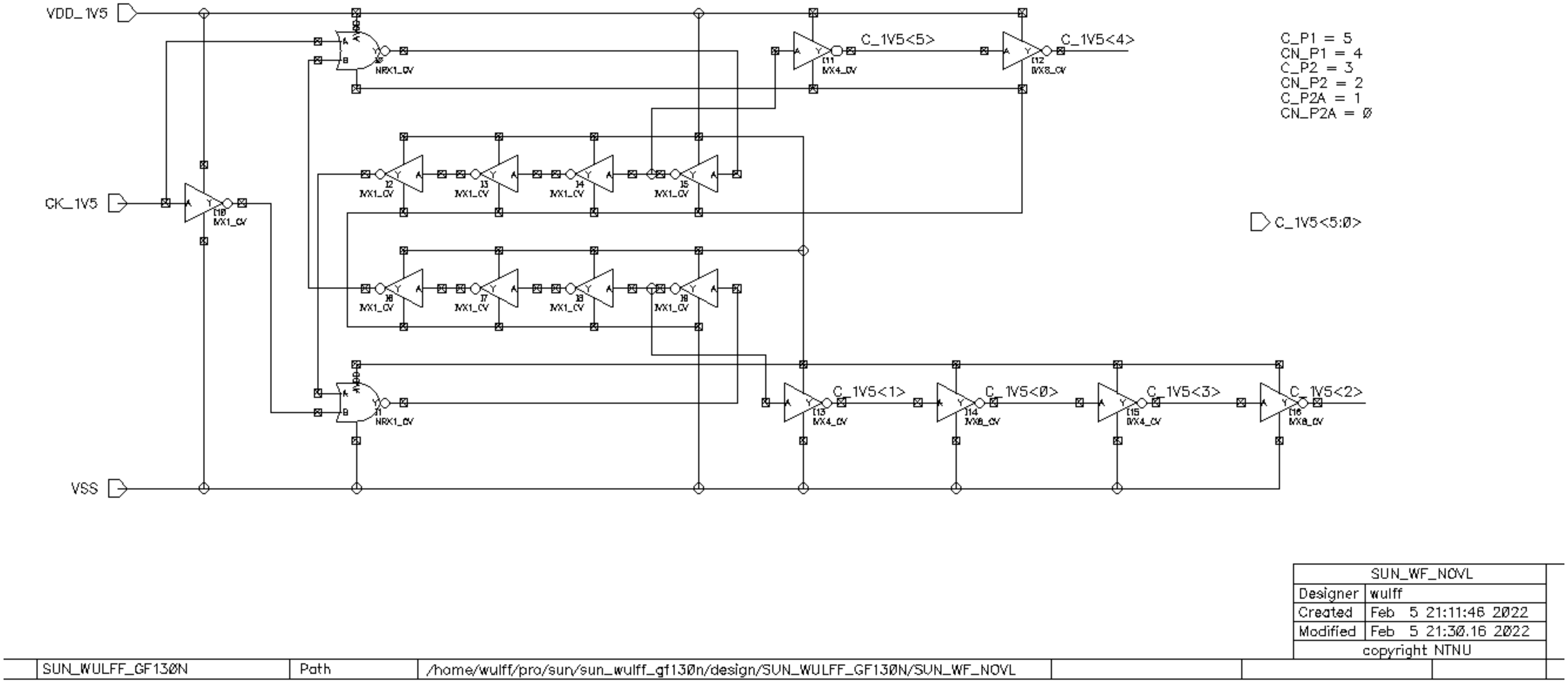
Non-overlapping clocks



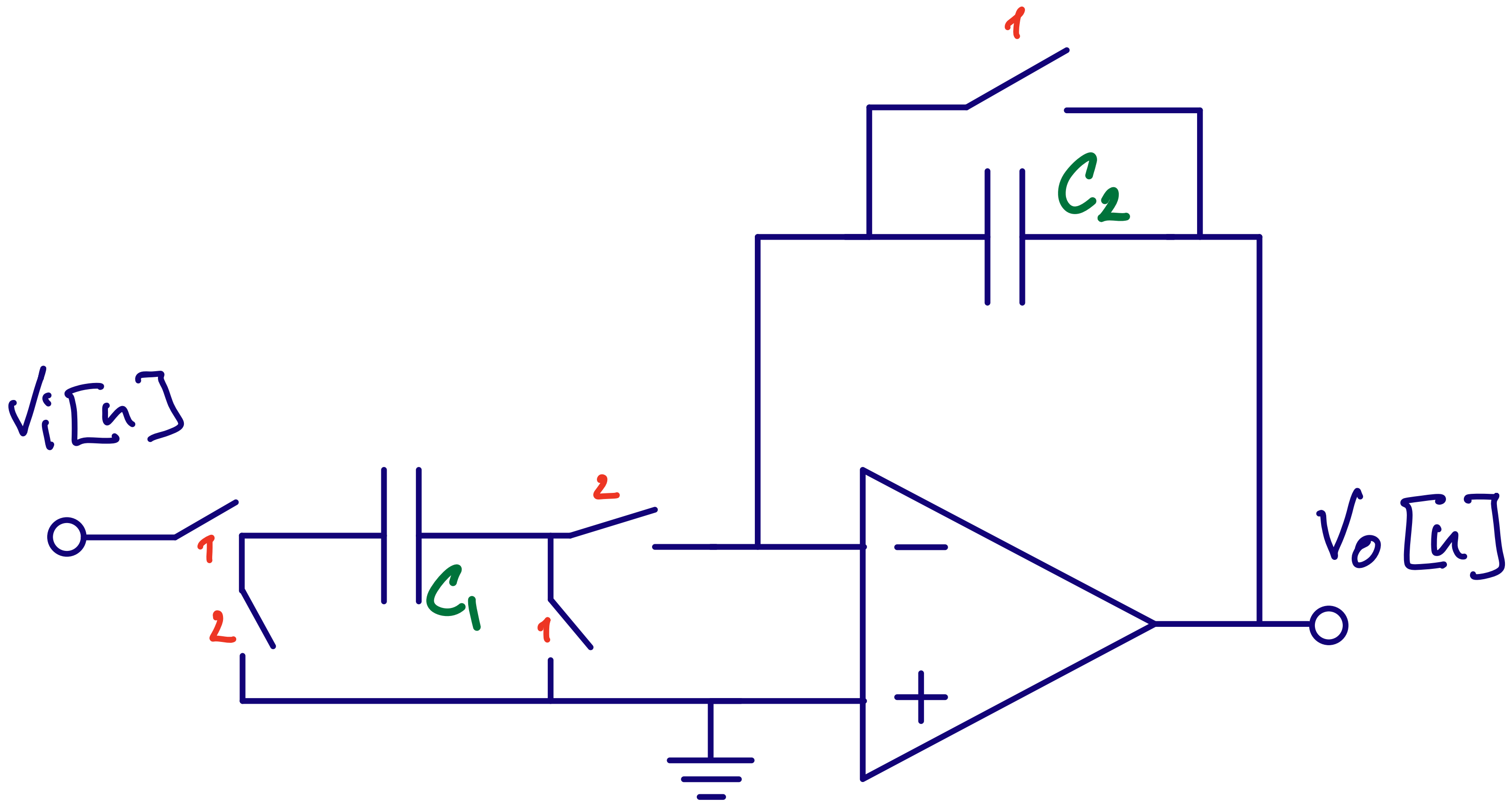
Ck
Φ1
Φ2



Non-overlap

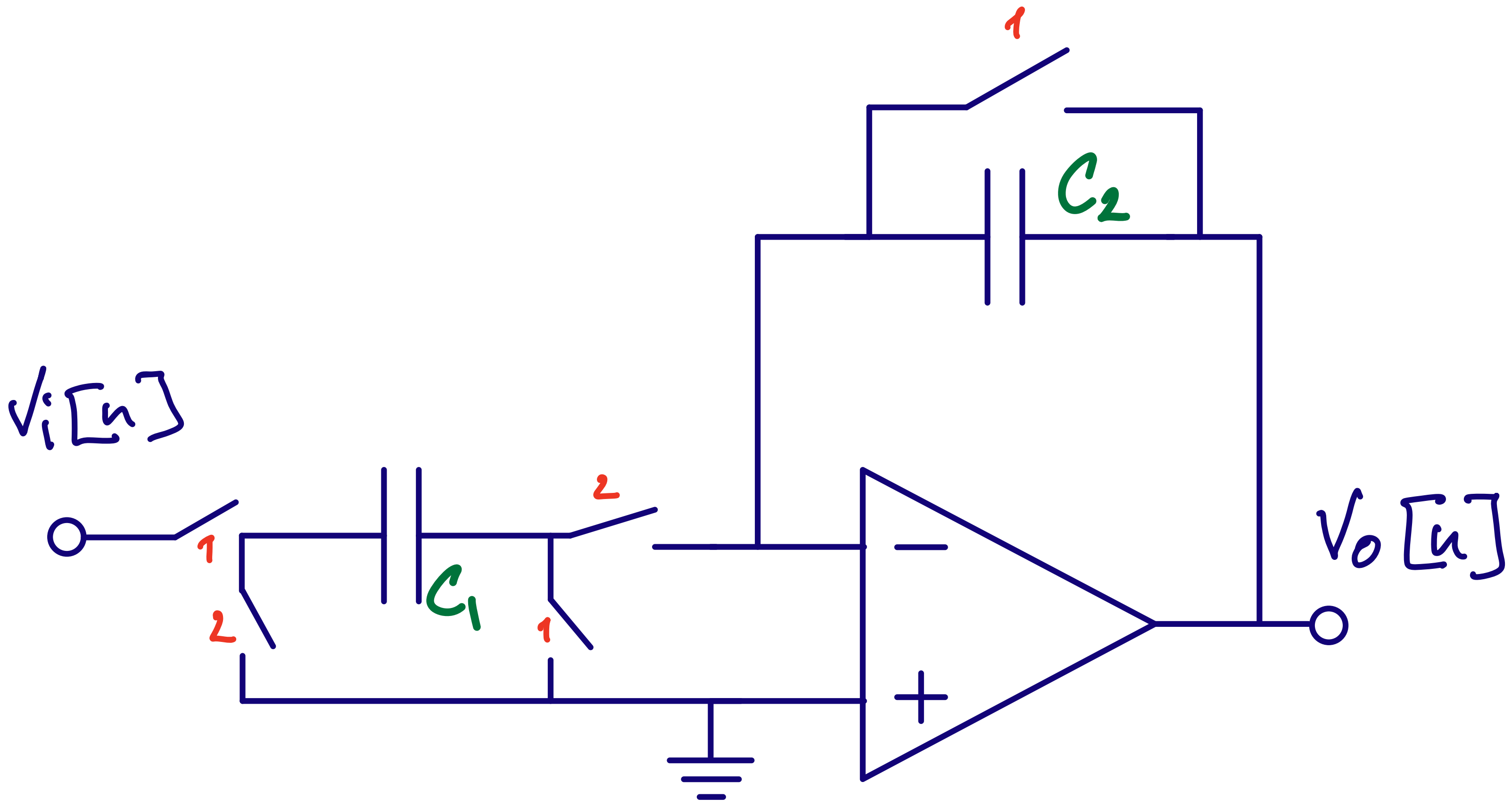

VDD_1V5
CK_1V5
VSS
C_1V5<5>
C_1V5<4>
C_1V5<1>
C_1V5<0>
C_1V5<3>
C_1V5<2>
C_1V5<5:0>
C_P1 = 5
CN_P1 = 4
C_P2 = 3
CN_P2 = 2
C_P2A = 1
CN_P2A = 0
SUN_WF_NOVL
Designer wulff
Created Feb 5 21:11:46 2022
Modified Feb 5 21:30.16 2022
copyright NTNU
SUN_WULFF_GF130N
Path
/home/wulff/pro/sun/sun_wulff_gf130n/design/SUN_WULFF_GF130N/SUN_WF_NOVL

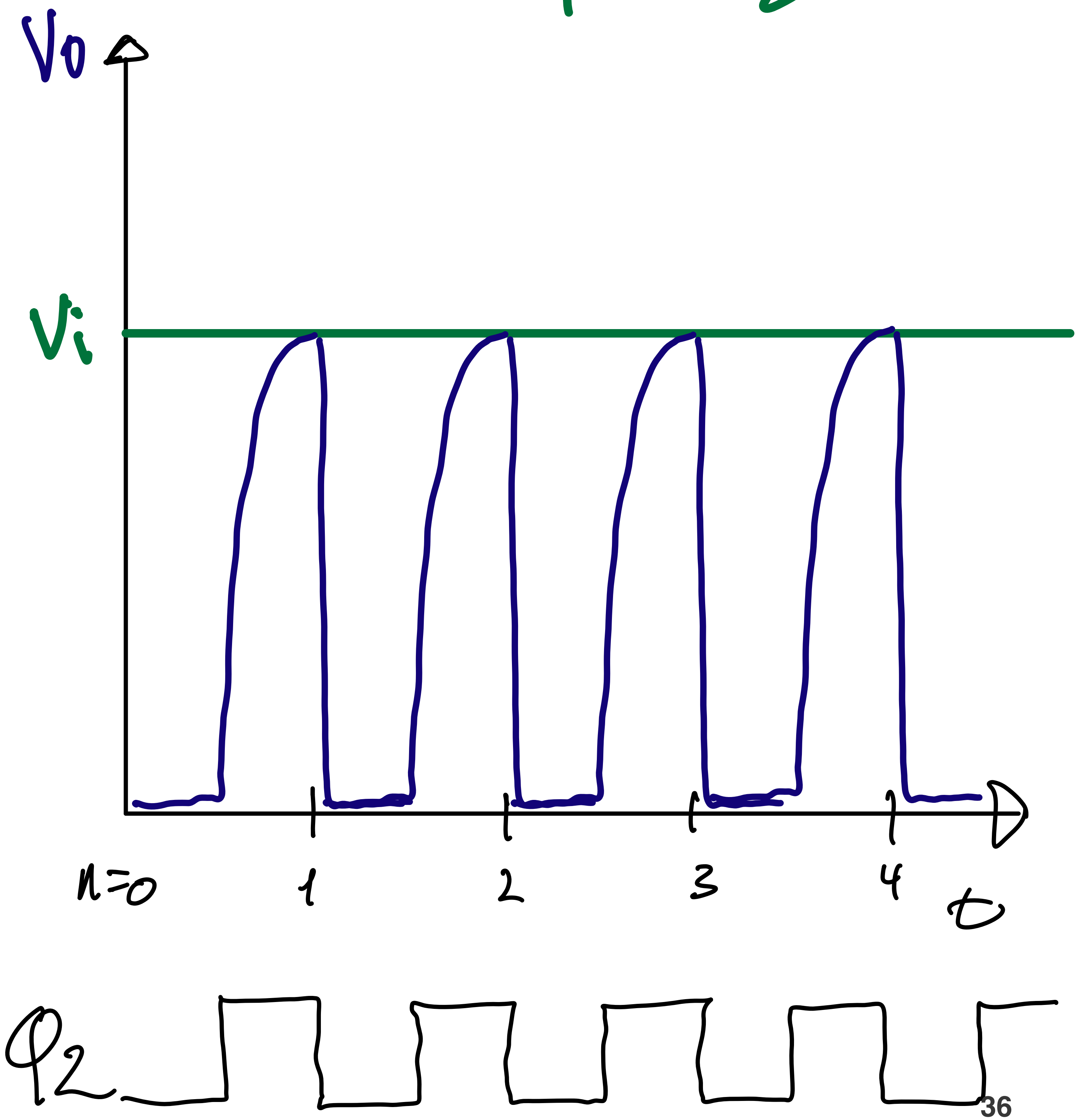
Principles

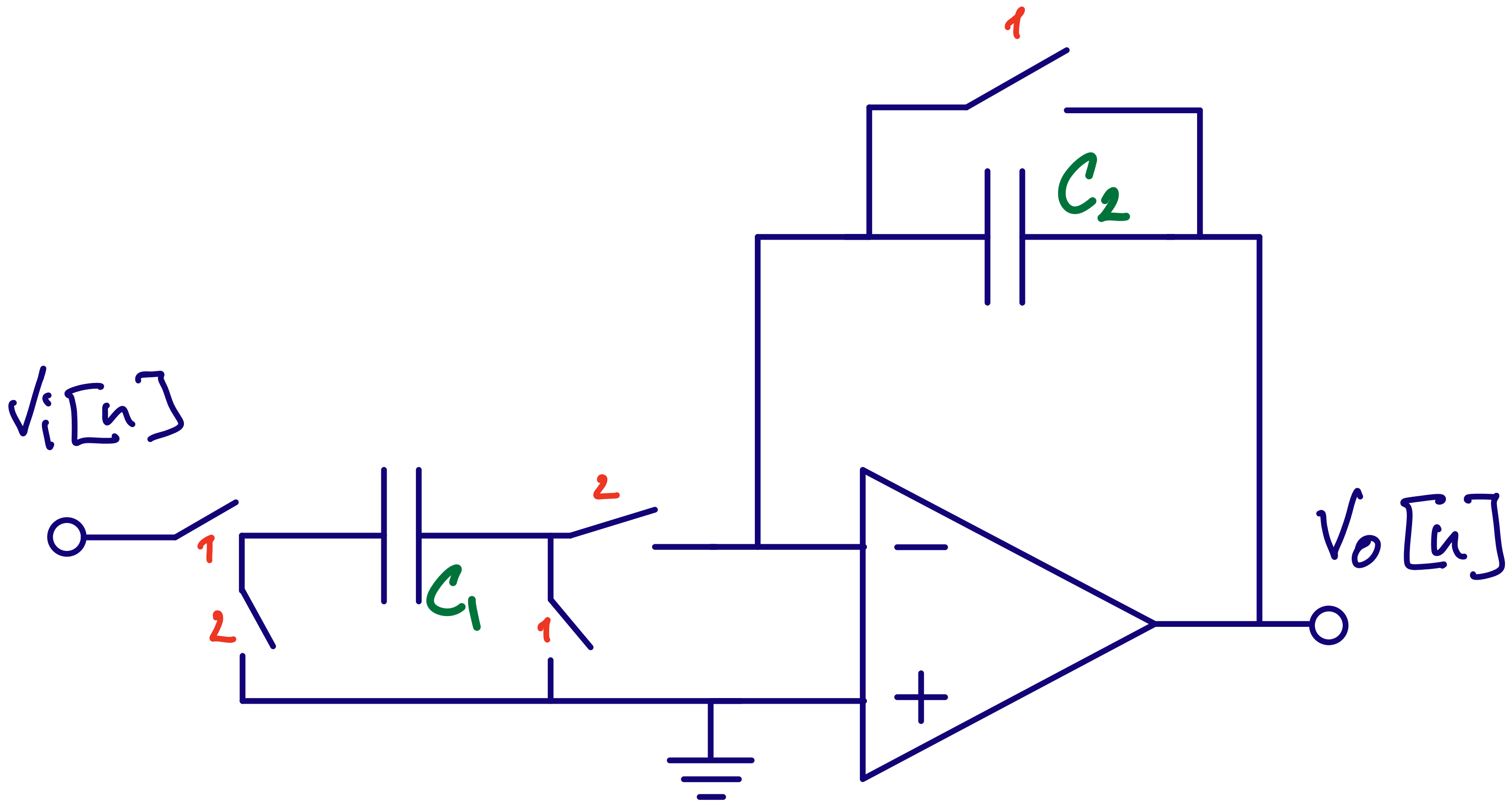


Vi[n]
Vo[n]
C1
C2
1
2
2
1
1

$C_1 = C_2$



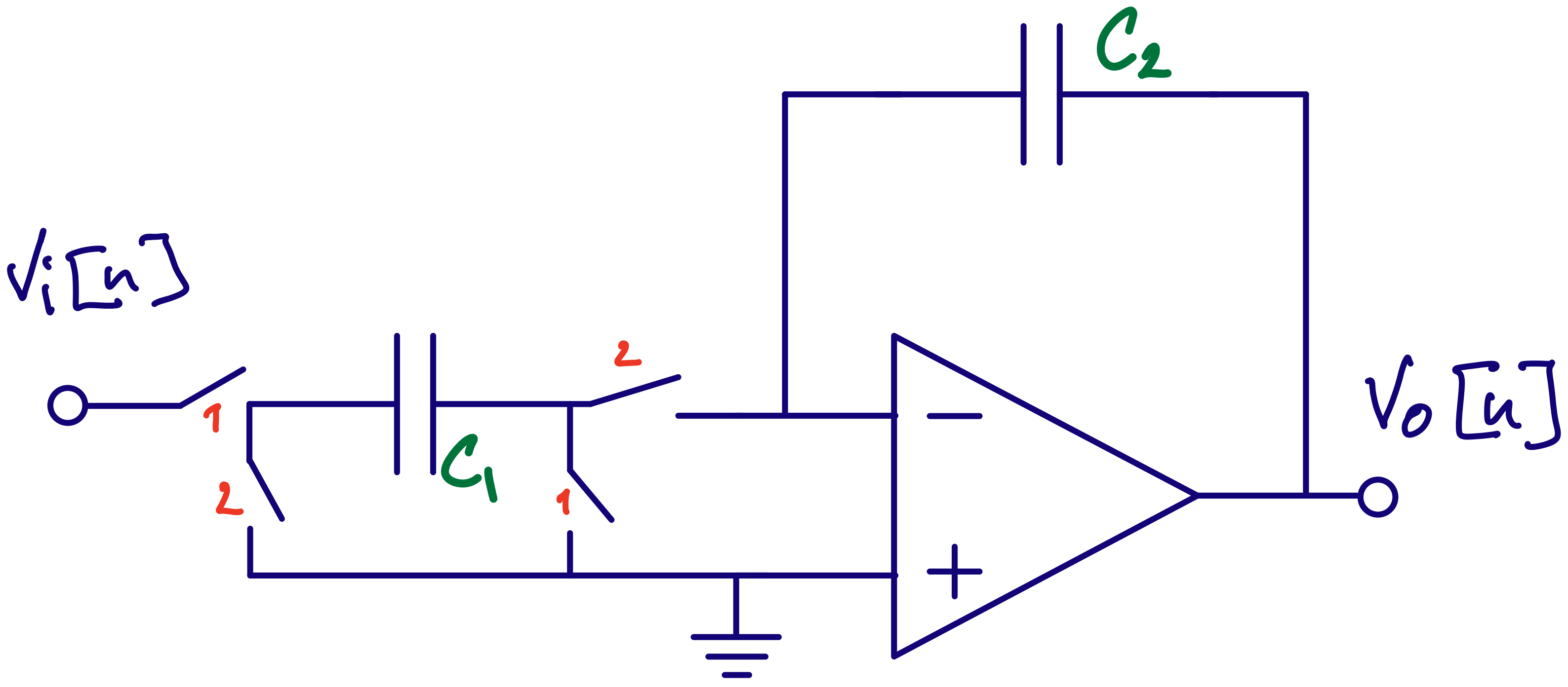




$$V_o[n+1] = \frac{C_1}{C_2} V_i[n]$$

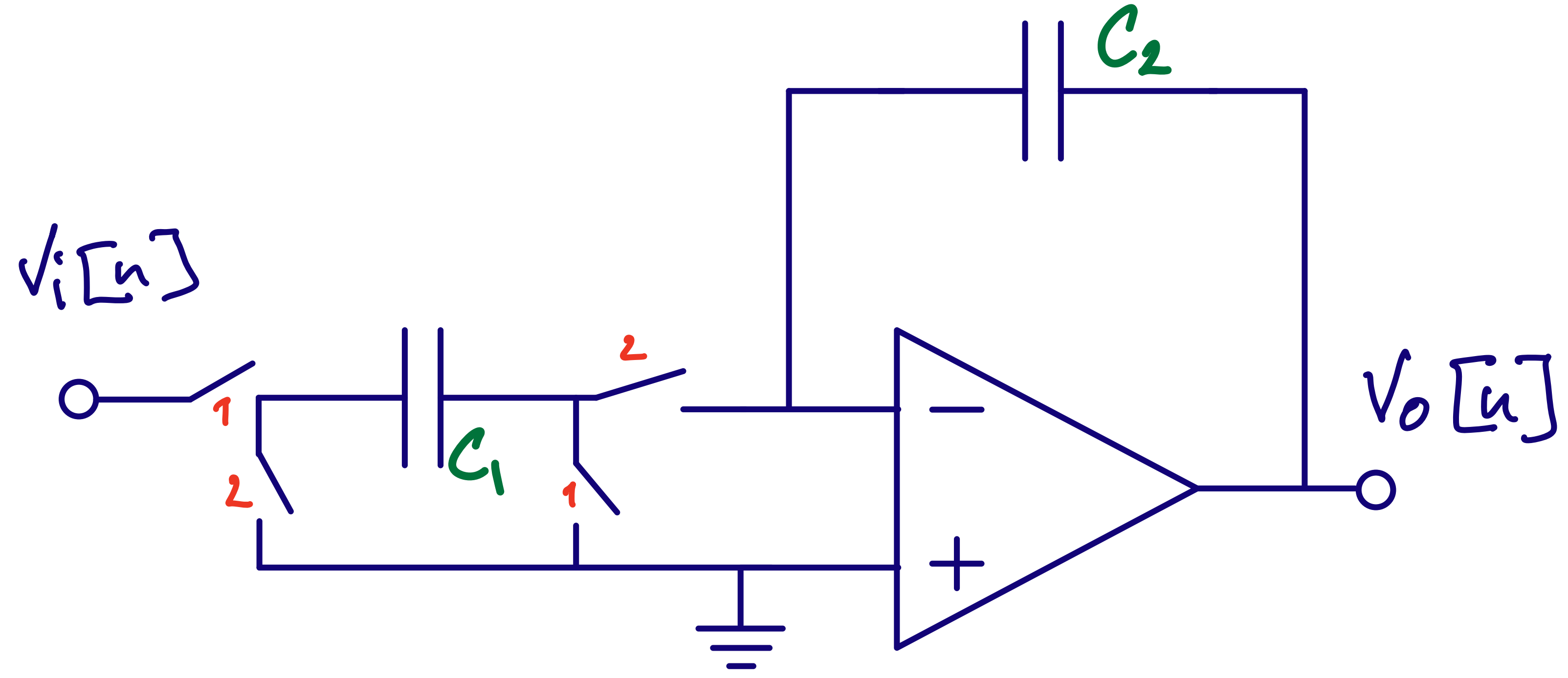
$$V_o z = \frac{C_1}{C_2} V_i$$

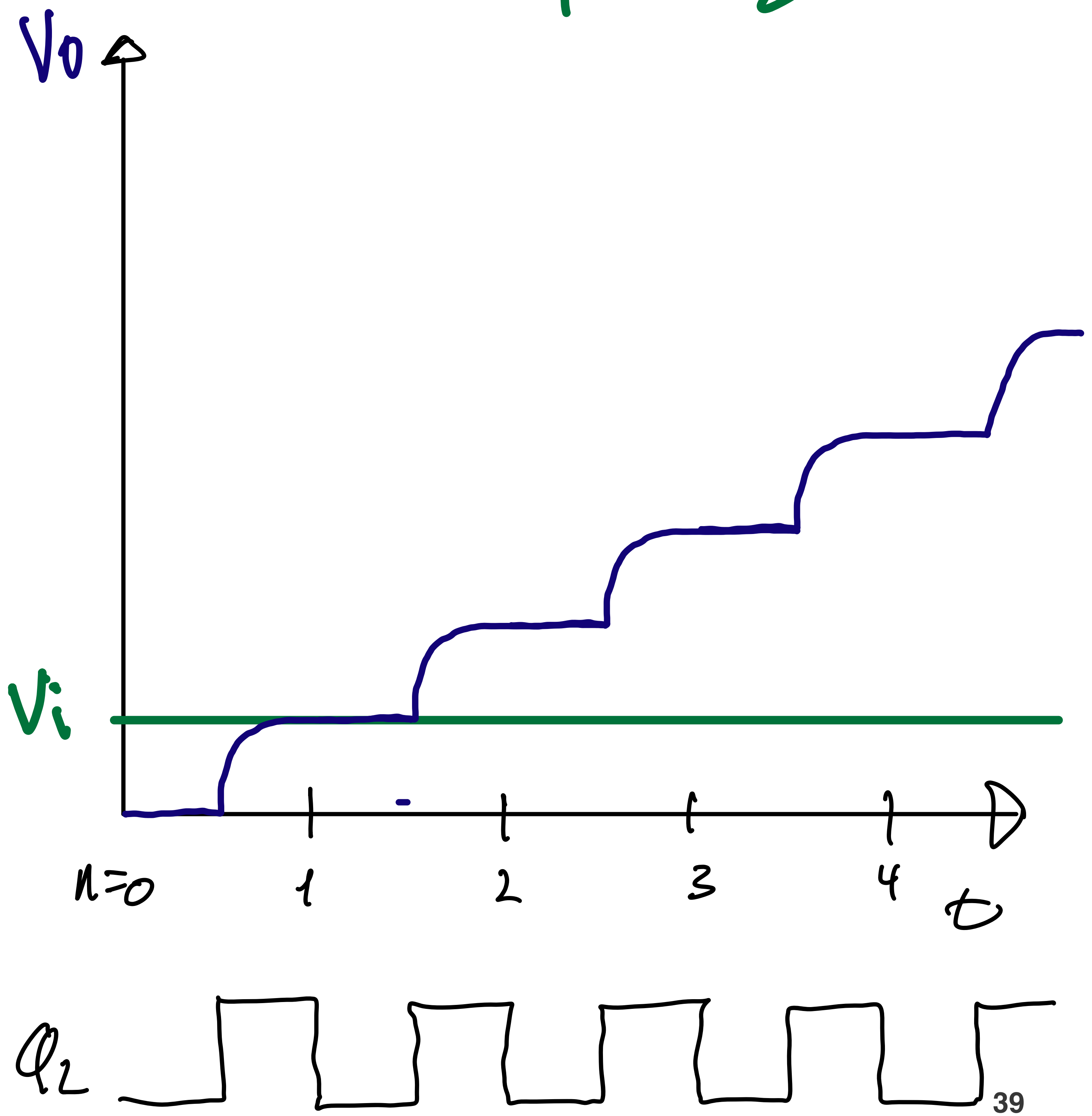
$$\frac{V_o}{V_i} = H(z) = \frac{C_1}{C_2} z^{-1}$$

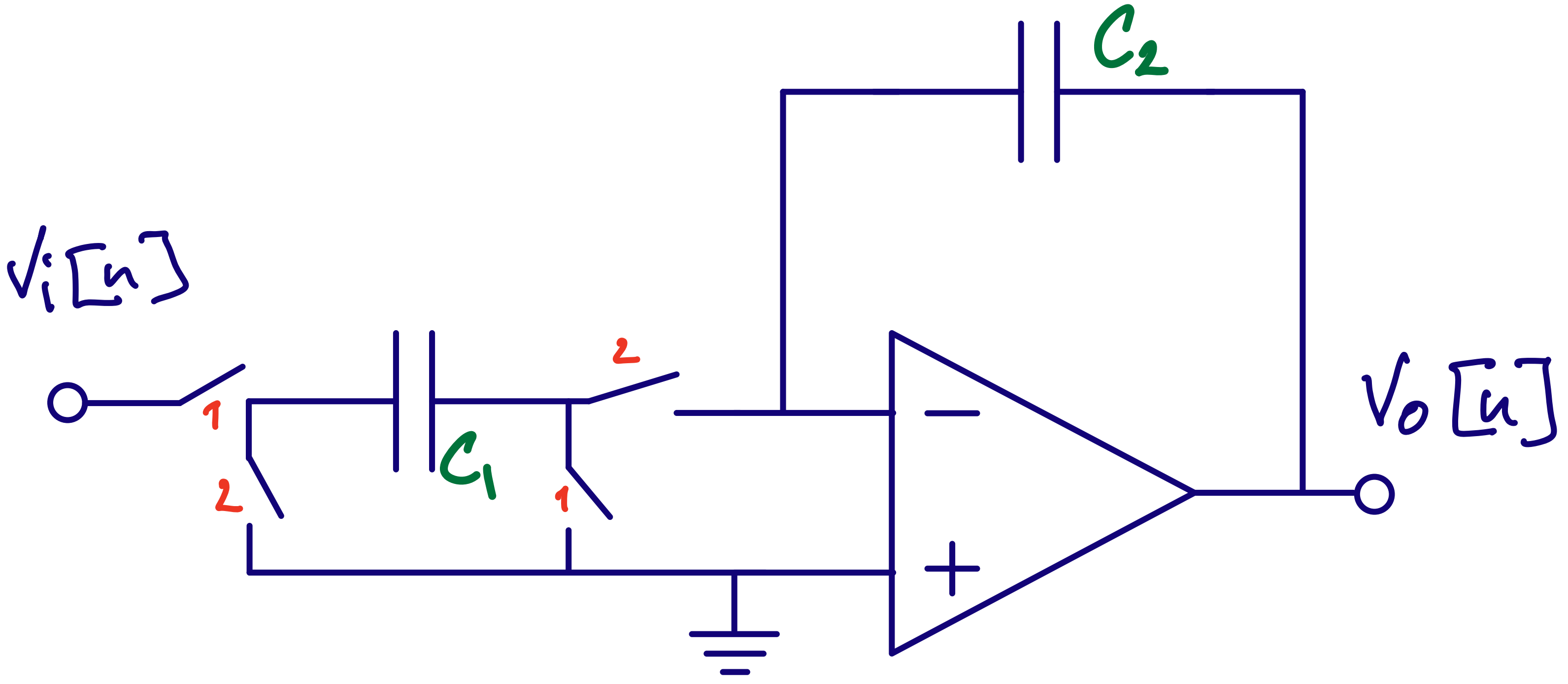


$V_i[n]$
1
2
C_1
2
1
C_2
−
+
$V_o[n]$

$C_1 = C_2$



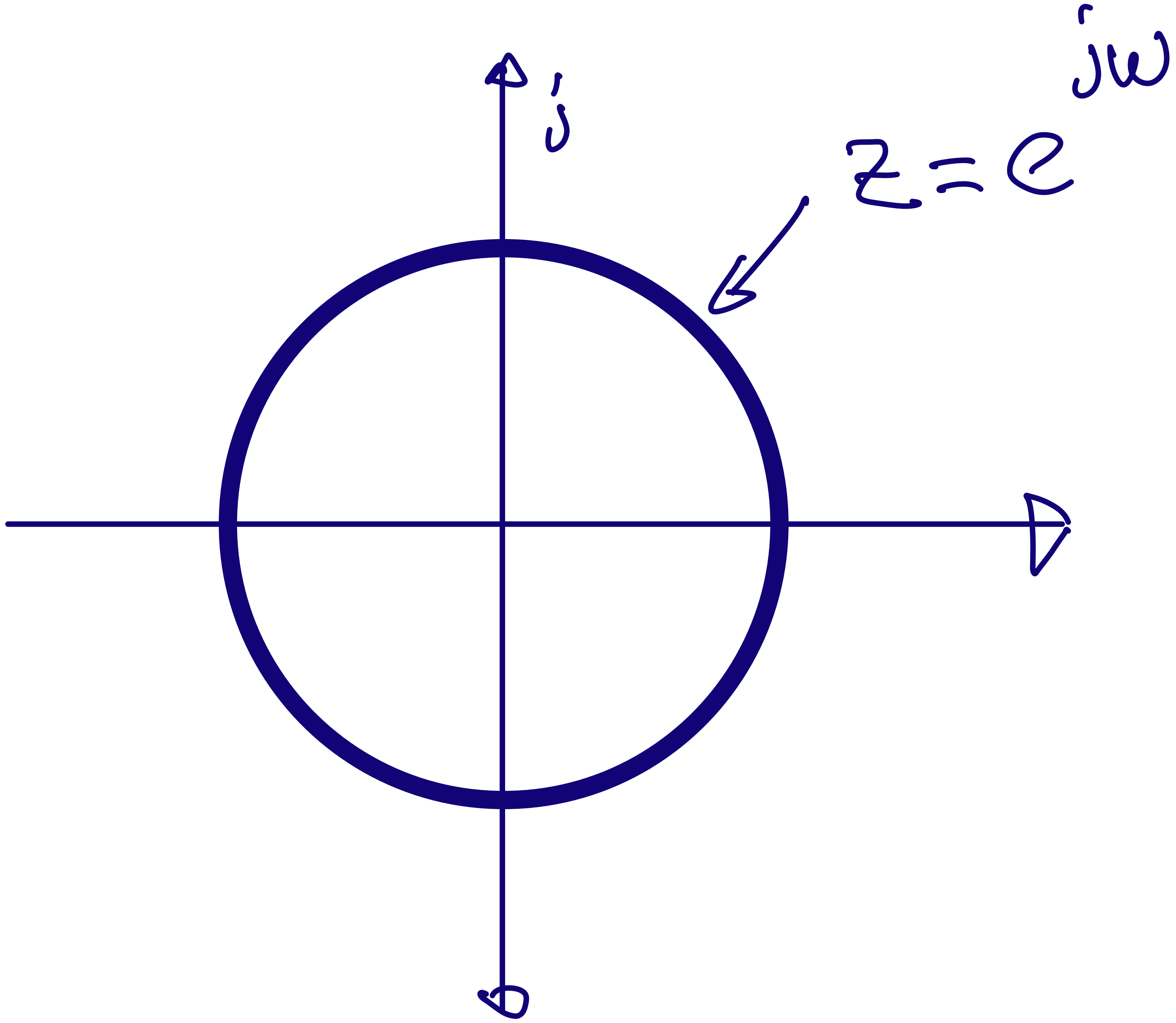




$$V_o[n] = V_o[n-1] + \frac{C_1}{C_2} V_i[n-1]$$

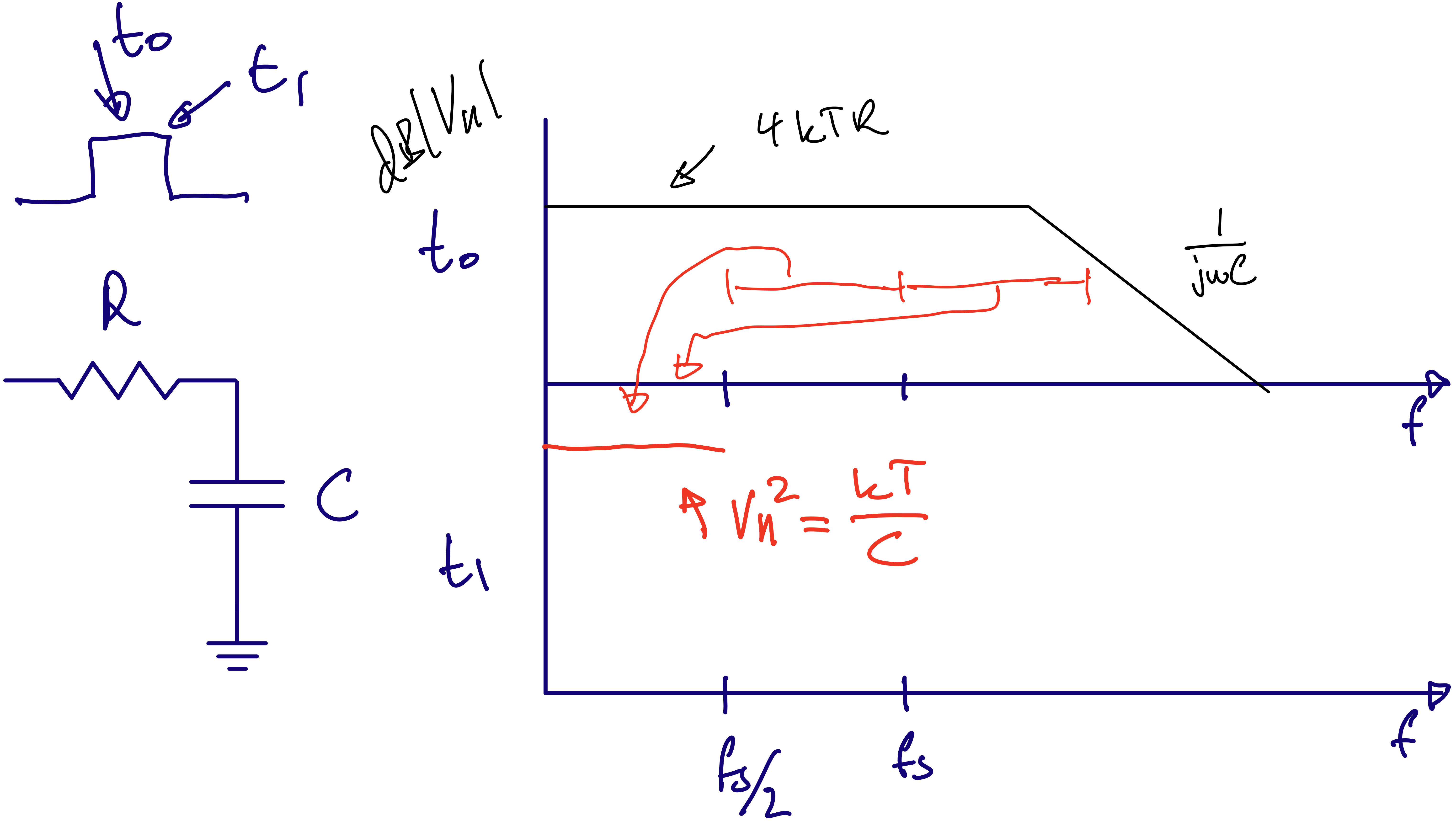
$$V_o - z^{-1} V_o = \frac{C_1}{C_2} z^{-1} V_i$$

$$H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{z^{-1} + 1} = \frac{C_1}{C_2} \frac{1}{z - 1}$$



$$H(z) = \frac{C_1}{C_2} \frac{1}{z - 1}$$

Noise



t_0
t_1
R
C
dB|Vn|
4kTR
$\frac{1}{j\omega C}$
t_0
t_1
f
f
$V_n^2 = \frac{kT}{C}$
$f_s/2$
f_s

Both phases add noise, $V_n^2 > \frac{2kT}{C}$

Mean

$$\overline{x(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)dt$$

Mean Square

$$\overline{x^2(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x^2(t)dt$$

Variance

$$\sigma^2 = \overline{x^2(t)} - \overline{x(t)}^2$$

where σ is the standard deviation.
If mean is removed, or is zero, then

$$\sigma^2 = \overline{x^2(t)}$$

Assume two random processes, $x_1(t)$ and $x_2(t)$ with mean of zero (or removed).

$$x_{tot}(t) = x_1(t) + x_2(t)$$
$$x_{tot}^2(t) = x_1^2(t) + x_2^2(t) + 2x_1(t)x_2(t)$$

Variance (assuming mean of zero)

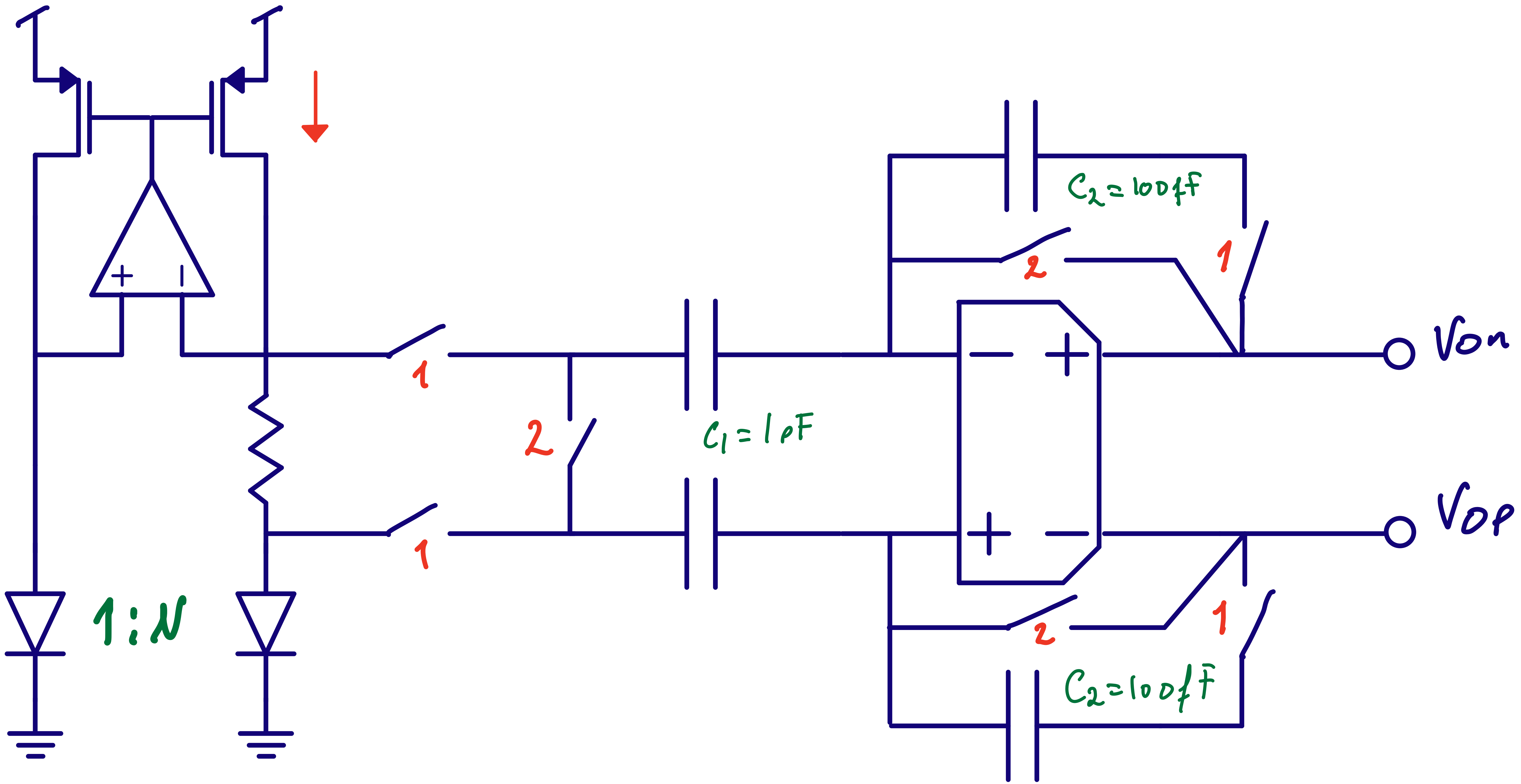
$$\sigma_{tot}^2 = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x_{tot}^2(t)dt$$

$$\sigma_{tot}^2 = \sigma_1^2 + \sigma_2^2 + \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} 2x_1(t)x_2(t)dt$$

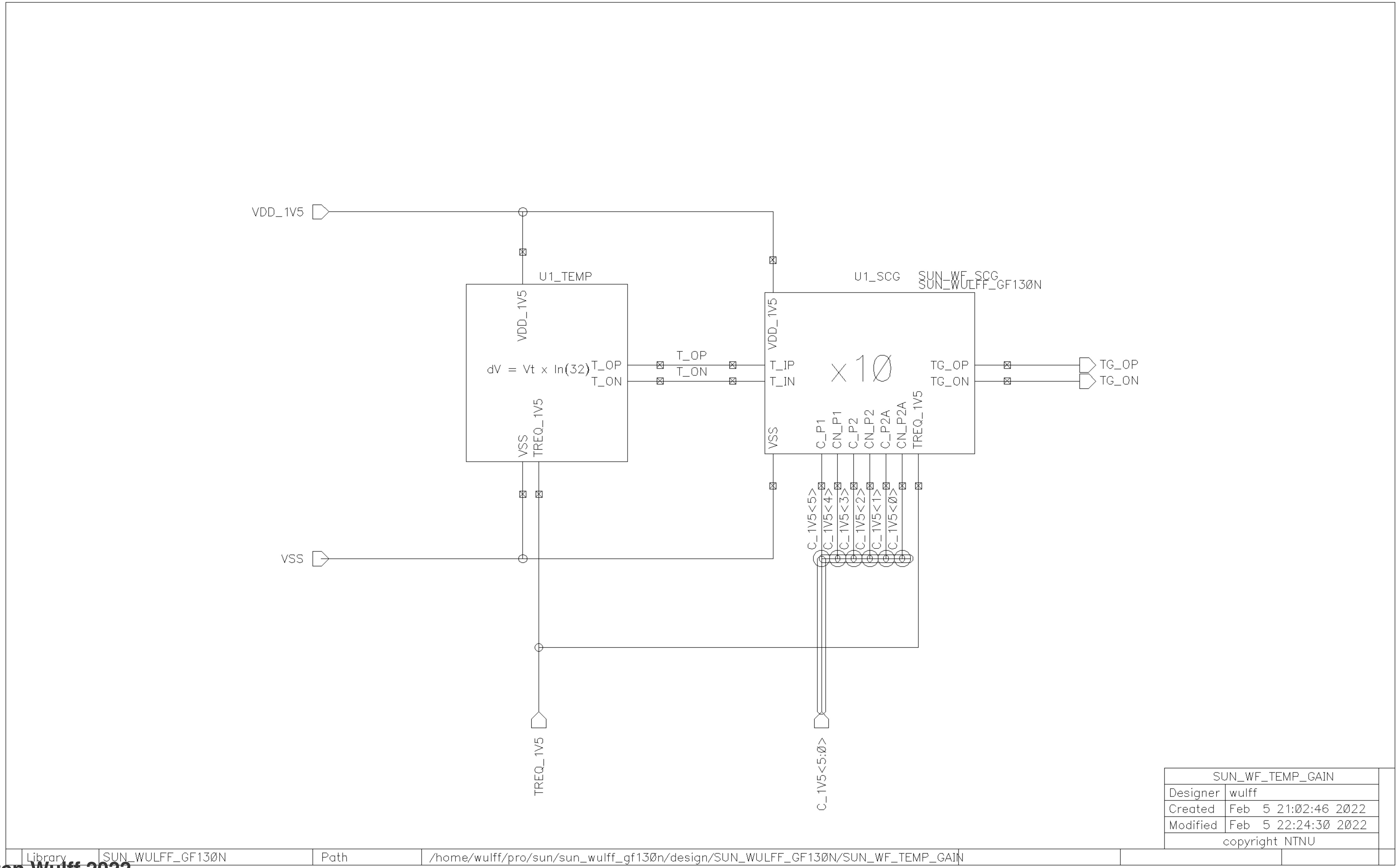
Assuming uncorrelated processes (covariance is zero), then

$$\sigma_{tot}^2 = \sigma_1^2 + \sigma_2^2$$

Example



1:N
1
1
2
$C_1 = 1pF$
$C_2 = 100fF$
$C_2 = 100fF$
2
1
2
1
Von
Vop


VDD_1V5
U1_TEMP
VDD_1V5
dV = Vt x ln(32)
T_OP
T_ON
VSS
TREQ_1V5
T_OP
T_ON
U1_SCG
SUN_WF_SCG
SUN_WULFF_GF130N
VDD_1V5
T_IP
T_IN
x10
TG_OP
TG_ON
VSS
C_P1
CN_P1
C_P2
CN_P2
C_P2A
CN_P2A
TREQ_1V5
TG_OP
TG_ON
VSS
C_1V5<5>
C_1V5<4>
C_1V5<3>
C_1V5<2>
C_1V5<1>
C_1V5<0>
TREQ_1V5
C_1V5<5:0>
SUN_WF_TEMP_GAIN
Designer wulff
Created Feb 5 21:02:46 2022
Modified Feb 5 22:24:30 2022
copyright NTNU
Library SUN_WULFF_GF130N
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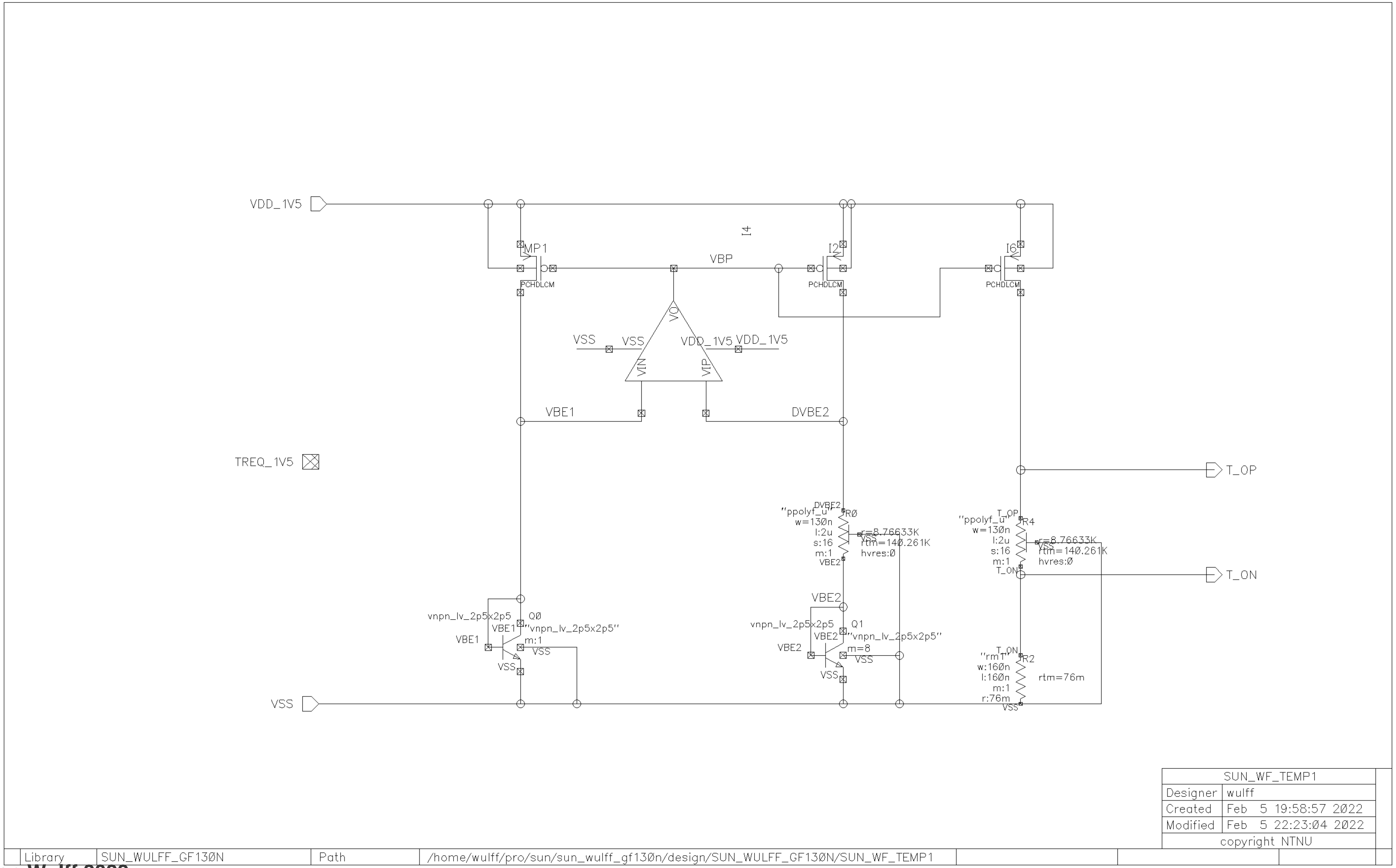
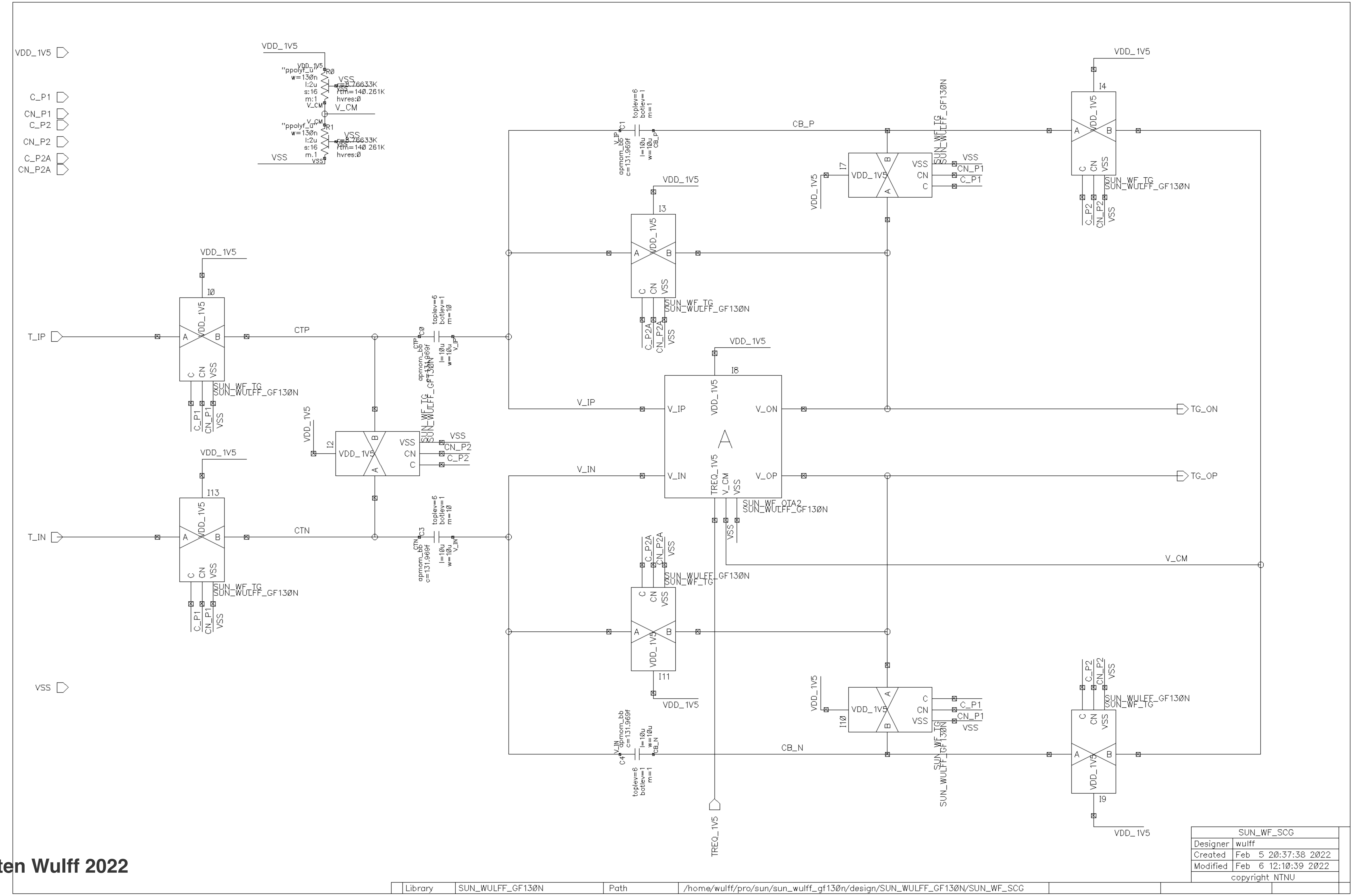

VDD_1V5
MP1
PCHDLCM
VBP
I4
I2
I6
VO
VSS
VSS
VDD_1V5
VDD_1V5
VIN
VIP
VBE1
DVBE2
TREQ_1V5
T_OP
T_ON
VSS
SUN_WF_TEMP1
Designer wulff
Created Feb 5 19:58:57 2022
Modified Feb 5 22:23:04 2022
copyright NTNU
Library SUN_WULFF_GF130N
Path /home/wulff/pro/sun/sun_wulff_gf130n/design/SUN_WULFF_GF130N/SUN_WF_TEMP1


VDD_1V5
C_P1
CN_P1
C_P2
CN_P2
C_P2A
CN_P2A
VSS
T_IP
T_IN
V_CM
CTP
CTN
CB_P
CB_N
V_IP
V_IN
V_ON
V_OP
TG_ON
TG_OP
TREQ_1V5
SUN_WF_TG
SUN_WULFF_GF130N
SUN_WF_OTA2
SUN_WF_SCG
Designer wulff
Created Feb 5 20:37:38 2022
Modified Feb 6 12:10:39 2022
copyright NTNU
Library SUN_WULFF_GF130N
Path /home/wulff/pro/sun/sun_wulff_gf130n/design/SUN_WULFF_GF130N/SUN_WF_SCG

Virtuoso® ADE Assembler Editing: TB_SUN_WULFF_GF130N TB_SUN_SC_TEMP_GAIN maestro

un EAD Parasitics/LDE Window Calibre Help

Basic

No Sweeps | Single Run, Sweeps and Corners | Reference:

Outputs Setup | Results

Detail | Filter ... | Replace | (None)

Parameter	t_sweep_0	t_sweep_1	t_sweep_2	t_sweep_3	t_sweep_4	t_sweep_5	t_sweep_6	t_sweep_7	t_sweep_8	t_sweep_9
bjt.scs	Bt	Bt	Bt	Bt	Bt	Bt	Bt	Bt	Bt	Bt
cap.scs	Ct	Ct	Ct	Ct	Ct	Ct	Ct	Ct	Ct	Ct
common.scs	Gt	Gt	Gt	Gt	Gt	Gt	Gt	Gt	Gt	Gt
diode.scs	Dt	Dt	Dt	Dt	Dt	Dt	Dt	Dt	Dt	Dt
mos.scs	Mtt	Mtt	Mtt	Mtt	Mtt	Mtt	Mtt	Mtt	Mtt	Mtt
res.scs	Rt	Rt	Rt	Rt	Rt	Rt	Rt	Rt	Rt	Rt
supply.scs	Vt	Vt	Vt	Vt	Vt	Vt	Vt	Vt	Vt	Vt
temperature	-40	-21.67	-3.333	15	33.33	51.67	70	88.33	106.7	125
temperature.scs	Tt	Tt	Tt	Tt	Tt	Tt	Tt	Tt	Tt	Tt

10 rows

Test	Output	Spec	eig	ss/F	Min	Max	t_sweep_0	t_sweep_1	t_sweep_2	t_sweep_3	t_sweep_4	t_sweep_5	t_sweep_6	t_sweep_7	t_sweep_8	t_sweep_9
MAIN	t_op															
MAIN	t_on															
MAIN	tg_op															
MAIN	tg_on															
MAIN	dvbe															
MAIN	dvbe_x10															
MAIN	t_sample				19u	...	19u	19u	19u	19u	19u	19u	19u	19u	19u	19u
MAIN	v_dvbe				50....	...	50.8m	54.15m	57.39m	60.54m	63.61m	66.61m	69.56m	72.46m	75.33m	78.2m
MAIN	v_dvbe_x10				50...	...	502.4m	535.6m	567.6m	598.7m	629.1m	658.8m	688m	716.7m	745.1m	773.5m
MAIN	GAIN				9.89	...	9.89	9.89	9.89	9.891	9.89	9.89	9.891	9.891	9.891	9.891

In the book that you really should read

Parasitic sensitive integrator

Gain circuit that zero's OTA offset

Correlated double sampling

VCO

Peak detectors

Thanks!