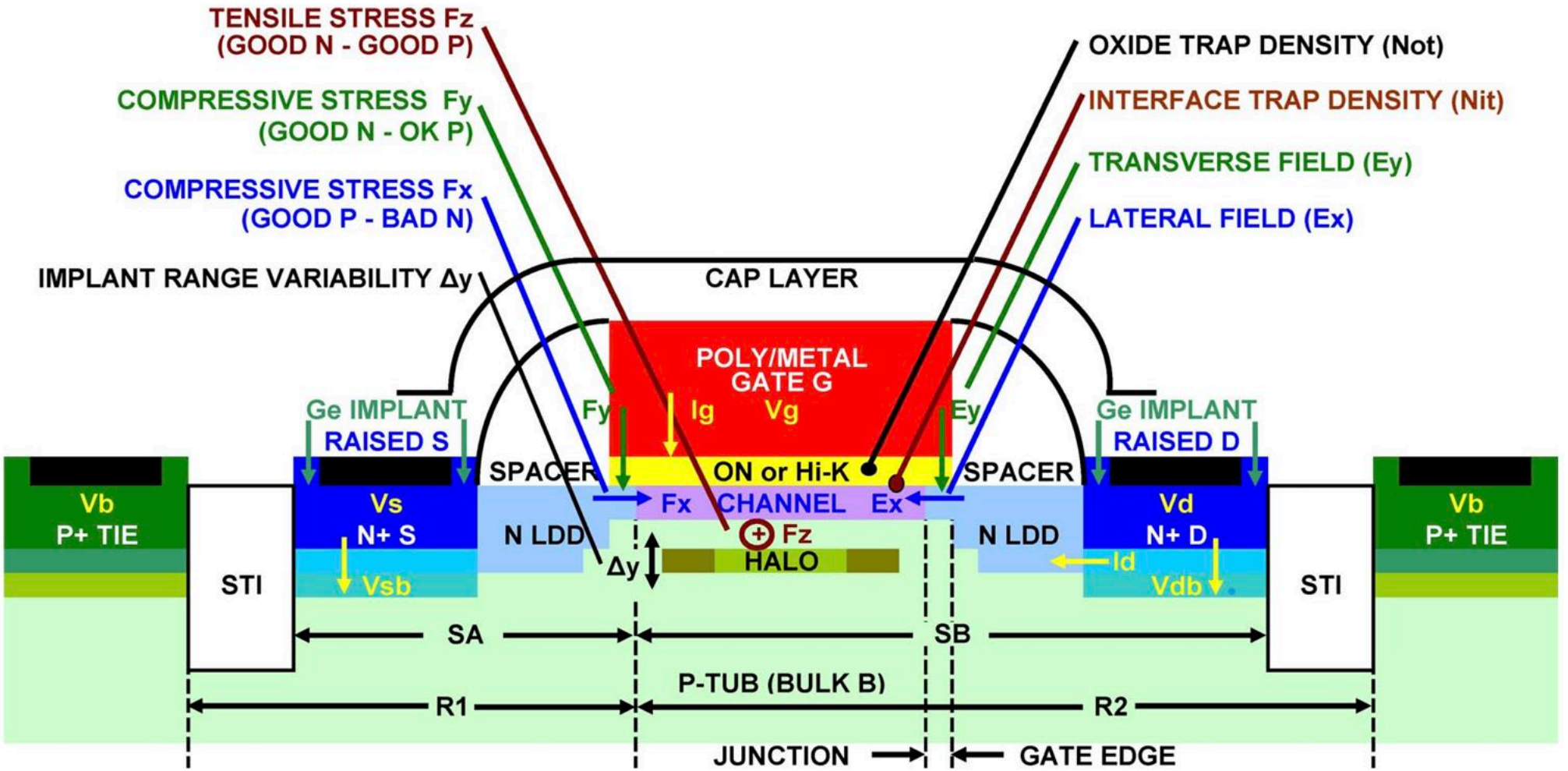

Fig. 2. ***NMOS cross-section. In addition to stress from cap layers and Ge raised source-drain (S-D) implants, device dimensions such as distance from source-channel boundary to nearby STI (SA and SB), proximity and regularity of overlying metal patterns, and short distances to other device patterns within the local*** $(< 2\ \mu m)$ ***stress field induce transverse*** (F_y) ***and lateral (*** F_x ***and*** F_z***) stress components, which affect threshold and mobility. Increasing the distance to P+ ties increases local tub (bulk) resistance components R1 and R2, which isolate the device MOS model substrate node from the device subcircuit symbol*** V_b ***node and degrade HF performance. Hot carrier reliability stress is dependent on the sum of transverse and lateral fields*** E_y ***and*** E_x***. These fields are increased near the drain by increasing source to bulk*** (V_{sb}) ***and drain*** (V_d) ***to gate*** (V_g) ***or source*** (V_s) ***voltages in various combinations. As hot carrier stress increases, damage to channel from interface trap density*** (N_{it}) ***affects threshold and mobility, while gate oxynitirde (ON) or high-dielectric-constant (Hi-K) insulator trap density*** (N_{ot}) ***affects threshold and gate leakage.***