TFE4188 - Lecture 3

Reference and bias

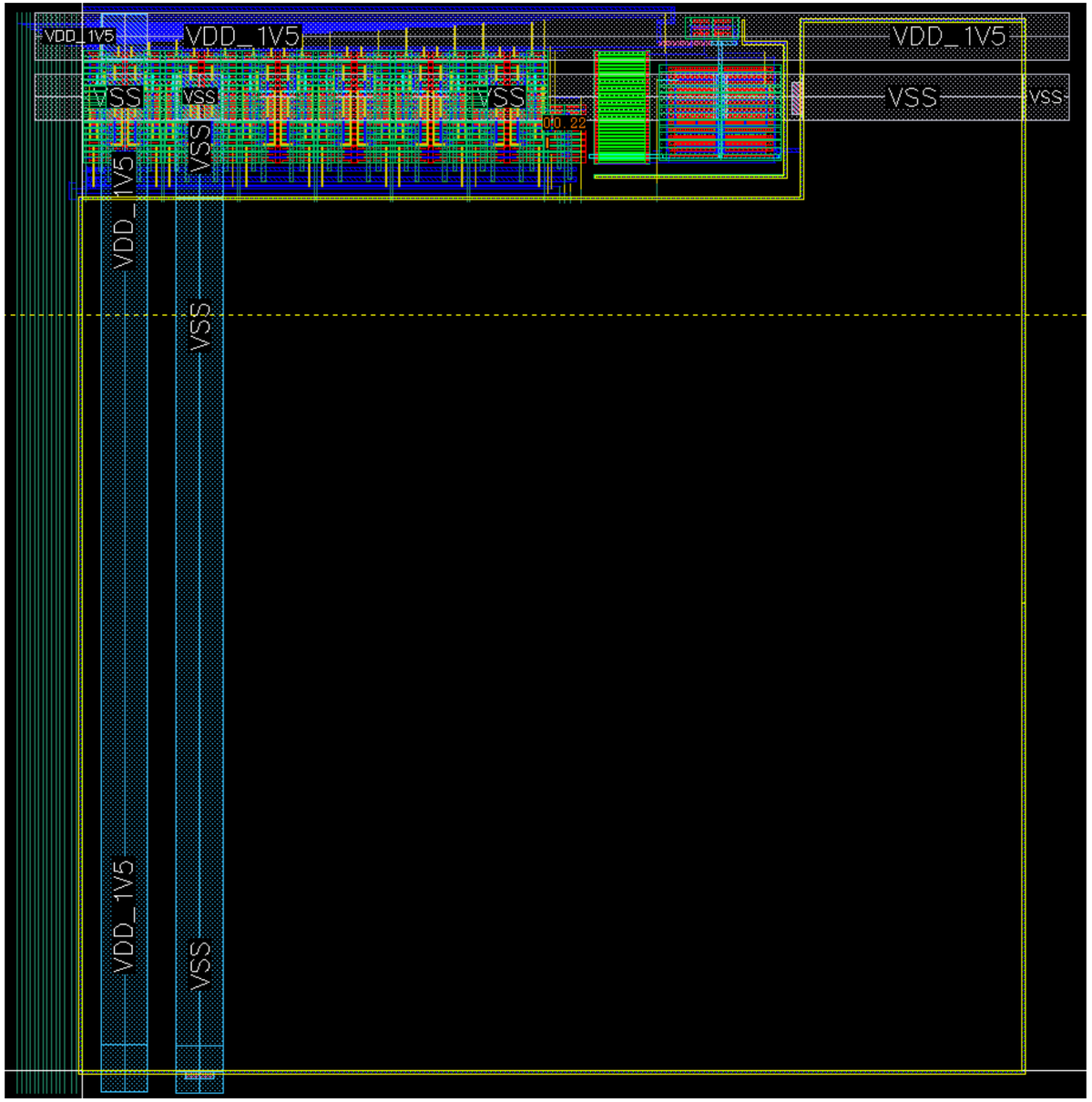
Housekeeping

Syllabus on https://github.com/wulffern/aic2022/blob/main/syllabus.md

Area of your design is constrained by SUN_AS_WRAP. You must all use that cell!

Specification review next week, you must follow the Spec checklist

Grading of the project includes the specification review


VDD_1V5
VDD_1V5
VDD_1V5
VSS
VSS
VSS
VSS
VSS
VDD_1V5
VSS
VDD_1V5
VSS

Grading of the project

Created by Carsten Wulff, last modified on 17.01.2022

The project counts for 45 % of the grade

Milestones	What does it mean	Checklist	Output	Points
M1 Specification	▪ Plan of what the circuit is going to do, and roughly how it's going to be implemented ▪ Plan of how you're going to verify functionality	Specifcation Review	Confluence	10
M2 Design review	▪ Prove functionality and performance with schematic simulation	Design Review	Confluence Schematic	10
M3 Layout review	▪ Placement, most blocks layed out	Layout Review	Confluence Schematic Layout	10
M4 Tapeout review	▪ LVS/DRC clean. Prove functionality and performance with parasitic extracted simulation	Tapeout Review	Confluence	20
Paper Design complexity / Good design descisions	▪ Write a paper describing your circuit. ▪ Your paper should look like https://ieeexplore.ieee.org/document/7906479 The source code is available https://github.com/wulffern/jssc2017 ▪ You must use the IEEEtran.cls ▪ Submitted manuscripts, describing both the theoretical and implementation aspects of an advance solid-state circuit design, are allowed to have up to 8 pages in the two-column format. This page limit is valid for the whole manuscript, but excluding references and bios. All figures must be sized such that they are properly readable. No modifications to the IEEE templates are allowed.		PDF submission on blackboard	50
Coolness factor	These are extra points.			10
Max points				**100**

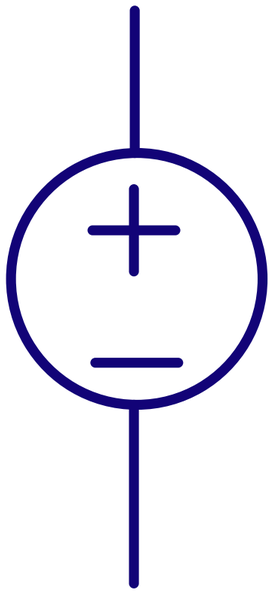
Week	Book	Monday	Project plan	Exercise
2	CJM 1-6	Course intro, what I expect you to know, project, analog design fundamentals	Specification	
3	Slides	ESD and IC Input/Output	Specification	x
4	CJM 7,8	**Reference and bias**	Specification	
5	CJM 12	Analog Front-end	M1. Specification review	x
6	CJM 11-14	Switched capacitor circuits	Design	
7	JSSC, CJM 18	State-of-the-art ADCs	Design	x
8	Slides	Low power radio recievers	Design	
9	Slides	Communication standards from circuit perspective	M2. Design review	x
10	CJM 7.4, CFAS,+DC/DC	Voltage regulation	Layout	
11	CJM 19, CFAS	Clock generation	M3. Layout review	x
12	Paper	Energy sources	Layout/LPE simulation	
13	Slides	Chip infrastructure	Layout/LPE simulation	x
14		Tapeout review	M4. Tapeout review	
15		Easter		
16		Easter		
17		Exam repetition		

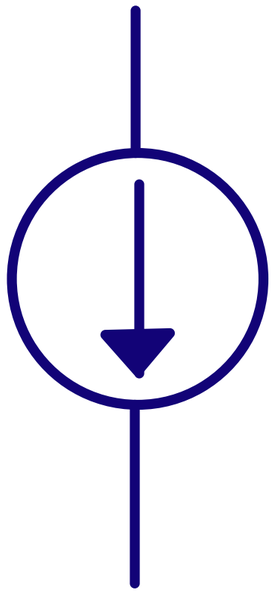
Goal for today

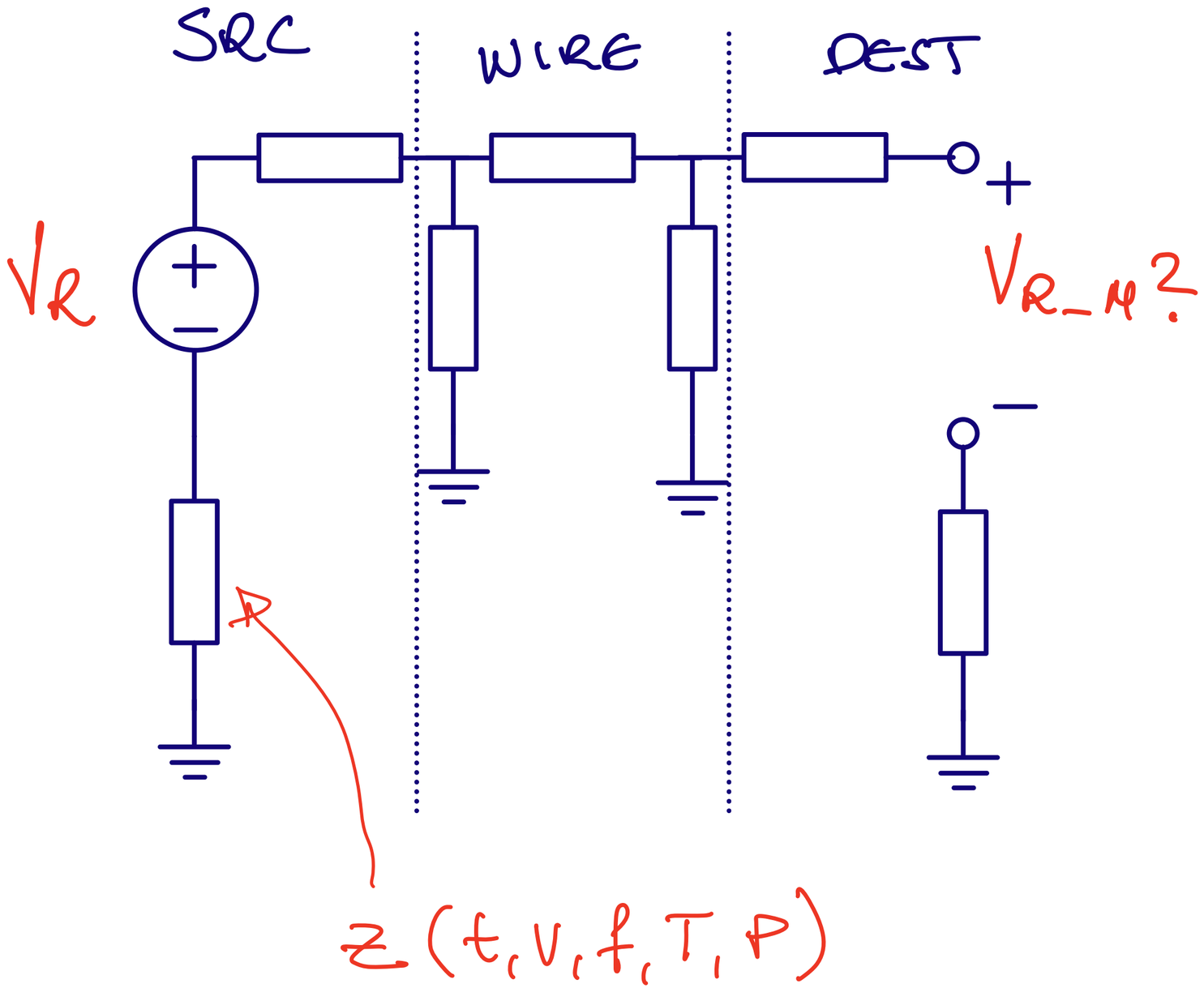
Understand **why** we need reference and bias circuits

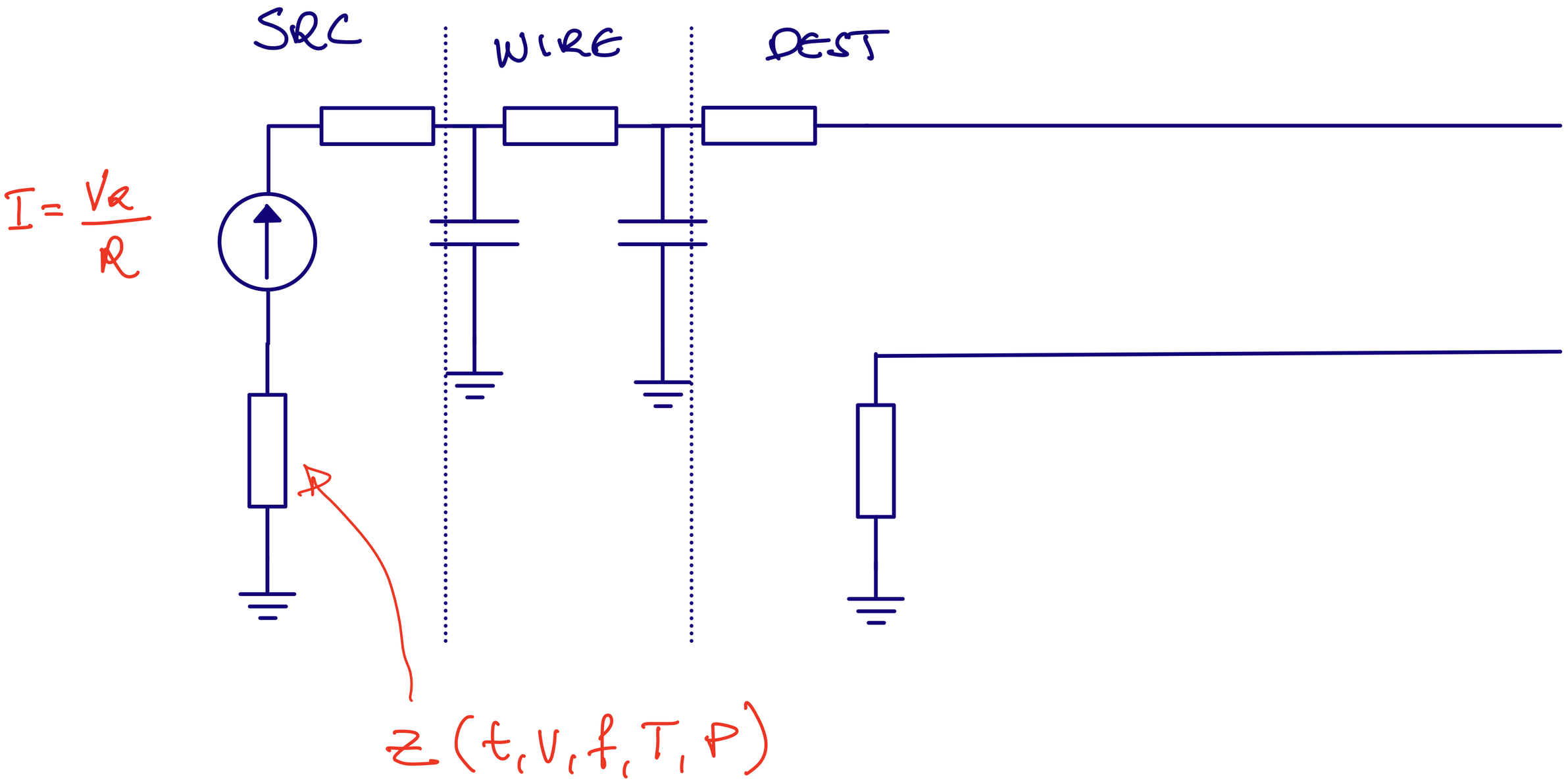
Introduction to **circuit architectures**

Why





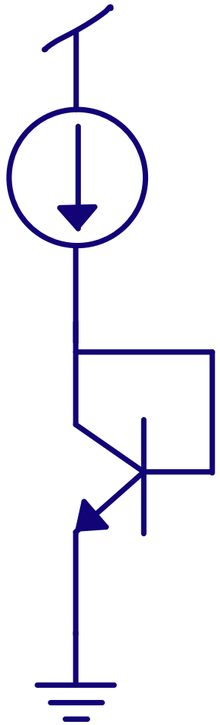

SRC
WIRE
DEST
+
V_R
V_{R_M}?
−
R
$Z(t, V, f, T, P)$

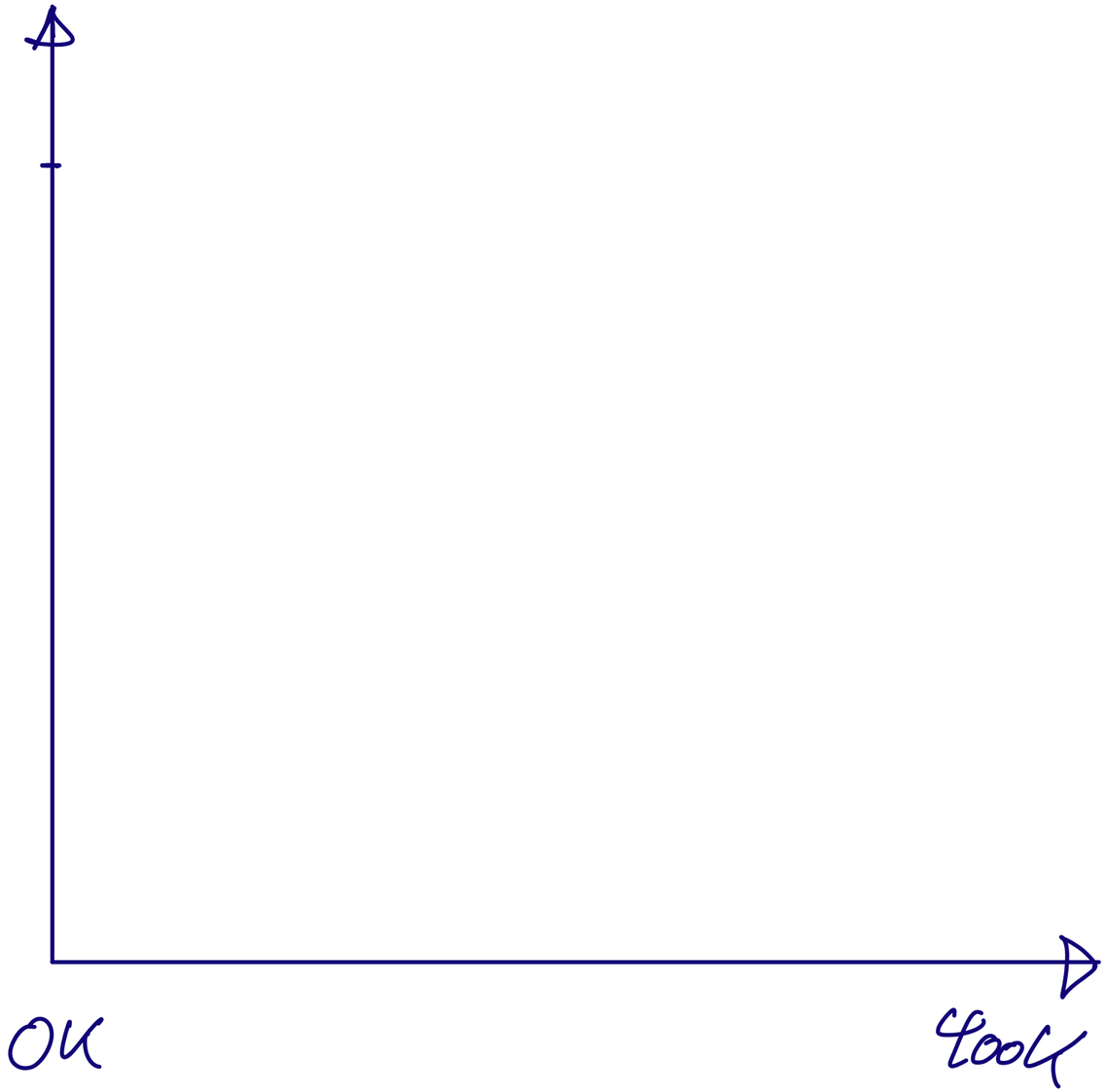

SRC
WIRE
DEST
$I = \frac{V_R}{R}$
R
$Z(t, V, f, T, P)$

What quantity do we have access to on an IC that is independent of PVT?

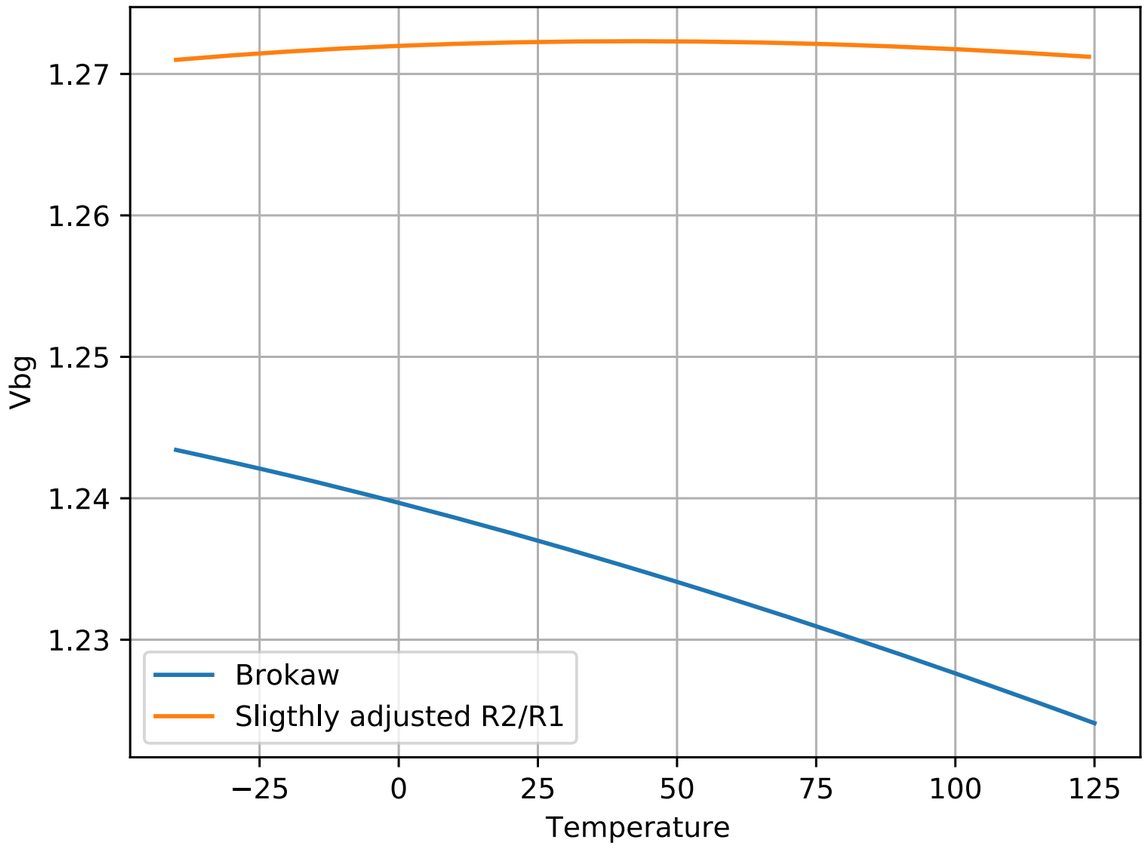
....

Bandgap voltage reference

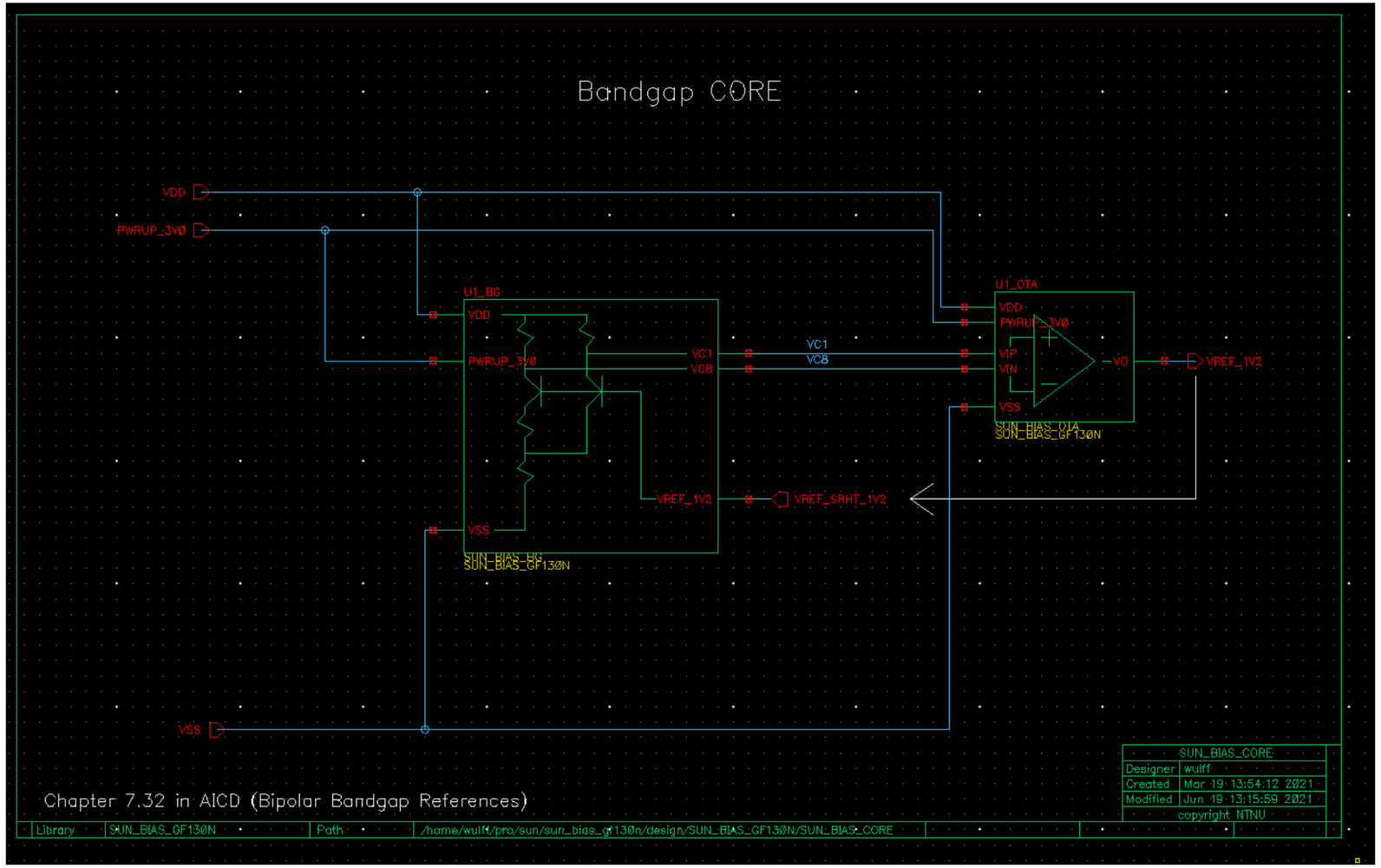


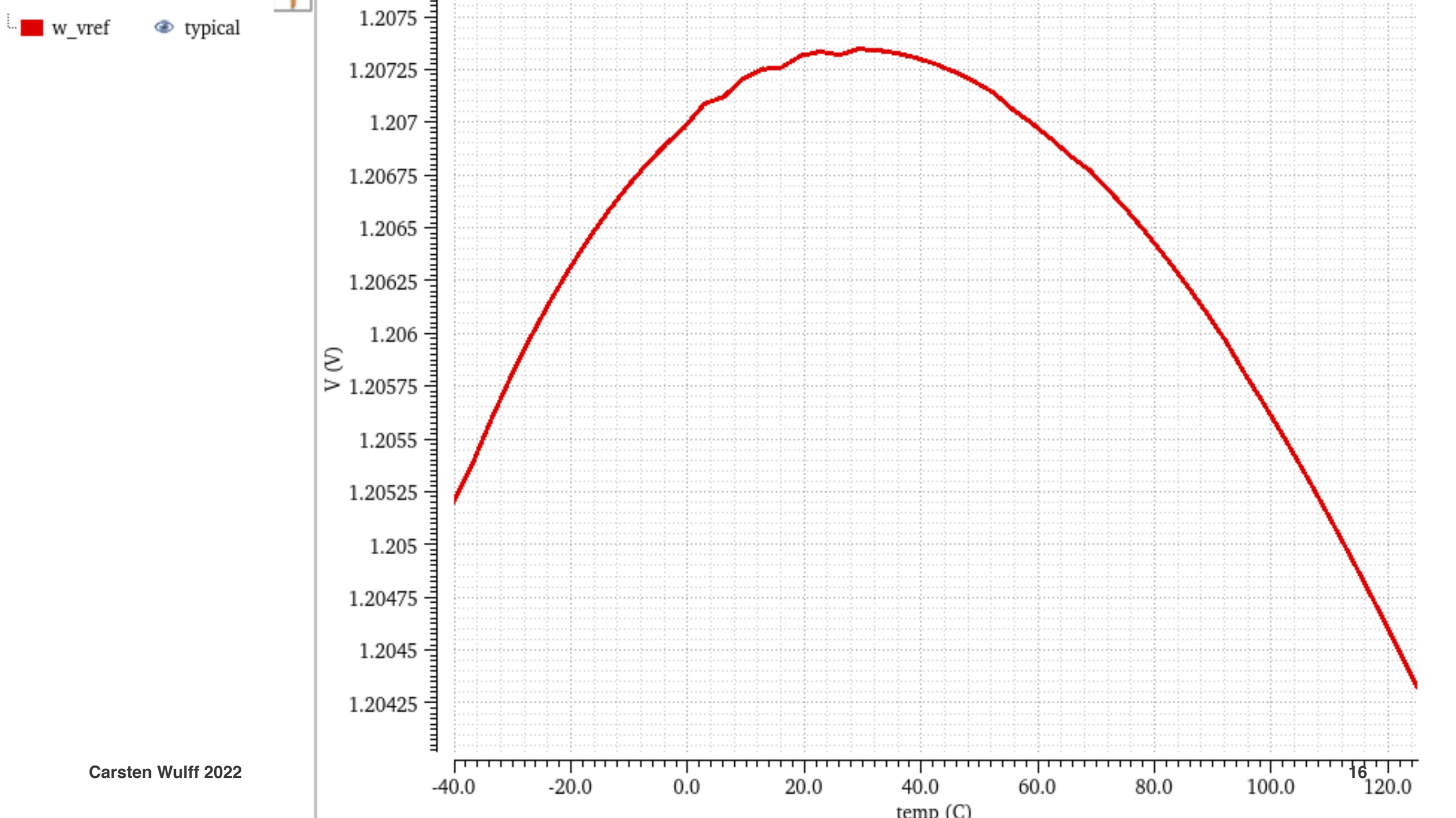

0V
4ooV

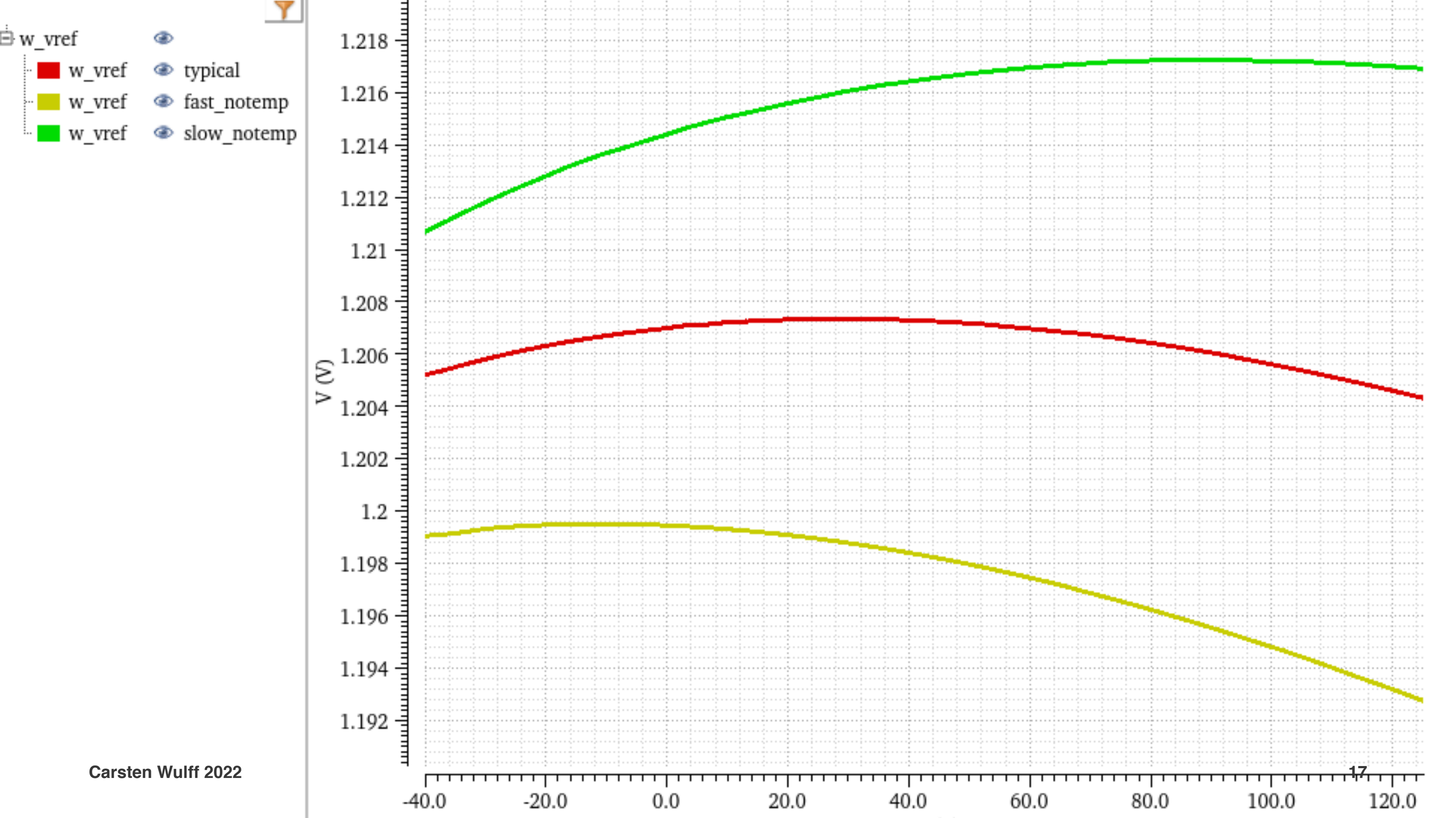
sun/sun_bias_gf130n/go/

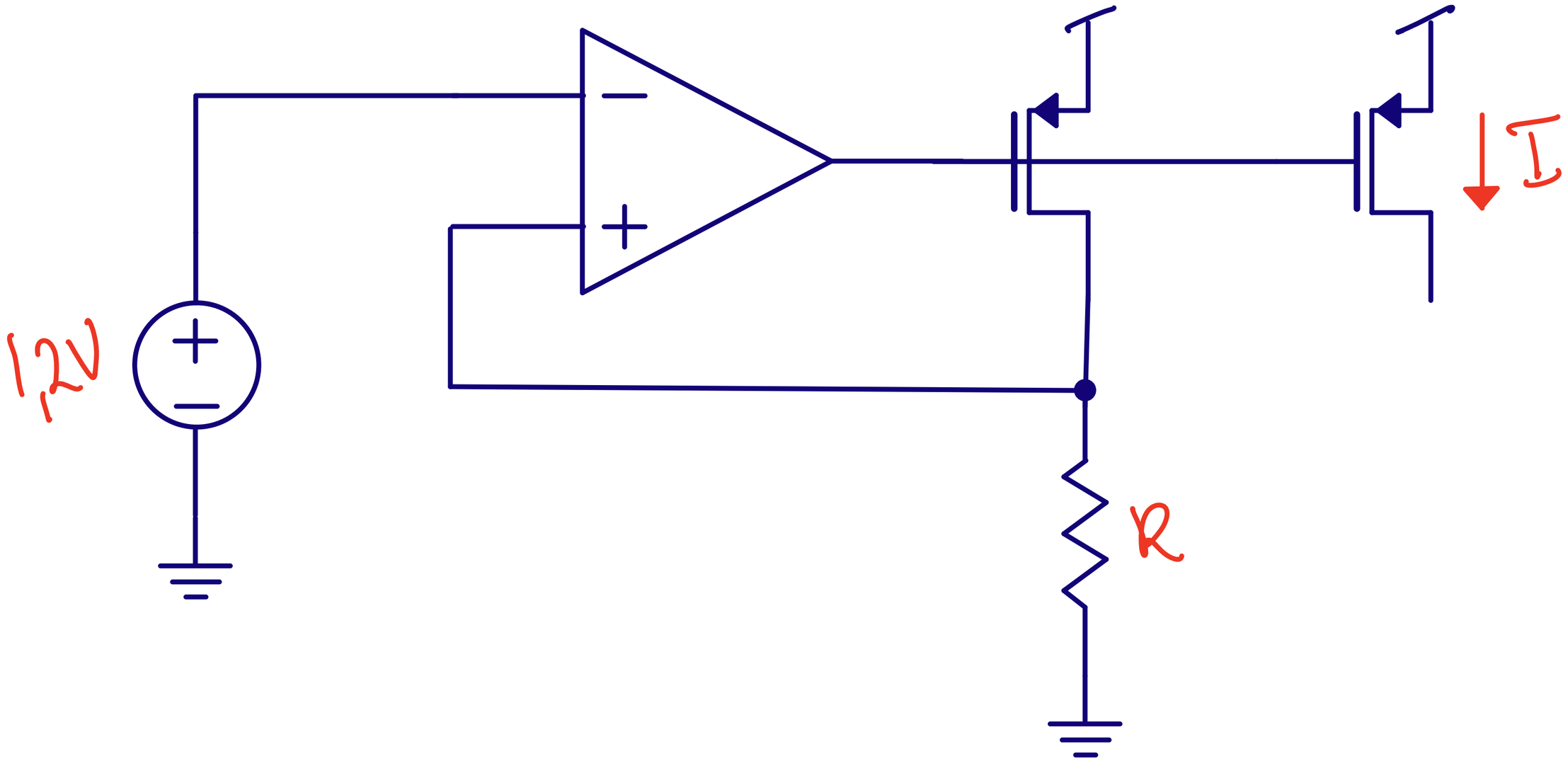


sun/sun_bias_gf130n/design/SUN_BIAS_GF130N/SUN_BIAS_CORE

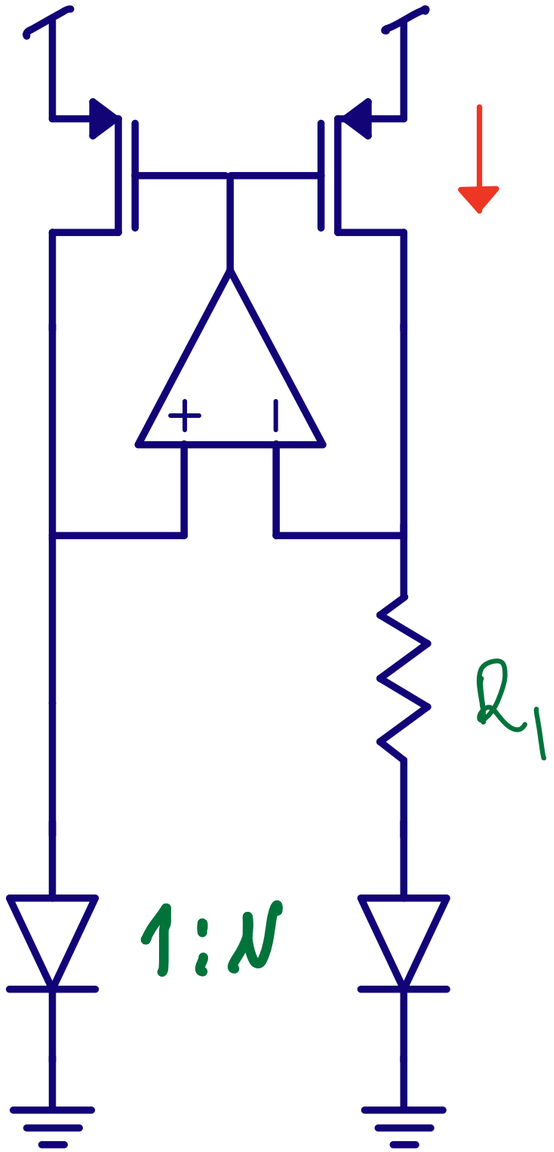


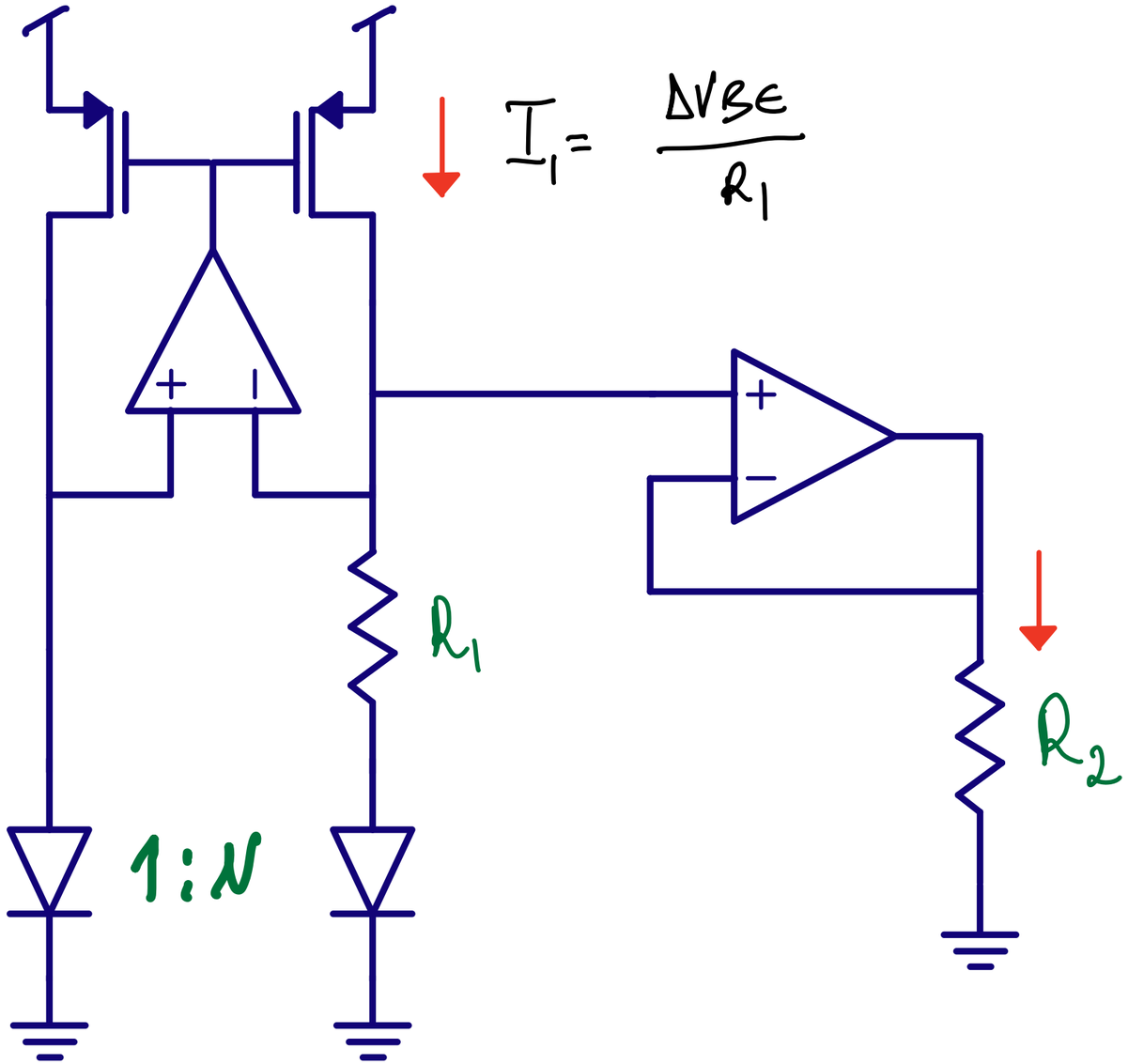

w_vref
typical
1.2075
1.20725
1.207
1.20675
1.2065
1.20625
1.206
1.20575
1.2055
1.20525
1.205
1.20475
1.2045
1.20425
V (V)
-40.0
-20.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
temp (C)

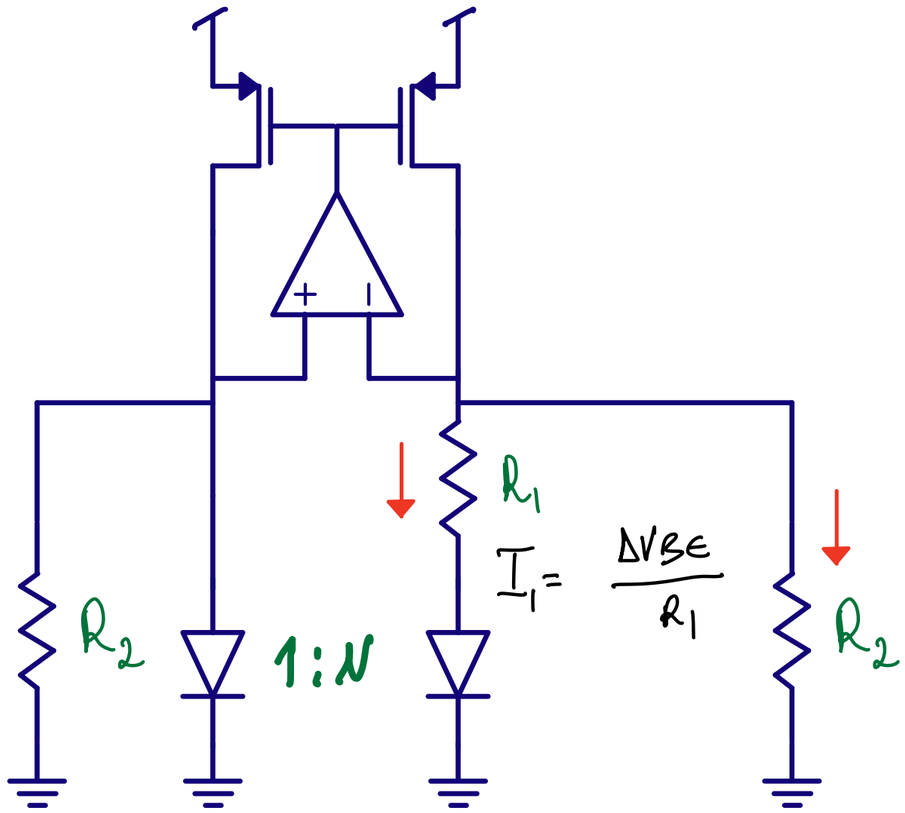

w_vref
w_vref
typical
w_vref
fast_notemp
w_vref
slow_notemp
V (V)
1.218
1.216
1.214
1.212
1.21
1.208
1.206
1.204
1.202
1.2
1.198
1.196
1.194
1.192
-40.0
-20.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0


12V
R
I

Low voltage bandgap

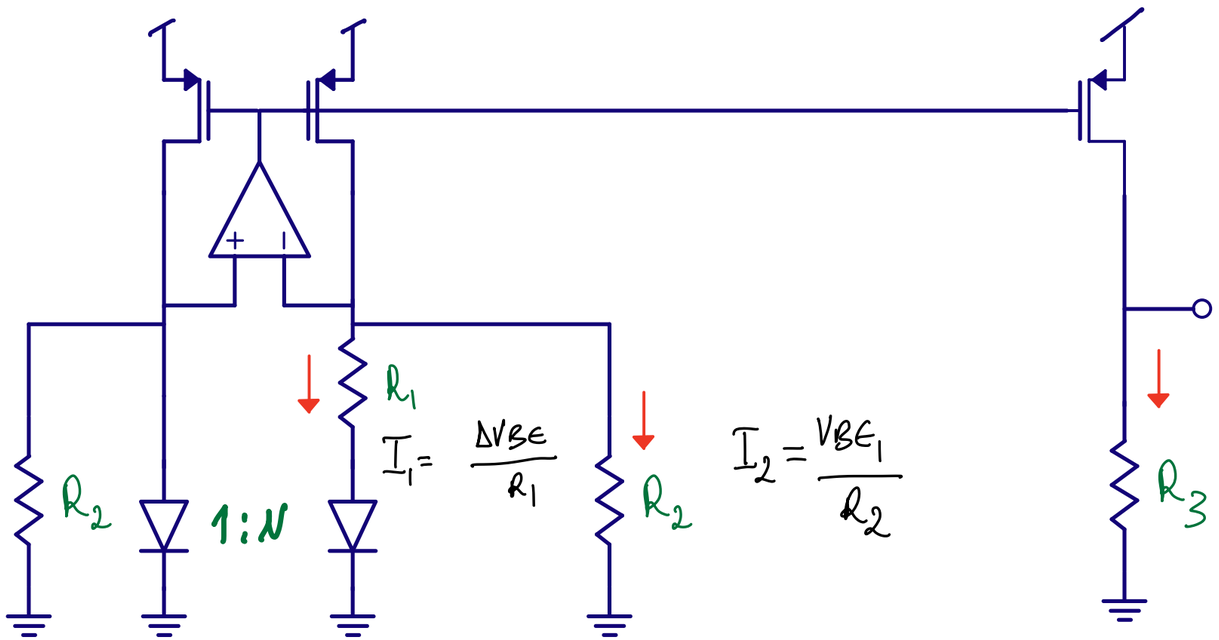

+
-
R_1
1:N


$I_1 = \frac{\Delta V_{BE}}{R_1}$
+
1
+
−
R_1
R_2
1 : N



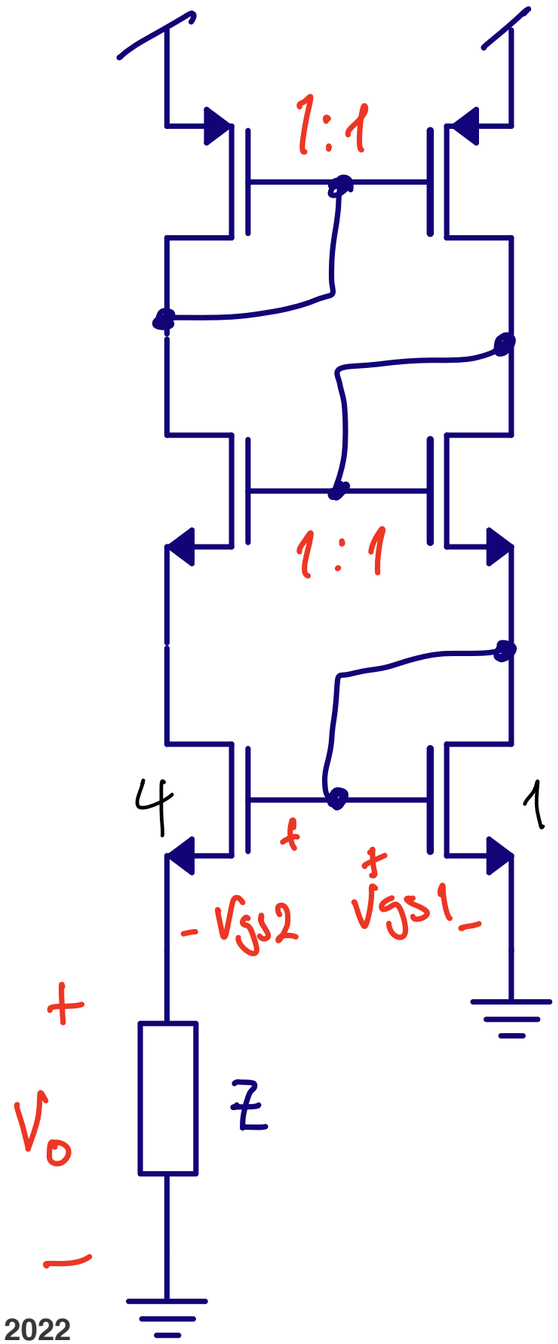
$$I_1 = \frac{\Delta V_{BE}}{R_1}$$

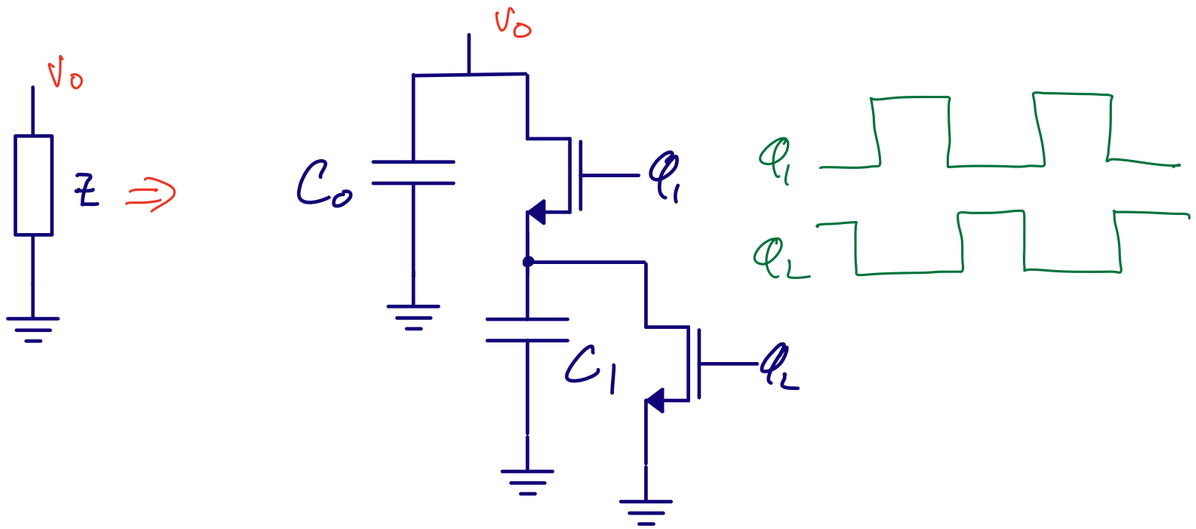
$$I_2 = \frac{V_{BE_1}}{R_2}$$

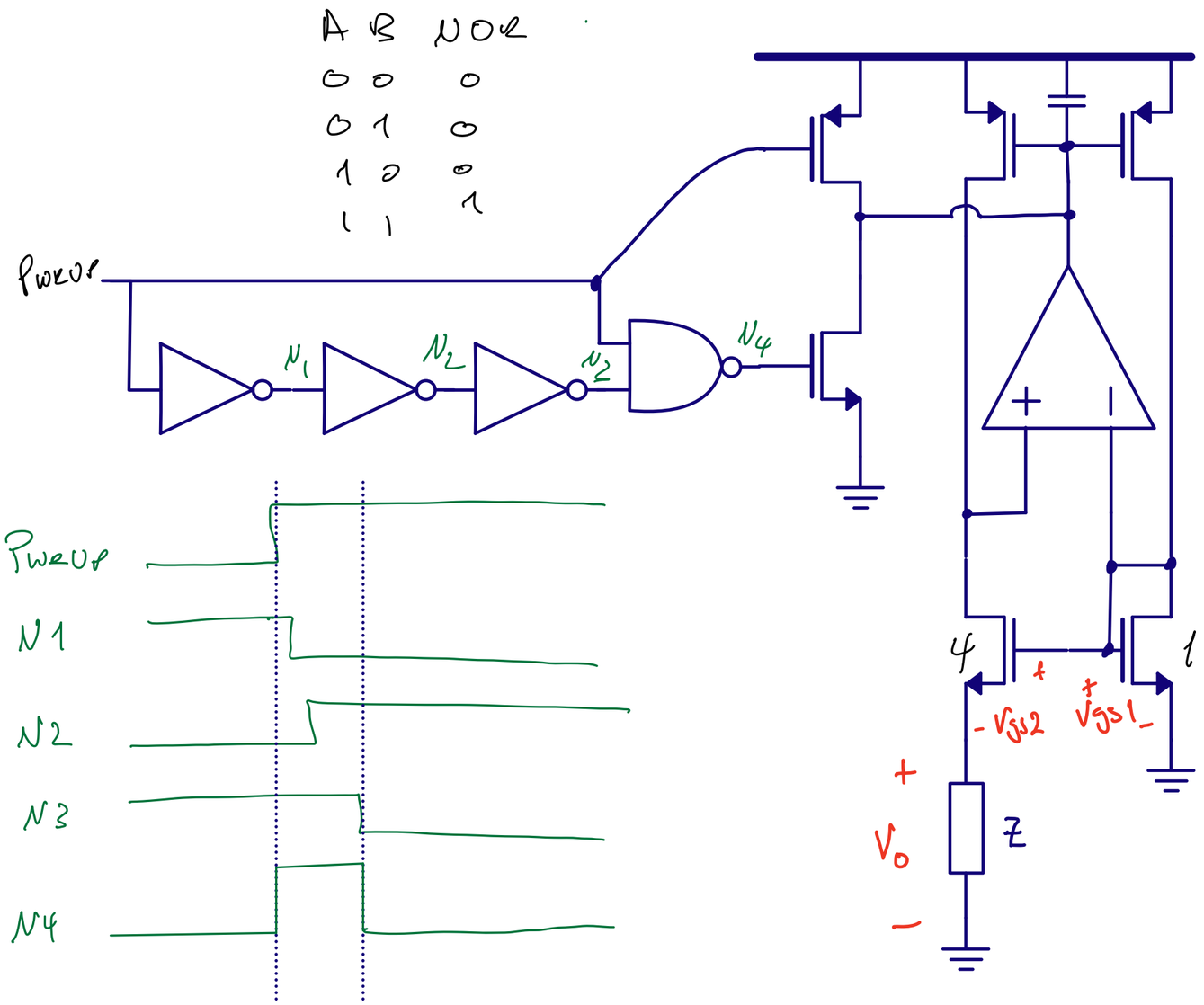

+
-
R1
I1 = ΔVBE / R1
R2
1:N
R2
I2 = VBE1 / R2
R3

Bias

Sometimes we just need a current


1:1
1:1
4
1
+
-
+
-
$-V_{gs2}$
V_{gs1}
+
V_0
-
Z


V_0
Z
V_0
C_0
Q_1
C_1
Q_2
Q_1
Q_2


A B NOR
0 0 0
0 1 0
1 0 0
1 1 1
PWRUP
N1
N2
N3
N4
PWRUP
N1
N2
N3
N4
4
1
- Vgs2
+ Vgs1 -
+
Vo
-
Z

Thanks!