TFE4188 - Lecture 1

ESD and I/O

Housekeeping

Groups sets on blackboard, make sure you sign up this week. The username you get does not have to correspond to your AIC group name.

Change of review plan. Moved spec, design, layout and tapeout review to better match exercises

According to the updated plan, we'll have the specification review in two weeks. To complete that, you should fill in a confluence page with the plan for the design. Follow Specification Checklist

Exam will likely be oral

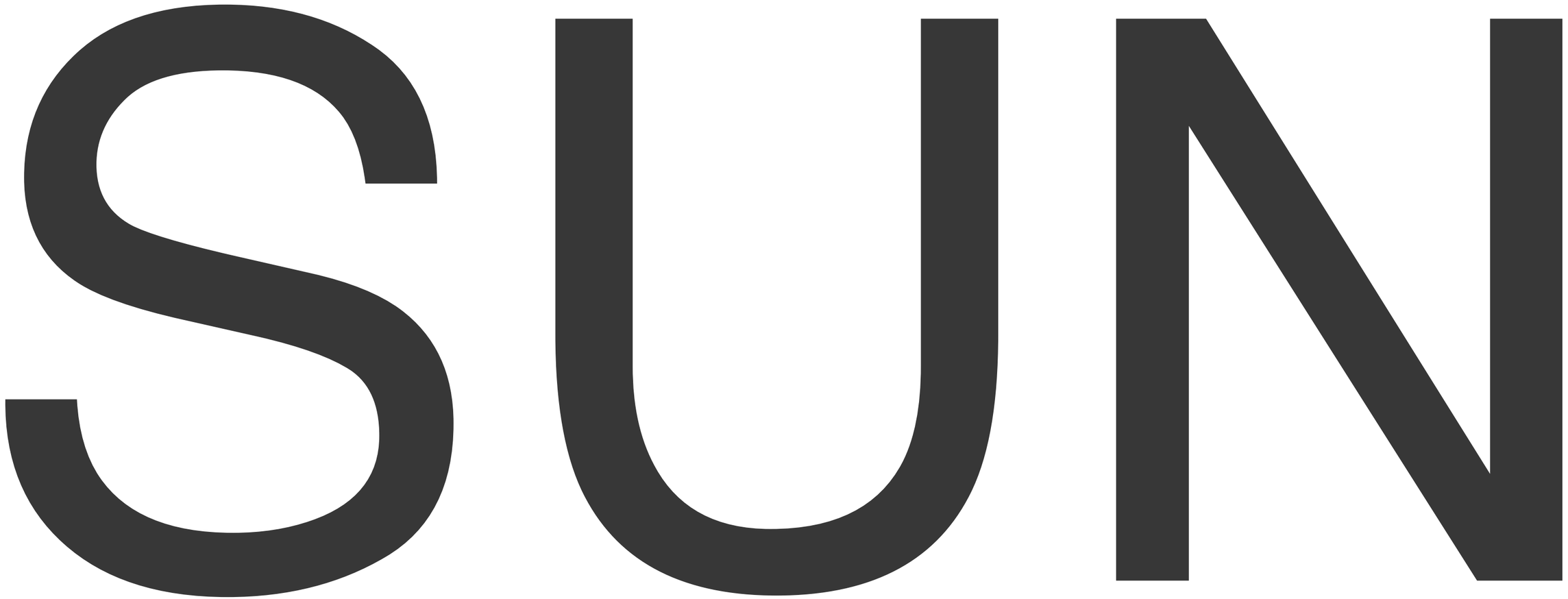
Will start f2f lectures from next week (24'th of January) in F6 gamle fysikk

Week	Book	Monday	Project plan	Exercise
2	CJM 1-6	Course intro, what I expect you to know, project, analog design fundamentals	Specification	
3	Slides	ESD and IC Input/Output	Specification	x
4	CJM 7,8	Reference and bias	Specification	
5	CJM 12	Analog Front-end	M1. Specification review	x
6	CJM 11-14	Switched capacitor circuits	Design	
7	JSSC, CJM 18	State-of-the-art ADCs	Design	x
8	Slides	Low power radio recievers	Design	
9	Slides	Communication standards from circuit perspective	M2. Design review	x
10	CJM 7.4, CFAS,+DC/DC	Voltage regulation	Layout	
11	CJM 19, CFAS	Clock generation	M3. Layout review	x
12	Paper	Energy sources	Layout/LPE simulation	
13	Slides	Chip infrastructure	Layout/LPE simulation	x
14		Tapeout review	M4. Tapeout review	
15		Easter		
16		Easter		
17		Exam repetition		

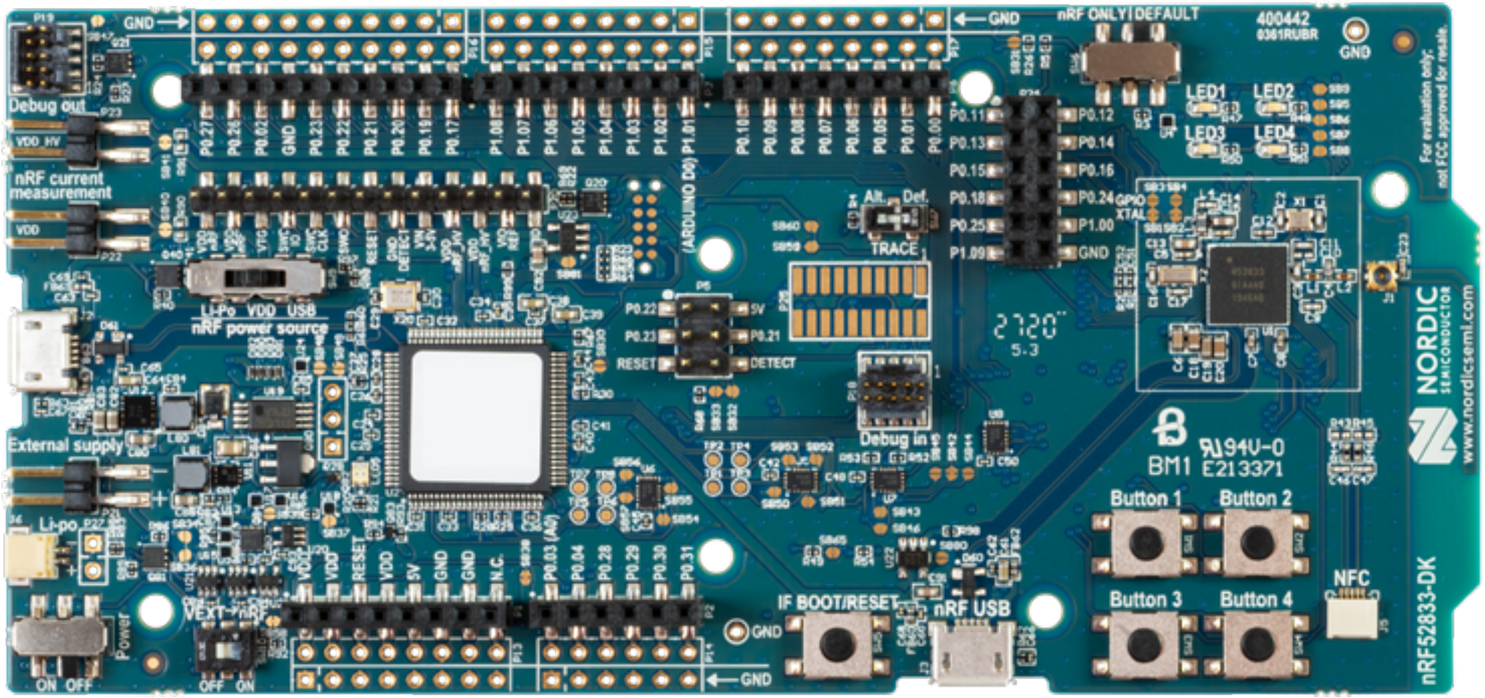
Goal for today

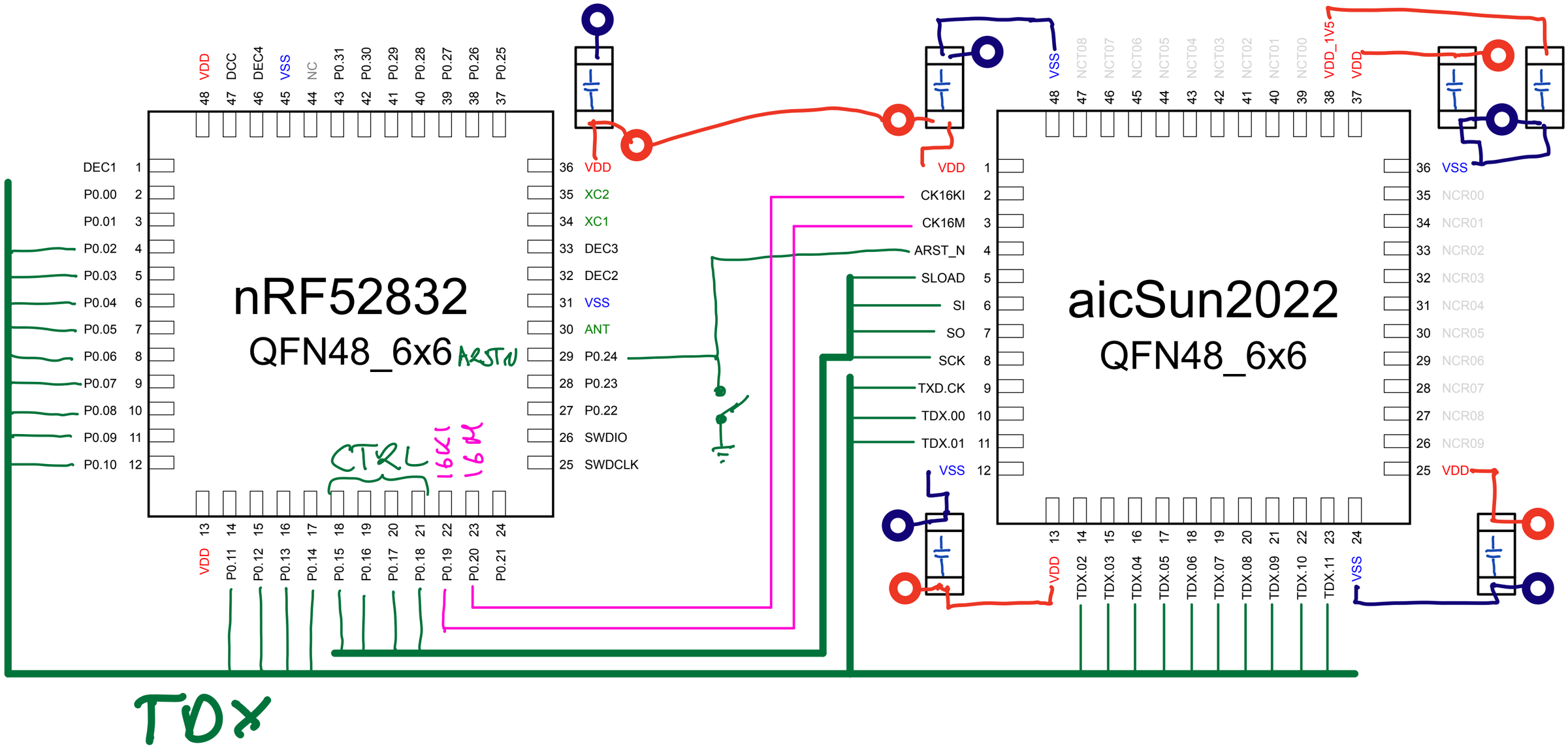
Understand the **real-world** constraints on our IC

Understand why you must **always handle ESD** on an IC

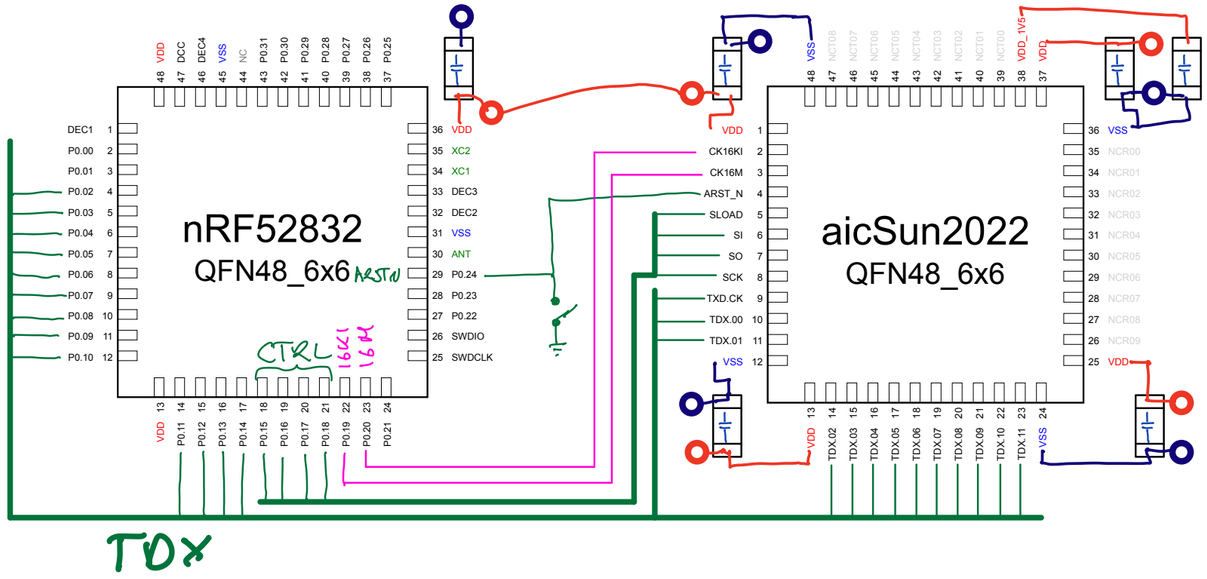

SUN

Plan: Make SUN PCB as a shield on top of a nRF52xxx Design Kit




nRF52832
QFN48_6x6
ARSTN
CTRL
16KI
16M
DEC1 1
P0.00 2
P0.01 3
P0.02 4
P0.03 5
P0.04 6
P0.05 7
P0.06 8
P0.07 9
P0.08 10
P0.09 11
P0.10 12
36 VDD
35 XC2
34 XC1
33 DEC3
32 DEC2
31 VSS
30 ANT
29 P0.24
28 P0.23
27 P0.22
26 SWDIO
25 SWDCLK
VDD 48
DCC 47
DEC4 46
VSS 45
NC 44
P0.31 43
P0.30 42
P0.29 41
P0.28 40
P0.27 39
P0.26 38
P0.25 37
VDD 13
P0.11 14
P0.12 15
P0.13 16
P0.14 17
P0.15 18
P0.16 19
P0.17 20
P0.18 21
P0.19 22
P0.20 23
P0.21 24
aicSun2022
QFN48_6x6
VDD 1
CK16KI 2
CK16M 3
ARST_N 4
SLOAD 5
SI 6
SO 7
SCK 8
TXD.CK 9
TDX.00 10
TDX.01 11
VSS 12
36 VSS
35 NCR00
34 NCR01
33 NCR02
32 NCR03
31 NCR04
30 NCR05
29 NCR06
28 NCR07
27 NCR08
26 NCR09
25 VDD
VSS 48
NCT08 47
NCT07 46
NCT06 45
NCT05 44
NCT04 43
NCT03 42
NCT02 41
NCT01 40
NCT00 39
VDD_1V5 38
VDD 37
VDD 13
TDX.02 14
TDX.03 15
TDX.04 16
TDX.05 17
TDX.06 18
TDX.07 19
TDX.08 20
TDX.09 21
TDX.10 22
TDX.11 23
VSS 24
TDX

Name	Min/Typ/Max	Comment
VDD	2.4 / 3.0 / 3.6	Supplied from nRF52DK. Second midlayer on SUN PCB
VDD_1V5	1.35 / 1.5 / 1.65	Internal LDO on SUN (Optional)
VSS	0	First midlayer on SUN PCB



Purpose

- Provide power to the IC
- Provide path for ESD currents

CK16KI

Digital output from LFXO on nRF52 (32768/2) via GPIOTE. Digital input on SUN

CK8M [1]

Digital output from HFCLK on nRF52 via PPI to GPIOTE. Digital input on SUN

---

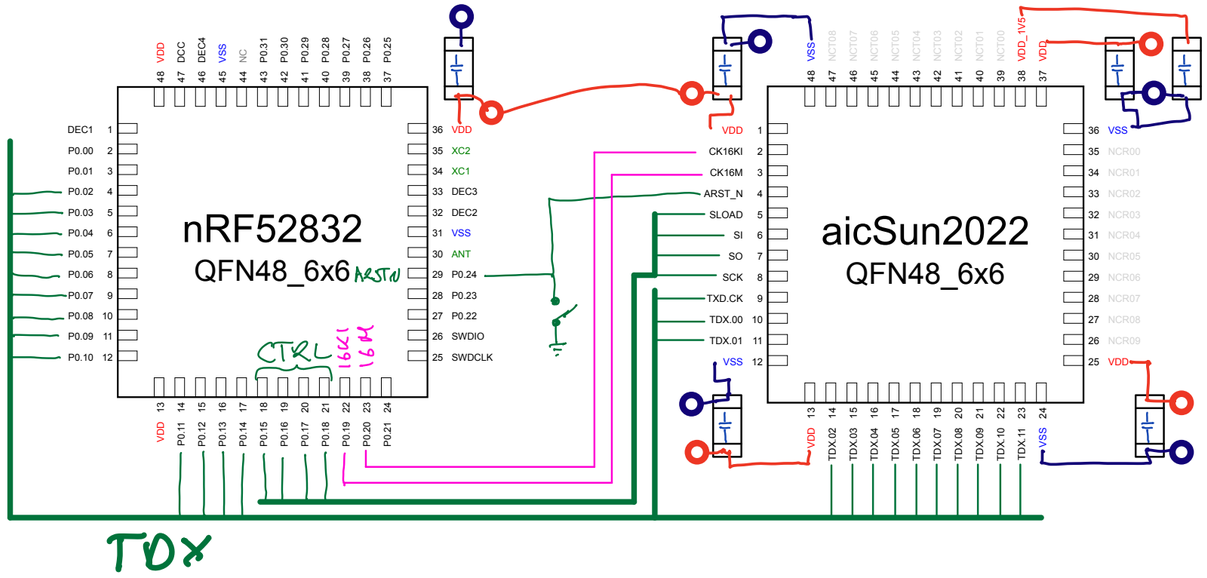
[1] After some thought. I don't think I can get 16MHz clock out of nRF52. The GPIO on nRF52 runs at 16 MHz, so 8 MHz is probably the highest we can go.

ARST_N

Active low reset.

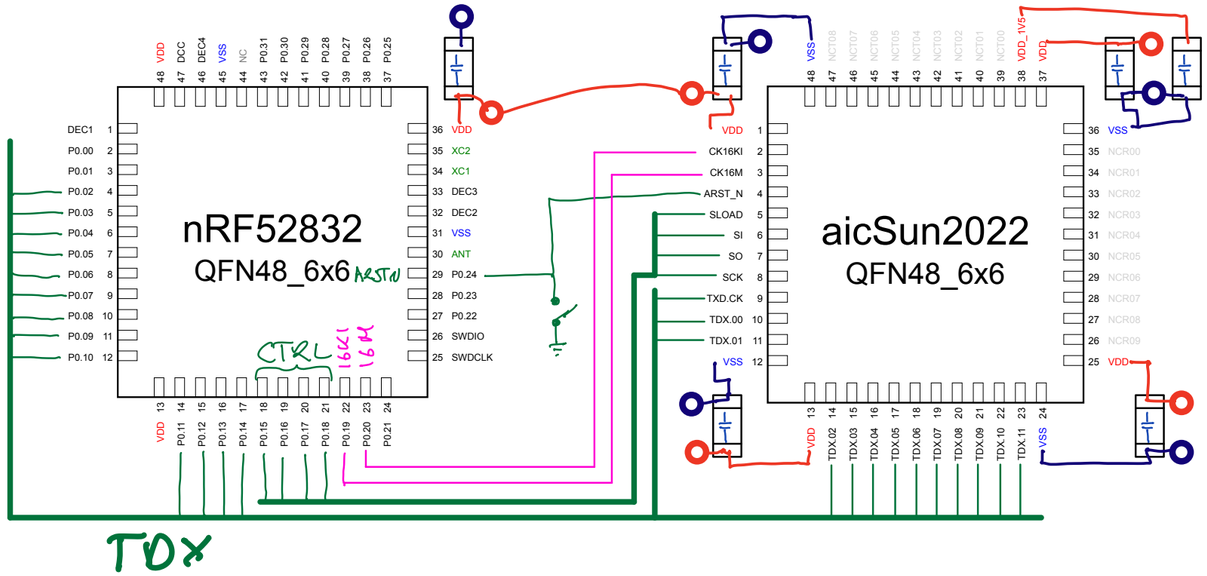
Output from nRF52 GPIO so we can do software reset, but also include a reset button on the PCB, just in case.

Ensures that all flip-flops are in a known state before we start to configure SUN



Control

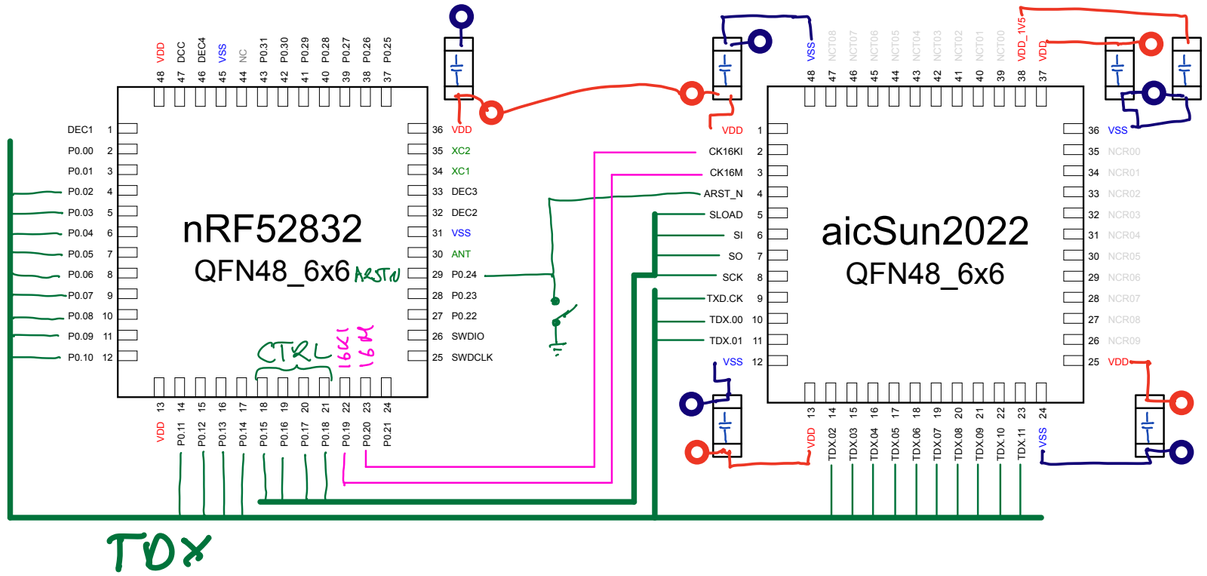
Name	Note	SUN
SLOAD	Serial load	Input
SCK	Shift clock	Input
SI	Shift in	Input
SO	Shift out	Output



Long shift register. Bit bang SI and SCK from nRF52. When all bits are shifted in, then set SLOAD high to load the control word.

TXD and TXD_CK

Name	Note	SUN
TXD	12-bit Digital output	Output
TXD_CK	Sample TXD on rising edge of TXD_CK	Output



If nRF52 is not fast enough to capture TXD at full speed, or has enough RAM to store values, then use Saleae logic analyzer.

Pin types on SUN

Type	Name	Level	ESD
Supply connected to IO ring	P_VH_EV	VDD	Connected to VDD rail. Core clamp to VSS rail
Supply to core	P_VC_EV	VDD	Pin clamp to VDD and VSS
VSS	P_VL_EV	VDD	Connected to VSS rail
Digital input	P_DI_EV	VDD	Pin clamp to VDD and VSS. Secondary protection
Digital output	P_DO_EV	VDD	Pin clamp to VDD and VSS.

The **real world** constrains our IC

Know how the real system looks before you make your design.

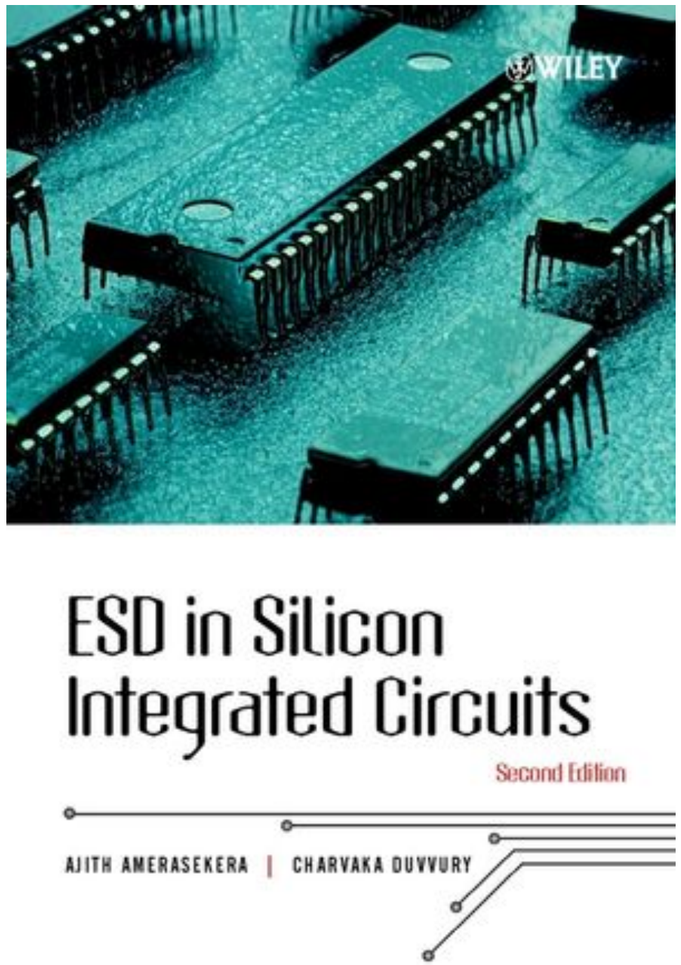
What limits voltage, temperature, input/output in testing?


ESD

Electrostatic Discharge

If you make an IC, you must consider Electrostatic Discharge (ESD) Protection circuits

Standards for testing at JEDEC



When do ESD events occur?

Before or during mounting on PCB

Human body model (HBM)

Charged device model (CDM)

After mounting on PCB

Human body model (HBM)

System level ESD

Human body model (HBM)

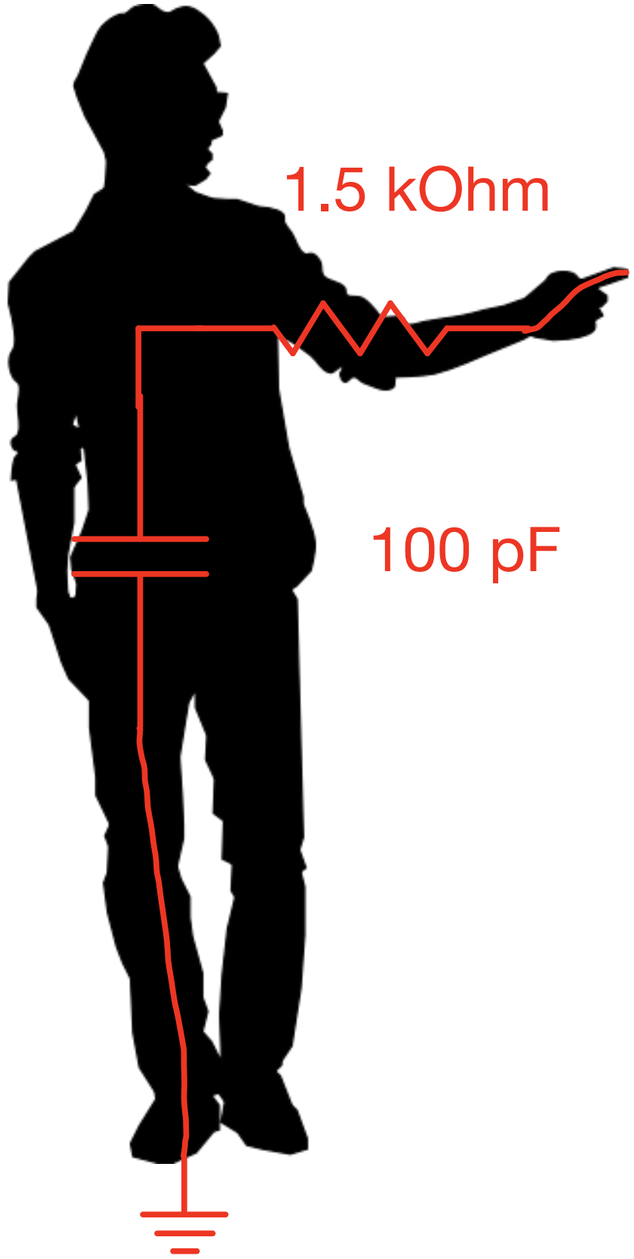
Models a person touching a device with a finger

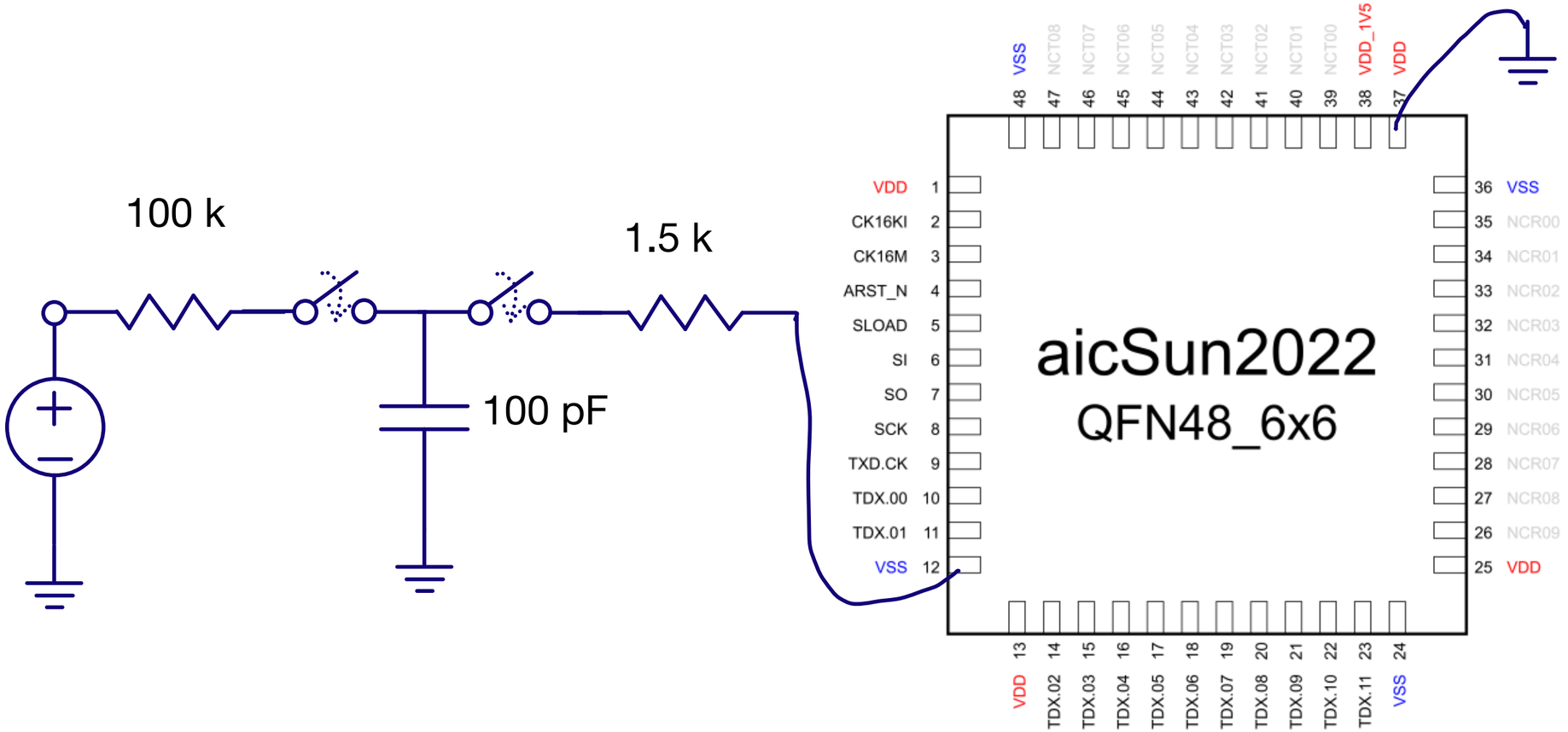
Long duration (around 100 ns)

Acts like a current source into a pin

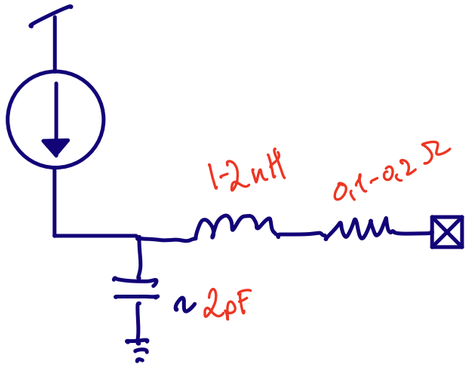
Can usually be handled in the I/O ring

4 kV HBM ESD $\Rightarrow$ 2.67 A peak current

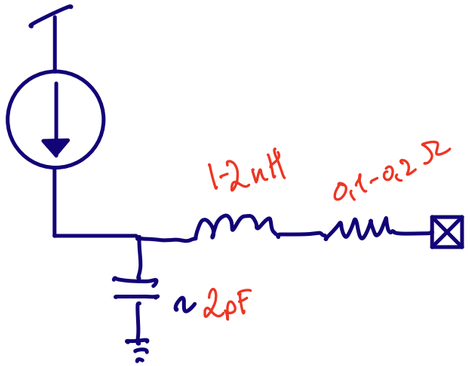



100 k
1.5 k
100 pF
aicSun2022
QFN48_6x6
VDD 1
CK16KI 2
CK16M 3
ARST_N 4
SLOAD 5
SI 6
SO 7
SCK 8
TXD.CK 9
TDX.00 10
TDX.01 11
VSS 12
48 VSS
47 NCT08
46 NCT07
45 NCT06
44 NCT05
43 NCT04
42 NCT03
41 NCT02
40 NCT01
39 NCT00
38 VDD_1V5
37 VDD
36 VSS
35 NCR00
34 NCR01
33 NCR02
32 NCR03
31 NCR04
30 NCR05
29 NCR06
28 NCR07
27 NCR08
26 NCR09
25 VDD
13 VDD
14 TDX.02
15 TDX.03
16 TDX.04
17 TDX.05
18 TDX.06
19 TDX.07
20 TDX.08
21 TDX.09
22 TDX.10
23 TDX.11
24 VSS

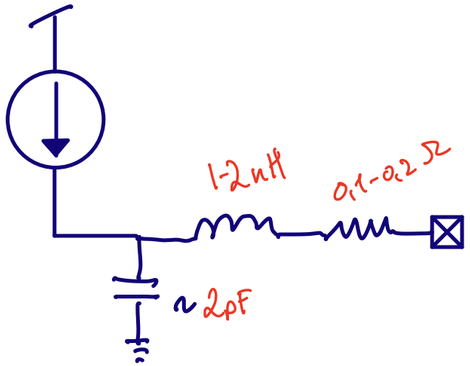
What could we do for VSS ⇒ VDD?



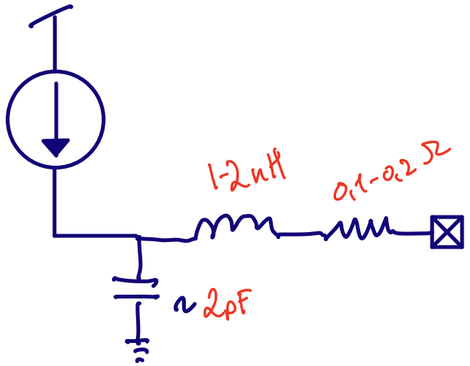
What could we do for VDD ⇒ VSS?

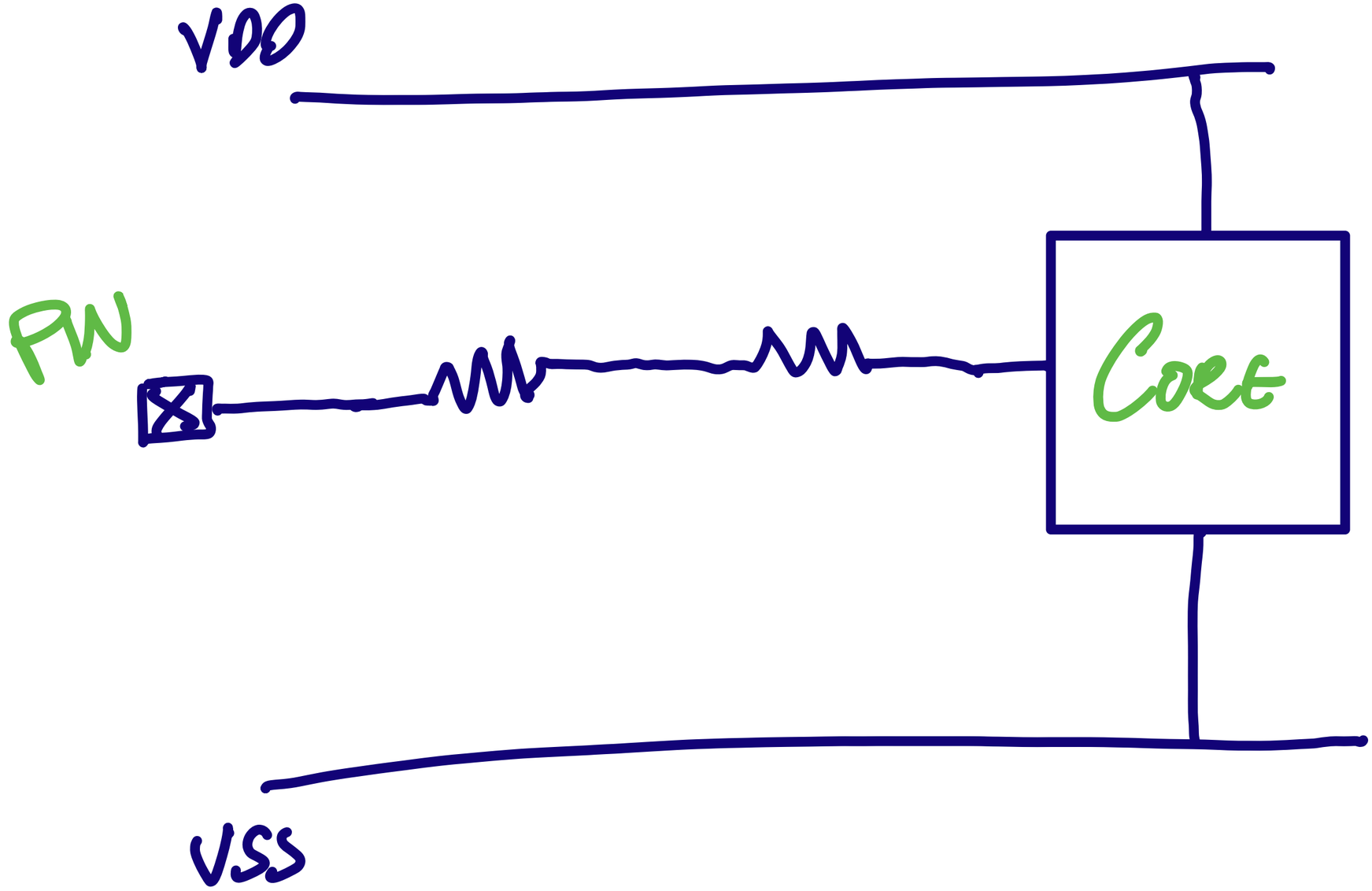


What could we do for PIN ⇒ VSS?

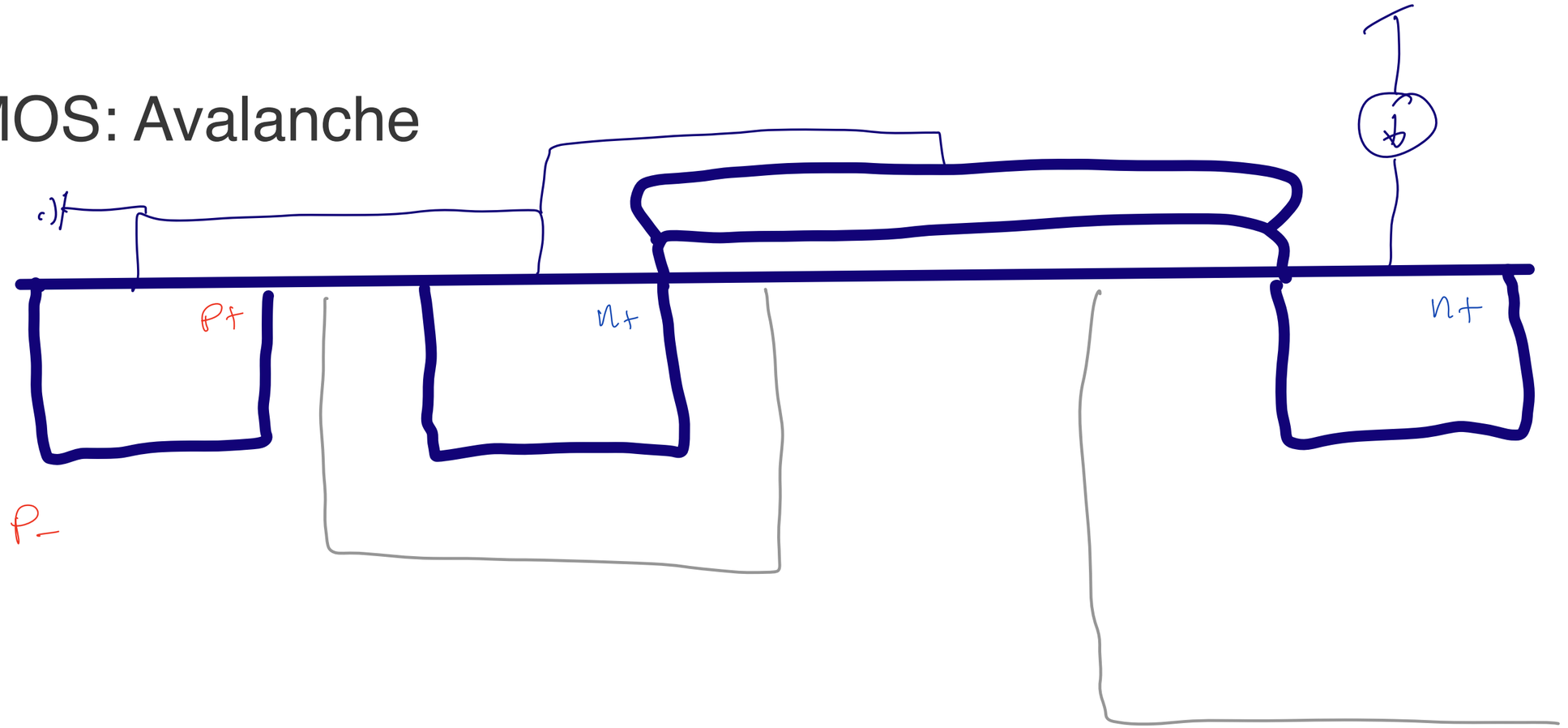


What could we do for VSS ⇒ PIN?



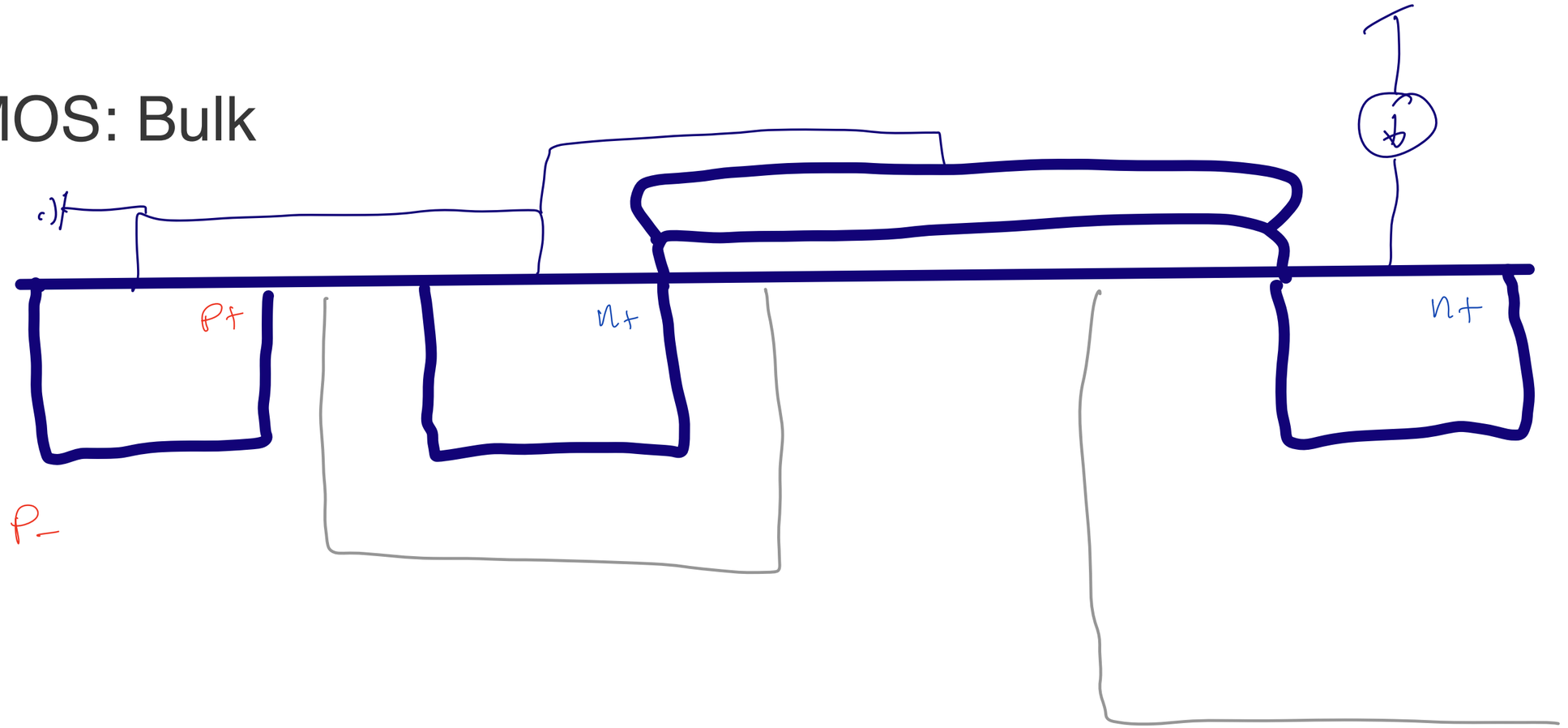

VDD
PW
Core
VSS

GGNMOS: Avalanche



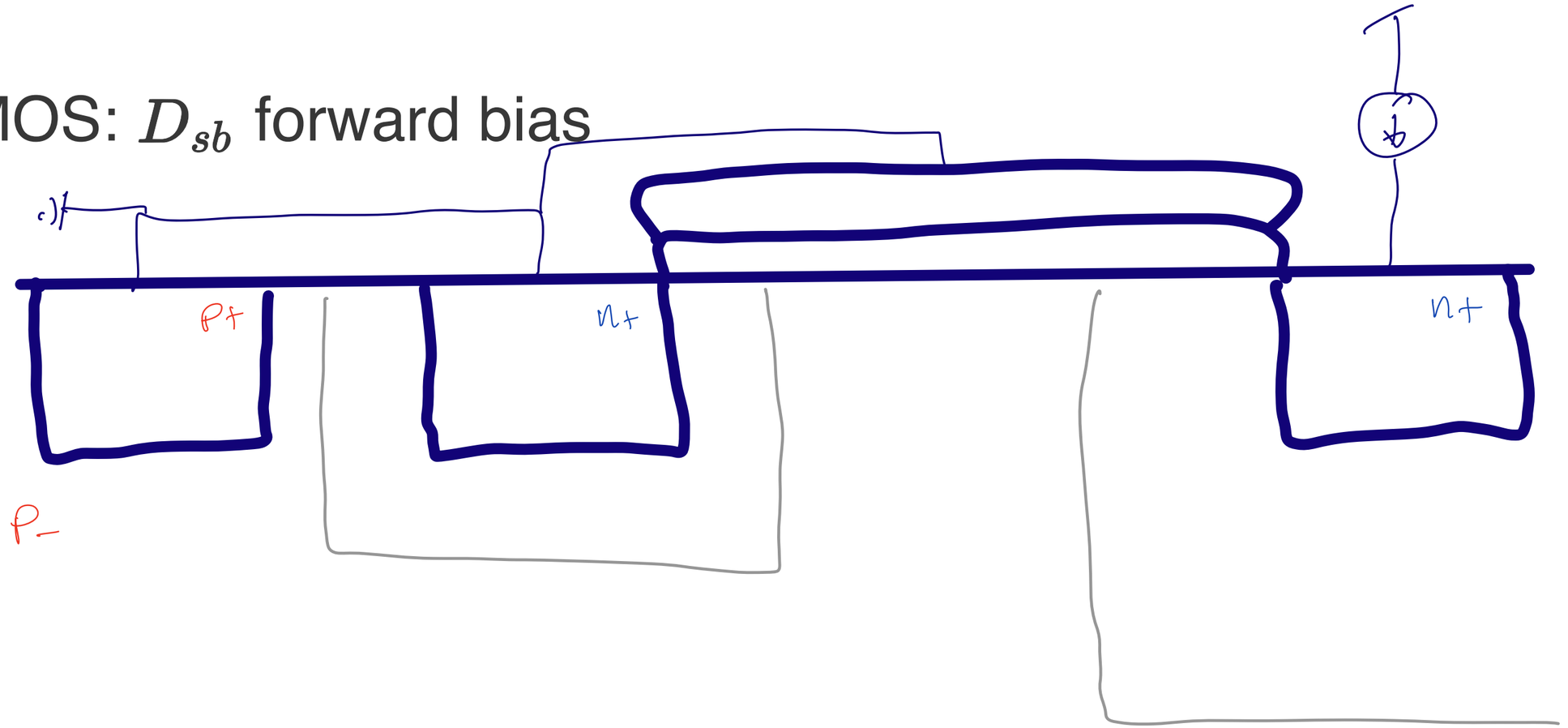
Not correct scale

GGNMOS: Bulk



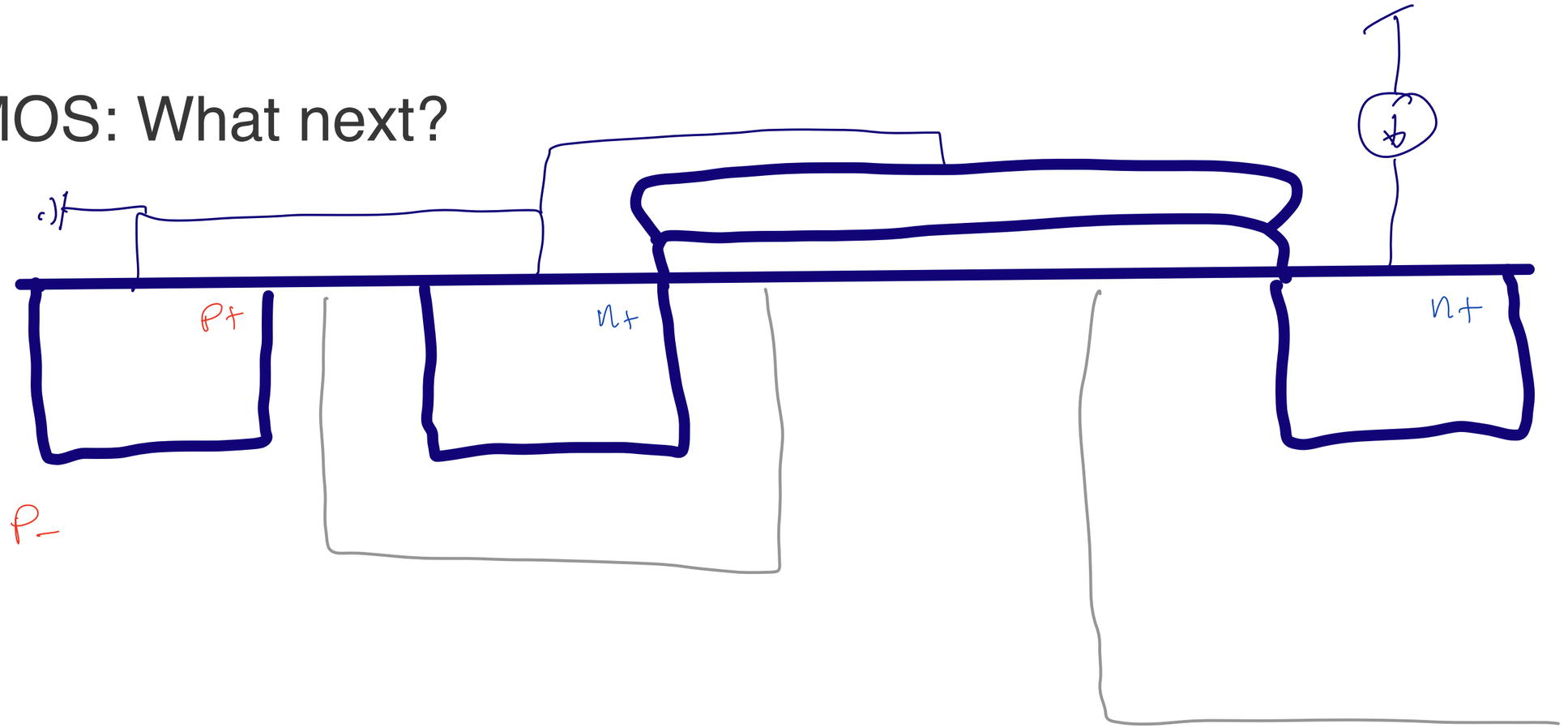
Not correct scale

GGNMOS: D_{sb} forward bias



not correct scale

GGNMOS: What next?



not correct scale

If you don't do the layout right[3]

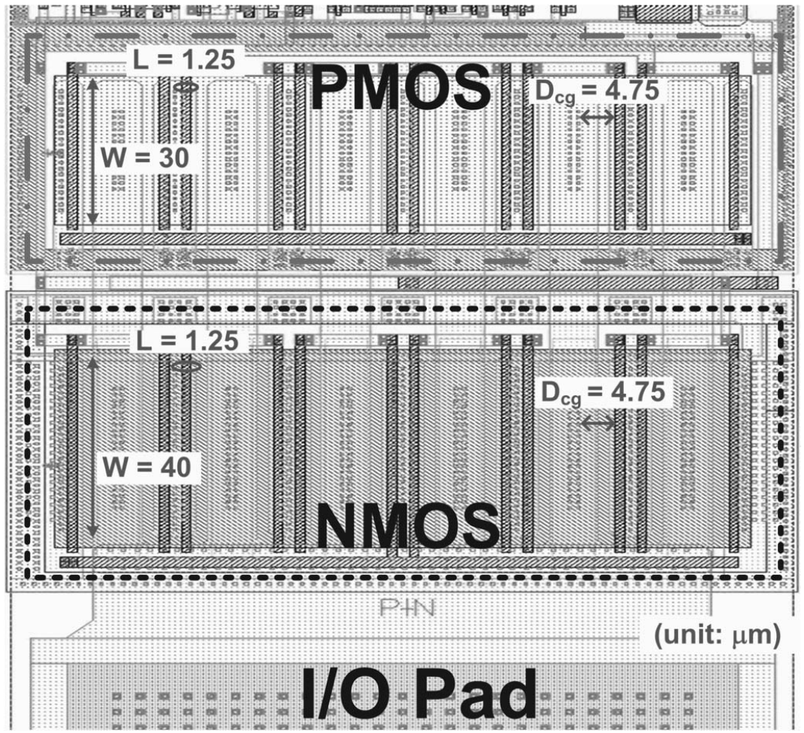


Fig. 5. Layout top view of the self-protecting fully silicided I/O buffer in a CMOS IC product.

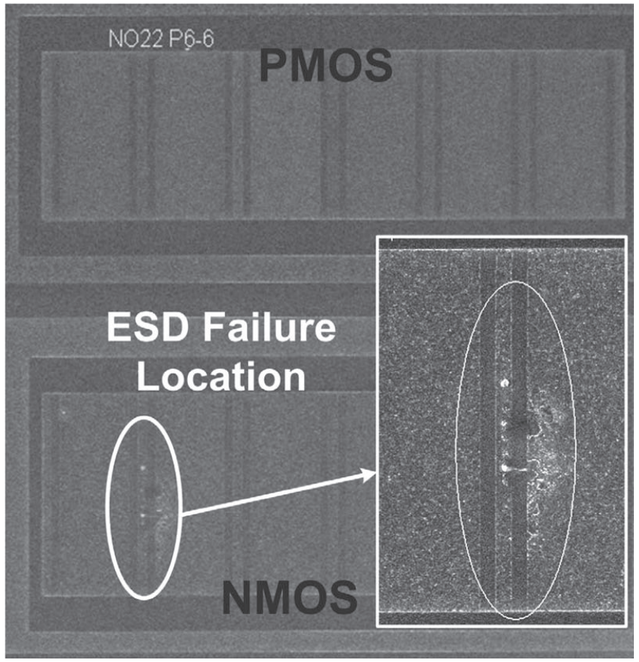


Fig. 6. SEM image of the fully silicided I/O buffer without ballasting after 2-kV PS-mode ESD stress. ESD failure is found on only one finger of the driver NMOS. Current filamentation is also observed on the surface of the driver NMOS without ballasting.

[3] New Ballasting Layout Schemes to Improve ESD Robustness of I/O Buffers in Fully Silicided CMOS Process

You must **always handle ESD** on an IC

- Do everything yourself
- Use libraries from foundry (gf013_esd)
- Get help www.sofics.com

Thanks!