```
{ "name": "IVX1_CV" ,
  "symbol" : "inv",
  "class" : "Layout::LayoutDigitalCell",
  "spice" : [
      ".subckt IVX1_CV A Y AVDD AVSS" ,
      "MN0 Y A AVSS AVSS NCHDL",
      "MP0 Y A AVDD AVSS PCHDL",
      ".ends IVX1_CV”],
  "addSchematicCoordinates" : {
      "MN0" : [ 0.25, 0, "R0"],
      "MP0" : [0.25, 0.5, "R0”]
  },
  "beforeRoute" : {
      "addDirectedRoutes" : [ ["M1","Y","MN:D-|--MP:D"], ["PO","A","MN:G-MP:G"] ]
  },
  "afterRoute"  : {
      "addPortOnRects" : [  ["A","M1", "MN0:G"] , ["Y", "M1", "MN0:D"]]
  }
}
```

What symbol to use, defaults to templates/skill/<name>.il

LayoutDigitalCell has extra functions for digital cells, and will add power rails.

Connectivity defined by SPICE. SPICE subcircuit can be read from a separate file

Help the schematic generator to place transistors so it’s easier to read schematics

Find rectangle on device MN:D, and route in M1 to rectangle MP:D using a left, up or down, left pattern.

Add port for A on the gate of MN0