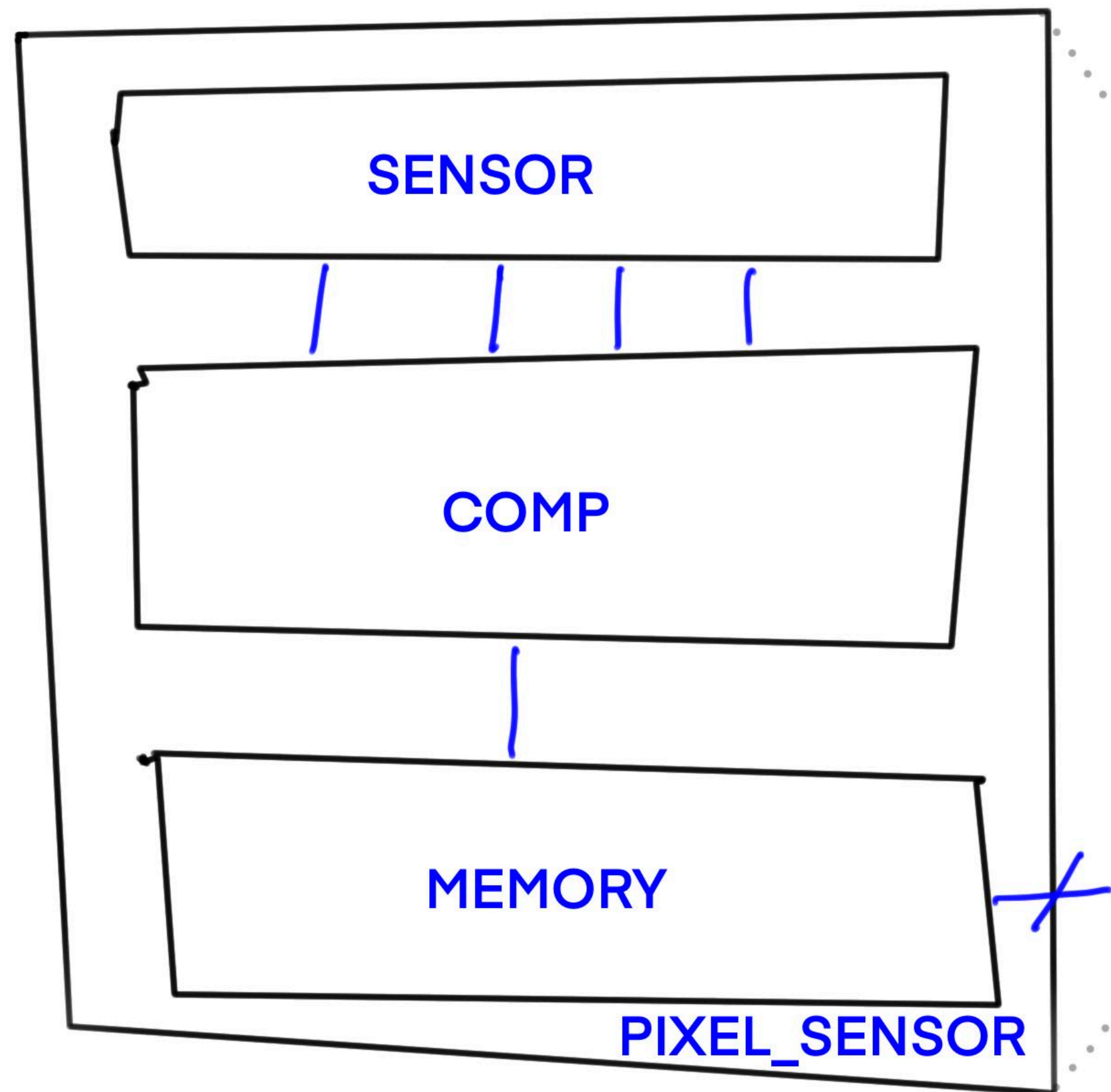


## Spice



## SystemVerilog

