工装平台模拟模块 AD7190 寄存器配置&上位机公式集合　2017/3/22

本文档仅提供和硬件相关的配置资料。

一.寄存器配置，其中硬件需求见以下列举，以官方规格书为准，其他默认或依软件要求来配置。

1.规格书第 21 页，MR19~18S=00。MR9~0 设频率最好在 50HZ 以下，保证精度，或由实验测定。

MR19 to MR18	CLK1 to CLK0	These bits are used to select the clock source for the AD7190. Either the on-chip 4.92 MHz clock or an external clock can be used. The ability to use an external clock allows several AD7190 devices to be synchronized. Also, 50 Hz/60 Hz rejection is improved when an accurate external clock drives the AD7190.

CLK1	CLK0	ADC Clock Source
0	0	External crystal used. The external crystal is connected from MCLK1 to MCLK2.
0	1	External clock used. The external clock is applied to the MCLK2 pin.
1	0	Internal 4.92 MHz clock. Pin MCLK2 is tristated.
1	1	Internal 4.92 MHz clock. The internal clock is available on MCLK2.

MR9 to MR0	FS9 to FS0	Filter output data rate select bits. The 10 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter, and the output data rate for the part. In association with the gain selection, it also determines the output noise (and, therefore, the effective resolution) of the device. When chop is disabled and continuous conversion mode is selected, the first notch of the filter occurs at a frequency determined by the relationship: *Filter First Notch Frequency* = (f_{MOD}/64)/*FS*

2.第 23 页，设 CON20=0；CON4=1（buffered mode）；CON3=0（双极）。

增益设三种：CON2TO0=000/011/100（增益 1/8/16）。

CON20	REFSEL	Reference select bits. The reference source for the ADC is selected using these bits.

REFSEL	Reference Voltage
0	External reference applied between REFIN1(+) and REFIN1(–).
1	External reference applied between the P1 and P0 pins.

CON4	BUF	Configures the ADC for a buffered or an unbuffered mode of operation. If cleared, the ADC operates in unbuffered mode, lowering the power consumption of the device. If set, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors

CON3	U/$\overline{B}$	Polarity select bit. When this bit is set, unipolar operation is selected. When this bit is cleared, bipolar operation is selected.
CON2 to CON0	G2 to G0	Gain select bits. Written by the user to select the ADC input range as follows:

G2	G1	G0	Gain	ADC Input Range (5 V Reference, Bipolar Mode)
0	0	0	1	±5 V
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	8	±625 mV
1	0	0	16	±312.5 mV
1	0	1	32	±156.2 mV
1	1	0	64	±78.125 mV
1	1	1	128	±39.06 mV

3.第 24 页，采样通道循环顺序：CHD=0100~0111，即 AIN1~AIN4 跟 AINCOM 的四个差分通道。

Table 20. Channel Selection

Channel Enable Bits in the Configuration Register										
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	Channel Enabled	Status Register Bits CHD[3:0]	Calibration Register Pair
							1	AIN1 to AIN2	0000	0
						1		AIN3 to AIN4	0001	1
					1			Temperature sensor	0010	None
				1				AIN2 to AIN2	0011	0
			1					AIN1 to AINCOM	0100	0
		1						AIN2 to AINCOM	0101	1
	1							AIN3 to AINCOM	0110	2
1								AIN4 to AINCOM	0111	3

二、上位机公式集合

AD7190 的数据格式见官方规格书第 33 页“DATA OUTPUT CODING”。原始值是无符号 24 位数字量，即 0~2^24。低误差＜±0.01%，低温漂＜±10PPM/度。用户可用标准件进行模拟量多点校验， 但无需再设置原始值校准，若偏差较大则人工换芯片。

转换速率依精度和工作效率折衷决定。

原始值数据流上传上位机，或者在 CPU 处理滤波上传，当前需要应用层公式如下（后续需求将陆续补充）：

设 CHD=0100 得原始值为 D1、CHD=0101 得 D2、CHD=0110 得 D3、CHD=0111 得 D4。

对应转成电压值 V1 / V2 / V3 / V4。转换公式：V = (D - 2^23) * 4.096 / (G * 2 ^ 23)；小数位尽量保留多。

其中 D 是 24 位原始值，G 是设置的增益值（CON2 TO CON0）。

实际应用：右扩展模块采集主板、整机工装；BD 模块校准工装；模拟量主机的整机校准工装。

1. PT100/PT1000/TCR 型信号回授电阻检测：连接介质存在阻抗，则实际基准值以 dRes 为准，单位 0.1 微伏。
   设 G=8； dRes = V3 * RF / (V2 － V1)；其中 RF 是当前切换的基准阻值（上位机可设，1 毫欧单位）。

2. TCV 型信号回授电压检测，实际基准值以 dVes 为准，单位 0.1 微伏：**设 G=16，dVes = V4 * 10 ^ 7。**

3. NTC 型信号回授检测：原理同第一点，实际基准值以 dRes 为准。设 G=1；

dRes (单位 10 毫欧)= V3 * RF / (V2 － V1)；其中 RF 是当前切换的基准电阻值（上位机可设，10 毫欧单位）。